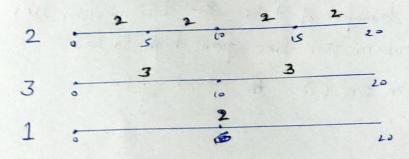
Name: Abhishek Srivastava. Rg No: 19 BCE 10071 Subject: Embedded System Date . May 16, 2022. Team End Examination. 1](6) registration number = 071 Delay = 071 (de # include regs 1-h> sbit mybit = P274; void MsDelay (unsigned int itime) unsigned int i,j; foo(int i=0; i < itime; L++) for (int j = 0; j<1000; j++); void main () while (1) mybit = ~ mybit;
MsDelay (071);

21(a) Generating UART communication packet Given hexadedicimal data = 45h Hence Equivalent birary = 01000101 Start bit Data frame Pasilybit Stapbit (1861) (6-9 data bit) (oto 1) To etast the toursfor of data, the transmission UART pulls the transmission line from high to Low from one (1) to clock cycle. Data forme 01000101 One data forme is HS 6it LS bit Data frame is sent with the Least Significant bit (LSB). Posity. Parity docribes the eveness or address of a . If the parity bit is a o/even parity, then I are Logic high bit in the data frame should total to an even number. number. . It the parity bit is 1 (odd), the 1 bit or Logic high in the data frame should total to an old number

It is highest for the process which has least dunning time posiod. Thus & has highest priority then 3 and lastly 1.

.: 2 > 3 > 1

Representation and Flow



Thus, process 2 executes aftimes for every 5 time units, process 3 executes 3 times for every 10 time units, and process 1 executes a times for every.

22331221112233522

3 (6)

Rate Monothic Schoduling.

Release time for all tasks = Os

Time Poid. Process. Execution Jime

 $n(2^{1/2}-1)=3(2^{1/2}-1)=0.7977$ $u = \frac{2}{20} + \frac{3}{5} + \frac{2}{10} = 0.9$

.: the combined utilization of 3 process is less than the threshold of those processes that means the above set of processes once scheduled and thus satisfy the Equation of the algorithm.

Scheduling time.

We calculate the LCM of time pooled of all process.

LCM (20,5,10), i.e, 20

Thus we can schedule so time units.

. When the parity bit matches the data, the UART knows that the transmission was fee e coops.

Therefore,

number Total no. of 1's = 3 and 3 is an ODP

in pasity bit = 1

Stop bit

To Signal the end of the data packet, the sending WART drives the data to ansmission line from the Low voltage to a high voltage of of (1) to (2) bit of duration.

It is the last bit of the packet and it indicates the end of the packet.

Timing Diagram

Parity bit Mark J Storte bit Clack 1010001011 8-databit Least Significant bitfirst.

```
Hinclude (regsI-h)
 Shit READ_ADC = PO^O
 Shit WRITE - ADC = POTI;
SLIE INTR-ADC POM2
char tempo [] = "0000"; unsigned char AD C-value;
int c;
not.
void delay-me (unsigned int time)
     int i,i
   for (i = 0; i < time; j+4)
void main ()
      Po = 0x00;
      P( = 0x00;
      P2 = 0 x 00.
      P3 = 0 x 04.
      IE = OX41;
     ITO = 2;
```

J.

Void ERE Void IBR - ex (void) PI = OXFF INTR-ADC = 1; READ - ADC = 1 WRITE-ADC =1. while (1) WRITE-ADC = 0 delayors (1); WRITE-ADC=1 while (INTR-ADC== 1); READ-ADC= 0 ADC_value = P3; C = ADC value * 1.95, if (c >99) temp > [0]=1+48; de l'empo [0]: tempo [i] =(C/10)/. 10 + 48; temps [2] = C7.10+ w; tempo [5] = 223. delay-me (10) READ-ADC= 3; 3 delay-me = 1000.



Here I am using externed entering in which I a am taking input of tempera ture from sunsor and converting it to to . " Cusing MODERADC.

PTO

