Embedded System Tutorial 2,3

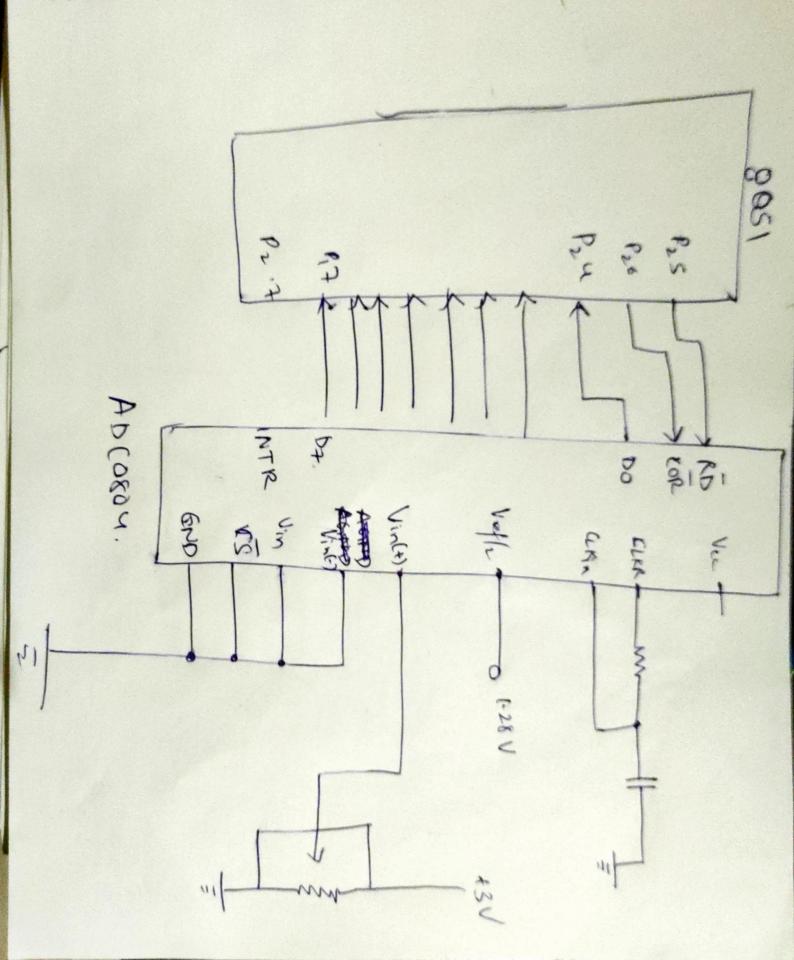
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Question-1

ADC -0804

the ADCO800 series from \$\frac{1}{2} \text{Vin(-)} \\ \text{National Semiconductor.} \\ \text{National National Semiconductor.} \\ National Nati	·The ADC-0804 IC is an 8-bit	200	00 17
National Semiconductor. National Semiconductor. 9 wod 12 13 14 15 15 16 16 16 16 16 16 16 16	I II A IX IN THE TOUR TO	(VinC+)	01 16
National Semiconducions 9 wood 12 ps 13 1 sorks with +5 v and has 12 ckr resolution of 8 bits 12 ckr The conversion time varies 2 ckr depending on the clacking 1 des signals applied to th CLK IN pin, 10 pgrb	II III AXIII APPRES	Vin(-)	01 15
National Semiconducions 9 wood 12 ps 13 1 sorks with +5 v and has 12 ckr resolution of 8 bits 12 ckr The conversion time varies 2 ckr depending on the clacking 1 des signals applied to th CLK IN pin, 10 pgrb	the ADCUGUO ACC	AGNO	03 14
resolution of 8 bits. The conversion time varies depending on the clacking ± 168 WR 3 signals applied to the CLK IN pin, 10 DGND	Mational Jemiconaucius	(mc) (2	05 13
resolution of 8 bild The conversion time varies depending on the clacking ± 668 signals applied to the CLK IN pin, 10 DGND	· 9 works with +5V and has	1 2 2	
The conversion time voices depending on the clacking to the Signals applied to the CLK IN pin, to parts	The life of X Dills		- 11
the conversion the clacking 1 dos wr 3 signals applied to the CLK IN 20 RD INTROS pin, 10 DGND	Was Magiles	CLKIN	
signals applied to the CLK IN 20 RD INTROS pin, 10 DGHD	· The conversion time vacabing to	168	
	depending on the country	10.5	WR 0 3
	signals explied to the LLN IN	RD	TNIROS
	Light of the state	2 40	AUT HUY
	pin,	DUIT	4

· But it cannot be fister than



St is an active low input used to activate the ADCOSOU

- · Sinput Signal in active Low . When CS=0, if a high-to-low pulse is applied to the RD bin.
- · The RD pin also reffered as Output Enable (OE.

WR-Waite-Start of Convenation.

- this is active low input, used to inform ADCO804 to start conversa process.
- 84 CS=0 when WR make a high-low-high

CLK IN and CLK R

- · CLK IN is an input pin connected to an external clock source.
- · To use internal clock generator, the CLKIN and CLK R are connected to the capacitor and a sesister.
 - · f = 1.1 RC.

* INTR - Interoupt - End on Conversation · This is an ofp bin and is in active low.

· After JNTR goes low, we make CSZO VIn (+) and VIn (-) · These are differential analog inputs.
· Vin = & vin (+) + vin (-) VCC · This is +5v power supply. est is an input voltaged used for reference · If this pin is open, the analog input voltage for the ADC0804 is in the sange of oto 5V. · These are digital data out the since ADC 0804 & parallel ADC orip DO-D7 Dont = Vin Step Size.

A Ground, D Ground There are it pins possibling the ground for both the analog signals and the lighted signals we have two grounded pins in order to isolate the analog Vin signal. Question 2 24th Internal Register. For reading MISO 42n data.