Cache hierarchy exploration with PIN: L3 replacement policies

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April 15, 2016

1 Cache Simulator Description

This project contains the source code for LRU cache simulator. The cache follows a 3-level heirarchy. The L1 cache is 32KB, 8 way and follows LRU replacement scheme. The L2 cache is 256KB, 8 way and also follows LRU replacement scheme. The L3 cache is 2MB, 16 way and follows LRU replacemement scheme. The block size, 64 Bytes, is consistent throughout. The hierarchy is inclusive.

2 Scheme of the experiments

The simulator is made to run on memory traces collected from a subset of SPEC 2006 benchmarks. The performance is evaluated on the basis of L3 MPKI.

3 Results

Benchmark	LRU (L3 MPKI)
bzip	12.9763
gcc	2.35393
hmmer	9.45461
mcf	39.4382
perlbench	0.220017
xalanbmk	44.3048