

## Abhimanyu Yadav <abhiy.iitk@gmail.com>

## **Project Proposal**

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Tue, Mar 15, 2016 at 8:01 AM

Hi Abhimanyu,

The project proposal is fine. Couple of things to keep in mind:

- 1. I will expect to see an evaluation (in terms of L3 MPKI) in a three-level cache hierarchy. Assume that L1 instruction cache is 32 KB 8-way, L1 data cache is 32 KB 8-way, L2 cache is 256 KB 8-way, and L3 cache is 2 MB 16-way. Assume that all levels use 64-byte blocks. Also, you can assume LRU replacement in L1 and L2 caches and experiment with L3 cache replacement policy and index functions.
- 2. In the report, just documenting the results will not earn you much score. I will expect an insightful analysis and explanation of the results.

Best regards Mainak [Quoted text hidden]