Introduction to DMA

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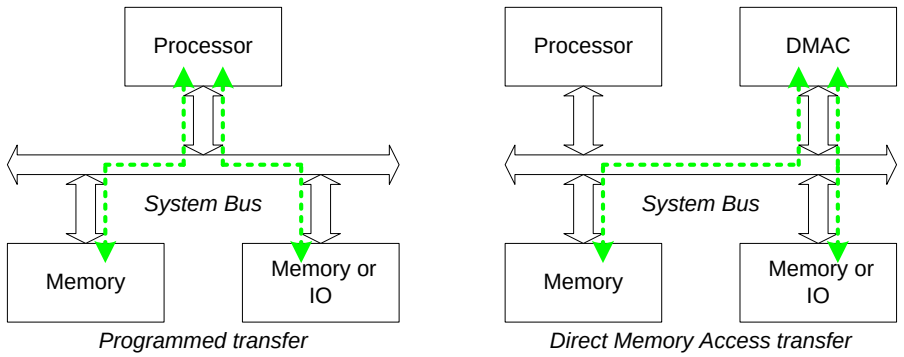
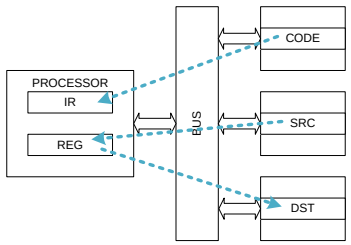
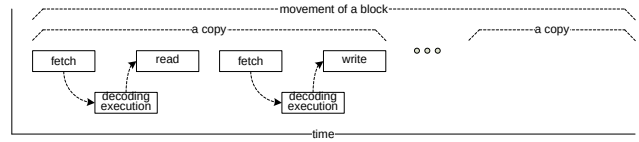
Data transfer



Transferring a block of memory

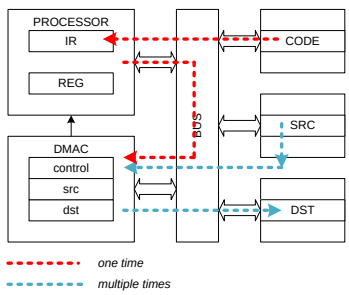
- Copying or moving a block of memory contents takes time since the processor needs to do followings
  - fetch instructions
  - decode/execute the instructions
  - read memories or registers
  - write memories or registers
- Potential problems
  - the processor wastes time to copy/move a block of memory
    - → performance degradation
  - the processor cannot do burst transfer
    - → low efficiency

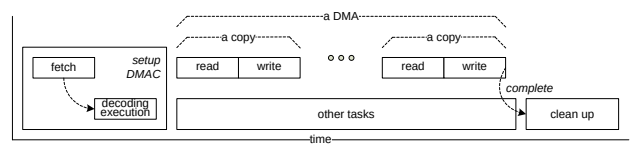




What is DMA and DMAC

- A direct memory access (DMA) is an operation in which data is copied (transported) from one resource to another resource in a computer system without the involvement of the processor.
- The task of a DMA-controller (DMAC) is to execute the copy operations of data from one resource location to another.
  - The copy of data can be performed from:
    - I/O-device to memory
    - memory to I/O-device
    - memory to memory
    - I/O-device to I/O-device

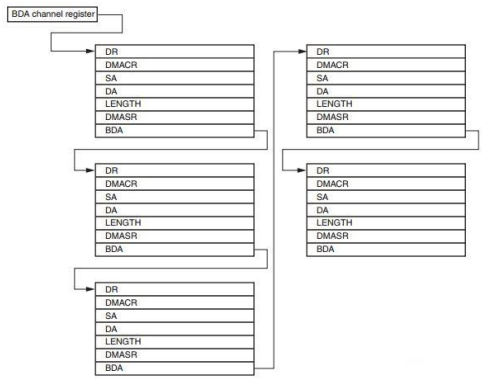




Features DMAC needs to support

- Registers to hold DMA information
  - source address
  - destination address
  - length of block to move
  - and other
- Notification of completion
  - flag setting for poling and/or
  - interrupt
- Burst transfer in order to get a better performance
- Minimize interference to the system operation
- Do not occupy system resource for a long time
  - Burst-based arbitration
    - do not hold system bus for a whole DMA operation
- Multiple DMA with reasonable scheduling
  - Multi-channel DMA
- Load balance among DMA channels
  - Fairness among DMA channels, e.g., chunk based round-robin
    - chunk is a series of bursts
- Scatter-gather operation
  - source/destination may not be continuous space
    - Due to virtual address paging mechanism

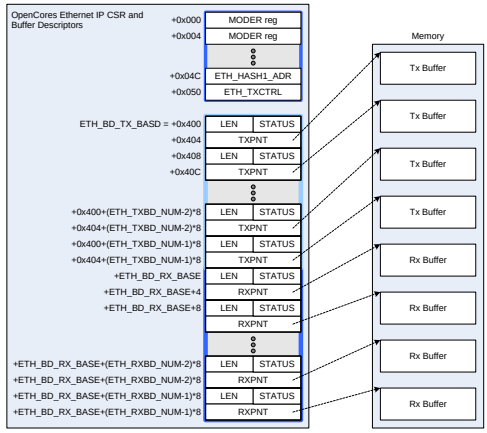
Linked-list buffer descriptor

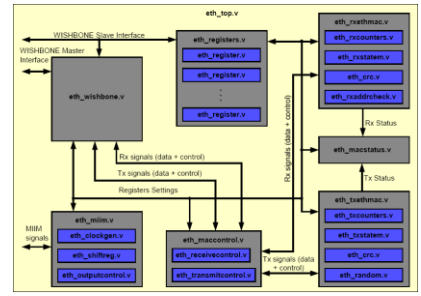


SR Packet Status Register
DMACR DMA Control Register
SA Source Address
DA Destination Address
LENGTH Length
DMASR DMA Status Register
BDA Buffer Descriptor Address (Link to next Buffer Descriptor)

DMAC embedded case

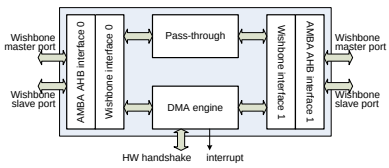
- OpenCores Ethernet MAC



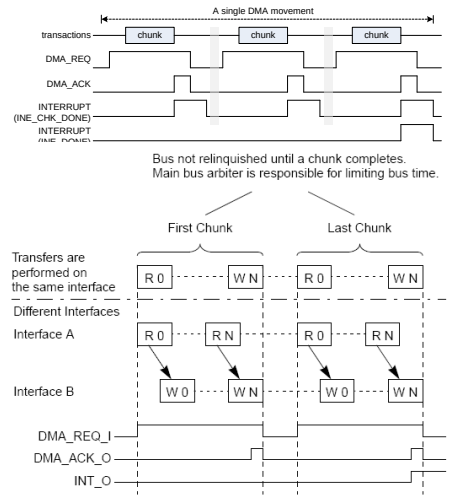


OpenCores DMAC

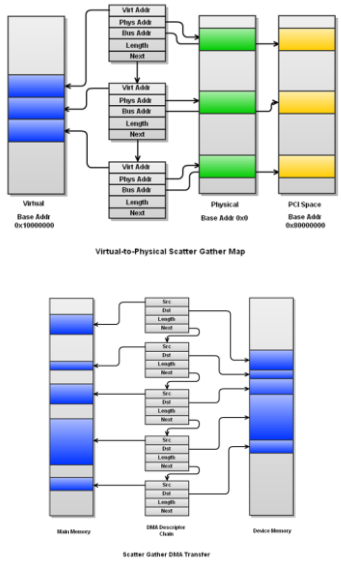
- Wishbone DMA/Bridge IP Core', Rudolf Usselman, www.opencores.org.
  - Up to 31 DMA Channels
  - 2, 4 or 8 priority levels
  - Linked List Descriptors Support
  - Circular Buffer Support
  - FIFO buffer support
  - Hardware handshake support
  - Interface
    - 2 Master interfaces
    - 2 Slave interfaces
  - Pass Through
    - act as bus bridge



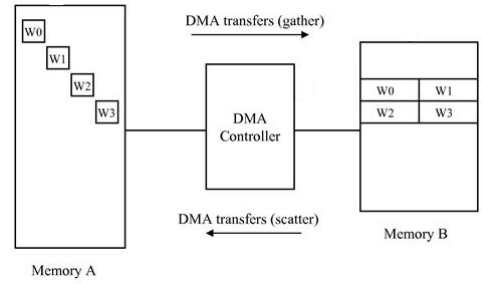
- A DMA consists of a series of chunk movement. Each chunk moves a number of data without yielding bus.



Scatter-gather



- Scatter-Gather DMA is data transfers from one non-contiguous block of memory to another by means of a series of smaller contiguous-block transfers.



Scatter-gather DMA