

# Engineering Program on RTL Design for FPGA Accelerator

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Ando Ki, Ph.D.

[adki@future-ds.com](mailto:adki@future-ds.com)

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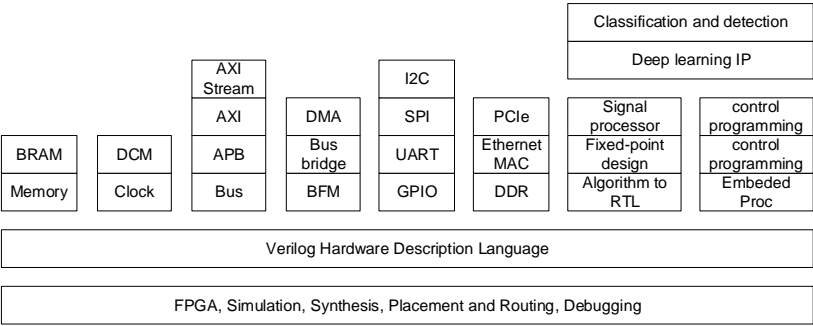
-- Contact information --  
Ando Ki, Ph.D.

[adki@future-ds.com](mailto:adki@future-ds.com)  
[www.Futue-DS.com](http://www.Futue-DS.com)

# Goals and objectives

- Understanding of RTL design flow
- Acquiring the working knowledge of RTL design
- Practicing development of RTL design using FPGA
- Understanding of Verilog HDL
- Understanding of FPGA
- Understanding of FPGA development environment
- Understanding of what can and cannot using FPGA

# Topics



# Lecture schedule

- Two or three hours per day
- Two or three days per week
- Thursday and Friday

# Coding guidelines

- Module name and file name should be the same
- Each directory should have directory clean-up script: Clean.bat, Clean.sh, Makefile
- Each HW IP would contain the following sub-directories

directory		remarks
bench	Test-bench	
	c/verilog/vhdl/systemc	Test-bench written in the specific language
beh	behavioral model if applicable	
	c/verilog/vhdl/systemc	behavioral model written in the specific language
doc	manual and other helpful document	
api	device driver if applicable and would contains the following sub-directory	
(drv)	c	
rtl	RTL model if applicable and would contains sub-directory like 'beh'	
(design)	verilog/vhdl/systemc/c	RTL model written in the specific language
sim	simulation related if applicable	
	modelsim/vcs/ncsim	Sub-directories for HDL simulator
syn	synthesis related if applicable	
	xst/synp/dc/fc/vivado	Sub-directories for logic synthesizer

(주)퓨처디자인시스템

34051 대전광역시 유성구 문지로 193, KAIST 문지캠퍼스, F723호  
(042) 864-0211~0212 / [contact@future-ds.com](mailto:contact@future-ds.com) / [www.future-ds.com](http://www.future-ds.com)

Future Design Systems, Inc.

Faculty Wing F723, KAIST Munji Campus, 193 Munji-ro, Yuseong-gu, Daejeon 34051, Korea  
+82-042-864-0211~0212 / [contact@future-ds.com](mailto:contact@future-ds.com) / [www.future-ds.com](http://www.future-ds.com)



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