Figure 1. System architecture (low-, medium-, XL-density devices) Flash FLITF DCode Cortex-M3 System **SRAM** Bus matrix DMA<sub>1</sub> DMA1 **FSMC** SDIO Ch.1 Bridge 2 Ch.2 APB1 Bridge 1 J APB2 Reset & clock Ch.7 control (RCC) ADC1 ADC2 ADC3 USART1 SPI1 **GPIOC** DAC SPI3/I2S SPI2/I2S GPIOD PWR DMA Request **GPIOE** BKP IWDG **GPIOF** bxCAN WWDG GPIOG EXTI AFIO USB TIM1 12C2 12C1 TIM7 DMA2 TIM8 TIM6 GPIOA GPIOB UART5 TIM5 UART4 USART3 USART2 TIM4 TIM3 TIM2 Ch.1 Ch.2 Ch.5 DMA request

Table 20. Port bit configuration table

ai14800c

Configuration mode		CNF1	CNF0	MODE1	MODE0	PxODR register	
General purpose	Push-pull	0	0	0	1	0 or 1	
output	Open-drain		1	1	0 or 1		
Alternate Function	Push-pull	1	0	1	Don't care		
output	Open-drain	'	1	see Ta	Don't care		
	Analog		0		Don't care		
Input	Input floating	0	1	00		Don't care	
Imput	Input pull-down	1	0		0		
	Input pull-up	1	J		1		

**Table 21. Output MODE bits** 

MODE[1:0]	Meaning
00	Reserved
01	Maximum output speed 10 MHz
10	Maximum output speed 2 MHz
11	Maximum output speed 50 MHz

## 9.2.1 Port configuration register low (GPIOx\_CRL) (x=A..G)

Address offset: 0x00 Reset value: 0x4444 4444

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNF	7[1:0]	MODE	7[1:0]	CNF	6[1:0]	MODE	E6[1:0]	CNF	5[1:0]	MODE	E5[1:0]	CNF	4[1:0]	MODE	E4[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNF	3[1:0]	MODE	3[1:0]	CNF	2[1:0]	MODE	E2[1:0]	CNF	1[1:0]	MODE	E1[1:0]	CNF	0[1:0]	MODE0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## 9.2.2 Port configuration register high (GPIOx\_CRH) (x=A..G)

Address offset: 0x04

Reset value: 0x4444 4444

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNF	15[1:0]	MODE	15[1:0]	CNF1	4[1:0]	MODE	14[1:0]	CNF1	3[1:0]	MODE	13[1:0]	CNF1	2[1:0]	MODE	12[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNF	11[1:0]	MODE	11[1:0]	CNF1	0[1:0]	MODE	10[1:0]	CNF	9[1:0]	MODE	E9[1:0]	CNF	3[1:0]	MODE	E8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

## 9.2.3 Port input data register (GPIOx\_IDR) (x=A..G)

Address offset: 0x08h

Reset value: 0x0000 XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDR15	IDR14	IDR13	IDR12	IDR11	IDR10	IDR9	IDR8	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

## 9.2.4 Port output data register (GPIOx\_ODR) (x=A..G)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw