German University in Cairo
Faculty of Media Engineering and Technology
Dr. Mohamed Elmahdy

December 27, 2014

Bar Code

CSEN-605 Digital Systems Design

Final Exam

Instructions: Please Read Carefully Before Proceeding.

1. The allowed time for this exam is **3 hours** (180 minutes).
2. (non-programmable) calculators are allowed.
3. No books or other aids are permitted for this test.
4. This exam booklet contains 17 pages, including this one. Three extra sheets of scratch paper are attached and have to be kept attached. **Note that if one or more pages are missing, you will lose their points. Thus, you must check that your exam booklet is complete**.
5. Please write your solutions in the space provided. If you need more space, **please use the back of the sheet containing the problem or on the three extra sheets and make an arrow indicating that.**
6. When you are told that time is up, please stop working on the test.

All the best.

Please, do not write anything on this page.

Exercise	1	2	3	4	5	6	7	Total
Maximum Marks	12	10	12	12	12	10	10	74.5*
Earned Marks								

*3.5 marks are bonus

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Exercise 1: (12 marks)

Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, (repeat) 001,…
Hint: if the present state is 000, the next state will be *don't care (XXX)*

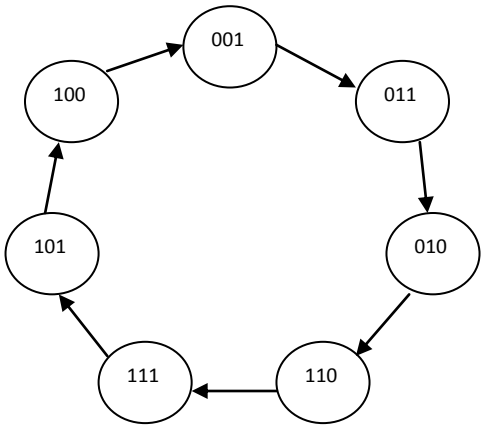
a. Design the counter using T flip-flops. Your design should include state diagram, state table, optimized state equations, and logic diagram. (11 marks)
b. What will happen if the counter is started in state 000? (1 mark bonus)

Hint: The characteristic table for T Flipflop is:

T	Q(t+1)
0	Q(t)
1	Q'(t)

Solution 1.a.

State diagram: (1 mark)



State table: (4 marks)

Present State			Next State			Flip-Flop Inputs		
C	B	A	C	B	A	T_C	T_B	T_A
0	0	0	X	X	X	X	X	X
0	0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	0	0	1
1	0	0	0	0	1	1	0	1
1	0	1	1	0	0	0	0	1
1	1	0	1	1	1	0	0	1
1	1	1	1	0	1	0	1	0

Flipflops input equations: (3 marks)

C \ BA	00	01	11	10
0	X	0	0	1
1	1	0	0	0

$T_C = C'A' + B'A'$

**Next state equations were accepted as well.

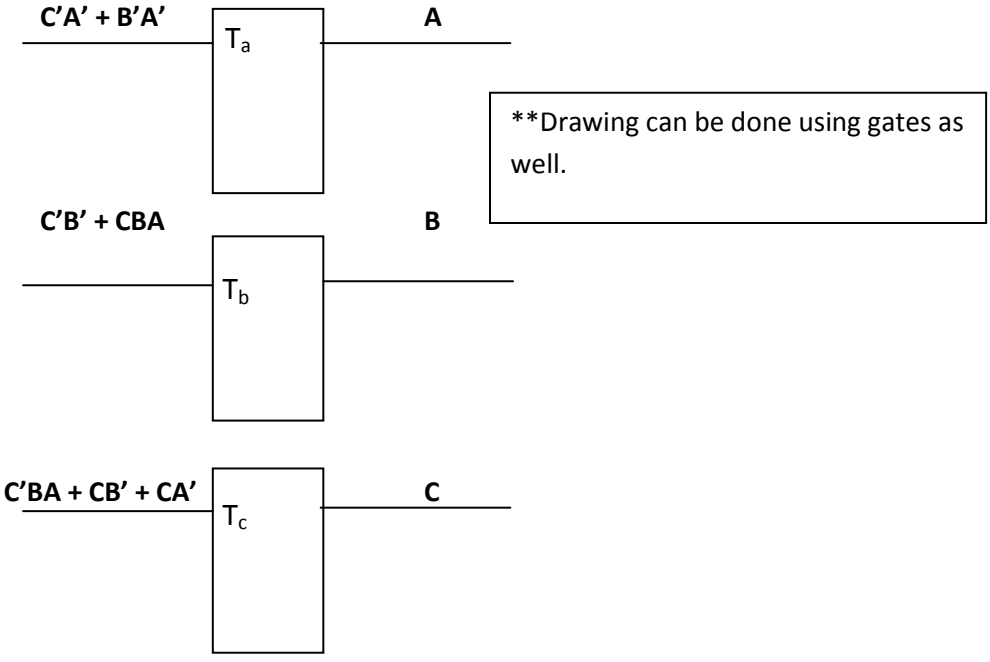
C \ BA	00	01	11	10
0	X	1	0	0
1	0	0	1	0

$T_B = C'B' + CBA$

C \ BA	00	01	11	10
0	X	0	1	0
1	1	1	0	1

$T_A = C'BA + CB' + CA'$

Logic Diagram: (3 marks)



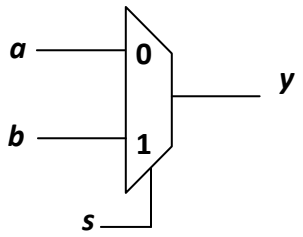
**Drawing can be done using gates as well.

Solution 1.b.

If the counter is started in state 000, next state will be 110 due to the optimization using the Kmaps.

Exercise 2: (10 marks)

For the 2x1 MUX shown below:



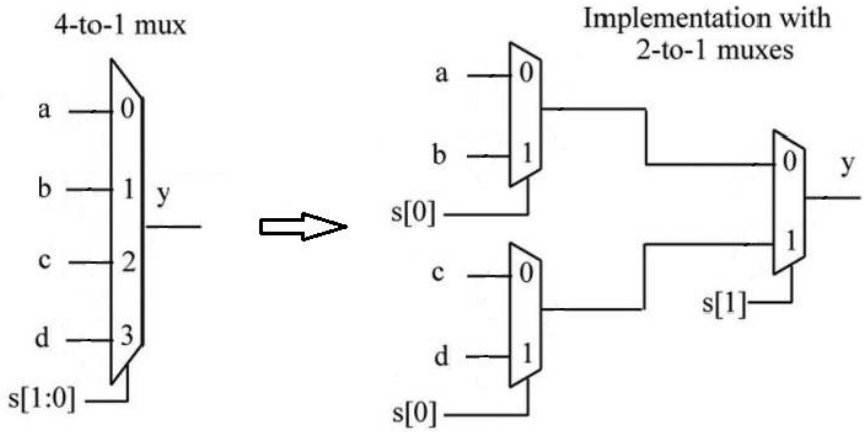
a) Implement a behavioral Verilog-HDL model of this 2x1 MUX. Name the module *mux_2_1.* (3 marks)

Solution 2.a.

```
module mux_2_1(y,a,b,s);
  input a,b,s;
  output y;
  always @(a or b or s)
    y = s ? b : a;
endmodule
```

b) Draw the modular block diagram that shows how to connect this 2x1 MUX to form a 4x1 MUX. (3.5 marks)

Solution 2.b.



c) Implement a Verilog-HDL model that describes the behavior of the modular design 4x1 MUX of your answer in part (b) by instantiating module *mux_2_1* ONLY (DO NOT use any other Verilog style or use any additional gates). Name the module *mux_4_1.* (3.5 marks)

Solution 2.c.

```
module mux_4_1(y,a,b,c,d,s);
  input a,b,c,d;
  input [1:0] s;
  wire w1, w2;
  output y;
  mux_2_1 aa(w1,a,b,s[0]);
  mux_2_1 bb(w2,c,d,s[0]);
  mux_2_1 cc(y,w1,w2,s[1]);
endmodule
```

Exercise 3 : (12 marks)

a) Compare between ASIC and FPGA designs in terms of unit cost, time-to-market, power, performance, and programmability? (2.5 marks)

Solution 3.a.

Feature	ASIC	FPGAs
Unit Cost	Low for high volume	moderate
TTM	Long	short
Power	Minimum	Not optimized
Performance	fastest	Not optimized
Programmability	No	Yes

b) Implement the following Boolean function using the CPLD shown below. On the diagram, show the programming of all switches and label all inputs and show the values of ***Sel*** and ***En*** on each macrocell. (9.5 marks)

$$f = AB + CD' + BC + AD'$$

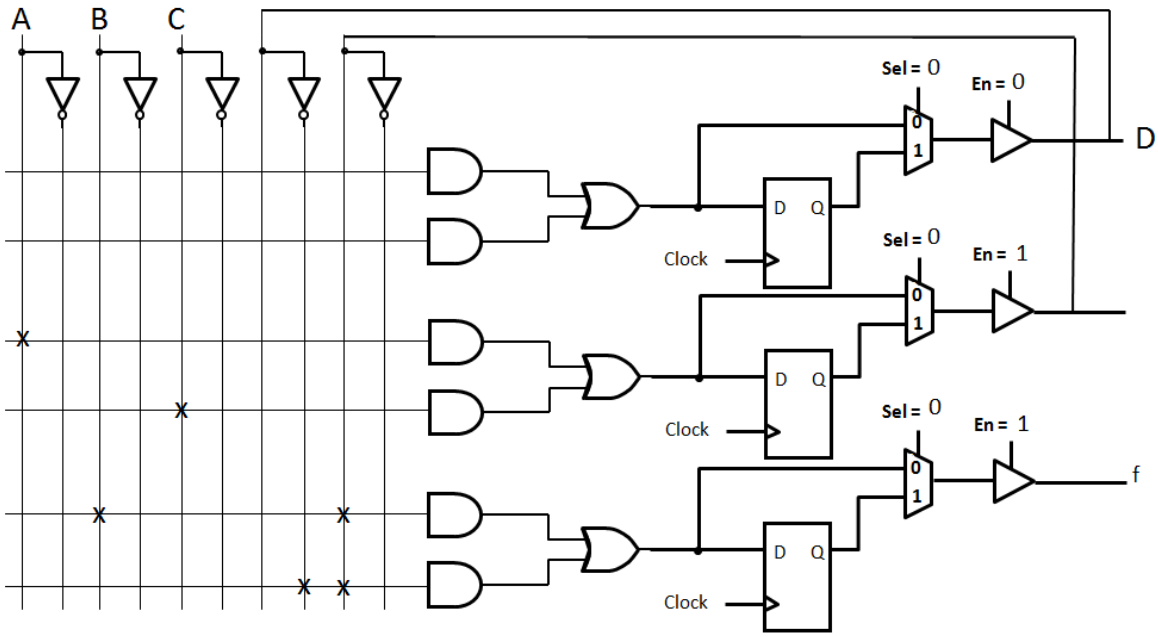
Solution 3.b.

Accepted simplifications:

f= B(A+C)+D'(A+C)

f= A(B+D')+ C(B+D')

f= (A'C' + B'D)'



Exercise 4: (12 marks)

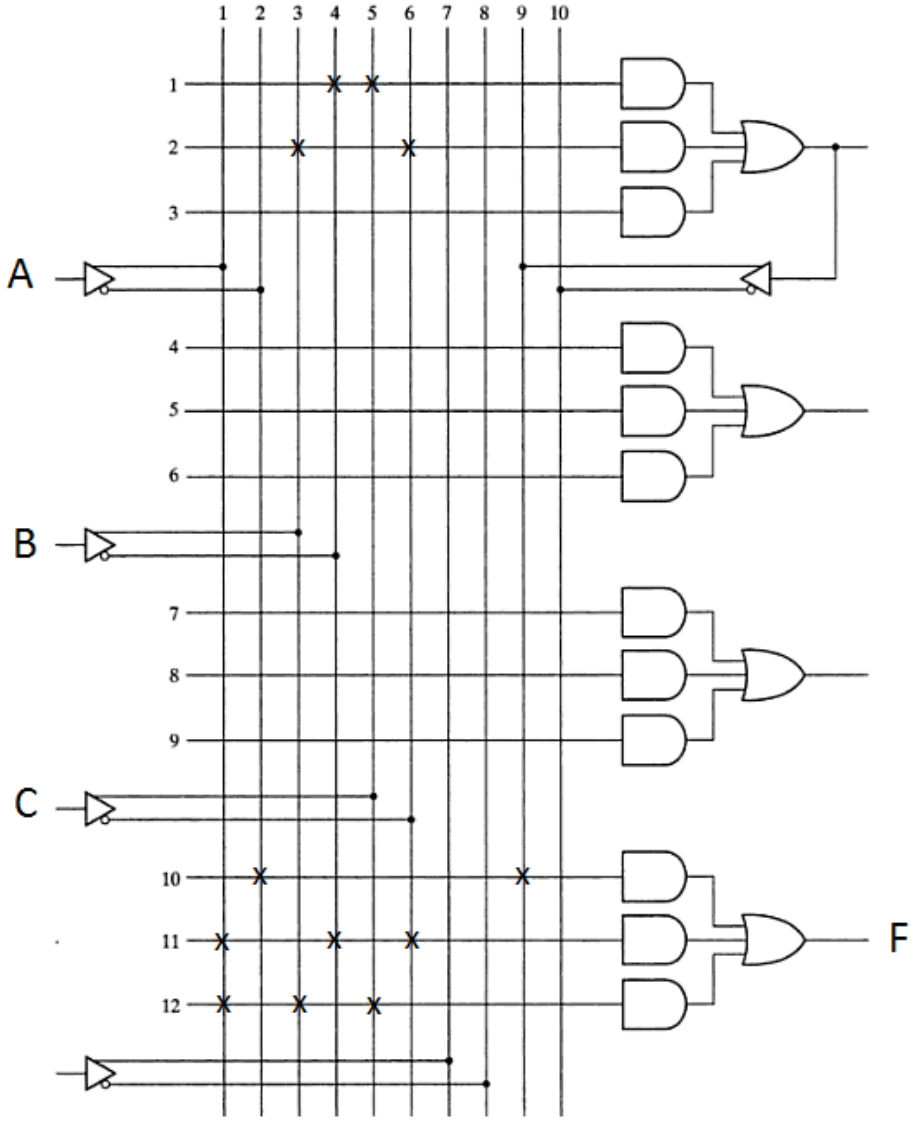
a) Implement the Function

$$F = A \oplus B \oplus C$$

Where $\oplus$ denotes XOR, using the PAL shown below. Show the programming of all switches. The inputs/outputs pins are pre-assigned as shown below. (10 marks)

Solution 4.a.

$$A \oplus B \oplus C = A'B'C + A'BC' + AB'C' + ABC$$
$$= A'(B'C + BC') + AB'C' + ABC$$



b) Compare between SRAM and DRAM in terms of number of transistors, storage mechanism, size, and cost? (2 marks)

Solution 4.b.

Feature	SRAM	DRAM
# of Transistors	large	low
Storage Mechanism	transistors	capacitance
Size	large	small
Cost	high	low

Question 5: (12 marks)

Design the control circuit of the sequential binary multiplier specified by the following state table using multiplexers, a decoder, and a register of D Flipflops (using the minimal number of Flipflops). You are also required to indicate whether the controls signals are Moore/Mealy and why?

Present State	Inputs			Next State	Control Signals				
	Start	Q[0]	Zero		Ready	Load_regs	Decr_P	Add_regs	Shift_regs
S_idle	0	X	X	*S_idle*	1	0	0	0	0
S_idle	1	X	X	*S_add*	1	1	0	0	0
S_add	X	0	X	*S_shift*	0	0	1	0	0
S_add	X	1	X	*S_shift*	0	0	1	1	0
S_shift	X	X	0	*S_add*	0	0	0	0	1
S_shift	X	X	1	*S_idle*	0	0	0	0	1

Solution 5:

Using binary state assignment, the minimum number of required flipflops is 2. (1.5 marks)

State codes:	G1	G0
S_idle	0	0
S_add	0	1
S_shift	1	0

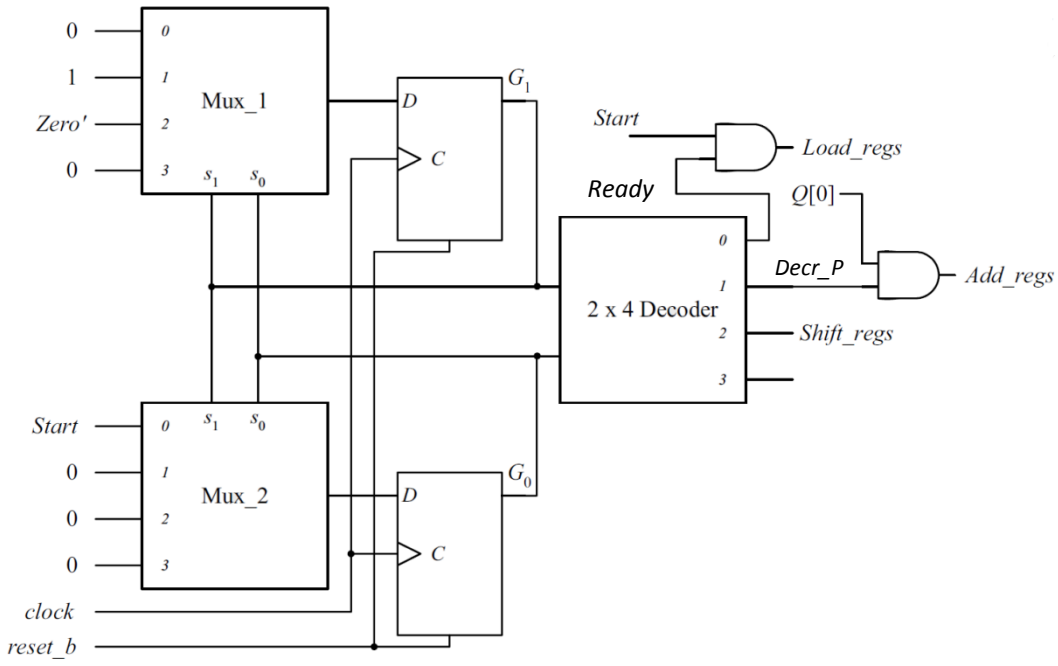
State Table:

Present State		Inputs			Next State		Control Signals				
G1	G0	Start	Q[0]	Zero	G1	G0	Ready	Load_regs	Decr_P	Add_regs	Shift_regs
0	0	0	X	X	0	0	1	0	0	0	0
0	0	1	X	X	0	1	1	1	0	0	0
0	1	X	0	X	1	0	0	0	1	0	0
0	1	X	1	X	1	0	0	0	1	1	0
1	0	X	X	0	0	1	0	0	0	0	1
1	0	X	X	1	0	0	0	0	0	0	1

MUX input conditions table: (4 marks)

Present State		Next State		Input conditions	Inputs	
G1	G0	G1	G0		MUX1	MUX2
0	0	0	0	Start'	0	Start
0	0	0	1	Start		
0	1	1	0	None	1	0
1	0	0	1	Zero'	0	Zero'
1	0	0	0	Zero		

Control Implementation: (4 marks)



Control Signals Type: (2.5 marks)

Ready, Decr_P and Shift_regs are moore since they depend on the present state only while Load_regs and Add_regs are mealy since they depend on the present state as well as the input.

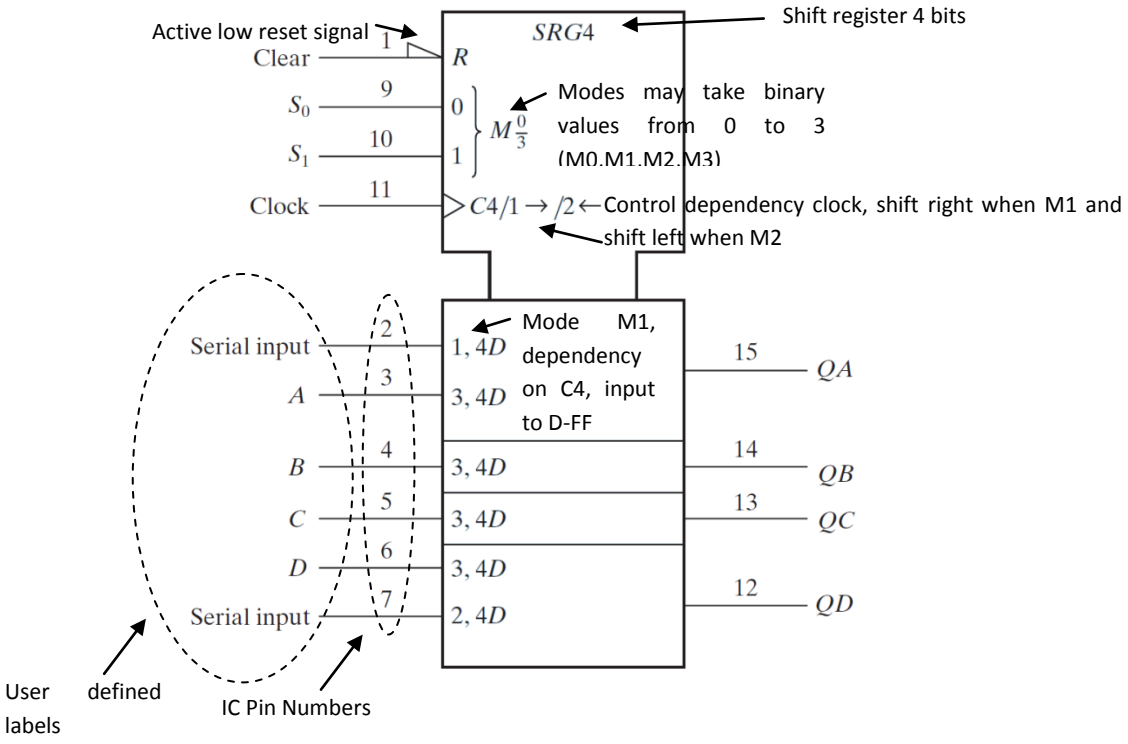
Question 6: (10 marks)

a) Briefly explain the function of the common control block when used with the standard graphic symbols.(1.5 marks)

Solution 6.a.

The inputs to a ***common control block*** control all lower sections of the diagram.

b) Explain all the symbols used in the standard graphic diagram of the following figure: (8.5 marks)



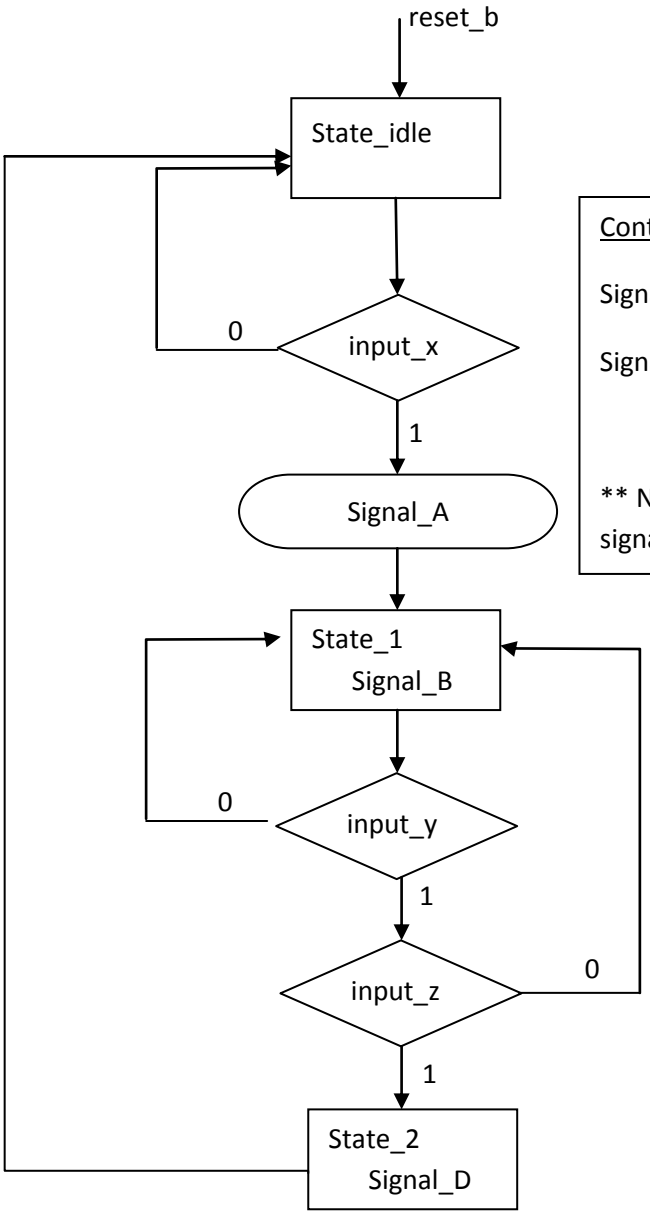
Exercise 7: (10 marks)

Draw the ASM chart that corresponds to the following controller HDL model. Show whether the control signals are Mealy/Moore and why?

```
module Controller_RTL (input_x, input_y, input_z, clock, reset_b);
  input input_x, input_y, input_z, clock, reset_b;
  reg [1: 0] state, next_state;

  parameter State_idle = 2'b00, State_1 = 2'b01, State_2 = 2'b10;

  always @ (posedge clock, negedge reset_b)
       if (reset_b == 0) state <= State_idle;
       else state <= next_state;

  always @ (state, input_x, input_y, input_z) begin
    next_state = S_idle;
    case (state)
     S_idle: if (input_x) next_state = State_1; else next_state = S_idle;
     State_1: if (input_y && input_z) next_state = State_2; else next_state = State_1;
     State_2: next_state = S_idle;
     default: next_state = S_idle;
    endcase
  end

  always @(state, input_x, input_y) begin
    Signal_A = 0;
    Signal_B = 0;
    Signal_C = 0;
    Signal_D = 0;
    case (state)
     S_idle: if (input_x) Signal_A = 1;
     State_1: begin Signal_B = 1; if (input_y) Signal_C = 0; end
     State_2: Signal_D = 1;
    endcase
  end
endmodule
```

Solution 7

ASM Chart: (9 marks)



Control Signals Type: (1 mark)

Signal_A is mealy.

Signal_B & Signal_D are moore.

** No penalization for including signal_C.

Extra sheet

Extra sheet

Extra sheet