COMPREHENSIVE SOLDER FATIGUE AND THERMAL CHARACTERIZATION OF A SILICON BASED MULTI-CHIP MODULE PACKAGE UTILIZING FINITE ELEMENT ANALYSIS METHODOLOGIES

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ABSTRACT

Viscoplastic finite-element simulation methodologies were utilized to predict ball and bump solder joint reliability for a silicon based five-chip multi-chip module package under accelerated temperature cycling conditions (0C to +100C, 5min ramp/5min dwell). The analyses utilized the ANSYS sub-modeling methodology by which global model simulation results were applied as boundary conditions in localized sub-models of the solder balls and bumps. Multiple ball and bump configurations consisting of both 63Sn/37Pb eutectic and 90Pb/10Sn high temperature solder materials were investigated. The solder structures accommodate the bulk of the plastic strain which is generated during accelerated temperature cycling due to the thermal expansion mismatch between the various stack-up materials in the silicon based package. Since plastic strain is a dominant parameter that influences low-cycle fatigue, it was used as a basis for evaluation of solder structural integrity.

The finite element analysis was extended to evaluate the steady-state thermal performance of the multi-chip module system. A full-symmetry, three-dimensional finite element model was required due to the non-symmetric nature of the five-chip multi-chip module package. The finite element analysis methodology utilized temperature dependent surface coefficients to account for the combined non-linear effects of natural convection and radiation heat transfer. Multiple analyses were executed in order to quantify the required case-to-ambient thermal resistance (θ_{ca}) necessary to properly cool the package with a heat sink or heat pipe apparatus.

The paper discusses the evaluation methodologies as implemented in the ANSYS finite element simulation software tool and the corresponding results for the solder bump/ball fatigue and steady-state thermal analyses. Some ANSYS parametric design language is included for the benefit of those readers who are familiar with the software tool.

Index Terms – microelectronic package characterization, solder fatigue analysis, viscoplastic strain energy density, thermal analysis, finite element modeling.

1. INTRODUCTION

The integrity of ball and bump solder joints is a major reliability concern in modern microelectronic packages. Temperature fluctuations caused by either power transients or environmental changes, along with the resulting thermal expansion mismatch between the various package materials, results in time and temperature dependent creep deformation of solder. This deformation accumulates with repeated cycling and ultimately causes solder joint cracking and interconnect failure. To minimize development costs and maximize reliability performance, advanced analysis is a necessity during the design and development phase of a microelectronic package. This requires the utilization of a life prediction methodology that is based on the damage mechanisms experienced in a field operation environment.

Several finite element based analysis methodologies have been proposed which predict solder joint fatigue life (e.g. Engelmaier [1]; Shine and Fox [2]; Wong et al [3]; Yamada [4]; Subrahmanyan et al. [5]; Dasgupta et al. [6]; Pao [7]; Clech et al. [8]; Syed [9]; Darveaux et al. [10]; and Darveaux [11]). Of all these methodologies, Darveaux's seems to be the most popular due to the ease in its implementation.

Darveaux's methodology links laboratory measurements of low-cycle fatigue crack initiation and crack growth rates to the inelastic work of the solder. It is a strain energy based approach, where the work term consists of time-dependent creep and time-independent plasticity. This inelastic behavior is captured in ANSYS using Anand's constituitive model [12]. The modeling methodology utilizes finite element analysis to calculate the viscoplastic strain energy density accumulated per cycle during thermal or power cycling. The strain energy density is then utilized with crack growth data to calculate the number of cycles to initiate a crack, and the number of cycles for the crack to propagate across a solder joint. The methodology has been previously presented in the successful analysis of various electronic assemblies. Amagai [13] generated lifetime predictions for a chip scale package on an organic printed circuit board. Fusaro and Darveaux [14] used the viscoplastic properties of eutectic solder to analyze the reliability of a copper baseplate attachment for a power module. Dougherty et al. [15] analyzed a micro-miniature electronic package. Recently, Johnson [16] utilized the methodology to predict board-level solder joint reliability of multiple ball grid array packages.

Unfortunately, there is a material limitation inherent to all of these methodologies since they assume the utilization of eutectic 63Sn/37Pb solder or some similar combination of solder materials (i.e. 62Sn/36Pb/2Ag). Life prediction methodologies for high temperature solder (90Pb/10Sn, 95Pb/5Sn, etc.) or future non-lead based interconnect materials, are almost non-existent due to their low volume use in today's microelectronics packaging industry. Therefore, for the sake of analytical uniformity, the average amount of viscoplastic strain energy density accumulated per thermal cycle for the interface elements which make up the +Z and -Z interconnect joints was instead used as a basis for the evaluation of the eutectic 63Sn/37Pb and high temperature 90Pb/10Sn solder materials investigated herein.

Thermal simulations of individual microelectronic packages using finite element or finite difference based software tools allow package designers to minimize prototype revisions and reduce overall turnaround time from design to production. For these reasons, the finite element analysis of the five-chip multi-chip module was extended to include a free-convection, steady-state thermal evaluation. Numerous studies investigating multi-chip module package thermal performance have been reported in the literature (e.g. Bar-Cohen [17]; Sullhan et al. [18]; Kromann [19]; Aghazadeh and Jain [20]; Stout [21]; Lall et al. [22]; Sofia [23]; Zahn [24-25]). In the case of the package evaluated for this study, two slightly different power configurations were evaluated in an attempt to determine the necessary cooling system (i.e. heat pipe, heat sink, etc.) for optimal operation in a laptop computer environment.

When performing package level thermal analysis using solid model finite element simulation tools, the convective surface loads which control the cooling of the electronics package are typically applied using heat transfer coefficients derived from suitable correlations. These correlations may assume convection from a flat plate situated either horizontally or vertically, and experiencing either laminar or turbulent flow across the surface. Furthermore, many of these correlations assume either a constant surface temperature (isothermal) or a constant surface heat flux (isoflux). Although computational fluid dynamics (CFD) codes are rapidly replacing the practice of estimating surface convection coefficients, the use of CFD models has been found to provide minimal improvement over solid model simulations when performing simple package level thermal analysis as discussed by Zahn et al. [26]. A study by Sarvar et al. [27] concluded that although it is not generally correct to assume a single convective heat transfer coefficient across heated and unheated surfaces, the use of more than one coefficient can be satisfactory, and that complex convection coefficient variations are not always necessary for a simple package level thermal analysis. The methodology utilized in this study to establish model boundary surface convection coefficients has been reported by Zahn and Stout [28] and implemented successfully in multiple package level thermal analyses.

2. SILICON BASED MULTI-CHIP MODULE PACKAGE

A 40x40mm, 697-ball (1.00mm pitch), five-chip silicon based multi-chip module (MCM) package was modeled using full three-dimensional symmetry as shown in Fig. 1. The basic structure of the MCM package consists of a "microboard" with etched drop-in through holes for the integrated circuit (IC) chips. Each IC chip is partnered with a corresponding "micropallet" utilized for connection continuity to the microboard where signals are routed between MCM IC's using copper traces. The IC/micropallet and micropallet/microboard solder bump connections are secured using standard underfill material. A layer of benzocyclobutene (BCB) between the silicon and solder balls and bumps acts to redistribute the package stress on the solder materials due to coefficient of thermal expansion mismatches in the package profile stackup. A simplified profile of the MCM package geometry is shown in Fig. 2.

3. SOLDER BALL AND BUMP FATIGUE FINITE ELEMENT MODEL

Viscoplastic finite-element simulation methodologies were utilized to predict ball and bump solder joint reliability of the silicon based five-chip MCM package under accelerated temperature cycling conditions. Due to the non-symmetric nature of the

MCM package geometry, a full symmetry three-dimensional "global" model was created. The global model simulation results were utilized to locate "worst-case" geometrical locations for the solder balls and solder bumps. These locations were further evaluated using detailed "local models" whereby the global model simulation results were applied as local model boundary conditions using the built-in ANSYS submodeling methodology [29].

Fatigue Model Basic Assumptions

A total of four global fatigue models were created to evaluate the multiple package profiles caused by two proposed solder ball and two proposed solder bump configurations (e.g. ball1/bump1, ball1/bump2, ball2/bump1, ball2/bump2). Linear elastic, time and temperature independent properties were assumed for all materials in the global models. The global models treated the underfill and solder bumps as a single composite layer with volumetrically smeared material properties. Global model material properties are displayed in Table 1.

Table 1. Global Fatigue Model Material Properties

Material	Young's Modulus (MPa)	Poissons Ratio	CTE (1/K)
Silicon	162716.27	0.278	2.56E-06
Copper	128931.96	0.344	16.61E-06
BCB	2900.00	0.340	52.00E-06
63/37	30641.69	0.350	24.50E-06
90/10	9638.46	0.350	28.96E-06
Underfill	3447.38	0.350	25.00e-06
FR4	XY 16850.09 Z 7375.40	XZ/YZ 0.390 XY 0.110	X/Y 14.50E-06 Z 67.20E-06

A total of six local models were created to predict solder fatigue conditions in the MCM package. Two of these local models were for the proposed ball configurations as shown in Fig's 3 and 4. Two local models were analyzed for the proposed bump configurations as shown in Fig's 5 and 6. Finally, two local models were created specifically to evaluate the microboard/micropallet and IC/micropallet interconnect bumps associated with the MPU chip as displayed in Fig. 7. Note that the local models utilized non-linear, viscoplastic, time and temperature dependent material properties for the 63Sn/37Pb and 90Pb/10Sn solder materials. Local model non-solder material properties were input as non-linear and temperature dependent in nature. Local model material properties used in the analysis are displayed in Table 2. ANSYS captures the inelastic behavior of the solder materials using Anand's mathematical relations [12]. The recommended Anand constants for 63Sn/37Pb [11] and 90Pb/10Sn are given in Table 3.

Table 2. Local Fatigue Model Material Properties

Material	Young's Modulus (MPa)	Poissons Ratio	CTE (1/K)
Silicon	162716.27	0.278	C0=-5.9E-06 C1=6.3E-08 C2=-1.6E-10 C3=1.51E-13
Copper	128931.96	0.344	C0=13.8E-06 C1=9.4E-09
BCB	2900.00	0.340	52.00E-06
63/37	C0=75842.33 C1=-151.68	0.350	24.50E-06
90/10	C0=23713.00 C1=-47.23	0.350	C0=24.5E-06 C1=1.5E-08
Underfill	3447.38	0.350	25.00e-06
FR4	XY C0=27923.77 C1=-37.16 Z C0=12203.72 C1=-16.20	XZ/YZ 0.390 XY 0.110	X/Y 14.50E-06 Z 67.20E-06

Property=C0+C1(Temp)+C2(Temp)^2+C3(Temp)^3
Where: Temp=Nodal Temperature in Kelvin

Table 3. Recommended Anand Constants

Constant	63Sn/37Pb	90Pb/10Sn	Units
C1	12.41	1.00	MPa
C2	9400	7416	1/K
C3	4.0E+06	2000	1/sec
C4	1.50	6.0E-04	
C5	0.303	0.303	
C6	1378.95	1.0E-09	MPa
C7	13.79	1.00	MPa
C8	0.07	1.0E-09	
C9	1.30	1.00	

Fatigue Model Computational Domain

The focus of this study was to predict the solder ball and bump fatigue for a select group of interconnections. Global and local models were developed using the ANSYS Parametric Design Language (APDL). Due to the non-symmetric nature of the problem, full-symmetry three-dimensional global models were created. Global models were approximately 110455 nodes and 99800 elements in size. Local models detailed the geometry's of only one solder ball or bump interconnect. The global models utilized ANSYS Solid45 structural elements whereas the local models incorporated the use of Visco107 elements for the solder materials, and Solid45 elements for all other structures.

Fatigue Model Boundary Conditions

In the global model the nodes located at three bottom corners of the FR4 printed circuit board upon which the five-chip MCM package was mounted were

constrained as shown in Fig. 8 using the ANSYS D command. A uniform temperature was applied to all global model elements using the ANSYS BFE command and the linear global model was executed for a steady-state structural analysis over 1 degree Kelvin of temperature change using the default frontal solver. This provided global model results in the form of displacements per degree Kelvin as shown in Fig. 9. From the global model simulation results, the locations for worst-case solder ball and solder bump interconnect locations was determined (see Fig. 10) based on the von Mises nodal stress and strain values. Local ball and bump models were created at the pre-determined worst-case locations and the ANSYS submodeling capability was utilized to interpret and apply displacement boundary constraints. Local ball models applied displacement constraints to the FR4 test board and silicon materials. Local bump models applied constraints to only the silicon materials as displayed in Fig. 11.

The sequence of APDL commands required to obtain the boundary constraints from the global model and apply them to a local model starts by writing a file which contains the local model nodes in which the user wants global model boundary constraints to be applied. Note that the user must save both the global and local models using the ANSYS SAVE command so their respective database (db) files can be resumed during the command sequencing.

```
/prep7                  ! enter preprocessor
esel,s,mat,,sili        ! select silicon elem
nsle                    ! select nodes of elem's
nwrite,local,nd         ! write node file
```

The above sequence of commands writes a file named "local.nd" which consists of the local model silicon node numbers and their locations in the global cartesian coordinate system. Next, the global model is resumed and boundary conditions are automatically interpolated from the global model simulation results based on the local model node locations. Note that this requires the local model to be generated at the same XYZ coordinates as the user would like to obtain results data from the global model simulation.

```
resume,global,db        ! resume global model
/post1                  ! enter postprocessor
allsel                  ! select everything
cbdof,local,nd,,local,cb ! write cut boundary
```

The above sequence of commands first resumes the global model, the postprocessor is then entered, all geometry's including nodes and elements are selected, and finally the local.nd file is used to locate and interpolate global model simulation results which are then stored in a file named "local.cb".

```
resume,local,db         ! resume local model
/prep7                  ! enter preprocessor
allsel                  ! select everything
/input,local,cb         ! apply boundary constraint
```

Finally, the global model simulation results are applied as boundary conditions (or constraints) in the local model. The above sequence of commands first resumes the local model, the preprocessor is then entered, all geometry's including nodes and elements are selected, and the global model simulation results are applied as boundary constraints. Note again that only those local model silicon nodes which were written to the "local.nd" file during the first grouped sequence of commands are applied with boundary constraints.

Since the boundary constraints applied to the local model are XYZ displacements for the 1 degree Kelvin temperature change which the linear global model was executed, they may be easily scaled in the thermal cycling of the local model depending on the temperature range to be evaluated using the ANSYS DSCALE command. The solder fatigue analysis used the following ANSYS solution setup commands:

```
eqslv,pcg,1.0e-08       ! set solver and tolerance
antype,static,new       ! set analysis type
nlgeom,on               ! turn on lrg def and strain
nropt,auto,,off         ! set newton-raphson soln

hightemp=100+273        ! high cycle temp (K)
highramp=300            ! low to high ramp (sec)
highdwel=300            ! high dwell (sec)

lowtemp=0+273           ! low cycle temp (K)
lowramp=300             ! high to low ramp (sec)
lowdwel=300             ! low dwell (sec)

delta=hightemp-lowtemp  ! delta cycle temp (K)
rampstep=delta/10       ! ramp substeps
```

Note that the analysis will use one substep for every 10 degree temperature change in a thermal ramp (rampstep=delta/10) as suggested by Darveaux [11]. The following sequence of commands were used to execute the first simulated thermal cycle:

```
tref,hightemp           ! set 0 strain at hightemp

! RAMP LOW
autots,off              ! turn off auto time step
nsubst,rampstep         ! set substeps for load step
bfe,all,temp,,lowtemp   ! apply temp to nodes
dscale,delta            ! scale boundary const
kbc,0                   ! linearly ramp temps
time,lowramp            ! set time at end of step
solve                   ! solve load step
save                    ! save data

! DWELL LOW
autots,on               ! turn on auto time step
```

```
nsubst,10,100,5          ! set time step size
bfe,all,temp,,lowtemp    ! apply temp to nodes
kbc,1                    ! maintain temps
time,lowramp+lowdwel     ! set time at end of step
solve                    ! solve load step
save                     ! save data

! RAMP HIGH
autots,off               ! turn off auto time step
nsubst,rampstep          ! set substeps for load step
bfe,all,temp,,hightemp   ! apply temp to nodes
dscale,1/delta           ! scale boundary const
kbc,0                    ! linearly ramp temps
time,lowramp+lowdwel+highramp
solve                    ! solve load step
save                     ! save data

! DWELL HIGH
autots,on                ! turn on auto time step
nsubst,10,100,5          ! set time step size
bfe,all,temp,,hightemp   ! apply temp to nodes
kbc,1                    ! maintain temps
time,lowramp+lowdwel+highramp+highdwel
solve                    ! solve load step
save                     ! save data
```

The above command sequence of ramp low, dwell low, ramp high, dwell high accounts for one simulated thermal cycle. Note that the same sequence of ramp low, dwell low, ramp high, dwell high commands are repeated for the amount of cycles the user would like to simulate. However, the user must adjust the ANSYS TIME command to reflect the time at the end of each load step. For instance, the next sequence of commands after dwell high would be ramp low, and the TIME command line would read as follows:

```
time,2*lowramp+lowdwel+highramp+highdwel
```

Since the same set of commands is repeated for each simulated thermal cycle, the user may reduce the amount of ANSYS APDL code by incorporating a do-loop which executes once for each desired cycle. However, the full command sequence is presented above for the benefit of the reader.

All local models were simulated over three full thermal cycles at which point the stress-strain hysteresis loop stabilized and the change in solder material plastic work from cycle to cycle became relatively constant. The average viscoplastic strain energy density accumulated between cycles 2 and 3 at the +Z and -Z interface element joints was utilized for all solder joint fatigue assessments.

```
/post1                   ! enter post processor

*do,i,8,12,4             ! get data load steps 8 & 12
set,i,last,1             ! read load step
etable,vt,volu           ! create elem volu table
etable,pt,nl,plwk        ! create elem work table
smult,vpt,vt,pt          ! create volu x work table
ssum                     ! sum vt's, pt's, and vpt's
*get,svpt,ssum,,item,vpt ! get summed vpt's value
*get,svt,ssum,,item,vt   ! get summed vt's value
wavg%i%=svpt/svt         ! calc wavg for load step
*enddo

deltaw=wavg12-wavg8      ! calc delta work
```

After the appropriate interface layer of elements was selected for the +Z or -Z interconnect joint, the above sequence of ANSYS APDL commands was executed to calculate the average viscoplastic strain energy density accumulated per thermal cycle. Note that 8 was the final load step executed as part of thermal cycle 2, and 12 was the final load step executed as part of thermal cycle 3. This stabilized solder joint viscoplastic strain energy density accumulated per thermal cycle was used to evaluate the fatigue resistance of the ball and bump interconnects and is presented in Section 5, "Fatigue Model Simulation Results".

4. THERMAL FINITE ELEMENT MODEL

The FR4 test board for the five-chip MCM package thermal model was expanded to the dimensions of a Joint Electron Device Engineering Council (JEDEC) standard four-layer thermal test board [30] as shown in Fig. 12. The 40x40mm MCM package was positioned at the center of the 101.5x101.5x1.6mm JEDEC test board. The thermal analysis only encompassed one global model configuration which utilized solder balls as shown in Fig. 3.

Thermal Model Basic Assumptions

Table 4. Thermal Model Material Properties

Material	Conductivity (W/mm·C)
Silicon	0.086
Copper	0.393
BCB	0.0002
63/37	0.050
90/10	0.036
Underfill	0.013
Static Air	2.635E-05
FR4	XY: 0.001 Z: 0.003

Due to the non-symmetric nature of the MCM package structure, a full-symmetry, three-dimensional finite element model was developed. Steady-state, laminar flow was assumed in a free or natural convection environment. These assumptions were reflected by the utilization of temperature dependent heat transfer coefficients which also assumed laminar flow and accounted for both natural convection and radiation heat transfer [28]. Like the global fatigue models, the thermal model treated the underfill and

solder bumps as a single composite layer with volumetrically smeared material properties. Thermal model material properties are displayed in Table 4.

Thermal Model Computational Domain

The focus of the thermal study was to perform a first order engineering evaluation to determine the appropriate enhanced cooling apparatus (i.e. heat sink, heat pipe, etc.) which would be necessary to cool the MPU chip to 65C in a 35C ambient environment. The thermal analysis utilized an edited global model from the solder fatigue study and therefore was approximately 110455 nodes and 99800 elements in size. The model incorporated eight node ANSYS Solid70 thermal elements for all material structures.

Thermal Model Boundary Conditions

Table 5. Thermal Analysis Power Configurations

IC Name	Power Config. 1 (Watts)	Power Config. 2 (Watts)
Northbridge	1.80	1.80
Southbridge	0.80	0.80
Cache RAM 1	2.75	1.50
Cache RAM 2	2.75	1.50
MPU	16.00	9.00

Dual surface isoflux free convection correlations were applied in simulations where a heat sink was not assumed. The isoflux surface coefficients were calculated using the sum of the dissipated powers for all five MCM chips. Isothermal free convection correlations were applied in simulations where a package surface cooling apparatus (i.e.heat sink, heat pipe, etc.) was assumed. In these simulations the package surface convection coefficient was applied as a uniform constant value. Thermal simulations were repeated until the appropriate package surface convection coefficient was found which would cool the MPU chip to 65C in a 35C ambient environment. The final surface convection coefficient was then utilized to calculate a case-to-ambient thermal resistance which would be required of the package surface cooling apparatus.

Chip power dissipations were applied as surface heat fluxes using the ANSYS SF command. Two different power configurations were analyzed as indicated in Table 5. Temperature dependent surface convection + radiation coefficients were applied by first generating a temperature table using the ANSYS MPTGEN command and then generating corresponding coefficients using the ANSYS MP command as follows:

```
c4upkg=4.911385E-25     ! set upper pkg coeff's
c3upkg=2.835000E-14
c2upkg=3.163860E-11
c1upkg=1.343671E-08
cnupkg=9.368580E-06

c4upcb=-2.744074E-13    ! set upper test pcb coeff's
c3upcb=1.219123E-10
c2upcb=-1.959122E-08
c1upcb=1.416470E-06
cnupcb=-2.276034E-05

c4lpcb=-1.372037E-13    ! set lower test pcb coeff's
c3lpcb=6.098165E-11
c2lpcb=-9.766855E-09
c1lpcb=7.206510E-07
cnlpcb=-8.869051E-06

mptgen,1,100,tamb,5     ! generate temp table

! generate temp dependent surface coefficient tables
mp,hf,20,cnupkg,c1upkg,c2upkg,c3upkg,c4upkg
mp,hf,21,cnupcb,c1upcb,c2upcb,c3upcb,c4upcb
mp,hf,22,cnlpcb,c1lpcb,c2lpcb,c3lpcb,c4lpcb
```

The c4, c3, c2, c1, and cn values for the various boundary surfaces are calculated by performing a fourth order curve fit of the convection + radiation surface coefficients over the desired temperature range. This was done automatically using a mathematical spreadsheet as discussed by Zahn and Stout [28]. Once the temperature dependent surface coefficient tables are generated, they are applied to the appropriate surface nodes using the ANSYS SF command.

```
tamb=35                 ! set ambient temp
sf,all,conv,-20,tamb    ! apply surface coeff to pkg
```

In the above command line example, the convection value is -20 indicating the use of temperature dependent convection table 20 generated previously by the ANSYS MP command line. The “tamb” value is the assumed ambient temperature of the cooling environment, which for the purpose of this analysis was set to 35C. Note that in those thermal simulations where an enhanced cooling apparatus was assumed attached to the surface of the MCM package, a uniform and constant surface convection coefficient was applied also using the ANSYS SF command.

5. FATIGUE MODEL SIMULATION RESULTS

The solder joint viscoplastic strain energy density accumulated per thermal cycle was used to evaluate the fatigue resistance of the ball and bump interconnects. For abbreviation purposes, we will refer to this as the amount of “plastic work” accumulated per cycle as displayed in Figures 13 through 16 for the various interconnect joints analyzed.

Figure 13 shows the local solder ball model fatigue results for the four analyzed MCM package configurations. The reader should refer to Fig’s 3 and 4 to view solder ball configurations 1 and 2

respectively. Due to the increased standoff height of ball configuration 2, the solder fatigue life proves to be superior. This is certainly the case for the -Z (ball/pcb) solder joint where the amount of plastic work per cycle is significantly reduced.

Figure 14 indicates that the solder bump fatigue for the Northbridge, Southbridge, and Cache RAM IC chips consistently occurs at the +Z end of the solder joint connecting the IC's to their respective micropallets. Bump configuration 2 (see Fig. 6), which is a combination of high temperature and eutectic solder, provides slightly improved -Z joint performance over bump configuration 1 (see Fig. 5). However, it is interesting to note that the 100% composed eutectic material of solder bump configuration 1 seems to provide improved fatigue performance over bump configuration 2 at the +Z joint of the IC's.

Since the bump profile connecting the MPU IC to it respective micropallet does not change during the course of this study (see Fig. 7), its fatigue life can only be influenced by changes to the Northbridge, Southbridge, and Cache RAM IC solder bump configurations, or the adjusted configurations of the solder balls. Figure 15 indicates that the fatigue of the MPU/micropallet solder bump interconnect joints (both +Z and -Z) are in no way sensitive to other ball or bump configurations investigated a part of this study.

The weakest solder reliability in the silicon based MCM package seems to be in the design of the MPU microboard/micropallet solder bump interconnect joints (see Fig. 7) whose profile is also frozen throughout the study. Figure 16 indicates that the amount of plastic work per cycle is by far the most damaging of the study. Although, the utilization of ball configuration 2 seems to relieve some of the damage, the bump +Z and -Z solder joints are still estimated to accumulate 0.10MPa of plastic work per thermal cycle. This is the worst combined +/- joint fatigue seen in the analysis and therefore, the point of greatest concern with respect to solder fatigue reliability in the silicon based five-chip MCM package.

6. THERMAL MODEL SIMULATION RESULTS

Table 6 indicates the free-convection steady-state junction temperature simulation results for MCM chip power configurations 1 and 2 indicated in Table 5 without a package heatsink apparatus. Figure 17 displays isotherm simulation results from the MCM chip power configuration 1 analysis. For both power configurations, thermal simulations were repeated until the appropriate package surface convection coefficient was found which would cool the MPU chip to 65C in a 35C ambient environment. The final surface convection coefficient was then utilized to calculate a case-to-ambient thermal resistance which would be required from the packages enhanced surface cooling apparatus (i.e. heat sink, heat pipe, etc.).

Table 6. Thermal Simulation Results, No Heatsink

	Power Config. 1 (C)	Power Config. 2 (C)
Northbridge	214.4	151.5
Southbridge	192.0	137.6
Cache RAM 1	227.9	155.4
Cache RAM 2	221.2	150.7
MPU	277.5	183.4

Table 7. Thermal Simulation Results, Added Heatsink

	Power Config. 1 (C)	Power Config. 2 (C)
Heatsink θ_{CA}	0.16 C/W	0.42 C/W
Northbridge	40.2	45.0
Southbridge	37.9	40.7
Cache RAM 1	42.9	45.5
Cache RAM 2	42.6	44.4
MPU	64.7	64.2

$$\theta_{CS} + \theta_{SA} = \frac{1}{h \cdot A}$$

Where:

θ_{CA}	Case to Ambient Thermal Resistance (C/W) $\theta_{CA} = (\theta_{CS} + \theta_{SA})$
θ_{CS}	Case to Sink Thermal Resistance (C/W)
θ_{SA}	Sink to Ambient Thermal Resistance (C/W)
h	Applied Package Surface Convection Coeff. ($W/mm^2 \cdot C$)
A	Surface Area of Package (40x40 mm^2)

Table 7 displays the θ_{CA} values and resulting MCM chip temperatures required to cool the MPU. Figure 18 shows the isotherm simulation results from MCM power configuration 1, after the corresponding θ_{CA} convection coefficient h-value was applied uniformly across the package surface. The analyst would use these resulting θ_{CA} values to investigate heat sink or heat pipe manufacturing vendor guides in an effort to locate cost effective case to sink (θ_{CS}) and sink to ambient (θ_{SA}) combinations which meet system cooling requirements. However, it should be noted that this is only a first order thermal analysis in an effort to determine package cooling requirements. Further analysis using computational fluid dynamics (CFD) simulation methodologies (i.e. ANSYS FLOTRAN) is strongly encouraged, including some system level analysis to better assess the circulation environment.

7. SUMMARY

Finite element analysis methodologies have been used to evaluate interconnect joint fatigue performance of multiple solder ball and bump configurations in a

silicon based five-chip MCM package. The fatigue analyses utilized the ANSYS sub-modeling methodology by which global model simulation results were applied as boundary conditions in localized sub-models of the solder balls and bumps. The finite element analysis was extended to include a full-symmetry three-dimensional steady-state thermal evaluation of the MCM package in order to determine the appropriate θ_{CA} required to cool the MPU chip to 65C in a 35C ambient environment. This included the use of non-linear surface convection + radiation coefficients to account for the heat loss to the ambient environment. Methodologies for simulation tool implementation were discussed including multiple examples in the use of the ANSYS Parametric Design Language for pre-processing, solution execution, and post-processing.

Although numerous methodologies exist to convert finite element simulation results (i.e. viscoplastic strain energy density) to cycles to failure under accelerated temperature cycling conditions, these methodologies assume eutectic solder materials. For reasons of analytical uniformity, only the average viscoplastic strain energy density accumulated per thermal cycle (i.e. plastic work/cycle) was used to evaluate the relative performance of the solder balls and bumps. This was done using only the solder interface elements at the +Z and -Z solder joint locations. For more detailed thermal analysis of heat sink attachments, the reader was encouraged to evaluate the use of computational fluid dynamic simulation methodologies such as that provided by the ANSYS FLOTRAN tool.

Finally, it would be optimal to extend the analysis in order to evaluate the effects of heat sink attachments on the second level reliability of solder ball and bump interconnect attachments.

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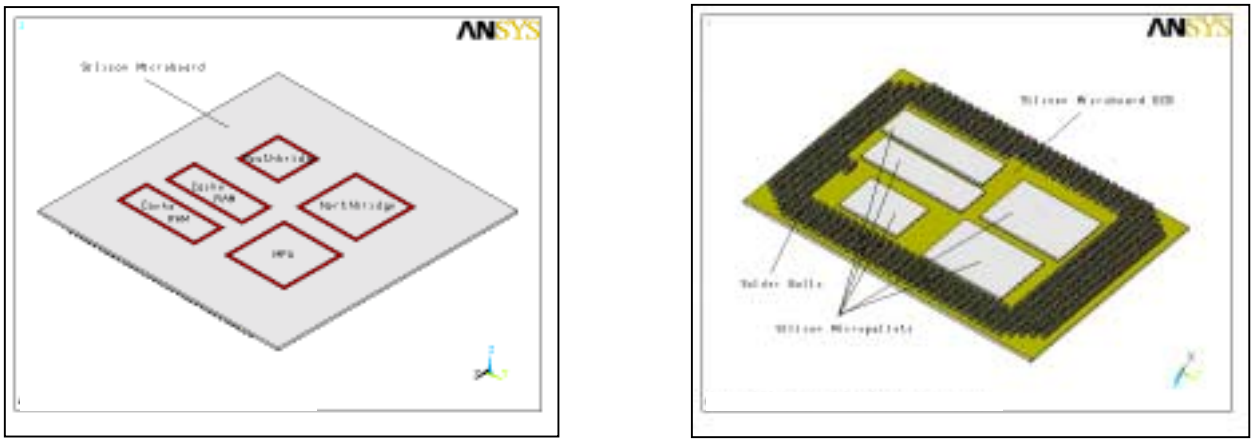


Fig. 1. Top and bottom views of silicon based five-chip MCM package.

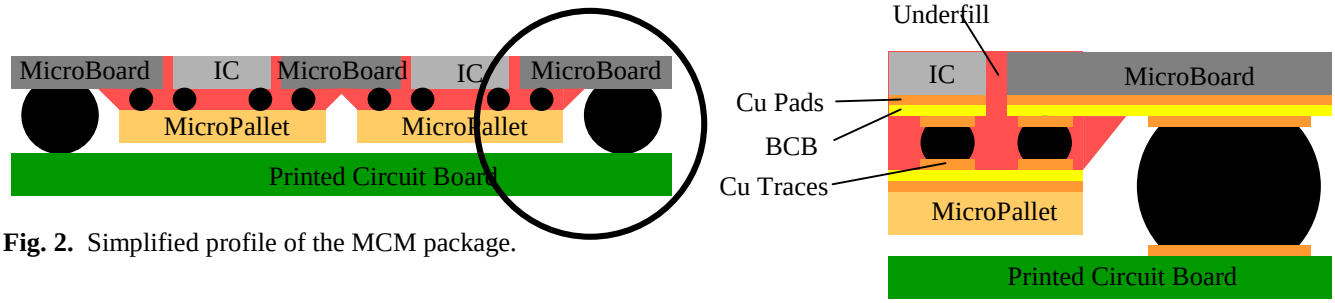


Fig. 2. Simplified profile of the MCM package.

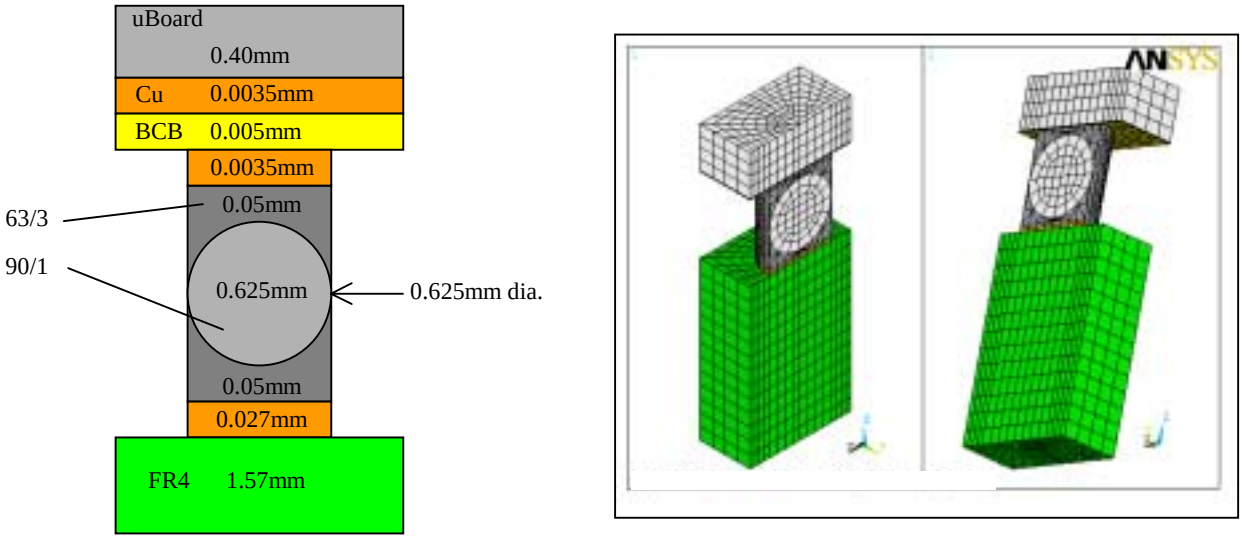


Fig. 3. Solder ball configuration 1.

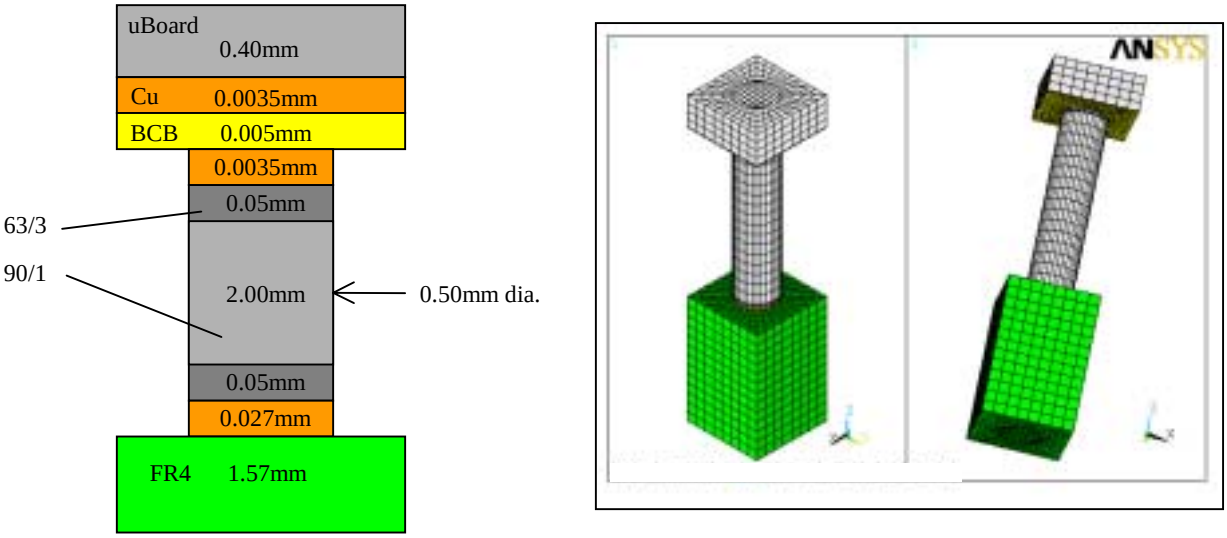


Fig. 4. Solder ball configuration 2.

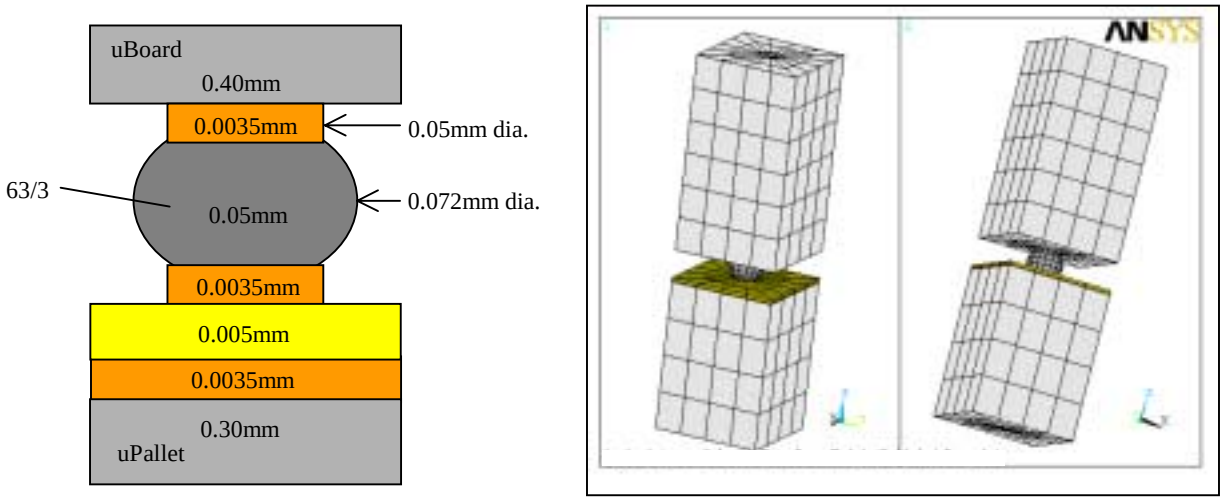


Fig. 5. Solder bump configuration 1.

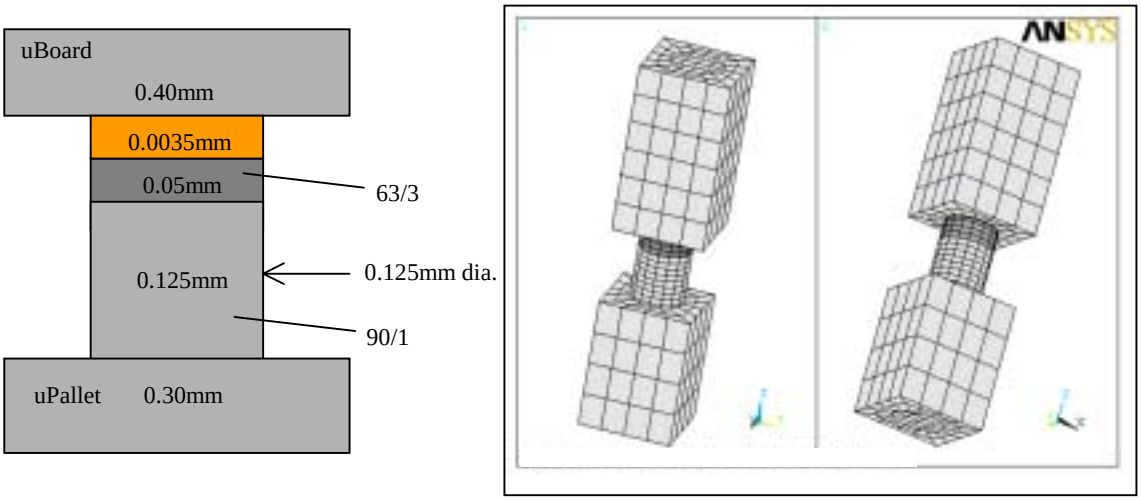
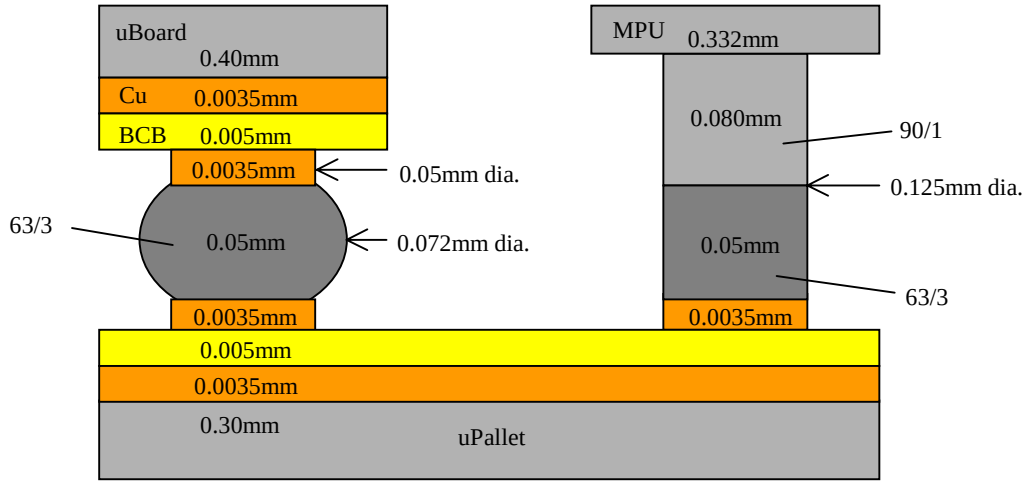


Fig. 6. Solder bump configuration 2.



uBoard/uPallet Bump Configuration

MPU/uPallet Bump Configuration

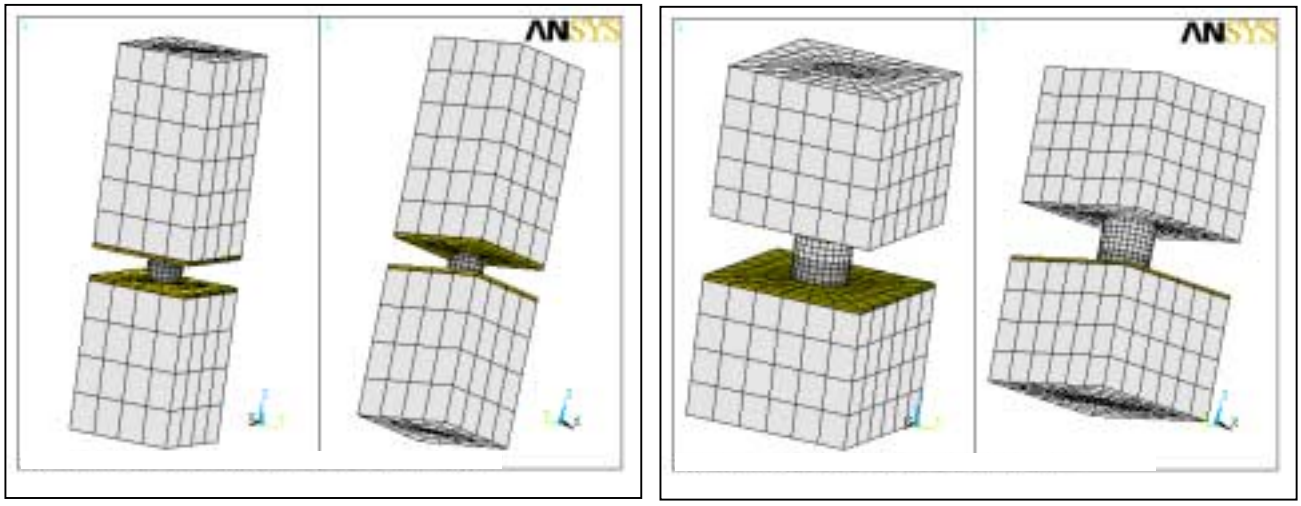


Fig. 7. MPU MicroBoard/Micropallet bump configuration and MPU IC/Micropallet bump configuration.

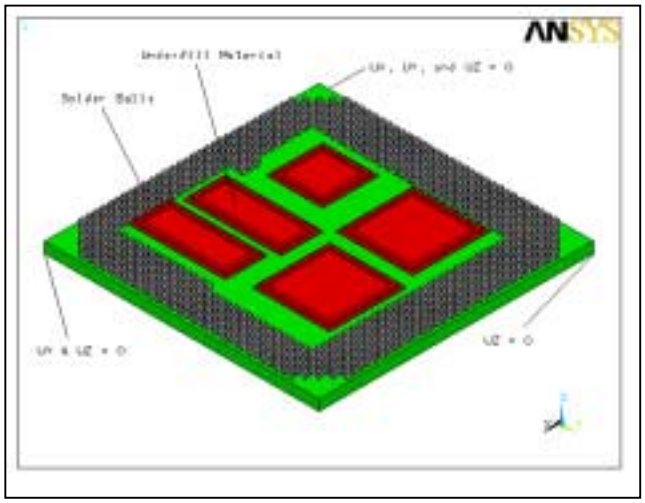


Fig. 8. XYZ constraints placed on the FR4 pcb.

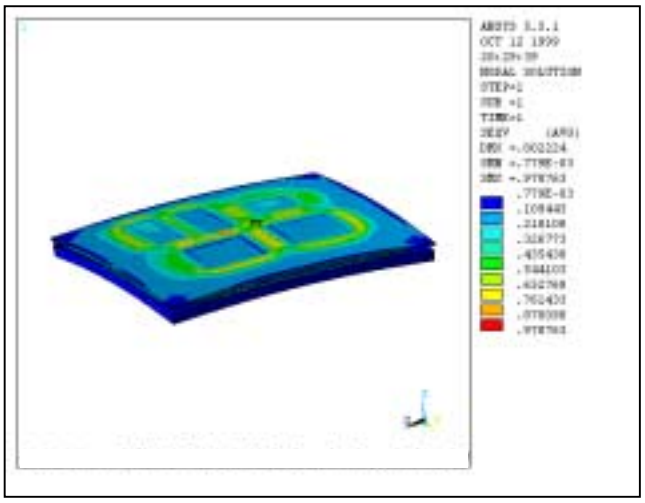


Fig. 9. Global fatigue results (displacements/K).

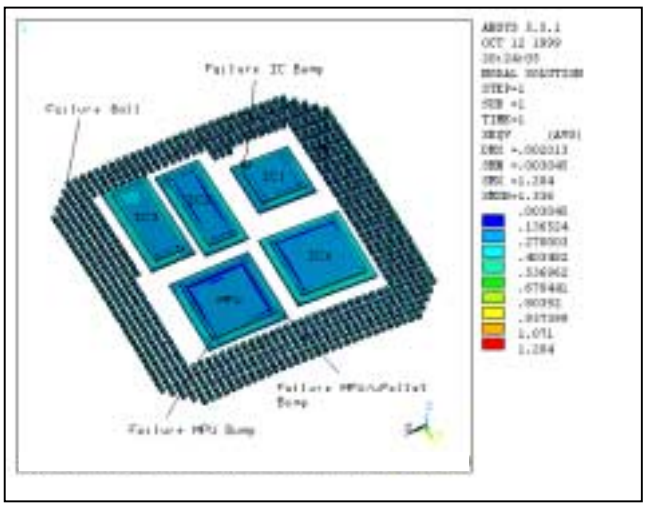


Fig. 10. Global model worst-case interconnect locations.

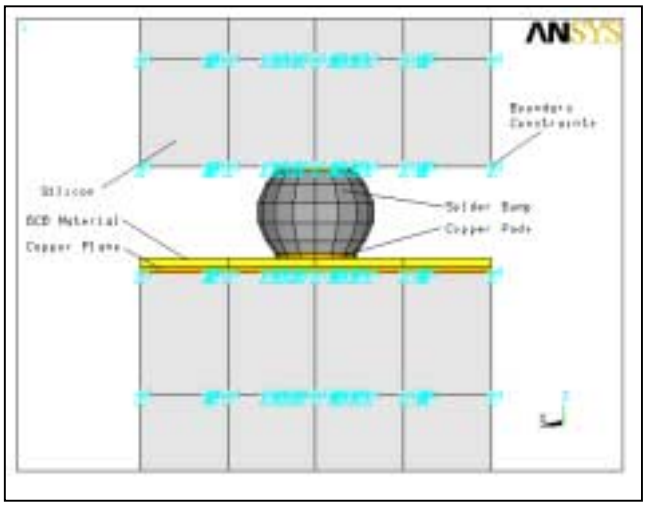
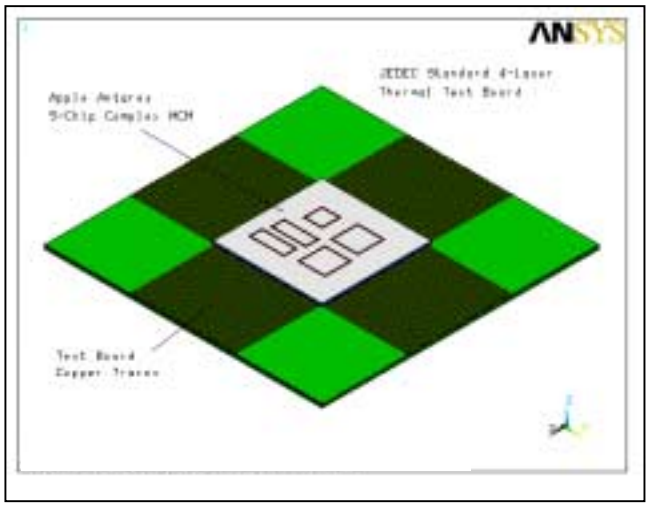


Fig. 11. Local fatigue model constraint application.



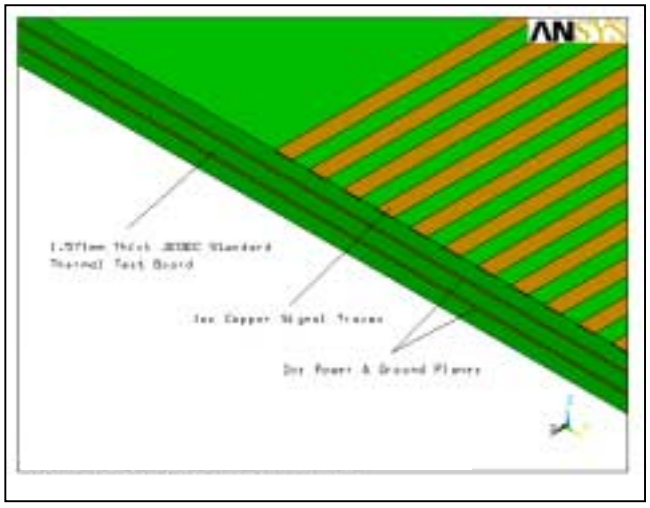


Fig. 12. Joint Electron Device Engineering Council (JEDEC) standard four-layer thermal test board

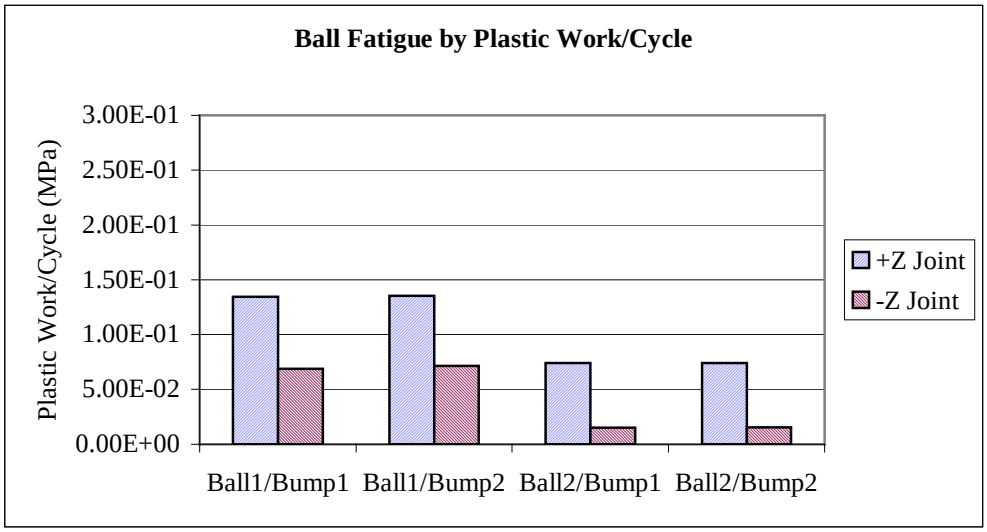


Fig. 13. Solder ball viscoplastic strain energy density for +Z and -Z joint elements.

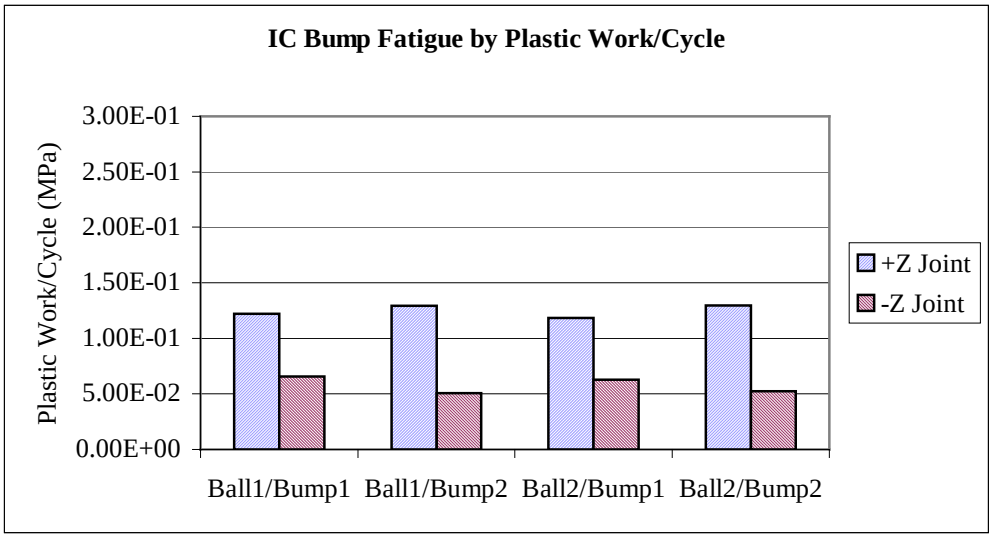


Fig. 14. IC solder bump viscoplastic strain energy density for +Z and -Z joint elements.

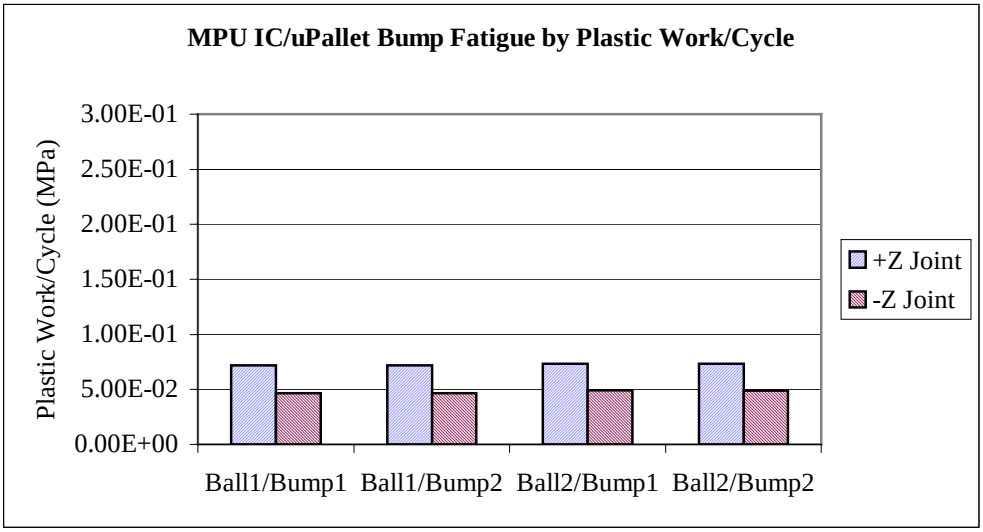


Fig. 15 IC MPU/uPallet solder bump viscoplastic strain energy density for +Z and -Z joint elements.

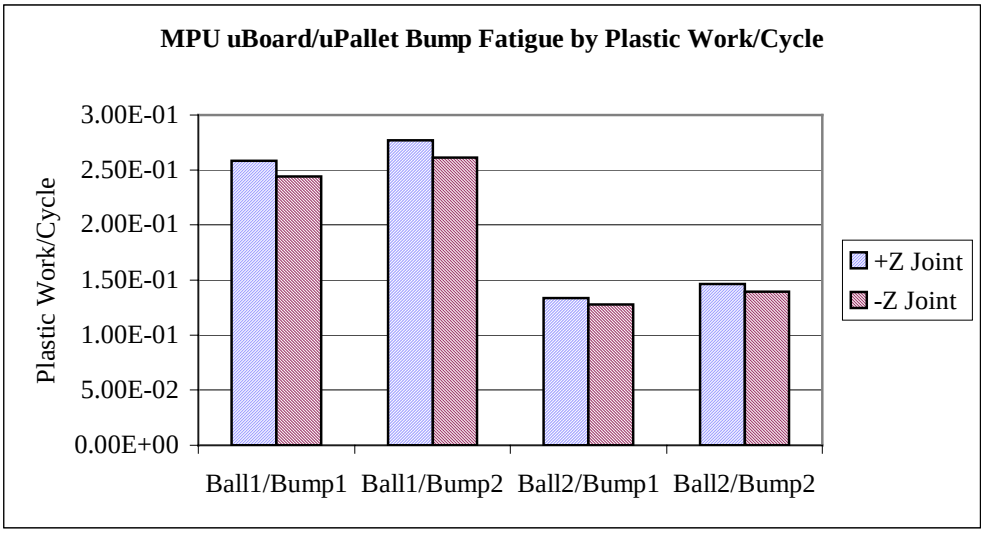


Fig. 16. IC MPU uBoard/uPallet solder bump viscoplastic strain energy density for +Z and -Z joint elements.

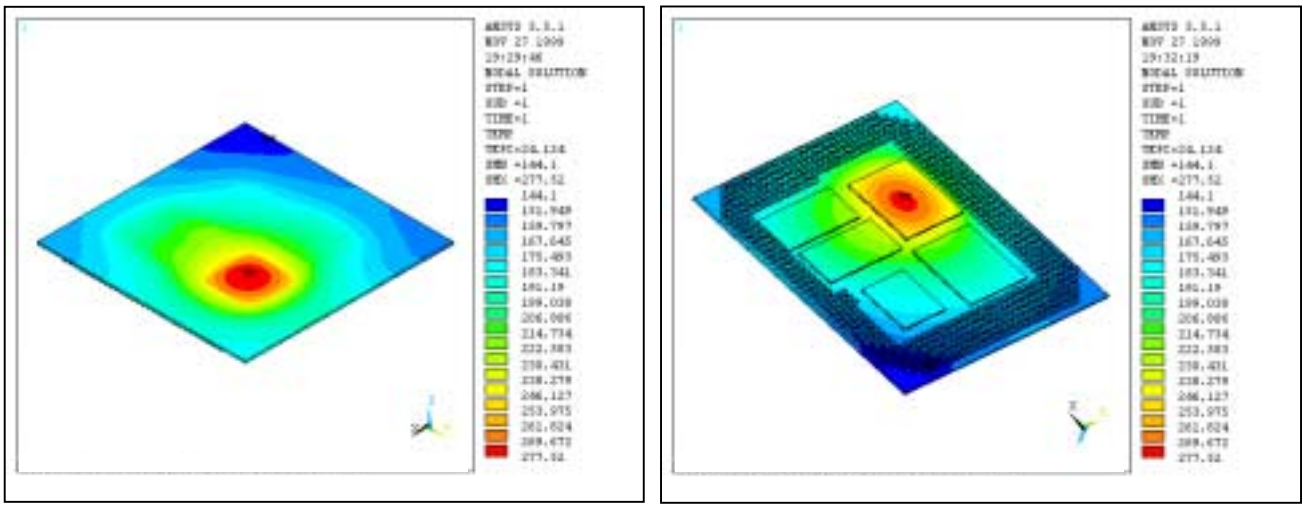


Fig. 17. Isotherm results from the MCM chip power configuration 1 analysis (no enhanced thermal cooling).

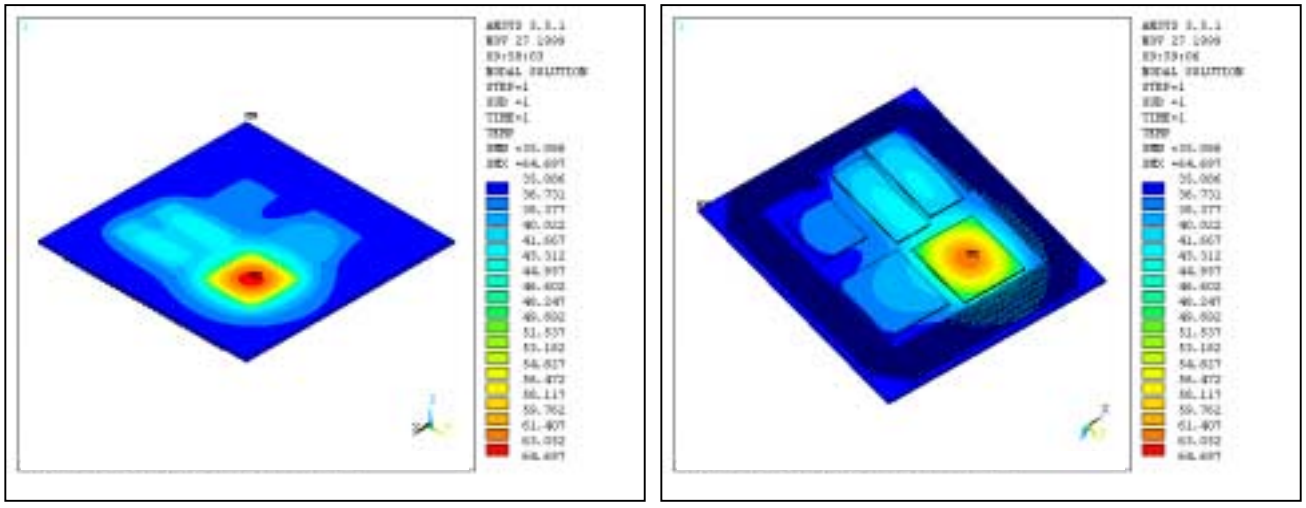


Fig. 18. Isotherm results from the MCM chip power configuration 1 analysis (θ_{CA} enhanced package cooling added).