

Optimizing Board-level Reliability of an Underfilled, Stacked Chip Scale Package

Zane E. Johnson
Nathan R. Schneck
1 June 2012

I. ABSTRACT

Previously benchmarked finite-element (FE) models of a stacked chip scale package (CSP) are used to identify optimum underfill material properties under drop-impact and accelerated temperature cycling (ATC) stress conditions. The simulation sets indicate that an underfill having a modulus of 2–6 GPa and CTE of 25 ppm/K maximizes drop life and does no harm to ATC performance for both Sn63Pb37 and SAC305 solder joints. The methodology described can be applied to other package styles, material sets, and stress conditions.

Index Terms—Electronic packaging, IC packaging, chip scale package, lead free, reliability, simulation, solder joint, finite element analysis, underfill, epoxy flux, SMT, modeling, stress, fatigue, viscoplasticity, shock, drop, optimization.

II. INTRODUCTION

This work focuses on the identification of optimum underfill properties for a particular stacked chip scale package (CSP) assembly. With a long history in flip chip (FC) and direct chip attach (DCA) applications, underfill has seen active development in recent years as second-level or package underfill [1]–[14]. As a consequence, the global underfill materials market has enjoyed rapid growth: \$38M USD in 2003, \$97M in 2005, \$138M in 2007, and in 2011 reaching \$204M [15]–[18]. This represents a compound annual growth rate (CAGR) of 23% over eight years.

Properly applied and cured, underfill spans the gap between the electronic package and printed circuit board (PCB) and encapsulates some or all of the solder joints. Underfill can be applied before surface-mount reflow (so-called “no-flow” underfill) or after reflow (“capillary” underfill). Cure schedules (temperature and duration) can vary widely, depending on the reaction kinetics of the polymer.

Underfill enhances solder joint robustness by reducing the strains imposed on the joints due to thermal expansion mismatch between the package and PCB [19]. It also serves to

The lead author may be contacted at john0167@umn.edu. This work is licensed under the Creative Commons Attribution-NonCommercial-ShareAlike 4.0 International License. To view a copy of this license, visit http://creativecommons.org/licenses/by-nc-sa/4.0/deed.en_US. This material is based on research sponsored by the Defense Microelectronics Activity (DMEA) under agreement number H94003-11-2-1101. The United States Government is authorized to reproduce and distribute reprints for government purposes, notwithstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the DMEA.

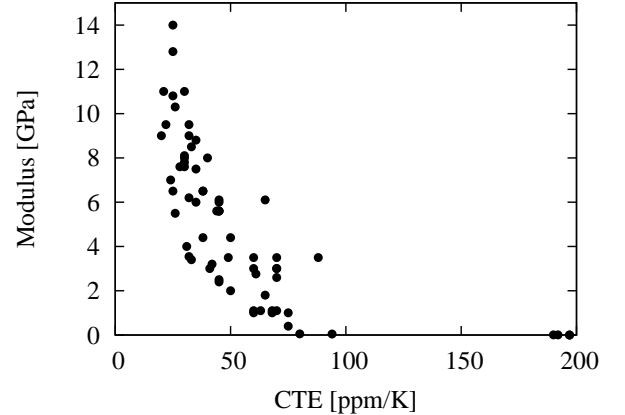


Fig. 1. Room temperature elastic properties of selected commercially-available underfills

seal the solder joints from corrosive or otherwise damaging environments. There are many factors that are important in choosing an underfill. The material must have adequate adhesion to both the PCB and the substrate. It also must have a cure schedule that is compatible with mainstream surface-mount technology (SMT) manufacturing flows. Perhaps most importantly, these added benefits must come without significant added cost.

Underfill is usually comprised of a thermoset organic polymer mixed with a particulate filler [20]. Given the wide range of polymeric formulations in existence, it should come as no surprise that the thermo-mechanical properties of underfill can vary widely. To understand the breadth of product offerings, a market survey of commercially-available underfills was performed. In the context of solder joint robustness, key underfill material properties include but are not limited to the elastic modulus and the coefficient of thermal expansion (CTE). A scatter plot of the properties of these underfills is shown in Fig. 1.

The application of underfill in an assembly can significantly improve the temperature cycling life of various types of electronic packages such as CBGAs, PBGAs, MAPs [21] and flip chips [22], [23]. However, given the wide-ranging underfill formulations on the market, choosing the best underfill for a given application can be a daunting task. Short-duration market windows demand timely decision-making, while reliability test costs are substantial. Fortunately, an FE model benchmarked against good-quality laboratory data can reduce

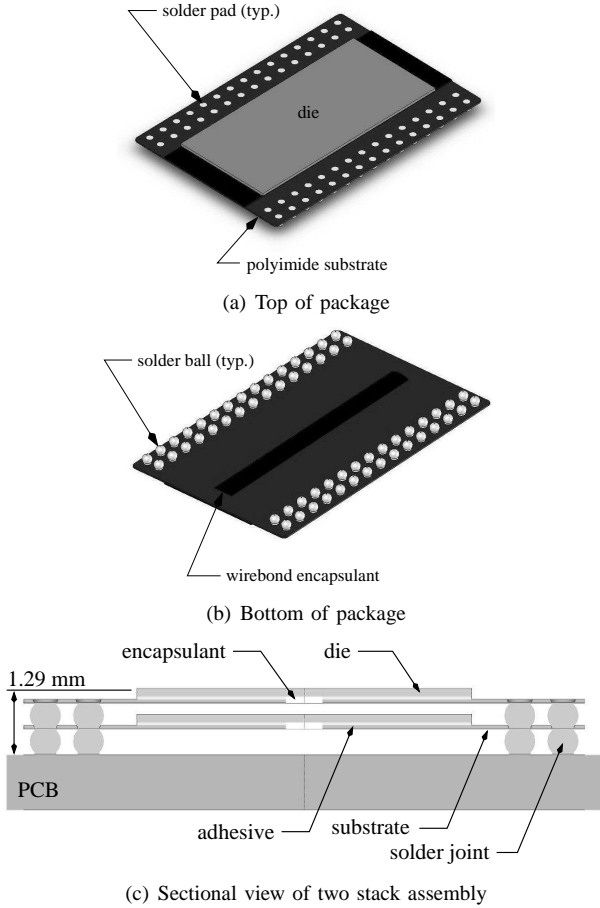


Fig. 2. The stackable chip scale package

development costs and substantially reduce the time required to qualify a new product or process.

III. CSP TEST VEHICLE

A commercially available “stackable” CSP was chosen for this study [24], [25]. The package is based on a 50 μm thick polyimide substrate with a single copper layer providing routing to 60 solder spheres arranged in a heavily depopulated 13×15 array. Two rows of solder spheres are placed on the long edges of the package, beyond the die edge, to allow packages to be stacked vertically. The package body size is 10.6×15.4 mm and supports a 6.1×12.9 mm die. The solder joint standoff height is 450 μm with a joint pitch of 0.8 mm spanwise and 1.0 mm lengthwise. The package is shown in Fig. 2.

Test vehicles were assembled in two configurations, a two package stack and an eight package stack. These are referred to as the “two-stack” and “eight-stack” and are shown in Fig. 3. For assemblies with underfill, a commercial dispense machine was used to fill the lowest two packages in the stack. A perimeter dispense pattern was used, with little or no voiding in the final cured material. Two commercially-available underfills were included in the study. Two solder alloys were included, Sn36Pb37 and SAC305 (Sn96.5Ag3.0Cu0.5). A four-layer test PCB was designed for drop testing that included multiple probe points to aid in failure analysis [26].

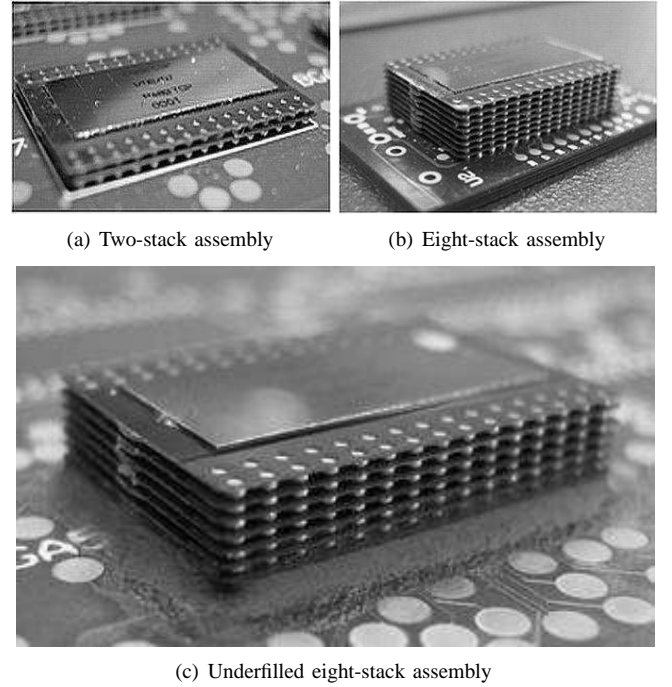


Fig. 3. The two and eight-stack chip scale package configurations

IV. FINITE ELEMENT SIMULATION

The primary goal of this work was to find a combination of underfill material properties that would maximize both ATC and drop-impact life for a stacked CSP. This was done using previously reported finite element models that were benchmarked against experimental data for drop-impact [26] and ATC testing [25]. The drop-impact models simulated the test conditions of JEDEC Standard JESD22-B111 [27] while the ATC models simulated the conditions of IPC 9701-A [28]. Results from the two FE models were used to identify an underfill having the optimum CTE and elastic modulus.

A. Solder Joint Shape

The shape and standoff height of the solder joint is an important issue in designing a complete package-on-PCB assembly and requires a separate modeling effort of its own. Solder-bearing paste is usually applied to the PCB pads prior to reflow. As the assembly enters reflow and the solder balls melt, the volume of solder in the ball joins with the solder in the paste and a nearly spherical joint forms. This truncated spherical shape is driven primarily by surface tension forces, with gravity and package weight typically having a negligible effect. As the assembly exits reflow, the solder solidifies and forms attachments to the copper pads on the substrate and PCB.

An FE-based tool [29] was used to calculate the solder joint standoff height and profile for this CSP package. Based on an initial surface shape and volume, the program evolves the surface to its minimum energy state through a gradient descent method. Previous work shows that this tool provides accurate predictions of BGA solder joint shapes [30].

TABLE I
WEIBULL PARAMETER SUMMARY OF DROP TEST DATA

	η	β	n
8 stack Sn63Pb37	62.0	3.10	8
8 stack SAC305	2.74	1.91	7
2 stack Sn63Pb37	110	6.83	5
2 stack SAC305	35.4	4.28	3
8 stack SAC305, underfill A	115	3.26	5
8 stack SAC305, underfill B	62.7	3.24	4
2 stack SAC305, underfill A	no fails in 250 drops		3
2 stack SAC305, underfill B	no fails in 250 drops		4

η : Weibull characteristic life, β : Weibull shape factor, n : no. of samples

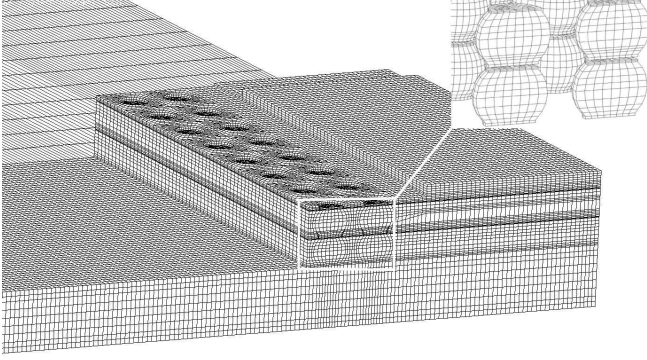


Fig. 4. Quarter-symmetry two-stack underfilled FE model (underfill removed from detail view)

B. Drop Test Modeling

Standards-compliant drop testing and failure analysis was performed and is described in detail in previous work [26], [31]. A summary of those test results is provided in Table I.

Pre-processing for the drop simulation was performed using a commercial FE package [32]. Another commercial FE tool was used in the solution phase [33], while a third commercial tool was used to post-process the stress-time history [34]. An eight-node hexahedral solid element was used to discretize the model geometry. Each node had nine degrees of freedom: velocity, acceleration, and translation in the x , y , and z directions [35]. A full integration option was used to improve solver stability. A meshed two-stack model is shown in Figure 4. Typical solution times were 35 hours for an eight-stack model and 25 hours for a two-stack model on a workstation having dual quad-core 2.6 GHz processors and 32 GB of RAM.

The JEDEC drop test imposes a short duration half-sinusoidal impulse (test condition B: 1500 g peak with 0.5 ms duration) on the assembly followed by resonant vibrations (ringing) of the PCB. These conditions are typically simulated using linear and elastic properties. In drop-impact modeling, the properties of the PCB and solder alloy are particularly important. Material constants for the materials in this stacked CSP assembly were taken from manufacturer data sheets and in most cases were confirmed by in-house testing [25]. All materials but the PCB were given linear-elastic properties and are shown in Table II. The PCB was treated as an anisotropic elastic material with properties derived from bend testing and FE modeling [26]. In the model, all interfaces are assumed

TABLE II
LINEAR-ELASTIC MATERIAL PROPERTIES

	E [Pa]	ν	α [ppm/K]	ρ [g/mm ³]
die	163×10^9	0.34	$= \alpha(T)$	2.33×10^{-3}
die bond	3.00×10^6	0.33	20.0	1.10×10^{-3}
encapsulant	3.00×10^6	0.33	260	1.42×10^{-3}
substrate	6.80×10^9	0.33	20.0	1.47×10^{-3}
underfill A	5.50×10^9	0.35	26.0	1.70×10^{-3}
underfill B	50.0×10^6	0.35	210	1.18×10^{-3}
solder pad	129×10^9	0.34	$= \alpha(T)$	8.90×10^{-3}
PCB	$E_x 24.8 \times 10^9$ $E_y 20.7 \times 10^9$ $E_z 10.0 \times 10^9$ $G_{xy} 11.0 \times 10^9$ $G_{xz} 8.93 \times 10^9$ $G_{yz} 7.44 \times 10^9$	$\nu_{xy} 0.11$ $\nu_{xz} 0.39$ $\nu_{yz} 0.39$	$\alpha_x 18.6$ $\alpha_y 18.6$ $\alpha_z 57.4$	1.91×10^{-3}

E: elastic modulus, ν : Poisson's ratio, α : CTE, ρ : mass density

TABLE III
TRILINEAR STRAIN (ϵ) AND STRESS (σ) DATA AT 293 K (INTERPOLATED FROM [36])

	Sn63Pb37	SAC405
ϵ_1, σ_1 [-, MPa]	0.0007, 21.7	0.0014, 56.0
ϵ_2, σ_2 [-, MPa]	0.003, 37.7	0.004, 77.3
ϵ_3, σ_3 [-, MPa]	1.00, 533.3	1.00, 1900
ν	0.35	0.36

“strong” and do not delaminate, including the underfill/solder interfaces.

Trilinear elastic-plastic behavior was assumed for the solders [36], with the material constants listed in Table III. Trilinear constants for SAC305 were unavailable at the time of this work, but the properties of SAC405 are similar and have been used with success to model SAC305 behavior [37]. The properties of SAC405 were used in this work to represent SAC305.

Application of the FE loads was based on a modified base excitation method [38], [39]. Instead of applying a constant force to the nodes, an acceleration time-history vector was applied. Regions where the circuit board was attached to standoffs were fixed to prevent out-of-plane displacements. The simulation duration was typically 10 ms, long enough to capture the initial impulse and several cycles of PCB resonant vibration.

To make reliability predictions using FE analysis, a damage parameter must be defined that will quantify failure risk. In this work, the peak normal nodal stress in the solder, at the interface between solder and pad, was selected as the damage parameter. The normal stress was used because it is easily extracted from FE results and is considered one of the primary drivers for initiating cracks in solder joints [40]. Also, an important step in benchmarking an FE model is to verify that the location of first failure observed in testing is reflected in the model. In both test and simulation, the two-stack assembly showed first failure and highest stress in the solder-PCB pad interface in the outermost (corner) solder joint. In the eight-stack assembly, first failure and highest stress occur in the outermost solder joint immediately above the underfilled layer.

Failure analysis was performed using mechanical cross-

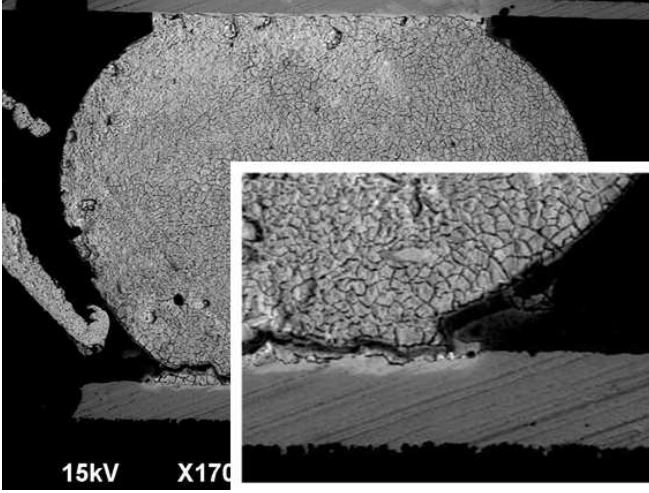


Fig. 5. SEM image of a failed SnPb solder joint in an 8-stack assembly [26].

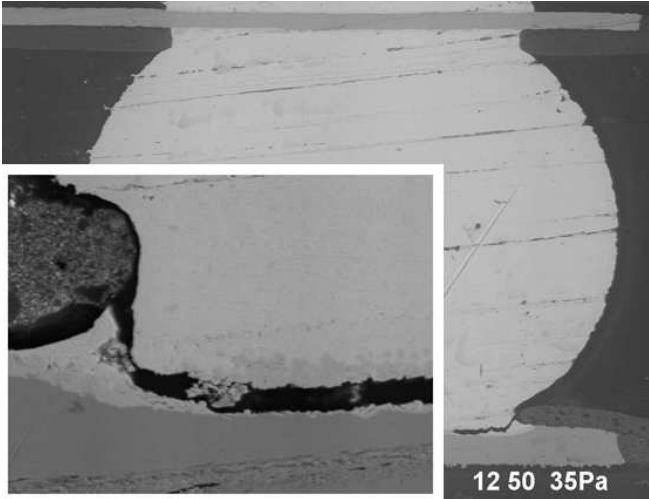


Fig. 6. SEM image of a failed SAC solder joint in an 8-stack assembly [26].

sectioning and scanning electron microscope (SEM) imaging. The SnPb joints showed crack initiation and propagation through the bulk solder in a zone near the intermetallic layer and solder pad, as in Fig. 5. In contrast, SAC solder joints showed a largely interfacial fracture through the intermetallic layer at the pad-solder interface, as in Fig. 6.

In previous work [26], linear regression correlations were developed that link the drop-impact Weibull characteristic life of the stacked packages to the maximum normal solder joint stress obtained from simulation. The regression took the form $\eta = m(\sigma_z) + b$, where η was the characteristic life of the package and σ_z was the maximum normal nodal stress in the critical solder joint (in units of MPa). For Sn63Pb37 there were two data points, providing the relationship $\eta = -9.06(\sigma_z) + 800$. Four data points were available for packages with SAC305 solder joints, providing the regression equation $\eta = -1.36(\sigma_z) + 184$. These equations are updates from what was previously reported [26].

TABLE IV
ANAND PARAMETERS FOR SOLDERS USED IN ATC SIMULATIONS

		Sn63Pb37 [42]	SAC305 [44]
s_o	[MPa]	12.41	45.9
Q/R	[1/K]	9400	7460
A	[1/s]	4.00×10^6	5.87×10^6
ζ		1.5	2.0
m		0.303	0.0942
h_o	[MPa]	1380	9350
s	[MPa]	13.79	58.3
n		0.070	0.015
a		1.3	1.5

TABLE V
THERMO-ELASTIC PROPERTIES OF SOLDERS USED IN ATC SIMULATIONS

		Sn63Pb37 [45]	SAC305 [46]
E	[MPa]	45.5 (200 K)	51.0
		7.58 (450 K)	
CTE	[ppm/K]	24.5	25.0
ν		0.35	0.35

C. ATC Modeling

Solder fatigue resulting from accelerated temperature cycling is a complex phenomena involving solid and fluid mechanics, metallurgy, and time- and temperature-dependent material behavior [41]. Solder in particular exhibits complex behavior in response to changes in temperature and imposed strain, making the thermo-mechanical simulation of package-level solder joint fatigue a significant challenge.

The literature provides a well-established methodology for making eutectic SnPb solder joint fatigue predictions based on nonlinear FE analysis [42]. For BGA packages under temperature cycling conditions, laboratory measurements of low-cycle fatigue crack initiation and crack growth were correlated to the viscoplastic strain energy density (SED) calculated in the solder joint. The viscoplastic solder behavior is captured using Anand's model [43].

The method typically delivers “2×” accuracy; i.e. the predicted Weibull characteristic life of the assembly is within a factor of two of the experimental value. The method provides a characteristic life prediction for each solder joint-pad interface. The overall package lifetime is then defined as that of the single joint interface having the lowest predicted lifetime. Detailed descriptions of the methodology are available [30], [42].

The nine material constants used in Anand's model for Sn36Pb37 and SAC305 are listed in Table IV. The thermo-elastic properties for the solder alloys are listed in Table V. Properties for the remaining materials in the assembly are listed in Table II.

A commercial FE code [32] was used for all modeling phases: pre-processing, solution, and post-processing. The model geometry is that of a three-dimensional “slice” similar to those used in numerous BGA solder joint reliability studies. The slice model passes through the thickness of the assembly, capturing all major components and a full set of solder joints.

The 8-stack assembly model is shown in Fig. 7. Symmetry boundary conditions were applied to the model faces that

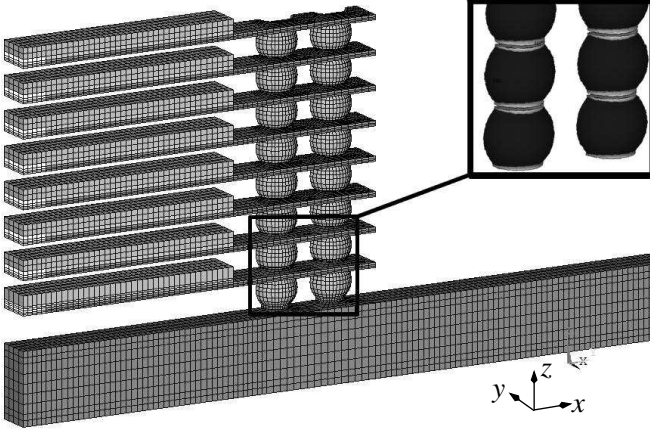


Fig. 7. The 8-stack slice model containing 54,000 nodes and 33,000 elements (detail view shows contours of strain energy density in the solder)

TABLE VI
COMPARISON OF SIMULATED AND MEASURED WEIBULL
CHARACTERISTIC LIFE (η) UNDER -40/125 °C ATC CONDITIONS

	α from simulation [25]	α from experiment [48]	ratio
8-stack	3530 cycles	3432 cycles	1.03
4-stack	4160	4473	0.93
1-stack	8220	n/a	n/a

intersect the origin, normal to the x and y axes. The nodes on the slice plane had their y displacements coupled. All other surfaces were unconstrained. As with the drop-impact model, no interface is allowed to delaminate, including the underfill-solder interface.

It should be noted that the design of this package lent itself particularly well to the slice representation. With its large die and sparse directional solder joint array, the package was truly an assemblage of identical slices. Previous work displayed excellent agreement between test and simulation, as shown in Table VI.

Using this methodology, various design factors and parameter sensitivities were explored. For example, mounting molded plastic BGA packages in a double-sided and symmetric manner can reduce fatigue life by a factor of two or three [30], [47]. For these stacked packages the effect was much smaller, as shown in Table VII. This is due to the thin, flexible nature of the polyimide substrate and the lack of a mold cap which effectively decoupled the solder joints from the stiffness imposed by the die and package structures.

TABLE VII
PREDICTED WEIBULL CHARACTERISTIC LIFE UNDER 0/100 °C ATC
CONDITIONS FOR SINGLE- AND DOUBLE-SIDED ASSEMBLIES

	single-sided	double-sided	ratio
8-stack	9,870 cycles	8,740 cycles	0.86
4-stack	12,200	9,800	0.80
1-stack	31,600	22,600	0.72

V. FE-BASED UNDERFILL OPTIMIZATION

With benchmarked FE models in hand, it is a relatively simple matter to conduct designed numerical experiments. Such experiments can be used to explore any number of design factors, material sets, or loading conditions. The use of FE modeling is particularly attractive when analyzing underfilled package assemblies, given the significant cost and time involved in the preparation and testing of physical parts. Benchmark FE models can, therefore, be an effective screening tool in identifying the most promising underfill formulations.

A. Drop Test Optimization

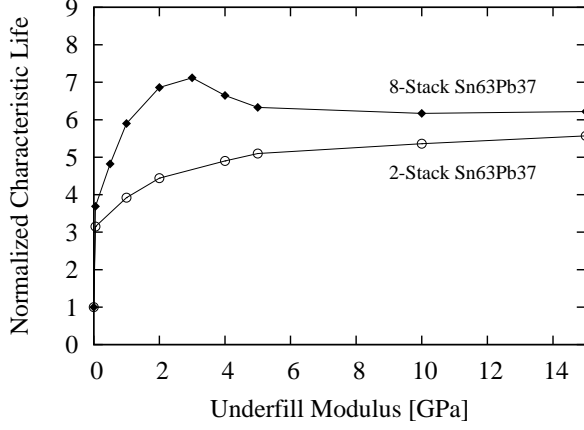
Four sets of drop-impact simulations were run. These sets consisted of two-stack and eight-stack assemblies involving Sn63Pb37 and SAC305 solder joints. Each set included eight simulations covering a range of underfill elastic modulus values. The modulus values ranged from zero (no underfill), a low-modulus unfilled (reworkable) underfill, and six additional cases representing underfills having modulus values of 2, 5, 10, and 15 GPa. The result from each run was converted to a lifetime prediction using the correlations presented earlier. Fig. 8 summarizes the results, with predicted lifetimes normalized to the “no underfill” case. In practical terms, the vertical axis in Fig. 8 represents the expected improvement in characteristic life as a function of the underfill modulus.

Fig. 8 clearly shows that the addition of underfill material lowered the maximum normal stress in the solder materials, which was expected and corresponded to a significant improvement in drop-impact life. Interestingly, the two-stack models followed a different trend than the eight-stack models. For the two-stack models, predicted lifetime steadily increased with modulus, though beyond 5 GPa the additional benefit was small. For the eight-stack models, predicted life sharply increased with modulus up to 3 GPa and slightly decreased beyond that value. For all models, underfills having a modulus in excess of 5 GPa provided little incremental benefit.

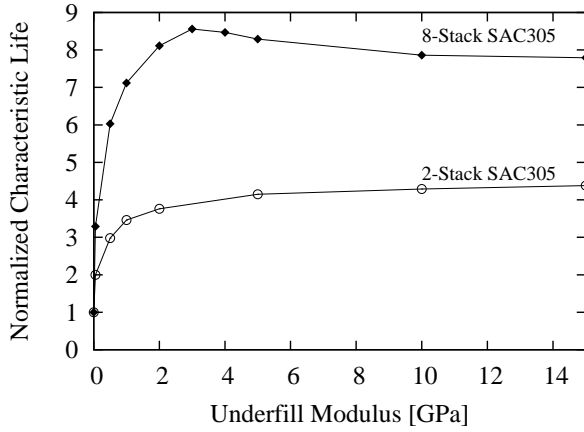
Eight-stack assemblies benefited greatly from the addition of underfill to the bottom two packages in the stack. Common underfills in the 2–5 GPa range provided a 6–8 \times improvement in predicted Weibull characteristic life, regardless of solder alloy. Two-stack assemblies experienced a smaller yet still significant 3–5 \times gain. In some cases, this marked improvement in life can mean the difference between market acceptance or rejection.

B. ATC Optimization

Four configurations of stacked packages were considered; the two-stack and eight-stack assemblies having solder joints comprised of either Sn63Pb37 or SAC305 alloy. The thermo-mechanical nature of ATC testing dictated that two underfill properties be varied in the simulation set: the elastic modulus and the CTE. The modulus was varied from zero (no underfill) to 15 GPa, the same range covered by the drop-impact modeling. The CTE was varied from 5 to 75 ppm/K. ATC conditions were 0–100 °C, with 10 minute ramp and 5 minute dwell periods.



(a) Sn63Pb37 solder



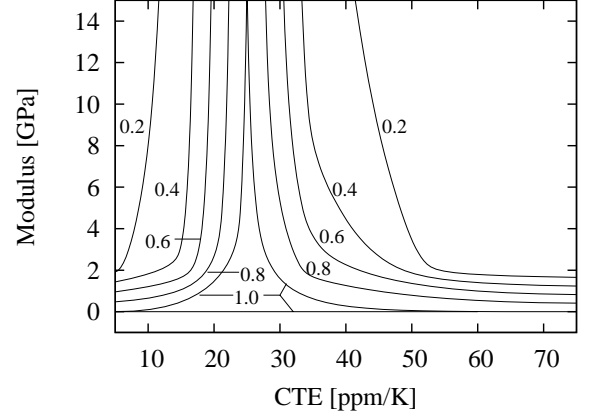
(b) SAC305 solder

Fig. 8. Drop-impact simulation results

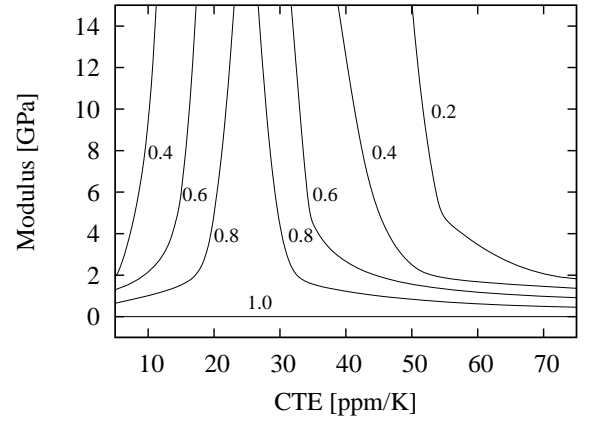
For assemblies containing Sn63Pb37 solder joints, the results are summarized in Fig. 9. Each simulation result was converted to a prediction of Weibull characteristic life [42] and then normalized to the no-underfill case. Contour labels represent the ratio of the predicted life of the underfilled part to the life of the non-underfilled part. All contour labels in Fig. 9 are at most unity, indicating that for most combinations of modulus and CTE the addition of underfill *reduced* predicted life.

For SAC305 joints, no correlation between SED in the solder and Weibull characteristic life was available, therefore direct calculation of characteristic life was not possible. Generally speaking though, FE-obtained SED is roughly inversely proportional to measured characteristic life [49]. The expected benefit from underfill can therefore be quantified by using the ratio of the non-underfilled SED to the underfilled SED. The contour labels shown in Fig. 10 are this ratio and represent the expected improvement in characteristic life. As with the SnPb results, however, regions where the contour labels are less than unity indicate underfill formulations that result in reduced characteristic life.

The lack of benefit for most underfill formulations in ATC is thought to result from the unique nature of the test vehicle package design. The solder joints are nearly free standing, cou-



(a) Two-stack configuration



(b) Eight-stack configuration

Fig. 9. Sn63Pb37 ATC simulation results

pled only through a fairly compliant 50 μm organic substrate. Any additional material in and around the solder joints would seem to serve only to constrain them further, thereby reducing fatigue life.

In summary, the addition of underfill did not significantly improve the ATC performance, and at best did no harm. The contours show that for modulus values below roughly 2 GPa, modulus was a more influential factor than CTE. Above 2 GPa, CTE was the more influential. In the region of 2 GPa and 25 ppm/K the underfilled characteristic life differs little from the non-underfilled. However, underfills that had a modulus of 2 GPa or more that deviated from a CTE of 25 ppm/K showed a sharply reduced characteristic life. This result emphasizes the need to choose package underfill carefully, with emphasis given to accurately measuring its thermo-mechanical properties.

VI. CONCLUSION

Considering the drop and ATC simulations together, a combination of underfill material properties can be selected to maximize drop life and minimize harm to ATC performance. This “optimum” underfill has an elastic modulus of between 2 and 6 GPa and a CTE of 25 ppm/K. These values work well for both two and eight-stack configurations and both solder alloys.

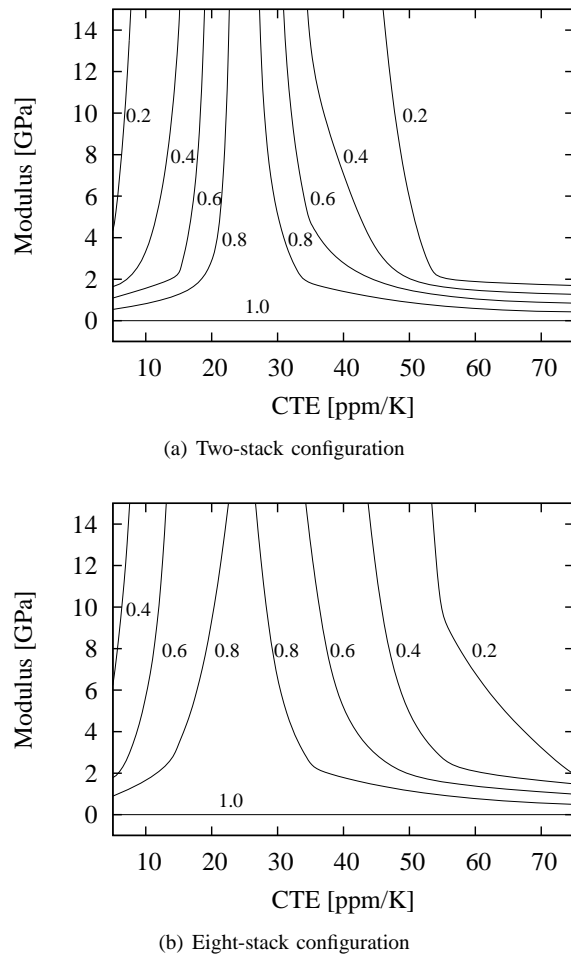


Fig. 10. SAC305 ATC simulation results

Referring to Fig. 1, there are several commercial underfills with properties in this range.

Note that the trends shown in Figs. 8, 9, and 10 will change for different package styles, material sets, stress conditions, and lifetime prediction methodologies. That said, we would expect most package styles to show an improvement in drop and ATC performance when an optimum underfill is employed, but it is not guaranteed. A systematic approach in identifying suitable underfill candidates is required, combined with judicious experimental work.

The screening and optimization methods used in this study are broadly applicable. They are particularly well-suited to parametric studies of design factors, material sets, and stress conditions. Such systematic studies can provide useful guidance in initial SMT design and in the selection of underfill materials for laboratory testing. The models are reasonably simple to construct and employ well-documented simulation techniques and lifetime prediction methodologies.

REFERENCES

- [1] J.-Y. Lee, T.-K. Hwang, H.-Y. Kim, M. Yoo, E.-S. Sohn, and J.-Y. Chung, "Study on the board level reliability test of package on package (PoP) with 2nd level underfill," in *57th Electronic Components and Technology Conference*, 2007.
- [2] C.-F. Chen, "effect of underfill settling on thermo-mechanical fatigue analysis of flip-chip eutectic solders," *Microelectronics Reliability*, vol. 48, pp. 1040–1051, 2008.
- [3] W. Engelmaier, "Reliability improvement with underfills," *Global SMT & Packaging Magazine*, vol. 6.3, pp. 66–67, March 2006.
- [4] A. J. Babiarz, A. R. Lewis, and R. L. Ciardella, "Automating underfill for non-traditional packages, secondary CSP underfill, stacked die, and no-flow underfill," in *SMTA Pan Pacific*, (Maui, Hawaii), January 2000.
- [5] H. Quinones, A. Babiarz, L. Fang, and Y. Nakamura, "Encapsulation technology for 3D stacked packages," in *ICEP/Microelectronics Tokyo*, (Tokyo), April 2002.
- [6] B. Perkins, "Design considerations for package on package underfill," *Advanced Packaging*, November 2008.
- [7] K. C. Choong, Y. C. Yin, V. Rudge, S. L. Szu, and E. Then, "Underfilling flip chip packages with transfer molding technologies," in *Electronics Packaging Technology Conference*, December 2004.
- [8] Anon., "Assemblies go PoP," *Circuits Assembly*, 2007.
- [9] S. J. Adamson, "Review of CSP and flip chip underfill processes and when to use the right dispensing tools for efficient manufacturing," in *GlobalTRONICS Technology Conference*, (Singapore), 2002.
- [10] H. Peng, R. W. Johnson, G. Flowers, E. Yeager, M. Konarski, A. Torres, and L. Crane, "Underfilling micro-BGAs," in *HD International Conference on High-Density Interconnect and Systems Packaging*, 2000.
- [11] J. Lui, R. W. Johnson, E. Yeager, M. Konarski, and L. Crane, "Processing and reliability of CSPs with underfill," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 26, pp. 313–319, October 2003.
- [12] M. Rampurawala, M. Meilunas, A. Gowda, and K. Srihari, "Mechanical reliability of underfilled CSP assemblies," in *37th Annual IMAPS Nordic Conference*, (Helsingor, Denmark), 2000.
- [13] T. Burnette, Z. Johnson, T. Koschmieder, and W. Oyler, "Underfilled BGAs for a variety of plastic BGA package types and the impact on board-level reliability," in *51st Electronic Components and Technology Conference*, 2001.
- [14] S. Rzepka, M. A. Korhonen, E. Meusel, and C.-Y. Li, "The effect of underfill and underfill delamination on the thermal stress in flip-chip solder joints," *ASME Journal of Electronic Packaging*, vol. 120, pp. 342–348, December 1998.
- [15] Anon, "Global semiconductor packaging materials outlook," tech. rep., TechSearch International, Austin, TX, 2003.
- [16] Anon, "Global semiconductor packaging materials outlook-2005 edition," tech. rep., TechSearch International, Austin, TX, 2005.
- [17] E. J. Vardaman, "Trends in semiconductor packaging materials," in *Semicon Singapore Conference*, (Suntec, Singapore), May 2008.
- [18] Anon, "Global semiconductor packaging materials outlook 2011/2012," tech. rep., SEMI and TechSearch International, 2011.
- [19] V. Gektin, A. Bar-Cohen, and J. Ames, "Coffin-Manson based fatigue model of underfilled flip chips," *IEEE transactions on components, packaging, and manufacturing technology, part A*, vol. 20, pp. 317–326, 1997.
- [20] K. Gilleo, "The chemistry and physics of underfill," in *Proc. NEPCON West*, pp. 280–292, 1998.
- [21] Z. Johnson and T. Koschmieder, "BGA underfills," *Advanced Packaging*, pp. 29–33, December 2001.
- [22] T. Braun, K.-F. Becker, M. Koch, V. Bader, R. Aschenbrenner, and H. Reichl, "High-temperature reliability of flip chip assemblies," *Microelectronics Reliability*, vol. 46, pp. 144–154, 2006.
- [23] K. Chen, D. Jiang, N. Kao, and J. Y. Lai, "Effects of underfill materials on the reliability of low-k flip-chip packaging," *Microelectronics and Reliability*, vol. 46, pp. 155–163, 2006.
- [24] http://www.tessera.com/technologies/products/z_mcp/ball_stacked.htm. Accessed on Dec. 20th 2008.
- [25] Z. Johnson, N. Schneck, A. Thoreson, and J. Stone, "Thermo-mechanical simulation of stacked chip scale packages with Moire interferometry validation," in *Proc. Tenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems ITherm '06*, pp. 1120–1125, May 30 2006–June 2 2006.
- [26] N. Schneck, Z. Johnson, C. Schaff, M. Bell, and J. Stone, "Drop testing and finite element simulation of stacked chip scale packages with and without underfill," in *Proc. 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems ITherm 2008*, pp. 853–861, 28–31 May 2008.
- [27] "Board level drop test method of components for handheld electronic products." JESD22-B111, JEDEC Solid State Technology Association, July 2003.
- [28] Anon, "IPC-9701A, Performance test methods and qualification requirements for surface mount solder attachments," 2006.
- [29] K. Brakke, *Surface Evolver Manual*. The Geometry Center, University of Illinois at Urbana-Champaign, 2003. v. 2.20i.

- [30] Z. Johnson, "Implementation of and extensions to Darveaux's approach to finite-element simulation of BGA solder joint reliability," in *49th Electronic Components and Technology Conference*, (San Diego, CA), 1999.
- [31] N. Schneek, "Drop-test reliability of the p489 ball grid array chip scale package," Master's thesis, North Dakota State University, 2008.
- [32] Anon., *ANSYS User's Guide*. ANSYS, Inc., 275 Technology Drive, Canonsburg, PA 15317.
- [33] Anon., *ANSYS LS-DYNA User's Guide*. ANSYS, Inc., 275 Technology Drive, Canonsburg, PA 15317.
- [34] Oasys USA, 155 Avenue of the Americas, New York, NY 10013.
- [35] *ANSYS LS DYN User's Guide, Release 10.0*. Canonsburg, PA., 2005.
- [36] S. Wiese and S. Rzepka, "Time-independent elastic-plastic behaviour of solder materials," *Microelectronics Reliability*, vol. 44, pp. 1893–1900, 2004.
- [37] N. Blattau and C. Hillman, "A comparison of the isothermal fatigue behavior of Sn-Ag-Cu to Sn-Pb solder." DfR Solutions.
- [38] C.-L. Yeh, Y.-S. Lai, and C.-L. Kao, "Evaluation of board-level reliability of electronic packages under consecutive drops," *Microelectronics Reliability*, vol. 46, pp. 1172–1182, 2006.
- [39] C.-L. Yeh and Y.-S. Lai, "Support excitation scheme for transient analysis of JEDEC board-level drop test," *Microelectronics Reliability*, vol. 46, pp. 626–636, 2006.
- [40] J. en Luan, T. Y. Tee, K. Y. Goh, H. S. Ng, X. Baraton, R. Bronner, and M. Sorrieul, "Drop impact life prediction model for lead-free BGA packages and modules," in *EuroSIME Conference*, 2005.
- [41] R. Darveaux, K. Banerji, A. Mawer, and G. Dody, "Reliability of ball grid array assembly," in *Ball Grid Array Technology* (J. Lau, ed.), McGraw-Hill, 1995.
- [42] R. Darveaux, "Effect of simulation methodology on solder joint crack growth correlation," in *Electronic Components and Technology Conference*, 2000.
- [43] L. Anand, "Constitutive equations for the rate-dependent deformation of metals at elevated temperatures," *ASME Journal of Engineering Materials and Technology*, vol. 104, pp. 12–17, 1992.
- [44] J. Chang, L. Wang, J. Dirk, and X. Xie, "Finite element modeling predicts the effects of voids on thermal shock reliability and thermal resistance of power device," *Welding Journal*, vol. 85, pp. 63s–70s, 2006.
- [45] J. H. Lau, ed., *Ball Grid Array Technology*. McGraw-Hill, Inc., 1995.
- [46] P. Lall, M. Shah, L. Drake, T. Moore, and J. Suhling, "Thermo-mechanical reliability management models for area-array packages on Cu-core and no-core assemblies," *SMTA*, vol. 21, no. 3, pp. 20–35, 2008.
- [47] A. Primavera and J. Pitarresi, "Measurement and prediction of reliability for double-sided area array assemblies," in *ECTC Conference*, pp. 1777–1783, IEEE, 2003.
- [48] Anon., "4 and 8 die μZ ® ball stack microelectronic packages (256 Mb DDR DRAM/1 Gb NAND flash)," reliability report ER-0489-R9999-00, Tessera Inc., 2004.
- [49] A. Syed, "simulation and life prediction of SnPb and Pb-free solder joints," in *57th ECTC Conference, Professional Development Course no. 11*, 2007.