DEVELOPMENT OF CONVECTIVE REFLOW-PROJECTION MOIRÉ WARPAGE MEASUREMENT SYSTEM AND PREDICTION OF SOLDER BUMP RELIABILITY ON BOARD ASSEMBLIES AFFECTED BY WARPAGE

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
George W. Woodruff School of Mechanical Engineering

Georgia Institute of Technology
April 2008

DEVELOPMENT OF CONVECTIVE REFLOW-PROJECTION MOIRÉ WARPAGE MEASUREMENT SYSTEM AND PREDICTION OF SOLDER BUMP RELIABILITY ON BOARD ASSEMBLIES AFFECTED BY WARPAGE

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To my father, for leading my academic path throughout all my life endeavors.

To my mother, for her eternal guidance, encouragement, and support.

To my wife, for giving me endless love, understanding, and sacrifices.

ACKNOWLEDGEMENTS

The completion of this research work requires the cooperation from many people. I would like to sincerely thank my advisor, Dr. I. Charles Ume, who gave me the great opportunity to work for this challenging project in the institute. During my four years in the graduate school, Dr. Ume provided me with invaluable advice and support in education as well as all my life. I would like to greatly appreciate his guidance with all my heart.

I would like to thank my PhD Thesis Reading Committee Members: Dr. Wayne Book, Dr. Suresh Sitaraman, Dr. C.F. Jeff Wu, Dr. Yeong Kim, and Dr. Jiahui Pan. I sincerely appreciate their time and useful inputs to make my thesis more complete.

I would also like to acknowledge Georgia Tech Center for Board Assembly Research and Packaging Research Center for allowing me access to the facilities and equipments for my test vehicle assembly and thermal cycling tests.

I would like to acknowledge mechanical engineering's machine shop for helping me with my hardware machining and manufacture.

I would like to thank my colleagues in Dr. Ume's group: Dr. Hai Ding, Dr. Reinhard Powell, Dr. Dathan Erdahl, Dr. Lizheng Zhang, Dr. Akio Kita, Dr. Bao Mi, Dr. Renfu Li, Tanvir Faisal, Jin Yang, Abel Valdes, Matthew Rogge, Tsun-Yen Wu, and Tyler Randolph for their valuable suggestions on my research work and making my experience in the graduate school more enjoyable.

I would also like to thank Dr. Wu's student Ying Hung for giving me insightful suggestions and assistance for the advanced statistical prediction modeling to correlate my experimental and finite element modeling results.

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LIST OF ABBREVIATIONS

ANOVA	Analysis of Variance
APDL	ANSYS Parametric Design Language
BT	Bismaleimide Triazine
CCD	Charge-Coupled Device
CFD	Computational Fluid Dynamics
CLPT	Classical Laminated Plate Theory
C-SAM	C-Mode Scanning Acoustic Microscope
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
DIP	Dual-In-line Package
DOE	Design of Experiment
DSP	Digital Signal Processing
FC	Flip Chip
FEA	Finite Element Analysis
GUI	Graphical User Interface
HDI	High Density Interconnect
IC	Integrated Circuit
IR	Infrared
LGA	Land Grid Array
lpi	Lines per Inch
MCM	Multi-Chip Module
MCM-D	MCM-Deposited Dielectric
MEMS	Micro-Electro-Mechanical Systems

MOEMS	Micro-Opto-Electro-Mechanical Systems
MS	Mean Squares
MSE	Mean Squared Error
MST	Micro-Systems Technology
PBGA	Plastic Ball Grid Array
PID	Proportional, Integral, and Derivative
POP	Package on Package
PTH	Plated Through Hole
PWB	Printed Wiring Board
PWBA	Printed Wiring Board Assembly
PZT	Piezoelectric Transducer
QFP	Quad Flat Package
RDRP	Ramp to Dwell, Ramp to Peak
RF	Radio Frequency
SLIM	Single-Level Integrated Module
SMA	Surface Mount Assembly
SMD	Surface Mount Device
SMT	Surface Mount Technology
SOC	System on Chip
SOP	System on Package
SS	Sum of Squares
SSR	Sum of Squared Regression Error
SST	Sum of Squared Total Error
TAB	Tape Automated Bonding
TQFP	Thin Quad Flat Package

UBM	Under Bump Metallurgy
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration
WLP	Wafer Level Packaging

SUMMARY

Out-of-plane displacement (warpage) is one of the major thermomechanical reliability concerns for board-level electronic packaging. Printed wiring board (PWB) and component warpage results from coefficient of thermal expansion (CTE) mismatch among the materials that make up the PWB assembly (PWBA). Warpage occurring during surface-mount assembly reflow processes and normal operations may cause serious reliability problems, such as severe solder bump failure, die cracking, and delamination of the solder bumps between electronic components and the PWB.

In this research, a projection moiré warpage measurement system capable of measuring the warpage of PWBs, PWBAs, and electronic packages during the convective reflow process was developed. This real-time, non-contact, and full-field measurement system was used to investigate the warpage of PWBAs assembled with chip packages during various thermal reflow processes. Based on the projection moiré system and finite element modeling (FEM), the effect of PWB warpage on solder bump fatigue reliability on board assemblies was studied.

In order to accurately simulate the reflow soldering process and to achieve the ideal heating rate of 2 °C/second, a convective heating system was developed and integrated with the projection moiré system. An advanced feedback controller was implemented to obtain the optimum heating responses using the heating system. The developed heating system has the advantages of simulating different types of reflow processes, and reducing the temperature gradients through the PWBA thickness to ensure that the projection moiré system can provide more accurate measurement results.

To simultaneously measure the warpage across the PWB and omnidirectional chip packages in a PWBA, automatic package detection and segmentation algorithms based on mask image model and active contour model (snake) were developed. They were used to detect and segment assembled packages from the PWB in a PWBA displacement image generated by the projection moiré system. The warpage of the PWB and chip packages can be determined separately irrespective of the package locations and orientations. Real-time continuous and composite Hermite surface models were constructed to estimate the PWB warpage values underneath the electronic packages.

The convective reflow-projection moiré measurement system was used to study PWBA warpage behavior during thermal reflow soldering processes. Different PWBA test vehicles were considered. The effects of package size, location, number, and different temperature profiles on PWBA warpage change were discussed in details. In addition, a repeatability study was performed to demonstrate the suitability, reliability, and repeatability of the projection moiré system for online experimental measurement.

The classical laminated plate theory was applied to study the warpage behavior of PWBs and PWBAs during the thermal reflow process. The rule of mixtures was used to estimate the effective material properties of PWBA composites. Closed form solutions of the differential equations for the PWB and PWBA deformation were generated to evaluate their warpage. The calculated warpage results were compared with experimental and FEM simulation results obtained under the same thermal loading and boundary constraints.

The effect of PWB warpage on the low cycle fatigue of the solder bumps on board assemblies was investigated using FEM and experimental study. The three-

dimensional (3-D) models of PWBAs with varying board warpage were used to estimate the solder bump fatigue life for different types of plastic ball grid array (PBGA) packages mounted on PWBs. In order to improve the accuracy of FE results, the projection moiré technique was used to measure the initial warpage of PWBs, and this warpage was used as a geometric input to the FEM. Both Sn-Pb and lead-free solder materials were used in this study. The simulation results were validated and correlated with the experimental results obtained using the projection moiré system and accelerated thermal cycling tests. Design of experiments and an advanced prediction model were generated to predict board level solder bump fatigue life based on the initial PWB warpage, package dimensions and locations, and solder bump materials.

This dissertation presents the first real-time, non-contact, and full-field warpage measurement system capable of measuring PWB/PWBA/electronic package warpage with the projection moiré technique during different thermal reflow processes. The experimental study and finite element modeling successfully document the correlation between PWB warpage and solder bump thermomechanical reliability on board assemblies.

CHAPTER 1

INTRODUCTION

Electronic packaging is a series of processes toward the end of the microelectronics manufacturing, where functional semiconductors and discrete elements are electronically interconnected and mechanically assembled. Electronic packages provide electrical as well as thermal and mechanical functions to semiconductor chips. They are the bridges that interconnect the integrated circuits (ICs) and other components into a system-level board to form electronic products. Thermomechanical reliability concerns during the assembly and the usage of electronic packages lead to the motivations and objectives of this research.

1.1. Electronic Packaging Technologies

During the past fifty years, electronic packaging technologies have been developed rapidly driven by the requirements of high-performance, low-cost, and increased reliability. To achieve high-functionality electronic products, integrated circuit (IC) technology was developed to integrate hundreds of transistors on a single semiconductor chip in early 1960s, and formed the basis of all modern electronic products. Continuous advances in reducing the size of the transistors allowed the progressive integration of up to millions of transistors on an IC, called very large or ultra large scale integration (VLSI or ULSI). Due to the lithographic technology, IC cost has sharply declined while performance has greatly improved over last 10 years. To be able to use these ICs, they have to be packaged, tested, and assembled on a system board [Tummala, 2001]. As such, the electronic package is an integral part of the

microelectronic system. It can protect, power, cool components, and provide electrical and mechanical connection between the IC chip and outside. The challenge for the packages is to provide all crucial functions required by the microelectronic devices without limiting the performance of the parts. In order to meet this challenge, the package technology has evolved from a simple metal to very complex multilayer ceramic and organic structures. As the semiconductor technology progresses towards higher level of integration, the design and production of the electronic packages becomes increasingly complex and challenging to meet the requirements of modern and future microelectronic systems.

Electronic packaging involves multiple functions at the IC level and at the system level. At the IC level, typically referred to Level 1, the packages act as IC carriers. The packages can provide the function of interconnection, power, cooling, and protection for ICs. Packaging a single IC does not generally lead to a complete system since a typical system requires a number of different active and passive devices. System-level packaging involves interconnection of all these components to be assembled on the printed wiring board (PWB). This system-level board assembly is typically referred to as Level 2 of the packaging hierarchy. By industrial requirements and standards, a single PWB may not carry all the components necessary to form the total system, since some systems require several processors to provide extremely high transactional throughputs. In such cases, connectors and cables typically connect the several PWB assemblies (PWBAs) necessary to generate the entire system. This is referred to as Level 3 of the packaging. The electronic packaging hierarchy is illustrated in Figure 1.1.

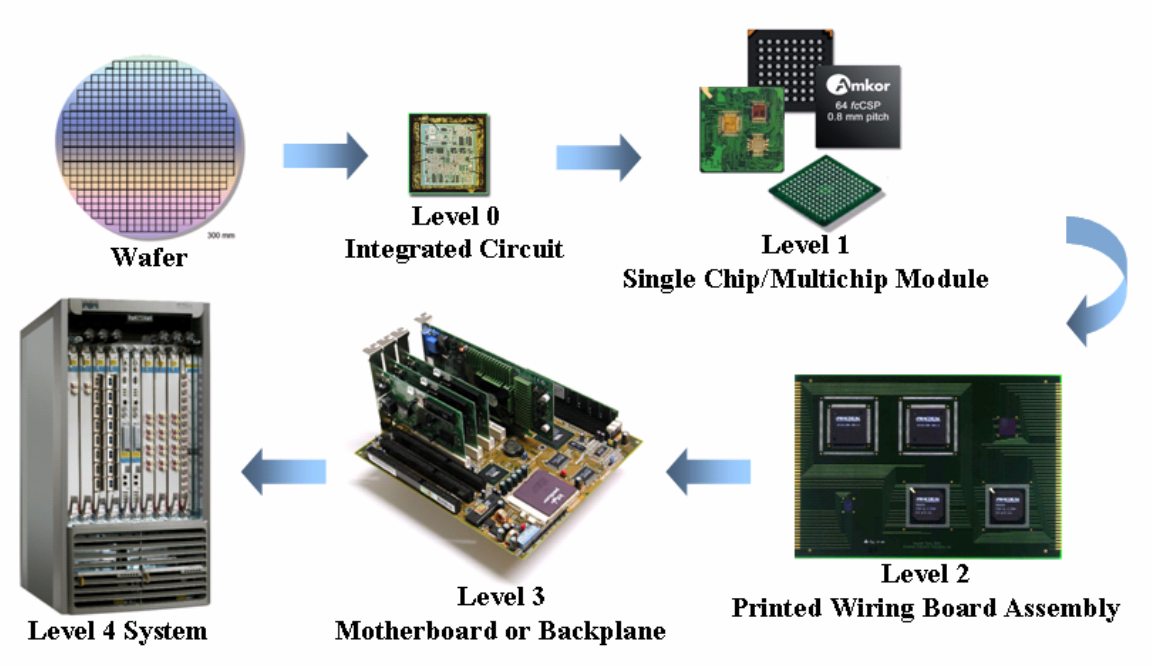


Figure 1.1. Electronic Packaging Hierarchy

Printed wiring board assembly is the process of building functional electronic systems from individual electrical packages. The assembly process involves mounting components on a PWB and soldering their leads to that board. The PWBs can not only provide electrical connections between different components, they also allow the heat generated by the packages to be transferred to the board and to be dissipated. The PWBs are the successful electrical and mechanical platforms for assembly since the introduction of semiconductors in the 1950s [Tummala, 2001].

The PWB assembly process is changing from through-hole assembly to surface mount assemble (SMA). Although both methods are widely used, the use of SMA has grown rapidly in the past decade. Size reduction of the electrical systems is the main reason for the above change. Through-hole assembly is achieved by inserting the leads of the electronic packages into plated holes in the board. While using surface mount

assembly, the packages are directly placed on the surface of the PWB. Figure 1.2 shows the typical surface mount assembly product line [Amkor, 2007].

Figure 1.2. Surface Mount Assembly Line

Surface mount assembly process includes stencil-printing solder paste to a PWB, placing the electronic components on the correct position, and then heating the entire assembly during thermal reflow soldering, so that the solder melts and forms solder bumps.

For solder-paste printing of fine pitches in industry, stencils are commonly used. A stencil is a thin sheet of metal, which has a pattern of holes through which the solder paste is pushed by a squeegee onto the desired positions on the PWB. Stencils are usually made of nickel, nickel-plated brass, stainless steel or plastic. The thickness ranges from 0.1 – 0.2 mm. Solder paste consists of small solder spheres, flux, and solvent. It is a thick gray paste with viscosity and can be divided into different types. The solder spheres are usually made of the eutectic 63Sn-37Pb alloy. Smaller solder spheres are more suitable for fine-pitch device assembly.

The pick-and-place machines are used to automatically pick up the electronic components and accurately place them at the correct position on a PWB. The mechanical and optical alignments can allow the optimal assembly. The machines used for smaller components are called chip-shooter, which have fast speed and moderate placement accuracy. The assembly machines for fine-pitch and large-sized packages have better accuracy and more flexibility, but on the other hand, they are slower and more expensive. The component feeders are mounted on a moving carriage, which can transports the next electronic component to be picked up by the pick-and-place machine.

The process of soldering can provide good electrical, mechanical, and thermal connections between the components and the PWB. All solder connections must indicate good wetting and adherence to the pads on the PWB. The amount of solder attaching the components to the board has significant impact on the reliability of the solder bumps.

Metal alloys used for solder bumps include combinations of tin (Sn), lead (Pb), silver (Ag), copper (Cu), and etc. The commonly used alloy is tin-lead (63%Sn-37%PB), because of its low cost, low melting temperature (183 °C), proven reliability and ability to join common assembly metals. The 63Sn-37Pb is a eutectic alloy, meaning that the transition between the solid state and the liquid state occurs over a very narrow temperature range. However, lead causes severe health problems. In order to eliminate the lead poisoning, lead-free alloys are developed to replace the eutectic solder 63Sn-37Pb. The most promising alloy that can be used as a lead-free solder is Sn-Ag-Cu or Sn-Ag alloys. These candidates have been shown to have similar or higher reliability, solderability, and durability than Sn-Pb. In particular, 95.5Sn-3.8Ag-0.7Cu alloy has a low melting point of 217 °C, with a small plastic range. It has demonstrated superior

tensile and compression strength compared to Sn-Pb alloy when subjected to thermal cycling tests.

Normally the SMA soldering process is achieved using a conveyorized thermal reflow oven. Different types of the reflow processes are used in industry including infrared (IR) reflow, vapor-phase reflow, in-line conduction reflow, hot-bar reflow, laser reflow, and forced-convection reflow [Lee, 2002].

Infrared reflow uses IR heating to heat the PWBAs during the reflow process. The IR heater emitter panels and elements are located in the temperature zones of the reflow oven to generate the infrared radiation heat. The temperature profile of the PWBAs can be determined by zone temperature and conveyor speed. IR heating can provide rapid heat transfer with low cost equipments. However, it may cause non-uniform heating for the PWBAs due to the color sensitivity of infrared radiation and assembly structures.

Vapor-phase reflow provides heating with the vapor of a fluorocarbon fluid which is boiled until reaching the vapor state. The reflow soldering temperature is the boiling point of the fluorocarbon fluid. A vapor-phase reflow oven consists of a preheat zone containing IR emitters before the PWBAs enter the vapor zone. The temperature profile of the PWBAs is determined by the vapor temperature, IR heater settings, and conveyor speed. Although the vapor-phase reflow can provide rapid uniform heating for the assemblies, it may cause thermal shock and damage the electronic components.

In-line conduction reflow applies a series of heated surfaces to heat the PWBAs. The assemblies directly contact with the heated surfaces, and are transferred from one surface to the next with a conveyor. The temperature of the heated surfaces and the conveyor speed determine the temperature profile of the PWBAs. In-line conduction

reflow is suitable for high temperature PWB materials such as ceramics. But it is not suited for epoxy boards and cannot reflow double-sided boards.

Hot-bar reflow provides a resistance soldering device, in which the electrode is made out of molybdenum through which an electric current is passed. The heat can be applied to the electrode either continuously or in a pulse form.

Laser reflow uses a laser to heat the PWB assemblies. It is suitable for heat sensitive PWBAs and densely electronic packages due to localized heating. But if the laser energy is too high, it may cause a number of defects such as solder charring and balling.

Forced convective reflow is the most commonly used reflow method in industry. Forced convective heating is able to provide uniform heating to minimize component cracking. But the convective heating transfer rate is slow, because the heater needs to heat the gas, and then transfer heat to the PWBAs through the gas. Typically the applied gases are air and nitrogen. Using nitrogen can reduce the formation of metal oxides to obtain good flux. Figure 1.3 shows a convective reflow oven used in industry [Research International, 2007]. Figure 1.4 shows different controlled temperature zones and reflow patterns inside the force convective oven. Each zone is kept at a specific temperature. The PWBAs are heated from both the top and bottom sides in the oven. The temperature profile on the PWBAs can be determined by the zone temperatures and the speed of the conveyor.

Figure 1.3. DeltaFlo 10LN Convective Oven

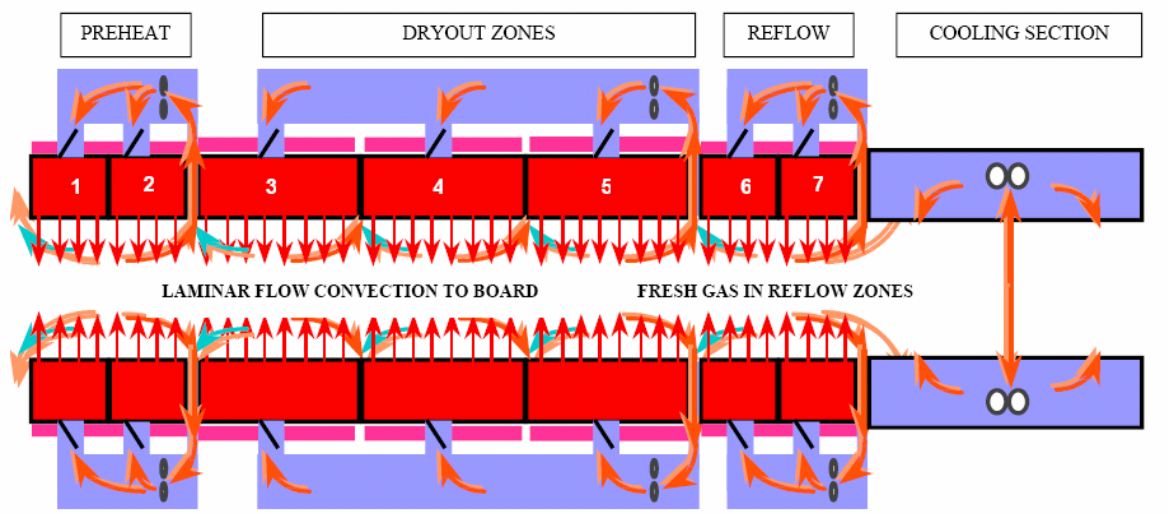


Figure 1.4. Forced Convective Reflow Patterns

The advantages of the surface mount technology are that the electronic components have smaller pitches than through-hole components; they do not use as much area on the topside, and do not use any area inside, or on the bottom-side of the PWB. The typical surface mount electronic packages include quad flat pack (QFP) packages, plastic ball grid array (PBGA) packages, and chip scale packages (CSPs). The PBGA packages utilize small solder balls for the connection between the components and the PWB. The solder balls provide a shorter electrical path and cause less degradation of the

signal, improving the overall performance of the circuits. The IC chip in a PBGA package can be interconnected to the package by wirebonding or flip chip technology. Figure 1.5 shows the thin quad flat pack (TQFP) package components and PBGA package components [Amkor, 2007].

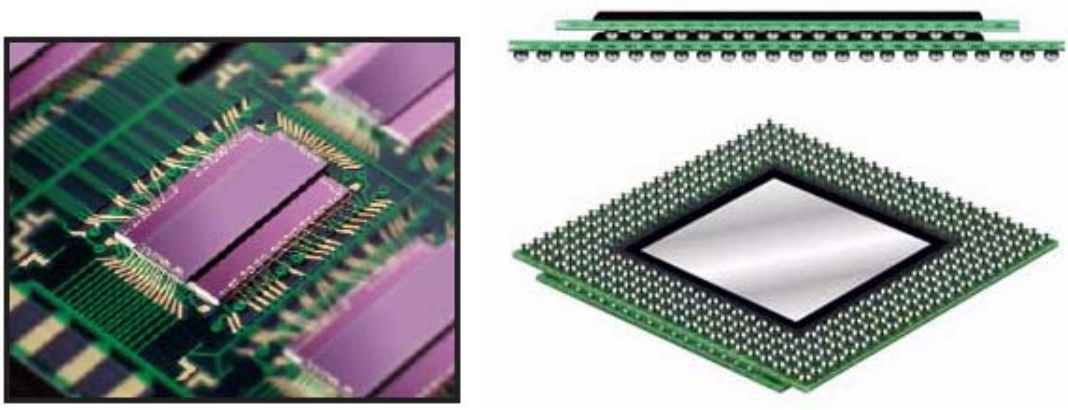
(a) (b)

Figure 1.5. (a) TQFP Packages; (b) PBGA Packages

A chip scale package (CSP) is defined as having a size that is a maximum of 1.2 times the size of the IC chip packaged. The CSPs can be well manufactured in the BGA format or the land grid array (LGA) format. The LGA has bare solder pads on the bottom side of the package. Flip chip and wirebonding techniques are both commonly used to build a CSP component.

Three-dimensional (3-D) packaging technologies exploit the third or Z height dimension to provide a volumetric packaging solution for higher integration and performance of electronic components. 3-D packages are able to provide multiple system level benefits including: reducing size and weight through increasing semiconductor

functions per unit area of PWBs; allowing more design freedom to create new volumetric packaging approach; Enabling higher electrical performance with shorter interconnect architectures with stacking; reducing system level costs. Current 3-D packages involve die stacking and package stacking technologies. Based on the die stacking technology, dies can be reliably stacked and interconnected with up to 9 stacks high, employing leading edge die attach, die spacing, wirebonding, and flip chip assembly capabilities. Die stacking is widely deployed in conventional leadframe-based packages such as QFP and CSP formats. Stacking of fully assembled and tested packages can help to overcome the technical limitations associated with complex die stacks. The package on package (POP) stacking technique has been widely used in digital camera, cell phone, and flash memory applications with stacking up to 8 packages high. Figure 1.6 shows a die-stacked CSP and a package-stacked PBGA package [Amkor, 2007].



(a) (b)

Figure 1.6. (a) Die-Stacked CSP Package; (b) Package-Stacked PBGA Package

As electronic packaging technology evolved from simple dual-in-line packages (DIPs) to more advanced and complex structures such as 3-D stacked packages, the reliability of electronic components and electronic assemblies has become a significant concern in the manufacturing industry.

1.2. Thermomechanical Reliability in Electronic Packaging Manufacturing

The reliability of electronic packaging is defined as the probability that this packaging will be operational within acceptable limits for a given period of time. Failure mechanisms in an electronic package may be caused by thermomechanical, electrical, chemical, or environmental mechanisms. In thermomechanical reliability analysis, the focus is on the failures caused by temperature loading conditions that electronic packages experience during manufacturing and service operations [Tummala, 2001]. Thermomechanical failure of electronic packages is usually associated with material failure in the form of plastic deformation, fatigue, voids, creep, delamination, fracture, etc. Figure 1.7 below shows some common failure modes of a flip-chip plastic ball grid array (FC-PBGA) package. The failure modes mainly come from the thermal mismatch between the various materials with different coefficients of thermal expansion (CTEs) in the package. Due to the thermal mismatch, significant thermal residual stresses may be generated after assembly and cause reliability problems. In this research, out-of-plane displacement (warpage) of printed wiring boards (PWBs), electronic packages, and printed wiring board assemblies (PWBAs) will be focused and investigated.

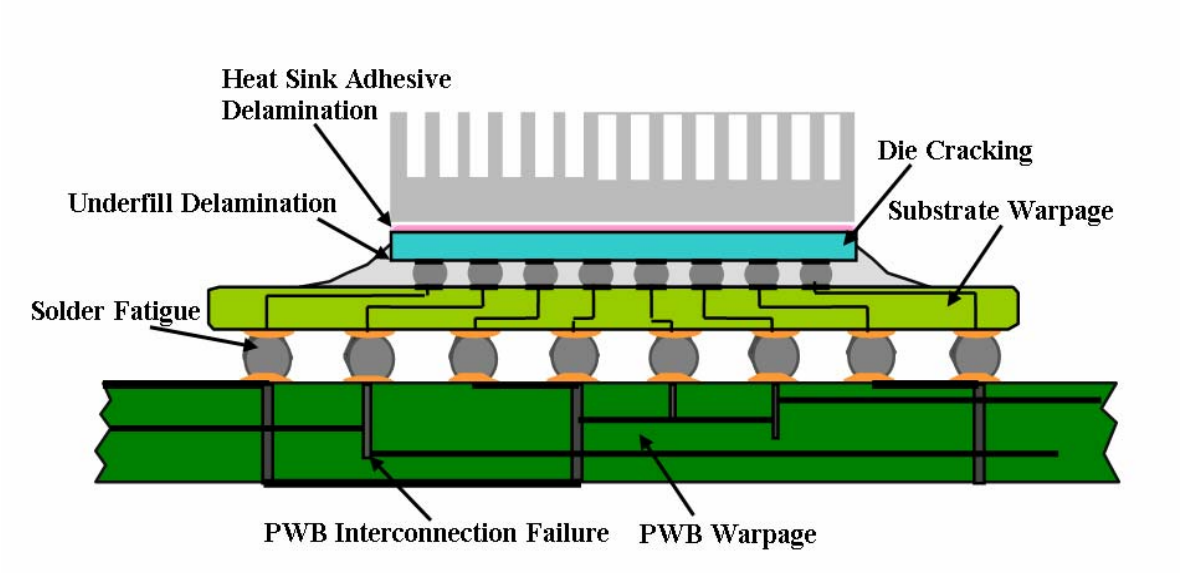


Figure 1.7. Common Failure Modes of FC-PBGA Package

Warpage is a major thermomechanical reliability concern for board-level electronic packaging. PWB and component warpage results from coefficient of thermal expansion (CTE) mismatch among the materials that make up PWBAs such as solder, copper, FR-4, encapsulation molding, and silicon. In addition, material elastic modulus, the thickness of PWBs and electronic packages, temperature loading conditions, and PWB boundary constrains have significant effects on the warpage of PWBs and assembled packages. Warpage occurring during surface-mount assembly reflow processes and normal operations may lead to severe solder bump fatigue failure, die cracking, component misregistration, and delamination of the solder bumps between electronic components and the PWB [Yeh et al., 1993]. Figure 1.8 shows a solder bump fatigue failure of PBGA package [Ejim, 1998]. Figure 1.9 depicts a die cracking in cross section and C-mode scanning acoustic microscope (C-SAM) [Wakharkar et al., 2005]. Figure 1.10 displays the component misregistration between a PBGA package and the

PWB [Asktechnology, 2006]. Figure 1.11 illustrates the delamination of interconnected solder bumps in C-SAM [Wakharkar et al., 2005].

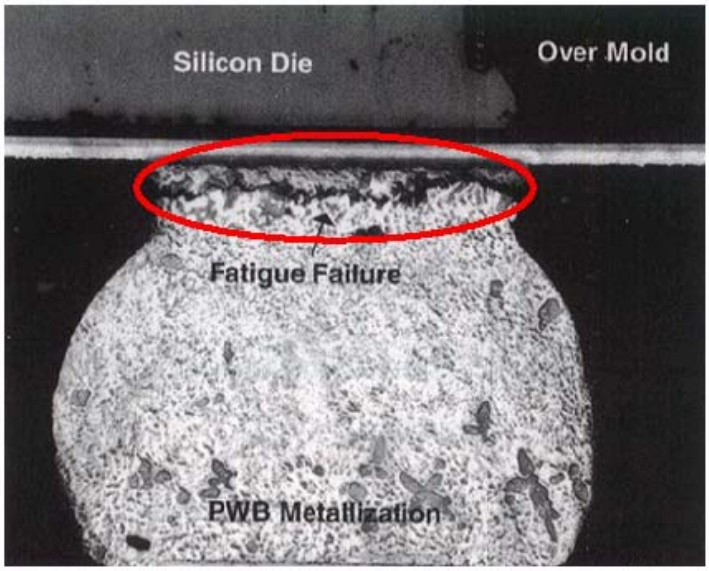
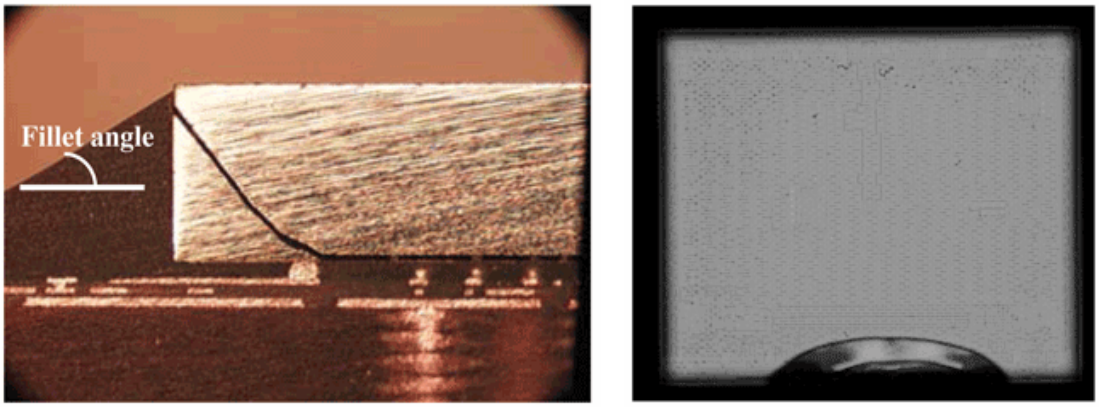


Figure 1.8. Solder Bump Fatigue Failure of PBGA Package



(a) (b)

Figure 1.9. Die Cracking in (a) Cross-Section and (b) C-SAM

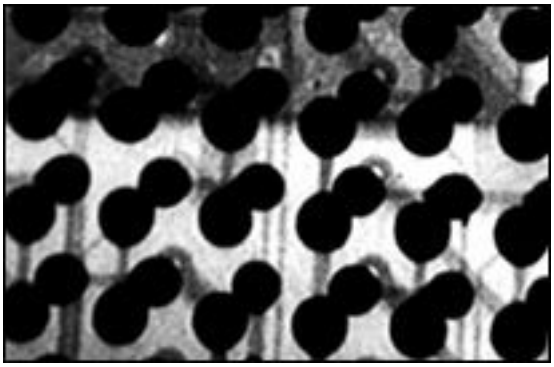


Figure 1.10. Misregistration between PBGA and PWB

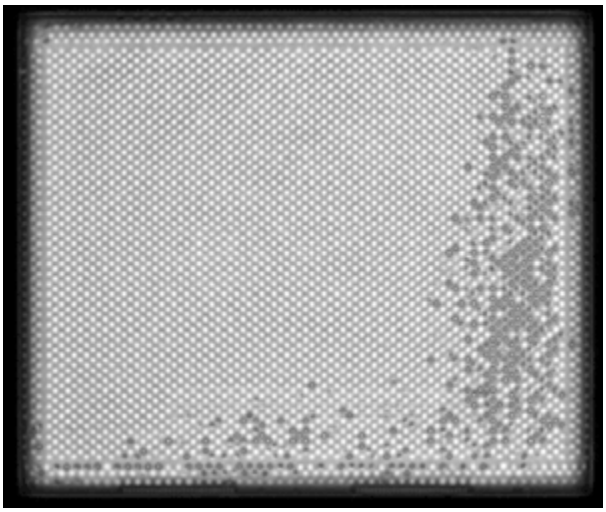


Figure 1.11. Delamination of Solder Bumps in C-SAM

As the electronic packaging industry continues to move towards the productions of thin PWBs, high density PWBAs, miniature electronic components, and 3-D stacked dies and packages, measurement and reduction of warpage become more significant and necessary in order to estimate and improve the reliability of electronic packaging in high volume manufacturing.

1.3. Research Objectives

In this research, an automatic real-time warpage measurement system with projection moiré and shadow moiré techniques was developed and implemented. The goal is to make the system versatile to simulate industrial assembly reflow processes, improve the system precision and reliability, measure and analyze the warpage of PWBs and different types of assembled electronic packages, accurately estimate PWB and PWBA warpage with the classical laminated plate theory, and provide valid numerical models to study the correlation between PWB warpage and solder bump failure on board assemblies. More specifically, the research objectives are:

I. To redesign and improve the convective heating system for use with the projection moiré and shadow moiré warpage measurement system. In order to successfully simulate any reflow soldering process and achieve the ideal heating rate of 2 °C/second, the convective heating system needs to be redesigned and implemented. More power will be supplied to the heaters; the heater surface area will be increased; and the system volume will be decreased. The PID controller for the heating system will be modified to obtain the optimal heating responses. The novel forced convective heating system will be integrated and implemented with the current warpage measurement system.

II. To separately measure the warpage across the PWB and omnidirectional chip packages in a PWBA, the automatic package detection and segmentation algorithms will be developed for the projection moiré measurement system. The current post-processing algorithm using active contour model (snake) has some limitations. It works only for up to two chip packages, and the package edges

must be in the horizontal and vertical directions with respect to the PWB edges. The algorithm cannot obtain accurate results if the maximum or minimum PWB warpage occurs directly underneath the packages of interest. In order to improve the post-processing algorithm, a novel segmentation algorithm based on mask image model will be developed. This approach will result in higher resolution and processing rate compared with the original algorithm using the snake model. Also, the snake algorithm will be improved so that both segmentation algorithms can be used to evaluate the warpage of the PWB and electronic packages in a PWBA separately irrespective of package locations and orientations. A real-time continuous and composite Hermite surface model will be generated to obtain accurate warpage results for the PWB areas underneath chip packages.

III. To utilize the convective reflow-projection moiré measurement system to study warpage of PWBA test vehicles. Based on the integrated warpage measurement system with the novel convective heating system and automatic package segmentation techniques, the warpage of PWBA test vehicles will be measured using the projection moiré technique during simulated thermal reflow processes, including typical and other type of convective reflow processes. Real-time measurement results will be compared and analyzed for different configurations.

IV. To apply the classical laminated plate theory to study the warpage behavior of PWBs and PWBAs during the simulated thermal reflow process. The rule of mixtures will be used to estimate the effective material properties of PWBA composites. Closed form solutions of the differential equations for the PWB and PWBA deformation from the classical lamination theory will be generated to

evaluate warpage. The board support conditions and thermal gradients through the sample thickness will be considered in the analytical models. In order to validate the above models, the calculated warpage results will be compared with experimental and numerical warpage values. The real-time warpage of PWB and PWBA samples will be measured using the projection moiré measurement system during a simulated convective reflow process. Finite element modeling (FEM) will be applied to estimate the sample warpage values under the same thermal loading and boundary constraints.

V. To study the effect of PWB warpage on the low cycle fatigue of solder bumps on board assemblies. Finite element modeling (FEM) is used for the strain-based life prediction of solder bumps on board assemblies. 3-D models of PWBAs with different board warpage are used to estimate the solder bump fatigue life for different types of packages on PWBs. In order to improve the accuracy of FE results, the initial warpage of PWBs will be measured by the projection moiré method, and used as a geometric input to the FEM. The PWBAs with known PWB warpage will be modeled to determine the influence of various levels of initial PWB warpage on the low cycle fatigue failure of solder bumps. The effect of different types of PBGAs with varying locations on solder bump fatigue will be studied. Both Sn-Pb and lead-free solder will be used in this study. Corresponding experimental accelerated thermal cycling tests will be performed to validate and correlate the simulation results. Design of experiments and an advanced prediction model will be developed in order to investigate the correlation between PWB warpage and solder bump thermal fatigue reliability on board assemblies.

Following this introduction, the literature relevant to the research objectives is reviewed in Chapter 2. The design and development of the convective heating system to accurately simulate the convective reflow process is discussed in Chapter 3. The development and improvement of the projection moiré post-processing algorithms is presented in Chapter 4. The performances of the two segmentation approaches based on their resolutions, processing rates, and measurement efficiencies are evaluated in this chapter. The experimental study on warpage behavior of the PWB assembled with different electronic packages will be discussed in Chapter 5. The effect of various thermal reflow processes on PWBA warpage will be included in this chapter. The theoretical analysis on the PWB and PWBA warpage based on the classical laminated plate theory will be investigated in Chapter 6. The effect of PWB warpage on the solder bump thermomechanical reliability on board assemblies will be studied in Chapter 7. Design of experiments and an advanced prediction model will be developed to investigate the correlation between PWB warpage and solder bump fatigue reliability based on the FEA solutions and experimental results. Conclusions, technical contributions, and recommendations for future work are presented in Chapter 8.

CHAPTER 2

LITERATURE REVIEW

Many researches have been performed to investigate the warpage of printed wiring boards (PWBs), printed wiring board assemblies (PWBAs), and electronic packages. An overview of the methods used to measure the warpage across PWBs, PWBAs, and electronic packages is presented in this chapter. In addition, the literature related to the correlation between warpage and solder bump reliability on board assemblies is reviewed.

2.1. Warpage Measurement

Warpage, also called out-of-plane displacement or flatness, is one of the major reliability concerns when stacking layers of different materials with distinct thermal and mechanical properties into a confined space. The thermal reflow soldering processes and normal temperature cycling can further aggravate the warpage of electronic packaging and assemblies. The PWB/PWBA warpage may lead to serious reliability problems and manufacturing difficulties, such as severe solder bump fatigue failure, die cracking, delamination, and misregistration of electronic components. Warpage can be measured by many different optical techniques such as profilometry, interferometry and moiré methods.

Profilometry can measure the sample surface profile by using a stylus or a laser to determine the warpage based on the depth deflection or laser's reflection at every point on the sample surface with respect to a reference point [Yeung & Yuen, 1996; Tee et al., 2001]. Profilometry method can provide high resolution results. However, the approach

has difficulty to measure the full-field surface topology, and not suitable for online use [Teng et al., 1996].

Interferometry method can be used to measure PWB sample warpage by splitting a continuous laser beam. One split beam is a reference, and the other beam is reflected from the sample surface and combined with the reference beam to create interference [Czarnek, 1990]. The PWB surface topology can be determined based on the interference pattern. Figure 2.1 shows an optical schematic of the interferometry technique used to measure the sample surface structure [Wyant, 2004]. The widely used interferometry methods include holographic interferometry, Twyman-Green interferometry and far infrared Fizeau interferometry. The advantages of the interferometry methods are that they can produce high resolution which is comparable to the wavelength of light, and they are non-contact methods [Qing et al., 1997; Tsai et al., 2004]. However, above methods can only be used to measure small samples such as flip chips; their optical setups are very complex, expensive, sensitive to noise, and unsuitable for full-field online use due to their limited sample applications [Verma & Han, 1998; Verma et al., 2001].

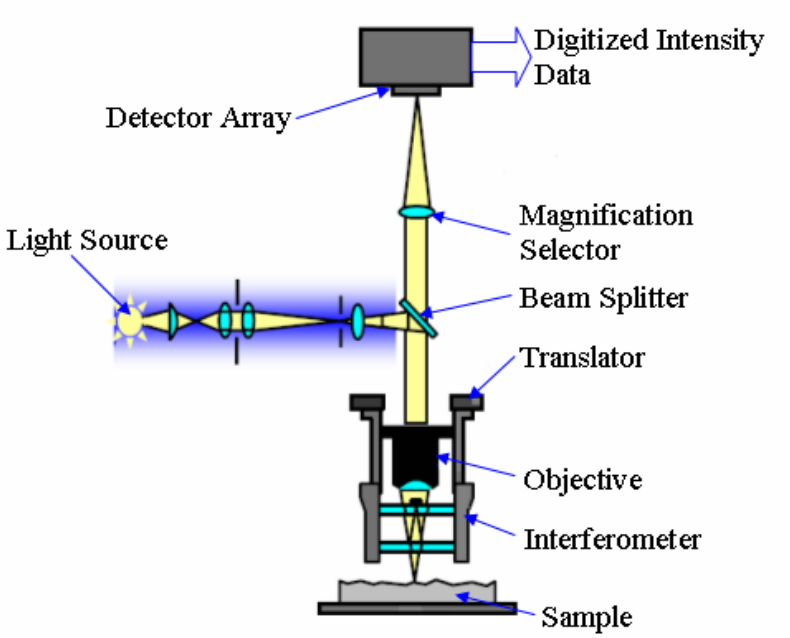


Figure 2.1. Optical Schematic of Interferometry Technique to Measure Surface Structure

Moiré methods have many advantages over profilometry and interferometry methods, and have emerged as real-time, non-contact, full-field, and superior techniques with high performance-to-cost ratio to measure sample warpage [Yeh et al., 1991; Yeh &Ume, 1993; Dang et al., 2000]. In this research, the shadow moiré and projection moiré warpage measurement methods are used [Ding et al., 2002; Ding et al., 2003].

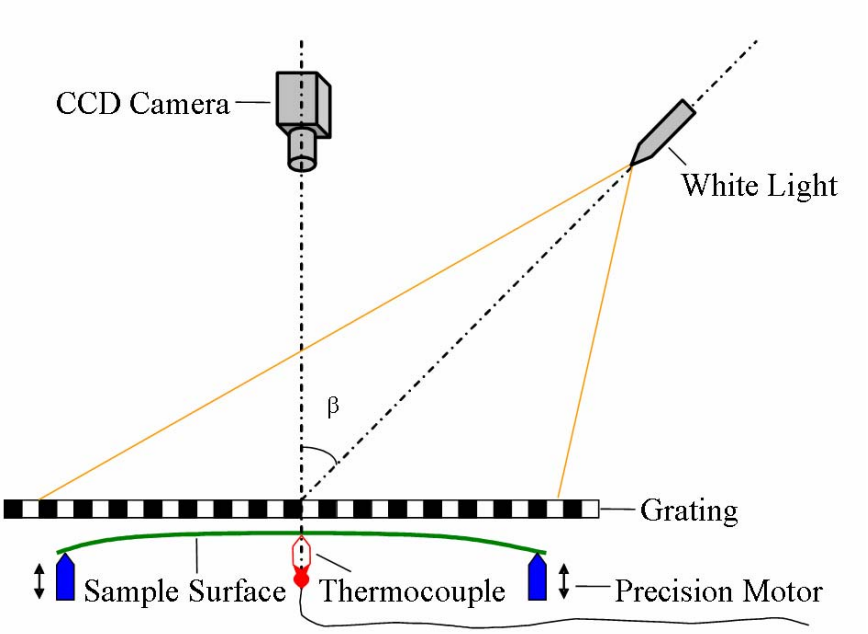


Figure 2.2. Shadow Moiré Optical Setup

The shadow moiré technique is a non-contact, full-field, and real-time warpage measurement method. The corresponding optical setup is shown in Figure 2.2. The shadow moiré fringe pattern can be generated by superposing two periodic images. One of the periodic images comes from a glass grating, and the other is the shadow of the grating lines which is generated by the white light source on a surface being measured. Small variations between the measured surface and the reference glass grating are magnified by moiré fringes and give a quantitative measurement of surface topology. The CCD camera can capture the moiré images and send them to a computer to calculate out-of-plane displacement with respect to the reference grating [Ding et al., 2002]. Precision motors connected to the sample holder can move the surface up and down and give a high resolution for phase stepping. Thermocouples are used to measure the temperatures of different locations on the sample in real-time thermal processes. The resolution of the

shadow moiré technique is equal to the pitch of the glass grating lines when $\beta = 45°$. The phase stepping technique can be used to increase the resolution by about 100 times.

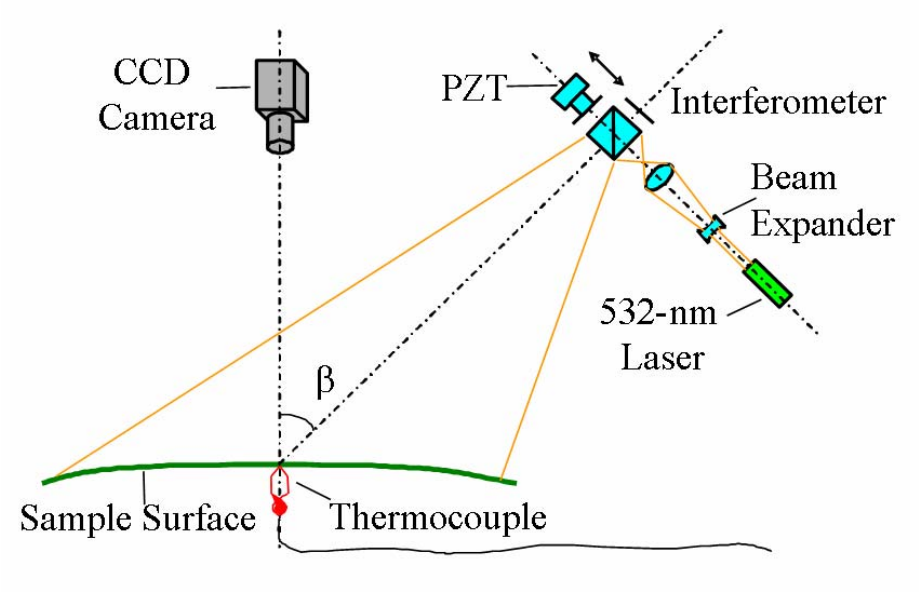


Figure 2.3. Projection Moiré Optical Setup

The projection moiré technique is also a non-contact, full-field, and real-time measurement method which uses similar moiré fringe pattern as the shadow moiré method. The main difference between the two moiré techniques is that the projection moiré technique uses a laser and an interferometer to generate periodic structures on the sample surface instead of a glass grating. The projection moiré optical setup is shown in Figure 2.3. A diode-pumped laser with a wavelength of 532 nm is expanded and then enters a Michelson interferometer. The interferometer's reference mirror is mounted on a piezoelectric transducer (PZT) for phase stepping, as do the precision motor in the shadow moiré method. Two projected grating images captured by a CCD camera at different time will be superposed to obtain moiré fringes and calculate surface topology

by computer. One image is the reference grating pattern captured when the grating lines are projected onto a flat reference surface, and the other image includes the deformed grating lines created by the sample surface being measured [Ding et al., 2003]. The resolution of the projection moiré system depends on the surface size being measured. Normally the CCD camera with 480 by 512 pixels can resolve 100 fringes in its full field. The four-step phase stepping technique can increase the measurement resolution by about 100 times. Therefore, if a sample surface has the size of L by L being evaluated, the resolution of the projection moiré measurement system is L/10,000.

The shadow moiré and projection moiré warpage measurement methods are complementary to each other. For PWBs without assembled packages, the shadow moiré technique is a good choice due to its higher resolution; for PWBs assembled with electronic components, the projection moiré technique should be chosen, because no glass grating is needed.

For both the shadow moiré and projection moiré warpage measurement techniques described above, warpage is calculated using Equation 2.1.

$$w = \frac{np}{\tan\alpha + \tan\beta} \tag{2.1}$$

where, w = out-of-plane displacement at the nth fringe order

n = fringe order

p = grating pitch

α = observation angle

β = illumination angle

For both the shadow moiré and projection moiré setups described above, the observation angle, α, is 0°, and the illumination angle, β, is 45°. The fringe order, n, is not required to be an integer, and can be determined by counting the fringes from the zeroth-order fringe in a moiré image. In order to obtain accurate warpage measurement results, the phase stepping method is applied to achieve precise fringe orders [Ding et al., 2002]. Then the warpage of the sample surface can be calculated.

The phase stepping method is able to increase the resolution of warpage measurement by about 100 times. Three-step and four-step phase stepping are the commonly used phase stepping methods. In this research, the projection moiré measurement system employs four-step phase stepping. The PZT moves the reference mirror of the Michelson interferometer back and forth so that the phase of four moiré images is changed by π/2 consecutively as shown in Equation (2.2).

$$\varphi(x,y) = \arctan\left(\frac{I_{3(x,y)} - I_{1(x,y)}}{I_{0(x,y)} - I_{2(x,y)}}\right) \tag{2.2}$$

where, $\varphi(x,y)$ = moiré fringe phase

$I_i(x,y)$ = light intensity at pixel (x,y) for image i

After calculating the phase using Equation (2.2), Equation (2.3) is used to determine the fringe order, n.

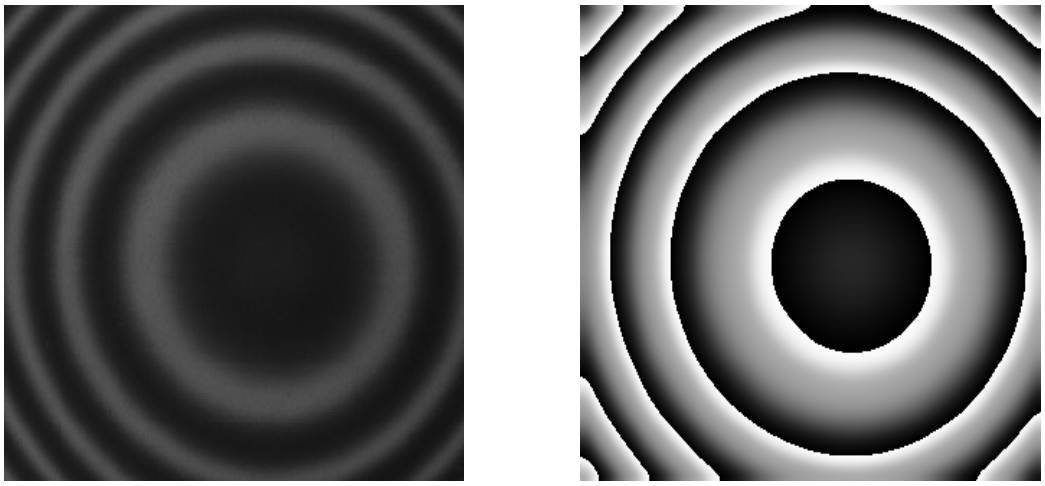
$$n = \frac{\theta(x,y)}{2\pi} \tag{2.3}$$

where, $\theta(x, y)$ = moiré fringe phase value after $\varphi(x, y)$ is made to vary between 0 and 2π (phase correction) and subsequently removing the 2π discontinuities (phase unwrapping).

The above process of computing phase using phase stepped images as shown in Equation (2.2) is called phase wrapping. Figure 2.4 shows a moiré fringe pattern and its corresponding wrapped phase image. The $\varphi(x, y)$ term computed using Equation (2.2) will vary between $-\pi/2$ and $\pi/2$. In order to obtain the correct fringe order, n, using Equation (2.3), the $\varphi(x, y)$ term need to vary between 0 and 2π. The process of transforming the phase image to vary between 0 and 2π instead of varying between $-\pi/2$ and $\pi/2$ is called phase correction. Then the phase unwrapping method is used to remove the 2π discontinuities.

There are many different phase unwrapping methods available. A method developed by Itoh can be used to unwrap a simple phase image by using a 1-D approach multiple times to cover a 2-D image [Itoh, 1982]. For any row or column that is N points long in a phase image, the unwrapped phase can be calculated from the wrapped phase. However, Itoh's method fails to correctly unwrap the complex phase images encountered in this research. Residues will be caused by shadows, noise, and contact of the sample and the glass grating for the shadow moiré system. Goldstein's method can be applied to unwrap such complex phase images by connecting adjacent pairs of residues [Goldstein et al., 1988]. The surface plot unwrapped by Goldstein's method still has discontinuous regions in some cases. The mask cut method is an improved unwrapping approach based on the Goldstein's method [Flynn, 1996]. It applies a mask image to prescribe how

residues are connected and then to obtain clean unwrapped surface plots for moiré warpage measurement systems.



(a) (b)

Figure 2.4. (a) Moiré Fringe Pattern; (b) Wrapped Phase Image

After phase unwrapping, the out-of-plane displacement, *w*, can be calculated from Equation (2.1) for different points on the PWBA sample surface. These calculated out-of-plane displacement values need to be rotated in order to obtain an accurate maximum warpage value for the test sample. The maximum warpage of a PWB is calculated by taking the difference between the maximum and minimum out-of-plane displacements on the PWB. For the board warpage calculation, the out-of-plane displacements are referenced from the lowest point on the PWB in the out-of-plane direction. Maximum warpage of a PWBA is calculated by taking the difference between the maximum and minimum out-of-plane displacements on the PWBA. For the assembly warpage calculation, the out-of-plane displacements are referenced from the lowest point on the PWBA in the out-of-plane direction. Maximum electronic package warpage is defined as

the difference between the maximum and minimum out-of-plane displacements on the electronic package. The out-of-plane displacements are referenced from the lowest point on the electronic package in the out-of-plane direction, not including the solder bumps.

Rotation of the out-of-plane displacement values eliminates rigid-body rotation. It allows maximum warpage comparison of differently oriented sample surfaces. As illustrated in Figure 2.5(a), the maximum warpage calculation is not unique when rigid-body-motion is present. When the characteristic plane of the surface is rotated to be horizontal as shown in Figure 2.5(b), a unique maximum warpage is identified. The characteristic plane can be calculated using different methods. The least square best surface fit is a common method to represent the characteristic plane of the out-of-plane displacement values. After the characteristic plane is obtained, it is subtracted from the sample surface so that the characteristic plane becomes horizontal which in turns produces a unique maximum warpage result [Ding, 2003; Powell, 2006].

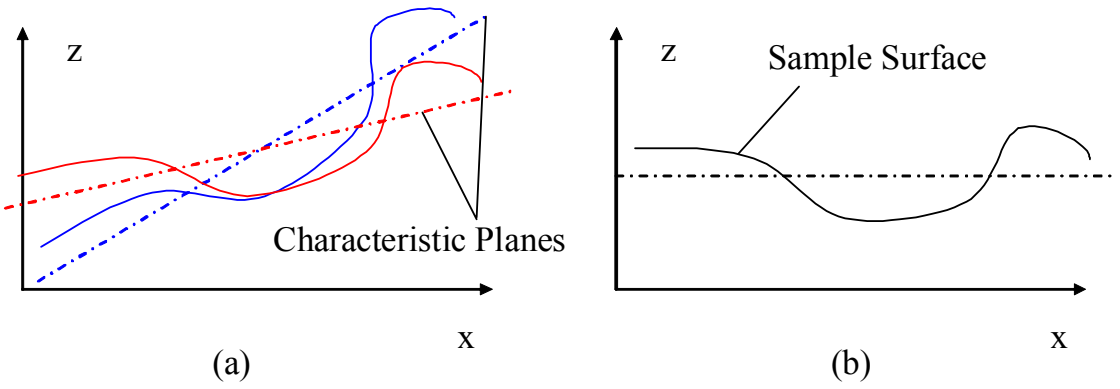


Figure 2.5. (a) Surface before Image Rotation; (b) Surface after Image Rotation

2.2. Warpage Measurement of Printed Wiring Boards

Thermally induced warpage of printed wiring boards has been investigated based on many different analytical and experimental approaches [Yeh et al., 1991]. The shadow moiré technique was determined to be the best method to measure PWB warpage. In order to determine whether the PWB material properties have significant effects on the PWB warpage, sensitivity analyses were conducted using FE analysis. The FE results showed that CTE is the most influential material property followed by Young's modulus and layer thickness [Yeh & Ume, 1993]. PWB warpage has been measured under a simulated wave soldering process using a novel effective warpage measurement system presented by Stiteler and Ume [Stiteler et al., 1996; Stiteler & Ume, 1997]. PWB warpage was compared due to simulated infrared and wave soldering processes. The results showed that higher warpage occurred on the PWBs heated using the simulated wave soldering process than boards heated using the simulated infrared soldering process. The difference between the two processes was due to the significantly higher through-thickness temperature gradient on the PWB during the simulated wave soldering process [Polsky et al., 2000]. In order to measure PWB warpage during forced convective reflow processes, a warpage measurement system with shadow moiré and projection moiré techniques was designed and developed [Powell & Ume, 2005]. The effects of moisture and gradual heating on warpage of high density interconnect (HDI) PWBs were studied using the shadow moiré technique. The results showed that moisture has effect on warpage and thicker HDI boards experience less warpage than the thinner counterparts [Petriccione & Ume, 1999]. The PWB warpage due to the solder masking process was investigated based on FE analysis. The study showed that using solder mask thicker than

1.1 mils results in lower warpage. Less warpage results can be obtained when the solder mask of the same thickness is applied to both sides of the PWB. CTE of the solder mask have the most significant effect on the PWB warpage followed by Young's modulus and Poisson's ratio, and the influential material properties affect thinner PWBs much more than thicker boards [Ume et al., 1997; Ume & Martin, 1997].

The temperature dependent materials of PWBs were characterized and used to predict PWB warpage during heating processes in FE analysis. The simulation results were compared with the shadow moiré experimental measurements to show the importance of using temperature dependent material properties in FEM [Fu & Ume, 1995]. The thermoelastic lamination theory was applied to predict the warpage of PWBs with and without traces during thermal cycling and infrared reflow. The warpage predicted by the analytical model was compared with the warpage measurements obtained using the shadow moiré technique. The study showed that the thermoelastic lamination theory model can be used to predict PWB warpage below the glass transition temperature, T_g, of FR-4. Above the T_g of FR-4, viscoelastic relaxation may be present [Polsky et al., 1998; Polsky & Ume, 1999]. The linear viscoelastic theory and classical lamination theory were also applied to predict the surface warpage in multidirectional woven-glass/epoxy laminates. The predicted results agreed well with the warpage measurements using a projection moiré method [Wang et al., 1992].

The effect of warpage on next generation high-density wiring substrates was studied. The substrates with high stiffness in addition to low CTE were necessary for reliability requirements [Banerji et al., 2002]. A process modeling methodology was developed to monitor the warpage and stresses during sequential multilayered substrate

fabrication. The model was validated by the shadow moiré experimental results. The study demonstrated that it was significant to incorporate viscoelasticity into the model in order to accurately predict the warpage of the substrate [Dunne & Sitaraman, 2000].

In this study, a convective heating system will be developed and integrated with the current shadow moiré and projection moiré warpage measurement system. The developed heating system has the advantages of simulating different types of reflow soldering processes, and reducing the temperature gradients through the thickness of PWBs and PWBAs so as to assist the moiré system to obtain more accurate warpage measurement results.

2.3. Warpage Measurement of Printed Wiring Board Assemblies & Chip Packages

The warpage of PWBs with surface mount components was studied using the shadow moiré technique with variable sensitivity [Han et al., 1993]. However, the shadow moiré method can only be used to measure local warpage and not global warpage of PWBAs. The warpage of PWBAs, consisting of J-leaded plastic leaded chip carriers (PLCCs), was investigated during IR reflow soldering based on FEM. After the reflow process, the formed solder bumps increased the stiffness of PWBAs, and the PWB warpage resulted in gaps at the lead-solder pad interface [Mittal et al., 1996].

The projection moiré technique is more suitable to measure the warpage of a PWB surface with assembled components. The technique was compared with the shadow moiré method at room temperature. The results showed that the two measurement techniques complement each other. A high quality warpage measurement system should incorporate both measurement techniques [Ding et al., 2002]. The projection moiré technique has been used to study the warpage of PWBAs such as a computer

motherboard and a communication base station module. The capability of the projection moiré measurement system was fully demonstrated [Ding et al., 2003]. In order to use the projection moiré system to accurately and separately determine the warpage of a PWB and chip packages in a PWBA, an automated image segmentation algorithm, based on active contour model (snake), was developed and applied to detect package locations in a displacement image of the PWBA. The snake can converge onto the edges of packages in an image after automatically constructed around the edges of interest. The automatic package detection algorithm allowed the projection moiré system to measure the warpage of PWBs and packages simultaneously and individually [Powell & Ume, 2006].

To predict PWBA warpage, an FE modeling methodology was developed based on modularized, parametric, and effective modeling schemes [Ding et al., 2003]. The effects of PBGA package placement on PWB warpage during the convective reflow were evaluated based on the projection moiré technique and FE modeling. The results showed that the number of PBGAs as well as their locations has effects on the warpage of the PWB. The FE results were used to make recommendations of the optimal PBGA placement locations on the PWB to minimize PWB warpage during reflow processes [Powell & Ume, 2006].

The warpage of different types of chip packages has been investigated. Numerous studies on the substrate warpage of large area multi-chip module-deposited (MCM-D) packages have been performed. The warpage measurement studies were developed on the substrates with different material properties using the shadow moiré technique [Dang et al., 2000; Dang & Ume, 2000; Bhattacharya et al., 2000]. The warpage of PBGA packages was measured using a real-time warpage measurement system with the

projected grating method. A high resolution measurement was provided by the system [He et al., 1998]. The effects of substrate thickness, package assembly process, die size, and encapsulation thickness and size on the warpage of an enhanced PBGA (EPBGA) package were studied. The results showed that encapsulation thickness is the most significant factor on the package warpage, with smaller encapsulation thickness resulting in higher warpage; maximizing the substrate thickness and minimizing the encapsulation size could reduce the impact of encapsulation height on package warpage [Liang, 1996]. The substrate warpage of a flip chip package during assembly was characterized using the shadow moiré technique [Zhang et al., 2003]. In order to optimize the reflow profile, the warpage of a flip chip assembly was investigated by the shadow moiré method. The study aided to develop a robust reflow process which resulted in yields of 98 % or greater [Muncy et al., 2003]. The warpage of the flip chip package was also studied during a simulated infrared reflow process. It was found that the warpage of the package decreased after the reflow process and then increased after the underfill application [Ding et al., 2005]. The warpage of a wafer level CSP package was studied during heating using moiré interferometry method. The results showed that nonlinear thermal deformations during heating are caused by creep and stress relaxation of the solder bumps [Ham & Lee, 2001].

In this research, automatic package detection and segmentation algorithms will be developed for the projection moiré system. The automated algorithms can segment the PWB with assembled omnidirectional chip packages, and determine their warpage separately, such that the projection moiré measurement system will possess higher accuracy, flexibility, and reliability.

2.4. Correlation Between Board-Level Warpage and Solder Bump Fatigue

Solder bump fatigue is a common failure mechanism of electronic devices and is believed to be either fully or partially responsible for 90 % of all structural and electrical failures [Tummala, 2001]. It is caused by cyclic thermomechanical stresses, and is severely affected by out-of-plane displacement of PWBs. This research will discuss the correlation between PWB warpage and the low cycle fatigue of solder bumps on board assemblies.

In order to estimate the fatigue life of solder bumps, an empirical relationship between strain and bump life was developed and widely applied [Coffin & Schenectady, 1954; Gektin et al., 1997]. Based on the finite element modeling, the effective strains of the models during thermal cycling simulation were calculated to predict the fatigue life of solder bumps [Yao et al., 1999]. The material properties of solder bumps are significantly influential factors to the bump reliability. The 63Sn-37Pb solder material was modeled with an elastic-plastic-creep model in FEA to assess the fatigue life of solder bumps in various packages such as flip chip assemblies, CSPs, and PBGAs [Muncy, 2004; Sumikawa et al., 2001; Tee et al., 2006]. The lead-free solder material is more reliable than traditional Sn-Pb solder. In order to characterize the mechanical properties of lead-free solder, the experimental temperature-dependent stress-strain curves were generated for applications in FEM [Pang et al., 2004]. The failure modes and reliability tests were performed for lead-free solder bumps in CSP and PBGA packages based on the elastic-plastic-creep model, viscoplastic model, and energy model of the solder material [Che & Pang, 2004]. The reliability of flip chips on board assemblies has been investigated based on in-situ stress and warpage measurements [Bansal et al., 2003].

The literature shows that the PWB warpage has effects on the fatigue life of the solder bumps on board assemblies. However, there are no full-field studies on the correlation between PWB warpage and solder bump fatigue of electronic packages. This research will fill this gap by studying the effect of the board warpage on solder bump fatigue reliability in PBGA packages.

CHAPTER 3

DEVELOPMENT OF CONVECTIVE REFLOW HEATING SYSTEM FOR WARPAGE MEASUREMENT

The forced convective heating system was redesigned and improved so that it can successfully simulate industrial reflow soldering processes. The projection moiré and shadow moiré techniques were integrated with the developed heating system to enable measuring warpage in real-time during different reflow processes. In order to achieve the ideal heating rate of 2 °C/second with the convective heating system, more power was supplied to the heaters, the heater surface area was increased, and the oven volume was decreased. A PID feedback controller was implemented to optimize heating responses. During the reflow process, the temperature gradients through the thickness of the printed wiring boards (PWBs), PWB assemblies (PWBAs) and electronic packages were reduced to decrease sample warpage and achieve accurate measurement results. The developed convective reflow-projection moiré warpage measurement system is the first real-time, non-contact, and full-field warpage measurement system capable of simulating any type of reflow soldering processes.

3.1. Convective Reflow Heating System Configurations

To effectively simulate thermal reflow soldering processes, one objective of this research is to develop a forced convective heating system to be used with the projection moiré and shadow moiré warpage measurement techniques.

Figure 3.1 shows the schematic of the convective reflow-moiré warpage measurement system, which can measure real-time warpage of PWBs, PWBAs, and electronic packages during infrared (IR) and convective heating reflow processes. The measurement system includes the optical equipment and setups for the projection moiré and shadow moiré techniques illustrated in Chapter 2.

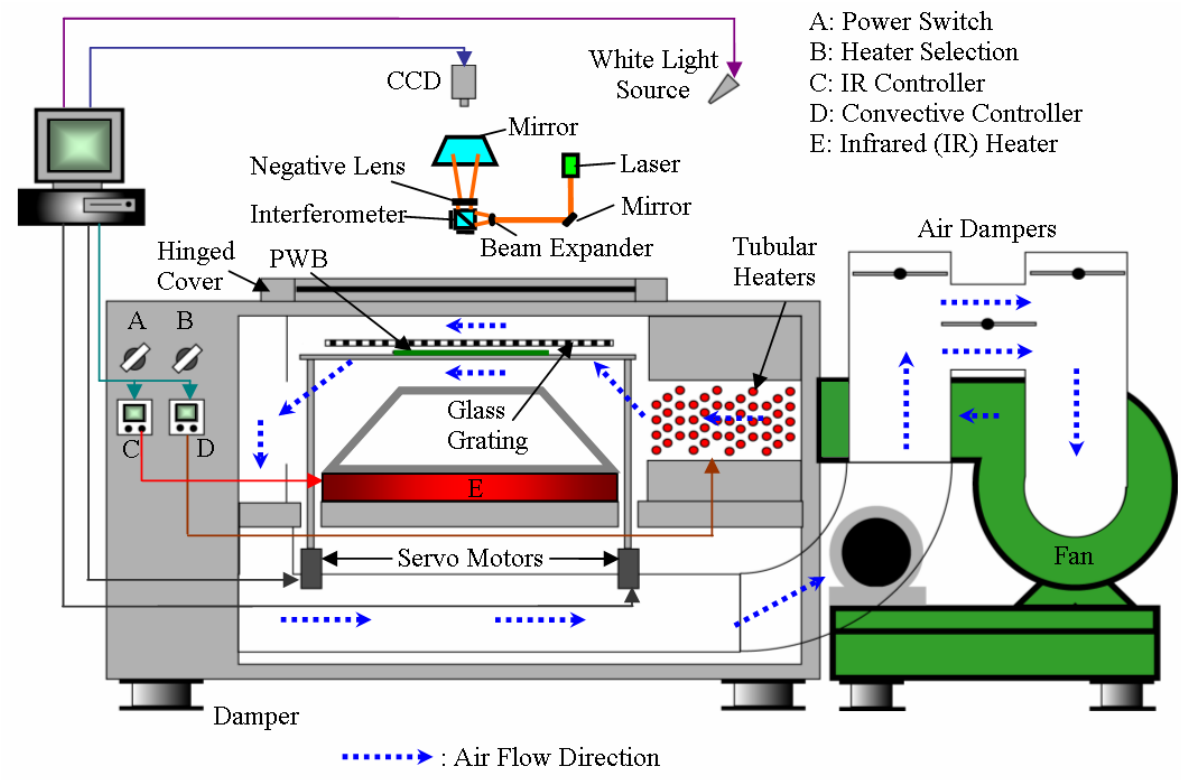


Figure 3.1. Schematic of Warpage Measurement System

An IR heater, located underneath the specimen in the oven chamber, supplies powerful heating. However, IR heating causes high temperature gradients through the thickness of PWB and PWBA samples, which may generate large warpage during the thermal reflow process. In order to overcome non-uniform heating on the specimen and

to obtain more accurate warpage measurement results, convective heating was considered for use in the system. Originally, 12 tubular heaters, with a total heating power of 36 KW, were located inside the oven chamber. A software controller created on the PC with LABVIEW is used to control the IR heating and convective heating to follow the given temperature profiles. A large centrifugal fan was installed at the right side of the oven to enable convection. The airflow circulation loop is shown in Figure 3.1. The centrifugal fan can adjust the airflow velocity across the tubular heaters to between 0 and 6.096 m/s through a variable frequency drive. The system isolates vibration of the fan from the oven by the use of flexible duct connectors and air dampers.

In order to successfully simulate industrial thermal reflow soldering processes, the forced convective heating system should be able to follow a typical ramp to dwell, ramp to peak (RDRP) temperature reflow profile, as shown in Figure 3.2.

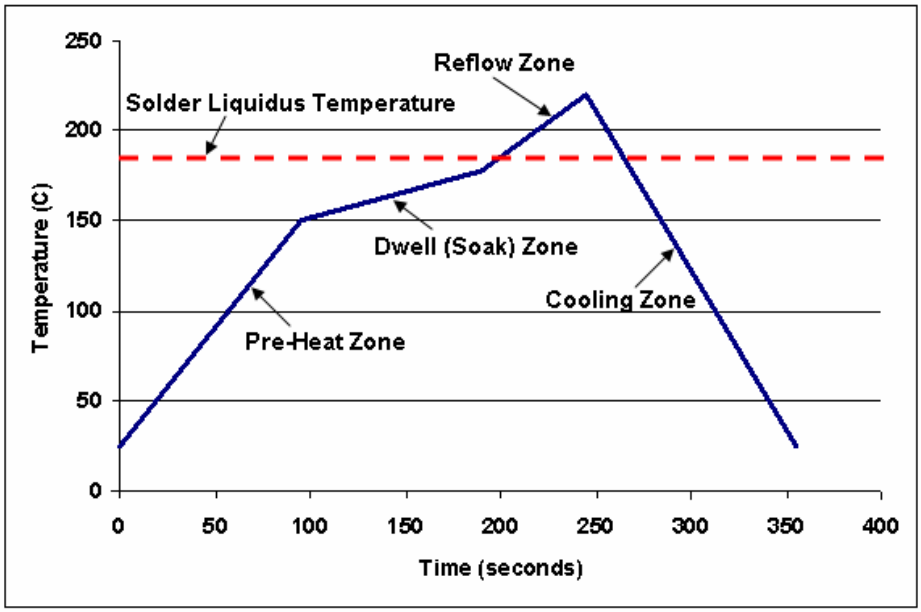


Figure 3.2. Typical RDRP Temperature Reflow Profile

The RDRP profile involves four different temperature zones: the pre-heat zone, the dwell or soak zone, the reflow zone, and the cooling zone. The reflow profile has a direct impact on manufacturing yield, solder bump integrity, and reliability of the PWB assemblies. A typical reflow oven has 5 to 9 heating zones and 1 to 2 cooling zones so that the temperature in the oven can be well controlled. In the pre-heat zone, the temperature is increased at a controlled rate to minimize thermal damage to the electronic packages and PWBs. A temperature heating ramp rate of 2 °C/second is typically used [Lee, 2002]. Higher ramp rates should be avoided, since they may cause thermal shock to the assembled components. The solvent in the solder paste is not allowed to evaporate slowly enough to avoid creating solder balls and short circuits between leads.

The dwell or soak zone can equalize the temperature of all surfaces being soldered and can activate the flux in the solder paste. The flux begins to wet the component leads and the solder pads on the PWB in the 150 to 180 °C range. The flux reduces metal oxides to expose the clean solderable metal.

In the reflow zone, the solder is heated above its liquidus temperature to a peak temperature that is normally from 215 to 225 °C. Rapid heating is used to ensure that the entire assembly quickly reaches the peak temperature, which allows solder to form good electrical and mechanical connections. Remaining at too high a temperature for too long may create excessive intermetallic layers, which have negative effects on solder bump reliability [Tummala, 2001].

Finally, the cooling zone enables the solder to solidify before exiting the reflow oven. It is very important to keep this step under strict control. If the PWBA is cooled

down too slowly, large grains will form in the solder bumps, resulting in fragile connections. Cooling down too fast may create other reliability problems.

Another temperature reflow profile is shown in Figure 3.3 [Lee, 2002]. The profile was developed and optimized using defect mechanism analysis. It consists of a slow temperature ramp with a rate of 0.5 to 1 °C/second to the solder liquidus temperature, a short dwell zone at the solder liquidus temperature, and a rapid reflow zone to the peak temperature.

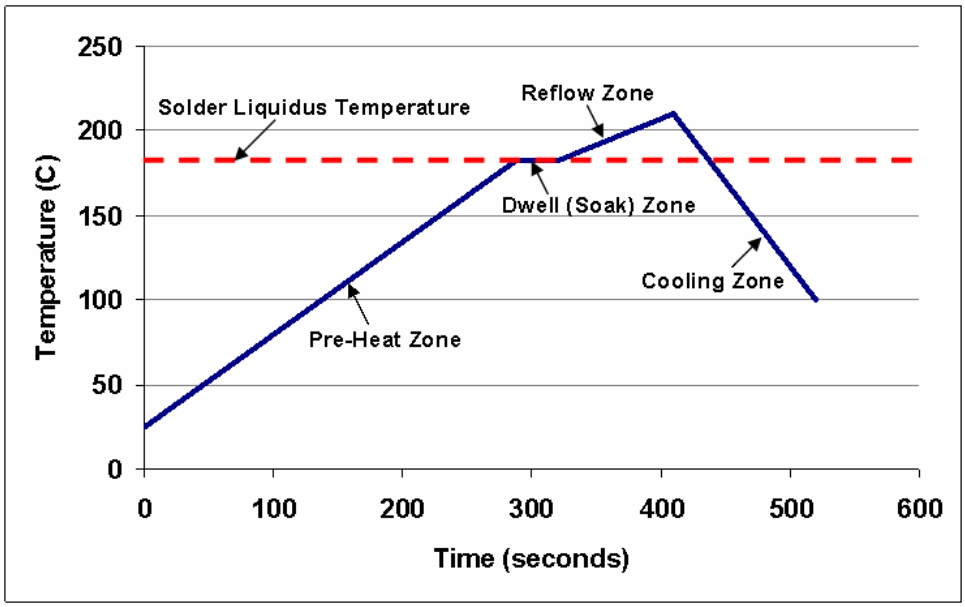


Figure 3.3. Lee Optimized Temperature Reflow Profile

The forced convective heating system developed in this research should be able to follow the temperature profiles shown in Figure 3.2 and Figure 3.3. Since the convective heating system has a single oven chamber, the temperature in the chamber needs to be well controlled and changed uniformly and continuously so that the PWBA samples do not have to pass through multiple heating chambers. The convective heating system has

several advantages. It uses a single chamber to finish the whole reflow process. Also, the system does not need the conveyor to pass through PWBA samples. Further, it is much more convenient to accurately control the sample temperature during the reflow process. Finally, the space occupied by the heating system was significantly decreased, and the cost of the equipment was further reduced.

3.2. Convective Reflow Heating System Modifications

3.2.1. Original Heating System Configurations

The previously existing convective heating system used 12 tubular heaters, with a total power of 36 KW, for the convection heating elements; the total heater surface area was about 0.58 m^2; and the oven chamber volume was 0.39 m^3.

A 1250 CFM centrifugal fan is located at the right side of the oven to enable the airflow circulation loop. The variable frequency driver of the fan controls the airflow rate through the heating system. There is a linear relation between the fan frequency and the air flow velocity, as shown in Equation (3.1). The convective heating processes were conducted by varying the fan frequency from 20 Hz to 30 Hz. The lower bound, 20 Hz, was chosen to prevent overheating of the tubular heaters due to insufficient airflow through the heater surfaces. If the fan frequency goes higher than 30 Hz, the fast airflow may cause the PWBA test vehicles to vibrate, which affects the accuracy of the warpage measurement results.

$$V_{air} = 0.396 f \tag{3.1}$$

where, V_{air} = airflow velocity (m/s)

f = fan frequency (Hz)

An experimental study established that the heating rate on test vehicles achieved a maximum value of about 0.55 °C/second in the original system when the fan frequency was 23 Hz. However, successfully simulating any manufacturing reflow process requires that the convective heating system achieves the ideal heating ramp rate of 2 °C/second. The following sections explain the design and improvements for the hardware and software of the novel heating system.

3.2.2. Hardware Development of Convective Heating System

Using the previous convective heating system, the maximum temperature difference through the PWBA thickness was less than 10 °C, which is significantly lower than that during infrared heating process. However, the temperature ramp rate on the sample surface, using convective heating, could only reach approximately 0.55 °C/second, which needed to be improved to 2 °C/second to simulate the ideal thermal reflow process. To evaluate the most efficient method for improving the PWB/PWBA heating rate, a computational fluid dynamics (CFD) model was generated to simulate the entire convective heating system in the analysis software, FLUENT. A 3-D model was used, based on the geometry shown in Figure 3.1. The temperature data on the PWBA test vehicles along with time were used to calculate the heating ramp rate in the convective system. Heat was applied to the PWBA samples for a total of 120 seconds.

Based on the CFD model, a 3-factor, 2-level, and full-factorial design of simulations was performed. The factors of interest include the heating system volume, the surface area of the heaters, and the heaters' total power [Powell, 2006]. Using the simulation results from the CFD model, a reduced regression model was created as shown in Equation (3.2).

$$R = (2.9 + 31.5A_h + 1.31P_h - 93.3V_s A_h + 1.30A_h P_h)/120 \quad (3.2)$$

where, R = heating ramp rate on test vehicle (°C/second)

V_s = system volume (m^3)

A_h = heater surface area (m^2)

P_h = heater power (KW)

The above regression equation represents a reduced bilinear model, expressing the sample temperature ramp rate as a function of the predictor variables and their two-factor interactions. Note that the three-factor interaction is omitted from Equation (3.2). Those interaction effects are not included because of the hierarchical ordering principle, which states that lower order effects are more likely to be important than higher order effects [Wu & Hamada, 2000]. In order to achieve the ideal heating ramp rate to simulate the RDRP convective reflow profile, all three factors in Equation (3.2) needed to be changed simultaneously. Some possible parameter settings with different heating ramp rates are shown in Table 3.1. The first run shows the performance of the current convective system.

Table 3.1. Possible Oven Parameter Settings with Different Heating Rates

Configuration	Heating Rate (°C/second)	System Volume (m^3)	Heater Surface Area (m^2)	Heater Power (KW)
1	0.6	0.39	0.58	36
2	1.0	0.37	1.60	36
3	1.5	0.36	2.15	44
4	2.0	0.35	2.32	55
5	2.5	0.33	2.32	68

In order to obtain the ideal heating rate of 2 °C/second, the convective heating system was redesigned to improve its performance. For the hardware design, the system was changed to supply more power to the heaters; the heater surface area was increased to more than 4 times the original area; and insulation was used to fill in the oven, decreasing the chamber volume.

A total of 12 finned tubular heaters were installed in the system to replace the original heaters. The new convective system provides a 3-phase power with 72 KW to support the new heaters. The 3-phase system uses less conductor material to transmit electric power than equivalent 1-phase, 2-phase, or direct-current systems at the same voltage to effectively provide the power. There are 4 to 5 fins per inch standing on each heater to increase the heating area. These finned heaters increased the heater surface area to 3.26 m^2, which is 5.62 times greater than the original heating area. Thermal insulation was used to fill in the oven to decrease the chamber volume allowing the system to reach the ideal heating ramp rate. The improved system volume is 0.31 m^3. Connections between the oven and the centrifugal fan and between the ducts were airproofed with thermal insulation wraps to achieve a better airflow circulation loop.

3.2.3. Software Development of Convective Heating System

A proportional (P), integral (I), and derivative (D) controller was chosen to control the finned tubular heaters to achieve the optimal heating response. Figure 3.4 shows the feedback control system diagram for the oven.

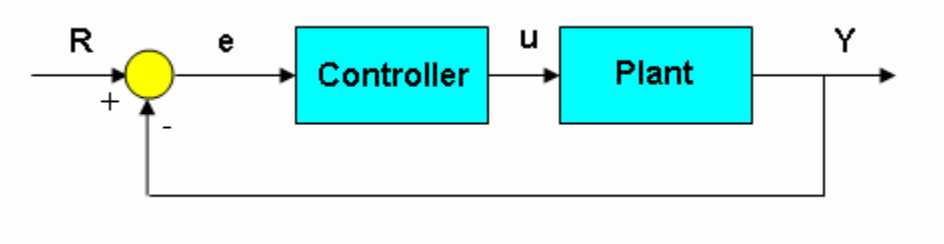


Figure 3.4. Feedback Control System Diagram

In Figure 3.4, the plant is the convective heating system that needs to be controlled. The controller is a PID controller which is used to provide the excitation and control the overall system behavior. Equation (3.3) shows the transfer function of the PID controller.

$$K_P + \frac{K_I}{S} + K_D S = \frac{K_D S^2 + K_P S + K_I}{S} \tag{3.3}$$

where, K_P = proportional gain

K_I = integral gain

K_D = derivative gain

In Figure 3.4, the error signal (e) is the difference between the desired input temperature value (R) and the actual output temperature (Y). The error signal (e) is sent to

the PID controller. The signal (u) generated from the controller is calculated by Equation (3.4). This signal (u) is sent to the plant to obtain the new temperature output value (Y). Based on the feedback control loop, a new error signal (e) is calculated, and the control process repeats continuously.

$$u = K_P e + K_I \int e dt + K_D \frac{de}{dt} \tag{3.4}$$

where, e = error signal

u = calculated signal from PID controller

K_P = proportional gain

K_I = integral gain

K_D = derivative gain

In the PID controller, the proportional gain (K_P) can reduce the rise time and the steady-state error for the temperature response; the integral gain (K_I) can eliminate the steady-state error; the derivative gain (K_D) can increase system stability, reduce overshoot, and improve transient response. For the convective heating system in this study, the PID controller was built in the software, LABVIEW virtual instruments, to realize the real-time control process for the heaters. To optimize the heating response, the proportional gain (K_P) is set to 10; the integral gain (K_I) is set to 1; and the derivative gain (K_D) is set to 0.35. Figure 3.5 shows the heating control block diagram designed using LABVIEW.

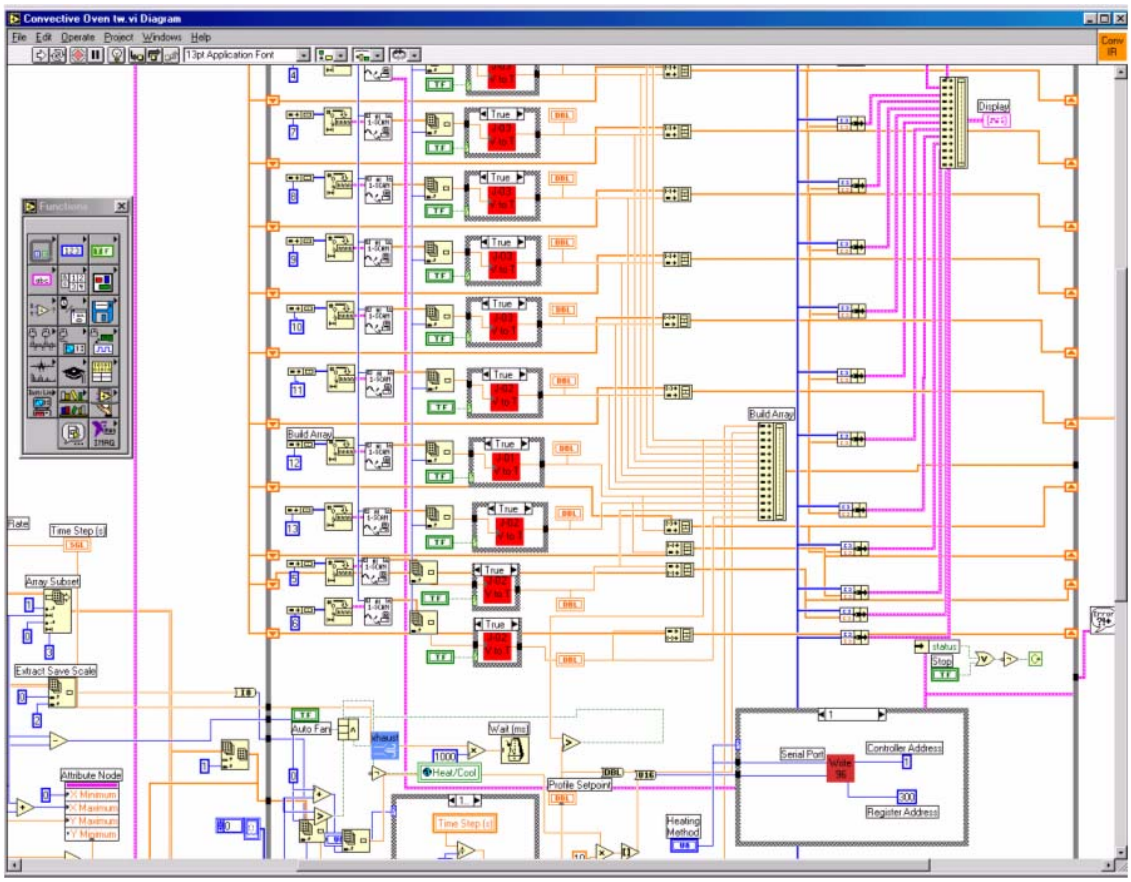


Figure 3.5. Heating Control Block Diagram in LABVIEW

The above PID controller was integrated with the measurement control, sensor testing, and other software design to realize a completely automated control for the real-time convective reflow-warpage measurement system. Figure 3.6 shows the convective heating control panel built with LABVIEW, which has 6 buttons to control the heating process and warpage measurement. There are 12 channels of thermocouples installed in the oven. They can be used to measure the temperature at different locations on the test vehicle during the thermal reflow process. Channel 1 is the feedback temperature sent to the PID controller. The ideal and actual temperature profiles can be displayed in the

center plot. The X-axis is the reflow time (seconds), and the Y-axis is the measured temperature (°C).

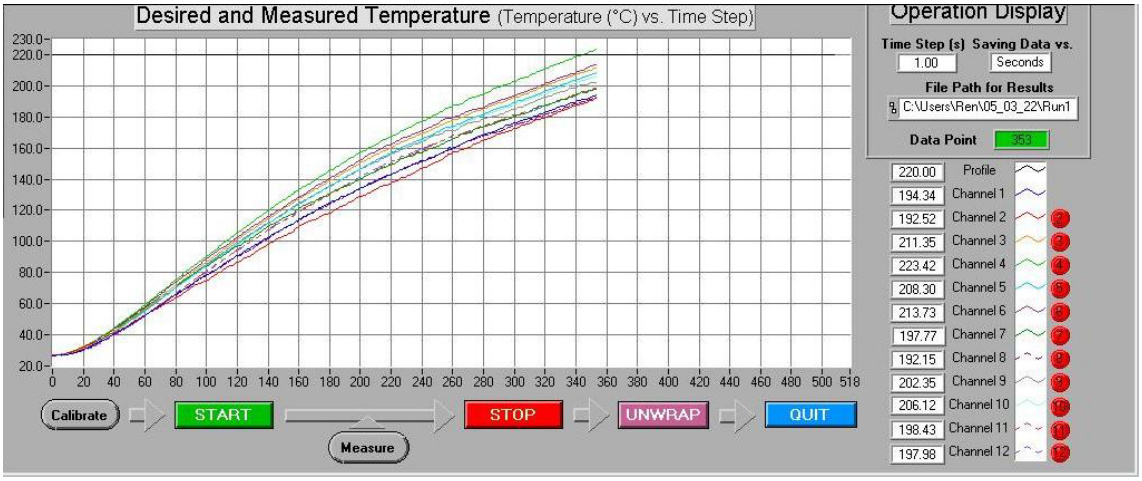


Figure 3.6. Convective Heating Control Panel in LABVIEW

3.2.4. Configurations of Improved Convective Heating System

Based on the improved hardware and software, the optimized convective heating system was used to conduct heating experiments to illustrate the system capabilities and configurations. The 12 channels of thermocouples were used to measure the temperatures at different locations on the PWB test vehicle with the size of 203.2 mm by 139.7 mm by 0.631 mm. Figure 3.7 shows the thermocouple placement on the PWB. At each of 6 locations, 2 thermocouples were attached at the top and bottom sides of the PWB respectively in order to measure the temperature gradient through the board thickness.

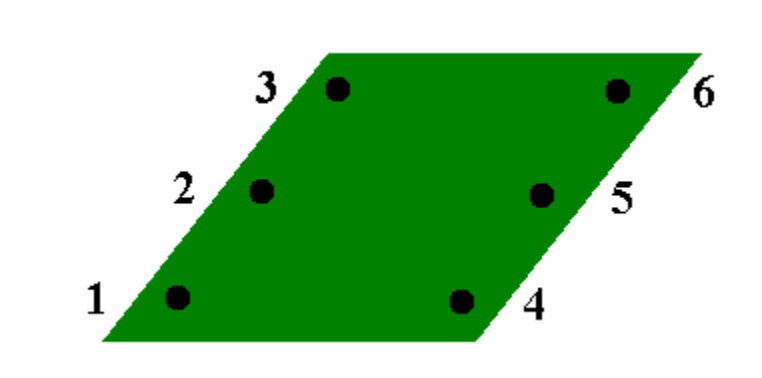


Figure 3.7. Thermocouple Placement on PWB Sample

A step temperature profile with the constant value of 210 °C was used to characterize the performance of the convective reflow oven. Table 3.2 shows the experimental results using the improved convective heating system with different airflow speeds.

Table 3.2 shows that the maximum heating ramp rate of 1.82 °C/second was obtained with the centrifugal fan frequency of 23 Hz. The improved heating rate is more than 3 times the original rate of 0.55 °C/second. The temperature difference through the board thickness is less than 3.34 °C, which is decreased more than 4 °C from the original difference of 7.80 °C. With the increased airflow speed, the heating rate, the 5 % settling time, and the overshoot are all slightly decreased. When the fan frequency goes higher than 24 Hz, the fast airflow may cause the PWB test vehicles to vibrate, which affects the accuracy of warpage measurements. Therefore, the convective heating oven is able to achieve its optimal performance at the fan frequency of 23 Hz: its maximum heating rate is 1.82 °C/second; the temperature gradient through PWB thickness is 3.18 °C; the 5 %

settling time is 212 seconds; the overshoot is 10.31 °C; and the airflow does not cause vibration of the test vehicles.

Table 3.2. Heating Performance of Improved Convective Reflow Oven

Case	Fan Frequency (Hz)	Max. Heating Rate (°C/sec)	Temperature Difference though Thickness (°C)	Settling Time 5% (sec)	Overshoot (°C)	PWB Vibration
1	21	1.81	3.27	207	10.77	No
2	22	1.81	3.31	220	10.66	No
3	23	1.82	3.18	212	10.31	No
4	24	1.80	3.29	217	10.26	No
5	25	1.78	3.19	208	9.54	Yes
6	26	1.78	3.23	204	9.13	Yes
7	27	1.77	3.34	197	9.10	Yes
8	28	1.74	3.31	188	8.78	Yes
9	29	1.73	3.27	190	8.35	Yes
10	30	1.70	3.24	189	8.34	Yes

Figure 3.8 shows the temperature profile for the 12 thermocouple locations during the convective heating experiment at the fan frequency of 23 Hz. Thermocouple placement is shown in Figure 3.7. The experimental results show that the temperature difference through the thickness is significantly lower than the temperature difference of 41.6 °C using the infrared heating. Therefore, the convective heating method is able to provide heat much more uniformly to decrease the PWBA warpage caused during the thermal reflow process. The top surface temperature of the PWB is slightly higher than its bottom surface. Also, the improved convective heating system can provide a fast heating ramp rate, making it possible to accurately simulate industrial convective heating reflow profiles.

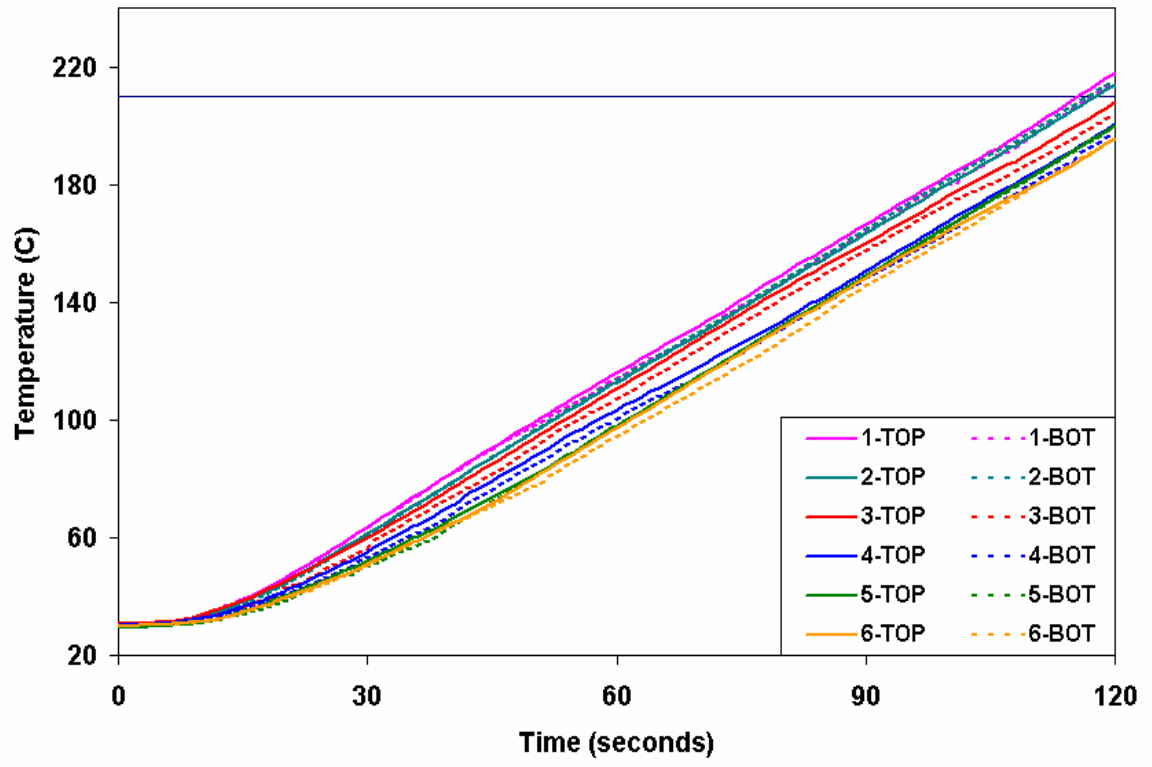


Figure 3.8. Thermocouple Temperature Profile During Convective Heating Process

The developed convective heating system was used to simulate industrial thermal reflow soldering processes, including the RDRP temperature profile and the Lee optimized reflow profile, as shown in Figure 3.2 and Figure 3.3, respectively. The RDRP profile and Lee profile were inputted into the PID controller through the LABVIEW virtual instrument interface.

Figure 3.9 shows the typical RDRP profile input and the measured temperature output. The convective reflow profile has a heating rate of 1.80 °C/second to the dwell zone, a dwell time of 80 seconds, a peak temperature of 230 °C, and a time period above 183 °C of 134 seconds. The melting temperature for the Sn-Pb alloy is 183 °C.

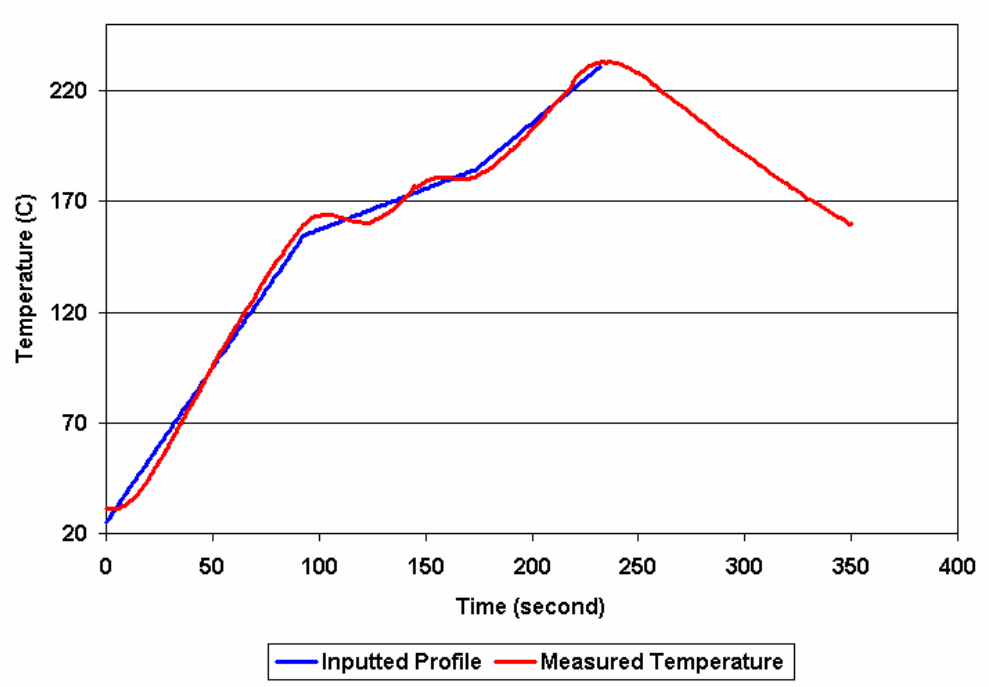


Figure 3.9. Simulation of RDRP Reflow Profile

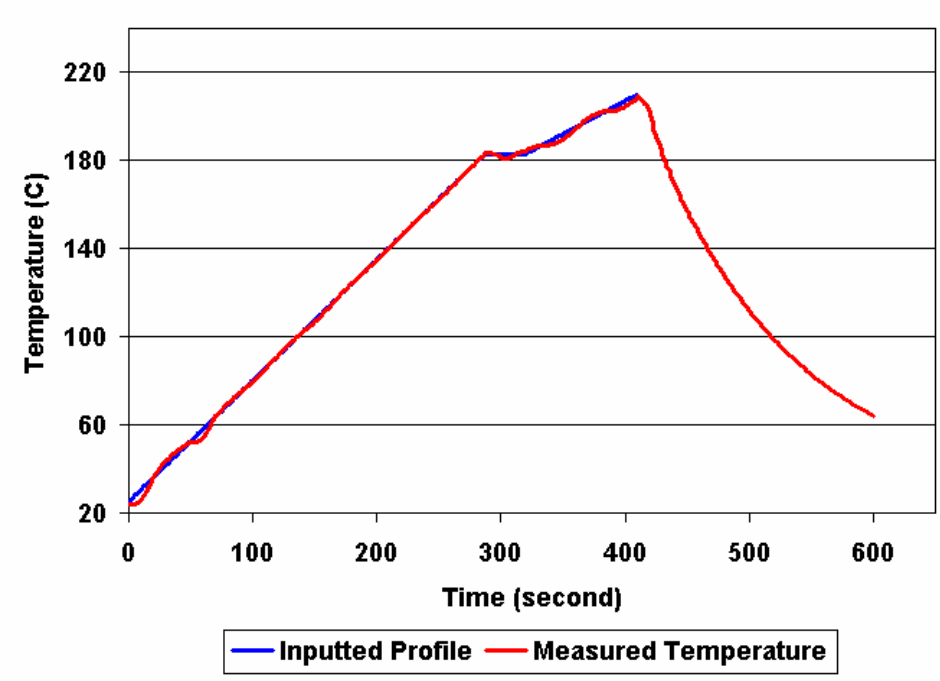


Figure 3.10. Simulation of Lee Optimized Reflow Profile

Figure 3.10 shows the Lee optimized profile input and the measured temperature output. The convective reflow profile has a heating rate of 0.65 °C/second to the dwell zone, a peak temperature of 210 °C, and a time period above 183 °C of 122 seconds.

Based on the experimental results, the developed convective reflow heating system can be used to successfully simulate industrial thermal reflow soldering processes. The heating system can achieve an ideal heating ramp rate, provide uniform heating and excellent transient responses, generate zero static state error, and reduce temperature gradients through the test vehicle thickness. The improved oven was integrated with the projection moiré and shadow moiré warpage measurement techniques to conduct real-time warpage measurement during the simulated convective heating reflow process. The developed convective reflow and projection moiré warpage measurement system is the first real-time, non-contact, and full-field warpage measurement system capable of simulating any type of reflow soldering processes.

3.2.5. Heating Efficiency of Convective Heating System

The first law of thermodynamics was used to estimate the ideal heating ramp rate of the air flow in the convective heating system with a heating input of 72 KW. Assuming there is no leakage in the reflow system, the total airflow energy rate can be calculated by Equation (3.5).

$$\frac{dE}{dt} = \delta Q - \delta w \tag{3.5}$$

where, dE/dt = total airflow energy rate (W)

δQ = inputted energy per unit time (W)

δw = work output from system per unit time (W)

There is no kinetic energy change, potential energy change, or work output energy in the convective heating system. The ideal airflow heating rate is given by Equation (3.6).

$$\frac{dT}{dt} = \frac{\delta Q}{\rho c V} \tag{3.6}$$

where, dT/dt = ideal airflow heating rate (°C/second)

δQ = inputted energy per unit time (W)

ρ = air density (kg/m^3)

c = air specific heat (kJ/(kg·°C))

V = system volume (m^3)

In Equation (3.6), the heater power is 72 KW, the volume of the convective heating system is 0.31 m^3, the air density is 1.16 kg/m^3, and the air specific heat is 0.72 kJ/(kg·°C). The calculated ideal air heating rate is 278.09 °C/second. The actual air heating rate is 22.14 °C/second, and the maximum test sample heating rate is 1.82 °C/second. The ideal air heating rate is significantly higher than the actual heating ramp rate. The reasons are that the actual convective heating system has a very large volume and is not completely airproof. Small air leakage occurs at the connections between the ducts. The system loses energy when the heat is transferred from the finned tubular

heaters to the air and from the air to the PWBA test vehicles. Increasing the heating efficiency in the convective reflow oven is required in future study.

3.3. Chapter Summary

In this chapter, the forced convective heating system was redesigned and integrated with the projection moiré and shadow moiré warpage measurement techniques. In order to achieve the ideal heating rate, a 3-phase power of 72 KW was supplied to the heaters; the heater surface area was increased to 3.26 m^2, which is 5.62 times larger than the original heating area; and the system volume was reduced to 0.31 m^3. Thermal insulation was used to fill the interior of the oven, decreasing its volume so that the system can reach the ideal heating ramp rate. Connections between the oven and the centrifugal fan and between the ducts were airproofed with thermal insulation wraps to ensure a better airflow circulation loop. The improved heating system is able to achieve the heating ramp rate of 1.82 °C/second, provide uniform heating and optimal transient responses, generate zero static state error, and reduce temperature gradients through test vehicle thickness. An advanced controller, created using LABVIEW virtual instruments, was implemented to control the heating performance of the oven and real-time warpage measurement during the thermal reflow process. The developed convective reflow-projection moiré warpage measurement system is the first real-time, non-contact, and full-field warpage measurement system capable of simulating any type of reflow soldering processes. The heating application efficiency still needs to be increased for future study. Compatible coolers are indispensable to be installed into the system, so that the convective reflow-projection moiré measurement system can be used to conduct

warpage measurement for PWBA test vehicles during the simulated accelerated thermal cycling tests.

CHAPTER 4

DEVELOPMENT OF PROJECTION MOIRÉ WARPAGE MEASUREMENT SYSTEM

In this chapter, an improved projection moiré warpage measurement system with two types of automatic package segmentation algorithms is presented. In order to use the projection moiré system to accurately and separately determine the warpage of a printed wiring board (PWB) and assembled electronic packages in a PWB assembly (PWBA), two package segmentation algorithms based on mask image model and active contour model (snake) were developed. They were used to detect and segment assembled packages from the PWB in a PWBA displacement image generated by the projection moiré system. The warpage of the PWB and chip packages can be determined individually irrespective of the package locations and orientations. The performances of the mask image and snake approaches based on their resolutions, processing rates, and measurement efficiencies were evaluated in this research. Real-time continuous and composite Hermite surface models were constructed to estimate the PWB warpage values underneath the electronic packages. The above automatic image segmentation algorithms were integrated with the projection moiré system to accurately evaluate the warpage of PWBs and assembled chip packages separately.

4.1. Projection Moiré Technique Post-Processing Algorithm

The projection moiré technique is complementary to the shadow moiré technique. The projection moiré system does not need a glass grating, it is more suitable to measure

a PWB surface with populated components, and it is also versatile to measure the boards and packages with various dimensions by simply adjusting its grating sizes. Yet it is more complex than the shadow moiré technique. The projection moiré system needs a post-processing algorithm to process the measured data and determine the warpage across the PWB and assembled packages respectively.

If the warpage of a populated PWB is measured using the projection moiré system without the post-processing algorithms, the maximum PWB warpage is calculated by directly taking the difference between the highest point on the chip package and the point on the PWB with the minimum out-of-plane displacement. This method cannot provide accurate measurement results for the PWBA warpage. Figure 4.1 shows an out-of-plane displacement plot of a PWB with one plastic ball grid array (PBGA) package measured using the projection moiré technique. The measured PWB is 203.2 mm by 139.7 mm by 0.631 mm, and the PBGA package is a 27 × 27 mm peripheral array package with 256 solder bumps and 1.27 mm bump pitch. The maximum PWB warpage result of 3634.9 microns as shown in Figure 4.1 is not correct. For a bare PWB, the maximum board warpage is calculated by taking the difference between the maximum and minimum out-of-plane displacements. However, for a PWB assembled with electronic packages, the above calculation is incorrect because the maximum out-of-plane displacement is taken as the highest point on the chip package. Also, the warpage values across the chip packages cannot be obtained directly. Therefore, in order to calculate the warpage across the PWB and assembled packages correctly for a PWBA, the post-processing algorithms should be used to segment the areas containing electronic packages from the rest of the

PWB, and determine the warpage across the PWB and assembled packages respectively [Powell & Ume, 2006].

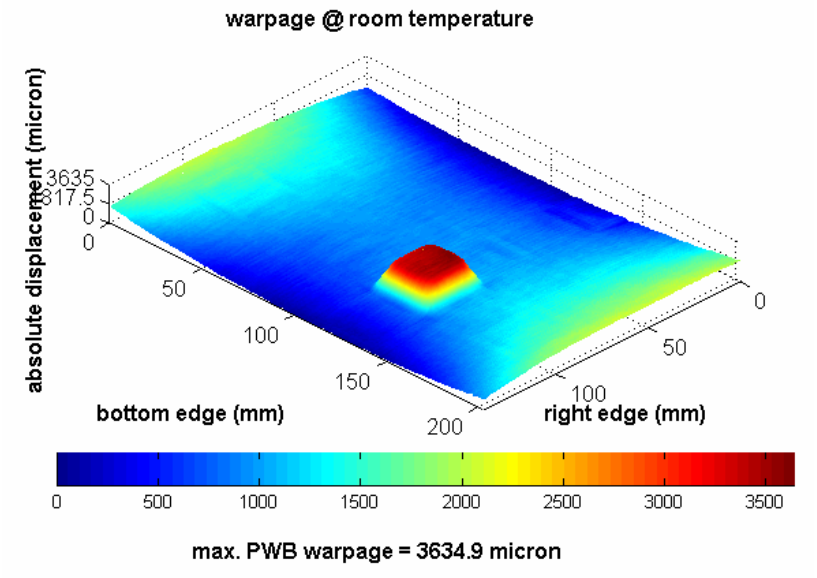


Figure 4.1. Warpage Measurement Plot of PWB with 27 × 27 mm PBGA Package Using Projection Moiré System

The post-processing algorithms include manual segmentation and automatic segmentation approaches. The manual segmentation method uses masks created manually to indicate the image pixels occupied by chip packages in a warpage plot of the PWBA. Then the unmasked image area can be used to calculate the PWB warpage, and the masked image area can be used to calculate the chip package warpage. The disadvantages of the manual segmentation are that the exact locations of the chip packages on the PWB must be known a priori. The manually created masks are not accurate since the PWBA warpage will change during the thermal reflow process. The segmentation process is tedious, and makes the projection moiré system unsuitable for online measurements. To

solve the problems associated with the manual segmentation method, automatic package detection and segmentation algorithms were developed for the projection moiré warpage measurement system. The automatic segmentation approaches do not require the chip package dimensions or locations to be known a priori, or to perform time consuming post-processing operations after measurements.

4.2. Automatic Package Detection and Segmentation Algorithms

4.2.1. Mask Image Model Segmentation Algorithm

The mask image model segmentation algorithm is an effective method to detect and segment assembled omnidirectional chip packages from the PWB. The well developed algorithm can individually evaluate the warpage across PWBs and assembled omnidirectional packages in arbitrary layouts with high resolution and high processing rate. Figure 4.2 shows the flowchart for generating the mask images to segment chip packages from the PWB.

At the beginning, the algorithm is to use Discrete Cosine Transform (DCT) based de-noising filters to decrease noise and increase contrast levels for the measured PWBA out-of-plane displacement plots generated from the projection moiré system. The definition of the two-dimensional DCT for an input image A and output image B is shown in Equation (4.1).

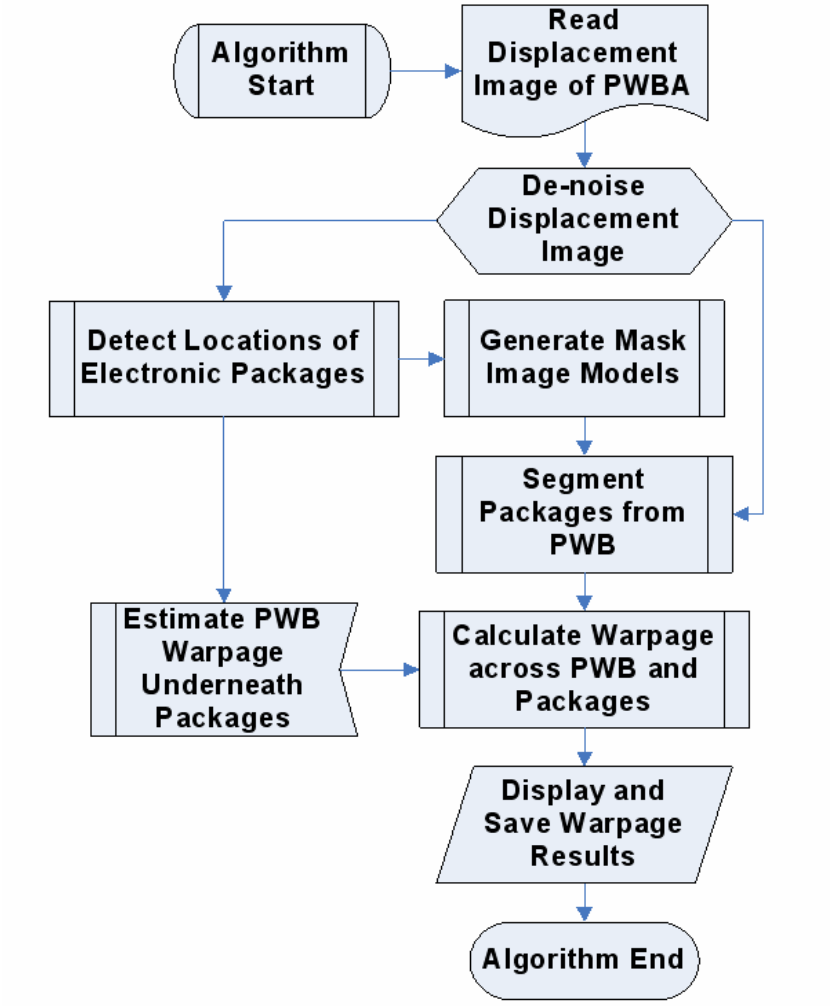


Figure 4.2. Mask Image Model Flowchart

$$B_{pq} = \alpha_p \alpha_q \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} A_{mn} \cos \frac{\pi(2m+1)p}{2M} \cos \frac{\pi(2n+1)q}{2N}, \quad \begin{matrix} 0 \le p \le M-1 \\ 0 \le q \le N-1 \end{matrix}$$

$$\alpha_p = \begin{cases} 1/\sqrt{M}, p = 0 \\ \sqrt{2/M}, 1 \le p \le M-1 \end{cases}, \quad \alpha_q = \begin{cases} 1/\sqrt{N}, q = 0 \\ \sqrt{2/N}, 1 \le q \le N-1 \end{cases} \tag{4.1}$$

where A is the original $M \times N$ image matrix, and B is the output denoised matrix [Gonzalez & Woods, 2001]. In the denoised PWBA displacement image, Canny's optimal edge detector is used to find the exterior edges of electronic packages based on

image gradients. Equation (4.2) and (4.3) are used to calculate the magnitude and direction of the gradient respectively [Canny, 1986].

$$|G| = \left[\left(\frac{\partial f}{\partial x} \right)^2 + \left(\frac{\partial f}{\partial y} \right)^2 \right]^{\frac{1}{2}} \tag{4.2}$$

$$\alpha = \tan^{-1} \left[\frac{\partial f}{\partial y} \Big/ \frac{\partial f}{\partial x} \right] \tag{4.3}$$

Based on the coordinates of the chip package which have been determined, the mask image model can be created by defining the pixel values inside the package area to be 1's, and outside the package area to be 0's. The mask image model has the advantages that it can be generated despite chip package locations and orientations. Even the packages are assembled with directional angles to the PWB edges, the mask images can be used to detect and separate the packages from the board. Figure 4.3 shows the mask image for the PWBA with a 35 × 35 mm PBGA package.

Figure 4.3. Mask Image Model for PWBA with 35 × 35 mm PBGA Package

Based on the calculation between the denoised PWBA image and the mask image, the package displacement image can be segmented from the PWB displacement image. The warpage across the board and assembled package is evaluated separately and accurately.

4.2.2. Active Contour Model and Greedy Algorithm

Active contour model (snake) has been used as another approach to detect and separate chip packages from the PWBA in a warpage image generated with the projection moiré system [Powell, 2006]. The snake is an energy minimizing spline, guided by external constraint forces, and influenced by image forces that pull it toward features such as lines and edges in an image [Kass et al., 1988]. The Greedy algorithm is a fast and stable numerical approach to solve the energy minimization problem [Williams & Shah, 1992]. The energy quantity being minimized by the Greedy algorithm is shown in Equation (4.4).

$$E = \int (\alpha(s)E_{cont} + \beta(s)E_{curv} + \gamma(s)E_{grad})\, ds \tag{4.4}$$

where, α, β, γ = weighting parameters

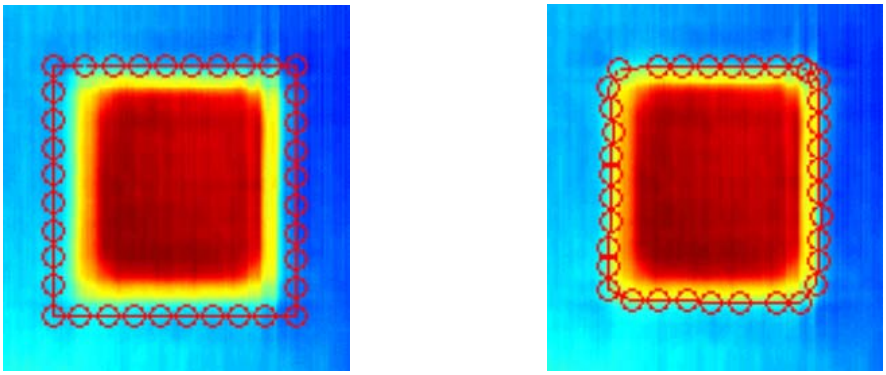
E_{cont} = continuity term

E_{curv} = curvature term

E_{grad} = image gradient term

For the purpose of edge finding, the weight parameter γ should be set higher than other two parameters α and β.

Before applying the Greedy algorithm to detect the package locations, the initial snake model needs to be constructed. In this research, the constructive method was improved to be more effective and flexible. To create the initial snake, Canny's optimal edge detector is used to find the exterior edges of electronic packages based on image gradients. The magnitude and direction of the gradient can be calculated using Equation (4.2) and (4.3) [Canny, 1986]. After the package exterior boundaries are determined in the displacement image, a rectangular snake with any number of points can be constructed around the location of the chip package. Then the Greedy algorithm is applied to accurately converge the initial snake to the chip package edges. Figure 4.4 (a) shows an initial snake contour around a 35 × 35 mm peripheral array PBGA package, and Figure 4.4 (b) shows the converged snake model after applying the Greedy algorithm. If the chip package is oriented with a directional angle to the PWB edges, the rectangular initial snake is extended to include all the package area. However, the algorithm will require more time to converge the initial snake to the package edges. Based on the package contour determined by the above method, the electronic package displacement image can be segmented from the PWB displacement image. Then the warpage across the board and assembled package is evaluated individually.



(a) (b)

Figure 4.4. (a) Initial Snake around 35 × 35 mm PBGA; (b) Converged Snake around 35 × 35 mm PBGA

4.2.3. Real-Time Composite Hermite Surface Model

In order to estimate the warpage values of the PWB area directly underneath the chip package, a real-time continuous and composite Hermite surface model is constructed. The parametric surface model is created by using the pixel values and image gradients near the package area, and replacing all the pixels corresponding to each package in the PWB warpage image with estimated pixel values. The geometric continuity between the parametric surface and other PWB areas is the first order parametric continuity (C^1), which is piece-wise continuous and tangent continuous. Equation (4.5) shows the definition of the Hermite surface model.

$$p(u,w) = F(u)BF(w)^T \tag{4.5}$$

$$F(s) = [(2s^3 - 3s^2 + 1), (-2s^3 + 3s^2), (s^3 - 2s^2), (s^3 - s^2)]$$

$$B = \begin{bmatrix} p_{00} & p_{01} & p_{00}^{w} & p_{01}^{w} \\ p_{10} & p_{11} & p_{10}^{w} & p_{11}^{w} \\ p_{00}^{u} & p_{01}^{u} & p_{00}^{uw} & p_{01}^{uw} \\ p_{10}^{u} & p_{11}^{u} & p_{10}^{uw} & p_{11}^{uw} \end{bmatrix}$$

where u and w ($u, w \in [0,1]$) are the two parametric variables to define the surface patch, p_{ij} (i, j = 0, 1) is the pixel value at each corner of the parametric surface, p_{ij}^{u} and p_{ij}^{w} are the image gradients in different directions, and p_{ij}^{uw} is the twist vector at the corner [Mortenson, 1985].

The automatic package segmentation algorithms based on the mask image model and snake model described above were integrated with the projection moiré system to evaluate the warpage across the PWB and omnidirectional chip packages in a PWBA separately and accurately. The performances of the two approaches, including their resolutions, processing rates, and measurement efficiencies, were compared based on the warpage case studies of PWBs populated with different types of electronic packages. The comparison results are discussed in the following sections.

4.3. Automatic Package Segmentation Algorithm Comparisons

4.3.1. Warpage Measurement Based on Mask Image Model and Snake Model

In order to compare the mask image segmentation and snake algorithms, the projection moiré system was used to measure the warpage across the PWB with different electronic packages. Figure 4.5 shows the warpage measurement result for a bare PWB, which has the dimension of 203.2 mm by 139.7 mm by 0.631 mm. Its maximum warpage is 2237.3 microns. Note that the maximum warpage is the difference between the

maximum and minimum out-of-plane displacements. Figure 4.6 shows the warpage measurement result for a 27 × 27 mm peripheral array PBGA package. The PBGA has 256 solder bumps and 1.27 mm bump pitch. The maximum warpage across the PBGA is 1871.7 microns. The above PBGA package was then loosely placed on the lower right side of the PWB sample as shown in Figure 4.5. The projection moiré system with the mask image segmentation and snake algorithms was used to measure the warpage across the PWB and the PBGA respectively. By using the snake model and Greedy algorithm, Figure 4.7 shows that the maximum warpage across the PWB is 2229.8 microns, and the maximum warpage across the PBGA is 1865.3 microns. On the other hand, by using the mask image segmentation method, the maximum warpage across the PWB is 2231.1 microns, and the maximum warpage across the PBGA is 1867.0 microns. The above measurement results show that both algorithms have high resolutions, and that they match each other very well. They show less than 0.4 % difference when compared with the warpage values obtained in Figures 4.5 and 4.6. The real-time composite Hermite surface was generated to determine the PWB warpage values underneath the chip package. The parametric surface replaced all the pixels corresponding to the package area in the PWB warpage image. The calculated maximum warpage of the PWB area underneath the PBGA is 732.3 microns, which has 1.3 % difference compared with the measurement result of 741.8 microns. Therefore, the Hermite surface models have the capability to define the PWB warpage values underneath the chip packages with very good accuracy.

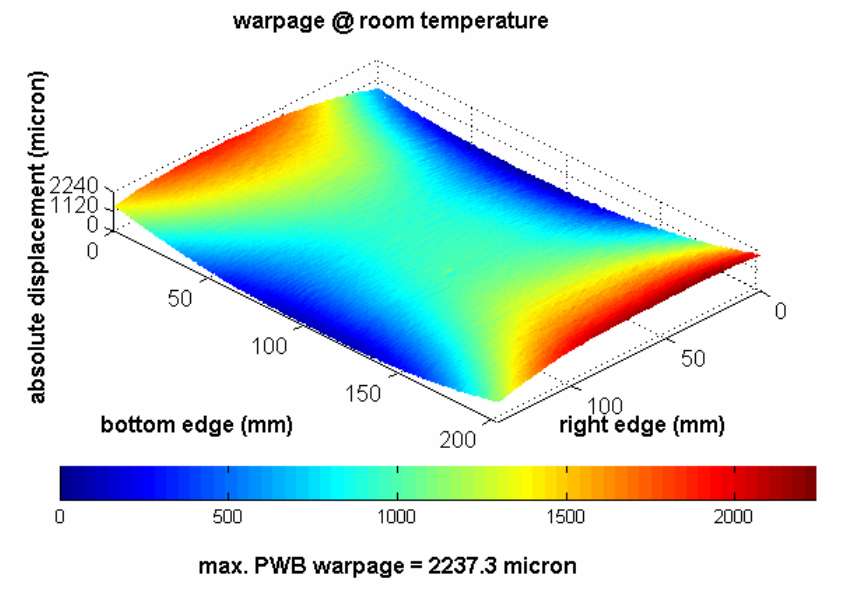


Figure 4.5. Warpage Measurement Plot of Bare PWB

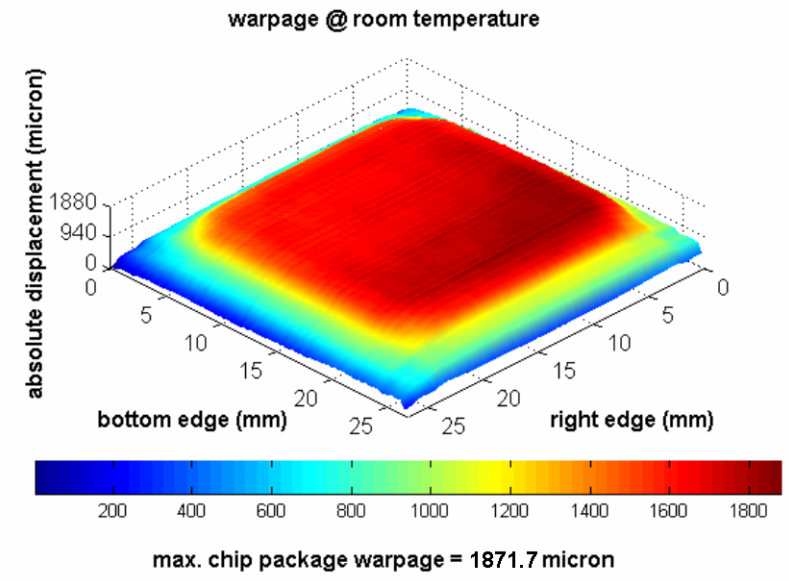


Figure 4.6. Warpage Measurement Plot of 27 × 27 mm PBGA Package

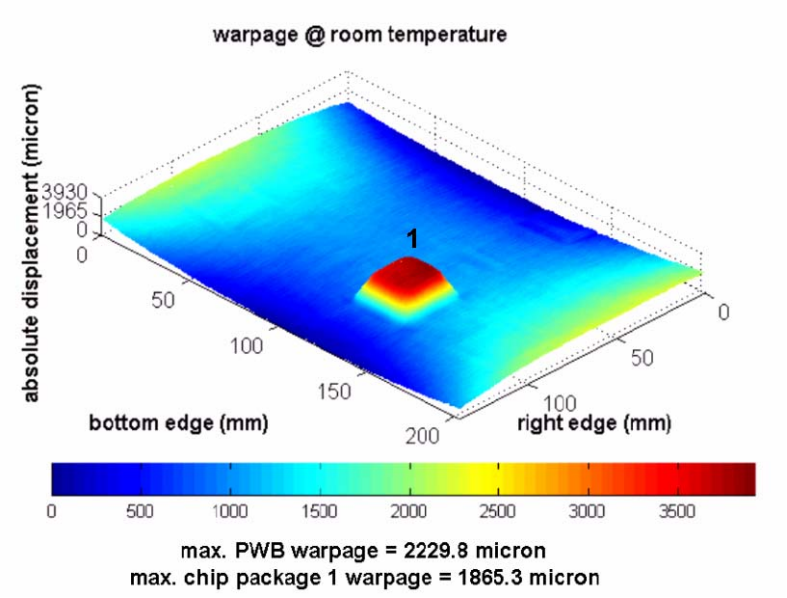


Figure 4.7. Warpage Measurement Plot of PWB with 27 × 27 mm PBGA Package Based on Snake Model

The automatic package segmentation algorithms can be used for the PWBs populated with more than one electronic package. The packages can be assembled at any location on the board and with any directional angle to the PWB edges. A 20 × 20 mm quad flat package (QFP) and a 27 × 27 mm PBGA were arbitrarily placed on the PWB sample with different directional angles to the board edges. The PWB and 27 × 27 mm PBGA are the same test samples as shown in Figures 4.5 and 4.6. The 20 × 20 mm QFP has the maximum warpage of 1028.1 microns which is measured by the projection moiré system. Figure 4.8 shows the warpage measurement plot for the PWBA with the above two packages based on the mask image model segmentation approach. Figure 4.9 shows the warpage result for the PWBA with the same two packages based on the snake segmentation method. For both cases, the maximum warpage results of each chip

package and the PWB have less than 0.5 % difference when compared with their warpage values before they were assembled.

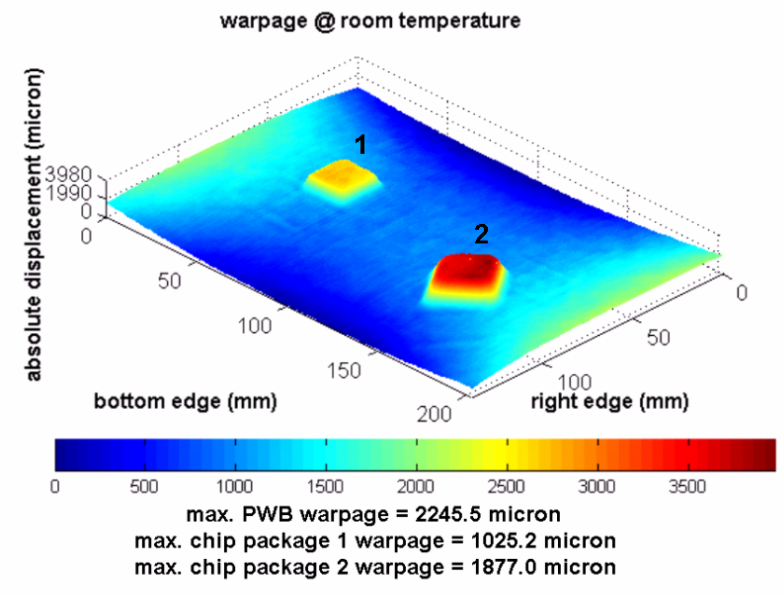


Figure 4.8. Warpage Measurement Plot of PWB with QFP (1) and PBGA (2) Based on Mask Image Model

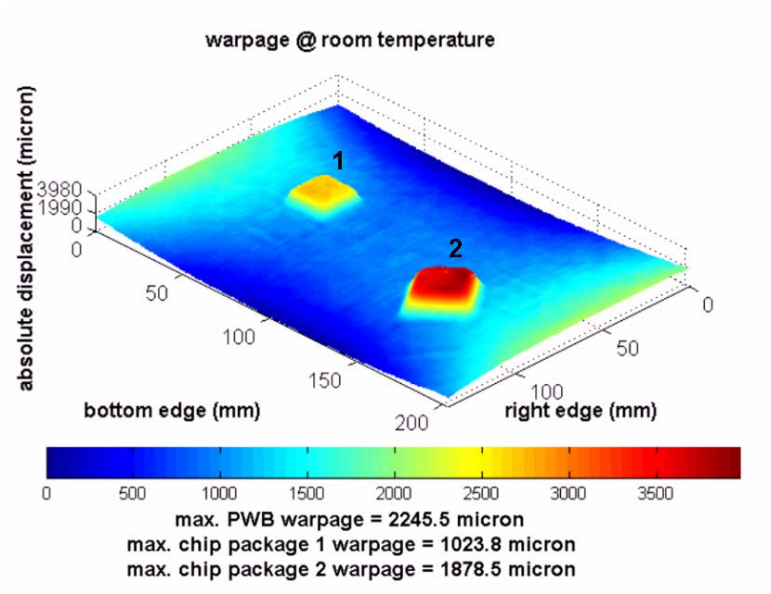


Figure 4.9. Warpage Measurement Plot of PWB with QFP (1) and PBGA (2) Based on Snake Model

One of the advantages of the automatic mask image model is that it can be used to evaluate the warpage of chip packages with small dimensions. A 10 × 10 mm chip scale package (CSP) was used in this research. The CSP has 81 solder bumps and 1.0 mm bump pitch. The maximum warpage across the CSP is 504.0 microns, which was measured by the projection moiré system. The above CSP and the 27 × 27 mm PBGA shown in Figure 4.6 were loosely placed on the PWB sample as shown in Figure 4.5. The projection moiré system with the mask image segmentation algorithm was used to measure the warpage across each package and the PWB respectively. Figure 4.10 shows that the maximum warpage across the CSP is 501.2 microns, which is 0.6 % different from the warpage value of 504.0 microns before assembly. When the same set of measurements was repeated with the snake algorithm, the maximum warpage across the CSP is 458.5 microns, and 9.0 % difference was obtained. The results show that the snake segmentation algorithm is not suitable to process the chip packages with the dimensions less than 10 × 10 mm. This is because the snake model has limited number of points to determine the exterior contour of the small package, and this causes large measurement errors.

In order to show the automatic mask image model can be used to evaluate the warpage of the chip package with small dimension, a 5 × 5 mm CSP package was used. The CSP has 64 solder bumps and 0.5 mm bump pitch. The maximum warpage across the CSP is 432.8 microns, which was measured by the projection moiré system. The above CSP package was loosely placed on a PWB sample with the maximum warpage of 2143.4 microns. The projection moiré system with the mask image segmentation algorithm was used to measure the warpage across the CSP and the PWB respectively.

Figure 4.11 shows that the maximum warpage across the CSP is 434.4 microns, which has 0.4 % difference with the warpage value of 432.8 microns before assembly.

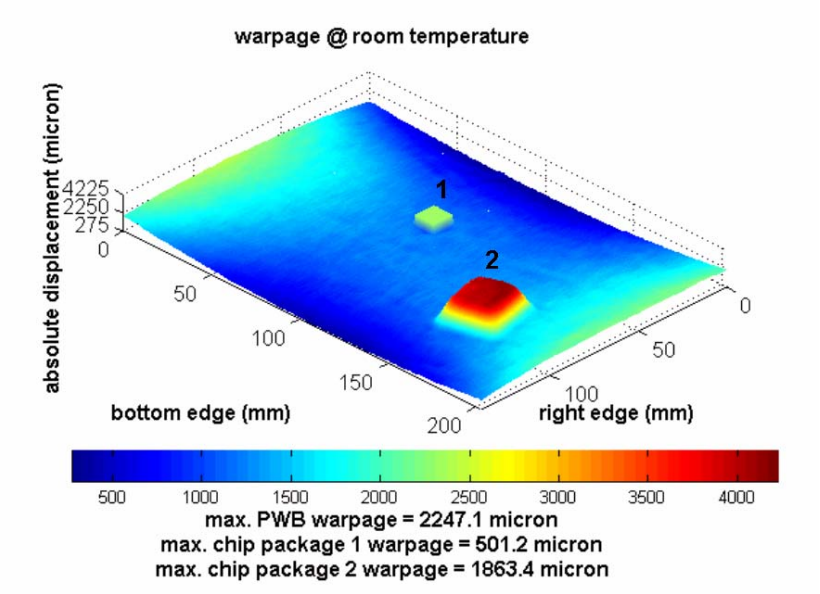


Figure 4.10. Warpage Measurement Plot of PWB with CSP (1) and PBGA (2) Based on Mask Image Model

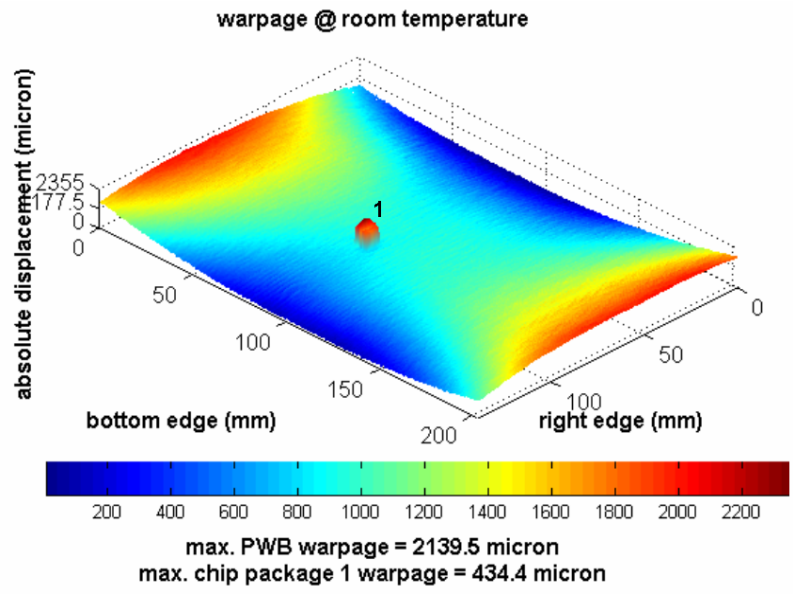


Figure 4.11. Warpage Measurement Plot of PWB with 5 × 5 mm CSP Based on Mask Image Model

4.3.2. Automatic Image Segmentation Algorithm Comparisons

Based on the above experimental studies, the performances of the mask image and snake segmentation algorithms were compared. For the PWBA populated with electronic packages with the dimensions larger than 10 × 10 mm, both the mask image model and snake model can be used to accurately process the warpage of the PWB and chip packages respectively. To accurately measure the warpage across the chip packages with the dimensions less than 10 × 10 mm, the mask image segmentation algorithm is more suitable. Both automatic package segmentation algorithms are able to evaluate the warpage of the PWB populated with multiple electronic packages. Using the mask image segmentation algorithm, the required detecting and processing time for the PWBA with one package is 4.72 seconds, and for the PWBA with two packages is 5.01 seconds. When the snake model is used, the required processing time for the PWBA with one package is 8.59 seconds, and for the PWBA with two packages is 9.84 seconds. The applied computer has 1.8 GHz CPU and 512 MB RAM. Therefore, the mask image segmentation method has higher measurement efficiency than the snake model method. The detailed comparisons between the two automatic image segmentation algorithms and the manual segmentation method are shown in Table 4.1.

Table 4.1. Comparison of Different Image Segmentation Algorithms

Image Segmentation Algorithm	Manual Method	Snake Model	Mask Image Model
Resolution	Low	High	High
Small Package Measurement	Possible	Suitable	Suitable
Multiple Package Measurement	Possible	Suitable	Suitable
Package Locations	Needed	Not Needed	Not Needed
Variability	Moderate	Good	Good
Digital Image Processing	Easy	Complex	Complex
Calculation	Easy	Complex	Moderate
Processing Rate	Low	Moderate	High
Measurement Efficiency	Low	Moderate	High

4.4. Chapter Summary

In this study, the automatic package segmentation algorithms based on the mask image model and snake model were developed for the projection moiré warpage measurement system. The mask image model can be generated by defining the pixel values inside the package area to be 1's, and outside the package area to be 0's; the snake model can converge to the exterior boundaries of chip packages by using the Greedy algorithm. Based on these segmentation algorithms, the improved projection moiré system can be used to measure the warpage across the PWB and assembled omnidirectional electronic packages respectively and accurately. Both the mask image

model and snake model can be used for real-time warpage measurements, and both have high resolutions to determine the warpage across the PWB and populated multiple chip packages. The mask image segmentation method has higher processing rate, and is better suited to evaluate the warpage of packages with small dimensions than the snake model. The real-time continuous and composite Hermite surface models are able to evaluate the PWB warpage values directly underneath the chip packages from the PWBA displacement images. The experimental measurements of the PWBAs with different types of electronic packages show that the projection moiré system with the two automatic image segmentation algorithms is able to measure the warpage across PWBs and multiple chip packages individually with high resolution. The performances of the two automatic algorithms and manual segmentation method were evaluated and compared to illustrate their suitability and flexibility for real-time warpage measurements in this research.

CHAPTER 5

EXPERIMENTAL STUDY OF PWBA WARPAGE BEHAVIOR USING CONVECTIVE REFLOW-PROJECTION MOIRÉ MEASUREMENT SYSTEM

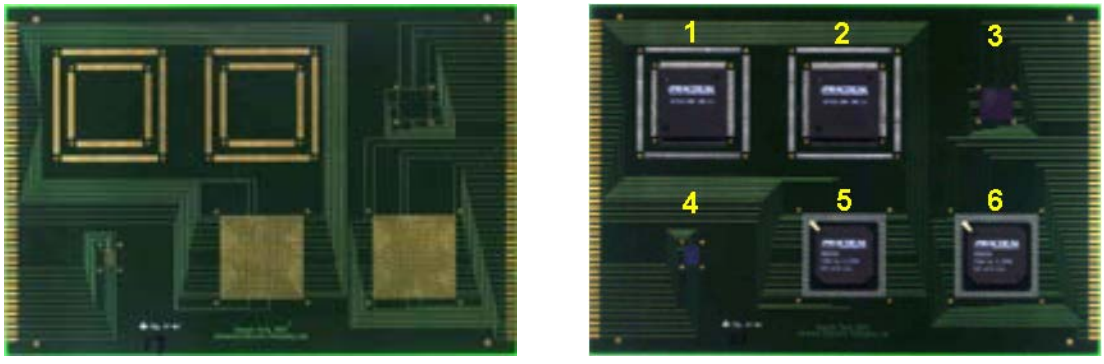
In this study, the warpage behavior of printed wiring board assemblies (PWBAs) during thermal reflow soldering processes was studied using the convective reflow-projection moiré measurement system. The PWB test vehicles used here were assembled with different types of electronic packages to study the board and package warpage behavior through the convective reflow processes. The typical ramp to dwell, ramp to peak (RDRP) reflow profile and Lee optimized reflow profile were simulated using the developed convective heating system. The projection moiré technique was used to measure the real-time warpage values across the PWBA samples during each thermal reflow process. The effects of package size, package location, package number, and different temperature profiles on the PWBA warpage change were discussed in details. This study led to a better understanding of warpage behavior across the PWB and electronic packages during and after the thermal reflow soldering processes. In addition, a repeatability study was performed to show the suitability and reliability of the projection moiré system for online experimental measurement.

5.1. PWBA Test Vehicles

The applied PWBA test vehicles consist of a 203.2 mm by 139.7 mm by 0.631 mm PWB and different electronic packages, including chip scale package (CSP), flip

chip (FC), plastic ball grid array (PBGA), and quad flat pack (QFP) packages. The PWB is composed of four copper layers and three FR-4 layers. The copper layers are half-ounce copper foils with the thickness of 18 μm. Specifically, the top copper layer on the PWB contains traces, which are 127 μm thick and have a pitch of 508 μm. The surface finish of the substrate bond pads is electroless nickel/immersion gold [Powell, 2006]. Figure 5.1 shows the bare PWB sample and the assembled PWBA sample with different types of electronic packages. Figure 5.2 shows the cross-section schematic of the PWB test vehicle.

Total 6 surface mount components can be assembled on the PWB sample as shown in Figure 5.1 (b). Two QFP packages with the dimension of 28 mm × 28 mm or 40 mm × 40 mm can be assembled at Location 1 and 2, respectively; a flip chip with the dimension of 12.7 mm × 12.7 mm can be assembled at Location 3; a CSP package with the dimension of 5.76 mm × 7.87 mm can be assembled at Location 4; two PBGA packages with the dimension of 27 mm × 27 mm or 35 mm × 35 mm can be assembled at Location 5 and 6, respectively.



(a) (b)

Figure 5.1. Bare PWB Sample (a) and Assembled PWBA Sample (b)

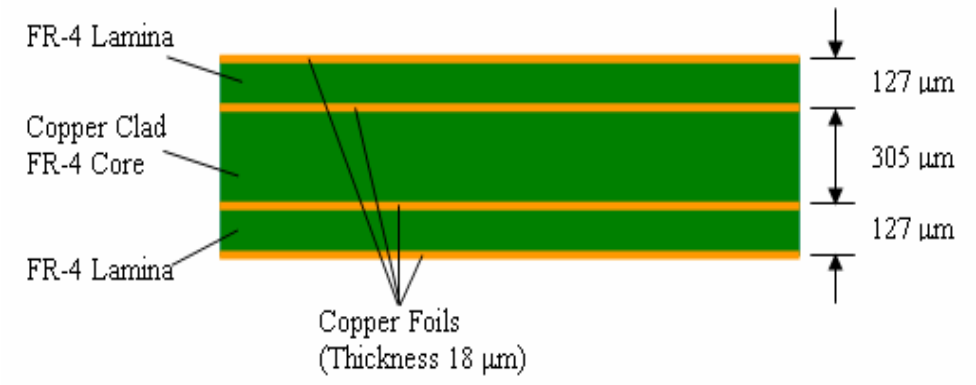


Figure 5.2. Cross-Section Schematic of Test Vehicle PWB

5.2. Experimental PWBA Warpage Measurement During Thermal Convective Reflow Processes

The convective reflow and projection moiré measurement system described in the previous chapters was used to measure the real-time warpage behavior of the PWBA test vehicles during different convective reflow processes. Typical RDRP reflow profile shown in Figure 3.9 and Lee optimized reflow profile shown in Figure 3.10 were used in this study. Three different PWBA structure configurations were considered. Configuration 1 is the PWB assembled with one 35 mm × 35 mm PBGA at Location 6; configuration 2 is the PWB assembled with two 35 mm × 35 mm PBGAs at Location 5 and 6 respectively; configuration 3 is the PWB assembled with 6 chip packages at every location. Each configuration was used to conduct both the RDRP and Lee convective reflow profiles. The projection moiré technique was used to measure the PWBA warpage at initial room temperature, 150 °C heating, 210 °C, 150 °C cooling, and final room temperature. The temperatures of 150 °C and 210 °C were chosen because they are the dwell temperature and peak temperature in the thermal reflow profiles, respectively.

The warpage measurement results of the PWBA with one 35 mm × 35 mm PBGA at initial room temperature, 150 °C heating, 210 °C, 150 °C cooling, and final room temperature during the RDRP reflow profile are shown in Figures 5.3 – 5.7.

The warpage measurement results of the PWBA with one 35 mm × 35 mm PBGA at 210 °C during Lee optimized reflow profile are shown in Figure 5.8.

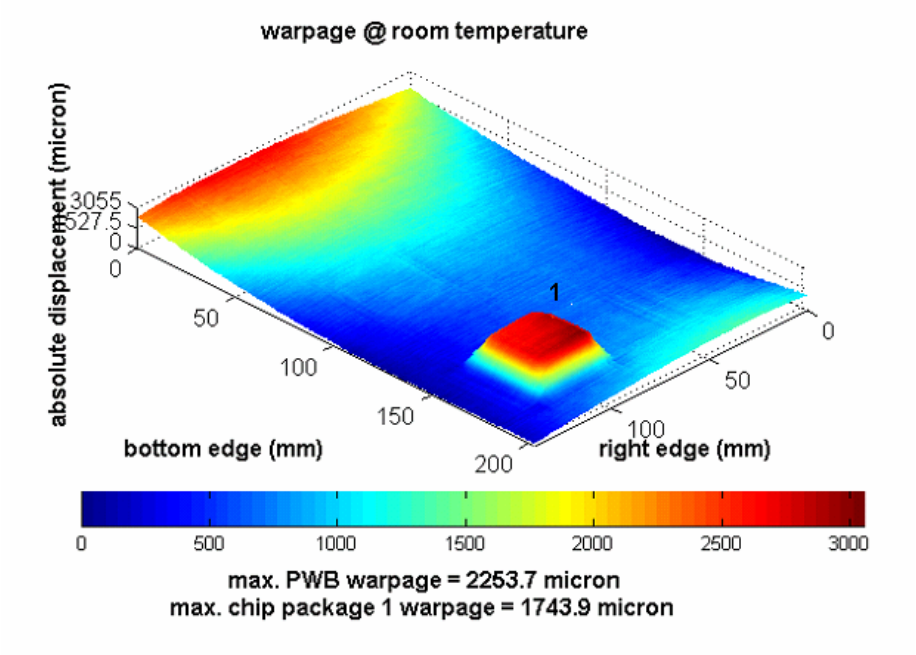


Figure 5.3. Warpage Measurement Plot of PWBA with 1 PBGA at Initial Room Temperature During RDRP Reflow Profile

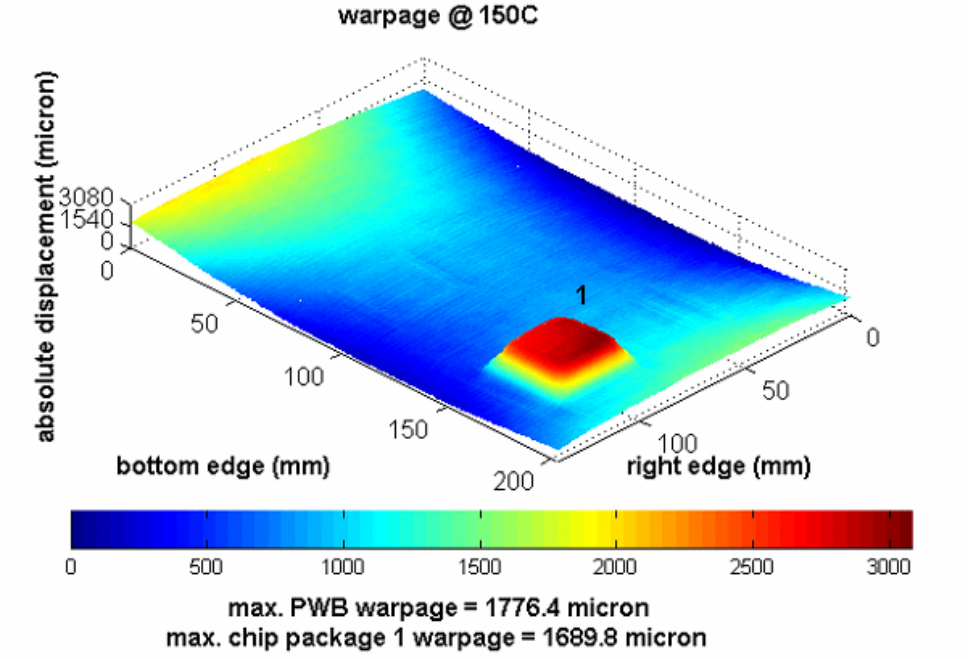


Figure 5.4. Warpage Measurement Plot of PWBA with 1 PBGA at 150 °C Heating During RDRP Reflow Profile

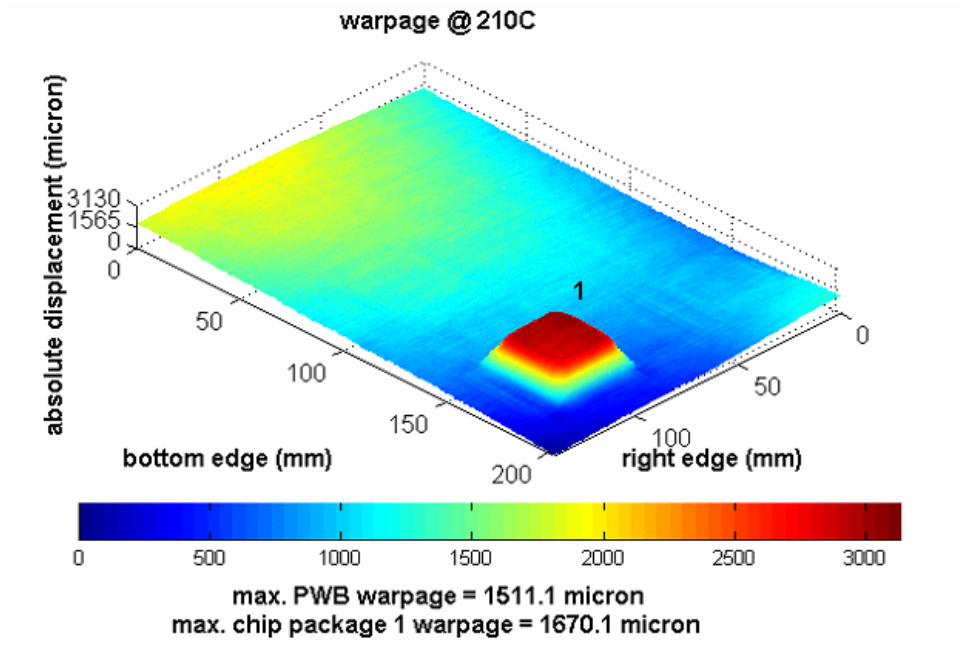


Figure 5.5. Warpage Measurement Plot of PWBA with 1 PBGA at 210 °C During RDRP Reflow Profile

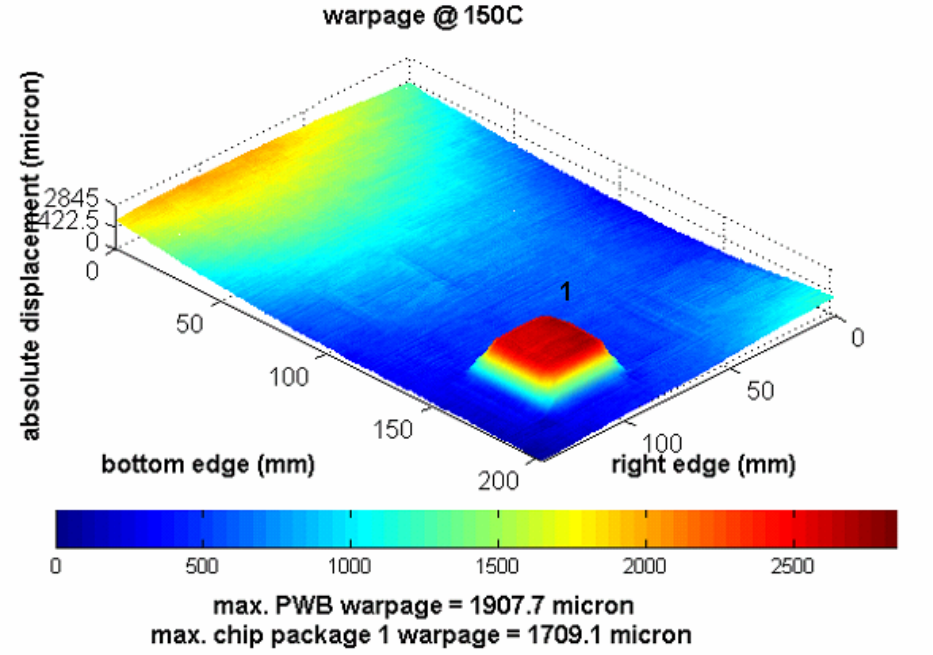


Figure 5.6. Warpage Measurement Plot of PWBA with 1 PBGA at 150 °C Cooling During RDRP Reflow Profile

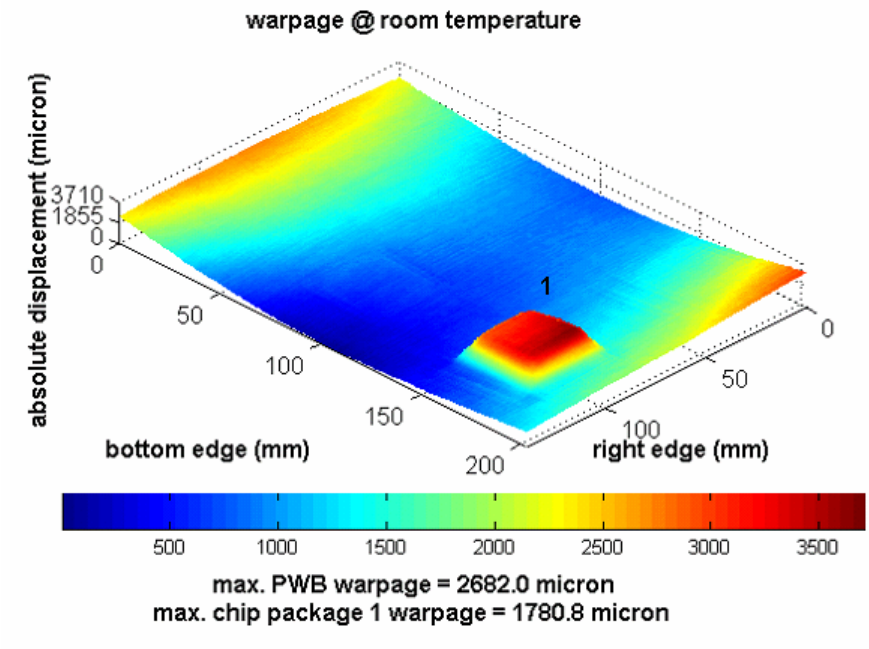


Figure 5.7. Warpage Measurement Plot of PWBA with 1 PBGA at Final Room Temperature During RDRP Reflow Profile

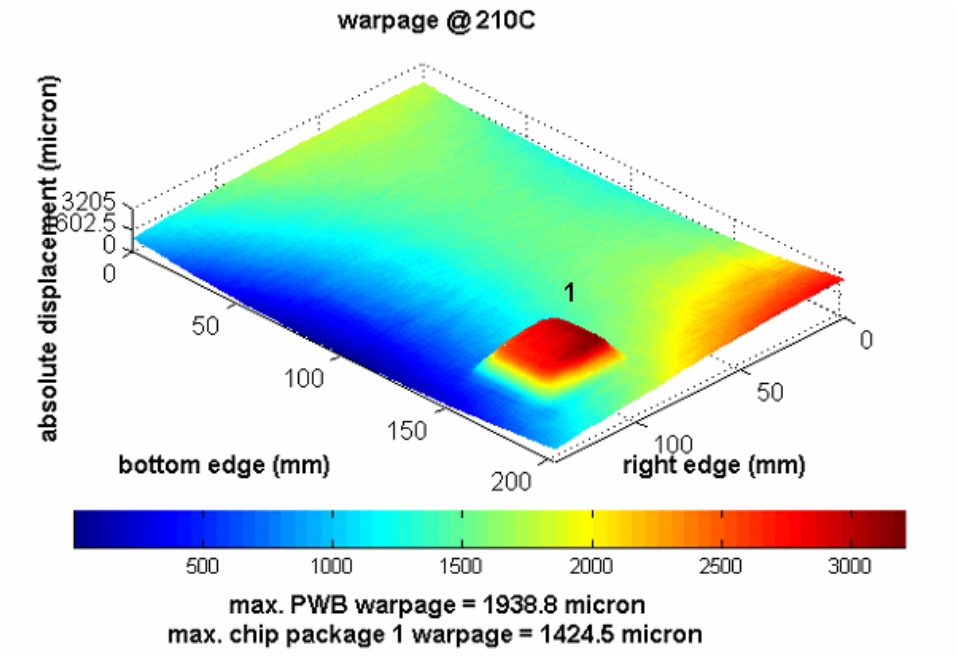


Figure 5.8. Warpage Measurement Plot of PWBA with 1 PBGA at 210 °C During Lee Optimized Reflow Profile

The warpage measurement results of the PWBA with two 35 mm × 35 mm PBGAs at initial room temperature, 150 °C heating, 210 °C, 150 °C cooling, and final room temperature during the RDRP reflow profile are shown in Figures 5.9 – 5.13.

The warpage measurement results of the PWBA with two 35 mm × 35 mm PBGAs at 150 °C heating, 210 °C, 150 °C cooling, and final room temperature during Lee optimized reflow profile are shown in Figures 5.14 – 5.17.

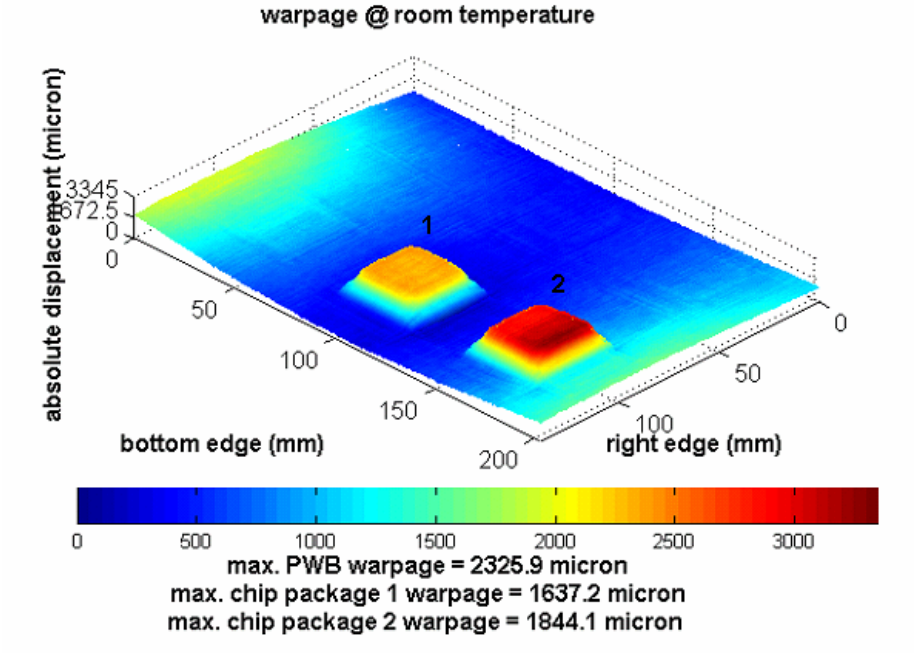


Figure 5.9. Warpage Measurement Plot of PWBA with 2 PBGAs at Initial Room Temperature During RDRP Reflow Profile

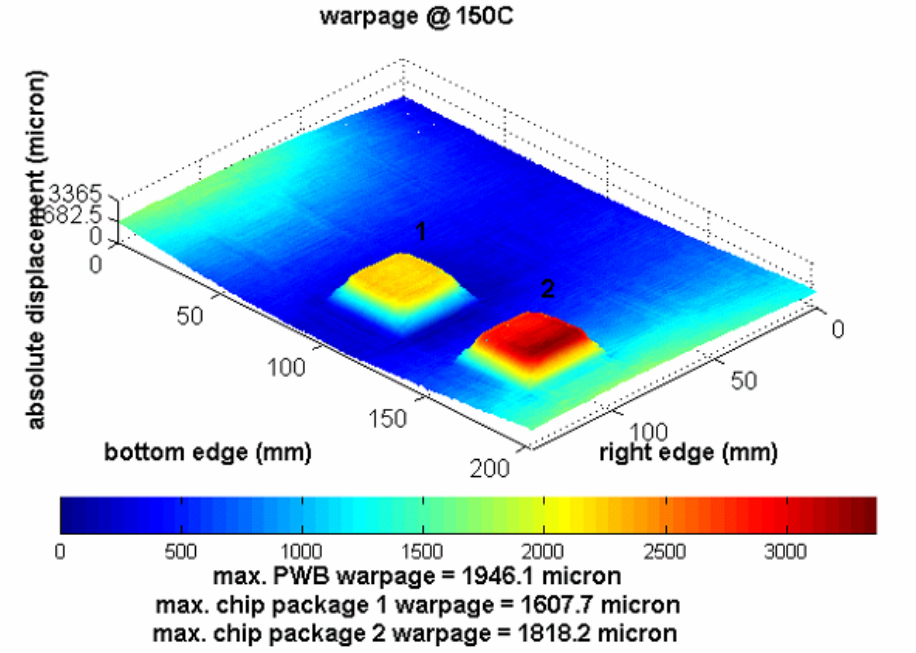


Figure 5.10. Warpage Measurement Plot of PWBA with 2 PBGAs at 150 °C Heating During RDRP Reflow Profile

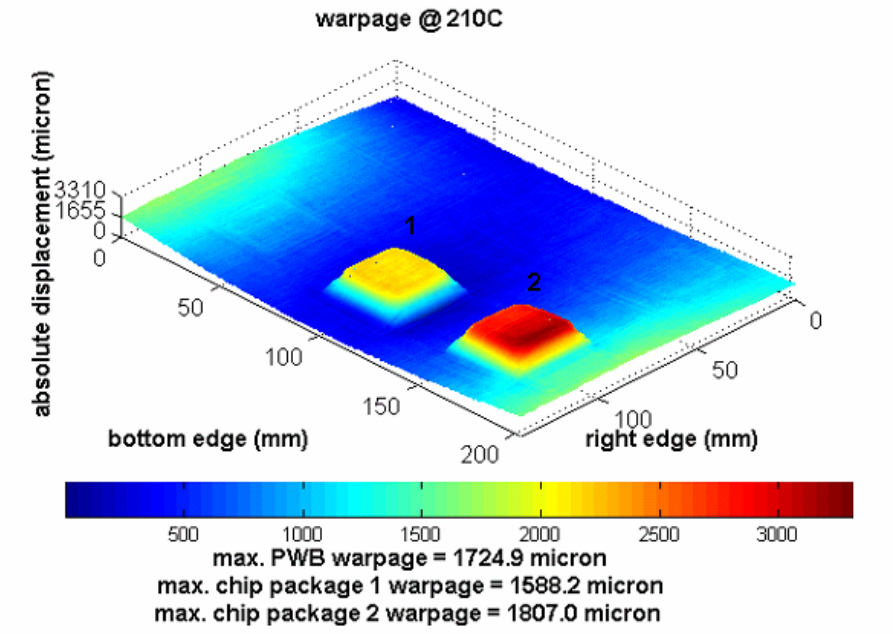


Figure 5.11. Warpage Measurement Plot of PWBA with 2 PBGAs at 210 °C During RDRP Reflow Profile

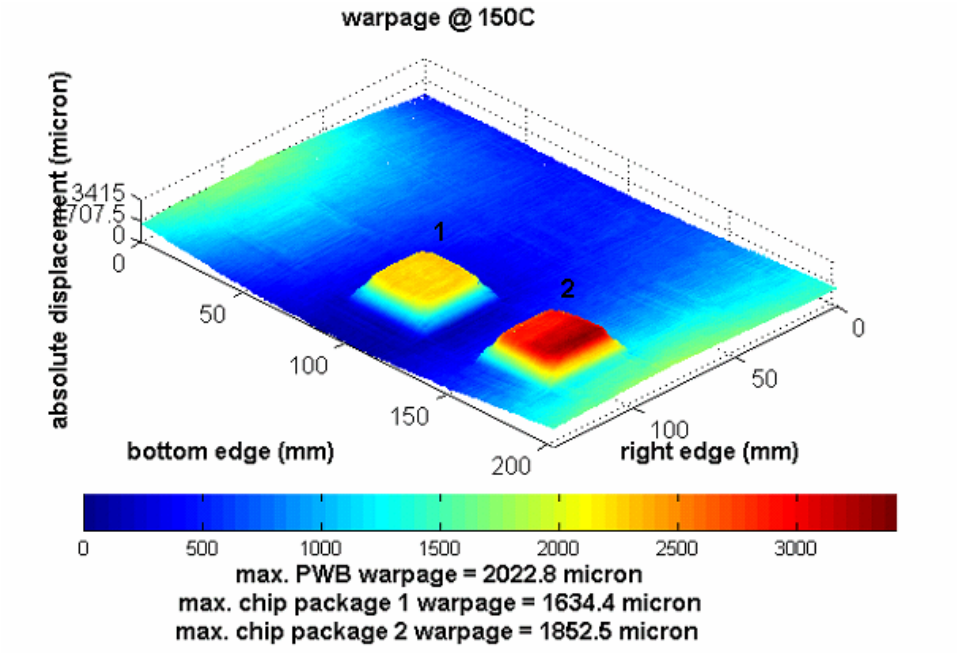


Figure 5.12. Warpage Measurement Plot of PWBA with 2 PBGAs at 150 °C Cooling During RDRP Reflow Profile

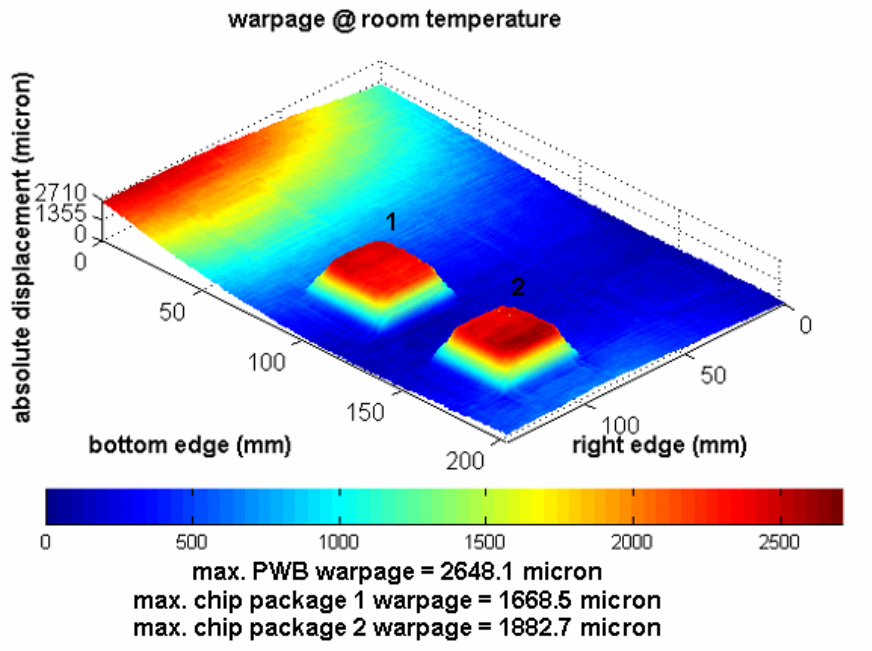


Figure 5.13. Warpage Measurement Plot of PWBA with 2 PBGAs at Final Room Temperature During RDRP Reflow Profile

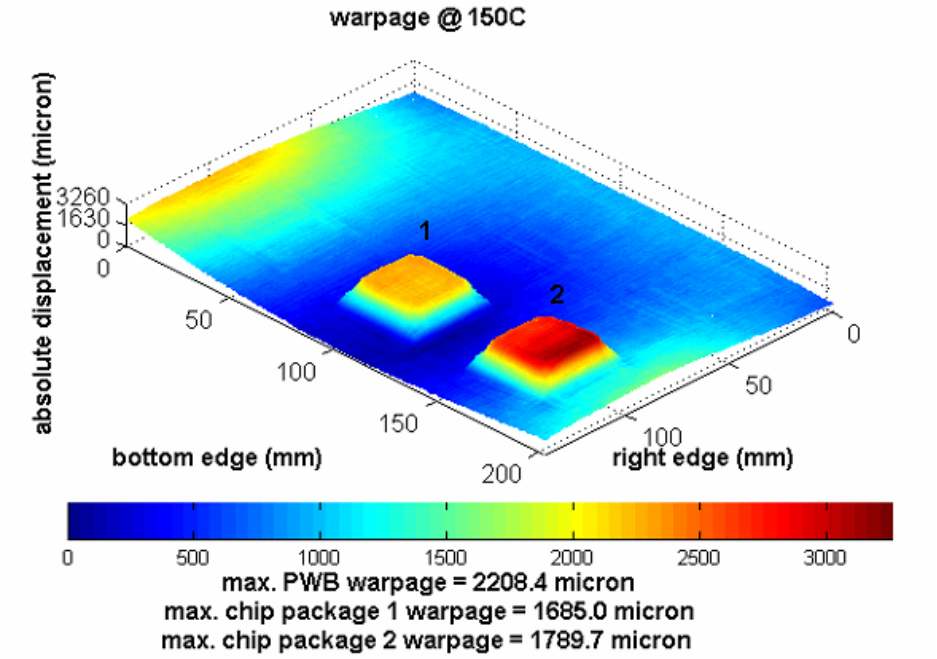


Figure 5.14. Warpage Measurement Plot of PWBA with 2 PBGAs at 150 °C Heating During Lee Optimized Reflow Profile

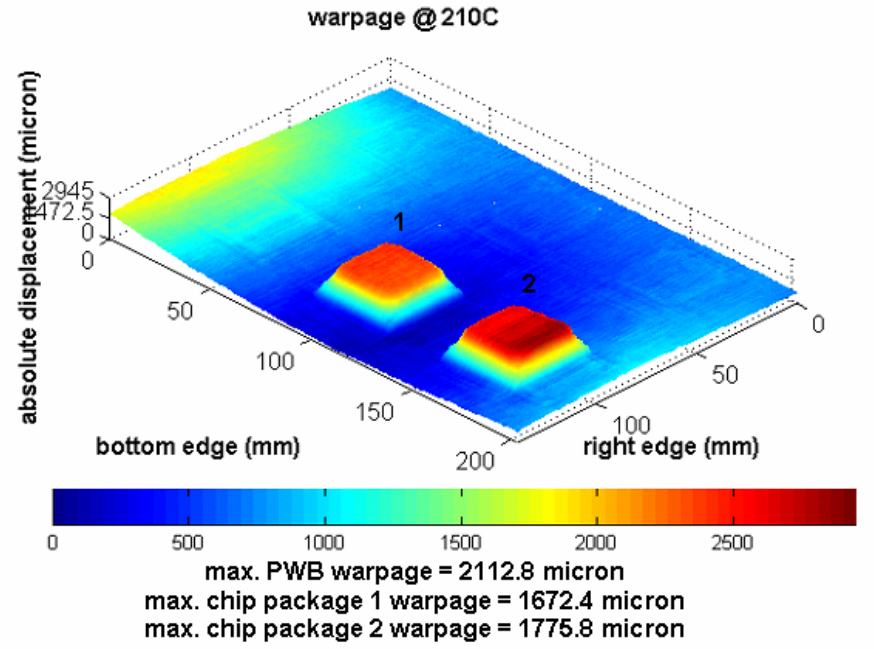


Figure 5.15. Warpage Measurement Plot of PWBA with 2 PBGAs at 210 °C During Lee Optimized Reflow Profile

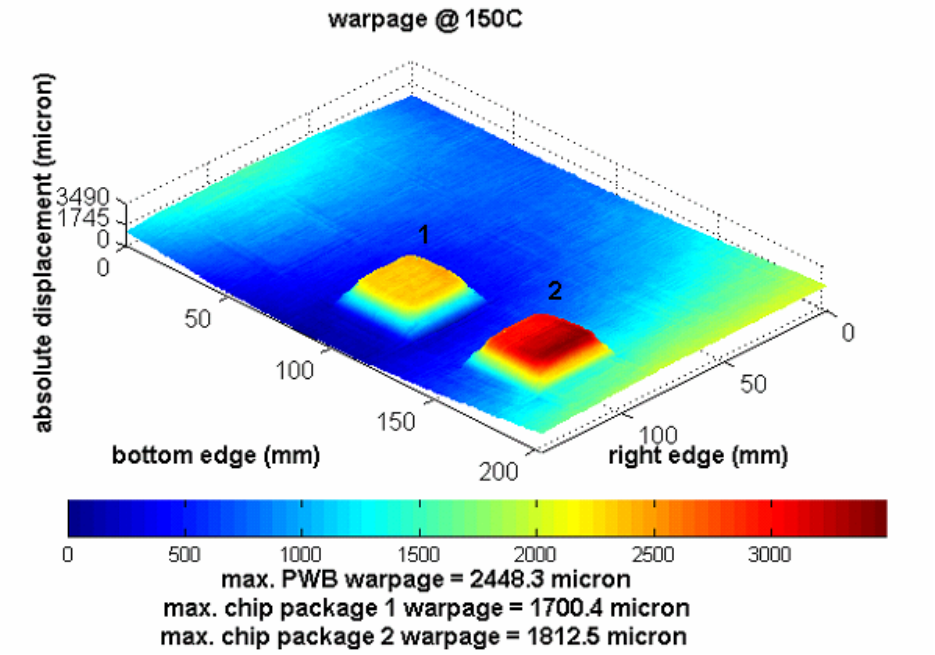


Figure 5.16. Warpage Measurement Plot of PWBA with 2 PBGAs at 150 °C Cooling During Lee Optimized Reflow Profile

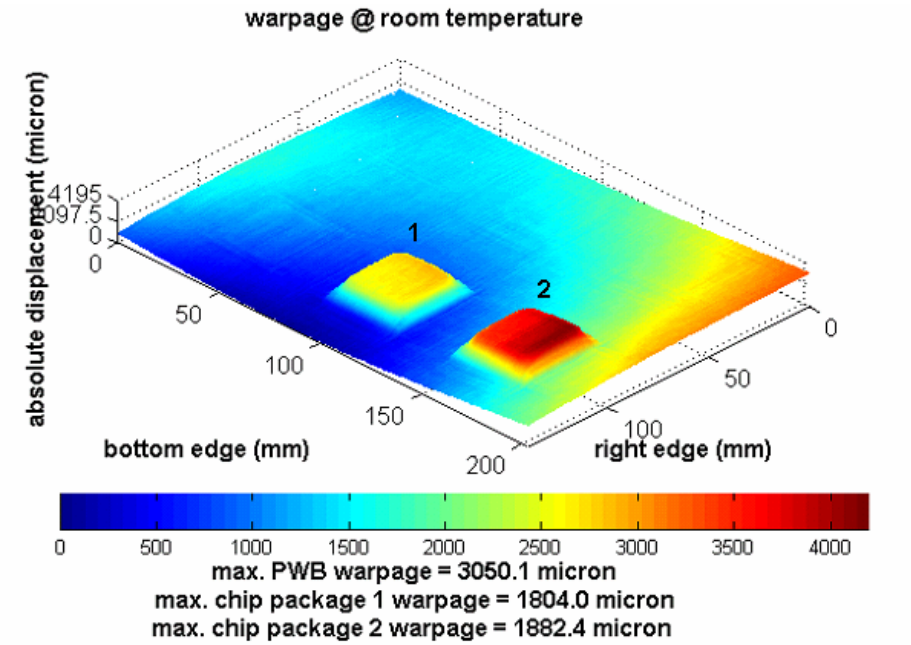


Figure 5.17. Warpage Measurement Plot of PWBA with 2 PBGAs at Final Room Temperature During Lee Optimized Reflow Profile

The warpage measurement results of the PWBA with 6 electronic packages at 150 °C heating and final room temperature during the RDRP reflow profile are shown in Figures 5.18 – 5.19. Two QFP packages with the dimension of 28 mm × 28 mm were assembled at Location 1 and 2, respectively; a flip chip with the dimension of 12.7 mm × 12.7 mm was assembled at Location 3; a CSP package with the dimension of 5.76 mm × 7.87 mm was assembled at Location 4; and two PBGA packages with the dimension of 27 mm × 27 mm were assembled at Location 5 and 6, respectively.

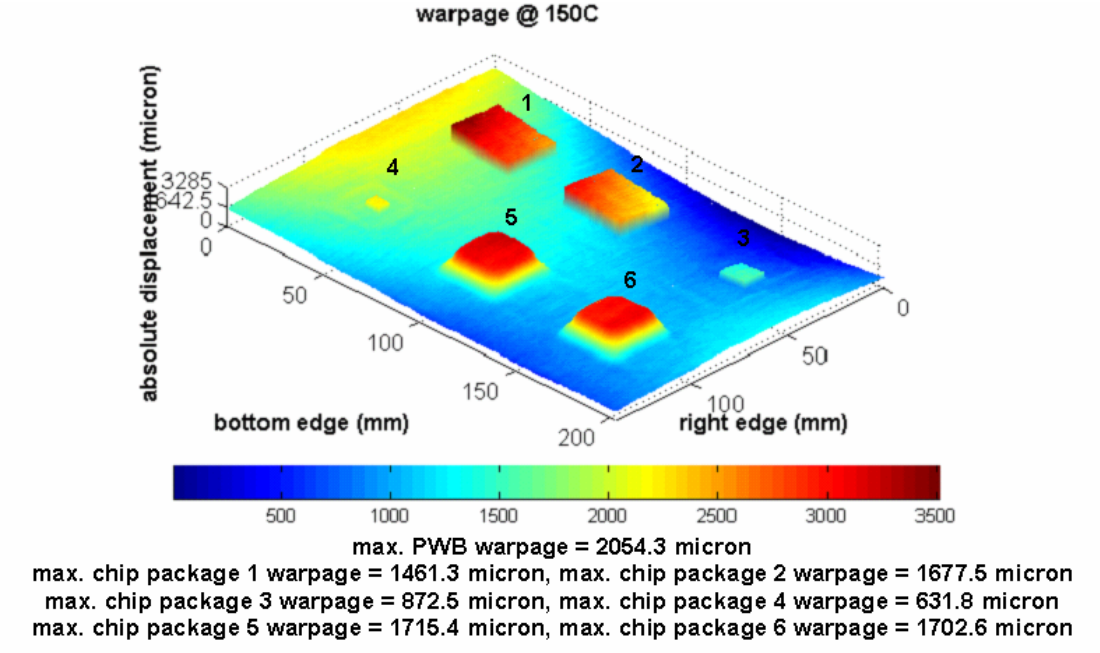


Figure 5.18. Warpage Measurement Plot of PWBA with 6 Chip Packages at 150 °C Heating During RDRP Reflow Profile

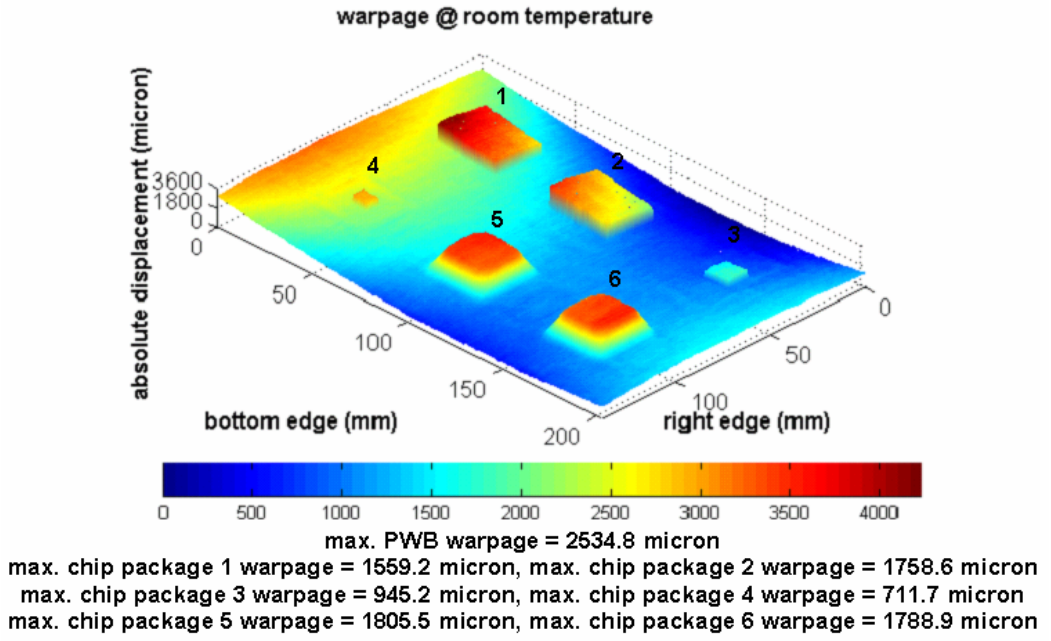


Figure 5.19. Warpage Measurement Plot of PWBA with 6 Chip Packages at Final Room Temperature During RDRP Reflow Profile

Table 5.1 shows the maximum warpage measurement results for the above 3 different PWBA configurations. Table 5.2 and Figure 5.20 show the relative measurement results of the maximum PWB warpage for the 3 PWBA configurations with respect to the warpage values at initial room temperature.

Table 5.1. Maximum Warpage Measurement Results for PWBA Configurations

PWBA Configurations	**Max. PWB Warpage of PWBA with 1 PBGA (μm)**		**Max. PWB Warpage of PWBA with 2 PBGAs (μm)**		**Max. PWB Warpage of PWBA with 6 Packages (μm)**	
Temperature Profile	RDRP	Lee	RDRP	Lee	RDRP	Lee
Initial Room Temperature	2253.7	2517.7	2325.9	2613.3	2301.1	2441.5
150 °C Heating	1776.4	2089.5	1946.1	2208.4	2054.3	2269.6
210 °C	1511.1	1938.8	1724.9	2112.8	1881.9	2097.3
150 °C Cooling	1907.7	2277.5	2022.8	2448.3	2186.8	2352.2
Final Room Temperature	2682.0	3040.0	2648.1	3050.1	2534.8	2755.8

Table 5.2. Relative Warpage Measurement Results for PWBA Configurations

PWBA Configurations	**Max. PWB Warpage of PWBA with 1 PBGA (μm)**		**Max. PWB Warpage of PWBA with 2 PBGAs (μm)**		**Max. PWB Warpage of PWBA with 6 Packages (μm)**	
Temperature Profile	RDRP	Lee	RDRP	Lee	RDRP	Lee
150 °C Heating	-477.2	-428.2	-379.8	-404.9	-246.8	-171.9
210 °C	-742.6	-578.9	-601.0	-500.5	-419.2	-341.2
150 °C Cooling	-346.0	-240.1	-303.1	-165.0	-114.3	-89.3
Final Room Temperature	428.3	522.3	322.2	436.8	233.7	314.3

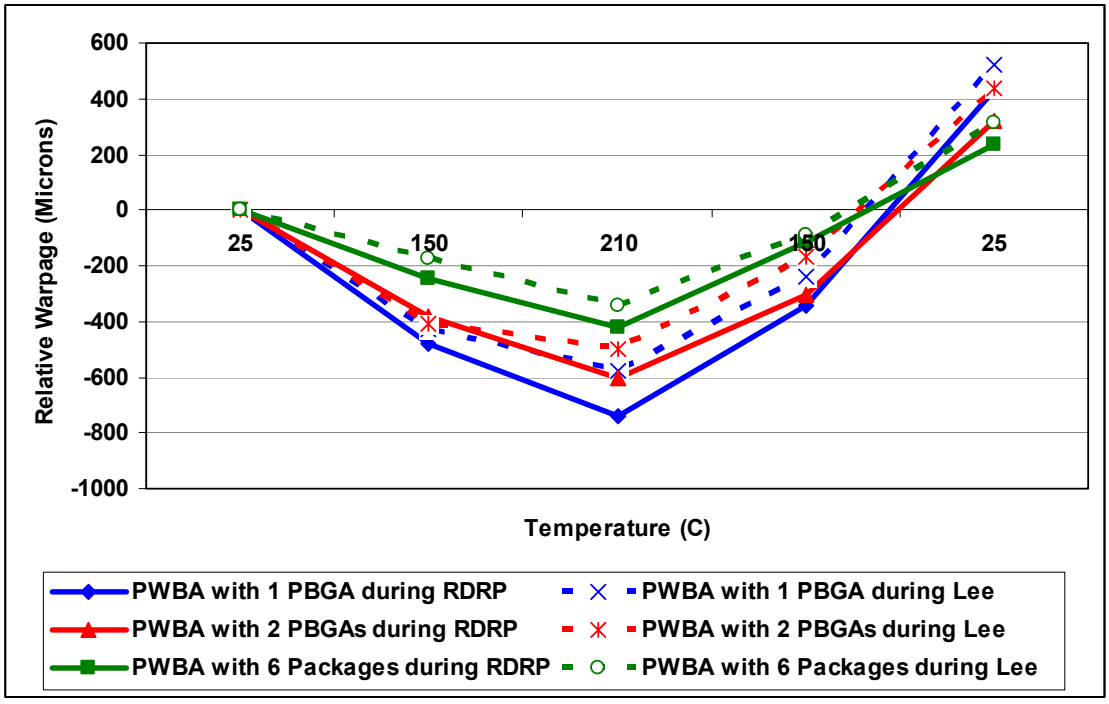


Figure 5.20. Relative Warpage Measurement Results of PWBA Configurations During RDRP and Lee Reflow Profiles

5.3. Discussion of PWBA Sample Warpage Measurement Results

The warpage of the PWBs populated with different electronic packages were measured, and the results are shown in Section 5.2. As shown in the previous PWBA warpage plots, for each assembly configuration, the PWB has a concave upward shape. With the temperature increasing from initial room temperature to the dwell temperature of 150 °C, and then to the peak temperature of 210 °C, the maximum warpage of the PWB and the assembled electronic packages decreased. When the temperature changed from the peak temperature back to the final room temperature, the maximum warpage of the PWB and the assembled packages increased. For each PWBA test vehicle used in this study, the maximum warpage values of the PWB and the packages at room temperature

after the convective reflow process are larger than the maximum warpage values at initial room temperature before the process. Table 5.1 shows the warpage measurement results for PWBA samples assembled with different electronic packages. The increased residual warpage across the PWBAs may cause thermal and mechanical reliability issues in the assemblies.

Figure 5.20 shows that the RDRP reflow profile and Lee optimized reflow profile have different effects on the warpage behavior of the PWBA test vehicles as the temperature changes. For the same PWBA configuration, the relative changes of the maximum warpage across the PWB and assembled chip packages are smaller during Lee optimized profile than those occurring during the RDRP profile. However, after Lee optimized profile, the PWBAs have larger residual warpage than those using the RDRP profile. This is because the RDRP reflow profile has a higher heating ramp rate and shorter process time period than Lee optimized reflow profile. Therefore, using the typical RDRP reflow profile can not only decrease the residual warpage across the PWBAs, it can also save time and cost of the surface mount assembly process. But note that the excessive temperature heating rate of higher than 4 °C/second may cause thermal shock during the reflow profile.

The experimental results show that with the increasing number of the assembled electronic packages, the maximum warpage change of the PWBA configurations decreased during the thermal reflow processes. The electronic packages have constraining effects on the PWB warpage change. Also, the packages in large size and assembled near the PWB center have larger constraining effects on board warpage than those in smaller size and assembled far from the board center. Different types of

packages have various effects on PWB warpage. PBGAs have larger effects on assembly warpage than FCs, CSPs, and QFPs because of their large size and small solder bump pitches.

5.4. Repeatability Study on Projection Moiré Measurement System

A repeatability study on the projection moiré warpage measurement system was conducted to determine the system suitability and reliability for online measurements. The projection moiré system was used to measure a PWB populated with one 35 mm × 35 mm PBGA at Location 6 at room temperature. The experimental measurement was performed 10 times for the same PWBA test vehicle. Table 5.3 shows the 10-run warpage measurement results of the PWB sample.

Table 5.3. PWBA Warpage Measurement Results for Repeatability Study

Measurement	Maximum PWB Warpage Value of PWBA with One PBGA (μm)
1	1814.2
2	1824.8
3	1819.4
4	1828.7
5	1817.9
6	1828.1
7	1826.4
8	1813.5
9	1825.5
10	1829.0

Based on the maximum warpage values across the PWB as shown in Table 5.3, the average maximum warpage value across the PWB is 1822.8, and the standard deviation is 5.9. The warpage confidence interval for the experimental measurement can be calculated using Equation (5.1).

$$w_{CI} = w_{avg} \pm z(\frac{\alpha}{2})\frac{\sigma}{\sqrt{n}} \tag{5.1}$$

where, w_{CI} = warpage confidence interval

w_{avg} = average warpage value

$z(\alpha/2)$ = 2.0 for 95 % confidence interval

σ = warpage standard deviation

n = number of measurement

Based on Equation (5.1), the warpage confidence interval for one experimental measurement is 1822.8 ± 11.8 microns. The repeatability for the projection moiré system is 0.6 %. Therefore, the projection moiré warpage measurement system has excellent suitability and reliability for online experimental measurement.

5.5. Chapter Summary

In this study, the warpage behavior of PWBAs during different thermal reflow soldering processes was studied using the convective reflow and projection moiré measurement system. Three different PWBA configurations were considered here. Configuration 1 is the PWB assembled with one 35 mm × 35 mm PBGA; configuration 2 is the PWB assembled with two 35 mm × 35 mm PBGAs; configuration 3 is the PWB

assembled with 6 chip packages. Each configuration was used to conduct both simulated RDRP and Lee convective reflow profiles. The projection moiré technique was used to measure the PWBA warpage at initial room temperature, 150 °C heating, 210 °C, 150 °C cooling, and final room temperature. The experimental results show the warpage behavior across the PWBs and assembled electronic packages during the thermal reflow processes. After Lee optimized profile, the PWBAs have larger residual warpage than those using the RDRP profile. Therefore, using the typical RDRP reflow profile can not only decrease the residual warpage across the PWBAs, also it can save time and cost of the surface mount assembly process. With the increasing number of electronic packages, the maximum warpage change of the PWBAs decreased during the thermal reflow processes. The electronic packages have constraining effects on PWB warpage change. Also, the packages in large size and assembled near the PWB center have larger constraining effects on board warpage than those in smaller size and assembled far from the board center. Different types of packages have various effects on the PWB warpage. This study provided general guidelines for PWBA layout design and for improving the thermal and mechanical reliability of integrated PWB assemblies. In addition, the repeatability study shows that the projection moiré warpage measurement system has excellent flexibility and reliability for online experimental measurement.

CHAPTER 6

THEORETICAL ANALYSIS OF PWB AND PWBA WARPAGE

The classical laminated plate theory (CLPT) was applied in this chapter to study the warpage behavior of printed wiring boards (PWBs) and PWB assemblies (PWBAs) during the thermal reflow process. The rule of mixtures was used to estimate the material properties of PWBA composites. Closed form solutions of the differential equations for the PWB and PWBA deformation were generated from the classical lamination theory description to evaluate warpage. The board support conditions and thermal gradients through the assembly thickness were considered in the analytical model. The calculated warpage results were compared with experimental results using the projection moiré measurement system in a simulated convective reflow process to evaluate the accuracy of the model. Finite element modeling (FEM) was applied to estimate the sample warpage values under the same thermal loading and boundary constrains.

6.1. Laminated Plate Theory of Composite Materials

A laminate is defined as a stack of layers or laminae, each with orthotropic and quasi-homogeneous properties. A composite lamina is a building block for laminates. Laminae are bonded together to form a laminate with the desired thickness and stiffness. Generally, the thickness of a laminate is small compared to its planar dimensions. The side-to-thickness ratio of a laminate is greater than 20 [Reddy & Miravete, 1995].

The classical laminated plate theory (CLPT) is an extension of the classical plate theory to laminated plates. In CLPT, the in-plane displacements are assumed to vary linearly through the thickness, and the transverse displacement is assumed to be constant

through the thickness. CLPT is found to be adequate for most applications where the thickness of the laminate is small in magnitude compared to the planar dimensions.

Each lamina is characterized by the properties: E_1, E_2, G_{12}, ν_{12}, ν_{21}, α_1, and α_2, where E is Young's modulus, G is shear modulus, ν is Poisson's ratio, and α is the coefficient of thermal expansion (CTE). The subscripts *1* and *2* denote the principal in-plane material directions.

Equation (6.1) shows the stress-strain relationships for a single layer of laminates in the principal material directions.

$$\begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \tau_{12} \end{bmatrix} = \begin{bmatrix} \frac{E_1}{1-\nu_{12}\nu_{21}} & \frac{E_1\nu_{21}}{1-\nu_{12}\nu_{21}} & 0 \\ \frac{E_1\nu_{21}}{1-\nu_{12}\nu_{21}} & \frac{E_{21}}{1-\nu_{12}\nu_{21}} & 0 \\ 0 & 0 & G_{12} \end{bmatrix} \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \gamma_{12} \end{bmatrix} \tag{6.1}$$

The strain terms in Equation (6.1) include the extensional, bending, and thermal components for sufficiently small deflections. Based on the assumption of linear strain, the strains are expressed in terms of displacements as Equation (6.2).

$$\begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \gamma_{12} \end{bmatrix} = \begin{bmatrix} \frac{\partial u_0}{\partial x} - \frac{\partial^2 w_0}{\partial x^2} - \alpha_1 \Delta T \\ \frac{\partial v_0}{\partial y} - \frac{\partial^2 w_0}{\partial y^2} - \alpha_2 \Delta T \\ \frac{\partial u_0}{\partial y} + \frac{\partial v_0}{\partial x} - 2\frac{\partial^2 w_0}{\partial x \partial y} \end{bmatrix} \tag{6.2}$$

where u_0, v_0, and w_0 are the displacements of the laminate mid-plate in the X, Y, and Z directions, respectively.

Then the above stress-train relationships for each layer are transformed into the laminate coordinate system using the standard two-dimensional stress-strain transformations. If each layer of the laminates is isothermal, the forces and moments for the laminates can be calculated according to Equation (6.3) and Equation (6.4) by summing the individual layer stresses [Polsky et al., 1998].

$$\begin{bmatrix} N_x \\ N_y \\ N_{xy} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{16} \\ A_{12} & A_{22} & A_{26} \\ A_{16} & A_{26} & A_{66} \end{bmatrix} \begin{bmatrix} \dfrac{\partial u_0}{\partial x} \\ \dfrac{\partial v_0}{\partial y} \\ \dfrac{\partial u_0}{\partial y} + \dfrac{\partial v_0}{\partial x} \end{bmatrix} - \begin{bmatrix} B_{11} & B_{12} & B_{16} \\ B_{12} & B_{22} & B_{26} \\ B_{16} & B_{26} & B_{66} \end{bmatrix} \begin{bmatrix} \dfrac{\partial^2 w_0}{\partial x^2} \\ \dfrac{\partial^2 w_0}{\partial y^2} \\ 2\dfrac{\partial^2 w_0}{\partial x \partial y} \end{bmatrix} - \begin{bmatrix} N_x{}^T \\ N_y{}^T \\ N_{xy}{}^T \end{bmatrix} \tag{6.3}$$

$$\begin{bmatrix} M_{xx} \\ M_{yy} \\ M_{xy} \end{bmatrix} = \begin{bmatrix} B_{11} & B_{12} & B_{16} \\ B_{12} & B_{22} & B_{26} \\ B_{16} & B_{26} & B_{66} \end{bmatrix} \begin{bmatrix} \dfrac{\partial u_0}{\partial x} \\ \dfrac{\partial v_0}{\partial y} \\ \dfrac{\partial u_0}{\partial y} + \dfrac{\partial v_0}{\partial x} \end{bmatrix} - \begin{bmatrix} D_{11} & D_{12} & D_{16} \\ D_{12} & D_{22} & D_{26} \\ D_{16} & D_{26} & D_{66} \end{bmatrix} \begin{bmatrix} \dfrac{\partial^2 w_0}{\partial x^2} \\ \dfrac{\partial^2 w_0}{\partial y^2} \\ 2\dfrac{\partial^2 w_0}{\partial x \partial y} \end{bmatrix} - \begin{bmatrix} M_{xx}{}^T \\ M_{yy}{}^T \\ M_{xy}{}^T \end{bmatrix} \tag{6.4}$$

where A_{ij}, B_{ij}, and D_{ij} are the extensional, coupling, and bending stiffness, respectively. They can be calculated using Equations (6.5) – (6.7).

$$A_{ij} = \sum_{k=1}^{n} \int_{z_k}^{z_{k+1}} Q_{ij}^{(k)} dz \tag{6.5}$$

$$B_{ij} = \sum_{k=1}^{n} \int_{z_k}^{z_{k+1}} Q_{ij}^{(k)} z dz \tag{6.6}$$

$$D_{ij} = \sum_{k=1}^{n} \int_{z_k}^{z_{k+1}} Q_{ij}^{(k)} z^2 dz \tag{6.7}$$

where n is the number of layers in the laminate and $Q_{ij}^{(k)}$ are the transformed stiffness coefficients of the k^{th} layer relative to the laminate coordinate system.

In Equation (6.3) and Equation (6.4), N^T and M^T can be calculated by using the following equations.

$$\left[N^T\right] = \sum_{k=1}^{n} \int_{z_k}^{z_{k+1}} Q^{(k)} \left[\alpha\right]^{(k)} \Delta T dz \tag{6.8}$$

$$\left[M^T\right] = \sum_{k=1}^{n} \int_{z_k}^{z_{k+1}} Q^{(k)} \left[\alpha\right]^{(k)} \Delta T z dz \tag{6.9}$$

Equation (6.3) and Equation (6.4) can be used to calculate the warpage of the laminate due to CTE differential and thermal gradients based on Equations (6.5) – (6.9). With the assumption that every individual layer is isothermal, Equations (6.10) – (6.12) show the equilibrium for the steady state conditions.

$$\frac{\partial N_x}{\partial x} + \frac{\partial N_{xy}}{\partial y} = 0 \tag{6.10}$$

$$\frac{\partial N_{xy}}{\partial x} + \frac{\partial N_{y}}{\partial y} = 0 \tag{6.11}$$

$$\frac{\partial^2 M_{xx}}{\partial x^2} + 2\frac{\partial^2 M_{xy}}{\partial y \partial x} + \frac{\partial^2 M_{yy}}{\partial y^2} + q + \overline{N}_x \frac{\partial^2 w_0}{\partial x^2} + 2\overline{N}_{xy} \frac{\partial^2 w_0}{\partial x \partial y} + \overline{N}_y \frac{\partial^2 w_0}{\partial y^2} = 0 \tag{6.12}$$

where q is the transverse force, and $\overline{N}_x$, $\overline{N}_{xy}$, and $\overline{N}_y$ are the in-plane applied forces.

The calculated forces and moments from Equation (6.3) and Equation (6.4) are substituted into the above differential equations to obtain three equations for the laminate displacements. Only Equation (6.12) needs to be solved to determine the warpage of the laminate. For the steady-state conditions without in-plane applied forces, the coupling stiffness, B_{ij}, is zero. Therefore, Equation (6.12) was simplified as Equation (6.13) [Reddy & Miravete, 1995].

$$[D_{11} \frac{\partial^4 w_0}{\partial x^4} + 2(D_{12} + 2D_{66}) \frac{\partial^4 w_0}{\partial x^2 \partial y^2} + D_{22} \frac{\partial^4 w_0}{\partial y^4}] - q = 0 \tag{6.13}$$

Equation (6.13) is a linear fourth-order partial differential equation with two independent variables, x and y. If the PWBA sample is a rectangular laminate with length a and width b, and it is simply supported at the ends of $y=0$ and b, the solution for the out-of-plane displacement w_0 has the form as shown in Equation (6.14).

$$w_0(x, y) = \sum_{m=1}^{\infty} W_m(x) \sin(\beta y) \tag{6.14}$$

where $\beta=m\pi/b$ and W_m is the amplitude of w_0.

Equation (6.14) was substituted into Equation (6.13), and then it became Equation (6.15).

$$W_m^{IV} = C_1 W_m + C_2 W_m'' + C_0 Q_m \tag{6.15}$$

$$C_1 = -\frac{D_{22}}{D_{11}}\beta^4,\ C_2 = 2\frac{(D_{12}+D_{66})}{D_{11}}\beta^2,\ C_0 = \frac{1}{D_{11}} \tag{6.16}$$

where Q_m is the Fourier series expansion of the transverse load.

Equation (6.15) is equivalent to a system of four first-order differential equations as shown in Equation (6.17) and Equation (6.18).

$$Z' = AZ + R \tag{6.17}$$

where

$$Z = \begin{bmatrix} W_m \\ W_m' \\ W_m'' \\ W_m''' \end{bmatrix},\ A = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ C_1 & 0 & C_2 & 0 \end{bmatrix},\ R = \begin{bmatrix} 0 \\ 0 \\ 0 \\ C_0 Q_m \end{bmatrix} \tag{6.18}$$

The solution to the above non-homogeneous system of equations is given by Equation (6.19) [Reddy & Miravete, 1995].

$$Z(x) = e^{Ax}K + e^{Ax}\int_0^x e^{-A\eta}Rd\eta \tag{6.19}$$

where K is a vector of constants, which is evaluated using the boundary conditions. The matrix e^{Ax} is defined by Equation (6.20).

$$e^{Ax} = [S]\begin{bmatrix} e^{\lambda_1 x} & 0 & 0 & 0 \\ 0 & e^{\lambda_2 x} & 0 & 0 \\ 0 & 0 & e^{\lambda_3 x} & 0 \\ 0 & 0 & 0 & e^{\lambda_4 x} \end{bmatrix}[S]^{-1} \tag{6.20}$$

where λ_i are the eigenvalues of the matrix A, and S is constructed with the eigenvectors of the matrix A.

For the case of free edges at $x=0$ and a, the boundary conditions are given below.

$$M_{xx} = 0,\ \frac{\partial M_{xx}}{\partial x} + \frac{\partial M_{xy}}{\partial y} = 0 \tag{6.21}$$

Equation (6.19) was substituted into the above boundary conditions. A system of four linear equations with four unknowns can be generated to solve the constant coefficients of K. Then the out-of-plane displacement of the laminate can be evaluated.

6.2. Estimation of Composite Material Properties

In order to further reduce the computational complexity of the analytical study, the effective material properties of PWBs and electronic packages can be used. The

material properties were calculated from their composite material properties using the rule of mixtures.

The rule of mixtures is an effective approach to estimate the composite material properties, based on an assumption that a composite property is the volume weighed average of the matrix and dispersed phase (fiber) properties.

According to the rule of mixtures, the properties of composite materials can be estimated using the following equations.

$$d_c = d_m V_m + d_f V_f \tag{6.22}$$

$$E_{cl} = E_m V_m + E_f V_f \tag{6.23}$$

$$E_{ct} = \frac{E_m E_f}{E_m V_f + E_f V_m} \tag{6.24}$$

$$\nu_c = \nu_m V_m + \nu_f V_f \tag{6.25}$$

$$\alpha_{cl} = \frac{\alpha_m E_m V_m + \alpha_f E_f V_f}{E_m V_m + E_f V_f} \tag{6.26}$$

$$\alpha_{ct} = (1+\nu_m)\alpha_m V_m + (1+\nu_f)\alpha_f V_f - \alpha_{cl}\nu_c \tag{6.27}$$

where, d = density

E = elastic modulus

ν = Poisson's ratio

α = CTE

V = volume fraction

(c, m, f) = (composite, matrix, fiber)

(l, t) = (longitudinal, transverse)

Based on the above equations, the effective material properties of the PWB and plastic ball grid array (PBGA) packages can be calculated. The applied PWB structure is the same as the previous test vehicle as shown in Figure 5.1, with the size of 203.2 mm by 139.7 mm by 0.631 mm. The PBGA packages used in this study has 256 63Sn-37Pb solder bumps, bump pitch of 1.27 mm, and dimension of 27 × 27 mm. The calculated effective material properties are shown in Table 6.1 [Polsky & Ume, 1999; Muncy, 2004; Pang et al., 2004]. These properties can be used in the analytical model to study the warpage of PWBs and PWBAs.

Table 6.1. Effective Material Properties of PWB and PBGA Samples at Room Temperature

Material	CTE (ppm/°C)	Elastic Modulus (GPa)	Poisson's Ratio	Thickness (μm)	Volume Fraction
FR-4	20	22.4	0.15	127,305,127	0.89
Copper Foil	18.9	79.5	0.32	18,18,18,18	0.11
Effective PWB	**19.7**	**28.7**	**0.17**	**631**	**1**
BT Substrate	15.0	14.0	0.15	320	0.25
Package Molding	17.5	15.0	0.15	1170	0.69
63Sn-37Pb	21	19.7	0.4	600	0.06
Effective PBGA	**17.2**	**15.0**	**0.16**	**2090**	**1**

6.3. Theoretical Assessment of PWB/PWBA Warpage

6.3.1. Analytical Modeling and Calculation

The PWB test vehicle used for analytical modeling and validation purpose has four copper layers and a symmetric cross-section structure. It consists of alternating FR-4 and copper layers as shown in Figure 5.2. The 27 × 27 mm PBGA packages were assembled on the PWB sample to study the PWBA warpage during the simulated convective thermal reflow process. The PWB/PWBA samples were subjected to a typical manufacturing reflow profile as shown in Figure 6.1. It is a ramp to dwell, ramp to peak (RDRP) reflow profile. The maximum temperature ramp rate is 1.80 °C/second in the pre-heat zone. The peak temperature is 220 °C. Twelve thermocouples, six on each surface of the board, were used to measure the specimen temperatures during the process, and to evaluate the temperature differences on the samples. The classical laminated plate theory and the rule of mixtures were used to study the warpage behavior of the analytical models during the thermal reflow process.

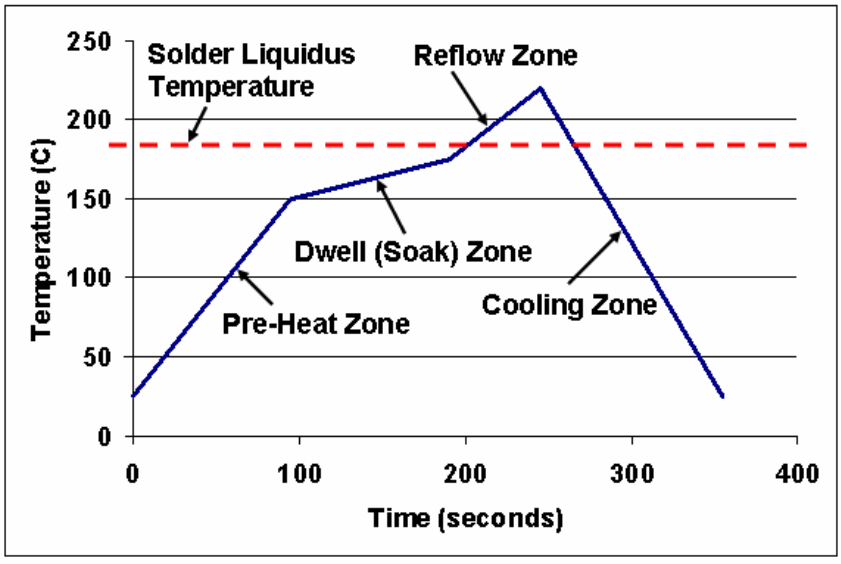


Figure 6.1. RDRP Temperature Reflow Profile for Analytical Warpage Study

Based on the temperature measurements during the experiment, the temperature gradient across the board surface was negligible, and the temperature gradient through the thickness was assumed to be uniform relative to the sample surface. The temperature change in the reflow profile was used as thermal loads in the warpage analytical models. PWB and PWBA warpage was calculated during the reflow process, and the results were superposed to evaluate cumulative warpage of the board and assembly, respectively.

In order to evaluate the PWB warpage during the thermal reflow, Equation (6.3) and Equation (6.4) were used to calculate the warpage caused by thermal loads, and Equation (6.14) was used to calculate the warpage caused by the weight of the board. According to the actual support conditions of the test sample, simple support along the short edges and free conditions along the long edges were used as the boundary conditions. The weight of the board was assumed as a constant distributed transverse load over the surface with a magnitude of 24 N/m^2.

In order to evaluate the PWBA warpage during the thermal reflow based on the classical laminated plate theory, it is assumed that a large enough number of PBGA packages were assembled on the surface of the PWB sample. These packages composed a new layer on the board surface. The effective material properties of the package layer were obtained using the rule of mixtures, and are shown in Table 6.1. The structure was assumed to be stress free at the temperature of 183 °C for 63Sn-37Pb solder bumps. Equation (6.3) and Equation (6.4) were used to calculate the warpage caused by thermal loads, and Equation (6.14) was used to calculate the warpage caused by the weight of the assembly. According to the actual support conditions of the test sample, simple support along the short board edges and free conditions along the long board edges were used as

the boundary conditions. The weight of the assembly was assumed as a constant distributed transverse load over the surface with a magnitude of 42 N/m^2.

6.3.2. Warpage Assessment and Comparison Based on Analytical Modeling

For the analytical PWB model, the initial warpage at room temperature is assumed to be zero. For the analytical PWBA model, the initial warpage at 183 °C is assumed to be zero. Figure 6.2 illustrates the three points selected for warpage assessment on the specimen. The calculated relative warpage values at the selected points during the thermal reflow process are shown in Figures 6.3 – 6.8.

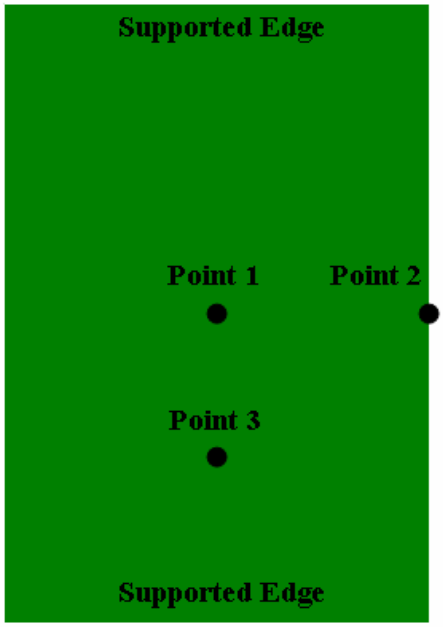


Figure 6.2. Selected Points for Warpage Correlation

The warpage results obtained from the analytical model were validated and compared with the experimental and numerical results. The developed convective reflow-projection moiré warpage measurement system as shown in Figure 3.1 was used to

measure the real-time warpage of the PWB and PWBA samples during the simulated reflow process. The applied PWB test vehicle, which is shown in Figure 5.1, has the same dimension and structure as the analytical model. The PWBA sample includes 6 electronic packages assembled on the board. The relative warpage results at the three selected locations on the PWB/PWBA were obtained by subtracting the initial warpage from subsequent measurements during the reflow process. The initial warpage of the PWB sample was obtained at room temperature. The initial warpage of the PWBA sample was obtained at 183 °C. The experimental relative warpage values of the PWB/PWBA samples are shown in Figures 6.3 – 6.8.

Three-dimensional finite element models of the PWB and PWBA samples were generated in ANSYS7.1 for numerical study. SHELL91 elements were used to mesh the PWB surface for their advantages in modeling layered shell or thick sandwich structures. For the PWBA model, the 27 × 27 mm PBGA packages, including package molding, BT substrate, and 63Sn-37Pb solder bumps, were modeled and meshed using SOLID95 elements, which are 3-D 20-node solid elements. Total 6 PBGA packages were modeled, and they are distributed over the PWB uniformly. The boundary conditions of the numerical PWB/PWBA models are the same as the above simple support conditions. The PWB model was subjected to a typical manufacturing thermal reflow profile as shown in Figure 6.1. The starting temperature of the PWBA model is 183 °C, at which the model was assumed to be a stress free structure. The PWB/PWBA material properties and detailed finite element modeling analysis are discussed in Chapter 7. The relative warpage values obtained from the finite element models for the three selected points are shown in Figures 6.3 – 6.8.

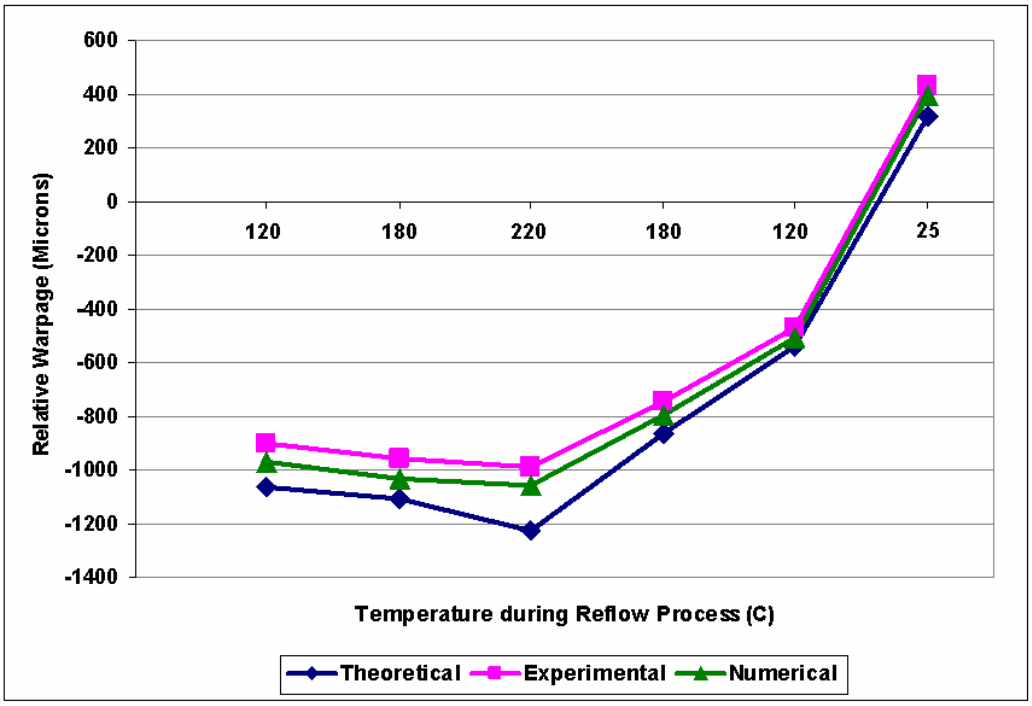


Figure 6.3. Relative Warpage of Point 1 on PWB Sample

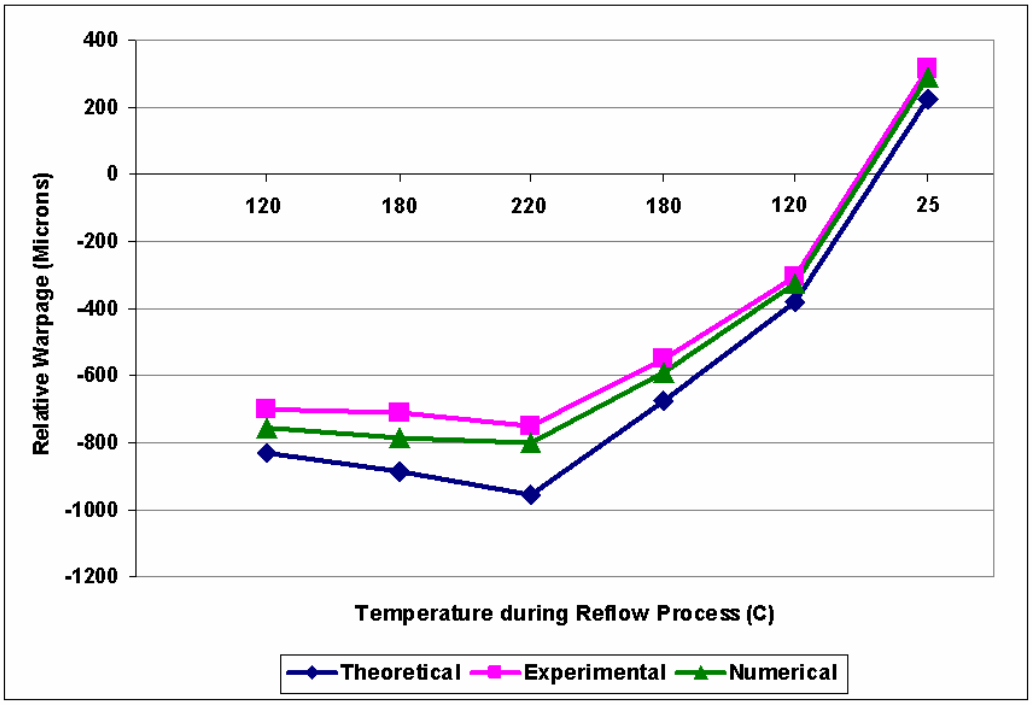


Figure 6.4. Relative Warpage of Point 2 on PWB Sample

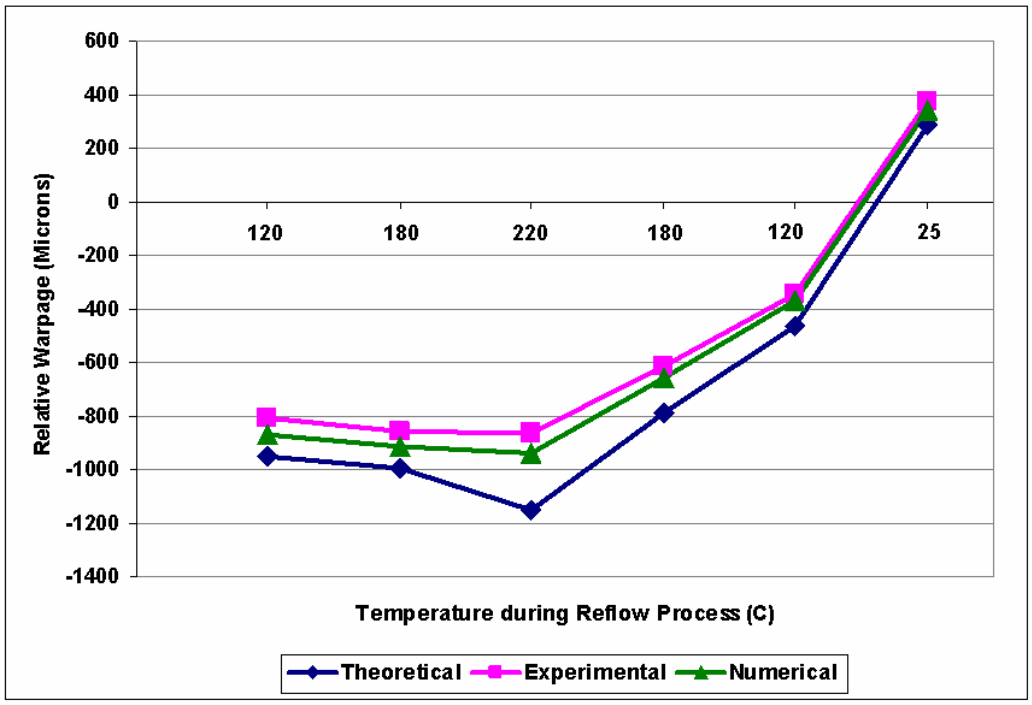


Figure 6.5. Relative Warpage of Point 3 on PWB Sample

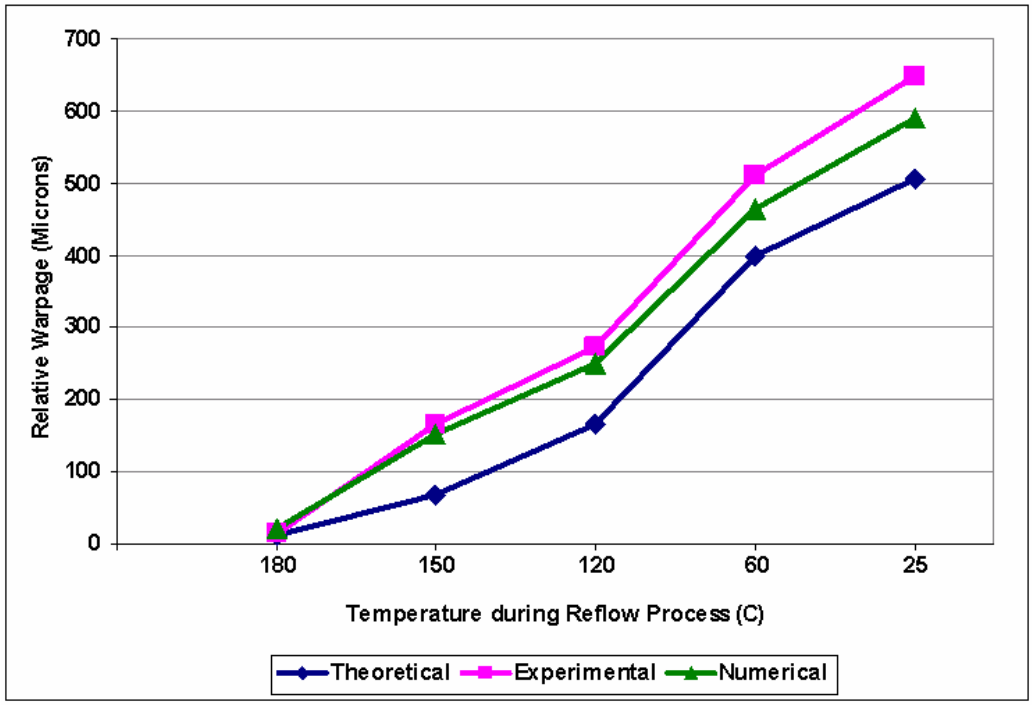


Figure 6.6. Relative Warpage of Point 1 on PWBA Sample

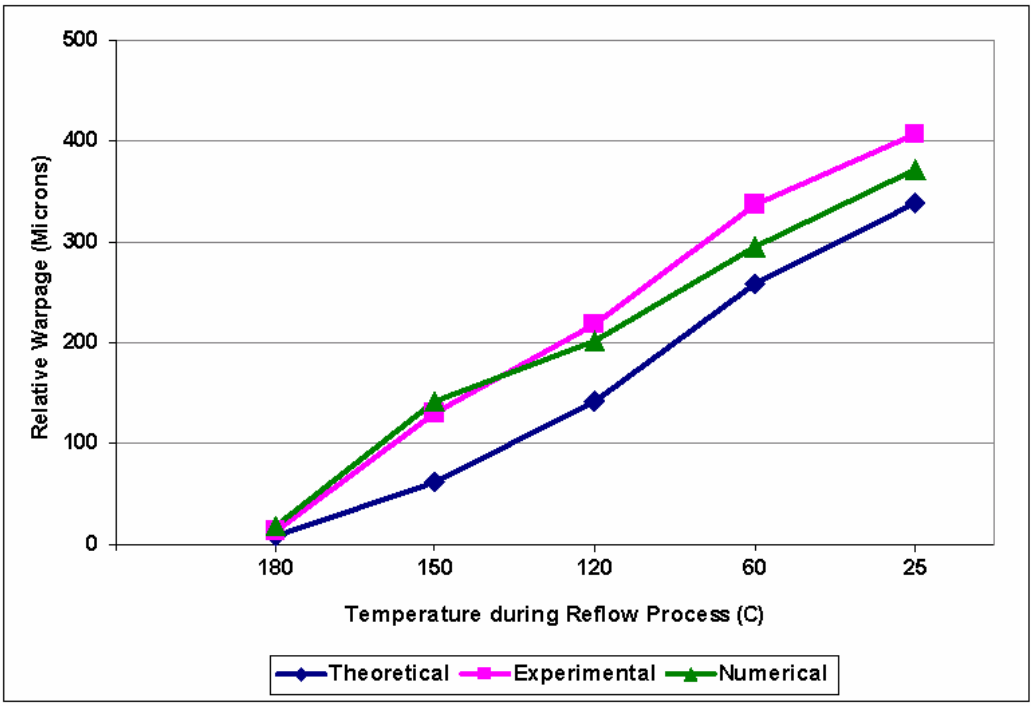


Figure 6.7. Relative Warpage of Point 2 on PWBA Sample

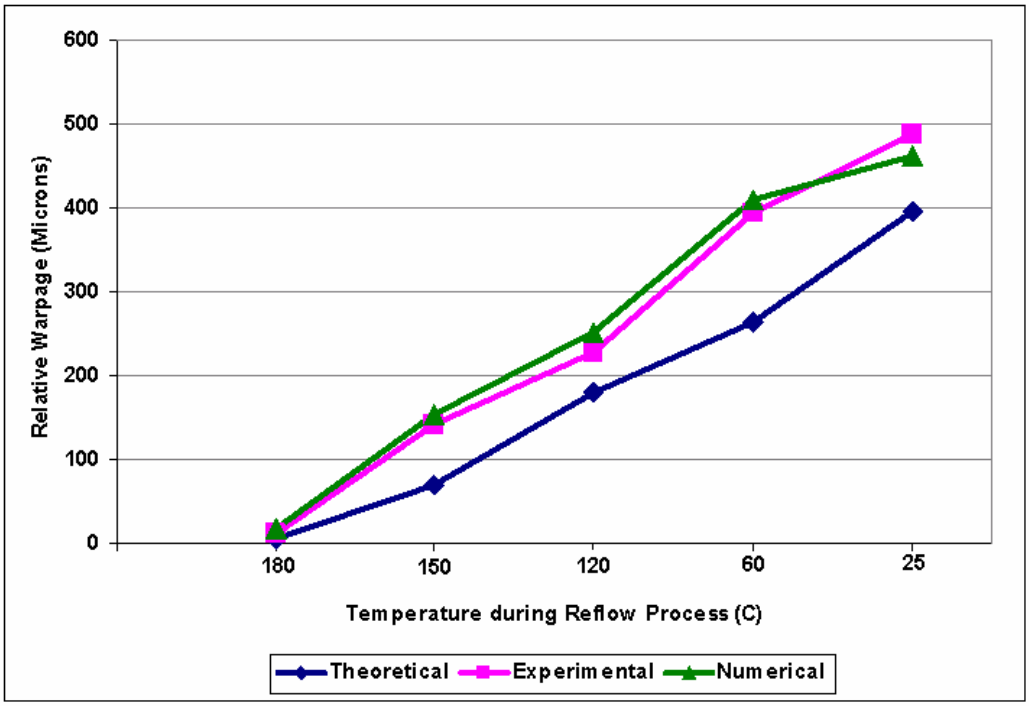


Figure 6.8. Relative Warpage of Point 3 on PWBA Sample

Figures 6.3 – 6.5 show that in the pre-heat zone of the thermal reflow process, the PWB warpage decreases quickly; in the dwell zone and reflow zone, the warpage change becomes slower; at the peak temperature, the PWB samples have the smallest absolute warpage values. Figures 6.3 – 6.8 show that in the cooling zone the warpage of the PWB/PWBA samples becomes larger; and after the reflow process, some residual warpage is generated on the samples.

The relative warpage results obtained from the analytical models and numerical models agreed well with the experimental results during the thermal reflow process. The simulation results of relative warpage values are slightly lower than the experimental results. The analytical models have the largest error (200 μm) relative to the experimental results at the peak temperature. These errors between the experimental and analytical results are due to the fact that in the analytical calculations, (1) through-the-thickness temperature gradient and CTE were assumed to be constant over different temperature ranges, while during the experimental measurements they varied through the whole temperature range, and (2) viscoelastic relaxation of the PWB/PWBA at the temperatures above its glass transition temperature, T_g = 125 °C, were not accounted for because the CLPT was developed for temperature-dependent elastic materials, and not viscoelastic materials. During the cooling zone of the reflow process, through-the-thickness temperature gradients decreased. Hence, the calculated results of the theoretical PWB/PWBA models have better agreement with the experimental results. Table 6.2 shows through-the-thickness temperature differences between the top and bottom surfaces of the PWB, and the top surface of the PBGA and bottom surface of the PWB during the reflow process.

Table 6.2. Through-the-Thickness Temperature Differences between PWB Surfaces, and PBGA and PWB Surfaces

Temperature (°C)	**25**	**120**	**180**	**200**	**220**	**180**	**120**	**25**
Temperature Difference through Thickness of PWB (°C)	0	2.4	2.8	3.1	3.3	2.7	2.3	0
Temperature Difference through Top of PBGA and Bottom of PWB (°C)	0	4.5	6.1	6.5	6.8	5.9	4.2	0

Comparing the results of Figures 6.3 to 6.5 and Figures 6.6 to 6.8 shows that the analytical results for the PWB compare more favorably with the experimental results than the PWBA results. The effective material properties used in the PWBA model may have contributed to the discrepancies between the analytical and experimental warpage results.

The warpage results generated from the FE models have higher accuracy than those from the theoretical calculation. This is because more precise PWB/PWBA models can be constructed in ANSYS, and accurate temperature-dependent material properties were included in the models. But the calculations for the FE models are much more complex and time consuming compared to the analytical models.

6.4. Chapter Summary

The classical laminated plate theory can be used to evaluate the warpage behavior of the PWB and PWBA samples during the thermal reflow process. Closed form solutions of the differential equations for the sample deformation from the classical lamination theory description were generated to assess warpage. The rule of mixtures was

used to estimate the effective material properties of the PWBA composites. The warpage values obtained from the theoretical models are highly sensitive to the thermal loads, the temperature gradients through the thickness of the samples, and the CTE values of the composite materials. The relative warpage results obtained from the analytical models and numerical models agreed well with the experimental results during the thermal reflow process. The simulation results of relative warpage values are slightly lower than the experimental ones. The analytical models have large discrepancy near the peak temperature due to viscoelastic relaxation and CTE change of the PWB/PWBA samples. The warpage results generated from the FE models have higher accuracy than those from the theoretical calculation. But the calculations for the FE models are much more complex and time consuming compared to the analytical models.

CHAPTER 7

FATIGUE ASSESSMENT OF SOLDER BUMPS ON BOARD ASSEMBLIES AFFECTED BY PWB WARPAGE

The objective of this research is to study the effect of printed wiring board (PWB) warpage on the low cycle fatigue of the solder bumps in plastic ball grid array (PBGA) packages. Finite element modeling (FEM) was used for the strain-based life prediction of solder bumps on board assemblies. In this study, three-dimensional (3-D) models of PWB assemblies (PWBAs) with varying board warpage were used to estimate the solder bump fatigue life for different types of PBGAs mounted on PWBs. In order to improve the accuracy of FE results, the projection moiré method was used to measure the initial warpage of PWBs, and this warpage was used as a geometric input to the FEM. The PWBAs with known PWB warpage were modeled to determine the influence of various levels of initial PWB warpage on the low cycle fatigue failure of solder bumps. The effect of different types of PBGAs with varying locations on solder bump fatigue was studied. Both Sn-Pb and lead-free solder materials were used in this study. The simulation results were validated and correlated with the experimental results obtained using the projection moiré technique and accelerated thermal cycling tests. An advanced prediction model was generated to predict board level solder bump fatigue life based on the initial PWB warpage, package dimensions and locations, and solder bump materials. This research shows that the initial PWB warpage has significant effects on fatigue reliability of solder bumps on board assemblies.

7.1. PWBA Test Vehicle

The applied PWBA structure is the same as the previous test vehicle as shown in Figure 5.1, which consists of a 203.2 mm by 139.7 mm by 0.631 mm PWB and 27 × 27 mm or 35 × 35 mm PBGA chip packages. The PWB is composed of four copper layers and three FR-4 layers. Figure 7.1 shows a cross-section schematic of the layered PWB along with its thickness dimensions. Specifically, the top copper layer of the PWB contains traces, which are 127 μm thick and have a pitch of 508 μm. The surface finish of the substrate bond pads is electroless nickel/immersion gold [Powell, 2006].

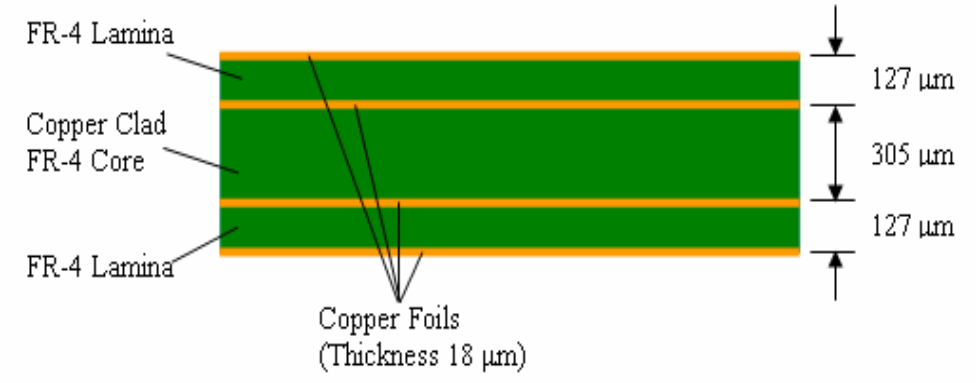


Figure 7.1. Cross-Section Structure of Layered PWB Test Vehicle

7.2. Finite Element Modeling to Estimate Fatigue Life of Solder Bumps Affected by PWB Warpage

7.2.1. Geometric Modeling and Meshing

In order to study the effect of PWB warpage on the low cycle fatigue of solder bumps in PBGA packages, 3-D finite element models of PWBAs with different degrees of board warpage were used to estimate the solder bump fatigue life for different types of

assembled PBGAs using ANSYS7.1 [Yao & Qu, 1999]. To improve the accuracy of FEA solutions, the PWB warpage was measured using the projection moiré method at the temperatures of 183 °C and 217 °C. These two temperatures are the solder stress free and starting temperatures for the PWBA models with 63Sn-37Pb solder bumps and 95.5Sn-3.8Ag-0.7Cu solder bumps, respectively. Three PWB samples with different initial warpage values were used in this study. Figure 7.2 shows one of the warpage measurement results of PWB sample 2 at the temperature of 183 °C using the projection moiré technique. Table 7.1 shows the maximum warpage measurement values for the three PWB samples at different temperatures.

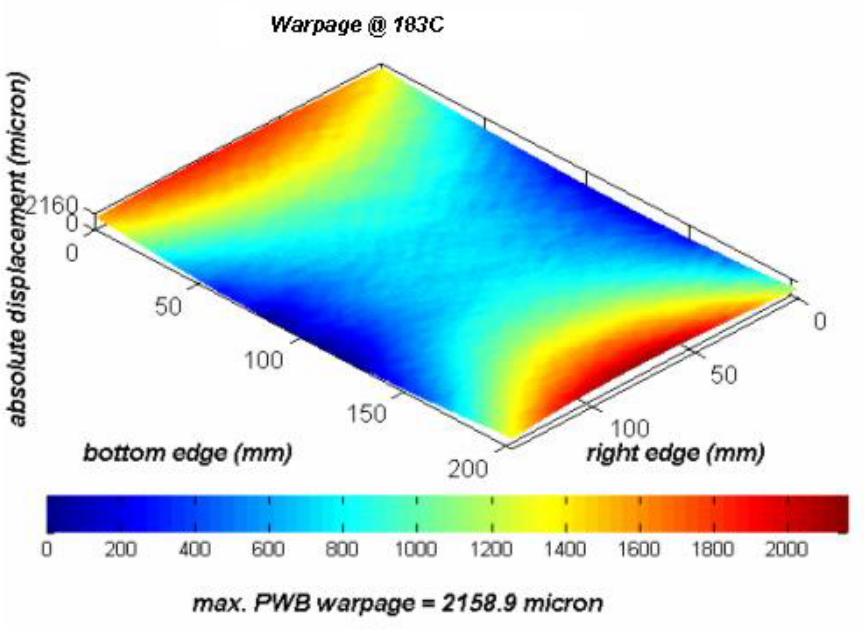


Figure 7.2. Warpage Measurement Result of PWB Sample 2 at 183 °C by Projection Moiré Method

Table 7.1. Maximum PWB Warpage Values at Different Temperatures

Temperature (°C)	Maximum Warpage of PWB Sample 1 (Microns)	Maximum Warpage of PWB Sample 2 (Microns)	Maximum Warpage of PWB Sample 3 (Microns)
25	2105.3	3076.6	3824.0
183	995.1	2158.9	3012.5
217	852.4	2008.2	2891.2

Based on the high resolution of the real-time projection moiré warpage measurement system, the warpage value at any location on the sample surface can be collected at each temperature level. In order to create a 3-D surface map of the PWB warpage, warpage was measured at 45 different locations on the PWB at the eutectic temperatures of 183 °C (Sn-Pb) and 217 °C (lead-free), respectively. Those measured points have equal intervals in horizontal and vertical directions on the sample surface, and are distributed over the PWB uniformly. The measured warpage values for the 45 specified points were inputted into FEM to generate the accurate geometry of the PWB surface with warpage for each sample at each temperature level. SHELL91 elements were used to mesh the PWB surface for their advantages in modeling layered shell or thick sandwich structures. Two types of PBGA packages, including package molding, BT substrate, and solder bumps, were modeled and meshed using SOLID95 elements, which are 3-D 20-node solid elements. Figure 7.3 shows the meshed PWB with a 35 × 35 mm PBGA package.

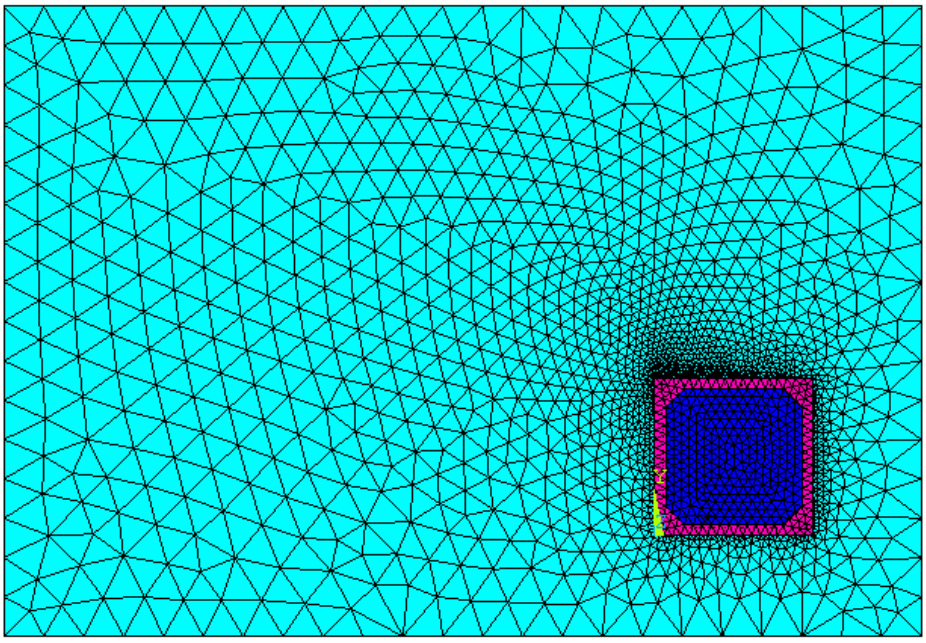


Figure 7.3. Meshed PWB with 35 × 35 mm PBGA Package

7.2.2. Material Properties for Modeling

The material properties used in the PWBA models are shown in Table 7.2 [Polsky & Ume, 1999; Muncy, 2004; Pang et al., 2004]. Table 7.2 shows the room temperature material properties, while Table 7.3 shows the temperature dependent material properties used in the FE modeling. Two types of solder bumps were simulated in the models: one is eutectic 63Sn-37Pb alloy, and the other is 95.5Sn-3.8Ag-0.7Cu alloy. They were both modeled as nonlinear, elastic-plastic-creep, isotropic, and temperature dependent [Pang & Chong, 2003; Che & Pang, 2004]. In order to obtain accurate simulation, temperature dependent material properties for Sn-Pb and lead-free solder obtained from the stress-strain curves in [Muncy, 2004; Pang et al., 2004] were used in the FE models.

Table 7.2. Room Temperature Material Properties Used for FE Simulation

Material		CTE (ppm/°C)	Elastic Modulus (GPa)	Property
PWB	**FR-4**	20.0	22.4	Linear Elastic, Orthotropic
	Copper Foil	18.9	79.5	Linear Elastic, Isotropic
Solder Bump	**63Sn-37Pb**	21.0	19.7	Non-Linear, Elastic-Plastic-Creep, Isotropic
	95.5Sn-3.8Ag-0.7Cu	21.0	50.3	
BT Substrate		15.0	14.0	Linear Elastic, Isotropic
Package Molding		17.5	15.0	Linear Elastic, Isotropic

Table 7.3. Temperature Dependent Material Properties Used for FE Simulation

Material	Temperature (°C)	CTE (ppm/°C)	Elastic Modulus (GPa)
FR-4	25	20	22.4
	95	20	20.7
	150	20	17.9
63Sn-37Pb	25	21	19.7
	125	21	11.7
95.5Sn-3.8Ag-0.7Cu	25	21	50.3
	125	21	25.3

7.2.3. Boundary Constraints and Thermal Cycling Tests

In the FEA model, the PWB length is in the X-direction, the PWB width is in the Y-direction, and the PWB thickness is in the Z-direction. The edge nodes of the PWB are supported along the width direction which is similar to the support condition of the PWBA in the projection moiré warpage measurement system. Therefore, to prevent any motion of the PWBA, there is a constraint in the Z-direction along the width edges of the PWB.

The FE simulation was utilized to investigate the solder bump fatigue reliability under standard thermal cycle conditions [JESD22-A104-A], between -40 °C and 125 °C every twenty minutes, keeping the dwell time as ten minutes at the two temperature extremes. The structure was assumed to be stress free at the temperature of 183 °C for 63Sn-37Pb solder bumps, and at the temperature of 217 °C for 95.5Sn-3.8Ag-0.7Cu bumps. It was cooled down to room temperature of 25 °C in 150 seconds. The temperature load step profile for FE models with Sn-Pb solder is shown in Figure 7.4. Ten complete thermal cycles were simulated.

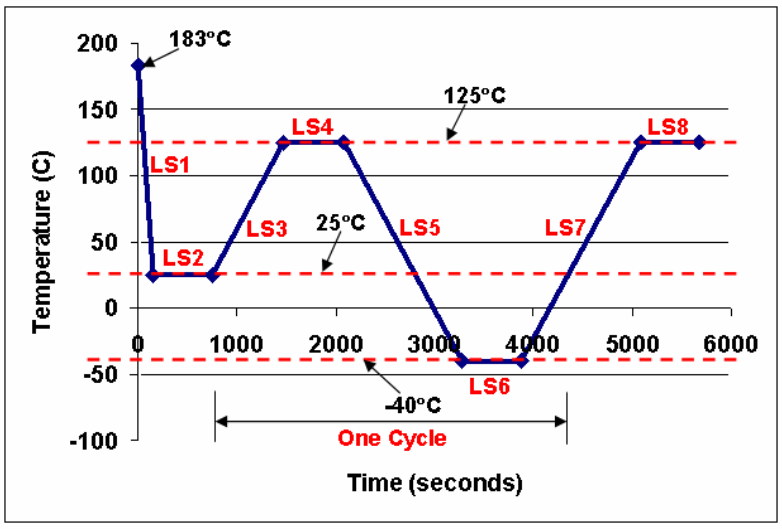


Figure 7.4. Temperature Load Step Profile for FE Models with Sn-Pb Solder

7.2.4. Fatigue Prediction and Analysis

Based on the finite element models developed in previous sections, the fatigue life of Sn-Pb and lead-free solder bumps were predicted using effective strain solutions of the models after ten thermal cycles. The effective plastic strain of the solder bumps can be calculated according to Equation (7.1) [Yao et al., 1999]

$$\varepsilon_{eff} = \frac{\sqrt{2}}{3}\sqrt{(\varepsilon_1-\varepsilon_2)^2+(\varepsilon_2-\varepsilon_3)^2+(\varepsilon_3-\varepsilon_1)^2} \tag{7.1}$$

where ε_i (i=1, 2, 3) are the principal strains.

The effective strain range is the strain difference between the two strains resulting from two extreme temperatures in each thermal cycle. The maximum effective strain value of the solder bumps was used for fatigue estimation. An empirical relationship between plastic strain and bump life, proposed by Coffin-Manson [Coffin & Schenectady, 1954; Gektin et al., 1997], has been widely used to predict solder bump fatigue life,

$$\Delta\varepsilon_p = \varepsilon_f (2N_f)^c \tag{7.2}$$

where $\Delta\varepsilon_p$ represents the plastic strain range, N_f is the total number of cycles to failure, ε_f (=0.325) is the fatigue ductility coefficient, and c (=-0.7~-0.5) is the fatigue ductility exponent.

7.2.5. FE Model Validation

To validate the FE model, the PWB test sample 1 with one 35 × 35 mm 63Sn-37Pb PBGA chip package as shown in Figure 7.5 was used. The FE model went through the first 4 temperature load steps in the thermal cycling simulation as shown in Figure 7.4: from 183 °C to room temperature in 150 seconds, then heated up to 125 °C, while keeping the dwell time as ten minutes at 25 °C and 125 °C. The PWB warpage entered into the FE model had a maximum value of 995.1 microns at 183 °C, which was the measurement result from the projection moiré experimental system using the corresponding PWB sample 1. At each end of the temperature load steps, the maximum PWB out-of-plane displacements from projection moiré experiments and FE model were compared and are shown in Table 7.4. Figure 7.5 and 7.6 also show the PWBA warpage plots from the experiment and FE model at the end of load step 1 (at room temperature). This data shows that the maximum difference between experimental and modeling results is 7.8 %. The FE model results agreed well with the corresponding experimental results, and can be used to study the correlation between PWB warpage and low cycle fatigue life of solder bumps on board assemblies.

Table 7.4. Maximum PWB Warpage Results of Experiments and FE Model at Different Temperatures

Temperature Load Steps	Max. PWB Warpage from Experiments (Microns)	Max. PWB Warpage from FE Models (Microns)	Differences
Initial 183 °C	995.1	980	1.5 %
Cooling to 25 °C	2055.2	2196	-6.4 %
Keeping 25 °C for 10 minutes	2041.6	2193	-6.9 %
Heating to 125 °C	1080.5	1172	-7.8 %
Keeping 125 °C for 10 minutes	1086.8	1171	-7.2 %

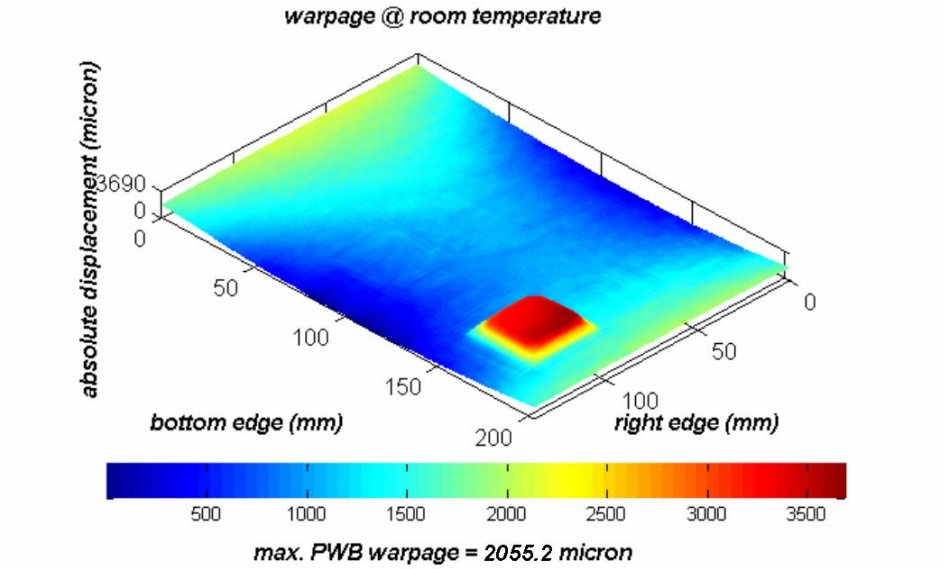


Figure 7.5. Out-of-Plane Displacement Measurement Result Using Projection Moiré System at Room Temperature

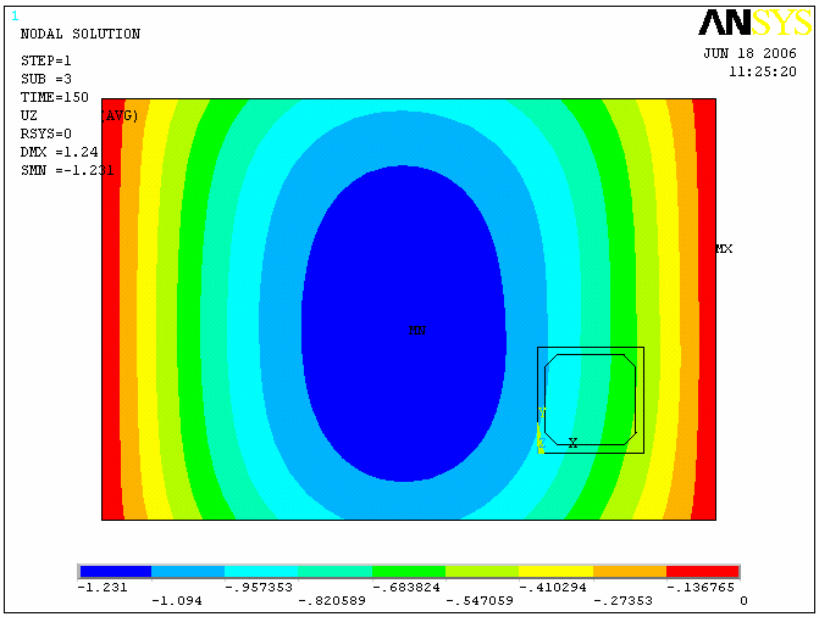


Figure 7.6. Out-of-Plane Displacement Plot of FE Model at Room Temperature

7.2.6. Effect of PWB Warpage on Solder Bump Fatigue

In this section, the FE models developed in previous sections were used to study the fatigue life of solder bumps on board assemblies affected by initial PWB warpage. Two types of PBGA packages, 27 × 27 mm and 35 × 35 mm packages, were used. Each PBGA package has Sn-Pb and Sn-Ag-Cu solder bumps, and can be placed at 3 different locations: location 1 is at the PWB center, location 2 is at a horizontal distance of 60 mm and a vertical distance of 30 mm from the PWB center, location 3 is at a horizontal distance of 78 mm and a vertical distance of 46 mm from the PWB center. The third location has the longest distance of 91 mm between the PWB center and package center. Based on the projection moiré measurement results, three different PWB samples as shown in Table 7.1 were modeled. The measured warpage values were entered into the FEM to improve the accuracy of the PWB surface geometry at the starting temperature.

The shape of the PWB warpage, convex up (+) or concave up (-), was also considered, i.e., the PBGA package can be assembled on both sides of each PWB.

The fatigue assessment of the solder bumps with maximum strain on board assemblies for 27 × 27 mm and 35 × 35 mm PBGA packages with Sn-Pb and Sn-Ag-Cu solder are shown in Figure 7.7 to Figure 7.10. The FE simulation results show that the initial PWB warpage has significant effects on the low cycle fatigue life of solder bumps in PBGA packages. For a PWB with higher initial warpage, the fatigue life of solder bumps on board assemblies is reduced. A PWB with concave shape will decrease the reliability of solder bumps more than a PWB with convex shape. If a PWB has a maximum initial warpage of -3.824 mm, the Sn-Pb solder bump fatigue life of a 27 × 27 mm PBGA located at the board center will be decreased by 31.5 %. In this case the lead-free solder bump fatigue life will be decreased by 26.2 %. The dimensions and locations of packages, and solder bump materials also affect the bump fatigue. Solder bumps will have longer fatigue life if the package is large in size and is located far from the PWB center. In addition, lead-free solder bumps are much more reliable than Sn-Pb solder bumps.

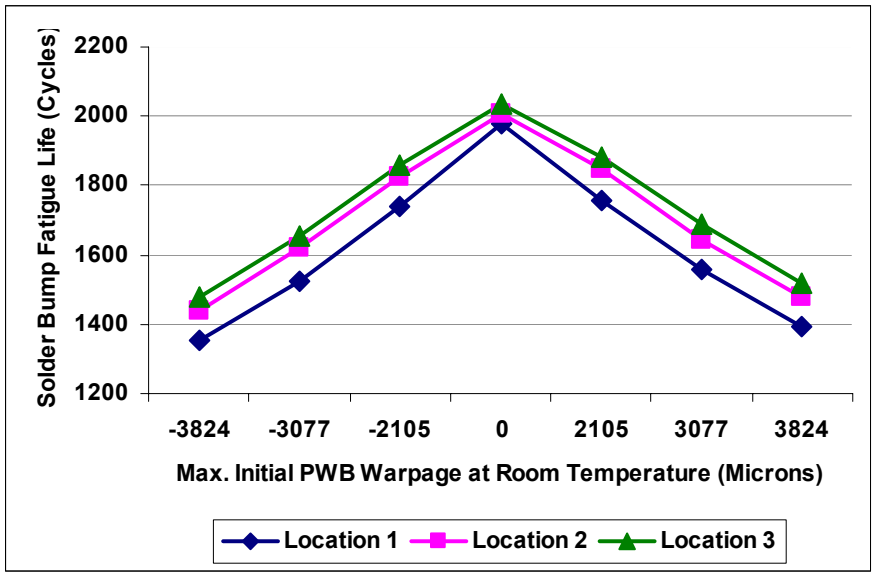


Figure 7.7. Sn-Pb Solder Bump Fatigue Assessment of 27 × 27 mm PBGA on Different PWB Locations

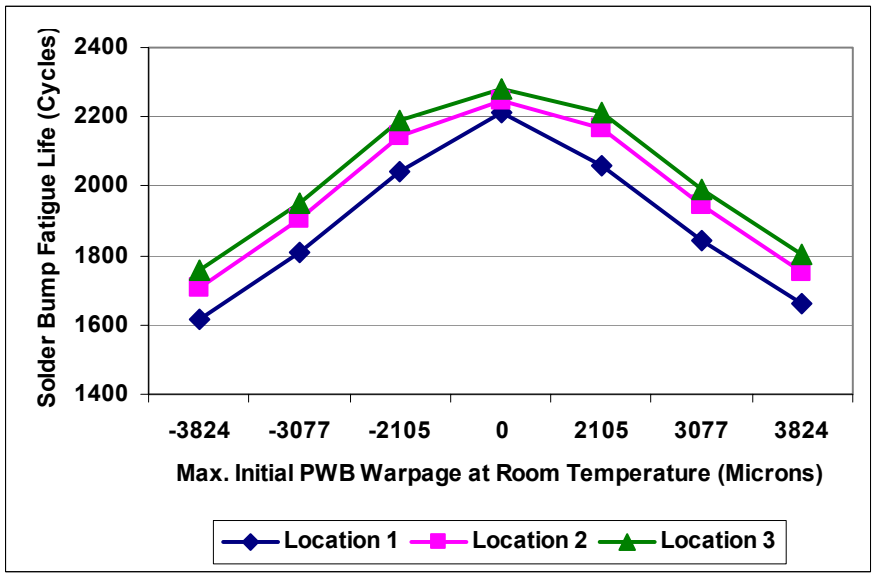


Figure 7.8. Lead-Free Solder Bump Fatigue Assessment of 27 × 27 mm PBGA on Different PWB Locations

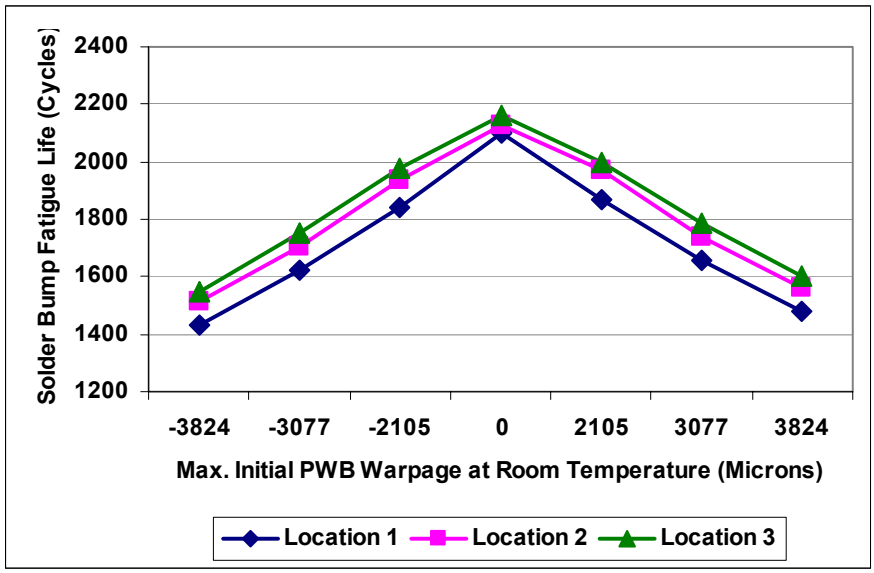


Figure 7.9. Sn-Pb Solder Bump Fatigue Assessment of 35 × 35 mm PBGA on Different PWB Locations

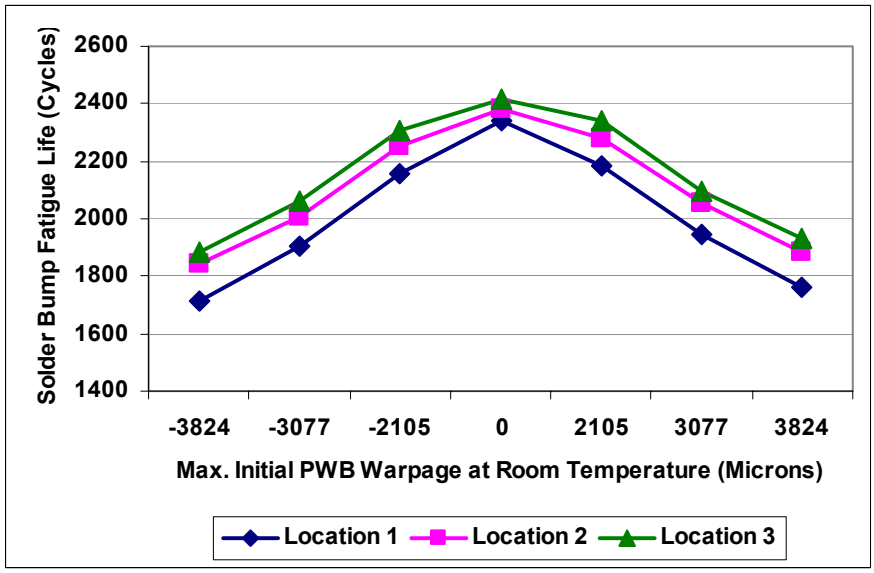


Figure 7.10. Lead-Free Solder Bump Fatigue Assessment of 35 × 35 mm PBGA on Different PWB Locations

7.3. Experimental Study on Solder Bump Fatigue Reliability Affected by PWB Warpage

In order to validate the above FEA simulation results, and accurately set up a correlation between PWB warpage and solder bump fatigue reliability on board assemblies, accelerated thermal cycling tests were performed using an ESPEC test chamber. The applied thermal cyclic conditions [JESD22-A104-A] have the temperature range between -40 °C and 125 °C as shown in Figure 7.4.

There are total 20 PWBs assembled with 27 × 27 mm or 35 × 35 mm PBGA packages used in this study. The projection moiré system was used to measure the warpage of the 20 PWBA samples at room temperature. Each PWB has different initial board warpage as shown in Table 7.5. Five boards among the test vehicles were assembled with 27 × 27 mm PBGA packages at location 2 respectively, which is at a horizontal distance of 60 mm and a vertical distance of 30 mm from the PWB center; five PWBs were assembled with 27 × 27 mm PBGA packages at location 4 respectively, which is at a horizontal distance of 0 mm and a vertical distance of 30 mm from the PWB center; five PWBs were assembled with 35 × 35 mm PBGA packages at location 2 respectively; five PWBs were assembled with 35 × 35 mm PBGA packages at location 4 respectively. The applied PBGA samples have daisy chain connections as show in Figure 7.11 [Amkor, 2007]. The initial resistance for each PBGA package is shown in Table 7.6.

Table 7.5. Initial PWB Sample Warpage at Room Temperature

Assembled Package Characteristics	**27 × 27 mm PBGA, 63Sn-37Pb, 256 solder bumps**		**35 × 35 mm PBGA, 63Sn-37Pb, 352 solder bumps**	
Package Location on PWB Sample	**Location 2**	**Location 4**	**Location 2**	**Location 4**
Max. Initial Warpage of PWB Sample 1 (Microns)	1706.4	1819.5	1754.2	1733.3
Max. Initial Warpage of PWB Sample 2 (Microns)	1997.0	2004.4	2022.7	2147.9
Max. Initial Warpage of PWB Sample 3 (Microns)	2109.8	2105.3	2098.1	2367.5
Max. Initial Warpage of PWB Sample 4 (Microns)	2433.3	3076.6	2536.6	2741.8
Max. Initial Warpage of PWB Sample 5 (Microns)	3176.1	3824.0	2878.3	3009.7

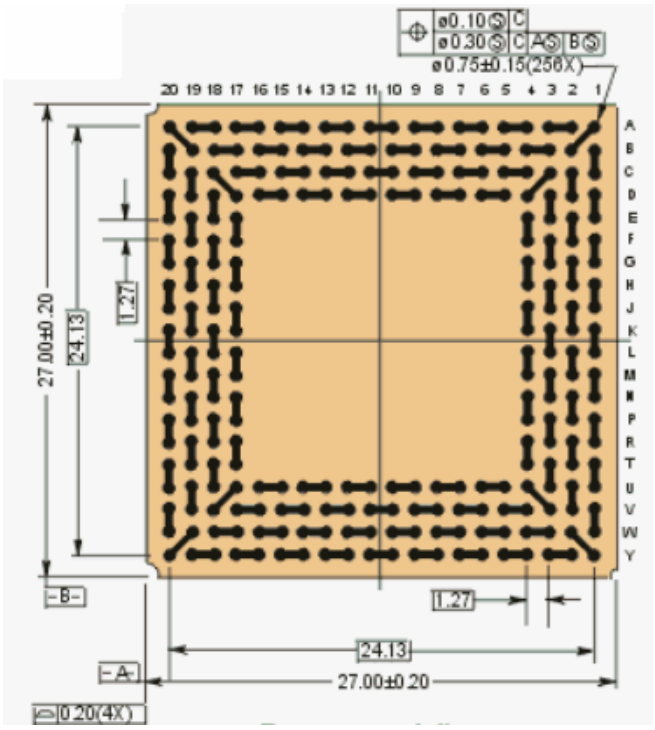


Figure 7.11. (a) 27 × 27 mm PBGA Daisy Chain Connections

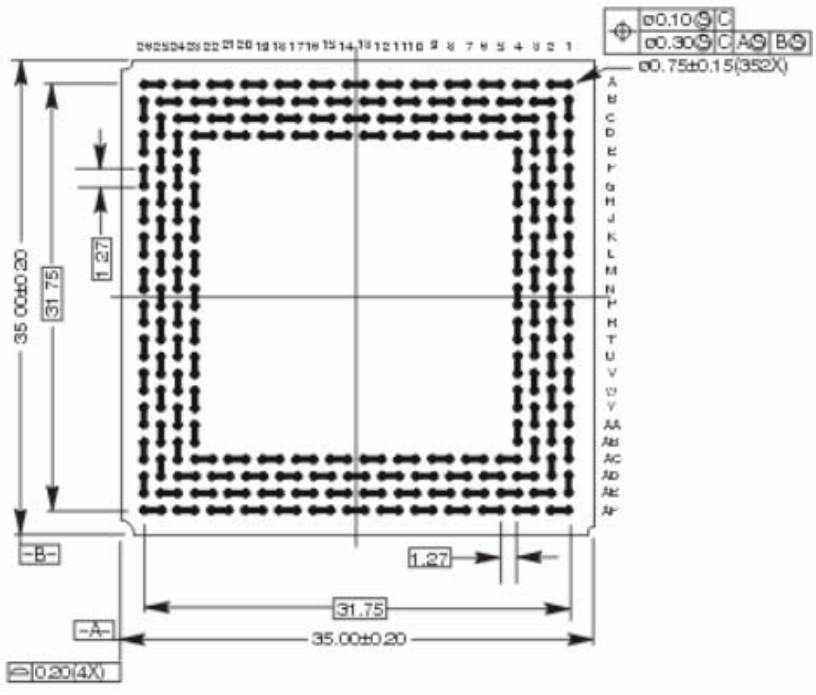


Figure 7.11. (b) 35 × 35 mm PBGA Daisy Chain Connections

Table 7.6. Initial Resistance of Daisy Chain PBGA Packages

Assembled Package Characteristics	**27 × 27 mm PBGA, 63Sn-37Pb, 256 solder bumps**		**35 × 35 mm PBGA, 63Sn-37Pb, 352 solder bumps**	
Package Location on PWB Sample	**Location 2**	**Location 4**	**Location 2**	**Location 4**
Package Resistance on PWB 1 (Ω)	0.3	0.3	0.2	0.2
Package Resistance on PWB 2 (Ω)	0.4	0.3	0.2	0.3
Package Resistance on PWB 3 (Ω)	0.3	0.2	0.2	0.2
Package Resistance on PWB 4 (Ω)	0.3	0.3	0.3	0.2
Package Resistance on PWB 5 (Ω)	0.2	0.3	0.2	0.2

The above PWBA samples were placed in the ESPEC test chamber to perform the standard thermal cycling test [JESD22-A104-A] with the temperature range from -40 °C to 125 °C. Failure of the solder bumps is defined when the resistance value is larger than 300 Ω in this study. The measured fatigue failure results are shown in Figure 7.12. The experimental test results show that the initial PWB warpage has significant effects on the low cycle fatigue life of solder bumps on PBGA packages. For a PWB with higher initial warpage, the fatigue life of solder bumps on board assemblies is reduced, which is consistent with the FEA simulation results. If the maximum initial warpage of the PWB samples changes from 1.706 mm to 3.176 mm, the Sn-Pb solder bump fatigue life of the 27 × 27 mm PBGA packages assembled at location 2 is decreased by 28.4 %, from 2900

cycles to 2075 cycles. The solder bumps have longer fatigue life if the package is small in size and is located far from the PWB center. The PWB samples have large deformations near the board center. Therefore, if the electronic package is assembled far from the PWB center, the initial board warpage has less effect on the fatigue reliability of solder bumps on board assemblies.

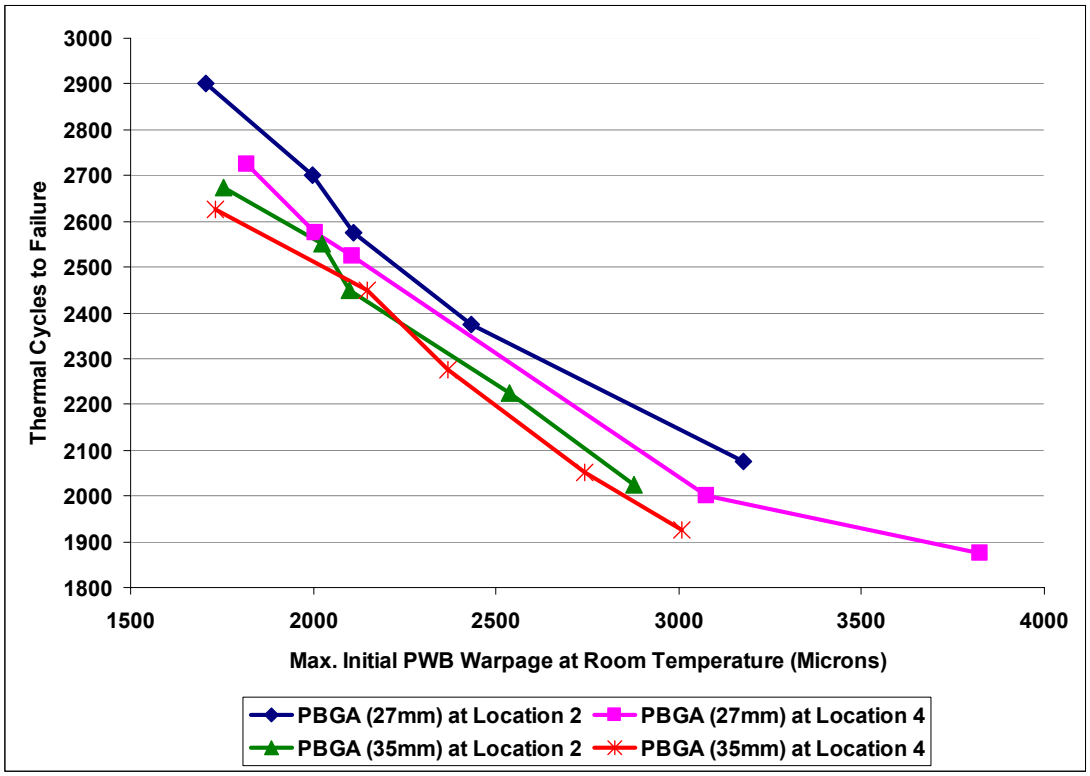


Figure 7.12. Solder Bump Fatigue Failure Affected by PWB Warpage

During the thermal cycling test, the warpage of the 20 PWB samples was measured using the projection moiré system after numbers of thermal cycles. Figure 7.13 shows the relative warpage change of the PWBs during the thermal cycling test. Each curve represents the average values of the maximum board warpage across five PWB

samples populated with 27 × 27 mm PBGA or 35 × 35 mm PBGA, at location 2 or location 4. A relative comparison for the warpage change is provided in the figure with respect to the maximum initial PWB warpage respectively. The experimental results show that with increasing the number of thermal cycles, the PWB warpage increases. The assembled PBGA packages constrain the deformation of the PWB samples during thermal cyclic conditions. For an electronic package in large size, and located near the board center, it will have more effect on the PWB warpage. For the 35 × 35 mm PBGA assembled at location 4, the maximum PWB warpage changed 25.7 % after 3000 thermal cycles; for the 27 × 27 mm PBGA assembled at location 2, the maximum PWB warpage changed 33.4 % after 3000 thermal cycles. The PWB warpage values after numbers of thermal cycles were measured using the projection moiré system, and the average values are shown in Table 7.7.

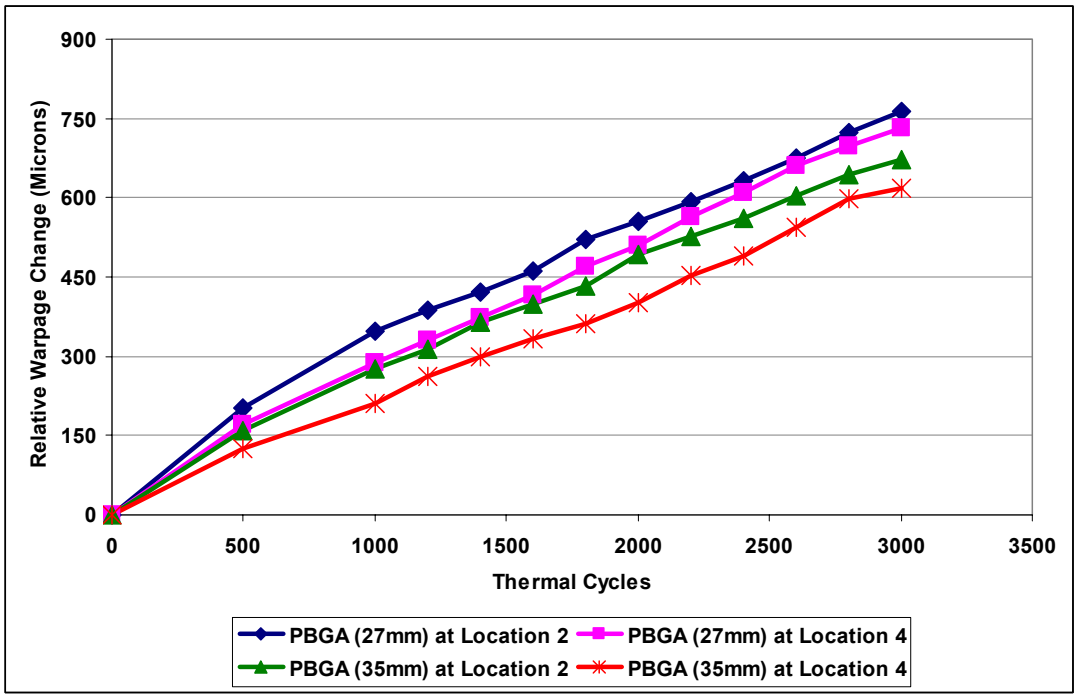


Figure 7.13. Relative Warpage Change of PWBs During Thermal Cycling Test

Table 7.7. Average PWB Warpage During Thermal Cycling Test

Assembled Package Characteristics	27 × 27 mm PBGA, 63Sn-37Pb, 256 solder bumps		35 × 35 mm PBGA, 63Sn-37Pb, 352 solder bumps	
Package Location on PWB Sample	**Location 2**	**Location 4**	**Location 2**	**Location 4**
Max. Initial PWB Warpage (Microns)	2284.5	2565.9	2257.9	2400.0
Max. PWB Warpage after 500 Cycles (Microns)	2485.9	2738.2	2418.7	2524.7
Max. PWB Warpage after 1000 Cycles (Microns)	2631.8	2852.7	2535.1	2611.2
Max. PWB Warpage after 1200 Cycles (Microns)	2672.9	2896.8	2572.4	2661.6
Max. PWB Warpage after 1400 Cycles (Microns)	2704.9	2939.5	2623.0	2700.0
Max. PWB Warpage after 1600 Cycles (Microns)	2745.9	2981.6	2657.6	2733.6
Max. PWB Warpage after 1800 Cycles (Microns)	2805.4	3035.5	2691.5	2762.4
Max. PWB Warpage after 2000 Cycles (Microns)	2839.7	3076.8	2750.2	2800.8
Max. PWB Warpage after 2200 Cycles (Microns)	2876.2	3130.5	2784.1	2853.6
Max. PWB Warpage after 2400 Cycles (Microns)	2917.3	3176.7	2820.2	2889.6
Max. PWB Warpage after 2600 Cycles (Microns)	2958.5	3225.4	2863.1	2944.8
Max. PWB Warpage after 2800 Cycles (Microns)	3008.7	3263.9	2901.5	2997.7
Max. PWB Warpage after 3000 Cycles (Microns)	3047.6	3297.3	2930.9	3016.9

7.4. Development of Statistical Analysis and Prediction Model

7.4.1. Design of Simulations and Regression Model

In order to study the correlation between PWB warpage and solder bump fatigue reliability, a five-factor design of simulations and a regression model were developed for Sn-Pb and lead-free solder bumps based on the FEA solutions. In the regression model, the response is the fatigue life time of solder bumps; the factors of interest are the maximum initial PWB warpage at room temperature, warpage shape, PBGA package dimension, location of package, and solder bump material. The PWB warpage shape can be convex up (+1) or concave up (-1). The length of the package is always referred to as the dimension of the package. The location of the package is determined from the PWB center to the package center. In Equation (7.3), whenever the solder bump material is Sn-Pb, "-1" is substituted for m_s, and the bump material is Sn-Ag-Cu, "+1" is substituted for m_s. Equation (7.3) shows a bilinear model expressing the response as a function of the five predictor variables and their two-factorial interactions.

$$N_r = \beta_0 + \beta_1 w_{\max} + \beta_2 w_{shape} + \beta_3 d_p + \beta_4 l_p + \beta_5 m_s + \beta_6 w_{\max} w_{shape} + \beta_7 w_{\max} d_p + \beta_8 w_{\max} l_p$$
$$+ \beta_9 w_{\max} m_s + \beta_{10} w_{shape} d_p + \beta_{11} w_{shape} l_p + \beta_{12} w_{shape} m_s + \beta_{13} d_p l_p + \beta_{14} d_p m_s + \beta_{15} l_p m_s \quad (7.3)$$

where, N_r = fatigue life estimation of solder bumps (cycles)

$w_{\max}$ = maximum initial PWB warpage at 25 °C (mm)

w_{shape} = warpage shape

d_p = package dimension (mm)

l_p = location of package (mm)

m_s = solder bump material

β_{0-15} = regression coefficients

Note that the three-factorial interactions are omitted from Equation (7.3). Those interaction effects are not included due to the hierarchical ordering principle, which states that lower order effects are more likely to be important than higher order effects [Wu & Hamada, 2000].

In regression analysis, those predictor factors whose regression coefficients are not significant may be removed from the full model. A more parsimonious model (i.e., one with fewer covariates) is preferred as long as it can explain the data well. Based on the best subset regression and stepwise regression methods performed for the model [Wu & Hamada, 2000], the reduced model used to predict the fatigue life for Sn-Pb and Sn-Ag-Cu solder bumps on board-level assemblies is shown in Equation (7.4).

$$N_r = 1855 - 165w_{\max} + 12d_p + 148m_s + 5.94w_{\max}w_{shape} + 0.219w_{\max}l_p + 0.0263d_p l_p \quad (7.4)$$

To verify Equation (7.4), a residual plot and a normal probability plot as shown in Figure 7.14 and 7.15 were used for the reduced model. The plots show that the distribution of residuals appeared to be random, and the normal probabilities followed a linear trend [Wu & Hamada, 2000]. Therefore, the regression model assumptions are correct and Equation (7.4) can be used to estimate the fatigue life of solder bumps affected by PWB warpage on board assemblies.

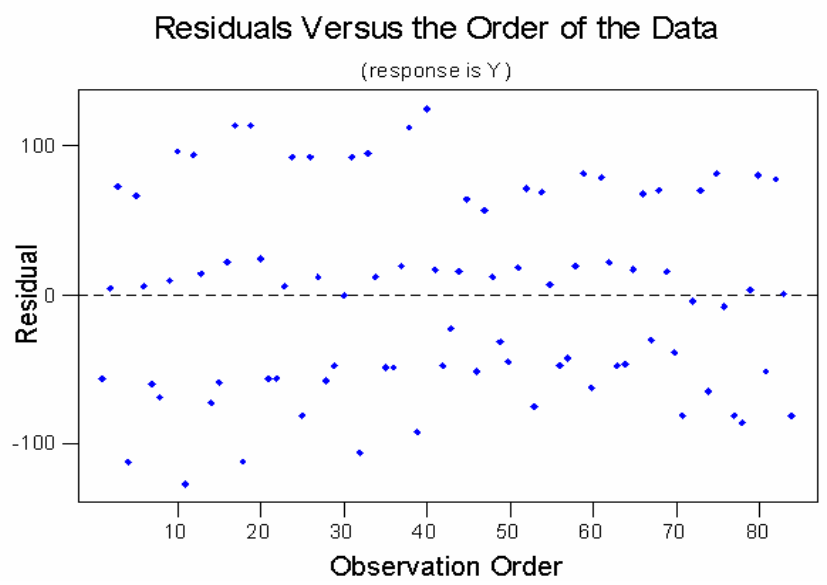


Figure 7.14. Residual Plot for Reduced Regression Model

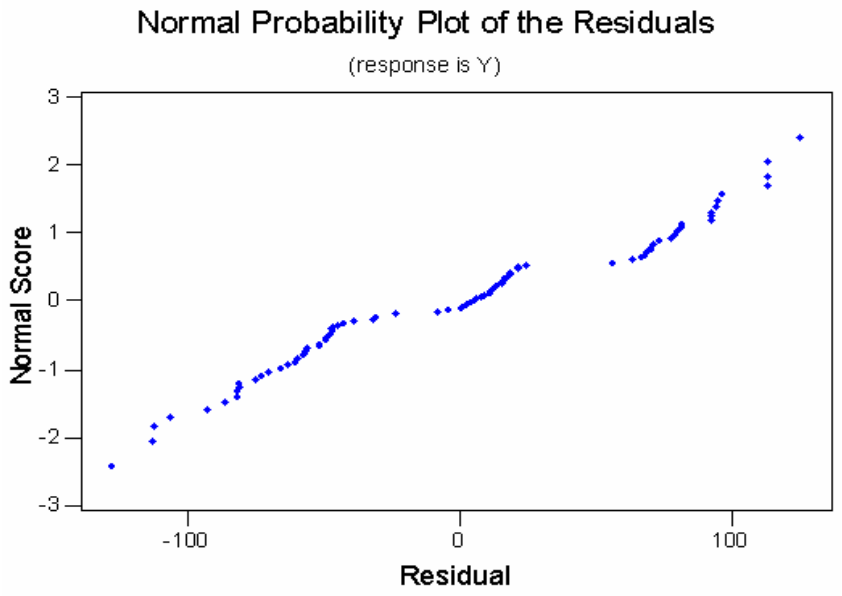


Figure 7.15. Normal Probability Plot for Reduced Regression Model

7.4.2. Advanced Model Fitting Based on FE Simulation Results

Regression analysis in Section 7.4.1 is intuitive and simple. However, there are some drawbacks. First, linear regression models usually assume random errors in the output. This is not true for most of the FE simulations because they usually yield a deterministic answer for a given set of inputs. That is, the same input produces identical output. Thus, a model which can interpolate outputs will be desirable. Secondly, the underlying system may be very complicated which can not be well approximated by the simple linear model. Therefore, more flexible nonlinear metamodels are called for.

The kriging model is the most popular method used for obtaining metamodels based on computer simulations [Sacks et al., 1989; Cappelleri et al., 2002; Pacheco et al., 2003; Santner et al., 2003; Sasena et al., 2005]. It is popular because it obtains interpolating metamodels which are suitable to conduct deterministic simulations. Assume the true function $N_k(\vec{x})$ ($\vec{x} \in R^p$), is a realization from a stochastic process. A commonly used kriging model, known as ordinary kriging, can be stated as follows:

$$N_k(\vec{x}) = \mu_0 + Z(\vec{x}) \tag{7.5}$$

where μ_0 is an unknown parameter, and $Z(\vec{x})$ is a weak stationary stochastic process with a mean of 0 and a covariance function of $\sigma^2\psi$. The covariance function is defined as in Equation (7.6).

$$\sigma^2\psi(\vec{h}) = \mathrm{cov}[N_k(\vec{x}+\vec{h}), N_k(\vec{x})] \tag{7.6}$$

where the correlation function $\psi(\vec{h})$ is a positive semidefinite function with $\psi(0) = 1$ and $\psi(-\vec{h}) = \psi(\vec{h})$.

In order to calculate the metamodel (or the predictor), assume that the true function is evaluated at m inputs $\{\vec{x}_1, \cdots, \vec{x}_m\}$, and $N_{out} = (N_1, \cdots, N_m)^T$ is the corresponding outputs. For an unobserved input *x*, the ordinary kriging predictor is shown in Equation (7.7).

$$\hat{N}_k(\vec{x}) = \hat{\mu}_0 + \varphi(\vec{x})^T \Psi^{-1}(N_{out} - \hat{\mu}_0 I) \tag{7.7}$$

where *I* is a column of 1's with a length of *m*, $\varphi(\vec{x}) = (\psi(\vec{x} - \vec{x}_1), \cdots, \psi(\vec{x} - \vec{x}_m))^T$, Ψ is an $m \times m$ matrix with the *ij*th element of $\psi(\vec{x}_i - \vec{x}_j)$, and $\hat{\mu}_0 = I^T \Psi^{-1} N_{out} / I^T \Psi^{-1} I$.

The kriging predictor as shown in Equation (7.7) is the best linear unbiased predictor, which minimizes the mean squared prediction error $E[\hat{N}_k(\vec{x}) - N_k(\vec{x})]^2$ under the model in Equation (7.3).

The most popular correlation function, Gaussian product correlation function is used in this research and shown in Equation (7.8). Other correlation functions such as cubic correlation function and Matérn correlation function can also be used [Santner, William, and Notz, 2003].

$$\psi(\vec{h}) = \exp\left(-\sum_{j=1}^{p} \theta_j h_j^2 \right) \tag{7.8}$$

$$\Theta = \left(\theta_1, \cdots, \theta_p\right)^T$$

The parameters σ_0^2 and Θ can be estimated by maximizing the likelihood [Santer, William, and Notz, 2003]. Thus, Equation (7.9) and Equation (7.10) can be obtained.

$$\hat{\Theta} = \arg\min_{\Theta}(m \log \hat{\sigma}_0^{\,2} + \log|\Psi|) \tag{7.9}$$

$$\hat{\sigma}_0^{\,2} = \frac{1}{m}(N_{out} - \hat{\mu}_0 I)^T \Psi^{-1}(N_{out} - \hat{\mu}_0 I) \tag{7.10}$$

In order to better understand the effect of the package assembly location in this research, three different locations were investigated with their exact coordinates in horizontal direction Hl_p and vertical direction Vl_p. In addition, one more factor was added into the prediction model to denote the PWB warpage existence. Therefore, total seven factors ($p = 7$) were considered in the kriging model. These factors are denoted by the vector $\vec{x}$. The correlation parameters Θ corresponding to the vector $\vec{x}$ were estimated by Equation (7.11). The ordinary kriging predictor is shown in Equation (7.12).

$$\hat{\Theta} = (0.01,\ 0.01,\ 0.01,\ 0.17,\ 4.28,\ 0.01,\ 0.04)^T \tag{7.11}$$

$$\hat{N}_k(\vec{x}) = 1101.6 + \varphi(\vec{x})^T \Psi^{-1}(N_{out} - 1101.6I) \tag{7.12}$$

In order to study the effects of different factors on the thermal fatigue reliability of solder bumps, the sensitivity analysis technique was applied on the ordinary kriging predictor as shown in Equation (7.12) [Welch et al., 1992]. Figure 7.16 shows the main effect plot of the different 7 factors. From Figure 7.16, the initial PWB warpage has significant effects on the solder bump fatigue reliability. The value of -1 for the warpage existence means there is no warpage on the PWB; the value of 1 means the warpage exists on the PWB. With the occurrence of board warpage, the solder bump fatigue reliability is significantly decreased. With the increasing of the maximum PWB warpage, from the value of -1 to 1, the solder fatigue life is constantly decreased. For the solder materials, the value of -1 means the Sn-Pb solder; the value of 1 means the Sn-Ag-Cu solder. Figure 7.16 shows that the lead-free solder is more reliable than the Sn-Pb solder. Also, the package dimension has some effects on the solder bump fatigue life. The package location and PWB warpage shape have small effects on the solder bump reliability.

Moreover, there are two significant interactions between the PWB warpage and solder materials as shown in Figure 7.17. Figure 7.17 (a) shows an interaction between the PWB warpage existence and the solder bump materials. The effect of PWB warpage on the fatigue life is higher with Sn-Pb solder than with lead-free material. The other interesting interaction is between the PWB warpage shape and the solder bump materials. Compared with the lead-free solder, Sn-Pb solder can produce more effects on the fatigue life when the warpage shape is changed.

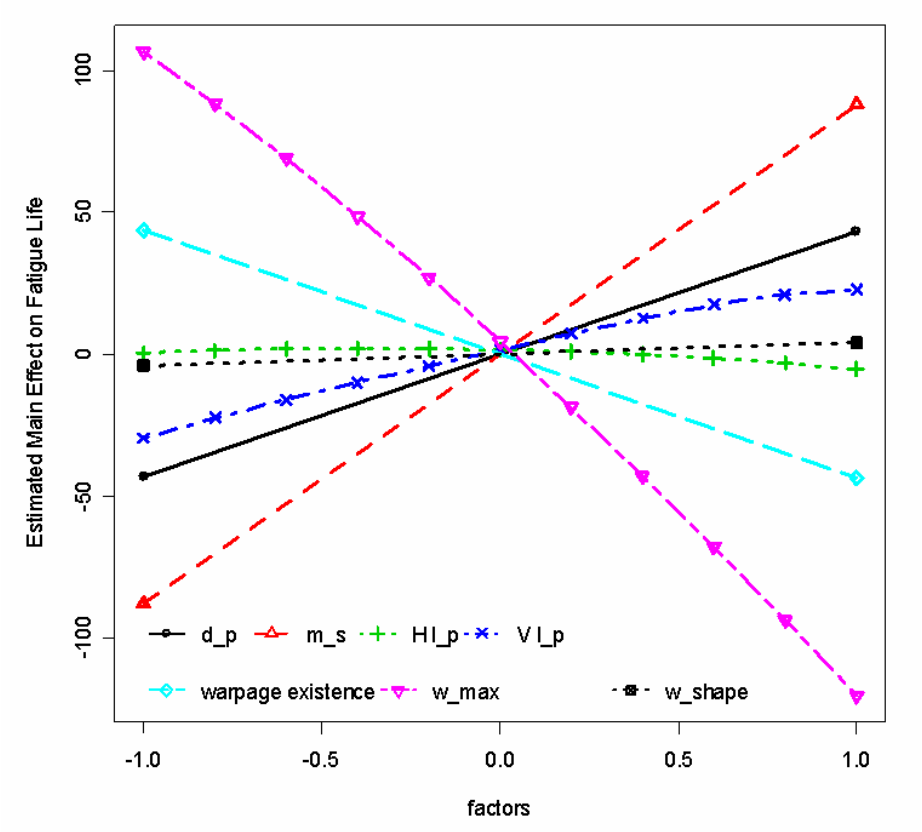
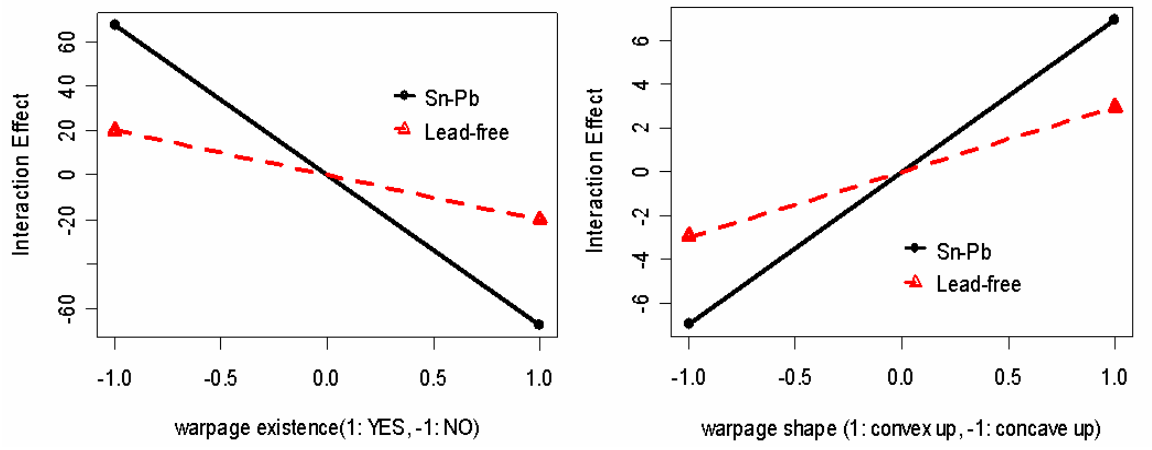


Figure 7.16. Main Effect Plot of 7 Factors on Solder Bump Fatigue Reliability



(a) (b)

Figure 7.17. Two Significant Interactions between PWB Warpage and Solder Materials

7.4.3. Analysis of Advanced Integrating Model

In the previous sections, the effect of PWB warpage on solder bump fatigue reliability was studied based on FE simulation results. However, the simulation results are not as accurate as the experimental results. On the other hand, although the physical experimental results are accurate, conducting such experiments is very expensive and time consuming. In order to effectively integrate the simulation and experimental data, a location adjustment model was developed as shown in Equation (7.13) [Qian et al., 2006]. The idea is to first fit a Gaussian process model using only the simulation results, and then adjust this model by limited physical experimental results.

$$N_f(\vec{x}) = N_k(\vec{x}) + \delta(\vec{x}) + err \tag{7.13}$$

where $N_f(\vec{x})$ represents the experimental results, $N_k(\vec{x})$ represents the FE simulation results, err is an additive error which follows a normal distribution with a mean of 0 and a variance of σ^2, and $\delta(\vec{x})$ is the location adjustment term.

Note that the experimental results $N_f(\vec{x})$ and the FE simulation results $N_k(\vec{x})$ may not always share the same parameter inputs as shown in Figure 7.18. This problem can be easily overcome by replacing $N_k(\vec{x})$ with $\hat{N}_k(\vec{x})$ estimated by Equation (7.12). Therefore, an integrated solder bump fatigue prediction model was generated as shown in Equation (7.14).

$$\hat{N}_f(\vec{x}) = \hat{N}_k(\vec{x}) + 1830.3 - 540 w_{\max} \tag{7.14}$$

where the location adjustment term is estimated by $\delta(x) = 1830.3 - 540 w_{\max}$ using the forward selection technique with R^2 at 0.7. That is, the difference between the FE simulation results and the experimental results can be explained by the maximum initial PWB warpage at 25 °C. Therefore, combining Equation (7.12), the final integrated model to predict solder bump fatigue life was obtained as shown in Equation (7.15).

$$\hat{N}_f(\vec{x}) = 2931.9 - 540 w_{\max} + \varphi(\vec{x})^T \Psi^{-1}(N_{out} - 1101.6I) \tag{7.15}$$

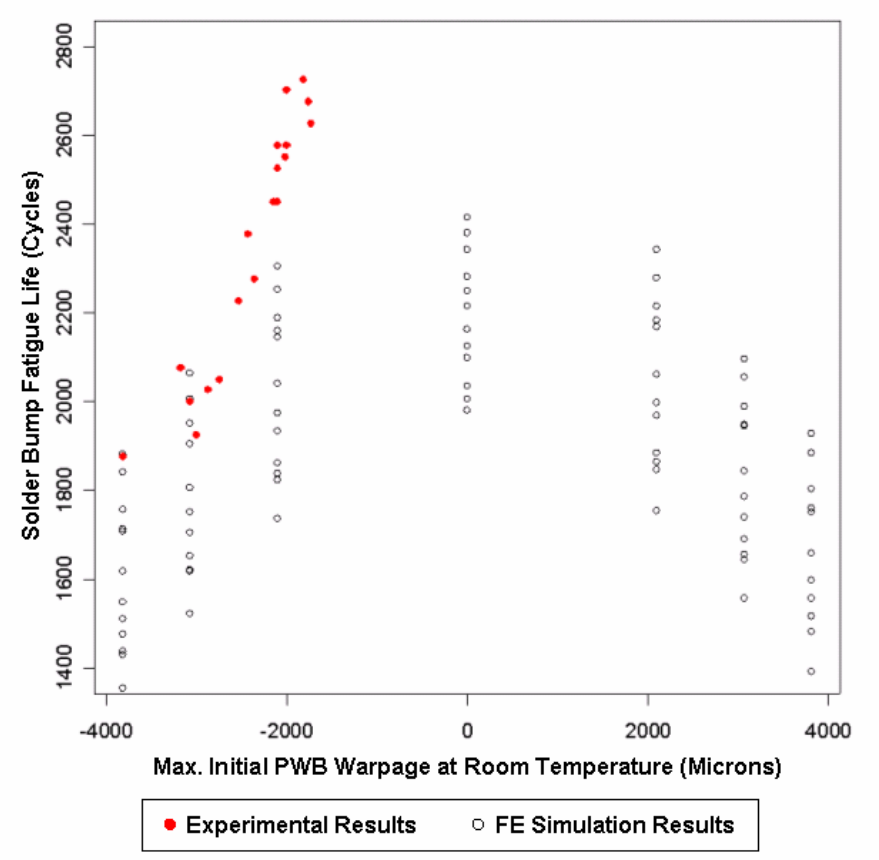


Figure 7.18. Combined Experimental and FE Simulation Results of Solder Bump Fatigue Reliability Affected by PWB Warpage

Based on the previous kriging model as shown in Equation (7.15), solder bump fatigue reliability was predicted and compared with the experimental results from the accelerated thermal cycling tests. Table 7.8 shows four different comparisons. The maximum difference of solder bump fatigue life between the kriging prediction model and the experimental results is 6.1 %. Therefore, the kriging prediction model as shown in Equation (7.15) is able to successfully estimate the solder bump fatigue reliability affected by PWB warpage with very high accuracy.

Table 7.8. Solder Bump Fatigue Reliability Comparison between Prediction Model and Experiments for Different Cases

Case	**1**	**2**	**3**	**4**
Max. Initial PWB Warpage at Room Temperature (mm)	1.833	2.013	2.171	2.425
Warpage Shape	Concave Up	Concave Up	Concave Up	Concave Up
PBGA Dimension (mm)	27 × 27	27 × 27	35 × 35	35 × 35
Distance from PBGA Center to Board Center (mm)	67	30	67	30
Fatigue Life from Prediction Model (Cycles)	2633	2465	2507	2277
Experimental Fatigue Life (Cycles)	2750	2625	2400	2250
Difference	-4.3 %	-6.1 %	4.4 %	1.2 %

7.5. Chapter Summary

In this research, the effect of PWB warpage on the low cycle fatigue of the solder bumps on PBGA packages was studied based on the projection moiré measurement system and finite element modeling. This study successfully documents the correlation between PWB warpage and fatigue reliability of solder bumps on board assemblies.

In order to improve the simulation accuracy, 3-D FE models were developed and validated according to the measured warpage values obtained from the projection moiré technique. The FE results show that initial PWB warpage has significant effects on fatigue reliability of solder bumps on PBGA packages. This is because the initial PWB warpage affects the shape, height, and diameter of the solder bumps on board assemblies. During the thermal cyclic conditions, PWB warpage causes large stress and strain in bumps, and reduces the bump fatigue reliability. For a PWB with higher initial warpage, the fatigue life of solder bumps on board assemblies is reduced. A PWB with concave shape will decrease the reliability of solder bumps more than a PWB with convex shape. The dimensions and locations of packages, and solder bump materials also affect the bump fatigue life.

To validate the above FEA simulation results, and accurately set up a correlation between PWB warpage and solder bump fatigue reliability on board assemblies, accelerated thermal cycling tests were performed using an ESPEC test chamber. The experimental test results are consistent with the above simulation results. For a PWB with higher initial warpage, the fatigue life of solder bumps on board assemblies is reduced. The solder bumps have longer fatigue life if the PWB has small initial warpage, and the chip package is small in size and is located far from the PWB center. In addition, with

increasing the number of thermal cycles, the PWB warpage increases. The assembled PBGA packages constrain the deformation of the PWB samples during thermal cyclic conditions. For an electronic package in large size, and located near the board center, it will have more effect on the board warpage. The above guidelines can be used to estimate the thermomechanical reliability of solder bumps on board assemblies with initial PWB warpage.

Design of experiments and an advanced prediction model were developed to study the correlation between PWB warpage and solder bump fatigue reliability based on the FEA solutions and experimental results. Based on the FE simulation results, a bilinear regression model was generated to estimate the fatigue life of solder bumps affected by PWB warpage. In order to correlate the experimental and simulation results, and further improve the accuracy of the prediction model, an advanced kriging model was developed in this study. The kriging model can be successfully used to investigate the correlation between PWB warpage and solder bump thermal fatigue reliability with very high accuracy.

In order to develop a more general analytical model to predict the solder bump fatigue life affected by initial PWB warpage on board assemblies, a parameter representing the board curvature should be included in the reduced bilinear regression model and the kriging model. Therefore, the prediction models can be used to predict the thermal fatigue reliability of solder bumps on PBGA packages for any PWB assembly.

CHAPTER 8

CONCLUSIONS

The research objectives, approaches, results, and conclusions for each research area in the thesis work are summarized in this chapter. Main research efforts and contributions are presented. Finally, the recommendations for future study are also provided.

8.1. Conclusions

Warpage is a major thermomechanical reliability concern for board-level electronic packaging. PWB and component warpage results from coefficient of thermal expansion (CTE) mismatch among the materials that make up PWBAs such as solder, copper, FR-4, encapsulation molding, and silicon. In addition, material elastic modulus, the thickness of PWBs and electronic packages, temperature loading conditions, and PWB boundary constraints have significant effects on the warpage of PWBs and assembled packages. Warpage occurring during surface-mount assembly reflow processes and normal operations may lead to severe solder bump fatigue failure, die cracking, component misregistration, and delamination of the solder bumps between electronic components and the PWB. As the electronic packaging industry continues to move towards the productions of thin PWBs, high density PWBAs, miniature electronic components, and three-dimensional (3-D) stacked dies and packages, measurement and reduction of warpage become more significant and necessary in order to estimate and improve the reliability of electronic packaging in high volume manufacturing.

In this research, an automatic real-time warpage measurement system with projection moiré and shadow moiré techniques was developed and implemented. The objective is to make the system versatile to simulate industrial assembly reflow processes, improve the system precision and reliability, measure and analyze the warpage of PWBs and different types of assembled electronic packages, accurately estimate PWB and PWBA warpage with the classical laminated plate theory, and provide valid numerical models to study the correlation between PWB warpage and solder bump thermal fatigue reliability on board assemblies.

In order to achieve the ideal heating rate, the forced convective heating system was redesigned and integrated with the projection moiré and shadow moiré warpage measurement techniques. A 3-phase power of 72 KW was supplied to the heaters; the heater surface area was increased to 3.26 m^2, which is 5.62 times larger than the original heating area; and the system volume was reduced to 0.31 m^3. Thermal insulation was used to fill the interior of the oven, decreasing its volume so that the system can reach the ideal heating ramp rate. Connections between the oven and the centrifugal fan and between the ducts were airproofed with thermal insulation wraps to ensure a better airflow circulation loop. The improved heating system is able to achieve the heating ramp rate of 1.82 °C/second, provide uniform heating and optimal transient responses, generate zero static state error, and reduce temperature gradients through test vehicle thickness. An advanced controller created using LABVIEW virtual instruments was implemented to control the heating performance of the oven and real-time warpage measurement during the thermal reflow process. The developed convective reflow-projection moiré warpage measurement system is the first real-time, non-contact, and full-field warpage

measurement system with the capability of simulating any type of reflow soldering processes.

The automatic package detection and segmentation algorithms based on the mask image model and snake model were developed for the projection moiré warpage measurement system. The mask image model can be generated by defining the pixel values inside the package area to be 1's, and outside the package area to be 0's; the snake model can converge to the exterior boundaries of chip packages by using the Greedy algorithm. Based on these segmentation algorithms, the improved projection moiré system can be used to measure the warpage across the PWB and assembled omnidirectional electronic packages respectively and accurately. Both the mask image model and snake model can be used for real-time warpage measurements, and both have high resolutions to determine the warpage across the PWB and populated multiple chip packages. The mask image segmentation method has higher processing rate, and is better suited to evaluate the warpage of chip packages with small dimensions than the snake model. The real-time continuous and composite Hermite surface models are able to evaluate the PWB warpage values directly underneath the chip packages from PWBA displacement images. The experimental measurements of the PWBAs with different types of electronic packages show that the projection moiré system with the two automatic image segmentation algorithms is able to measure the warpage across PWBs and multiple chip packages individually with high resolution. The performances of the two automatic algorithms and manual segmentation method were evaluated and compared to illustrate their suitability and flexibility for real-time warpage measurements in this research.

The warpage behavior of PWBAs during different thermal reflow soldering processes was studied using the convective reflow and projection moiré measurement system. Three different PWBA configurations were considered here. Configuration 1 is the PWB assembled with one 35 mm × 35 mm PBGA; configuration 2 is the PWB assembled with two 35 mm × 35 mm PBGAs; configuration 3 is the PWB assembled with 6 chip packages. Each configuration was used to conduct both simulated RDRP and Lee optimized convective reflow profiles. The projection moiré technique was used to measure the PWBA warpage at initial room temperature, 150 °C heating, 210 °C, 150 °C cooling, and final room temperature. The experimental results show the warpage behavior across the PWBs and assembled electronic packages during the thermal reflow processes. After Lee optimized profile, the PWBAs have larger residual warpage than those using the RDRP profile. Therefore, using the typical RDRP reflow profile can not only decrease the residual warpage across the PWBAs, it can also save time and cost of the surface mount assembly process. With the increasing number of electronic packages, the maximum warpage change of the PWBAs decreased during the thermal reflow processes. The electronic packages have constraining effects on PWB warpage change. Also, the packages in large size and assembled near the PWB center have larger constraining effects on board warpage than those in smaller size and assembled far from the board center. Different types of packages have various effects on the PWB warpage. This study provided general guidelines for PWBA layout design and for improving the thermal and mechanical reliability of integrated PWB assemblies. In addition, the repeatability study shows that the projection moiré warpage measurement system has excellent suitability and reliability for online experimental measurement.

The classical laminated plate theory can be used to evaluate the warpage behavior of the PWB and PWBA samples during the thermal reflow process. Closed form solutions of the differential equations for the sample deformation from the classical lamination theory were generated to assess warpage. The rule of mixtures was used to estimate the effective material properties of the PWBA composites. The warpage values obtained from the theoretical models are highly sensitive to the thermal loads, the temperature gradients through the thickness of the samples, and the CTE values of the composite materials. The relative warpage results obtained from the analytical models and numerical models agreed well with the experimental results during the thermal reflow process. The simulation results of relative warpage values are slightly lower than the experimental ones. The analytical models have large discrepancy near the peak temperature due to viscoelastic relaxation and CTE change of the PWB/PWBA samples. The warpage results generated from the FE models have higher accuracy than those from the theoretical calculation. But the calculations for the FE models are much more complex and time consuming compared to the analytical models.

In this research, the effect of PWB warpage on the low cycle fatigue of the solder bumps on PBGA packages was studied based on the projection moiré measurement system and finite element modeling. This study successfully documents the correlation between PWB warpage and fatigue reliability of solder bumps on board assemblies.

In order to improve the simulation accuracy, 3-D FE models were developed and validated according to the measured warpage values obtained from the projection moiré technique. The FE results show that initial PWB warpage has significant effects on fatigue reliability of solder bumps on PBGA packages. For a PWB with higher initial

warpage, the fatigue life of solder bumps on board assemblies is reduced. A PWB with concave shape will decrease the reliability of solder bumps more than a PWB with convex shape. The dimensions and locations of packages, and solder bump materials also affect the bump fatigue life.

To validate the above FEA simulation results, and accurately set up a correlation between PWB warpage and solder bump fatigue reliability on board assemblies, accelerated thermal cycling tests were performed using an ESPEC test chamber. The experimental test results are consistent with the above simulation results. For a PWB with higher initial warpage, the fatigue life of solder bumps on board assemblies is reduced. The solder bumps have longer fatigue life if the package is small in size and is located far from the PWB center. In addition, with increasing the number of thermal cycles, the PWB warpage increases. The assembled PBGA packages constrain the deformation of the PWB samples during thermal cyclic conditions. For an electronic package in large size, and located near the board center, it will have more effect on the board warpage. The above guidelines can be used to estimate the thermomechanical reliability of solder bumps on board assemblies with initial PWB warpage.

Design of experiments and an advanced prediction model were developed to study the correlation between PWB warpage and solder bump fatigue reliability based on the FEA solutions and experimental results. Based on the FE simulation results, a bilinear regression model was generated to estimate the fatigue life of solder bumps affected by PWB warpage. In order to correlate the experimental and simulation results, and further improve the accuracy of the prediction model, an advanced kriging model was developed in this study. The kriging model can be successfully used to investigate the correlation

between PWB warpage and solder bump thermal fatigue reliability with very high accuracy.

8.2. Summary of Contributions

In this research, a real-time automatic warpage measurement system using the projection moiré and shadow moiré techniques during convective reflow processes was developed and implemented. The experimental system with the automatic package segmentation algorithms can simultaneously measure the warpage across PWBs and assembled omnidirectional chip packages in PWBAs. The correlation between PWB warpage and solder bump thermomechanical reliability was investigated based on the projection moiré system and finite element modeling. The detailed research contributions and impact are listed below.

I. A convective heating system was developed and integrated with the projection moiré warpage measurement system. The convective heating system can be applied to simulate reflow soldering processes with the maximum temperature ramp rate of 1.82 °C/second, provide uniform heating and optimal transient responses, generate zero static state error, and reduce temperature gradients through PWBAs, so that the projection moiré and shadow moiré warpage measurement system can provide more accurate warpage measurement results. An advanced controller created using LABVIEW was implemented to control the heating performance of the oven and real-time warpage measurement during the thermal reflow process. The developed convective reflow-projection moiré warpage measurement system is the first real-time, non-contact, and full-field warpage measurement system with the capability of simulating any type of reflow

soldering processes.

II. The automatic package detection and segmentation algorithms based on the mask image model and snake model were developed for the projection moiré warpage measurement system. The automatic algorithms can segment the PWB and assembled chip packages in any layout so that the warpage of the PWB and packages can be determined individually. Both the mask image model and snake model can be used for real-time warpage measurements, and both have high resolutions to determine the warpage across the PWB and populated multiple chip packages. The mask image segmentation method has higher processing rate, and is better suited to evaluate the warpage of chip packages with small dimensions than the snake model. The real-time continuous and composite Hermite surface models are able to evaluate the PWB warpage values directly underneath the chip packages from PWBA displacement images. The experimental measurements of the PWBAs with different types of electronic packages show that the developed post-processing techniques significantly increase the accuracy, flexibility, and reliability of the projection moiré measurement system.

III. The warpage behavior of PWBAs during different thermal reflow soldering processes was studied using the convective reflow and projection moiré measurement system. Three different PWBA configurations were considered in this study. The projection moiré technique was used to measure the PWBA warpage at initial room temperature, 150 °C heating, 210 °C, 150 °C cooling, and final room temperature during the typical RDRP and Lee optimized reflow profiles. The experimental results show that comparing with Lee optimized

profile, using the typical RDRP reflow profile can not only decrease the residual warpage across the PWBAs, it can also save time and cost of the surface mount assembly process. This study demonstrated the effects of different electronic packages on PWBA warpage, and provided general guidelines for PWBA layout design and for improving the thermal and mechanical reliability of integrated PWB assemblies.

IV. A repeatability study was performed on the convective reflow-projection moiré warpage measurement system. The study demonstrates that the projection moiré warpage measurement system has excellent suitability, reliability, and repeatability for online experimental measurement.

V. The classical laminated plate theory was used to evaluate the warpage behavior of the PWB and PWBA samples during the thermal reflow process. Closed form solutions of the differential equations for the sample deformation from the classical lamination theory were generated to assess warpage. The rule of mixtures was used to estimate the effective material properties of the PWBA composites. The warpage values obtained from the theoretical models are highly sensitive to the thermal loads, the temperature gradients through the thickness of the samples, and the CTE values of the composite materials. The relative warpage results obtained from the analytical models and numerical models agreed well with the experimental results during the thermal reflow process. The simulation results of relative warpage values are slightly lower than the experimental ones. The analytical models have large discrepancy near the peak temperature due to viscoelastic relaxation and CTE change of the PWB/PWBA samples. This

research provided an effective theoretical warpage prediction model to lead a better understanding to the PWBA warpage behavior during the thermal reflow assembly process. Also, this theoretical model saved much calculation time and cost compared to other analytical and numerical models.

VI. The effect of PWB warpage on the low cycle fatigue of the solder bumps on PBGA packages was studied based on the projection moiré measurement system and finite element modeling. This study successfully documents the correlation between PWB warpage and fatigue reliability of solder bumps on board assemblies. Finite element models were applied to predict the solder bump reliability on board assemblies affected by PWB warpage. The FE results show that initial PWB warpage has significant effects on fatigue reliability of solder bumps on PBGA packages. For a PWB with higher initial warpage, the fatigue life of solder bumps on board assemblies is reduced. A PWB with concave shape decreases the reliability of solder bumps more than a PWB with convex shape. The dimensions and locations of packages, and solder bump materials also affect the bump fatigue life.

VII. To accurately set up a correlation between PWB warpage and solder bump fatigue reliability on board assemblies, accelerated thermal cycling tests were performed. The experimental test results are consistent with the FE simulation results. For a PWB with higher initial warpage, the fatigue life of solder bumps on board assemblies is reduced. The solder bumps have longer fatigue life if the package is small in size and is located far from the PWB center. In addition, with increasing the number of thermal cycles, the PWB warpage increases. The assembled PBGA

packages constrain the deformation of the PWB samples during thermal cyclic conditions. The above guidelines can be used to estimate the thermomechanical reliability of solder bumps on board assemblies with initial PWB warpage.

VIII. Design of experiments and an advanced prediction model were developed to study the correlation between PWB warpage and solder bump fatigue reliability based on the FEA solutions and experimental results. Based on the FE simulation results, a bilinear regression model was generated to estimate the fatigue life of solder bumps affected by PWB warpage. In order to correlate the experimental and simulation results, and further improve the accuracy of the prediction model, an advanced kriging model was developed in this study. The kriging model can be successfully used to investigate the correlation between PWB warpage and solder bump thermal fatigue reliability with very high accuracy. Also, it saved a lot of cost and time for conducting experiments. This is the first research work that accurately documents the correlation between PWB warpage and the thermomechanical reliability of solder bumps on board assemblies.

8.3. Recommendations for Future Work

After the completion of this thesis study, there are still many challenging research facets to be explored. They include the development of the projection/shadow moiré warpage measurement system and the warpage study of the PWBs and different electronic packages in PWBAs. Some recommendations for future research work are listed below.

I. For the convective heating system, the heating application efficiency needs to be increased for future study, so that the system can utilize the power provided

further effectively and completely. Compatible coolers are desired to be installed into the system, so that the convective reflow-projection moiré measurement system can be used to conduct warpage measurement for PWBA test vehicles during the simulated accelerated thermal cycling tests.

II. A completely automated projection moiré measurement system needs to be integrated with the convective heating control system. Currently, two computers need to be operated simultaneously to perform the warpage measurement experiments during thermal reflow processes. These two systems could be unified into a single control system in order to conduct real-time warpage measurement more effectively and accurately.

III. This research successfully discussed how the PWB warpage affects the solder bump fatigue reliability on board assemblies. Furthermore, the correlation between the PWBA warpage and other failure modes of the electronic packages on board assemblies needs to be considered, for example, the delamination between the solder bumps and PWB, the interconnection failure on the board, package misregistration, and so on. The corresponding experimental study and finite element analysis could be conducted in the above areas.

IV. In order to develop a general analytical model to predict the solder bump fatigue reliability affected by initial PWB warpage on board assemblies, a parameter representing the board curvature should be included in the reduced bilinear regression model and the kriging model. Therefore, the prediction models can be used to predict the thermal fatigue reliability of solder bumps on PBGA packages for the PWBAs with different structures and dimensions.

V. Three-dimensional (3-D) packaging technologies have been widely used in many electronic products. The 3-D packages exploit the third or Z height dimension to provide a volumetric packaging solution for higher integration and performance of electronic components. Warpage is a significant reliability issue in stacked dies and stacked packages. Detailed investigation on the warpage behavior of the 3-D packages needs to be conducted in future research work to ensure the manufacturing of high-reliability and low-cost 3-D packages.

VI. As the environmental requirements to manufacture green electronic products, halogen-free flame retardants are desired to be used into PWBAs. Thermomechanical reliability and the corresponding manufacturing process of these novel materials need to be studied. The effects of the halogen-free materials and modified assembly processes on the PWBA warpage behavior need to be investigated using the convective reflow-projection moiré measurement system.

APPENDIX A

MATLAB CODE FOR AUTOMATIC PACKAGE DETECTION AND SEGMENTATION ALGORITHM

Appendix A includes the MATLAB source code designed for the automatic package detection and segmentation algorithm.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% Generation of Mask Image Model for 2 PBGA packages
% Input the data file created from the projection moiré system (*.out)
% Input the data type, data size, plot scale, and the corresponding mask file.
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% Definition

data_file='*.out';
data_type='int16';
data_size=[512, 480];
plot_scale=0.00039;
mask_file='Mask';

%Read file.out

fid_read = fopen(data_file,'r');
displacement = fread(fid_read,data_type);
fclose(fid_read);

displacement = reshape(displacement,data_size)';
displacement = double(displacement)*plot_scale*1000*25.4;  % unit: mm


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% Apply rectangular mask to the PWBA displacement image

fid_read = fopen(mask_file,'r');
```

```
mask = fread(fid_read,'uint8');
fclose(fid_read);
mask = reshape(mask,data_size)';
[mask_r mask_c] = find(mask~=0);
mask_r_min = min(mask_r); mask_r_max = max(mask_r);
mask_c_min = min(mask_c); mask_c_max = max(mask_c);
displacement = displacement(mask_r_min:mask_r_max,mask_c_min:mask_c_max);

% end


% Find the package edges in the displacement image

displacement1=EDGE(displacement,'canny',0.3);

%displacement2=edge(displacement,'sobel',10);
%displacement3=edge(displacement,'prewitt',10);
%displacement4=edge(displacement,'log',0.7);
%displacement5=edge(displacement,'roberts',15);
%displacement6=edge(displacement,'zerocross',0.8);
%imhist(displacement);

%figure;
%imshow(displacement1);


%Denoising using DCT filter

[row col] = size(displacement);
length = row*col;
disp_DCT = dct2(displacement);
disp_DCT_vec = reshape(disp_DCT,1,length);
disp_DCT_sort = sort(abs(disp_DCT_vec));
tao = disp_DCT_sort(round(length*0.98));

disp_DCT_mask = wthresh(disp_DCT,'s',tao);

% Inverse DCT

displacement = idct2(disp_DCT_mask);


% Find package edges in the displacement image after denoising;

displacement1_dn=EDGE(displacement,'canny',0.3);

%imshow(displacement1_dn);
%displacement2_dn=edge(displacement,'sobel',6.3);
%displacement3_dn=edge(displacement,'prewitt',6.3);
%displacement4_dn=edge(displacement,'log',0.55);
%displacement5_dn=edge(displacement,'roberts',7);
%displacement6_dn=edge(displacement,'zerocross',0.55);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% There are 2 PBGA packages in the displacement image.
% The following program can determine the package locations respectively.

b = bwboundaries(displacement1,'noholes');
b_size=size(b);


chip1_max_row=1;
chip1_min_row=row;
chip1_max_col=1;
chip1_min_col=col;


chip2_max_row=1;
chip2_min_row=row;
chip2_max_col=1;
chip2_min_col=col;

for i=1:b_size(1)

   j=b{i};
   j1=j(:,1)';
   j2=j(:,2)';

   if (chip1_max_row<max(j1)) && (chip1_min_row>min(j1)) && ((chip1_max_col<max(j2)) ||
(chip1_min_col>min(j2)))

      % chip1=j;
      chip1_max_row=max(j1);
      chip1_min_row=min(j1);
      chip1_max_col=max(j2);
      chip1_min_col=min(j2);

   elseif (chip2_max_row<max(j1) && chip2_min_row>min(j1)) && ((chip2_max_col<max(j2)) ||
(chip2_min_col>min(j2)))

      % chip2=j;
      chip2_max_row=max(j1);
      chip2_min_row=min(j1);
      chip2_max_col=max(j2);
      chip2_min_col=min(j2);

   end
end



% Generate Mask 1 for PBGA 1

mask1_x=[chip1_min_col,chip1_max_col,chip1_max_col,chip1_min_col,chip1_min_col];
mask1_y=[chip1_max_row,chip1_max_row,chip1_min_row,chip1_min_row,chip1_max_row];
mask1=poly2mask(mask1_x,mask1_y,row,col);
figure;
```

```
imshow(mask1);


% Generate Mask 2 for PBGA 2

mask2_x=[chip2_min_col,chip2_max_col,chip2_max_col,chip2_min_col,chip2_min_col];
mask2_y=[chip2_max_row,chip2_max_row,chip2_min_row,chip2_min_row,chip2_max_row];
mask2=poly2mask(mask2_x,mask2_y,row,col);
figure;
imshow(mask2);



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Warpage Calculation for PWB

displacement=Rotation(displacement,'Yinyan LS'); %Rotation for PWB
dispcal=displacement;

min_displacement = min(min(dispcal));
max_displacement = max(max(dispcal));

min_z = floor(min_displacement/5)*5;  % Make min Z a multiple of 5
max_z = ceil(max_displacement/5)*5;  % Make max Z a multiple of 5

dif_displacement = max_displacement - min_displacement;


if dif_displacement < 1e-9,  % if it is a plane

  min_z = -1; max_z = 1;
  displacement = ones(size(displacement))*min_displacement;

end



% Warpage Calculation for PWB without packages

dispcal_PWB=dispcal.*(ones(row,col)-mask1-mask2);

max_PWB_temp=max(max(dispcal_PWB));
min_PWB_temp=min_displacement;

dif_PWB_temp=max_PWB_temp-min_PWB_temp;



% Warpage Calculation for chip package 1 in any directional angle with respect to the PWB edges

dispcal_chip1=dispcal.*mask1;
chip1=dispcal_chip1(chip1_min_row:chip1_max_row, chip1_min_col:chip1_max_col);
```

```
% Rotation for PWB and chip package 1


chip1=Rotation(chip1,'Yinyan LS');

max_chip1=max(max(chip1));
min_chip1=max_chip1;
temp_min=min(min(chip1));

[chip1_r, chip1_c]=size(chip1);

for i=1:chip1_r
   for j=1:chip1_c

      if chip1(i,j)<min_chip1 && chip1(i,j)~=temp_min,
        min_chip1=chip1(i,j);
      end

   end
end

dif_chip1=max_chip1-min_chip1;



% Warpage Calculation for chip package 2 in any directional angle with respect to the PWB edges

dispcal_chip2=dispcal.*mask2;

chip2=dispcal_chip2(chip2_min_row:chip2_max_row, chip2_min_col:chip2_max_col);


% Rotation for PWB and chip package 2


chip2=Rotation(chip2,'Yinyan LS');

max_chip2=max(max(chip2));
min_chip2=max_chip2;
temp_min=min(min(chip2));

[chip2_r, chip2_c]=size(chip2);

for i=1:chip2_r
   for j=1:chip2_c

      if chip2(i,j)<min_chip2 && chip2(i,j)~=temp_min,
        min_chip2=chip2(i,j);
      end

   end
end


dif_chip2=max_chip2-min_chip2;
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Warpage calculation underneath the PBGAs


[PWB_Comp_min1,
PWB_Comp_max1]=Comp_Surf(chip1_min_row,chip1_max_row,chip1_min_col,chip1_max_col,displace
ment);


[PWB_Comp_min2,
PWB_Comp_max2]=Comp_Surf(chip2_min_row,chip2_max_row,chip2_min_col,chip2_max_col,displace
ment);


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% Final warpage results for the PWB


max_PWB=max([max_PWB_temp,PWB_Comp_max1,PWB_Comp_max2]);

min_PWB=min([min_PWB_temp,PWB_Comp_min1,PWB_Comp_min2]);

dif_PWB=max_PWB-min_PWB;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% Plot displacement

% Set figure and axis properties


length = length_in_x*25.4;
width = width_in_y*25.4;


[row col] = size(displacement);


dispcal=displacement;

min_displacement = min(min(dispcal));
max_displacement = max(max(dispcal));

min_z = floor(min_displacement/5)*5;  % Make min Z a multiple of 5
max_z = ceil(max_displacement/5)*5;  % Make max Z a multiple of 5


dif_displacement = max_displacement - min_displacement;
```

```
if dif_displacement < 1e-9,

  min_z = -1;
  max_z = 1;
  displacement = ones(size(displacement))*min_displacement;

end


figure('Color','white','Units','pixels','Position',[300 75 620 440]);        %[500 50 560 420]

x=0:length/(col-1):length;
y=0:width/(row-1):width;


h_surf=surf(x,y,displacement);

axis([0 length 0 width]); axis('ij');

set(gca,'Units','pixels','Position',[50 80 540 315],'FontSize',12);        %[30 60 520 315]

set(gca,'DataAspectRatio',[1,1,(max_z-min_z)*20/(length+width)]);

set(gca,'ZLim',[min_z,max_z],'ZTick',[min_z,(max_z+min_z)/2,max_z]);



% Labels, title, and text

t_xlabel = 'bottom edge (mm)';
t_ylabel = 'right edge (mm)';
t_zlabel = 'absolute displacement (mm)';


t_text = sprintf('max. PWB warpage = %2.1f mm\nmax. chip package 1 warpage = %2.1f mm\nmax. chip
package 2 warpage = %2.1f mm', dif_PWB,dif_chip1,dif_chip2);


h_title = title('warpage @ room temperature','Units','pixels','Position',[200 280]);

h_xlabel = xlabel(t_xlabel,'Units','pixels','Position',[130 10]);
h_ylabel = ylabel(t_ylabel,'Units','pixels','Position',[320 10]);
h_zlabel = zlabel(t_zlabel,'Units','pixels','Position',[-45,135]);

h_text = text(200,-100,t_text,'Units','pixels');


set(h_title,'FontSize',12,'FontWeight','bold','HorizontalAlignment','center');
set(h_xlabel,'FontSize',12,'FontWeight','bold');
set(h_ylabel,'FontSize',12,'FontWeight','bold');
set(h_zlabel,'FontSize',12,'FontWeight','bold');

set(h_text,'FontSize',12,'FontWeight','bold','HorizontalAlignment','center');


% Adjust the plot
```

```
view(45,30);

grid on;

shading interp;

% Set the colormap

colormap(jet);

% Set the colorbar

h_colorbar = colorbar('horiz');


% Finished

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% Continuous and Composite Surface Model
function [z_min,z_max]=Comp_Surf(y_min,y_max,x_min,x_max,M)
%
% Input the location of the chip package. Matrix includes all pixels of the PWBA displacement.
% Construct a C1 Hermite Surface Model to simulate the PWB area underneath the package.
%
% y means the row number, and x means the column number.
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


P00=[y_min,x_min,M(y_min,x_min)]';
P01=[y_min,x_max,M(y_min,x_max)]';
P10=[y_max,x_min,M(y_max,x_min)]';
P11=[y_max,x_max,M(y_max,x_max)]';


Pw00=[0,1,M(y_min,x_min)-M(y_min,x_min-1)]'; % Gradient in X
Pw01=[0,1,M(y_min,x_max+1)-M(y_min,x_max)]';
Pw10=[0,1,M(y_max,x_min)-M(y_max,x_min-1)]';
Pw11=[0,1,M(y_max,x_max+1)-M(y_max,x_max)]';


Pu00=[1,0,M(y_min,x_min)-M(y_min-1,x_min)]'; % Gradient in Y
Pu01=[1,0,M(y_min,x_max)-M(y_min-1,x_max)]';
Pu10=[1,0,M(y_max+1,x_min)-M(y_max,x_min)]';
Pu11=[1,0,M(y_max+1,x_max)-M(y_max,x_max)]';


Puw00=cross(Pu00,Pw00); % Twist Vectors
Puw01=cross(Pu01,Pw01);
Puw10=cross(Pu10,Pw10);
Puw11=cross(Pu11,Pw11);


% Pixel values in Z

B=[P00(3),P01(3),Pw00(3),Pw01(3);P10(3),P11(3),Pw10(3),Pw11(3);Pu00(3),Pu01(3),Puw00(3),Puw01(3
);Pu10(3),Pu11(3),Puw10(3),Puw11(3)];


i=1;


for u=0:0.2:1

   for w=0:0.2:1

      U=[u^3,u^2,u,1];
      W=[w^3,w^2,w,1];
      MF=[2,-2,1,1;-3,3,-2,-1;0,0,1,0;1,0,0,0];
      P(i)=U*MF*B*MF'*W';
      i=i+1;
```

```
    end

end


%Find the max. and min. pixel values.

z_max=max(P);
z_min=min(P);



% Finished

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

APPENDIX B

ANSYS APDL CODE FOR FINITE ELEMENT MODELING

Appendix B includes the APDL source code designed for the finite element modeling to study the correlation between the PWB warpage and solder bump thermal fatigue reliability on board assemblies in ANSYS.

```
!*************************************************************************************

!************************************************** Geometric Modeling

/PREP7

! PBGA Modeling

K,10001,6.5,2.5,0.56            ! Set Key Points for Geometric Modeling
K,10002,2.5,6.5,0.56
K,10003,2.5,28.5,0.56
K,10004,6.5,32.5,0.56
K,10005,28.5,32.5,0.56
K,10006,32.5,28.5,0.56
K,10007,32.5,6.5,0.56
K,10008,28.5,2.5,0.56
K,10009,6.5,2.5,1.73
K,10010,2.5,6.5,1.73
K,10011,2.5,28.5,1.73
K,10012,6.5,32.5,1.73
K,10013,28.5,32.5,1.73
K,10014,32.5,28.5,1.73
K,10015,32.5,6.5,1.73
K,10016,28.5,2.5,1.73

FLST,2,8,3                      ! Package Geometric Modeling

FITEM,2,10012
FITEM,2,10013
FITEM,2,10014
FITEM,2,10015
```

```
FITEM,2,10016
FITEM,2,10009
FITEM,2,10010
FITEM,2,10011

A,P51X                  ! Package Geometric Modeling
FLST,2,8,3

FITEM,2,10004
FITEM,2,10005
FITEM,2,10006
FITEM,2,10007
FITEM,2,10008
FITEM,2,10001
FITEM,2,10002
FITEM,2,10003

A,P51X                  ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10011
FITEM,2,10003
FITEM,2,10002
FITEM,2,10010

A,P51X                  ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10002
FITEM,2,10001
FITEM,2,10009
FITEM,2,10010

A,P51X                  ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10001
FITEM,2,10008
FITEM,2,10016
FITEM,2,10009

A,P51X                  ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10007
FITEM,2,10008
FITEM,2,10016
FITEM,2,10015

A,P51X                  ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10014
FITEM,2,10006
FITEM,2,10007
FITEM,2,10015
```

```
A,P51X                          ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10014
FITEM,2,10006
FITEM,2,10005
FITEM,2,10013

A,P51X                          ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10005
FITEM,2,10013
FITEM,2,10012
FITEM,2,10004

A,P51X                          ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10004
FITEM,2,10012
FITEM,2,10011
FITEM,2,10003

A,P51X                          ! Package Geometric Modeling
FLST,2,4,3

FITEM,2,10011
FITEM,2,10010
FITEM,2,10002
FITEM,2,10003

A,P51X                          ! Package Geometric Modeling

FLST,2,10,5,ORDE,2

FITEM,2,1
FITEM,2,-10
VA,P51X
BLC4,0,0,35,35,0.56             ! Substrate Modeling


! Solder Bump Modeling

SPH4,1.625,1.625,0.375          ! Generate the First Solder Bump
FLST,3,1,6,ORDE,1
FITEM,3,3

VGEN, ,P51X, , ,0,0,-0.225, , ,1
VSBA,      3,     11
VDELE,      4

BLC4,0,0,10,10,2
FLST,3,1,6,ORDE,1

FITEM,3,3
```

```
VGEN, ,P51X, , ,0,0,-2.45, , ,1
FLST,2,4,6,ORDE,3

FITEM,2,1
FITEM,2,-3
FITEM,2,5

VPTN,P51X
VDELE,      7, , ,1
VDELE,      4, , ,1

FLST,3,1,6,ORDE,1                ! Generate Different Solder Bumps with pitch 1.27 mm
FITEM,3,6
VGEN,26,P51X, , ,1.27,0,0, ,0

FLST,3,1,6,ORDE,1                ! Generate Different Solder Bumps with pitch 1.27 mm
FITEM,3,28
VGEN,26,P51X, , ,0,1.27,0, ,0

FLST,3,1,6,ORDE,1                ! Generate Different Solder Bumps with pitch 1.27 mm
FITEM,3,6
VGEN,26,P51X, , ,0,1.27,0, ,0

FLST,3,1,6,ORDE,1                ! Generate Different Solder Bumps with pitch 1.27 mm
FITEM,3,78
VGEN,25,P51X, , ,1.27,0,0, ,0

BLC4,0,0,203.2,139.7

FLST,3,1,5,ORDE,1
FITEM,3,419
AGEN, ,P51X, , ,-144.1,-22.35,-0.45, , ,1


!*********************************************************************************

!************************************************** Material Properties


! FR-4   2

MPTEMP                           ! Input Temperature Dependent Material Properties

MPTEMP,1,303,368,383,398,423,543


! FR-4 Elastic Modulus

MPDATA,EX,2,1,22400,20680,19970,19300,17920,16000
MPDATA,EZ,2,1,22400,20680,19970,19300,17920,16000
MPDATA,EY,2,1,1600,1200,1100,1000,600,450


! FR-4 Poisson's Ratio

MPDATA,NUXZ,2,1,0.1360,0.1360,0.1360,0.1360,0.1360,0.1360
```

```
MPDATA,NUXY,2,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425
MPDATA,NUYZ,2,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425


! FR-4 Coefficient of Thermal Expansion

MPDATA,ALPX,2,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPZ,2,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPY,2,1,86.5e-6,86.5e-6,243e-6,400.e-6,400.e-6,400.e-6


! FR-4 Shear Modulus

MPDATA,GXZ,2,1,630,600,550,500,450,441
MPDATA,GXY,2,1,199,189,173,157,142,139.3
MPDATA,GYZ,2,1,199,189,173,157,142,139.3



! Solder Bump   3

MP, ALPX, 3, 21.0E-6

MPTEMP                          ! Input Temperature Dependent Material Properties
MPTEMP, 1, 248, 298, 358, 398

MPDATA, EX, 3, 1, 27390, 19650, 15270, 11680
MPDATA, EY, 3, 1, 27390, 19650, 15270, 11680
MPDATA, EZ, 3, 1, 27390, 19650, 15270, 11680

MPDATA, GXY,3,1,9782,7018,5454,4171
MPDATA, GYZ,3,1,9782,7018,5454,4171
MPDATA, GXZ,3,1,9782,7018,5454,4171

MP, NUXY, 3, 0.4
MP, NUYZ, 3, 0.4
MP, NUXZ, 3, 0.4

TB, MKIN, 3, 4                  ! Create Table for Stress and Strain Relationship
TBTEMP, , STRAIN

TBDATA, 1, 0.0010, 0.0020, 0.0030, 0.0040, 0.0050
TBTEMP, 248
TBDATA, 1, 27.39, 41.36, 47.93, 50.30, 50.77
TBTEMP, 298
TBDATA, 1, 19.65, 29.68, 34.12, 36.35, 37.24
TBTEMP, 358
TBDATA, 1, 15.27, 22.51, 26.00, 27.83, 28.64
TBTEMP, 398
TBDATA, 1, 11.68, 16.12, 18.56, 19.88, 20.55

TB, CREEP, 3, 1, 1              ! Create Creep Calculating Formulation
TBDATA, 7, 1.84E-4, 5.2, 0, 6013.95, 0, 1
```

```
! PBGA Molding   4

MP,EX  ,4,15000                 ! Input Material Properties
MP,PRXY,4,0.15
MP,ALPX,4,17.5e-6
MP,DENS,4,3.0e-6



! BT FR4   5

MP,EX  ,5,14000                 ! Input Material Properties
MP,PRXY,5,0.15
MP,ALPX,5,15e-6
MP,DENS,5,3.0e-6



! PWB Copper   6

MP,EX  ,6,79510                 ! Input Material Properties
MP,PRXY,6,0.32
MP,ALPX,6,18.94e-6
MP,DENS,6,8.94e-6



!*********************************************************************************

!************************************************** Element Assignment

ET,1,SOLID45                    ! Define Element Type

ET,2,SOLID95                    ! Define Element Type

ET,3,SHELL91,,1                 ! Define Element Type

ET,4,PLANE82                    ! Define Element Type



! PWB

pwb_len = 203.2                 ! PWB Length in X-Direction: 8"
pwb_wid = 139.7                 ! PWB Width in Y-Direction: 5.5"
pwb_nls = 7                     ! PWB Number of Layers

*DIM,pwb_hls,ARRAY,pwb_nls

pwb_het = 0.631                 ! PWB Height in Z-Direction: 0.0248"
pwb_hls(1) = 0.018,0.127,0.018,0.305,0.018,0.127,0.018

! Assign Real Constants

sh91 = 3
```

```
mat_pwf = 2
mat_pwc = 6


R,sh91                          ! Real Constants for SHELL91

RMODIF,sh91,1   ,pwb_nls
RMODIF,sh91,19  ,mat_pwf,0,pwb_hls(2)     ! 2nd layer: FR-4
RMODIF,sh91,25  ,mat_pwc,0,pwb_hls(3)     ! 3rd layer: Copper
RMODIF,sh91,31  ,mat_pwf,0,pwb_hls(4)     ! 4th layer: FR-4
RMODIF,sh91,37  ,mat_pwc,0,pwb_hls(5)     ! 5th layer: Copper
RMODIF,sh91,43  ,mat_pwf,0,pwb_hls(6)     ! 6th layer: FR-4
RMODIF,sh91,13  ,mat_pwc,0,pwb_hls(1)     ! 1st layer: Copper trace
RMODIF,sh91,49  ,mat_pwc,0,pwb_hls(7)     ! 7th layer: Copper trace



!*********************************************************************************

!************************************************* Meshing


! Glue

FLST,2,101,5,ORDE,101

FITEM,2,11                      ! Select Elements to Glue
FITEM,2,22
FITEM,2,26
FITEM,2,28
FITEM,2,33
FITEM,2,39
FITEM,2,43
FITEM,2,47
FITEM,2,51
FITEM,2,55
FITEM,2,59
FITEM,2,63
FITEM,2,67
FITEM,2,71
FITEM,2,75
FITEM,2,79
FITEM,2,83
FITEM,2,87
FITEM,2,91
FITEM,2,95
FITEM,2,99
FITEM,2,103
FITEM,2,107
FITEM,2,111
FITEM,2,115
FITEM,2,119
FITEM,2,123
FITEM,2,127
FITEM,2,131
FITEM,2,135
```

```
FITEM,2,139                    ! Select Elements to Glue
FITEM,2,143
FITEM,2,147
FITEM,2,151
FITEM,2,155
FITEM,2,159
FITEM,2,163
FITEM,2,167
FITEM,2,171
FITEM,2,175
FITEM,2,179
FITEM,2,183
FITEM,2,187
FITEM,2,191
FITEM,2,195
FITEM,2,199
FITEM,2,203
FITEM,2,207
FITEM,2,211
FITEM,2,215
FITEM,2,219
FITEM,2,223
FITEM,2,227
FITEM,2,231
FITEM,2,235
FITEM,2,239
FITEM,2,243
FITEM,2,247
FITEM,2,251
FITEM,2,255
FITEM,2,259
FITEM,2,263
FITEM,2,267
FITEM,2,271
FITEM,2,275
FITEM,2,279
FITEM,2,283
FITEM,2,287
FITEM,2,291
FITEM,2,295
FITEM,2,299
FITEM,2,303
FITEM,2,307
FITEM,2,311
FITEM,2,315
FITEM,2,319
FITEM,2,323
FITEM,2,327
FITEM,2,331
FITEM,2,335
FITEM,2,339
FITEM,2,343
FITEM,2,347
FITEM,2,351
FITEM,2,355
FITEM,2,359
```

```
FITEM,2,363                    ! Select Elements to Glue
FITEM,2,367
FITEM,2,371
FITEM,2,375
FITEM,2,379
FITEM,2,383
FITEM,2,387
FITEM,2,391
FITEM,2,395
FITEM,2,399
FITEM,2,403
FITEM,2,407
FITEM,2,411
FITEM,2,415
FITEM,2,419

AOVLAP,P51X


FLST,2,102,6,ORDE,2
FITEM,2,1
FITEM,2,-102

VGLUE,P51X                     ! Glue Whole PWBA Model


! Mesh Package Molding

VSEL,S,LOC,X,0,35              ! Mesh Package Molding
VSEL,R,LOC,Y,0,35
VSEL,R,LOC,Z,0.56,1.73

CM,bgamold,VOLU

MSHKEY,0
MSHAPE,1,3D

ESIZE,4                        ! Set Mesh Size
VATT,4,-1,1

VMESH,bgamold


! Mesh Solder Bumps

VSEL,S,LOC,X,0,35              ! Mesh Solder Bumps
VSEL,R,LOC,Y,0,35
VSEL,R,LOC,Z,0,-0.45

CM,bgabump,VOLU

MSHKEY,0
MSHAPE,1,3D

ESIZE,0.9                      ! Set Mesh Size
VATT,3,-1,2
```

```
VMESH,bgabump


! Mesh Package Substrate

VSEL,S,LOC,X,0,35               ! Mesh Package Substrate
VSEL,R,LOC,Y,0,35
VSEL,R,LOC,Z,0,0.56

CM,bgasub,VOLU

MSHKEY,0
MSHAPE,1,3D

ESIZE,4                         ! Set Mesh Size
VATT,5,-1,2

VMESH,bgasub


! Mesh PWB

ASEL,S,LOC,X,-84.1,119.1        ! Mesh PWB
ASEL,R,LOC,Y,-52.35,87.35
ASEL,R,LOC,Z,-0.449,-0.451

CM,pwb,AREA
AATT,-1,sh91,sh91

MSHKEY,0
MSHAPE,1,2D

ESIZE,9                         ! Set Mesh Size

AMESH,pwb

FINISH                          ! Finish Meshing


!*************************************************************************************

!************************************************** Boundary Conditions

/SOL

FLST,2,2,4,ORDE,2

FITEM,2,840
FITEM,2,842

/GO

DL,P51X, ,UZ,                   ! Set Boundary Constrains in Z-Direction
```

```
!*************************************************************************************

!************************************************** Temperature Profile

/SOLU

nlgeom,on                       ! Turn on Large Deformation
autots,on                       ! Turn on Automatic Time Stepping for Solution

TREF,456                        ! Set Reference Temperature at Stress Free Temperature

allsel,all
BF,all,temp,298                 ! Set Thermal Loading

tmp_uif = 298
tmp_grd = 3.1                   ! Set Temperature Gradient through PWB

ar30 = tmp_uif + tmp_grd*3
ar31 = tmp_uif + tmp_grd*2
ar32 = tmp_uif + tmp_grd
ar33 = tmp_uif
allsel,all

ESEL,ALL
ESEL,S,TYPE,,sh91

BFE,ALL,TEMP,29  ,ar33,ar33,ar33,ar33    ! Set PWB Bottom Layer
BFE,ALL,TEMP,25  ,ar33,ar33,ar33,ar33
BFE,ALL,TEMP,21  ,ar32,ar32,ar32,ar32
BFE,ALL,TEMP,17 ,ar32,ar32,ar32,ar32
BFE,ALL,TEMP,13 ,ar31,ar31,ar31,ar31
BFE,ALL,TEMP,9 ,ar31,ar31,ar31,ar31
BFE,ALL,TEMP,5 ,ar30,ar30,ar30,ar30
BFE,ALL,TEMP,1 ,ar30,ar30,ar30,ar30      ! Set PWB Top Layer

allsel,all

TIME,150                        ! Set Ending Time for Load Step

NSUBST,3,9,1

OUTRES,all,last                 ! Output Result of Last Sub-Step

SOLVE
SAVE, case1_LS1,DB,             ! Save Result


! Load Step 2: t=10min, T=25C

allsel,all
BF,all,temp,298                 ! Set Thermal Loading

TIME,750                        ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last                 ! Output Result of Last Sub-Step
```

```
SOLVE
SAVE, case1_LS2,DB,              ! Save Result


! Load Step 3: t=727sec, T=25C-->125C

allsel,all
BF,all,temp,398                  ! Set Thermal Loading

TIME,1477                        ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS3,DB,              ! Save Result


! Load Step 4: t=10min, T=125C

allsel,all
BF,all,temp,398                  ! Set Thermal Loading

TIME,2077                        ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS4,DB,              ! Save Result


! Load Step 5: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218                  ! Set Thermal Loading

TIME,3277                        ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS5,DB,              ! Save Result


! Load Step 6: t=10min, T=-40C

allsel,all
BF,all,temp,218                  ! Set Thermal Loading

TIME,3877                        ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS6,DB                ! Save Result
```

```
! Load Step 7: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,5077                       ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS7,DB               ! Save Result


! Load Step 8: t=10min, T=125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,5677                       ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS8,DB,             ! Save Result


! Load Step 9: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,6877                       ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS9,DB,             ! Save Result


! Load Step 10: t=10min, T=-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,7477                       ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS10,DB              ! Save Result


! Load Step 11: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading
```

```
TIME,8677                    ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS11,DB           ! Save Result


! Load Step 12: t=10min, T=125C

allsel,all
BF,all,temp,398              ! Set Thermal Loading

TIME,9277                    ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS12,DB          ! Save Result


! Load Step 13: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218              ! Set Thermal Loading

TIME,10477                   ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS13,DB          ! Save Result


! Load Step 14: t=10min, T=-40C

allsel,all
BF,all,temp,218              ! Set Thermal Loading

TIME,11077                   ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS14,DB           ! Save Result


! Load Step 15: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398              ! Set Thermal Loading

TIME,12277                   ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last
```

```
SOLVE
SAVE,case1_LS15,DB              ! Save Result


! Load Step 16: t=10min, T=125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,12877                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS16,DB             ! Save Result


! Load Step 17: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,14077                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS17,DB             ! Save Result


! Load Step 18: t=10min, T=-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,14677                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS18,DB              ! Save Result


! Load Step 19: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,15877                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS19,DB              ! Save Result
```

```
! Load Step 20: t=10min, T=125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,16477                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS20,DB             ! Save Result


! Load Step 21: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,17677                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS21,DB             ! Save Result


! Load Step 22: t=10min, T=-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,18277                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS22,DB              ! Save Result


! Load Step 23: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,19477                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS23,DB              ! Save Result


! Load Step 24: t=10min, T=125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading
```

```
TIME,20077                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS24,DB,        ! Save Result


! Load step 25: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218             ! Set Thermal Loading

TIME,21277                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS25,DB,        ! Save Result


! Load Step 26: t=10min, T=-40C

allsel,all
BF,all,temp,218             ! Set Thermal Loading

TIME,21877                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS26,DB         ! Save Result


! Load Step 27: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398             ! Set Thermal Loading

TIME,23077                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS27,DB          ! Save Result


! Load Step 28: t=10min, T=125C

allsel,all
BF,all,temp,398             ! Set Thermal Loading

TIME,23677                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last
```

```
SOLVE
SAVE, case1_LS28,DB,            ! Save Result


! Load Step 29: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,24877                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS29,DB,            ! Save Result


! Load Step 30: t=10min, T=-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,25477                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS30,DB              ! Save Result


! Load Step 31: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,26677                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS31,DB              ! Save Result


! Load Step 32: t=10min, T=125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,27277                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS32,DB             ! Save Result
```

```
! Load Step 33: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,28477                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS33,DB             ! Save Result


! Load Step 34: t=10min, T=-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,29077                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS34,DB              ! Save Result


! Load Step 35: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,30277                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS35,DB              ! Save Result


! Load Step 36: t=10min, T=125C

allsel,all
BF,all,temp,398                 ! Set Thermal Loading

TIME,30877                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS36,DB             ! Save Result


! Load Step 37: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading
```

```
TIME,32077                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS37,DB         ! Save Result


! Load Step 38: t=10min, T=-40C

allsel,all
BF,all,temp,218             ! Set Thermal Loading

TIME,32677                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS38,DB          ! Save Result


! Load Step 39: t=20min, T=-40C-->125C

allsel,all
BF,all,temp,398             ! Set Thermal Loading

TIME,33877                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS39,DB          ! Save Result


! Load Step 40: t=10min, T=125C

allsel,all
BF,all,temp,398             ! Set Thermal Loading

TIME,34477                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE, case1_LS40,DB         ! Save Result


! Load Step 41: t=20min, T=125C-->-40C

allsel,all
BF,all,temp,218             ! Set Thermal Loading

TIME,35677                  ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last
```

```
SOLVE
SAVE, case1_LS41,DB             ! Save Result


! Load Step 42: t=10min, T=-40C

allsel,all
BF,all,temp,218                 ! Set Thermal Loading

TIME,36277                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS42,DB              ! Save Result


! Load Step 43: t=7.88min, T=-40C-->25C

allsel,all
BF,all,temp,298                 ! Set Thermal Loading

TIME,36750                      ! Set Ending Time for Load Step
NSUBST,3,9,1
OUTRES,all,last

SOLVE
SAVE,case1_LS43,DB              ! Save Result



!************************************************** Finished

!*******************************************************************************
!*******************************************************************************
```

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