Effect of Package Design and Layout on BGA Solder Joint Reliability of an Organic C4 Package

Biju Chandran[a], Deepak Goyal[b] & Jeffrey Thomas[b]
Deepak.x.goyal@intel.com
Biju.i.chandran@intel.com, Jeffrey.w.thomas@intel.com
Intel Corporation
a-CH5-157 / b-CH5-148
5000, W. Chandler Blvd.
Chandler, AZ

Abstract

Ball Grid Array (BGA) is currently the interconnect of choice for attaching microprocessors on a printed circuit board (PCB). The reliability of solder joints is one of the critical issues in BGA surface mount technology (SMT). During reliability testing, BGA fatigue failures were observed on test vehicles (TV). Finite element analysis and physical failure analysis were used to determine the risk to the product in the field. As part of this effort, parametric finite element analysis was carried out to determine the effect of design features like the package size, and BGA pattern on the propensity of fatigue failure. The results of the finite element analysis and physical failure analysis showed that the risk to fatigue failure was much greater on a peripheral / partial grid array package than in a full grid array package.

Introduction

Ball Grid Array (BGA) is currently the interconnect of choice for attaching microprocessors on a printed circuit board (PCB). The reliability of solder joints is one of the critical issues in BGA surface mount technology (SMT). Solder joint fatigue failure is one of the key modes of failure of surface mounted components subjected to thermal excursions in the field or during reliability testing. This is especially true of joints made of eutectic lead-tin solder, which are about 65% of their melting temperature, in the absolute scale, at room temperature. There are a number of factors that influence the fatigue life of an SMT part. In addition to the obvious contributions of the CTE mismatch between the constituent materials, and the temperature delta the package is subjected to, factors like BGA size, grid pattern, and package size greatly affect the reliability of the BGA solder joint. This paper studies the impact of parameters like: BGA size, pattern (full grid array vs. peripheral array), and die/package size, on the fatigue damage accumulation in a BGA solder joint during thermal cycling, using finite element analysis.

During temperature cycle (T/C) reliability stressing of test vehicles, complete cracks were found at the BGA to PCB interconnect on packages with peripheral array of the BGA joints. Physical analysis identified the solder ball cracking near the package lands to BGA joints resulting from solder fatigue. These experimental observations of BGA fatigue were used to validate the Finite Element model and to bench mark the model results to known failure. Mechanical modeling and physical analyses were found to be in good agreement explaining the crack location, propagation and crack lengths.

Based on this data, the effect of package design parameters on the propensity of BGA fatigue failure are predicted, and recommendations are made for future package designs. Furthermore, the identified maximum damage accumulation locations for different BGA patterns provides insight as to where to cross-section samples during future testing.

Four different test vehicles were studied -

Table 1: Test Vehicles studied.

TV1	Peripheral array BGA with 800x800 mils die on a 42.5x42.5 mm OLGA [17] package mounted on FR4 substrate.
TV2	Peripheral array BGA with 717x604 mils die on a 42.5x42.5 mm OLGA [17] package mounted on FR4 substrate.
TV3	Full grid array BGA with 400x400 mil die on a 32x32 mm OLGA [17] package mounted on FR4 substrate.
TV4	Full grid array BGA with 800x800 mils die on a 42.5x42.5 mm OLGA [17] package mounted on FR4 substrate.

Theory

Numerical technique.

Finite element analysis is typically used to understand the risk due to fatigue failure of a solder joint. Since low cycle fatigue is a strain related phenomenon, the inelastic strain (or the inelastic strain energy) build up in a solder joint is usually used to understand the risk of a solder joint to fatigue failure. Inelastic strain in a solder joint is the sum of the plastic strain and the creep strain in the joint. Eutectic lead tin solder is at 65% of its melting temperature at room temperature. Therefore creep is a dominant deformation mechanism in the range of operating (or test) temperatures of a typical electronic package. The inelastic strain (or the strain energy) is typically correlated to the number of expected cycles of life using the Coffin-Manson relation (or a derivative of this relation). Since solder joint fatigue failure is a critical failure mode affecting the reliability of electronic packages, there is a considerable amount of published literature describing different constitutive creep relations.

Solder joint creep:

Creep is the slow deformation of a material under a stress that results in a permanent change in shape. Generally creep pertains to rates of deformation less than about 1%/minute. Faster rates are typically associated with mechanical working

(like forging and rolling). Although creep can occur at any temperature, it is significant only at temperatures exceeding about one-half of the solder alloys absolute melting temperature. At lower temperatures, creep is characterized by an ever decreasing strain rate while at higher temperatures, creep deformation proceeds through three distinct stages. Figure 1 shows a schematic representation of creep in both temperature regimes.

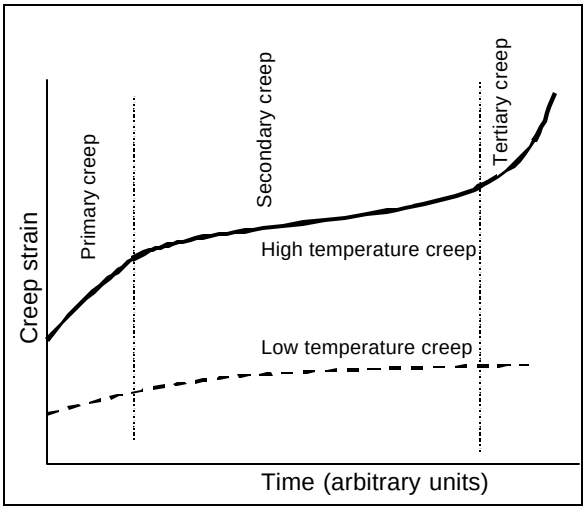

Figure 1: Schematic representation of high and low temperature creep.

When the material is loaded, there is an immediate (time independent) extension, which can be elastic or a combination of elastic and time independent plastic. This time independent extension is typically more at higher temperatures due to the lower modulus of the material. The material then deforms at a very rapid rate (primary creep), which decreases as time proceeds. This is observed due to work hardening of the material. At low temperatures, this behavior can occur indefinitely. At higher temperatures, when the rate of work hardening is balanced by thermally activated recovery processes, the rate of deformation becomes independent of time and strain (steady state). Although considerable deformation can occur under the steady state conditions, the material eventually enters the third stage of creep (tertiary creep), where the deformation proceeds at an ever increasing rate until the material can no longer support the applied stress and fracture occurs.

Creep deformation rate in a material at low to medium stress levels (1E-3 G) is usually described by the Wertmann-Dorn equation[1,2]:

$$\frac{d\tilde{a}_c}{dt} = \frac{(A_1 G b)}{k T}\left[\frac{b}{d}\right]^p \left[\frac{\hat{o}}{G}\right]^n D_0 \exp\left(\frac{-Q}{k T}\right) \qquad (1)$$

where, $d\tilde{a}_c/dt$ is the creep strain rate, G is the shear modulus, b is the burgers vector corresponding to a crystal dislocation, k is the Boltzmann constant, T is the absolute temperature, d is the grain size, τ is the applied shear stress, Do is the frequency factor, Q is the activation energy for the deformation process, $D_0 \exp\left(Q/k T\right)$ is the diffusion coefficient, and, p,n and A_1 are constants. It should be mentioned that eqn. (1) was originally proposed to describe steady state creep strain rate. However, since usually for eutectic Pb-Sn alloy the transient creep region comprises only a small fraction of the total creep strain in the temperature range of interest, one can consider eqn. (1) to apply for the total creep strain rate[3].

The mechanisms that control creep deformation in a solder material are termed dislocation and diffusion creep. Dislocation creep occurs due to the motion of crystal dislocations in response to an imposed stress, and is the predominant creep mechanism in solders at large stresses and high temperatures. Diffusion creep is characterized by the diffusion of vacancies in response to the applied stress. This creep mechanism is active in solders at high temperatures and low stresses. The grain size dependence of diffusion creep is characterized by the two variants of this creep mechanism – Nabarro Herring and Coble creep[2,4].

There are a number of variations of eqn. 1 which have been proposed in literature to describe the creep rate[5-9] of solder joints. Most of these relations use empirical constants obtained using tensile or shear testing of the solder material. The inelastic strain or the strain energy build up in the solder joint during one temperature cycle is then used to determine the fatigue life of the solder joint using variations of the Coffin-Manson relation. The Coffin-Manson relation describes the relation between the cyclic inelastic strain range and the low cycle fatigue life, much the same as the Basquin relation describes the relation between cyclic stress and high cycle fatigue life. The basic form of the Coffin-Manson relation is expressed as:

$$\frac{\Delta\tilde{a}_p}{2} = \tilde{a}_f' (2N_f)^c \qquad (2)$$

where,

$\Delta\tilde{a}_p/2$ = Plastic strain amplitude
$2N_f$ = Cycles to failure
ε'_f = Fatigue ductility coefficient
c = Fatigue ductility exponent

ε'_f and c are fatigue properties of the material. In reality, however, they are empirical constants. Typically, these empirical constants have different values depending upon the geometry and the loading history of the part being studied. Because of the empirical nature of these fatigue constants, there are a number of different forms of the fatigue life relation and related constants published in the literature. For example, Satoh et., al[10] describe a relation of the form $N_f = c(\Delta\varepsilon_p)^{-1.5}$ to describe the fatigue life of leaded solder joints, while Lau J.H., et al.,[11] use a relation of the form $N_f = 2.277E\text{-}3(\text{Max } \varepsilon_{eqv})^{-2.61}$ to describe the life of leaded solder joints, and a relation of the form $N_f = 3.013(\Delta\varepsilon_{total})^{-0.924}$ to describe the fatigue life of leadless solder joints. Hong, B.Z [12] uses a relation $N_f = 1.2928(\Delta\varepsilon_{eqv})^{-1.96}$ predict the fatigue life of ceramic BGAs. Daveaux R.[13] correlates the plastic strain energy density build up in a solder joint to the expected

life for crack initiation, and the crack propagation rate using the relations

$$N_{init} = C_1 \left(\Delta W_{ave}\right)^{C_2}, \text{ and } \frac{da}{dN} = C_3 \left(\Delta W_{ave}\right)^{C_4} \qquad (3)$$

The constants C_1 through C_4 were obtained by comparing numerically obtained plastic strain energy values to experimentally observed failure rates. Darveaux obtained values for C_1 between 13173 and 27258, C_2 between –1.39 and –1.45, C_3 between 1.72 and 3.92, and C_4 between 1.12 and 1.15, depending upon the element size at the interface. In all these cases, the constants were obtained by curve fitting experimental failure data of similar samples.

Because of the empirical nature of the published fatigue constants, and the strong dependence of the predicted life to these constants (power law relation ship), predicting absolute number of cycles to failure using these relations are highly error-prone. One way to circumvent this problem is to derive appropriate empirical constants from experimental failure data of similar solder joints. Another more feasible approach is to use solder joint of known failure history as a baseline case and predict the expected increase (or decrease) in life of one joint with respect to the base line solder joint. For example, if it is known that solder joint A starts failing at 1000 cycles of T/C X (-55 to 85 °C). The fatigue life of another joint B can be obtained by:

$$N_B = N_A \left[\frac{\Delta W_B}{\Delta W_A}\right]^{C_2} \qquad (4)$$

Typically, what is usually known is that solder joint A survives a 1000 cycles of T/C X without failure. Then equation 4 can be used to determine the risk to solder joint B to survive a 1000 cycles of T/C X.

It should be pointed out that eqn. (4) is used to determine crack initiation. In low cycle fatigue, the majority of the life of a joint is expended in crack propagation. Darveaux R. [13], and Lau. J. [11] have observed that only 10% of the life of a joint is spent in crack initiation, while the remaining 90% of its life is spent in propagating the crack. Therefore, using eqn. (4) alone to determine the useful fatigue life of a part is overly conservative. If enough information is available as to the failure history of the baseline case – solder joint A, then more realistic life predictions of solder joint B can be made. For example, if it is known that cross-sections of solder joint A have revealed small cracks after a 100 cycles of T/C X. And, after a 1000 cycles of T/C X, the crack length is about 50% of the diameter of the solder joint. Then, the expected lifetime of joint B to initiate a crack, and the number of cycles it would take for the crack to reach 50% of the solder diameter can be made.

Numerical analysis details

Three dimensional non-linear finite element models of a silicon die on an OLGA [17], substrate, BGA attached to an FR4 substrate, were created using the finite element code ANSYS™ 5.5. The solder material was modeled as a visco-plastic solid, the OLGA and the FR4 material as orthotropic solids, and all other materials as linear elastic materials. To simplify the model, the silicon die was assumed to be attached to the OLGA substrate using a homogeous material layer having equivalent properties as that of the c4 bumps and the underfill encapsulant. The assembly process induced (cool down from reflow) warpage of the die was compared to the measured warpage. A good match was obtained, thereby validating the model. It should be noted that the material properties used in this analysis have been calibrated and validated numerous times during previous studies. Therefore, a good match with measured values was obtained without having to adjust substrate stiffness parameters. The linear part of the material properties used in these analyses are given in Table 2.

Table 2: Material properties used in the analyses.

Material	E (Gpa)		CTE ppm	Poisson's ratio / G
Silicon	130		3.2	0.3
FR4	In-plane	10.47	12.2	G = 6.87
	Out-of-plane	3.08	55.4	G = 2.39
OLGA	In-plane	17	16	G = 5
	Out-of-plane	7.8	51	G = 2.29
Die attach	6.2		28	0.3
Solder	Temp			
	-30°C	39	23.3	0.31
	-13°C	36		0.32
	22°C	30		0.35
	45°C	24		0.36
	100°C	18.2		0.40
	125°C	15.2		0.41

ANSYS™ has viscoplastic (rate dependent plasticity) elements following Anand's constitutive law [14] as a standard option. The primary features of the Anand's rate dependent constitutive law are that there are no explicit yield conditions. Yielding is supposed to occur at all non-zero values of stress. Although at low stress, the rate of plastic flow is immeasurably small. Anand's law is broken down into a flow equation,

$$\frac{d\varepsilon_p}{dt} = A\left[\sinh\left(\xi \frac{\sigma}{s}\right)\right]^{1/m} \exp\left(\frac{-Q}{kT}\right) \qquad (5)$$

and three evolution equations which describe the strain hardening or strain softening of the material.

$$\frac{ds}{dt} = \left[h_0 \left|B\right|\right]^a \frac{B}{\left|B\right|} \frac{d\varepsilon_p}{dt}$$

$$B = 1 - \frac{s}{s^*} \qquad (6)$$

$$s^* = \hat{s}\left\{\frac{d\varepsilon_p / dt}{A} \exp\left(\frac{-Q}{kT}\right)\right\}^n$$

Here,

$\frac{d\varepsilon_p}{dt}$	=	effective inelastic deformation rate
σ	=	effective cauchy stress
h_o	=	hardening constant
s	=	deformation resistance
s^*	=	Saturation value of s
$\hat{s}$	=	time derivative of s.

T	=	absolute temperature
m	=	strain rate sensitivity to stress
a	=	strain rate sensitivity to hardening

The inelastic strain in Anand's definition of the material is temperature and stress dependent as well as dependent on the rate of loading. Determination of these material parameters is typically done by curve fitting a series of stress-strain data at various temperature and strain rates as in Anand [14] or Brown et. al. [15].

Darveaux [13] had found earlier that Anand's viscoplasticity can be used suitably to describe solder materials and determined approximate values of constants to be used. These same parameter values were used in this work and are given in Table 3.

Table 3: Parameters describing the Anand's law of eutectic Pb-Sn solder.

Parameter	Value
s (psi)	1800
Q/k (1/K)	9400
A (1/sec)	4.0E6
ξ	1.5
h_0 (psi)	2.0E5
m	0.303
s^ (psi)	2.0E3
n	0.07
a	1.3

The goal of the simulations was to calculate the plastic work per unit volume of the solder material (or the viscoplastic strain energy density) accumulated per temperature cycle. The plastic work build up in the solder joint for different cases is then compared.

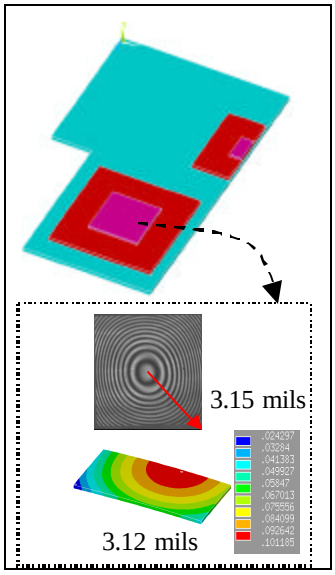

Figure 2 : Finite element model of a test vehicle with peripheral array OLGA SMT mounted on a substrate using BGA joints (similar to TV1 and TV2).

Figure 2 shows a 3D finite element model of a test vehicle with peripheral grid array OLGA mounted on a FR4 substrate. Since the area of interest in this package was the BGA bumps under the Peripheral array OLGA, non-linear properties were assigned to only those solder bumps. The assembly was subjected to a load step that simulated the cool-down of the assembly from bonding temperature, and the response of the assembly was noted. The inset in Figure 2 compares the model predicted warpage of the die surface to the die warpage that was measured using Fizeau interferometry. Note that the predicted value matches the measured value well. Figure 3 shows the inelastic strain energy build up in the BGA joints under the peripheral array OLGA package after the load step.

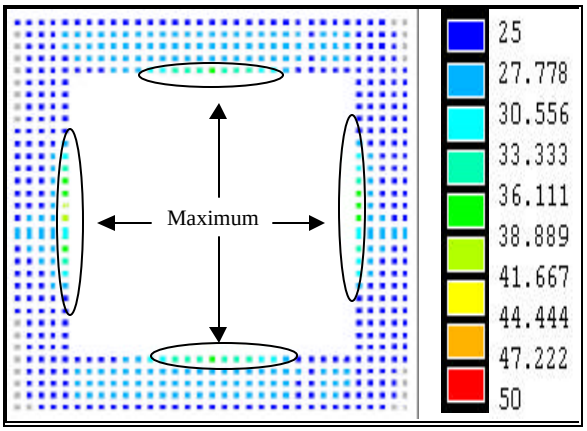

Figure 3: Inelastic strain energy density in the peripheral array OLGA SMT mounted on FR4 substrate, induced due to the assembly process.

As can be seen in Figure 3, the maximum damage accumulation occurs on the inner-most row of BGAs near the center of the die. In this model the BGAs were modeled coarsely (as cubes) to limit the size of the model. In-order to improve predictability and identify failure initiation sites, the resolution of the solder bumps needed to be improved. Due to the large size of the model, the resolution of the solder bumps could not be increased further in this model.

A "slice" model (one BGA wide) of a large die peripheral array package on a FR4 substrate was therefore created to save on computation time. Figure 4 shows a finite element model of the slice model.

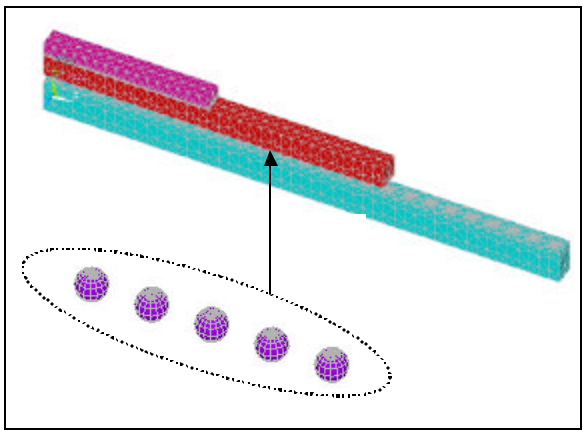

Figure 4: High resolution finite element model of a strip of the assembly.

To ensure that the required accuracy of the model was maintained after this simplification, this model was subjected to the assembly process loading step, and the model calibrated by comparing the predicted and measured values of the die warpage and in-plane deformation of the innermost BGA. Figure 6 shows an in-plane moire image of the inner most BGA under the peripheral package in the test vehicle. A good correlation to the measured data was achieved after increasing the modulus of the substrate materials about 15%. Initially, the strip model over predicted the die warpage because of the decrease in stiffness of the assembly in the case of the strip model, as compared to the full 3D case. Although this over prediction of warpage will not affect the results (since they are derived by comparison of two cases), the modulus of the substrates was increased to match the measured warpage.

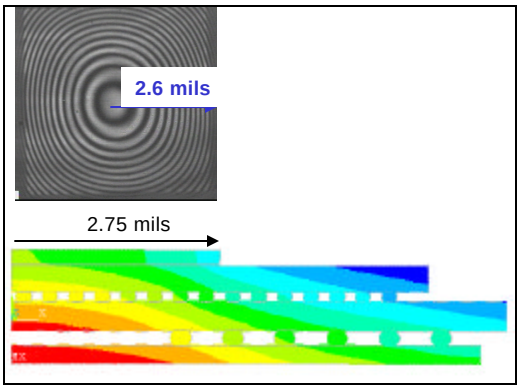

Figure 5: Comparison of predicted and measured warpage due to reflow, on the die surface.

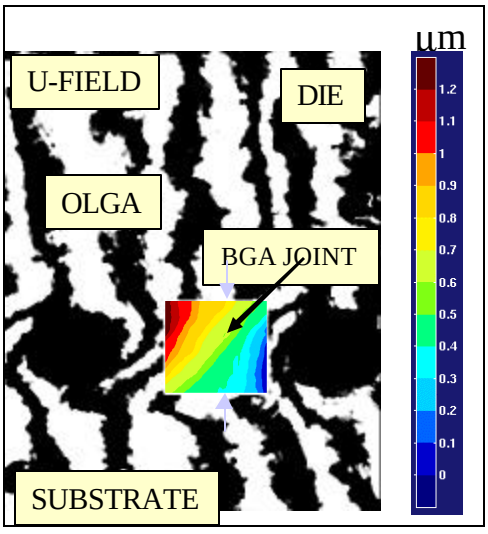

Figure 6: In-plane moire image of the inner most BGA under the peripheral array OLGA package.

Due to the symmetry of the assembly, only half of the structure was modeled. Since the state of stress and strain in the solder joints are of most interest in this study, the BGA joints are meshed with well-shaped hexahedral elements, while all the other materials are meshed rather coarsely with tetrahedral elements. All parametric studies were performed using the strip model.

The thermal loading subjected to the assembly was cool-down from reflow and one cycle of T/C X. The time taken to cool-down the assembly from solder melting temperature was chosen arbitrarily as 2 minutes. Previously measured temperature profile on the package mounted on a FR4 substrate assembly during T/C X (shown in Figure 7) was used to simulate the temperature cycle load step. One load step was used to simulate the assembly process step, and five load steps were used to simulate one cycle of T/C X.

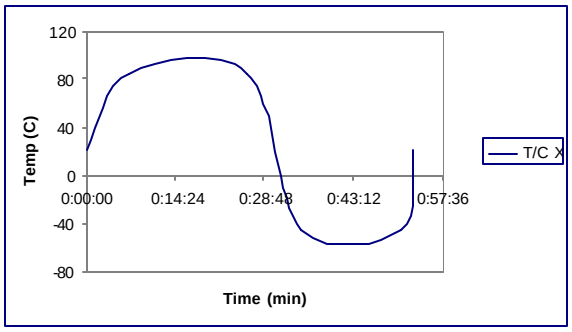

Figure 7: One cycle of T/C X - Measured on the package mounted on a FR4 substrate (TV1)

Results & Discussions

Figure 8 shows the plastic work accumulated in the BGA solder joints at the end of the loading cycle.

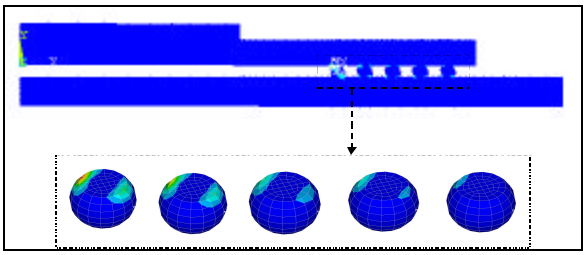

Figure 8: Plastic work build up in the BGA solder elements after all the complete loading cycle.

Inelastic energy is built up in the solder material only, since all the other materials were assumed to be linear elastic. Note that the maximum strain energy is accumulated in the solder joint closest to the die edge. The maximum value is at the solder/OLGA interface closest to the die edge.

Figure 9 shows the increase in strain energy in the worst case element during the load step. As can be seen in Figure 9, inelastic energy is built up in the solder joint during the assembly process step, which increases during the temperature cycle. Recall that Anand's constitutive law does not have a distinct yield point and that the inelastic stain depends on the rate of loading, stress, and the temperature. It is seen that there is an increase in strain energy during ramps and during the low temperature soak. The increase in strain energy during the ramps, are likely due to the dependence of Anand's constitutive law on the load rate. And, the increase in strain energy at low temperature soak is because of the high stress in the solder joint at low temperatures. It is seen that the strain energy increases only at a very small rate during high temperature hold. This is probably due to the fact that, even though higher temperatures are more favorable

for creep mechanisms to be active (and therefore, increase inelastic strain energy), the stress in the joints is very low, causing the inelastic energy to increase at a very small rate.

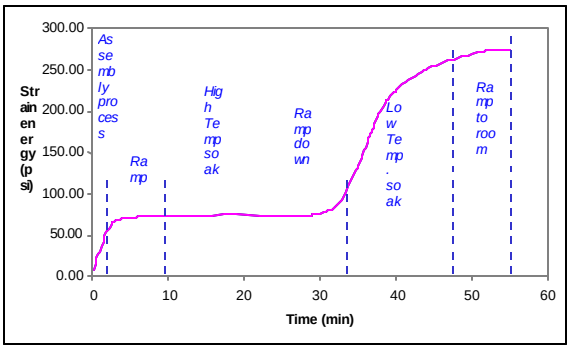

Figure 9: Increasing strain energy during the load cycle.

To understand the dependence of the mesh size on the predicted strain energy values, the element size at the interface of the worst case solder ball (the closest to the die) was progressively refined, and the analysis rerun. Figure 10 shows the peak strain energy density at the interface for four different cases. The element size at the interface in each case was half the size of the previous case. That is the element size at the solder/OLGA interface in 'Case D' is half that of "Case C', one-fourth that of 'Case B' and one-eighth that of 'Case A'.

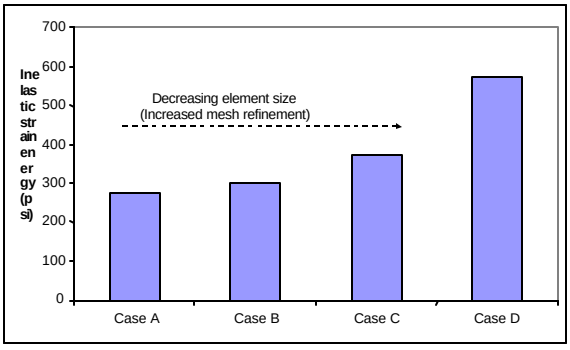

Figure 10: Increasing strain energy at interface as mesh density is refined - singularity.

It is seen from Figure 10 that the calculated strain energy density continues to increase as the element size decreases. That is, there are singularities at the edges of the joint. Since the strain energy values do not converge as the mesh is refined, the absolute value of the strain energy is meaningless. A fracture mechanics approach, where a crack is modeled into the joint, and the j-integral around the crack tip [16] is calculated, is sometimes employed to circumvent this problem. A less elegant but simpler method sometimes employed is to keep the element size consistent from model to model, and derive conclusions not from the absolute value of the strain energy density predicted, but by comparisons between different cases.

As is evident from Figure 8 and Figure 3, the maximum damage accumulation occurs in BGAs closest to the die in the case of a peripheral array package mounted to an FR4 substrate. That is, fatigue failure would first occur on BGAs in the inner most row close to the center of the die. Also, according to the model, the site of first failure initiation would be the OLGA/solder interface closest to the die, as shown in Figure 11. Figure 12 shows a scanning electron micrograph (SEM) of a BGA solder fatigue crack after 1000 cycles of T/C X on a peripheral array package, the centermost joint of the innermost BGA row. It is clear that the severity of cracking was maximum in this joint. This is in full agreement with the results presented in Figure 3. The crack extended through the BGA joint. Figure 13 plots the observed fatigue failure locations on the peripheral array package on an FR4 substrate. The data points indicate the percentage of the solder diameter that was cracked, for each solder ball, on the inner most row of four packages.

As is evident from Figure 13, the location of observed failure matched well with what was concluded from the model. Failure analysis results presented in Figures 11 and 12 show that the failure initiation site in a BGA was at the solder ball to OLGA land matching the location predicted by the model.

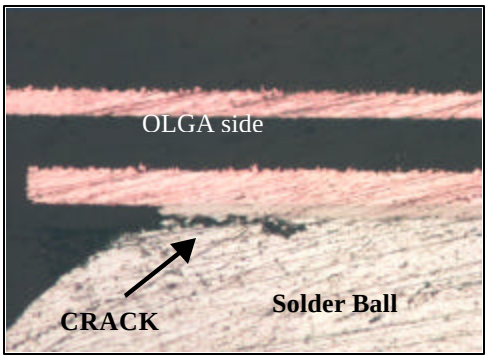

Figure 11: Cross-section optical micrograph of solder fatigue crack after 1000 cycles of T/C X on peripheral array BGA package from TV1. Note that the cracking first initiated near the joint side close to the die edge in complete agreement with the modeling results.

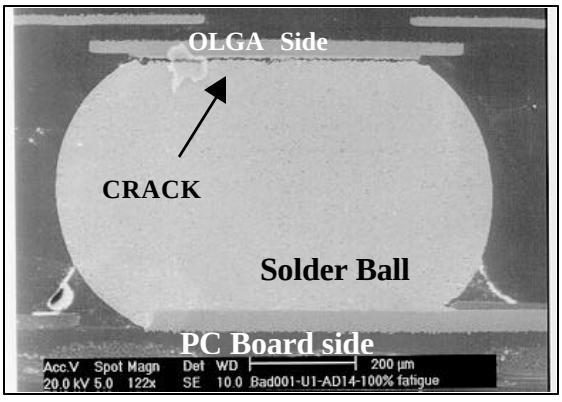

Figure 12: Cross-section scanning electron micrograph of a solder fatigue crack after 1000 cycles of T/C X on a peripheral array package mounted on a FR4 substrate test vehicle 1 (TV1). The crack extended throughout the BGA joint diameter. This particular BGA joint was the centermost joint in the innermost row of the BGAs.

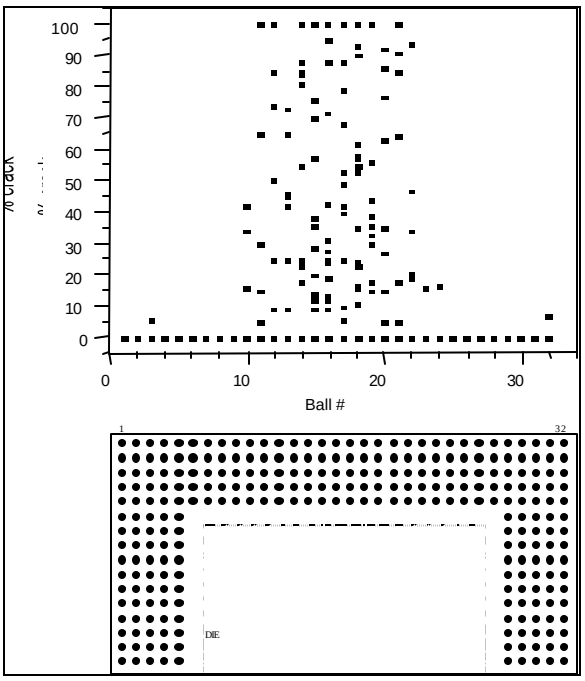

Figure 13: Observed failure pattern on TV1 (a peripheral array package with large die on a substrate) after 500 cycles of T/C X.

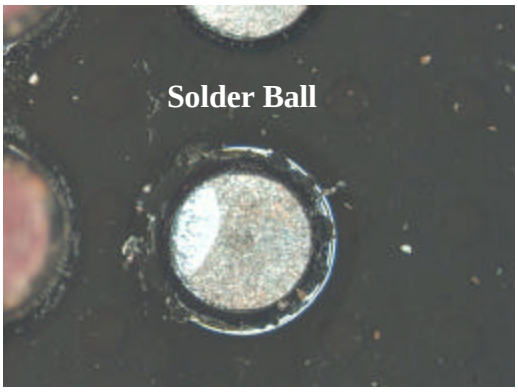

Figure 14: Optical micrograph of solder fatigue crack after 1000 cycles of T/C X on peripheral array package (TV1). This micrograph was obtained after mechanically removing the OLGA package from the PC board. The gray region on the lands shows the extent of solder fatigue cracking.

During failure analysis a novel technique of mechanically removing the OLGA in order to map the solder fatigue cracking near the OLGA/solder ball interface was developed. Figures 14 and 15 show optical micrographs of the extent of solder fatigue cracking after mechanical removal of the OLGA package from the PC board. These figures show the cracking near the OLGA / solder interface on the joint that had solder fatigue cracking. During the mechanical removal the solder joints that had fatigue cracks were found to fail at the OLGA land to solder ball interface similar to the joint shown in Figure 14. On this fracture surface the darker region was found to correspond to the pre-existing crack while the brighter region was due to extension of the crack during mechanical removal. Figure 15 shows an array of BGA joints extending from the edge of the die on OLGA to the center of the die (left to right). The inner most row and the center most BGA joint shows the maximum cracking (similar to Figure 14). The extent of cracking was found to decrease from the centermost ball to the edge (right hand side to the left hand side in the Figure). This observation is also in complete agreement with the mechanical modeling.

To understand the risk to the peripheral array package during power cycling stress, the model was subjected to load cases simulating the temperature swings seen by the package during power cycling. Temperature measurements at different regions of the test vehicle provided information as to the temperatures seen by the peripheral array package during power cycling (seen in Figure 16). As seen from Figure 16, the temperature extremes experienced by the package and the cycle time, for power cycling is significantly less than that in temperature cycle X. Packages of different form factors (TV1, TV2, TV3 and TV4) were also modeled using the same basic assumptions and subjected to the T/C X load, to understand the risk from this failure mode, and to better understand the phenomenon which causes this failure. Figure 17 plots the strain energy build up in the worst case solder joint for each of the different cases.

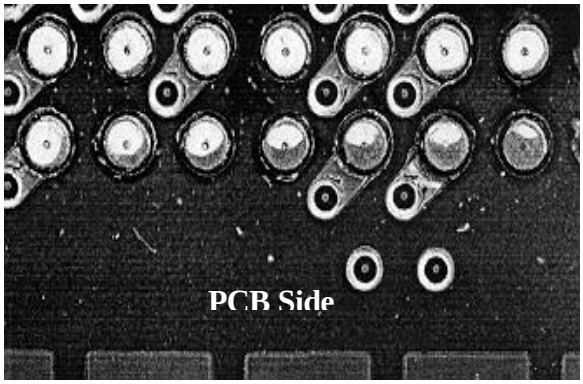

Figure 15 Optical micrograph of solder fatigue crack on an array of BGA joints after 1000 cycles of T/C X on a peripheral array package (TV1). This micrograph was obtained after mechanically removing the OLGA package from the PC board and demonstrates the extent of solder joint cracking with respect to the BGA joint position on the board.

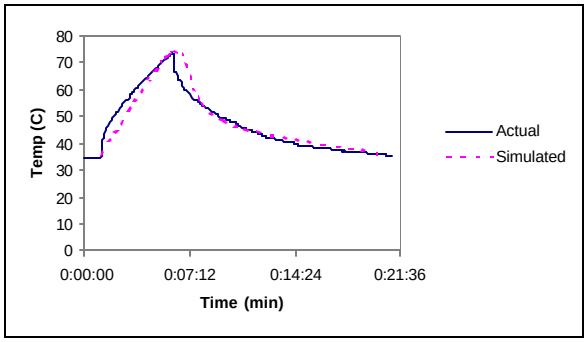

Figure 16: Temperature of the peripheral array package during power cycling (P/C) stress.

As can be seen in Figure 17, the strain energy build up in the peripheral array package solder joint is significantly lower after one power cycle as compared to one cycle of T/C X. This is due to the smaller temperature swing and the shorter duration of a power cycle as compared to a cycle of T/C X. Using equation 4 (and its counterpart for crack propagation), the acceleration factors between temperature cycle X and power cycling, for BGA fatigue failure of the peripheral array package mounted on the test vehicle substrate were determined to be:

$$\left|N_{P/C}\right|_{Initiation} = (11 \text{ to } 12) * \left|N_{T/C\ X}\right|_{Initiation}$$

$$\left(\frac{da}{dN}\right)_{P/C} = (\approx 0.13) * \left(\frac{da}{dN}\right)_{T/C\ X}$$

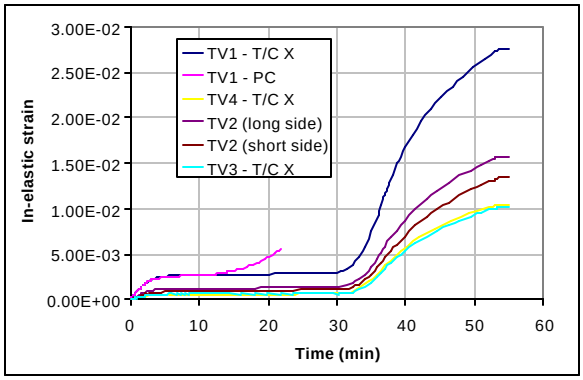

Figure 17: Strain energy density build in the worst case BGA for different cases to understand the effect of die size and peripheral vs. full array BGA joints. Strain energy build-ups after T/C X and P/C stresses are also compared.

This indicates that crack initiation would occur in power cycling only after about 11X the number of cycles as that in temp cycle X. Also, the rate of crack propagation in power cycling would be significantly lower than that in temp cycle X. Cross-sections of units after 2500 cycles of power cycling did not reveal any cracks.

Comparison of TV1 and TV2 revealed the effect of die size on peripheral array BGA solder fatigue. The two curves in Figure 17 represent the strain energy accumulation in inner row BGAs under the long axis and the short axis of the die on peripheral array BGA in test vehicle 2. As seen in the figure, the damage accumulation for the case of test vehicle 2 is lower than that in the case of test vehicle 1 for the same loading condition. This is due to the smaller size of the die. Computing acceleration factors like before, the acceleration factor between the test vehicle 1 and the test vehicle 2 are seen to be:

$$\left|N_{TV2}\right|_{Initiation} = (2.5 \text{ to } 3.5) * \left|N_{TV1}\right|_{Initiation}$$

$$\left(\frac{da}{dN}\right)_{TV2} = (\approx 0.37) * \left(\frac{da}{dN}\right)_{TV1}$$

Figure 18 compares the observed crack lengths for the test vehicle 1 and test vehicle 2 after 500 cycles of T/C X. As can be seen in the figure, the crack lengths in the test vehicle 2 with smaller die are significantly smaller than that in the test vehicle 1 with larger die.

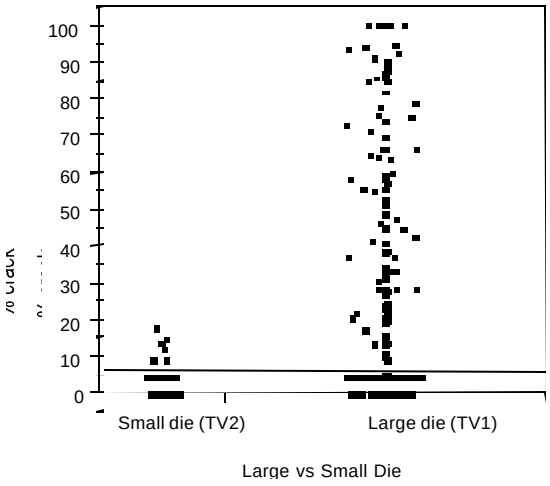

Figure 18: Variation of fatigue crack lengths between large (test vehicle 1) and small (test vehicle 2) die mounted on the FR4 substrate after 500 T/C X.

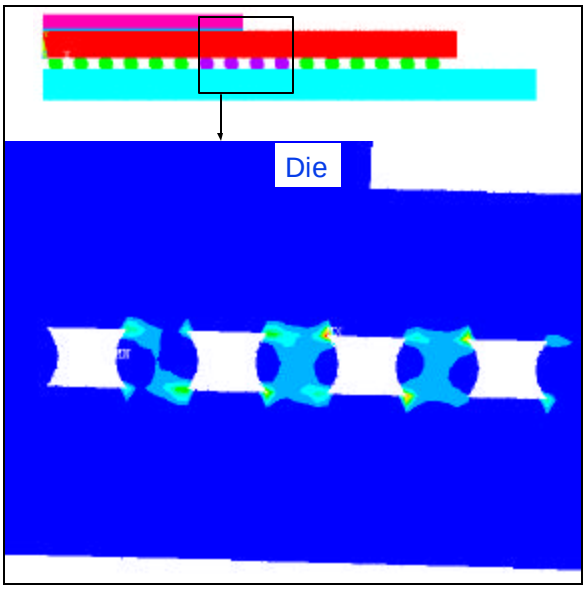

Figure 19: Accumulated strain energy density on the BGA's under a full grid array package.

To understand the impact of the BGA pattern on the level of fatigue failure, the model with test vehicle 1 was modified to include a full grid array and analyzed. A model of a test vehicle 3 package which is smaller in size than the die on the test vehicle 1 package (800x800 mils die on a 42.5x42.5 mm OLGA), but similar in BGA layout was also created and analyzed for comparison. Figure 13 includes curves for these cases also. As can be seen, covering the entire OLGA package with BGA bumps decreases the damage accumulation in the solder joint significantly. Figure 19 shows the location of maximum inelastic strain energy accumulation for the test vehicle 1 package with a full grid array. As can be seen in figure 19, the location of maximum

damage accumulation are the BGAs under the edge of the die (die shadow BGAs).

Experimental confirmation of the decrease in fatigue failure in full grid array packages comes from temperature cycle results of Test Vehicle 4 packages (similar in size to test vehicle 1, but having a full grid array BGA pattern).

Conclusions

The peripheral grid array packages can be highly susceptible to fatigue failure during temperature cycling on the innermost row of the solder balls. The variables affecting the solder fatigue life of the peripheral array packages are the die size and temperature cycle conditions (temperature and time). It has been demonstrated that the risk of solder fatigue cracking is low in the field use conditions. It was further demonstrated that populating an OLGA package with a full grid array of bumps increases the reliability of the packages during temperature cycling. A novel technique of mechanical removal of OLGA in order to understand the extent of solder joint cracking was developed. The physical failure analysis observations were found to be in good agreement with the mechanical modeling results. The above results also suggest that mechanical modeling and pro-active physical failure analysis must be performed to clearly understand the reliability risk of peripheral array packages for any future packaging needs.

Acknowledgments

The authors would like to acknowledge the contributions of Tony Chan, Mike Mello, Joel Mortimer, Shalabh Tandon and Mike Lombardi.

References

1. Lagneborg R., "Creep: Mechanisms and Theories", Creep and Fatigue in High Temperature Alloys, Ed. Bressers J., Applied Science Publishers Ltd., London, 1981.
2. Evans R.W., and Wilshire B., Creep of Metals and Alloys, The Institute of Metals, London, 1985.
3. Hacke, P.L, Sprecher, A.F., and Conrad, H., "Microstructure coarsening during thermo-mechanical fatigue of pb-sn solder joints", *Journal of Electronic Materials*, V.26, N.7, 1997, pp. 774-782.
4. Lupinc V., "Creep: Introduction and Phenomenology", Creep and Fatigue in High Temperature Alloys, Ed. Bressers J., Applied Science Publishers Ltd., London, 1981.
5. Knecht, S. et. Al., "Constitutive relation and creep-fatigue life model of eutectic tin-lead solder", *IEEE Transactions on Conponents, Hybrids, and Manufacturing Technology*, V13., N2, June 1990.
6. Solomon et. Al., "Energy Approach to the fatigue 0f 60/40 solder part II – Influence of hold time and assymetric loading", *ASME International Mechanical Engineering Conference and Exposition*., San Fransisco, CA., Nov12-17, 1995.
7. Darveaux R., et al., "Constitutive Relations for Tin based Solder Joints", *Proceedings of the 42nd ECTC conference*, 1992
8. Pao Y-H., et. al., "Thermomechanical and Fatigue Behavior of High Temperature Lead and Lead-free Solder Joints", *J. of Electronic Packaging*, 1995.
9. Iannuzzelli, R.J., et. al., "Solder Joint Reliability Prediction by the Integrated Matrix Creep Method", *J. of Electronic Packaging*, June 1996.
10. Satoh R., et al., "Thermal Fatigue Life of Pb-Sn Alloy Interconnections", *IEEE Trans on CHMT*, Vol 14., N1, March 1991, pp. 224-232.
11. Lau J.H., and Pao, Y.H., Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, McGraw-Hill, 1997.
12. Hong, B.Z., "Finite element Modeling of Thermal Fatigue and Damage of Joints in a Ceramic Ball Grid Array Package", *J. of Electronic Materials*, V26, N7, pp. 814-820, 1997.
13. Darveaux R., et al., "Reliability of Plastic Ball Grid Array Assembly", Ball Grid Array Technology, Ed. J. Lau., Mc-Graw Hill, New York, 1995.
14. Anand, L., "Constitutive Equations for Hot-Working of Metals", *International Journal of Plasticity*, Vol 1., pp.213-231, 1985
15. Brown, S.B., et al., "An Internal Variable Constitutive Model for Hot Working of Metals", *International Journal of Plasticity*, Vol 5. Pp.95-130, 1989.
16. Meyers, M.A., and Chawla, K.K., Mechanical Metallurgy, Principles and Applications, Prentice-Hall, London, 1984.
17. Shukla, R., Murali, V., Bhansali, A., Flip Chip CPU Package Technology @ Intel: a Technology and Manufacturing Overview, *Proceedings of 49th Electronic Components and Technology Conference*, May 1999, Vol. 49, P.945.