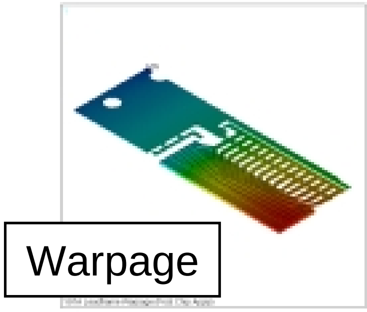
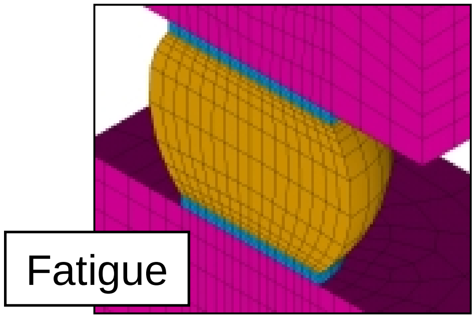




Semiconductor Package Simulations: Assembly, Test, & Reliability

February 16, 2001

Steven Groothuis
Micron Technology, Inc.
Assembly Department

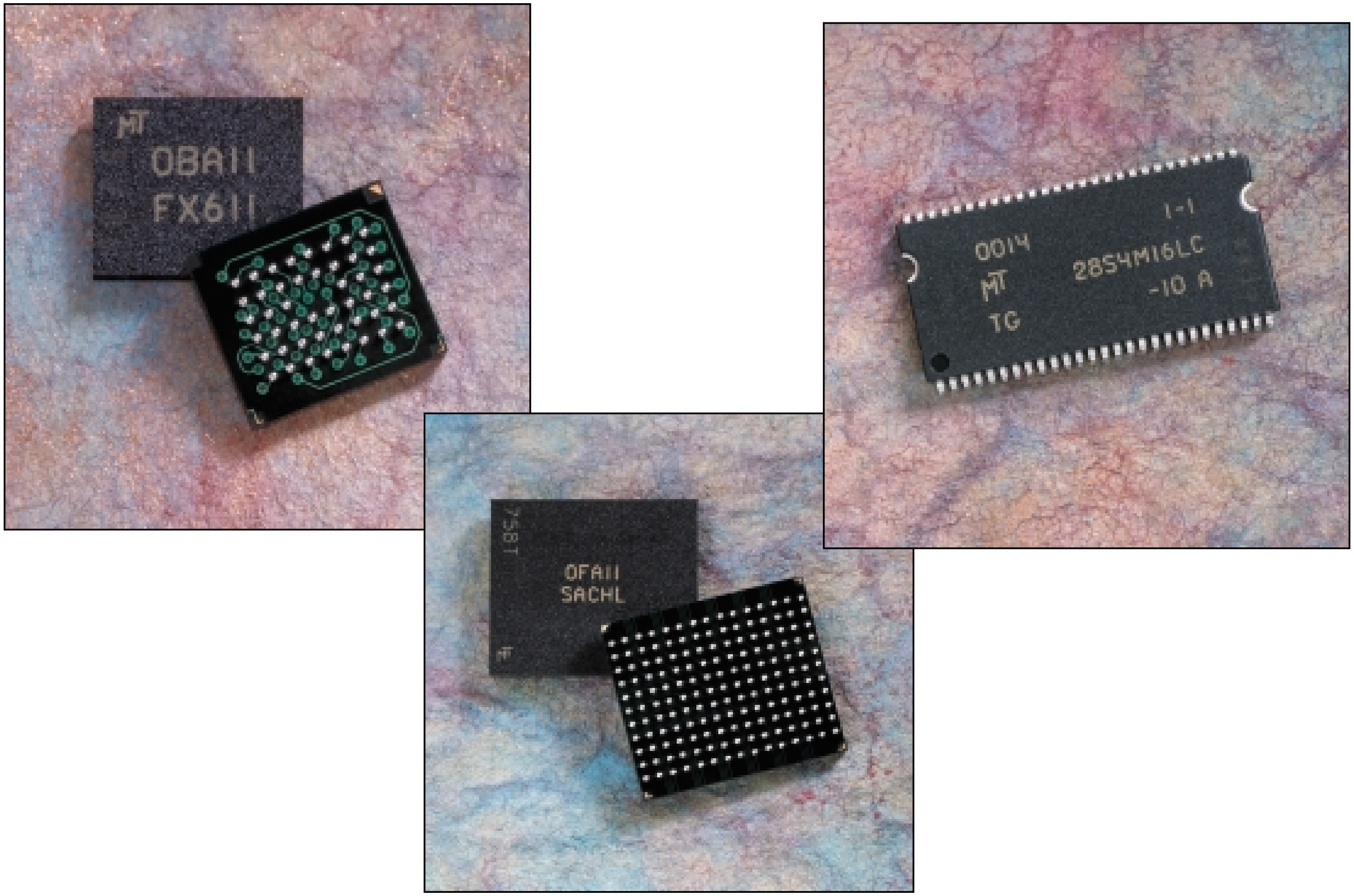
Outline

- Background
- ANSYS/Mechanical
  - Semiconductor package stresses (Linear)
  - Solder joint fatigue & reliability (Nonlinear)
- ANSYS/Thermal
  - Thermal resistance modeling (Steady-State)
  - Assembly equipment & processes (Transient)
- ANSYS/LS-DYNA
  - Assembly process simulations (Impact Modeling)
- Conclusions

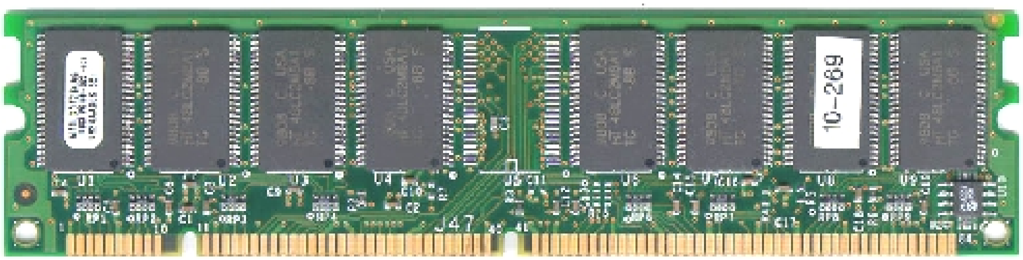
Background

- Packaging and assembly of semiconductor devices involves most areas of mechanics and physics.
- Performance and reliability are essential for market acceptance.
- Standard test and simulation methods are developing for thermal performance through JEDEC (Joint Electron Device Engrg. Council)
- SEMI and ASTM standards are available for mechanical characterization.

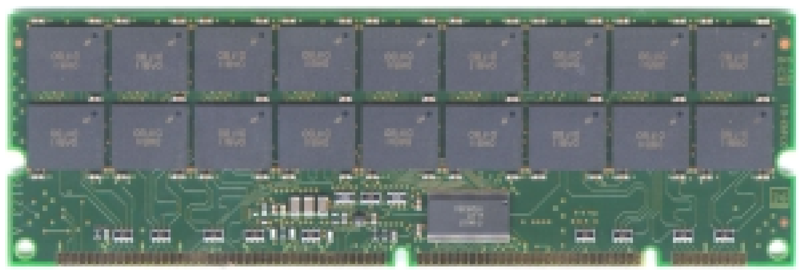
Package Configurations



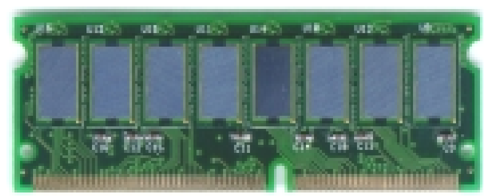
Module Package Technology



TSOP on DIMM



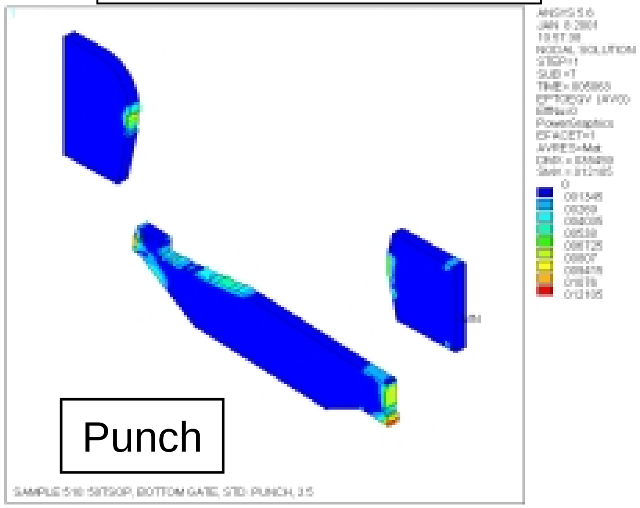
FBGA on SODIMM

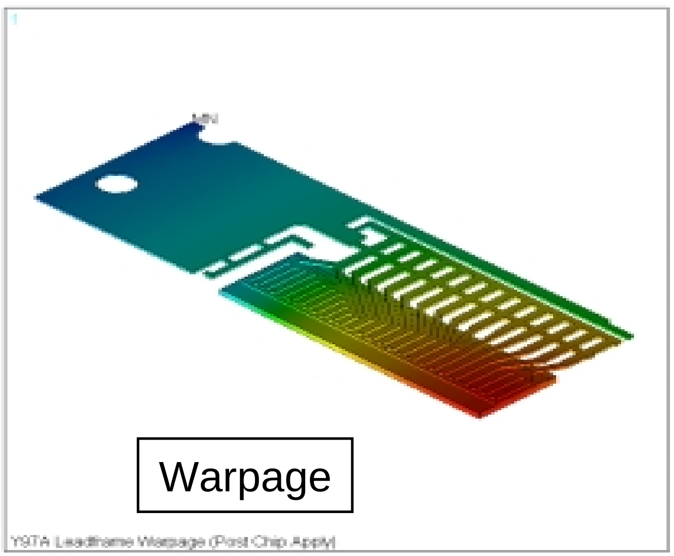


Flip Chip on Module

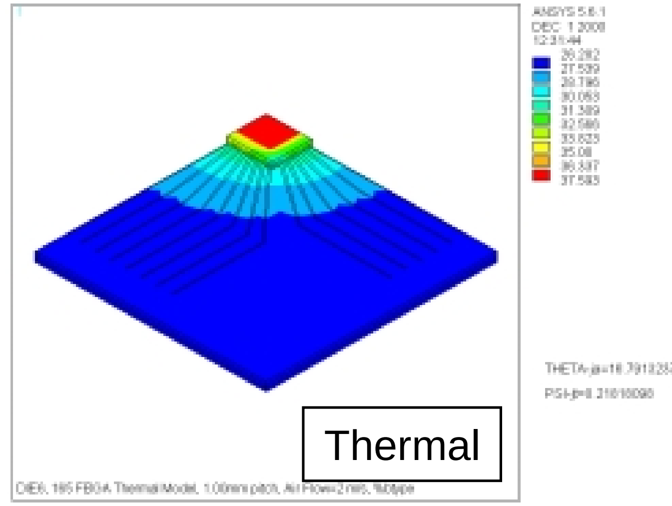
Micron Technology, Inc.

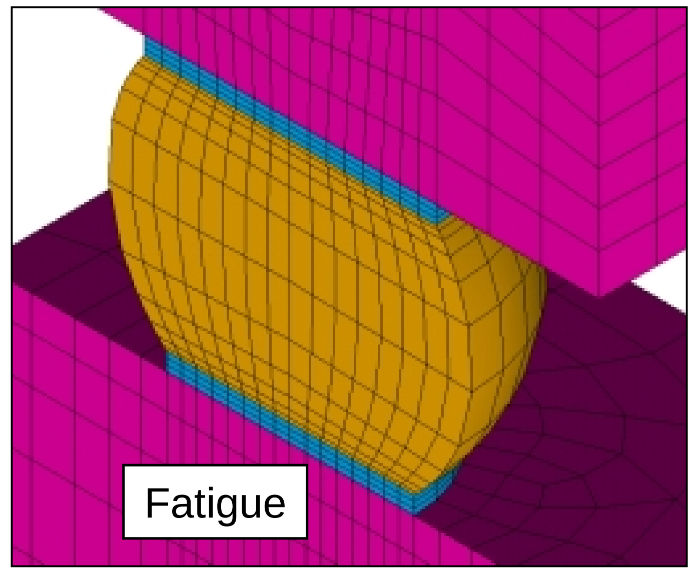
Process Simulation





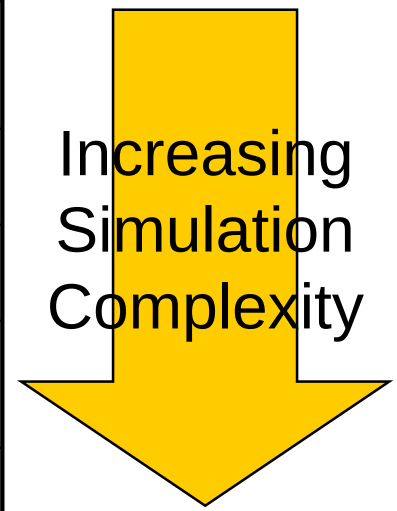
Performance Simulation





Packaging Material Theory

TOPIC	METROLOGY	MATERIAL PROPERTIES	MODELING	FAILURE CRITERIA
Bulk Stress	Strain Gauge Test Structures Moiré Interferometry	Modulus, Coef. Thermal Expansion, Poisson’s Ratio (T)	Thermoelasticity (stress & strain)	Strength of Materials (UTS or elongation at break)
Fatigue	Measure S-N Curves (crack growth - da/dN)	Ductility Factors, Viscoplasticity, & Creep parameters	Material Nonlinearities	Modified Coffin-Manson equation
Moisture Effects	Measure moisture distribution and kinetics	Diffusion & Solubility Coef. (%RH, T)	Model moisture diffusion	Hydrostatic pressure and hydrolysis effect
Residual Stress	Residual stress measurements (warpage)	Relaxation Modulus (t,T)	Viscoelasticity	Available for superposition with other calculated stresses
Adhesion	Measurement of interfacial fracture energy	Energy factors - G_c & γ_c	Fundamental models	$G_{I, II}$ vs. G_c
Scaling Effects	Mechanical testing of film specimens (in-situ techniques)	Material properties (e.g., modulus as function of size)	Micromechanical effects	To be defined

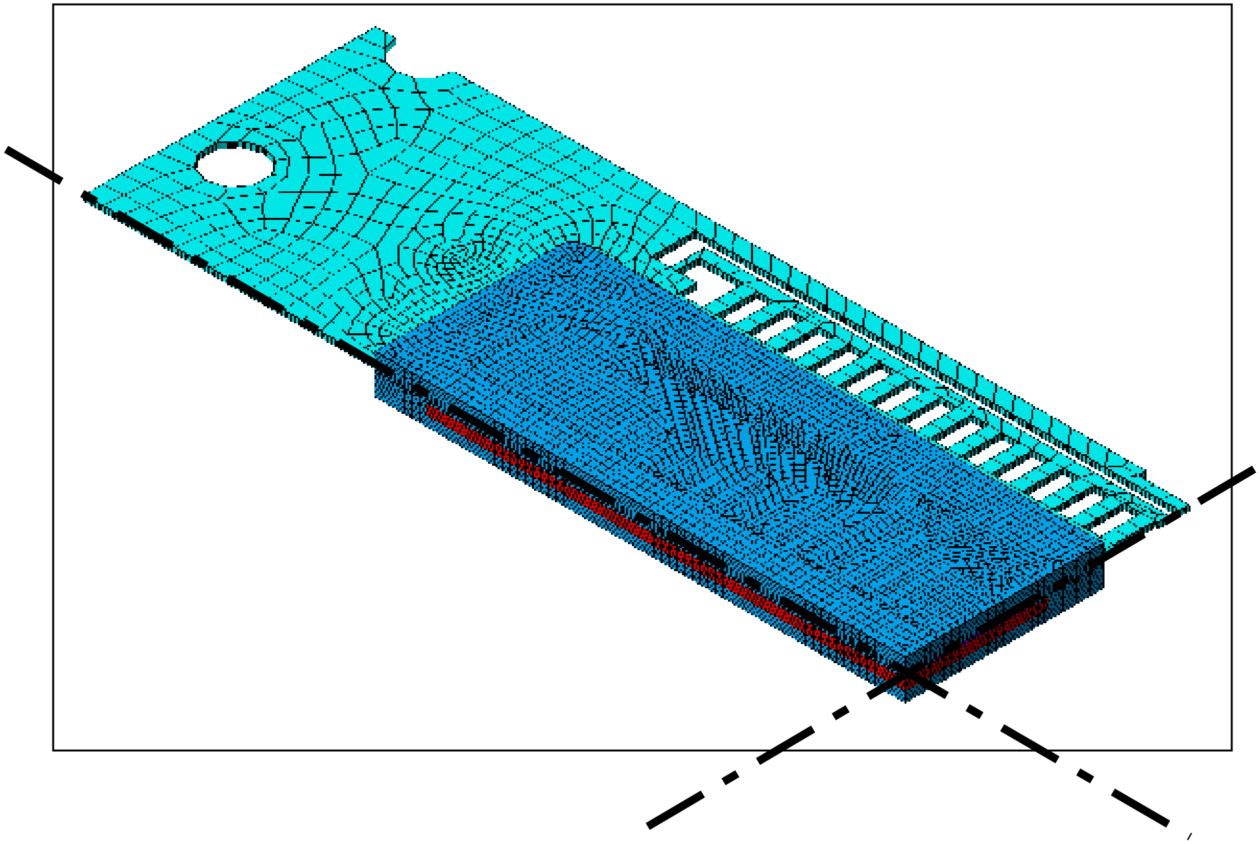


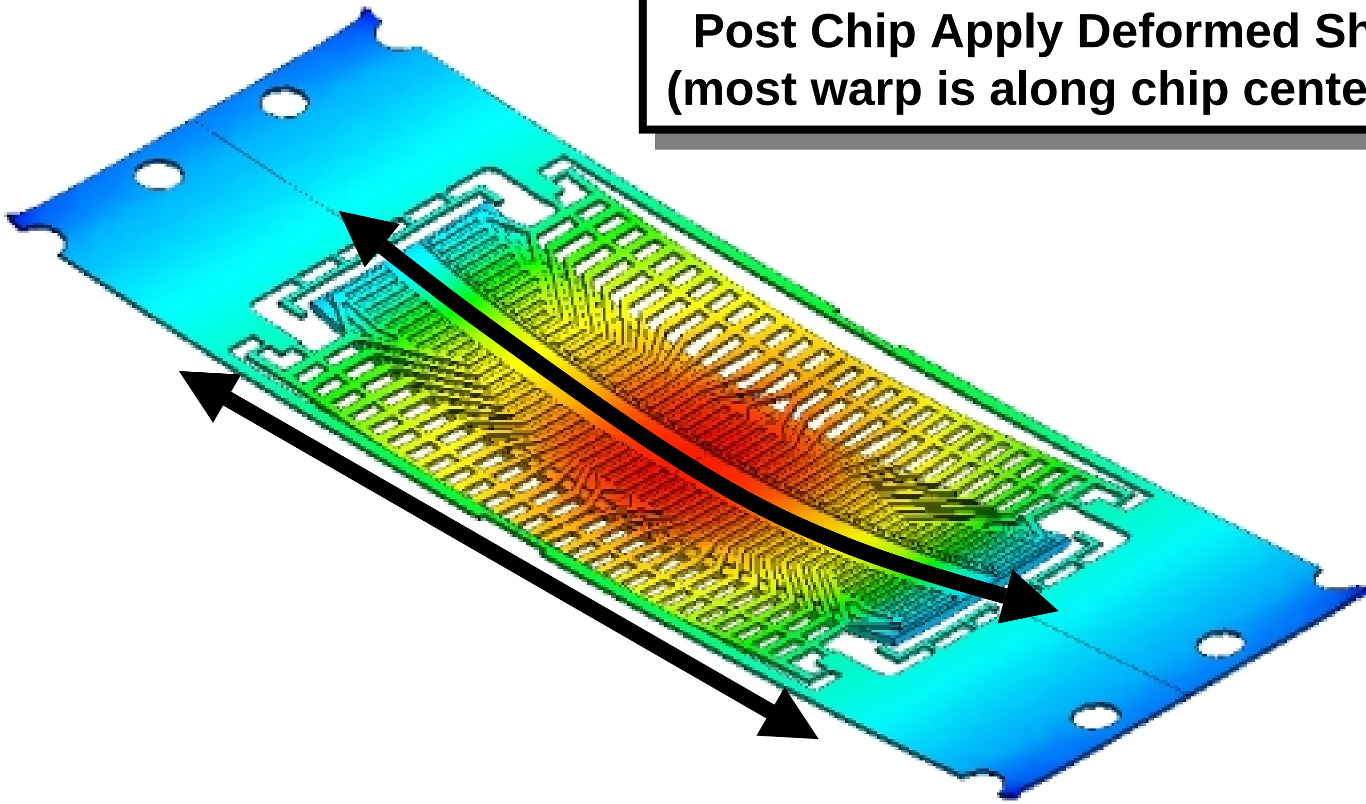
Mechanical Simulation

Temperature-Dependent Stress

Nonlinear Solder Fatigue & Reliability

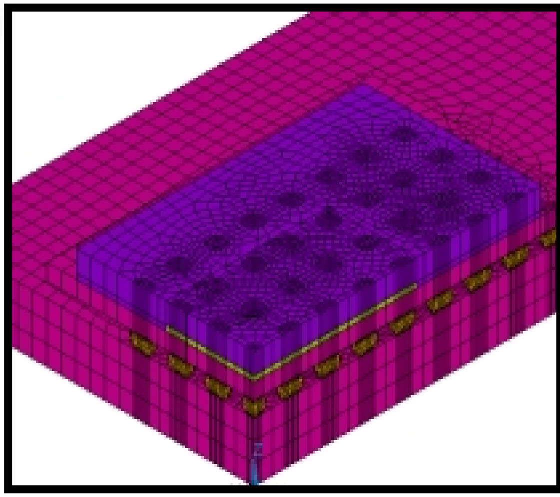
Thermomechanical Stress Model

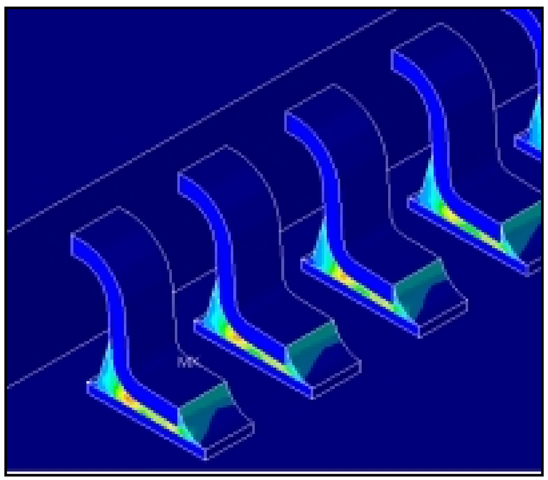




Post Chip Apply Deformed Shape (most warp is along chip centerline)

Solder Joint Reliability





Package Definition

Model Generation
[/PREP7]

Full-model Process | Submodel Process
[CBDOF]

Thermomechanical Solution
[/SOLUTION]

Anand Viscoplasticity
[TB,ANAND]

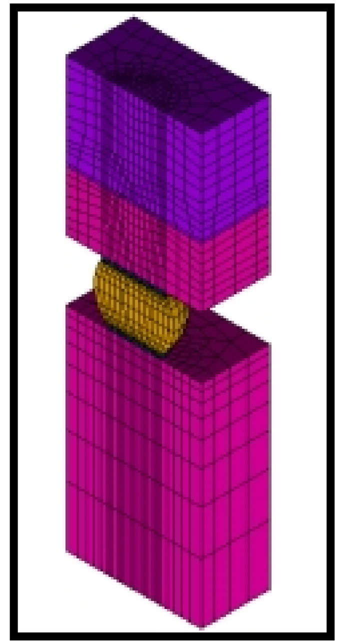
Nonlinear Plasticity
[TB,MISO]

Post-processing
[/POST1]

Plastic Work Density
[PLNS,NL,PLWK]

Total Strain Energy Density
[PLNS,SENE]

ANSYS APDL
SJR Predictions



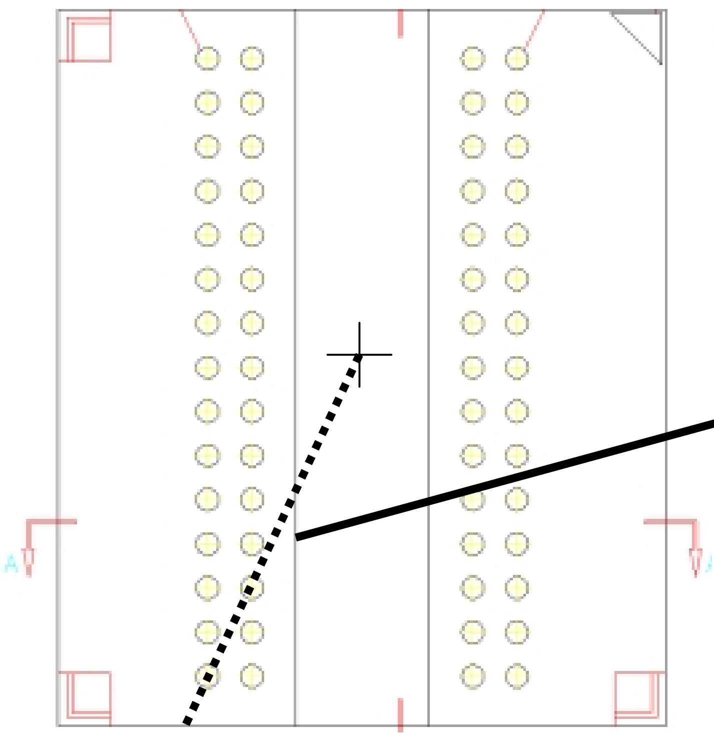
<u>Darveaux's</u>

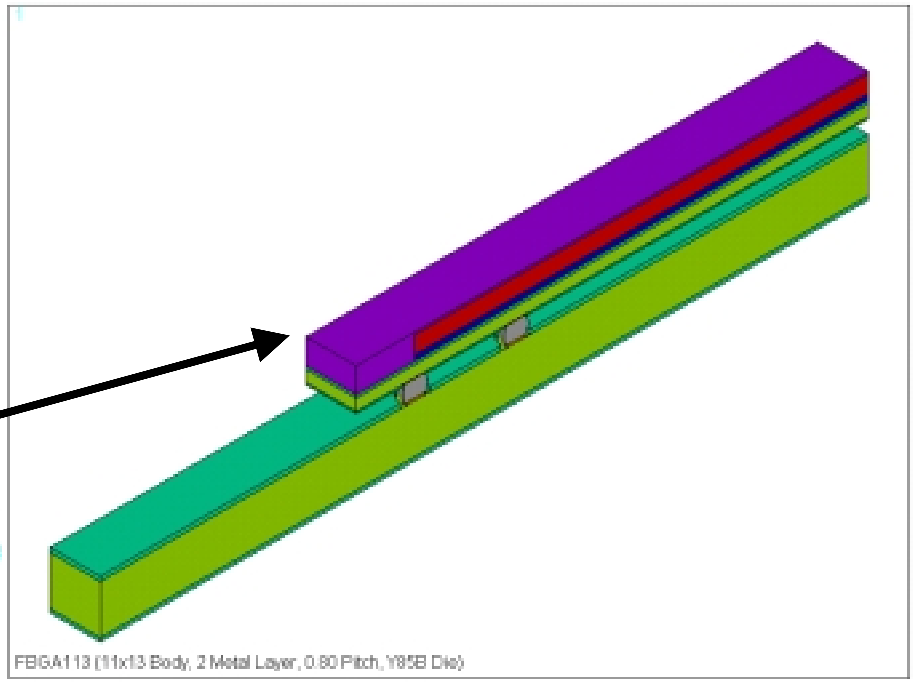
$$N = C_1 \, \Delta W_{ave}^{\;C_2}$$

$$\frac{da}{dN} = C_3 \, \Delta W_{ave}^{\;C_4}$$

$$\alpha = N + \frac{a}{da/dN}$$

Generalized Strain Models





Courtesy: Bret Zahn, ChipPac, Inc.

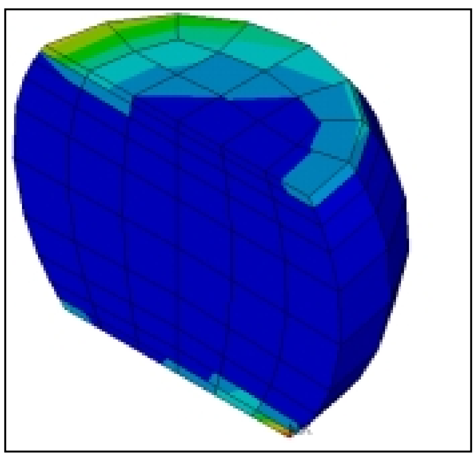
SJR Life Prediction Method

Calculate Strain Energy Density Accumulated per Cycle → ΔW

Calculate Number of Cycles to Crack Initiation → N_0

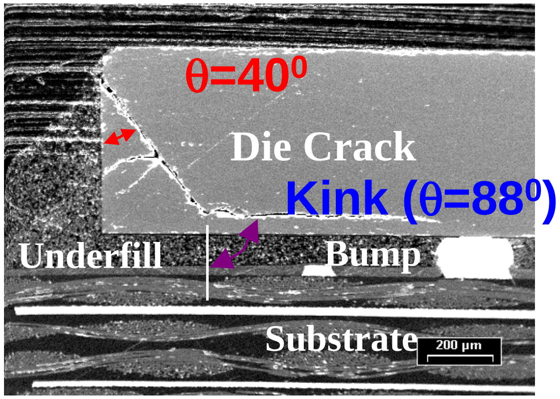
Calculate Crack Growth Rate → da/dN

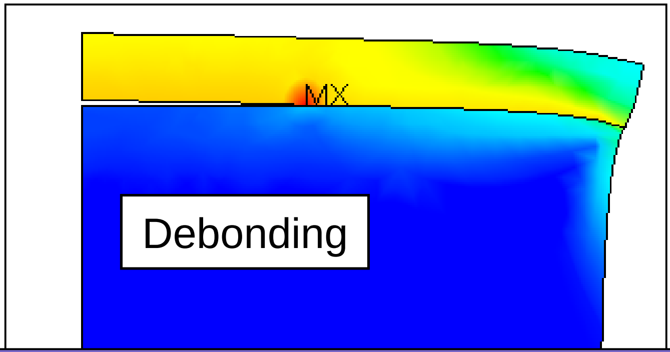
Calculate Fatigue Life Based on Joint Length → N_f



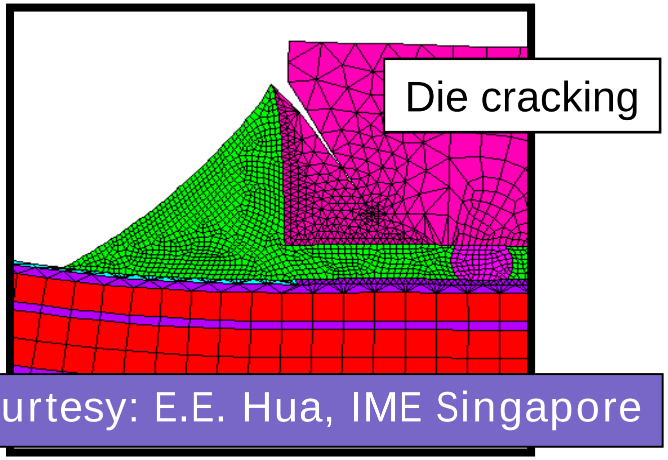
Advanced FEA

- Advanced FEA
  - Fracture Mechanics: assuming a pre-existing crack or delaminated interface, use displacement to calculated the strain energy release rate for crack growth





Courtesy: Metin Ozen, MCR Associates



Courtesy: E.E. Hua, IME Singapore

Thermal Simulations

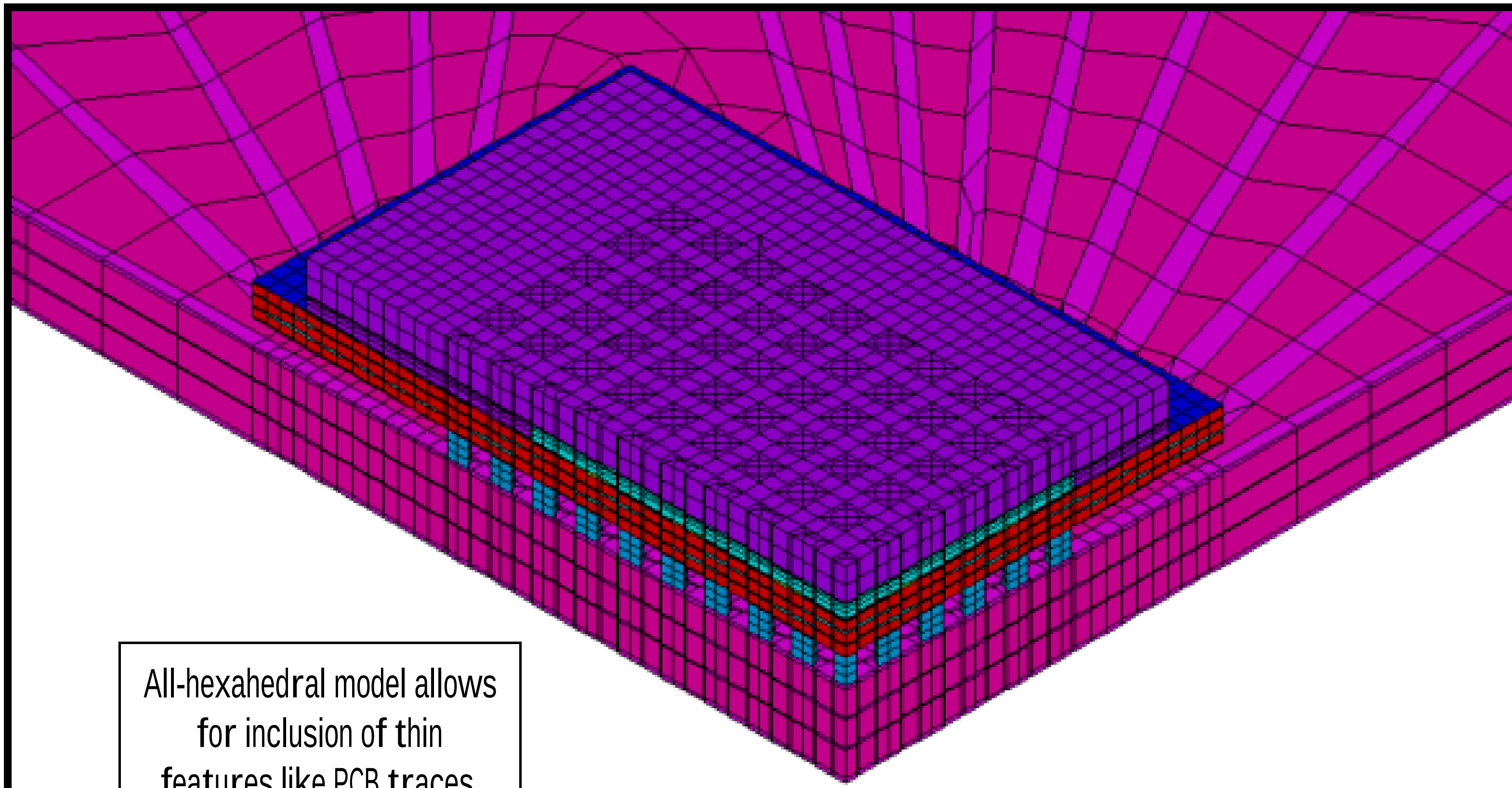
Thermal Resistance Modeling

Assembly Equipment & Process Simulation

CONTROL MACRO

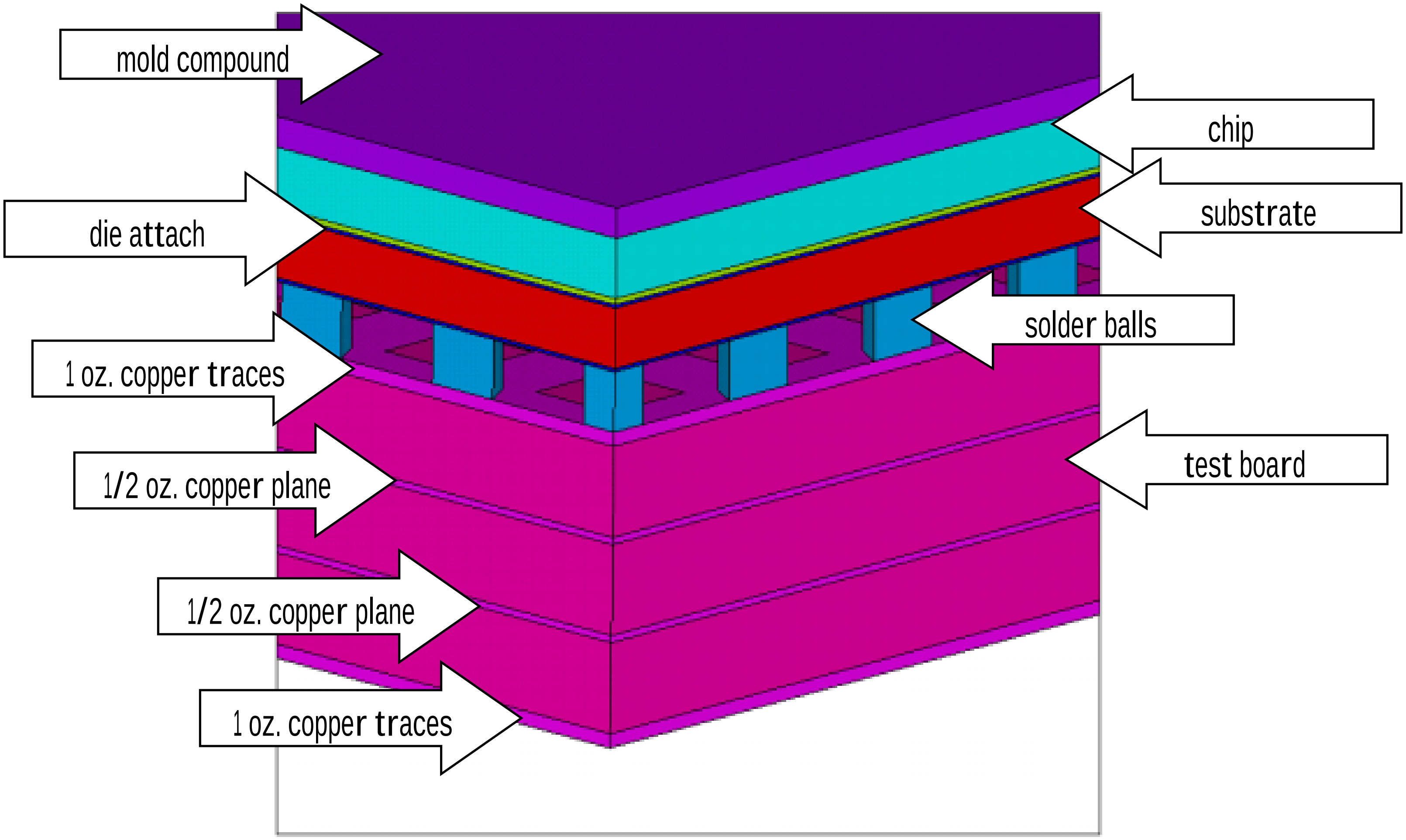
- **Thermal Model**
  Construction
  - **Die Parameters**
    Die size
    Power dissipation
  - **Package Parameters**
    Package size
    Array configuration
    (e.g., 4RR)
  - **PWB Parameters**
    Layer configuration
    (1S0P, 2S0P, 2S2P)
- **Boundary Conditions**
  Convection, Fixed Temp.,
  and Heat Flux
  - **Top Cold Plate**
    Theta JC
  - **Ring Cold Plate**
    Theta JB
  - **Forced Convection**
    Theta JMA
    Psi JT
  - **Free Convection**
    Theta JA
    Psi JT
- **Results Evaluation**
  Theta and Psi
  Calculations
  - **Velocity Dependence**
    Theta JA & Psi-JT
  - **Fixed Conditions**
    Theta JB & JC

All-Hexahedral Mesh

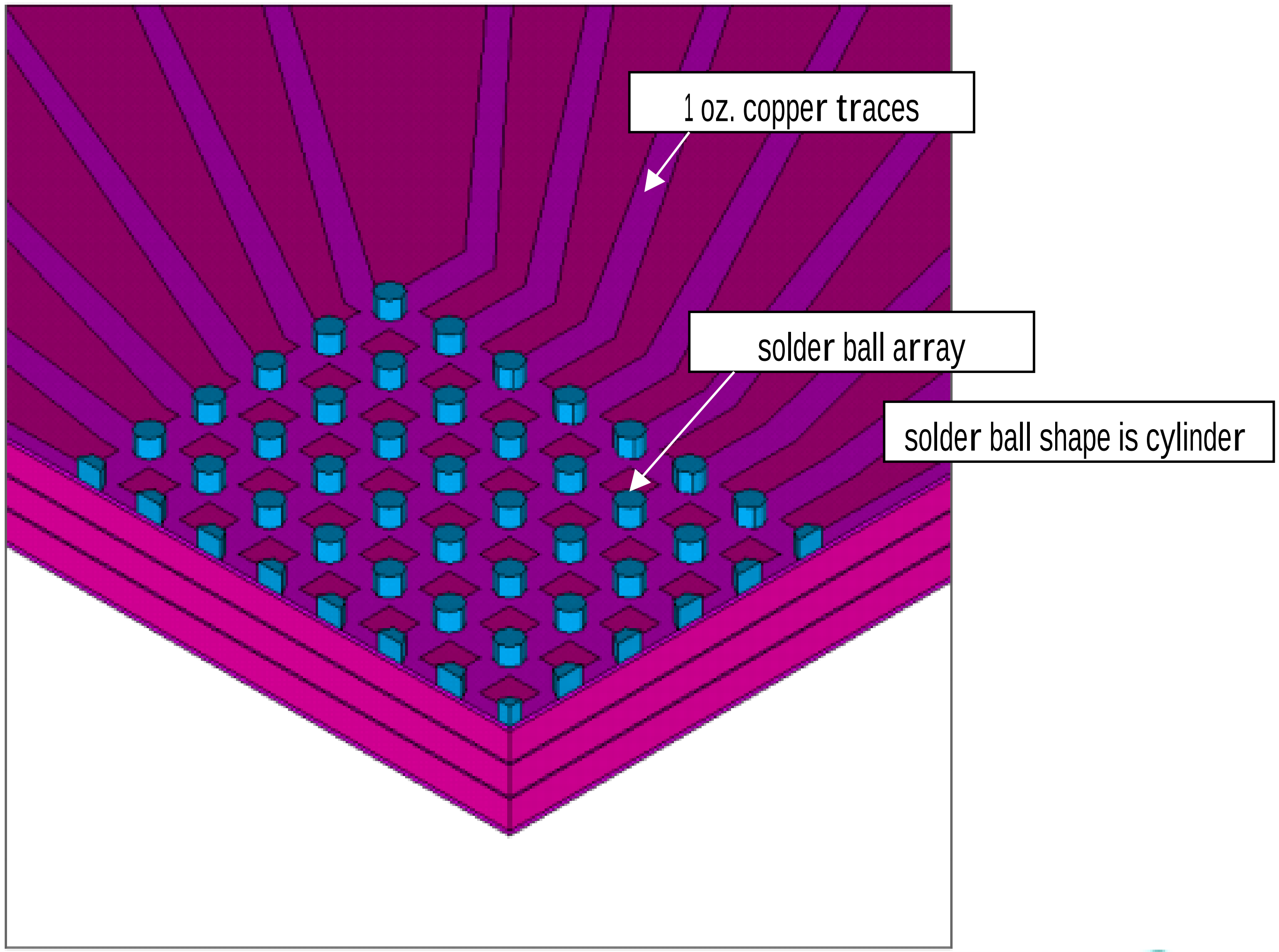


All-hexahedral model allows for inclusion of thin features like PCB traces, die attach, and tapes.

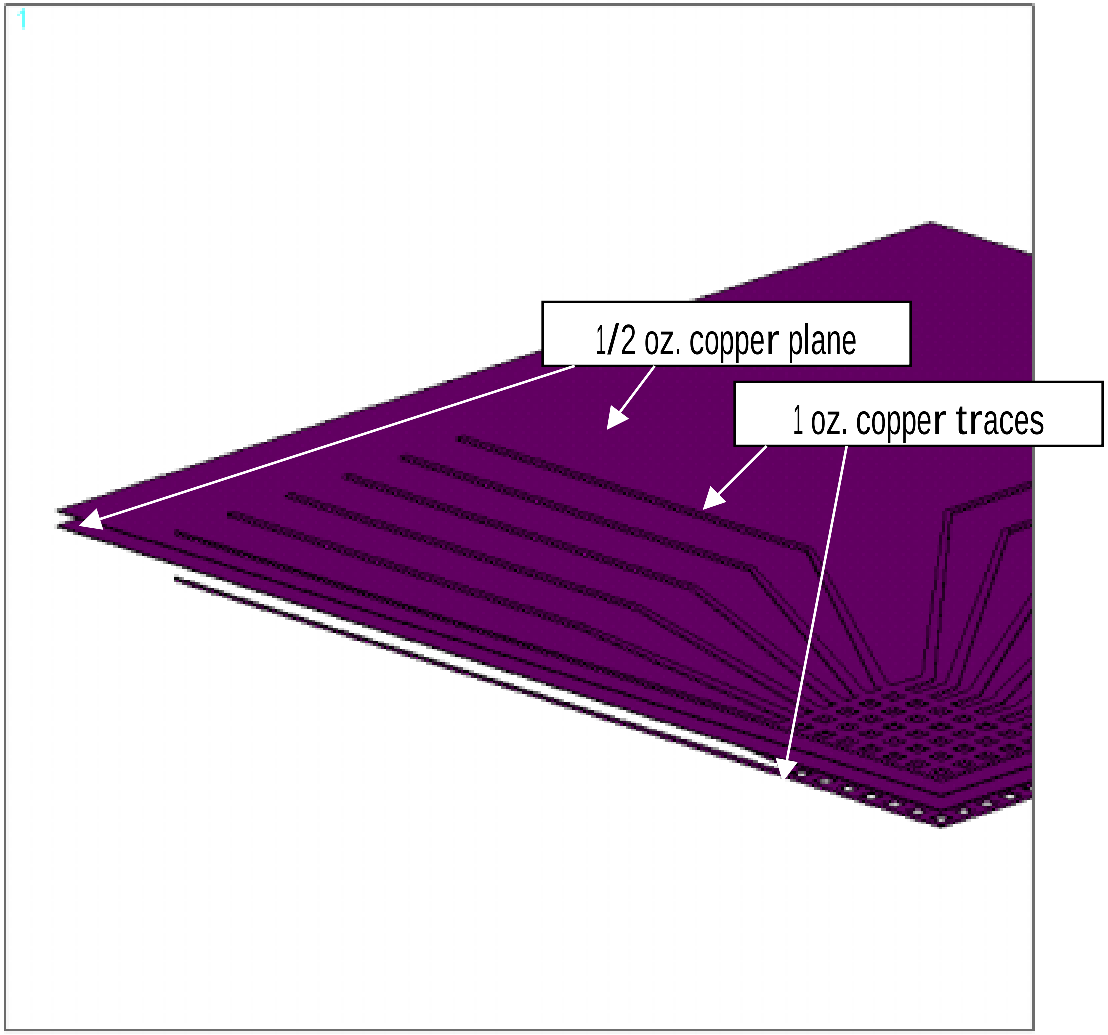
ANSYS Solid Model



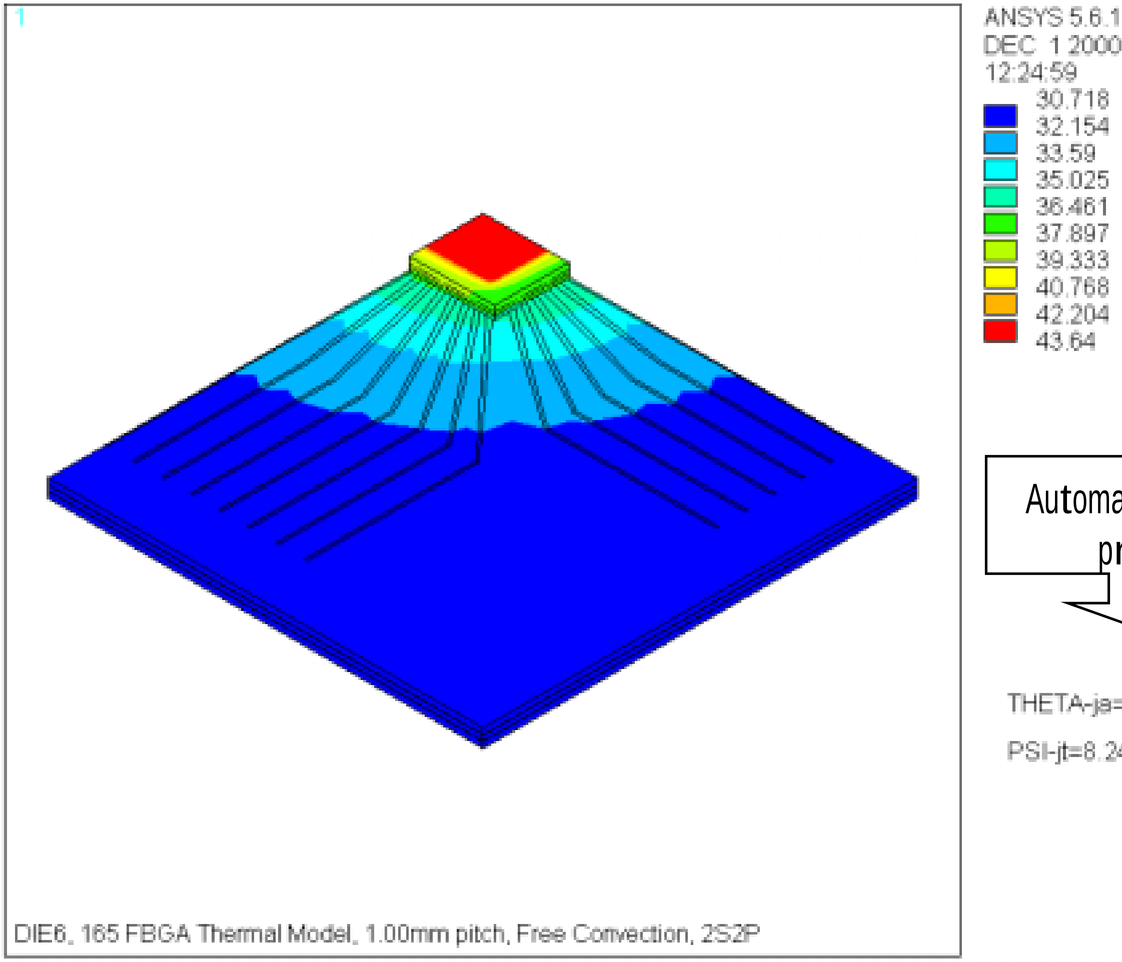
Solder Ball Array



Test Board Traces & Planes



Free Convection

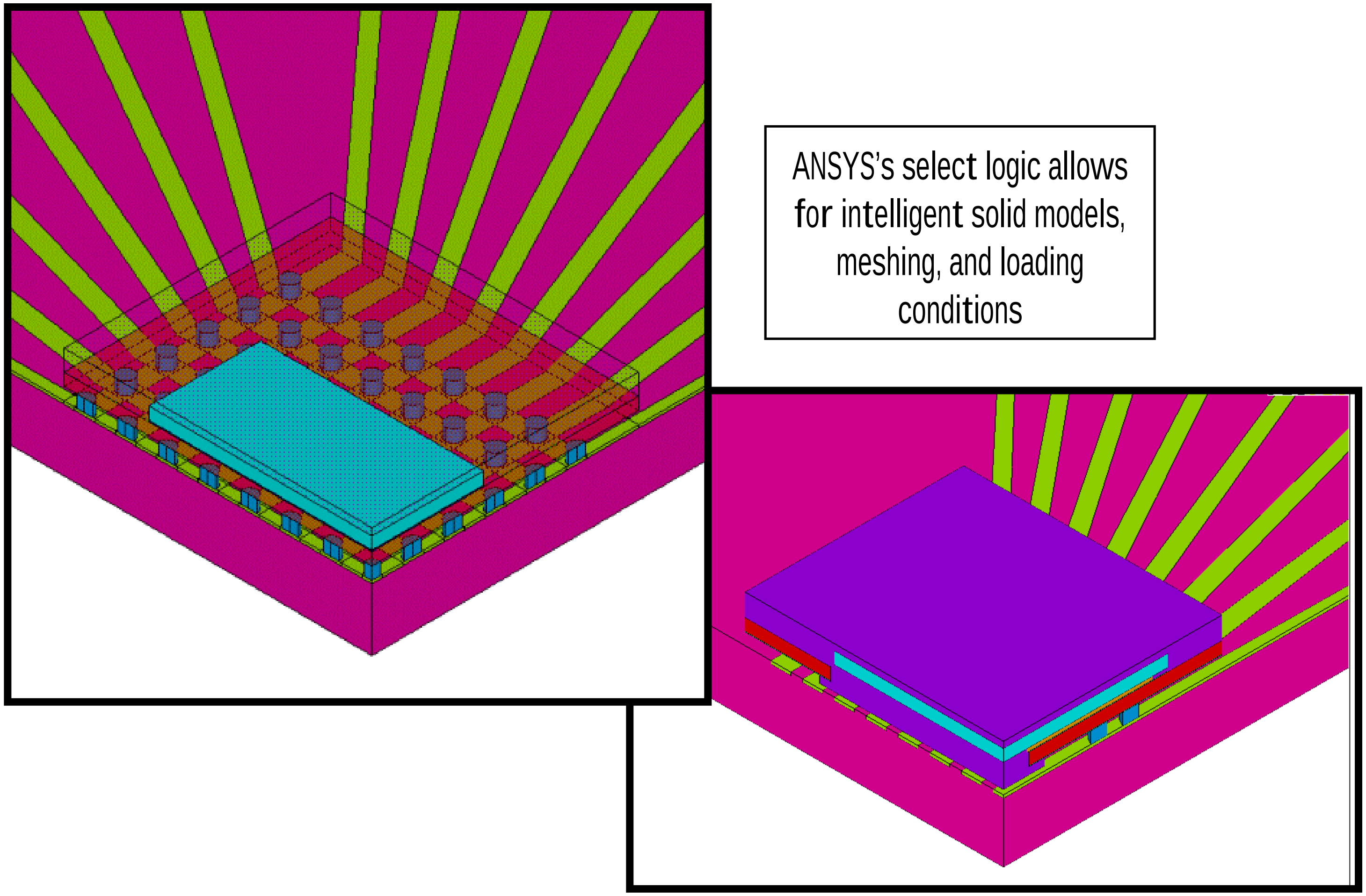


Automated results printing

THETA-ja=24.8527449

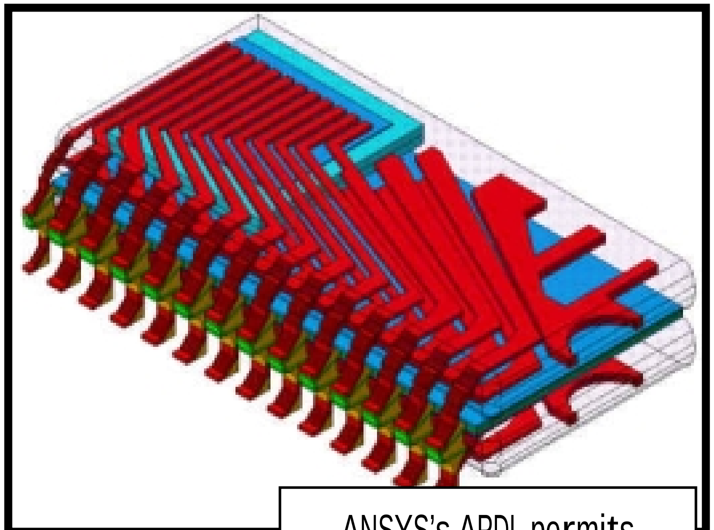
PSI-jt=8.24741211E-02

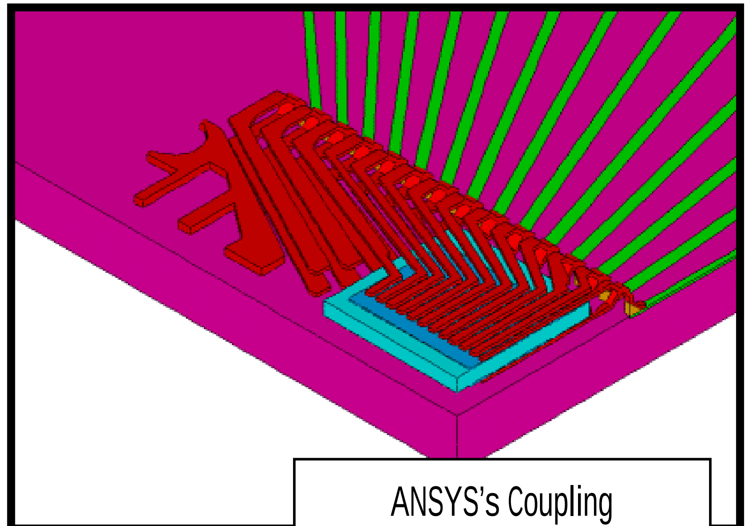
Automated Simulation



ANSYS's select logic allows for intelligent solid models, meshing, and loading conditions

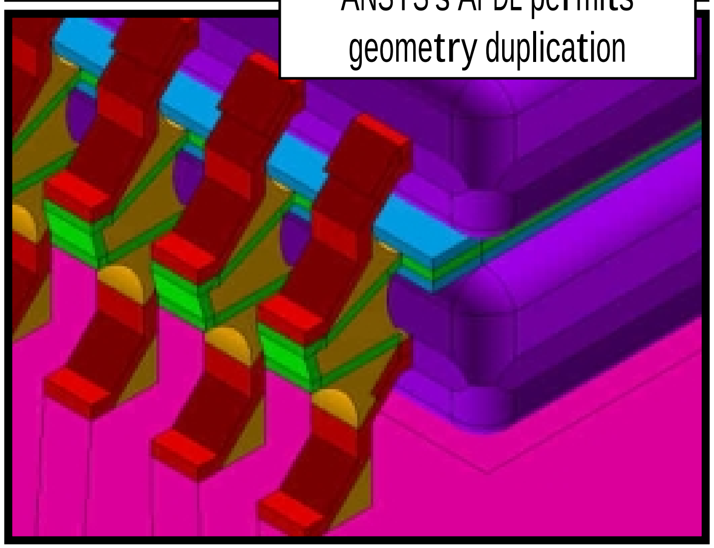
Complex Solid Model

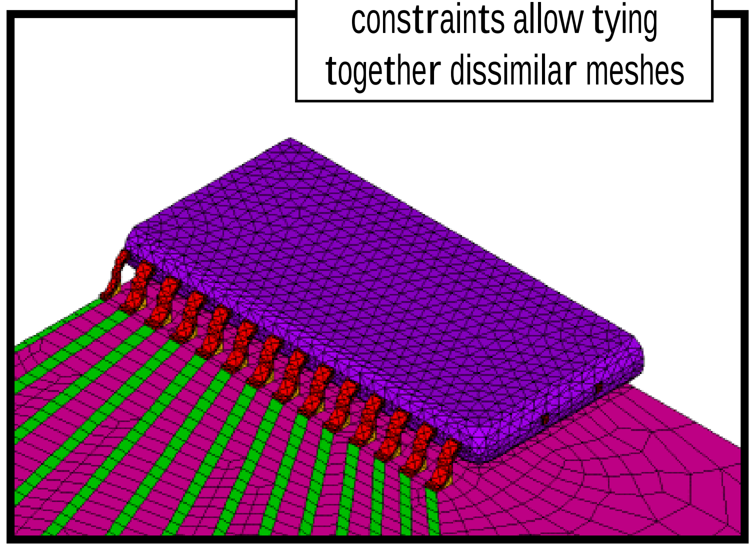




ANSYS's APDL permits geometry duplication

ANSYS's Coupling constraints allow tying together dissimilar meshes

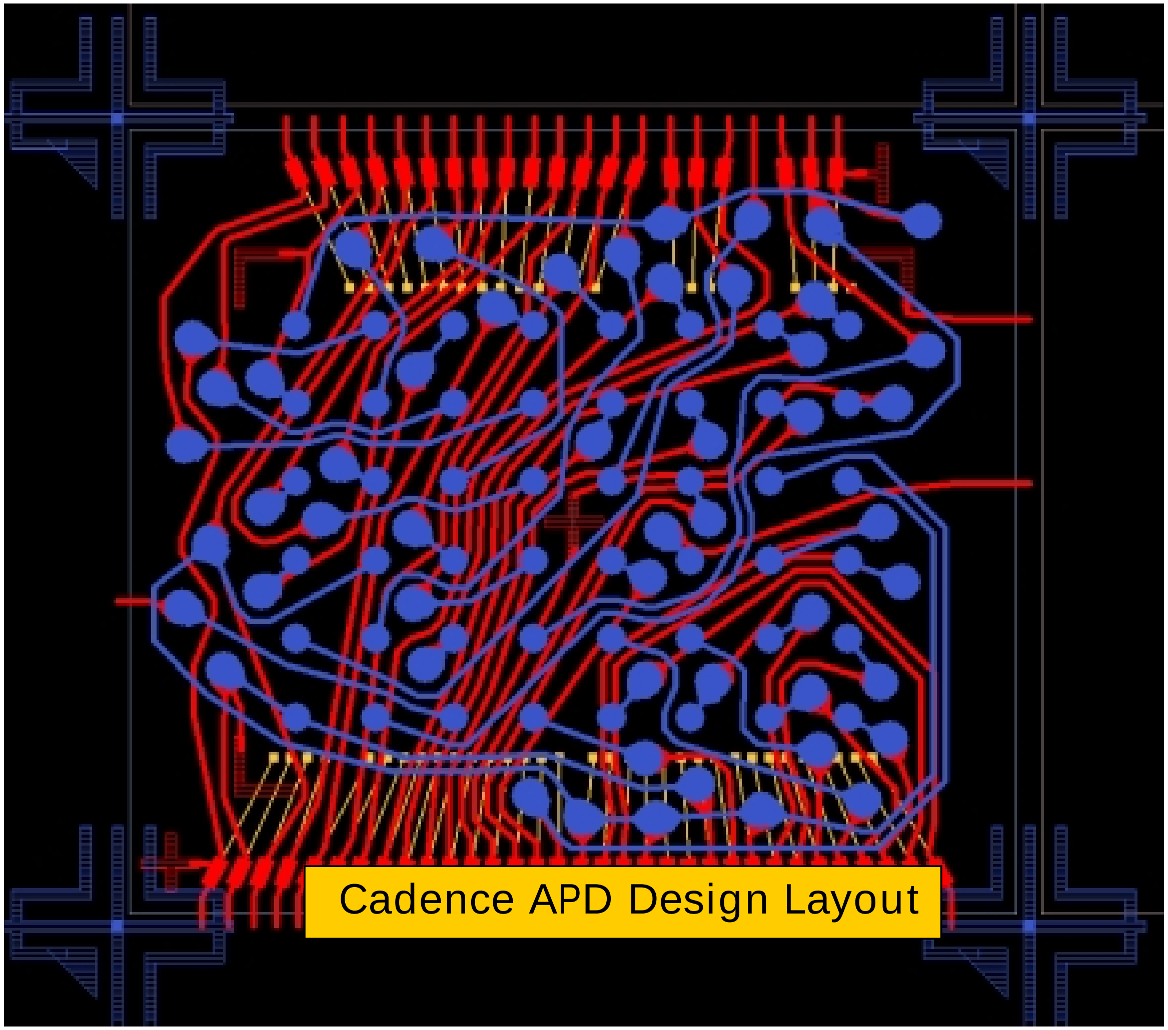




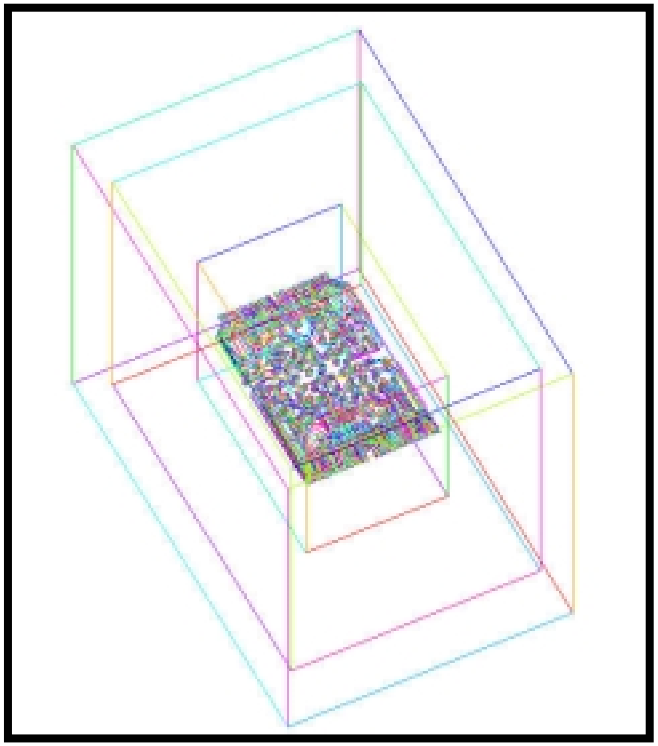
Convection Coefficients

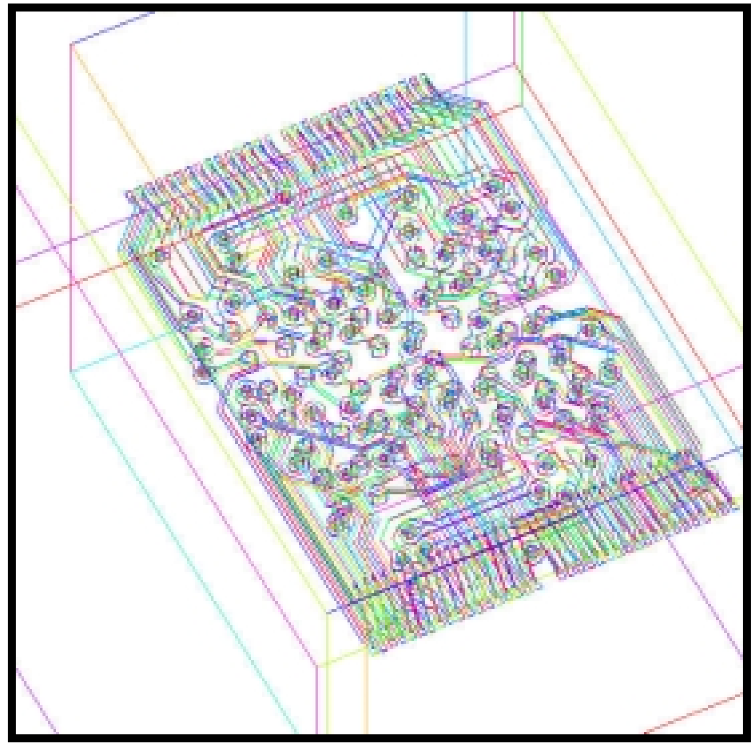
Location	JEDEC 2-Layer Test Board (Isothermal)	JEDEC 4-Layer Test Board (Isoflux)
Free Convection • Top of Package • Top of PCB	$\bar{h}_{up} = 1.336 \cdot \left(\frac{T_S - T_\infty}{\left(\frac{area}{2 \cdot perimeter} \right)} \right)^{0.25}$	$\bar{h}_{up} = 0.551 \cdot \left(\frac{q^{0.185}}{\left(\frac{area}{2 \cdot perimeter} \right)^{0.260}} \right)$
Free Convection • Bottom of PCB	$\bar{h}_{down} = 0.668 \cdot \left(\frac{T_S - T_\infty}{\left(\frac{area}{2 \cdot perimeter} \right)} \right)^{0.25}$	$\bar{h}_{down} = 0.520 \cdot \left(\frac{q^{0.166}}{\left(\frac{area}{2 \cdot perimeter} \right)^{0.336}} \right)$
Forced Convection • All Horizontal Surfaces	$h_{forced} = 5.289 \cdot \left(\frac{v}{L} \right)^{0.5}$	
Radiation • All Horizontal Surfaces	$h_{radiation} = \varepsilon_{package(PWB)} \cdot \sigma \cdot (T_S + T_\infty) \cdot (T_S^2 + T_\infty^2)$	

Cadence Layout



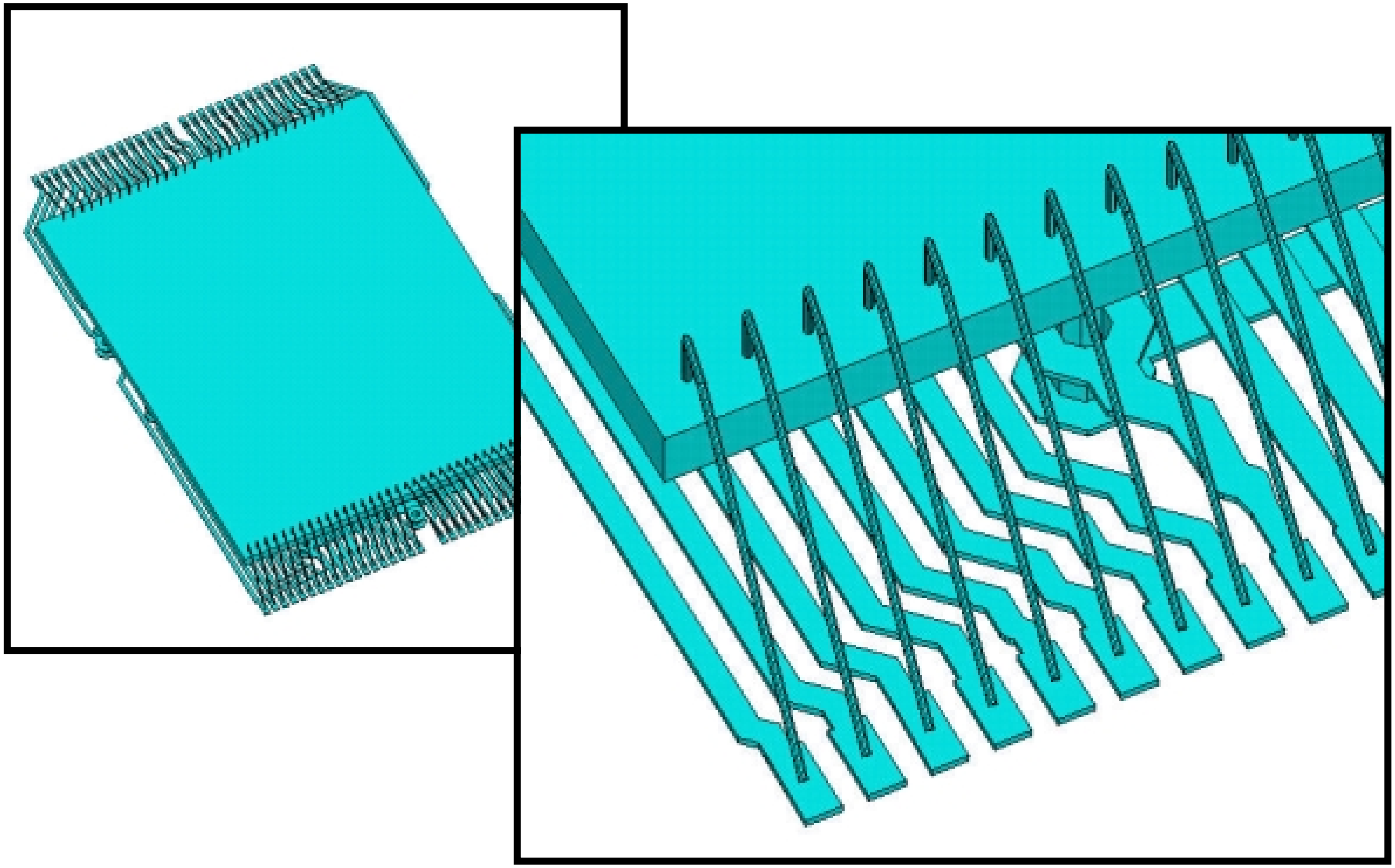
All Volumes Imported



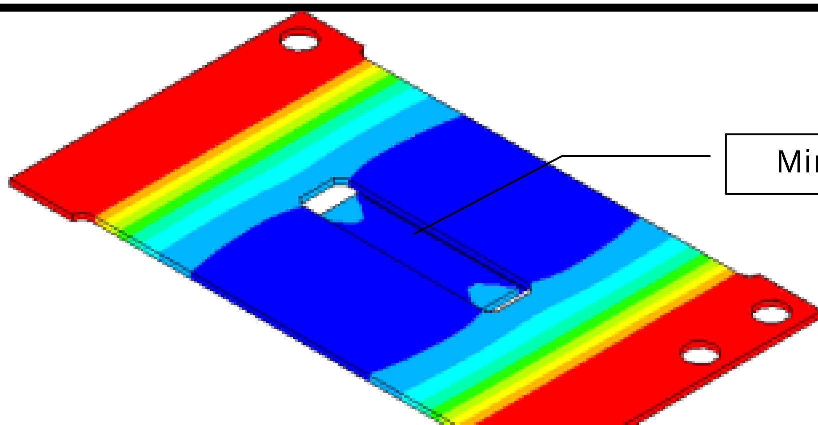


Cadence APD to ALINKS (SAT) to ANSYS (SAT Import)

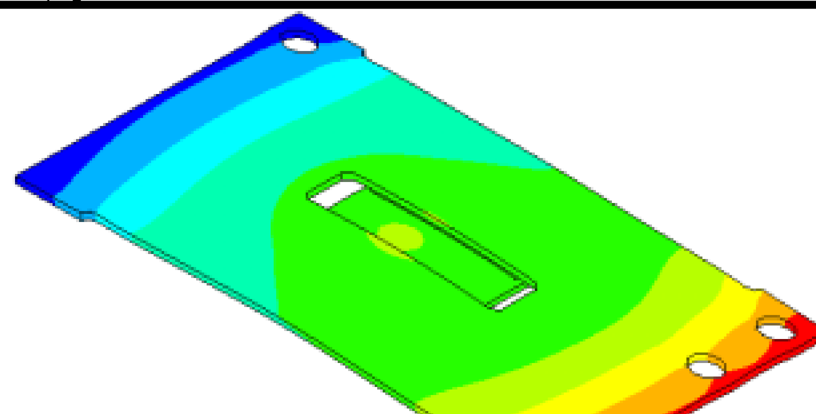
Chip and Conductors



Preheating Warpage



• Temperature profile after 10 seconds on preheater



• Warpage profile after 10 seconds on preheater (strip warpage is 29 microns)

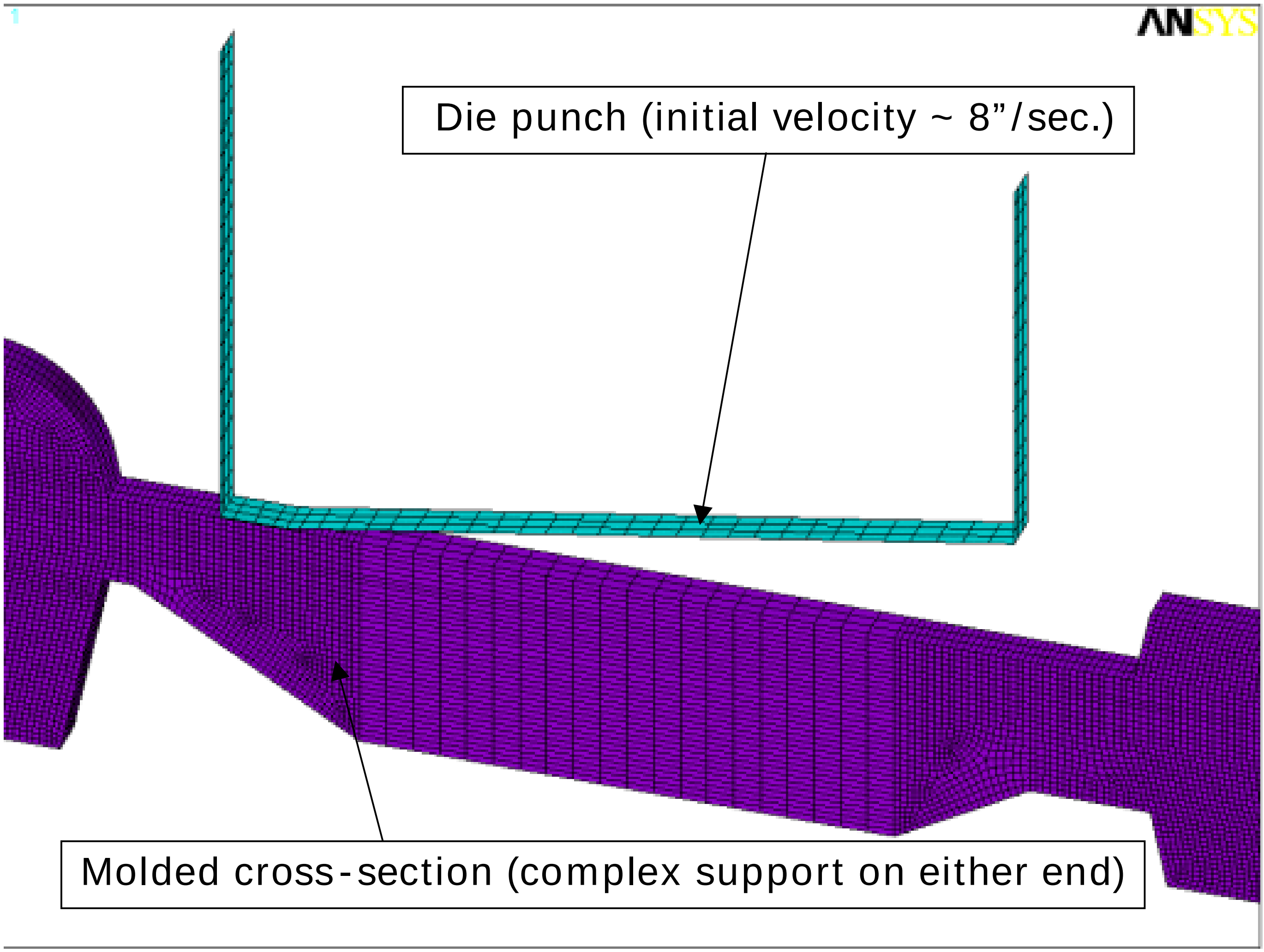
Impact-Related Simulation

Molded Gate Punch Simulation

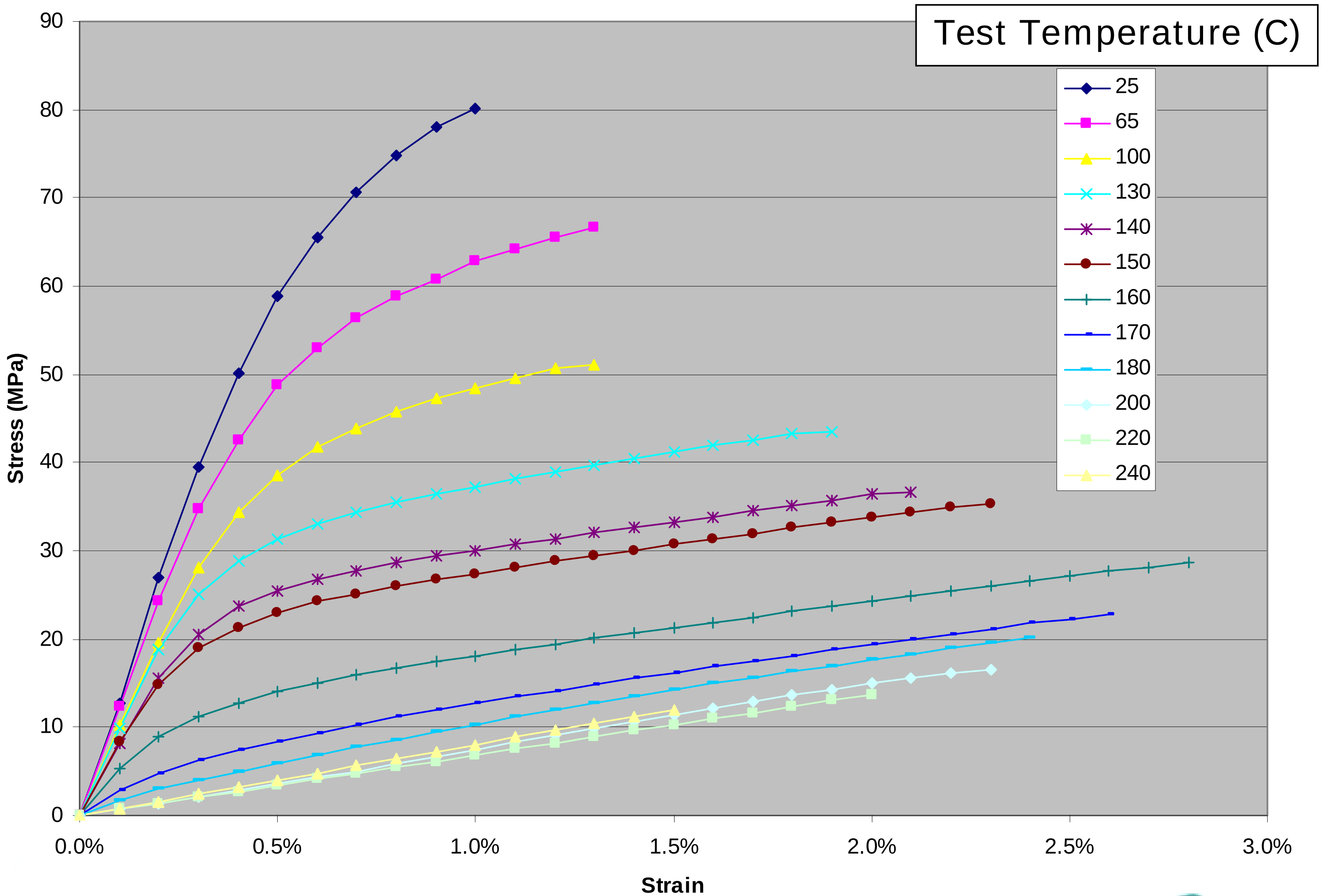
Punch Simulation

- Achieve simulation of die punching through semi-ductile mold compound (<2% strain at break) using eroding boundary conditions.
- Evaluate effects of die punching of various molded gate shapes
- Determine velocity effects on “cleanliness” of fracture

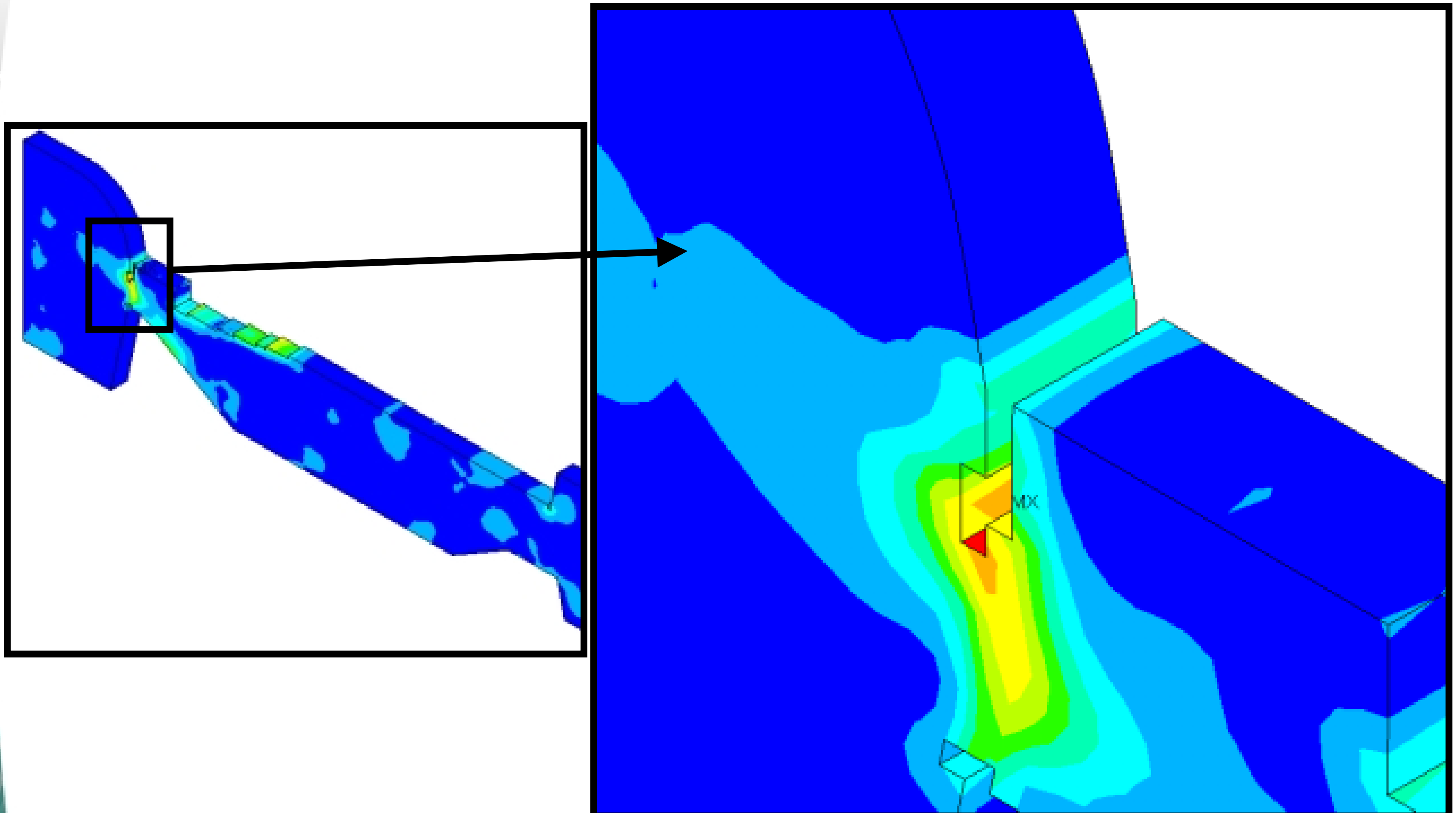
Solid Model/Mesh



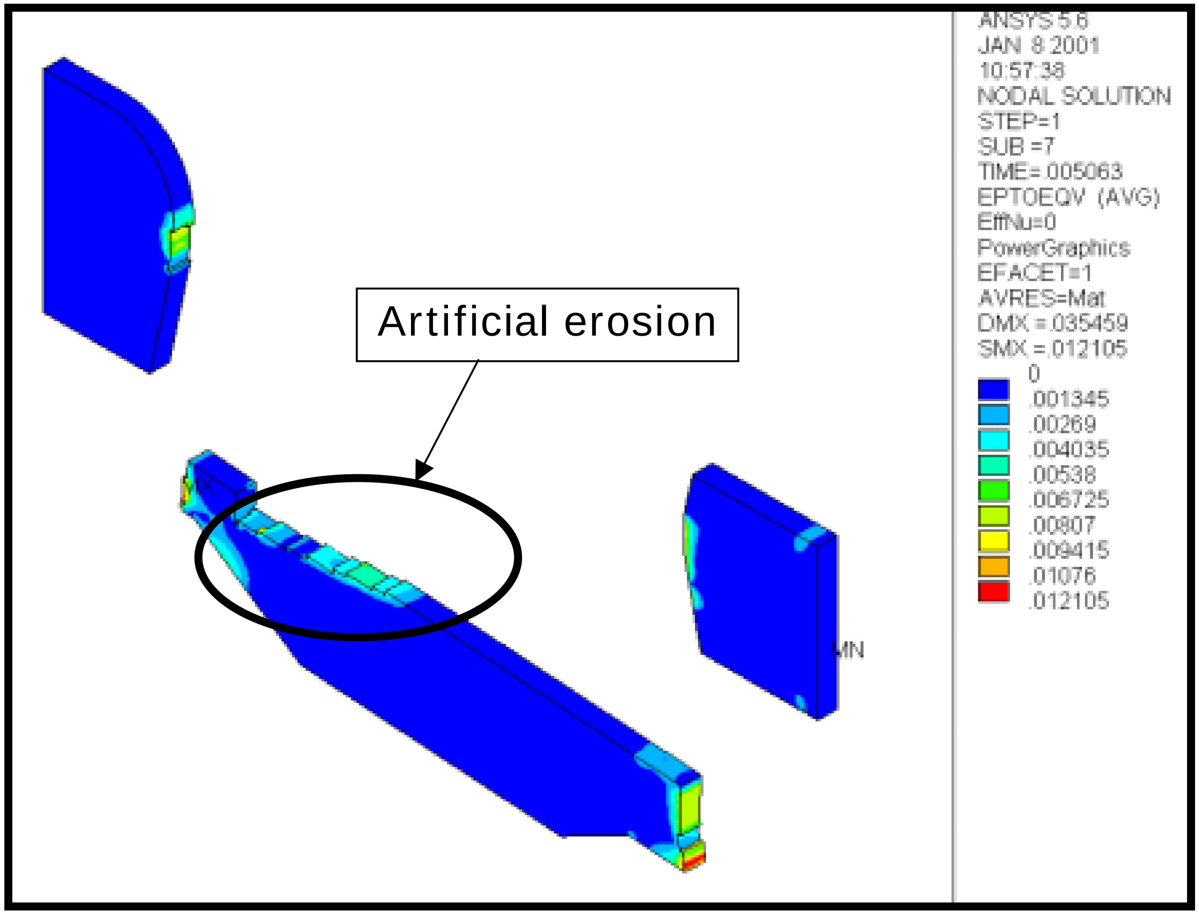
Typical Mold Compound

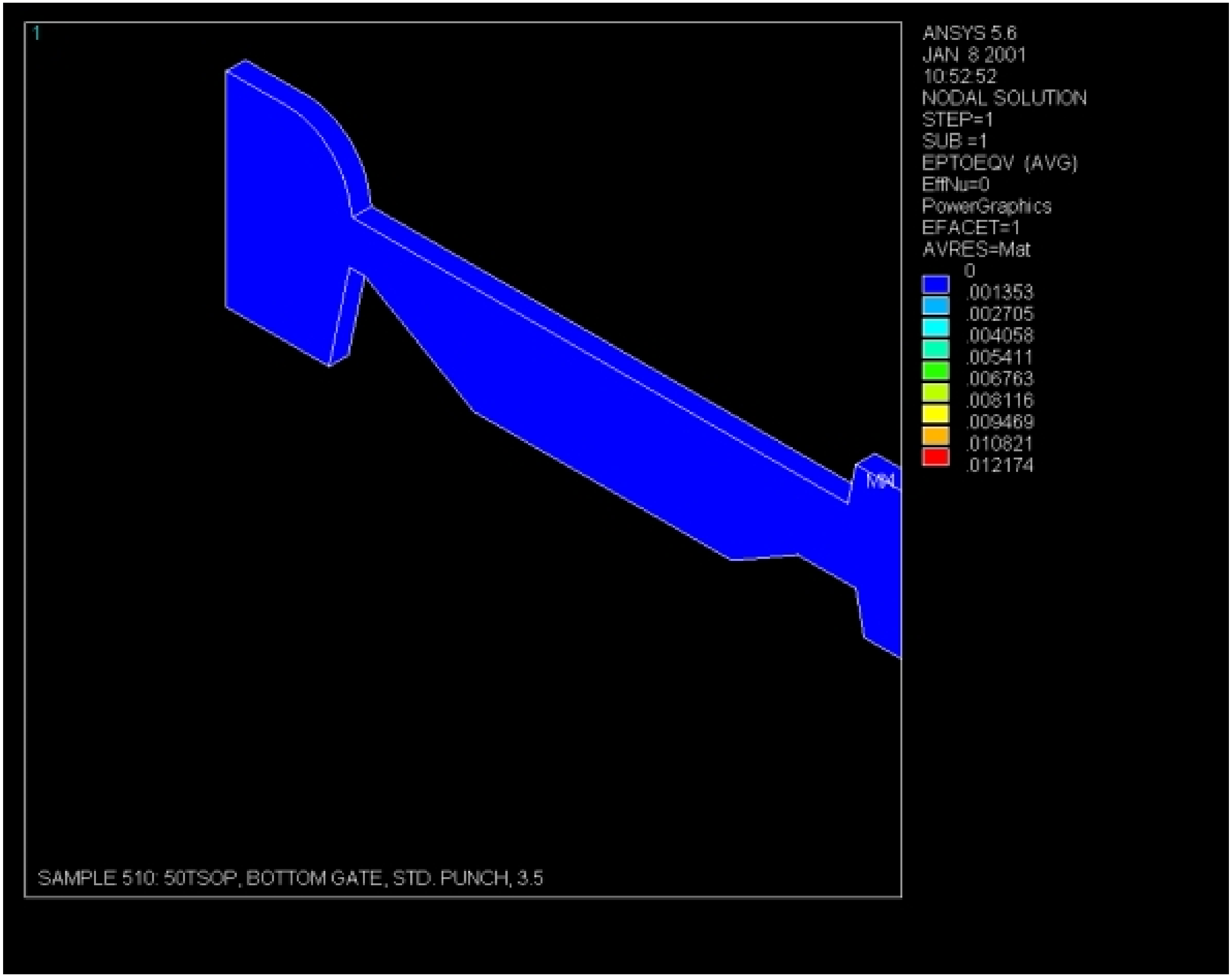


Crack Initiation



Complete Break




1
ANSYS 5.6
JAN 8 2001
10:52:52
NODAL SOLUTION
STEP=1
SUB =1
EPTOEQV (AVG)
EffNu=0
PowerGraphics
EFACET=1
AVRES=Mat
0
.001353
.002705
.004058
.005411
.006763
.008116
.009469
.010821
.012174
MX
SAMPLE 510: 50TSOP, BOTTOM GATE, STD. PUNCH, 3.5

Advanced Simulation

- Application to Silicon Wafer Level Simulation
  - Thin film effects vs. bulk effects
  - Coupled-field analyses (e.g., Joule heating)
- Integrated Tools
  - Linking mold flow to mechanical simulations
  - Scaling chip to system performance and vice versa
- Process Equipment Simulation
  - Chemical kinetics, high-speed thermal transport, and part-to-equipment interactions (e.q., sliding contacting).

Wafer Fab Applications

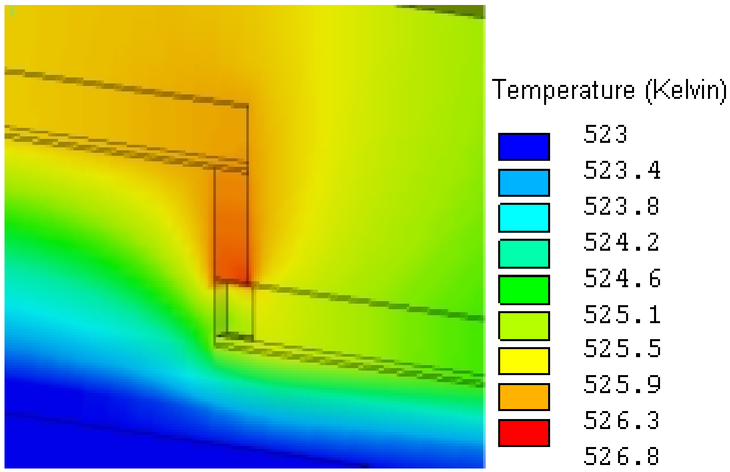


FIG. 6 (top). A contour plot showing the temperature distribution due to Joule heating under J=10^6 A/cm^2 and the substrate T=250°C (523 K). The depletion length is 0.42 µm and the consequent ΔR is 9.4 Ω.

Thermoelectric Simulation
Wafer Level Metallization & Vias

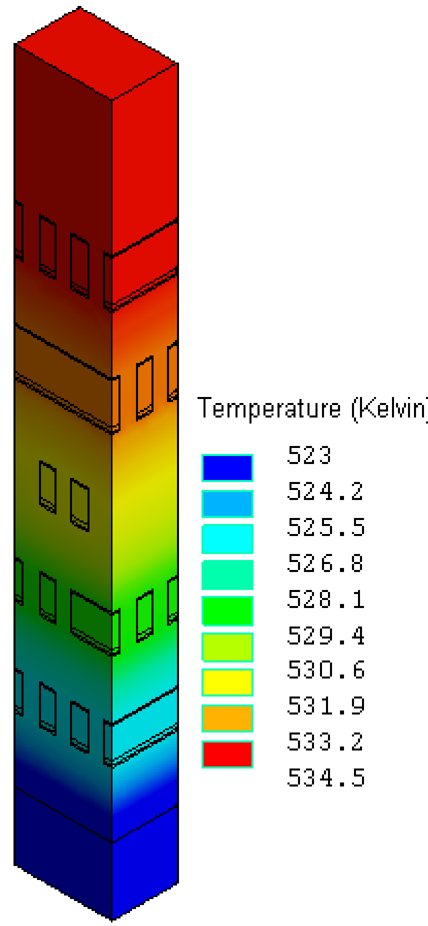
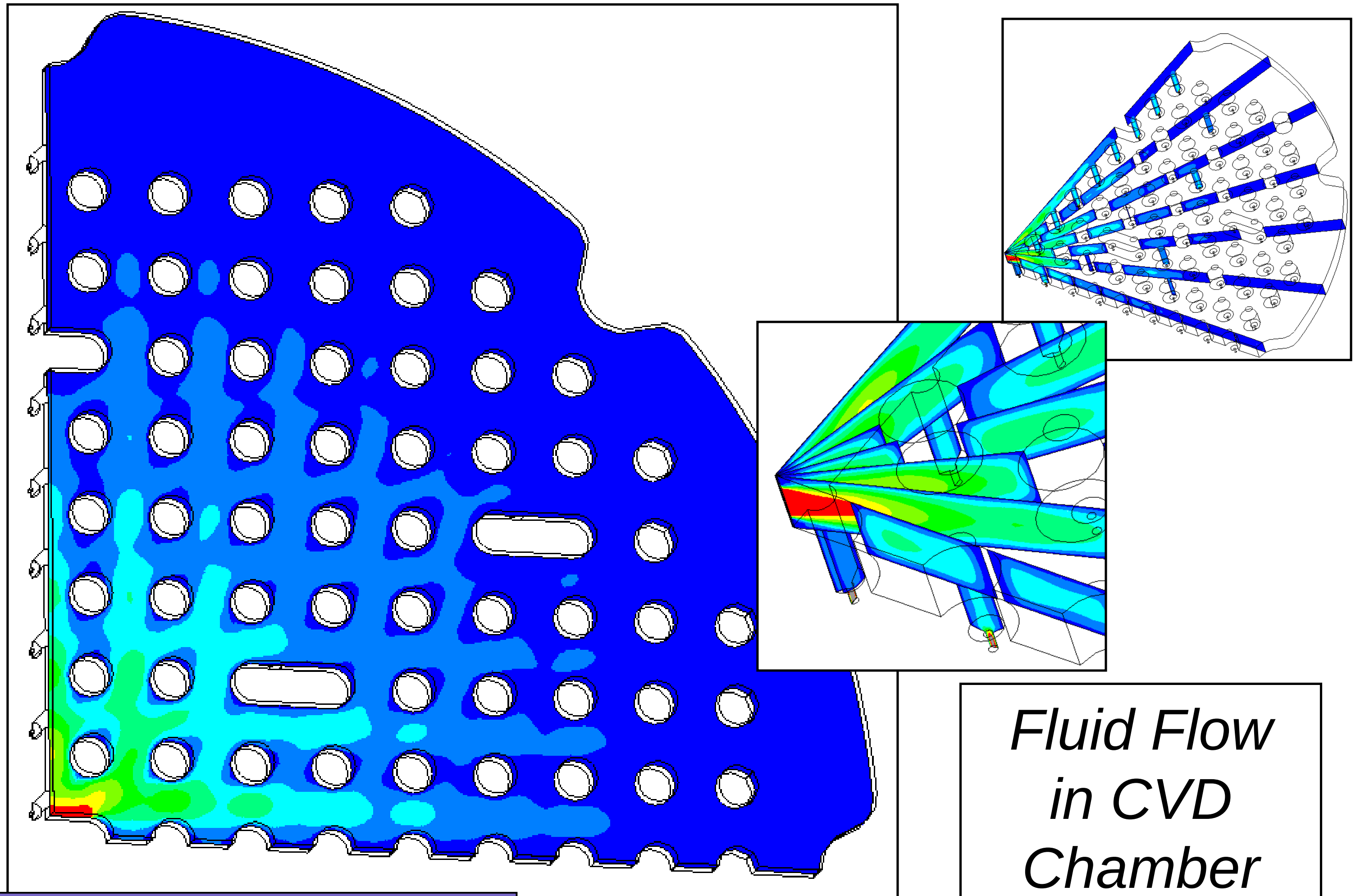


FIG. 7 (right). A contour plot showing the temperature distribution in 5-level interconnects due to Joule heating under J=10^6 A/cm^2 and the substrate T=250°C (523 K).

Courtesy: S.Kang, Lucent Technologies, Inc.

Wafer Process Simulation



Fluid Flow in CVD Chamber

Courtesy: PADT, Incorporated

Conclusions

- ANSYS simulations have <u>wide application</u> among semiconductor manufacturing and reliability testing processes.
- <u>Automation</u> of solid model, meshing, and post-processing is one key to productivity.
- Simulating <u>coupled-field effects</u> requires some materials, mechanics, and physics expertise to produce reasonable results.
- <u>Exchange</u> of non-proprietary APDL routines can provide some of the needed productivity gains.