Finite Element Based Solder Joint Fatigue Life Predictions for a Same Die Stacked Chip Scale Ball Grid Array Package

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Abstract

Viscoplastic finite-element simulation methodologies were utilized to predict solder joint reliability for a same die size, stacked, chip scale, ball grid array package under accelerated temperature cycling conditions (-40C to +125C, 15min ramps/15min dwells). The effects of multiple die attach material configurations were investigated along with the thickness of the mold cap and spacer die. The solder structures accommodate the bulk of the plastic strain that is generated during accelerated temperature cycling due to the thermal expansion mismatch between the various materials that encompass the stacked die package. Since plastic strain is a dominant parameter that influences low-cycle fatigue, it was used as a basis for evaluation of solder joint structural integrity. The paper discusses the analysis methodologies as implemented in the ANSYS finite element simulation software tool and the corresponding results for the solder joint fatigue life. Some ANSYS parametric design language commands are included for the benefit of those readers who are familiar with the tool.

Introduction

As the demand for more functionality in electronic systems continues to grow, more effort is focused on the development of system-in-a-chip devices. For years, the least expensive way to add more functions to an electronic system was to integrate more functions into the individual chips themselves. However, cost and yield issues can prevent such integration from being economically feasible. Furthermore, some chip sets that logically belong together to form a system or subsystem cannot be integrated into a single die due to differences in the die materials. Such is the case with silicon and gallium arsenide. High-density packaging technologies have advanced to the point where intentionally splitting a single chip system into multiple dice can provide both performance and cost advantages. System-in-a-package solutions are expected to grow significantly in market share, offering a favorable combination of cost, speed, and density.

One classification of a system-in-a-package solution gaining wider acceptance is the stacked-die package, where the main concern is saving space. It is feasible that in such a package, the stacked die may be of the same size, thus requiring the insertion of a spacer between the two active die in order to facilitate wire bonding to each of the die surfaces. The solder joint fatigue reliability concerns of such a package are analyzed herein under accelerated temperature cycling conditions (-40C to +125C, 15min ramps/15min dwells). Such conditions are commonly evaluated as part of the package qualification process.

The integrity of solder joints is a major reliability concern in modern microelectronic packages. Temperature fluctuations caused by either power transients or environmental changes, along with the resulting thermal expansion mismatch between the various package materials, results in time and temperature dependent creep deformation of solder. This deformation accumulates with repeated cycling and ultimately causes solder joint cracking and interconnect failure. To minimize development costs and maximize reliability performance, advanced analysis is a necessity during the design and development phase of a microelectronic package. This requires the utilization of a life prediction methodology that is based on the damage mechanisms experienced in a field operation environment.

Several finite element based analysis methodologies have been proposed which predict solder joint fatigue life (e.g. Engelmaier [1]; Shine and Fox [2]; Wong et al. [3]; Yamada [4]; Subrahmanyan et al. [5]; Dasgupta et al. [6]; Pao [7]; Clech et al. [8]; Syed [9]; Darveaux et al. [10]; and Darveaux [11]). It should be noted that there is a material limitation inherent to many of these methodologies since they assume the utilization of eutectic 63Sn/37Pb solder or some similar combination of solder materials (i.e.
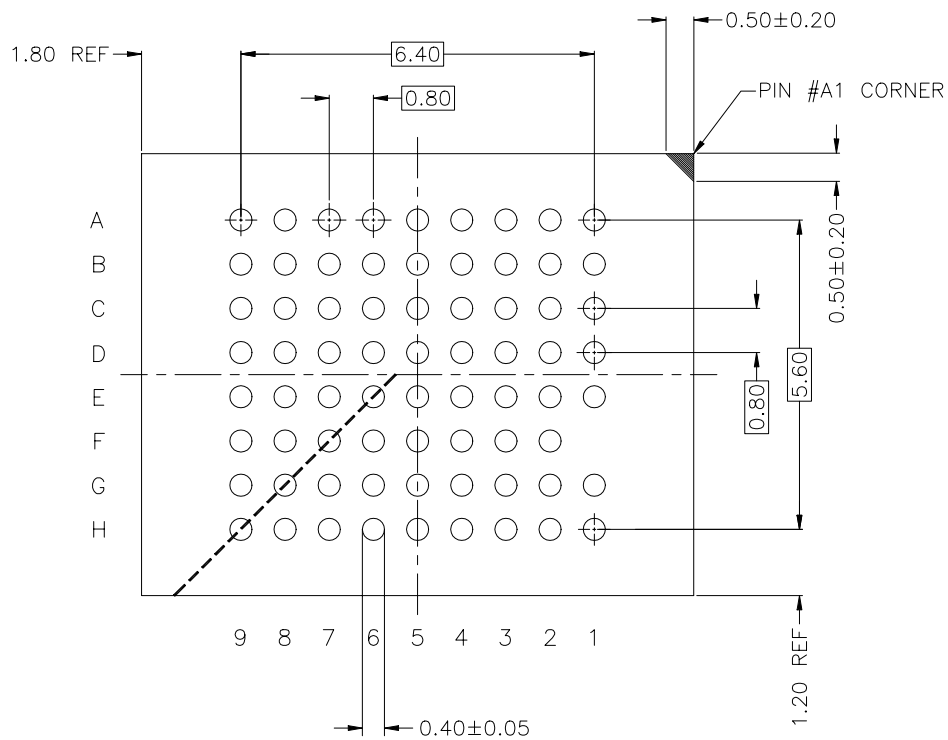
62Sn/36Pb/2Ag). Life prediction methodologies for high temperature solder (90Pb/10Sn, 95Pb/5Sn, etc.) or future lead-free based interconnect materials, are almost non-existent due to their low volume use or relative infancy in today's microelectronics packaging industry.

Of all these methodologies, Darveaux's seems to be the most popular due to the ease in its implementation. Darveaux's methodology links laboratory measurements of low-cycle fatigue crack initiation and crack growth rates to the inelastic work of the solder. It is a strain energy based approach, where the work term consists of time-dependent creep and time-independent plasticity. This inelastic behavior is captured in ANSYS using Anand's constitutive model [12]. The modeling methodology utilizes finite element analysis to calculate the viscoplastic strain energy density accumulated per cycle during thermal or power cycling. The strain energy density is then utilized with crack growth data to calculate the number of cycles to initiate a crack, and the number of cycles for the crack to propagate across a solder joints diameter.
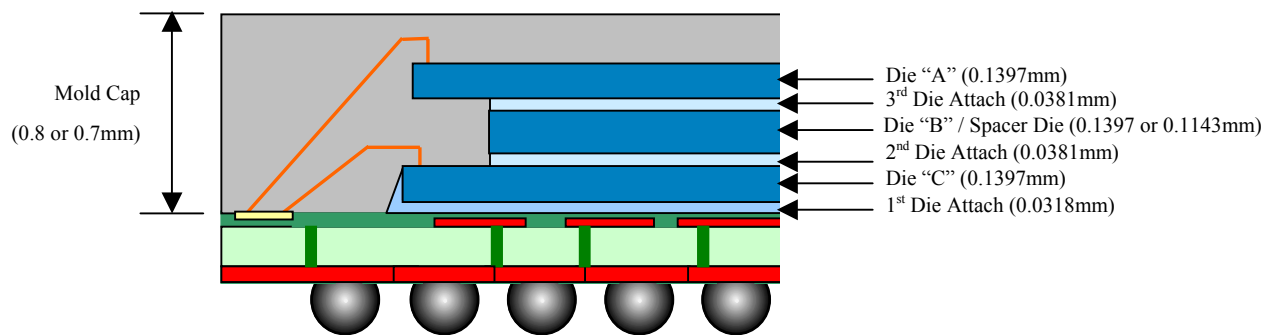
Darveaux's methodology has been previously presented in the successful analyses of various electronic assemblies from multiple industry sources. Amagai [13] generated lifetime predictions for a chip scale package on an organic printed circuit board. Fusaro and Darveaux [14] used the viscoplastic properties of eutectic solder to analyze the reliability of a copper baseplate attachment for a power module. Dougherty et al. [15] analyzed a micro-miniature electronic package. Johnson [16] and Pitaressi et al. [17] utilized the methodology to predict board-level solder joint reliability of multiple ball grid array packages. Recently, Zahn [18] and Goetz and Zahn [19] extended the methodology to predict both solder ball and solder bump reliability of a multi-chip silicon based system-in-package. In many of these publications, the authors have presented reliability test data that validates the accuracy of Darveaux's methodology within +/-2X, which is considered state of the art for this type of complex physical analysis.

Same Die Size Stacked Chip Scale Ball Grid Array Package
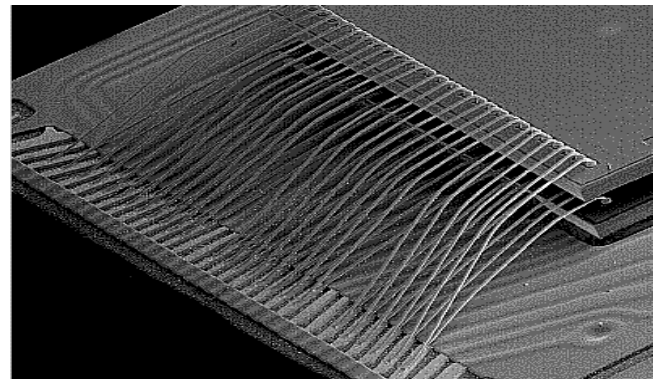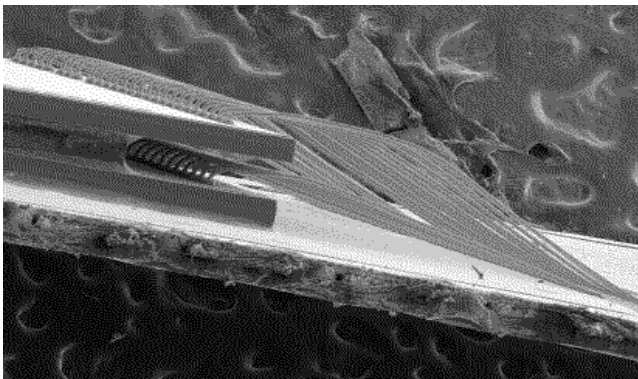
A 10x8mm, 72-ball (9x8 Full Matrix), 0.80mm pitch package was analyzed using a same size stacked die configuration.   The die size was measured at 7.9x6.4mm. The package outline drawing is displayed in Fig. 1. The basic structure of the stacked die package is shown in Fig. 2. A "spacer" die is placed between the two active die to facilitate wire bonding as displayed in Fig's 3 and 4. The layer dimensions of the printed circuit board and package substrate are given in Fig's 5 and 6. Dimensional details of the re-flowed solder ball along with the package substrate and printed circuit board solder re-flow pads are shown in Fig. 7.

Figure 1 - Package outline drawing

Die "A" (0.1397mm)
3rd Die Attach (0.0381mm)
Die "B" / Spacer Die (0.1397 or 0.1143mm)
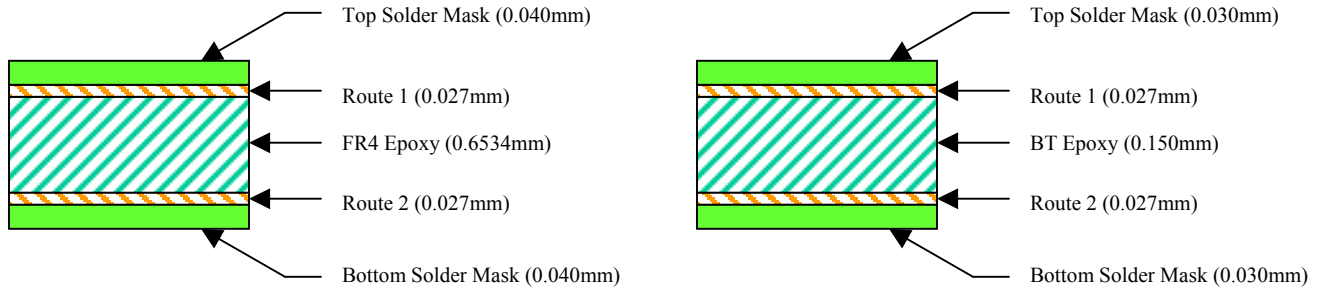2nd Die Attach (0.0381mm)
Die "C" (0.1397mm)
1st Die Attach (0.0318mm)

Mold Cap
(0.8 or 0.7mm)
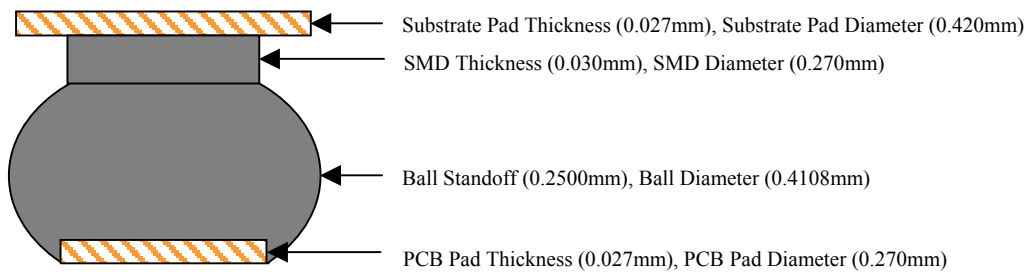
Figure 2 - Basic structure of stacked die package

Figures 3 & 4 - Wire bonding of a same size stacked die package

Top Solder Mask (0.040mm)

Route 1 (0.027mm)

FR4 Epoxy (0.6534mm)

Route 2 (0.027mm)

Bottom Solder Mask (0.040mm)

Top Solder Mask (0.030mm)

Route 1 (0.027mm)

BT Epoxy (0.150mm)

Route 2 (0.027mm)

Bottom Solder Mask (0.030mm)

Figures 5 & 6 - Layer dimensions of printed circuit board and package substrate respectively

Substrate Pad Thickness (0.027mm), Substrate Pad Diameter (0.420mm)

SMD Thickness (0.030mm), SMD Diameter (0.270mm)

Ball Standoff (0.2500mm), Ball Diameter (0.4108mm)

PCB Pad Thickness (0.027mm), PCB Pad Diameter (0.270mm)

Figure 7 - Dimensional details of reflowed solder ball along with package and printed circuit board pads

Solder Ball Fatigue Models

Viscoplastic finite-element simulation methodologies were utilized to predict solder ball joint reliability of the same size stacked die chip scale package under accelerated temperature cycling conditions (-40C to +125C, 15min ramps/15min dwells). Due to the complex physics that encompass this type of non-linear transient finite element analysis, only a diagonal slice of the package was modeled in order to facilitate reasonable model run times. The utilization of a diagonal slice assures that a worst-case situation is simulated where the perimeter solder ball is the furthest distance from the package center neutral point. The diagonal slice is shown by the bold print dashed line in Fig. 1. Although this is not considered a perfect diagonal slice, it will provide results that are within the +/-2X published accuracy of Darveaux's methodology. The resulting diagonal slice model is shown in Fig's 8 and 9. The entire model utilized a mapped (or structured) finite element mesh that consisted of 6504 nodes and 4764 elements. Typical solution run times were 2 hours (Dual Processor, 800 MHz Pentium III, 1GByte RAM, NT Operating System).
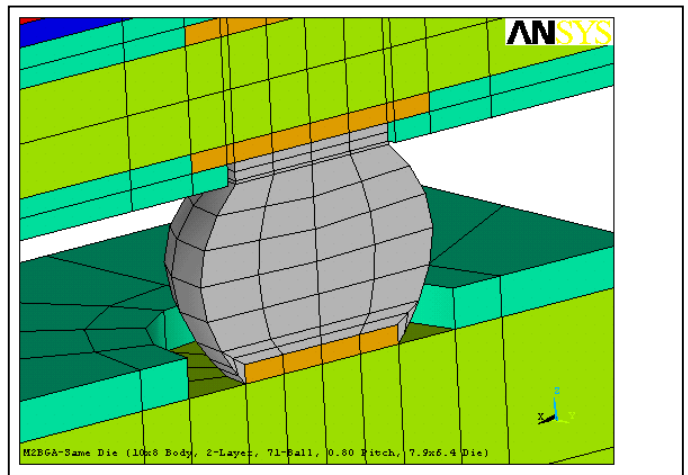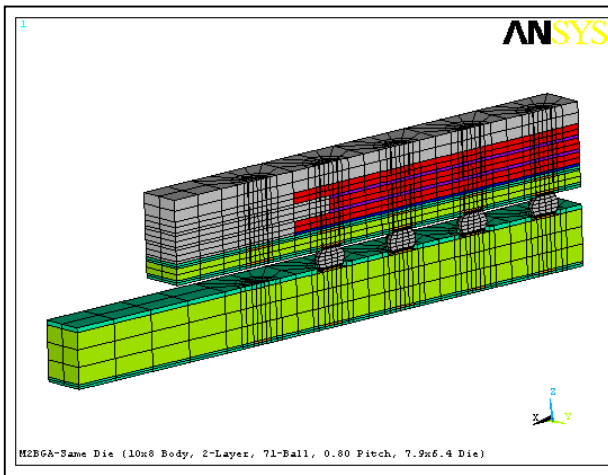
Figures 8 & 9 - Diagonal slice finite element model and resulting mesh

The diagonal slice model passes through the thickness of the package assembly, capturing all major components and a full set of solder joints. The use of a slice model involves a choice on the part of the analyst on the boundary constraints to be applied at the slice plane. The plane is neither a free surface nor a true symmetry plane. The reasonable compromise of coupling the y-displacements of the nodes on the slice plane was chosen. This has the effect that the slice plane is free to move in the y-direction, but that the surface is required to remain planar. Boundary constraints applied to a typical slice model are shown in Fig. 10. Note that for all analyses presented in this paper, the printed circuit board x-dimension (or length) was set at 1.25X that of the modeled package slice x-dimension. UX was not coupled at the printed circuit board +X vertical surface as shown in Fig. 10. Coupling this surface is a good choice if another package is assumed to exist adjacent to the modeled package. When assuming an adjacent package, the printed circuit board length should be set to extend one-half the distance between the modeled package and the assumed adjacent package. The y-dimension (or width) of the slice model is one-half the solder ball pitch. Note that for a diagonal slice model, the ball pitch is the hypotenuse (1.1314mm) of the true ball pitch (0.80mm) as is evident by the ball separation along the bold print dashed line in Fig. 1.
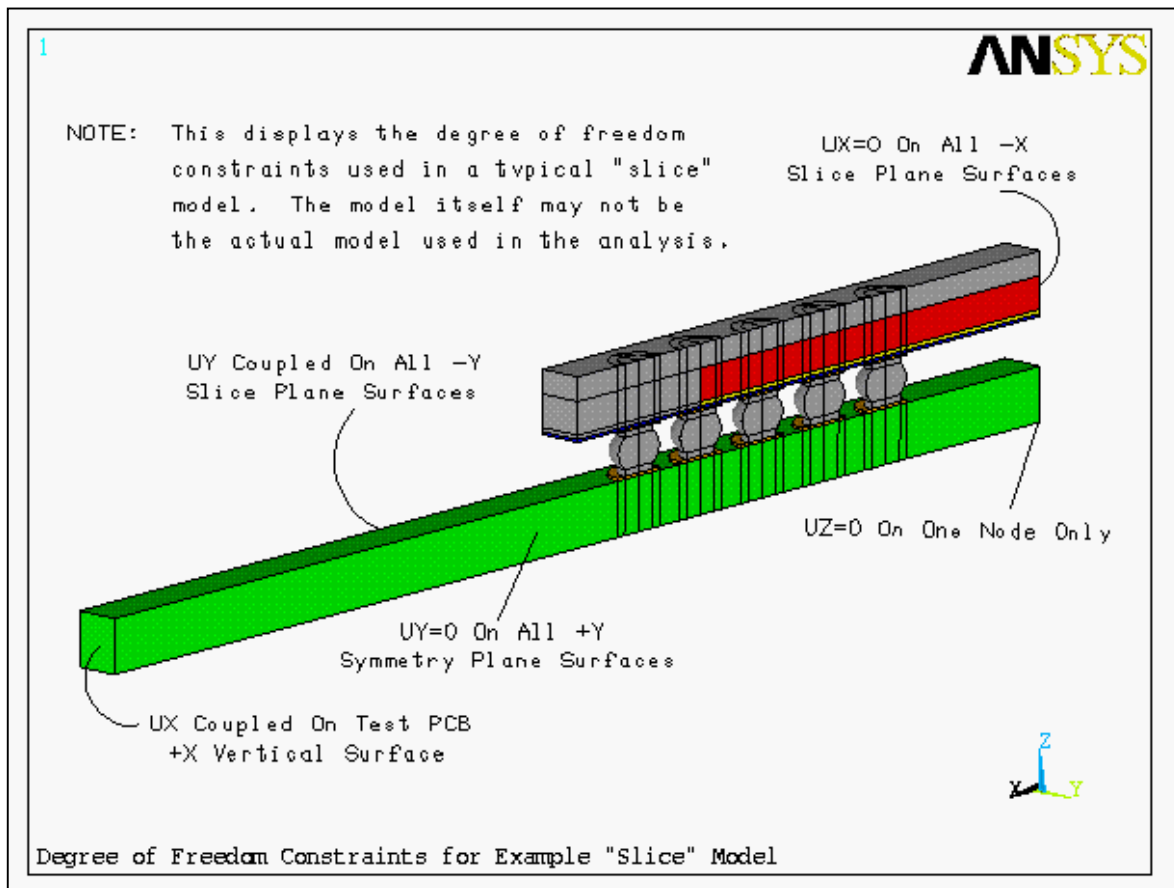
Figure 10 - Boundary constraints applied to a typical slice model.

Material Properties and Modified Anand Constants

Linear and non-linear, elastic and plastic, time and temperature independent and dependent material properties were incorporated in the finite element models as displayed in Tables 1 and 2. As an alternative to a rate-independent plasticity approach, Darveaux [11, 20] has presented solder constitutive relations based on Anand's [12] model for rate-dependent plasticity. Anand's constitutive model incorporates viscoplasticity, a time-dependent plasticity phenomenon, where the development of plastic strains is dependent on the rate of loading. Viscoplasticity is defined by unifying plasticity and creep. Anand's model does not consider rate-independent plasticity. Therefore, Darveaux modified the constants in Anand's constituitive relation to account for both time-dependent and time-independent phenomenon. These modified Anand constants are given in Table 3 [20]. Using ANSYS as the finite element analysis tool, the Anand plasticity data table was activated for the solder ball material and incorporated the constants as given in Table 3. Solder ball materials were meshed in ANSYS using the VISCO107 elements, whereas all other package materials were meshed using SOLID45 elements.

Solder Joint Fatigue Life Prediction Methodology

By measuring the crack growth rate of actual solder joints, Darveaux [20] was able to establish four crack growth correlation constants (K1 through K4) along with two equations by which finite element simulation results could be used to calculate thermal cycles to crack initiation along with crack propagation rate per thermal cycle. However, the methodology is sensitive to the finite element modeling procedure. First, care must be taken in controlling the element thickness at the interface between the eutectic solder and copper pad. Second, element volumetric averaging of the stabilized change in plastic work within this controlled eutectic solder element thickness must be used. This procedure reduces singularity issues whereby the size of the finite element mesh affects plastic work simulation results.

Although equation constants for varying interface element thicknesses are provided by Darveaux [20], the element interface thickness utilized by all models discussed herein was 0.0254mm (1mil). This thickness equates to the first two layers of solder ball material elements at the package substrate and printed circuit

board interface joints (see Fig. 9). It should also be noted that Darveaux's methodology requires that the solder ball and solder mask material elements not be joined in the finite element model. This is due to the non-adhesion between solder and mask materials. Given a solder mask defined solder joint at the package substrate, Darveaux recommends a 0.0127mm (0.5mil) gap between the solder ball and solder mask material in the finite element model. This gap is visible in Fig. 9. Corresponding K1 through K4 crack growth correlation constants for a 0.0254mm (1mil) solder joint element thickness are given in Table 4. The equations for the calculation of thermal cycles to crack initiation "N_o" and crack propagation rate per thermal cycle "da/dN" are shown below as (1) and (2) respectively.

$$N_o = K1 \left(\Delta W_{ave} \right)^{K2} \qquad (1)$$

$$\frac{da}{dN} = K3 \left(\Delta W_{ave} \right)^{K4} \qquad (2)$$

Where "ΔW_{ave}" is the element volumetric average of the stabilized change in plastic work within the controlled eutectic solder element thickness. The characteristic solder joint fatigue life "α" (number of cycles to 63.2% population failure) can then be calculated by summing the cycles to crack initiation with the number of cycles it takes for the crack to propagate across the entire solder joint diameter "a" as shown in equation (3).

$$\alpha = N_o + \frac{a}{da/dN} \qquad (3)$$

It should be noted that material intermetallic layers, along with intermetallic spikes directed perpendicular to the intermetallic layers, typically form at the solder pad / solder ball interfaces. The mechanical effects of these intermetallics on the fatigue life of the solder joints are not directly included in the finite element models. However, since the fatigue life prediction methodology developed by Darveaux was derived using measurement data taken from actual solder joints, which presumably contained similar intermetallic structures, their influence is believed to be indirectly incorporated into the predicted results.

ANSYS Solution Methodology

Once the slice model has been completed as displayed in Fig's 8 and 9, and the boundary constraints have been applied as indicated in Fig. 10, the ANSYS solution setup commands are as follows:

```
! SET SOLUTION OPTIONS
/solu                    ! enter soln processor
eqslv,pcg,1.0e-08        ! set solver and tollerance
antype,static,new        ! set analysis type
nlgeom,on                ! set large def and strain
nropt,auto,,off          ! set newton-raphson soln
outres,all,last          ! write data to .rst file
```

The thermal cycle temperature and time variables can be set in ANSYS using variable names and equations as follows:

! SET THERMAL CYCLE VARIABLES

hitmp=125+273   ! set hi cycle temp (K)

hirmp=15*60   ! set lo-hi ramp time (sec)

hidwl=15*60   ! set hi dwell time (sec)

lotmp=-40+273   ! set lo cycle temp (K)

lormp=15*60   ! set hi-lo ramp time (sec)

lodwl=15*60   ! set lo dwell time (sec)

delta=hitmp-lotmp   ! calc delta temp

rmpstp=delta/10   ! calc ramp substeps

Note that the analysis will use one substep for every 10 degrees K of temperature change in a thermal ramp load step as suggested by Darveaux [11] and as calculated by the variable "rmpstp" above.

Once the solution setup is complete two thermal cycles are simulated. The ANSYS zero strain reference temperature is set to the high temperature "hitmp" of the thermal cycle sequence. Each thermal cycle consists of four load steps (ramp low, dwell low, ramp high, and dwell high). Thus a complete simulation of two thermal cycles consists of eight load steps. Other publications that incorporate Darveaux's methodology have indicated the simulation of three thermal cycles (twelve load steps). However, it has been this authors experience that the difference in predicted fatigue life when simulating two thermal cycles, as opposed to three thermal cycles, has been less than 5% and in the conservative direction (i.e. a reduced number of predicted thermal cycles to failure). By only simulating two thermal cycles, simulation run times can be reduced by 30-35%.

The below sequence of ANSYS commands indicates the setting of the zero strain reference temperature along with those required for the first thermal cycle (i.e. first four load steps).

tref,hitmp   ! set zero strain temp

! RAMP LOW (LOAD STEP 1)

autots,off   ! turn off auto time step

nsubstp,rmpstp   ! set substeps

bf,all,temp,lotmp   ! apply temp to all nodes

kbc,0   ! linearly ramp loads

time,lormp   ! set time

solve   ! solve load step

! DWELL LOW (LOAD STEP 2)

autots,on   ! turn on auto time step

```
nsubstp,10,100,1          ! set substeps

bf,all,temp,lotmp         ! apply temp to all nodes

kbc,1                     ! maintain loads

time,lormp+lodwl          ! set time

solve                     ! solve load step
```

! RAMP HIGH (LOAD STEP 3)

```
autots,off                ! turn off auto time step

nsubstp,rmpstp            ! set substeps

bf,all,temp,hitmp         ! apply temp to all nodes

kbc,0                     ! linearly ramp loads

time,lormp+lodwl+hirmp    ! set time

solve                     ! solve load step
```

! DWELL HIGH (LOAD STEP 4)

```
autots,on                 ! turn on auto time step

nsubstp,10,100,1          ! set substeps

bf,all,temp,hitmp         ! apply temp to all nodes

kbc,1                     ! maintain loads

time,lormp+lodwl+hirmp+hidwl     ! set time

solve                     ! solve load step
```

To finish the simulation of the second thermal cycle, the above ANSYS command groups for load steps 1 through 4 are repeated. However, the "time" for load steps 5 through 8 must be adjusted appropriately.

Once two thermal cycles (eight load steps) have completed execution, it is necessary to obtain the ΔW_{ave} for the worst-case solder joint. The worst-case solder joint can be identified by plotting the nodal plastic work of the solder ball materials at the end of the eighth load step. Once the worst-case solder joint has been identified, only the 0.0254mm (1mil) thick layer of solder ball material elements at the joint interface are selected using the ANSYS ESEL (element select) command. The below sequence of ANSYS commands are then used to calculate ΔW_{ave}.

```
! CALC AVG PLASTIC WORK FOR CYCLE 1

set,4,last,1

etable,vtable,volu

etable,vsetable,nl,plwk

smult,pwtable,vtable,vsetable

ssum

*get,sumplwk,ssum,,item,pwtable

*get,sumvolu,ssum,,item,vtable
```

wavg1=sumplwk/sumvolu

! CALC AVG PLASTIC WORK FOR CYCLE 2

set,8,last,1

etable,vtable,volu

etable,vsetable,nl,plwk

smult,pwtable,vtable,vsetable

ssum

*get,sumplwk,ssum,,item,pwtable

*get,sumvolu,ssum,,item,vtable

wavg2=sumplwk/sumvolu

! CALC DELTA AVG PLASTIC WORK

dwavg=wavg2-wavg1

Since Darveaux provides crack growth correlation constants in English units, it is important to remember to convert the simulated ΔW_{ave} (ANSYS constant "dwavg") from units of MPa to units of psi by multiplying by 6.894757×10^{-3}. Also, the solder joint diameter should be converted from units of mm to units of inches by dividing by 25.4. These values can then be substituted into equations (1) through (3) to obtain cycles to crack initiation, crack propagation rate, and solder joint characteristic fatigue life respectively.

Fatigue Model Results

A total of eight package diagonal slice models were created to evaluate corresponding solder joint fatigue effects using multiple die attach material configurations while also varying the thickness of the mold cap and spacer die. Table 5 indicates the die attach material configurations investigated which consisted of standard conductive and non-conductive die attach materials along with an experimental epoxy film. The reader should reference Fig. 2 to identify the locations of the three die attach layers. Two variations of the spacer die and mold cap thickness were investigated using the same die attach material configurations as shown in Table 5. A spacer die thickness of 0.1397mm (5.5mil) had a corresponding mold cap thickness of 0.8mm. A spacer die thickness of 0.1143mm (4.5mil) resulted in a mold cap thickness of 0.7mm.

0.1397mm Spacer Die with 0.80mm Mold Cap

Table 6 indicates the detailed simulation results for the 0.1397mm (5.5mil) spacer die with 0.8mm mold cap thickness. The worst-case results are shown for the solder ball joints at the package substrate and printed circuit board. Note that for all die attach configuration options the first failure solder joint at both the package substrate and printed circuit board occurred at the outside solder ball (4th ball from model center). Simulation results indicate that the solder joint characteristic life is best when using die attach configuration option B (non-conductive die attach for all three layers) and worst when using option C (epoxy film die attach for all three layers). The package deformation trend at the maximum Δtemperature from the zero strain reference temperature is shown in Fig's 11 and 12. It is evident in these figures that the outside solder ball will absorb the bulk of the plastic strain. Another trend is evident in that the ends of the two active die (i.e. top and bottom die) are pushed in opposite directions away from the center spacer die due to the expansion of the mold cap material that fills the gap between these die. This trend may lead to wire bond separation failures during thermal cycling qualification.
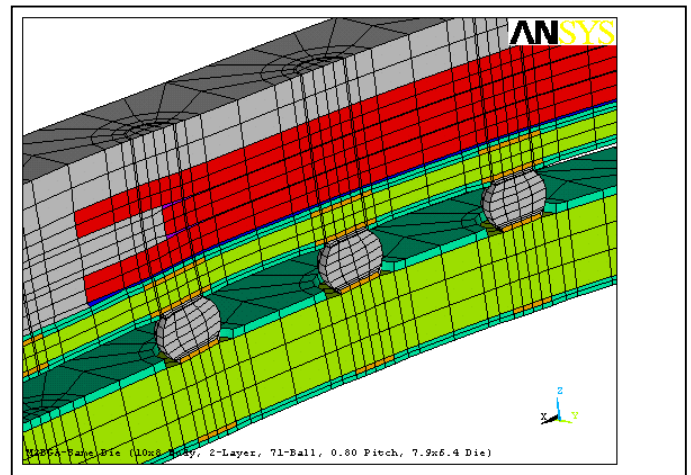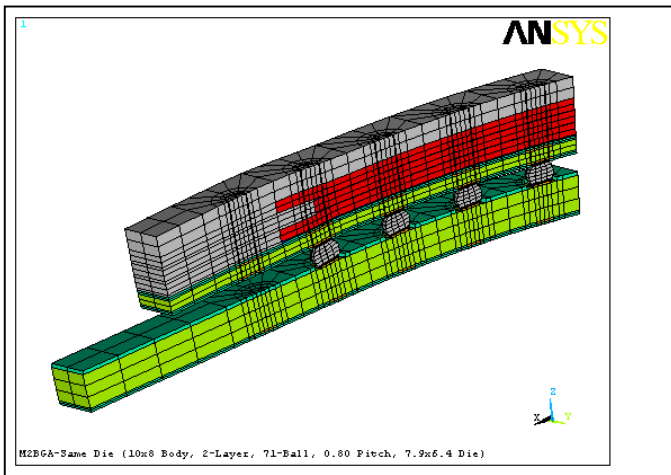
Figures 11 & 12 - **Package deformation trend at the maximum Δtemperature from the zero strain reference temperature.**

0.1143mm Spacer Die with 0.70mm Mold Cap

Table 7 indicates the detailed simulation results for the 0.1143mm (4.5mil) spacer die with 0.7mm mold cap thickness. The worst-case results are shown for the solder ball joints at the package substrate and printed circuit board. It is interesting to note that the first failure solder joint at the package substrate occurs in the 3rd ball from the model center for die attach configurations A and B as opposed to the outside solder ball as was the case for all die attach configurations in Table 6. The first failure solder joint at the printed circuit board occurs at the outside solder ball for all die attach configurations as was seen previously. The reduced mold cap and spacer die configuration has a dramatic effect on the fatigue life for both the package substrate and printed circuit board solder joints. The fatigue life of the package substrate solder joints increased by 95-108%, depending on the die attach configuration. The fatigue life of the printed circuit board solder joints increased by 82-86%. This dramatic improvement can be attributed to the packages increased flexibility, thus reducing the amount of plastic strain absorbed by the solder structures during accelerated temperature cycling.

Summary

A finite element analysis based methodology for estimating accelerated temperature cycling solder joint characteristic fatigue life has been applied to predict the reliability performance of a same die size, stacked, chip scale, ball grid array package. The method uses the ANSYS finite element analysis tool along with Anand's viscoplastic constitutive law. Darveaux's crack growth rate model was applied to calculate solder joint characteristic life using simulated viscoplastic strain energy density results at the package substrate and printed circuit board solder joints.

Four die attach material configurations were evaluated along with two mold cap and corresponding spacer die thicknesses. Simulations indicate die attach configuration B (non-conductive die attach for all three layers) provides the best solder joint characteristic fatigue life performance for both mold cap and spacer die thickness configurations. However, the 0.1143mm spacer die with the 0.7mm mold cap provides characteristic life results that are 82-108% greater than the 0.1397mm spacer die and 0.8mm mold cap. This dramatic improvement in solder joint characteristic fatigue life is believed to be due to the increased flexibility of the thinner package thus reducing the amount of plastic strain absorbed by the solder structures.

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Tables

Table 1. Model Material Properties.

Component (Material)	Elastic Moduli (MPa)	Shear Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)
Ball (63Sn37Pb)	75842-152T	-	24.5×10^{-6}	0.35
Conductive Attach (Proprietary)	See Table 2	-	See Table 2	0.35
Chip (Silicon)	162716	-	$-5.88 \times 10^{-6} + 6.26 \times 10^{-8}T$ $-1.6 \times 10^{-10}T^2 + 1.5 \times 10^{-13}T^3$	0.28
Conductor (Copper)	128932	-	$13.8 \times 10^{-6} + 9.44 \times 10^{-9}T$	0.34
Epoxy Film (Proprietary)	2230-5.27T	-	$41 \times 10^{-6} < T_g, 288K$ $110 \times 10^{-6} >/= T_g, 288K$	0.35
Mold Cap (Mold)	15513	-	15.0×10^{-6}	0.25
Non-Conductive Attach (Proprietary)	See Table 2	-	See Table 2	0.35
PCB Core (FR4)	27924-37T (XY) 12204-16T (Z)	12600-16.7T (XY) 5500-7.3T (YZ & XZ)	16.0×10^{-6} (XY) 84.0×10^{-6} (Z)	0.39 (XZ & YZ) 0.11 (XY)
PCB Mask (Dry Film)	4137	-	30.0×10^{-6}	0.40
Substrate Core (BT)	24132	-	16.0×10^{-6} (XY) 35.0×10^{-6} (Z)	0.30
Substrate Mask (Dry Film)	4137	-	30.0×10^{-6}	0.40

T is Material Property Temperature in Kelvin

T_g is Material Glass Transition Temperature in Kelvin

Table 2. Conductive and Non-Conductive Die Attach Material Properties.

Conductive Die Attach				Non-Conductive Die Attach			
Temp (K)	Elastic Moduli (MPa)	Temp (K)	CTE (1/K)	Temp (K)	Elastic Moduli (MPa)	Temp (K)	CTE (1/K)
223	3557	233	7.4×10^{-5}	198	3844	233	1.09×10^{-4}
298	2758	296	7.5×10^{-5}	298	866	268	1.10×10^{-4}

423	151	306	1.0×10^{-4}	423	125	278	1.30×10^{-4}
523	144	311	1.09×10^{-4}	523	119	283	1.40×10^{-4}
		316	1.19×10^{-4}			288	1.50×10^{-4}
		326	1.43×10^{-4}			298	1.69×10^{-4}
		473	1.44×10^{-4}			473	1.70×10^{-4}

Table 3. Darveaux Modified Anand Constants [11, 20].

Constant	Parameter	Value	Definition
C1	S_o (MPa)	12.41	Initial Value of Deformation Resistance
C2	Q/R (1/Kelvin)	9400	Activation Energy/Boltzmann's Constant
C3	A (1/sec)	4.0E-06	Pre-Exponential Factor
C4	ξ (dimensionless)	1.5	Multiplier of Stress
C5	m (dimensionless)	0.303	Strain Rate Sensitivity of Stress
C6	h_o (MPa)	1378.95	Hardening Constant
C7	s (MPa)	13.79	Coeff. of Deformation Resistance Saturation Value
C8	n (dimensionless)	0.07	Deformation Resistance Value
C9	a (dimensionless)	1.3	Strain Rate Sensitivity of Hardening

Table 4. Darveaux K1 through K4 Crack Growth Correlation Constants [20].

Constant	Value
K1	22400 cycles/psi
K2	-1.52
K3	5.86×10^{-7} in/cycle/psi
K4	0.98

Table 5. Die Attach Configuration Options.

Configuration Option	1st Die Attach	2nd Die Attach	3rd Die Attach
Option A	Conductive	Non-Conductive	Non-Conductive
Option B	Non-Conductive	Non-Conductive	Non-Conductive
Option C	Film	Film	Film

Option D	Conductive	Film	Film

Table 6. Detailed Simulation Results – 0.1397mm (5.5mil) Spacer and 0.80mm Mold Cap.

Data Description	Option A	Option B	Option C	Option D
Ball/Substrate Solder Joint				
Failure Joint (From Center)	4	4	4	4
Delta Plastic Work/Cycle (MPa)	0.2429E+00	0.2324E+00	0.3660E+00	0.3276E+00
Delta Plastic Work/Cycle (psi)	35.23	33.71	53.09	47.51
Crack Initiation (cycles)	100	107	53	63
Crack Growth Rate (mm/cycle)	0.4883E-03	0.4677E-03	0.7298E-03	0.6547E-03
Solder Joint Diameter (mm)	0.2700	0.2700	0.2700	0.2700
Crack Propagation (cycles)	553	577	370	412
Characteristic Life (cycles)	653	684	423	476
Ball/Test Board Solder Joint				
Failure Joint (From Center)	4	4	4	4
Delta Plastic Work/Cycle (MPa)	0.7286E-01	0.7002E-01	0.9438E-01	0.8483E-01
Delta Plastic Work/Cycle (psi)	10.57	10.16	13.69	12.30
Crack Initiation (cycles)	622	661	420	494
Crack Growth Rate (mm/cycle)	0.1501E-03	0.1443E-03	0.1934E-03	0.1742E-03
Solder Joint Diameter (mm)	0.2700	0.2700	0.2700	0.2700
Crack Propagation (cycles)	1799	1871	1396	1550

Characteristic Life (cycles)	2421	2532	1816	2044
Model Size and Run Time Info.				
Total Model Nodes	6504	6504	6504	6504
Total Model Elements	4764	4764	4764	4764
CPU Run Time (Hrs)	1.95	1.97	2.06	1.99

Table 7. Detailed Simulation Results – 0.1143mm (4.5mil) Spacer and 0.70mm Mold Cap.

Data Description	Option A	Option B	Option C	Option D
Ball/Substrate Solder Joint				

Failure Joint (From Center)	3	3	4	4
Delta Plastic Work/Cycle (MPa)	0.1231E+00	0.1212E+00	0.1953E+00	0.1682E+00
Delta Plastic Work/Cycle (psi)	17.86	17.58	28.32	24.40
Crack Initiation (cycles)	280	287	139	174
Crack Growth Rate (mm/cycle)	0.2509E-03	0.2471E-03	0.3943E-03	0.3407E-03
Solder Joint Diameter (mm)	0.2700	0.2700	0.2700	0.2700
Crack Propagation (cycles)	1076	1093	685	793
Characteristic Life (cycles)	1356	1379	824	967
Ball/Test Board Solder Joint				
Failure Joint (From Center)	4	4	4	4
Delta Plastic Work/Cycle (MPa)	0.4244E-01	0.4113E-01	0.5435E-01	0.4912E-01
Delta Plastic Work/Cycle (psi)	6.15	6.00	7.88	7.12
Crack Initiation (cycles)	1415	1472	971	1133
Crack Growth Rate (mm/cycle)	0.8834E-04	0.8609E-04	0.1126E-03	0.1020E-03
Solder Joint Diameter (mm)	0.2700	0.2700	0.2700	0.2700
Crack Propagation (cycles)	3056	3136	2398	2648
Characteristic Life (cycles)	4471	4608	3370	3781
Model Size and Run Time Info.				
Total Model Nodes	6504	6504	6504	6504
Total Model Elements	4764	4764	4764	4764
CPU Run Time	1.88	1.93	2.02	1.99