Flip Chip Reliability Modeling Based on Solder Fatigue as Applied to Flip Chip on Laminate Assemblies

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Abstract

In order to successfully implement reliable flip chip packaging technology it is desirable to ensure solder fatigue as the limiting mechanical failure mechanism. Doing so enables the packaging engineer to design to specific reliability standards, as solder fatigue is a known and predictable failure mechanism. Indeed, other flip chip failure modes such as silicon fracture and underfill delamination are ill-defined in terms of practical failure models, and often lead to unpredictable and early reliability failures.

Solder fatigue models can serve as valuable tools in predicting and maintaining solder fatigue as a failure mode throughout all stages of flip chip design, qualification and implementation into a production application. A 63Sn/Pb solder fatigue model has been previously developed based on a correlation of flip chip solder fatigue data combined with nonlinear finite element analysis. This model has been successfully applied in the prediction of PBGA and CSP fatigue lives as well as a parametric study investigating the reliability of flip chip assemblies and the influence of specific design parameters. In this investigation, flip chip reliability predictions are generated based on solder fatigue modeling and compared to actual thermal cycling reliability data. The influence of both solder fatigue and underfill delamination are considered in interpretation of the experimental data.

Key words: flip chip, underfill, organic circuit board, solder fatigue, finite element analysis, reliability.

Introduction

The mechanical reliability of flip chip devices assembled to ceramic substrates has historically been limited by solder fatigue due to thermal stresses generated by coefficient of thermal expansion (CTE) mismatch of adjoined materials. In recent years, greater demands placed on the electrical performance of flip chips combined with lower cost requirements have spurned the growth in interest of flip chip on laminate technology. While the advent of underfill has enabled the production of reliable flip chip on laminate assemblies, it has further increased the importance in understanding the role of underfill and the interaction it can have on failure modes beyond solder fatigue. The underfill encapsulant acts as a bridge or constraint between the die and substrate, and significantly reduces the amount of relative displacement and corresponding stress within the flip chip solder joints. However, the interaction of the underfill and the substrate may introduce new failure modes which could lead to early failures of flip chip assemblies.

For example, while the use of underfill may significantly increase fatigue life, methods of applying and curing underfill have the residual effect of causing bending within the flip chip assembly. The assembly is essentially in a stress-free state during underfill cure (typically 150°C) due to the plasticity of the solder. However, CTE mismatch between the die, underfill and substrate generates bending as the assembly cools. The backside of the die is then in a state of tension, leaving it susceptible to brittle fracture [1]. Similarly, the underfill itself may fail in the form of delamination. Underfill delamination failures may occur at the substrate interface as well as the die interface. In both cases, interfacial cracks grow over time, eventually propagating through an interconnect. While underfill delamination is a commonly observed flip chip failure mode, it is not a well-understood failure mechanism. As such, few models exist which attempt to describe

such a phenomena. Those that do are either overly simplistic (such as those comparing lap shear data to interfacial shear stress), or require extensive and thorough experimentation (e.g., interfacial fracture models). To date, underfill delamination is best quantified through well thought out design of experiments.

In contrast to underfill delamination, solder fatigue is a relatively well-understood and repeatable failure mechanism. Furthermore, models exist which can accurately predict the solder fatigue life of a given flip chip assembly (for example, see [2]). Hence, solder fatigue as a failure mechanism can be controlled. With the advent of underfill, solder fatigue lives can be extended to satisfy most reliability requirements. The key to a reliable flip chip assembly, then, is to promote design, material and process decisions which eliminate delamination and maximize fatigue life. Doing so allows for solder fatigue modeling to take a more prominent role in the design of a flip chip system. For instance, reliability predictions may be easily generated during the design phase of a flip chip application subjected to a variety of thermal profiles. Design modifications may then be investigated to determine an optimum materials set.

Of course, all reliability modeling must go hand in hand with experimental confirmation whenever possible. The following paper demonstrates how solder fatigue modeling may be used to predict reliability of flip chip on laminate assemblies as well as aid in interpreting experimental results. Reliability predictions are generated for four different assemblies subjected to thermal cycling. The results are then compared to actual thermal cycling failure data.

63Sn/Pb Solder Fatigue Model

The 63Sn/Pb solder fatigue model employed in this study was first introduced by Popelar in [2], and subsequently applied to parametric studies of flip chip on ceramic and organic substrates in [2] and [3], respectively. Fundamentally, the solder fatigue model correlates the amount of creep strain energy dissipated per thermal cycle with the characteristic Weibull life of the critical solder joint. This correlation is depicted in Figure 1, along with a power law fit to the data. Each data point represents an experimentally measured fatigue life of either a flip chip, PBGA or CSP device. The data represents assemblies to ceramic and organic substrates, with and without underfill, for various flip chip sizes, designs and solder joint geometries. The data also represents thermal profiles ranging from 0/100°C, 20 minute cycles, to –50 to 150°C, 80 minute cycles.

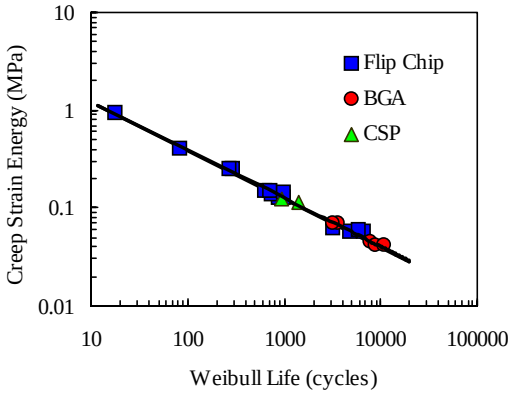


Figure 1. 63Sn/Pb solder fatigue correlation [1].

For each data point shown in Figure 1, a two-dimensional plane strain finite element model has been generated for the flip chip assembly and analyzed using the ANSYS™ general purpose finite element software. The model represents a cross-section of the assembly from the center of the die to the corner-most bump. All materials in the model are assumed to behave linearly with the exception of the solder. As such, only the elastic modulus, CTE and Poisson's ratio are required to analyze the models. For the solder, however, a creep constitutive equation is also required which correlates the steady-state creep strain rate $d\varepsilon_{cr}/dt$ of the solder with temperature and the applied stress σ. From each finite element model, a corresponding creep hysteresis curve is generated from which the amount of creep strain energy dissipated per thermal cycle may be calculated. The power law fit of Figure 1, then, defines the correlation between dissipated creep energy and the characteristic Weibull life. Based on this fit, the solder fatigue model may be expressed as [2]

$$W_{cr} = 3.86 N_f^{-0.495} \qquad (1)$$

where W_{cr} is the creep energy dissipated per thermal cycle (in MPa), and N_f is the Weibull life. For a given flip chip application subjected to a specific thermal profile, the amount of creep energy dissipated may be determined using finite element analysis, and Equation (1) may then be employed to accurately determine the fatigue life of the system.

Recall that the two-parameter Weibull distribution has the form [4]

$$F(x) = 1 - e^{-(x/\theta)^{\beta}} \qquad (2)$$

where F(x) is the probability of failure at x number of cycles, β is the shape parameter or Weibull slope, and θ is the characteristic Weibull life. By definition, the Weibull life defines the number of cycles where 63.2 percent of the parts have failed. For solder fatigue the Weibull slope may be estimated as 6. Hence, for a given flip assembly and thermal profile, the Weibull life may be predicted using Equation (1) and reliability predictions may be made using Equation (2).

It is important to note that the fatigue life correlation of Figure 1 is very strong throughout the range of measured fatigue lives. Predicted fatigue lives typically fall within 15 percent of measured lives, which is of the same order of magnitude of the variation seem among experimental results. Note also that the correlation is just as strong for flip chips with underfill as it is for flip chips without. Without underfill, the solder joint loading is dominated by shear loads, with little contribution attributed to tensile loading. With underfill, contributions from shear and tensile loads are of the same order of magnitude. The fact that the model can accommodate both of these extreme loading conditions is a strong indicator as to the validity of the fatigue model.

Table 1. Summary of PBGA and CSP results.

Device Type	Thermal Profile	Measured Life	Predicted Life
BGA1	–40/125°C	7682	8100
BGA2	–40/125°C	3534	3260
BGA2	–40/125°C	3207	3260
BGA2	0/100°C	8924	8940
BGA2	0/100°C	10,675	8940
CSP1	–40/125°C	960	1060
CSP2	–40/125°C	1389	1220

Because the original solder fatigue model, and indeed the correlation expressed in Figure 1, is based exclusively on experimentally measured flip chip fatigue lives, it is entirely possible that the model is a characteristic of the solder joint, and not the solder itself. Hence data has been gathered for PBGA [5,6] as well as CSP assemblies [7]. Seven such assemblies have been analyzed and included in Figure 1 to determine how well the fatigue model performs when applied to devices other than flip chips. The results are summarized in Table 1 and show that the model is accurate for PBGA and CSP sized solder joints. Thus the model has been verified as a characteristic of the solder joint itself, independent of solder joint geometry. The PBGA data also expands the working range of the model to beyond 10,000 cycles.

Flip Chip Test Vehicle

The following experimental test vehicle and subsequent reliability data was first presented by Roech et al. in [8] and [9]. The test vehicle and matching substrate have been developed by the Hewlett-Packard Company as a means to investigate thermal cycling reliability. The test die consist of 8 mm daisy chain die stepped and repeated across a wafer. Based on how the wafer is diced, 8, 16 and 24 mm die can be constructed.

Two different substrate types were employed: one which was glass reinforced, and one which was reinforced by aramid fiber. The construction of the substrates is shown in Figure 2. The figure shows only half of the cross-section. The reinforced core was covered with a non-reinforced micro via layer. The wiring was done mainly on the second layer of the board. All connections to the flip chip were made directly through via-in-pad locations connected to the second layer of the board, avoiding any need for solder mask, and therefore maximizing the height of the gap which the underfill must fill. No copper traces were located under the die.

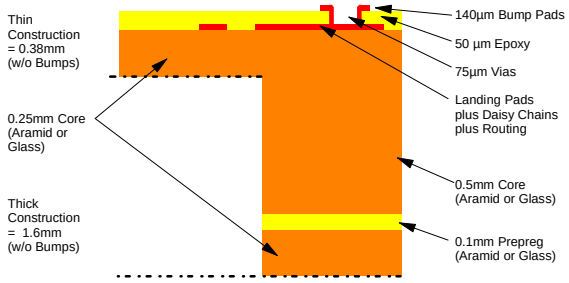


Figure 2. Schematic cross section of substrate construction [8].

The via-in-pad locations consisted of 75 µm vias and capture pads of 140 µm in diameter, leaving a 25 µm annular ring around the via itself. Exposed metallization was manufactured with organic coating (OCC).

Since the die were bumped with 95Pb/Sn solder, a process was developed to provide a flattened 63Sn/Pb eutectic cap on the via-in-pad locations. Only the eutectic cap was reflowed during assembly.

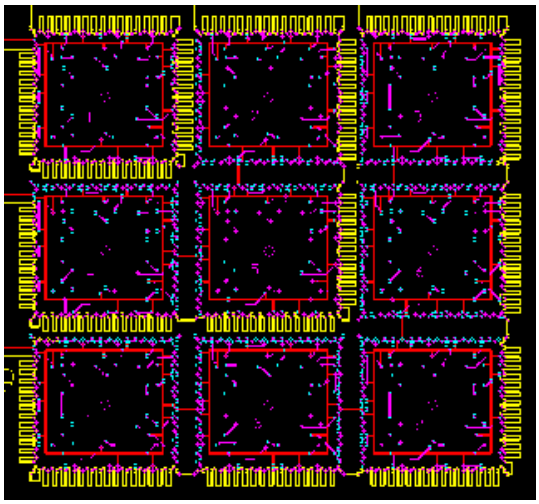


Figure 3. Wiring diagram of test substrate [8].

The wiring pattern for the substrate is shown in Figure 3. This pattern allowed one substrate to be used with three different die sizes. An 8 mm die can be mounted on the upper left location, a 16 mm die across the 4 upper left locations, and a 24 mm die across all 9 locations.

Substrates of 0.38 and 1.6 mm thicknesses were constructed for both the glass and aramid reinforced configurations. CTE measurements were taken via Moire interferometry in both the x and y directions, the results of which are shown in Table 2. The glass reinforced substrates showed a higher CTE than the aramid reinforced. Note also that the CTE measurements are higher in the 0.38 mm substrates. This is consistent with higher resin to reinforcement ratios in these constructions.

Table 2. Summary of CTE measurements.

Construction	CTEx (ppm/C)	CTEy (ppm/C)
Non-woven/Aramid/1.6 mm	9	8
Non-woven/Aramid/0.38 mm	13	12
Woven/Glass/1.6 mm	18	18
Woven/Glass/0.38 mm	24	25

All parts were assembled using standard flip chip placement equipment and a standard reflow profile for eutectic solder. An aqueous flux was employed which required a cleaning process after reflow. Before underfill, all parts were dried for one hour to remove excess moisture. Underfill application was performed at 100°C and cured for one hour at 150°C.

Test Procedure

A total of four combinations of substrate constructions and dies sizes will be reported on, as described in Table 3. Each cell consisted of 32 assemblies, 28 of which were subjected to thermal cycling under continuous electrical monitoring. Remaining assemblies were also thermally cycled, but removed from the chamber in weekly intervals for delamination inspection via C-mode scanning acoustic microscopy (CSAM).

The thermal profile employed in this investigation consisted of a –20/110°C profile with a 5 minute dwell at -20°C, 12 minute ramps and a 20 minute dwell at 110°C. The cycle period is 49 minutes. Each part was scanned a minimum of 60 times per cycle. The cycle number, part number, maximum resistance and temperature at which the maximum resistance occurred were recorded. The failure criterion for all parts was defined as a 5 percent deviation in maximum resistance.

Table 3. Summary of experimental test matrix.

Cell No.	Substrate Thick. (mm)	Substrate Construction	Die Size (mm)
13	1.6	Aramid	16
15	0.38	Glass	16
1	0.38	Aramid	24
6	1.6	Glass	24

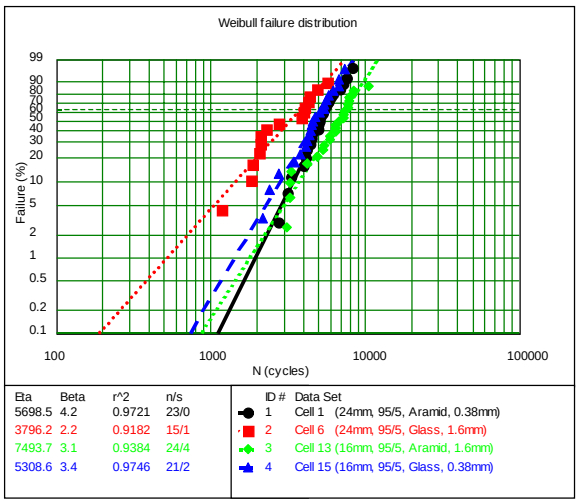


Figure 4. Weibull failure distributions [8].

Experimental Results

A detailed description and analysis of the failure distributions and failure mechanisms observed

during the thermal cycling tests were first presented by Roesch et al. in [8] and [9]. Figure 4 shows the failure distributions of the four cells while Table 4 summarizes the corresponding Weibull slopes and lives.

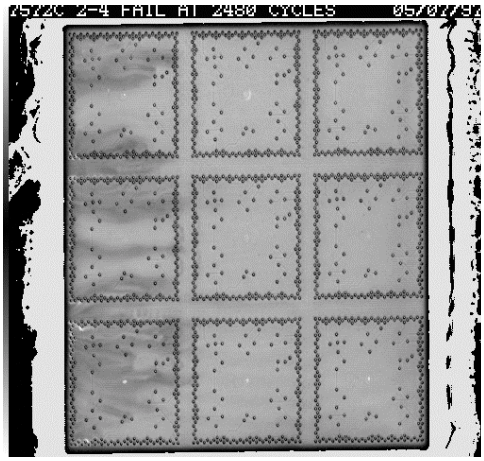
Table 4. Summary of Weibull statistics.

Cell No.	Weibull Life	Weibull Slope	R^2
13	7494	3.1	0.9384
15	5309	3.4	0.9746
1	5699	4.2	0.9721
6	3796	2.2	0.9182

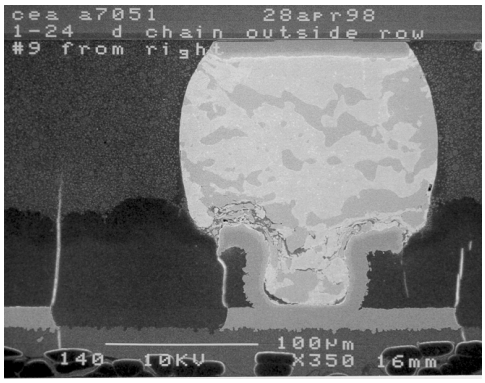
Analyses of the failed devices yielded two separate failure mechanisms. The predominant failure mechanism observed was solder fatigue within the eutectic cap. An example of this mechanism is depicted in Figure 5. Figure 5a shows a CSAM which reveals no underfill delamination. Figure 5b shows the corresponding failed bump with a fatigue crack extending through the eutectic cap. Noting that the fatigue resistance of 95Pb/Sn is greater than that of eutectic solder, it is interesting that the fatigue crack did indeed travel through the path of least resistance.

The second failure mechanism observed was underfill delamination at the die/underfill interface, as shown in Figure 6. Note the white region of the CSAM in Figure 6a which indicates delamination. Correlating bump failures were due to the direct continuation of the delamination between the die and underfill as shown in Figure 6b. In essence, interfacial crack growth at the die/underfill interface resulted in delamination where the crack simply propagated through all solder joints in its path.

While the majority of the failures were due to solder fatigue, the Weibull data of Table 4 considers delamination failure modes as well. This leads to Weibull slopes less than the typical value of 6 seen for solder fatigue alone, an indicator of mixed failure modes. Though the early failures due to delamination tend to skew the Weibull slope, it is felt that enough solder fatigue data exists in cells 13, 15 and 1 such that the corresponding Weibull lives are representative of fatigue lives. This conclusion is based in part on the shape of the Weibull curves as well as the corresponding failure distributions. However, it is not felt that the Weibull data of Cell 6 satisfactorily represents a solder fatigue failure mechanism. Indeed, the shape of the Weibull curve yields a bimodal distribution indicating a significant number of early failures due to delamination.



(a)

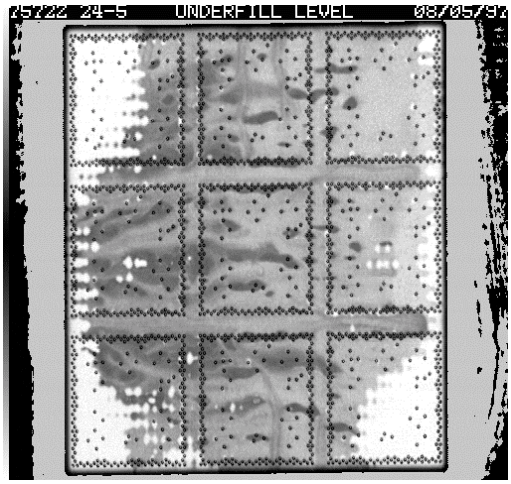


(b)

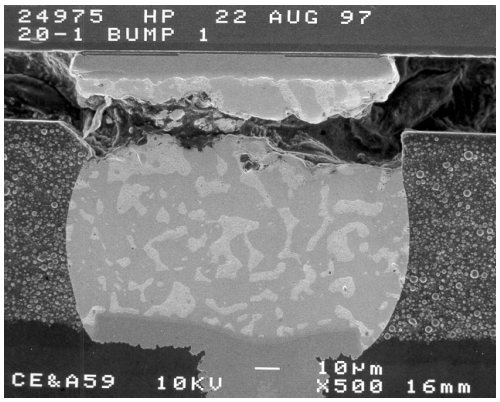
Figure 5. Solder fatigue failure mechanism [9]. (a) CSAM showing no delamination. (b) Fatigue of eutectic solder cap.

Modeling Results

A finite element model was generated for each of the four flip chip assemblies described in Table 3. The substrate properties used in the model are as defined in Table 2, while the material properties of the underfill were measured at Hewlett-Packard. Figure 7 depicts a typical finite element model, showing a magnified view of the solder joint geometry employed. From the finite element analyses, corresponding fatigue lives were predicted using the methodology described above. Table 5 compares the predicted Weibull lives with measured. Note that in some cases the predicted fatigue life matches very well with the measured life while in other cases it does not. The source of error is believed to be due to the delamination failures which exist in the experimentally measured lives but which are not accounted for in the predicted fatigue lives.



(a)



(b)

Figure 6. Underfill delamination failure mechanism [9]. (a) CSAM showing delamination (white region). (b) Interfacial delamination propagating through a solder joint.

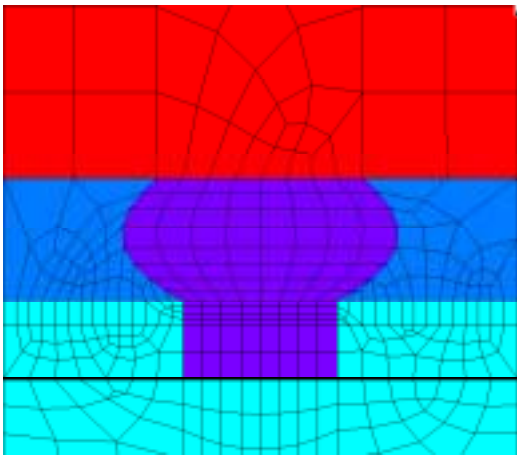


Figure 7. Typical finite element model.

Table 5. Predicted and measured Weibull lives.

Cell No.	Measured Life	Predicted Life	%
13	7494	7310	2.5
15	5309	5050	4.9
1	5699	7590	33.1
6	3796	5840	53.8

Based on the predicted fatigue lives, the variable with the most influence on fatigue life is substrate material. Namely, the aramid reinforced substrates (Cells 13 and 1) yield higher predicted fatigue lives than the glass reinforced substrates (Cells 15 and 6), a direct result of CTE differences between the two materials. The aramid reinforced substrates have less of a CTE mismatch with the silicon than do the glass reinforced substrates. Hence they yield a greater fatigue life. Beyond that, substrate thickness and die size are second order effects. This is consistent with earlier modeling results reported by Popelar [2, 3]. In general, flexing of a flip chip assembly will increase fatigue life because the flexing will dissipate energy which would otherwise be absorbed by the solder joints. Increasing substrate thickness will increase the effective stiffness of the assembly, reducing the amount of flexure. The result is a decrease in fatigue life. For the present study, the change in substrate thickness results in a small change in stiffness relative to the silicon die. Hence there is a relatively small change in fatigue life from one substrate thickness to another. Presumably the substrate thickness could be decreased to the point where a significant change in the stiffness of the assembly is incurred, resulting in a corresponding significant change in fatigue life.

Once Weibull slopes and lives have been defined, reliability predictions are readily made using Equation (2). For example, Table 6 compares first failure predictions based on experimentally generated Weibull distributions and those generated through solder fatigue modeling. Specifically, the first failures listed in Table 6 correspond to a 90 percent probability that no parts will fail before the life listed. Note that a Weibull slope of 6 has been assumed for the solder fatigue modeling predictions.

The results in Table 6 magnify the effect of delamination on reliability. This is due in part to the effect delamination has on Weibull life. More importantly, though, for the prediction of first failures, the effect of delamination serves to lower the Weibull slope, significantly reducing the probability of a device surviving a given amount of thermal cycles. In other words, the presence of underfill

delamination increases the probability of a premature first failure. Hence, as an exclusive failure mechanism, solder fatigue is far more attractive compared to underfill delamination.

Table 6. Comparison of predicted first failures.

Cell No.	First Failure (Measured)	First Failure (Modeling)	%
13	3630	5020	38.3
15	2740	3470	26.6
1	3340	5210	56.0
6	1370	4010	192.7
Based on a 90 percent probability.			

Conclusions

A previously validated solder fatigue model has been employed in evaluating and predicting the reliability of four separate flip chip assemblies subjected to thermal cycling. Both experimental and modeling results demonstrate the effect that underfill delamination has on flip chip reliability. In particular, the results show that while mixed mode failure mechanisms may yield acceptable Weibull lives, the presence of underfill delamination has adverse effects on first failures. In other words, delamination can lead to premature failure while solder fatigue can provide a consistent and repeatable failure free life.

In cases where solder fatigue was the predominant failure mode, the fatigue model accurately predicted corresponding Weibull lives. However, because the model does not consider underfill delamination, accurate Weibull lives were not predicted for experimental cells containing significant delamination failures. As such, the discrepancy between predicted and measured fatigue lives can serve as a valuable indicator of mixed failure modes.

Acknowledgments

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