IMPACT OF BALL VIA CONFIGURATIONS ON SOLDER JOINT RELIABILITY IN TAPE BASED CHIP-SCALE PACKAGES

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ABSTRACT

Three-dimensional finite element analysis has been applied to determine the time-dependent solder joint fatigue response of a tape based chip-scale package under accelerated temperature cycling conditions (-40C to +125C, 15min ramps/15min dwells). The effects of differing ball via configurations due to variations in both package assembly and tape vendors were investigated, including the use of punched, etched, laser etched, and enhanced re-flow pad area vias. The solder structures accommodate the bulk of the plastic strain that is generated during accelerated temperature cycling due to the thermal expansion mismatch between the various materials that encompass the chip-scale package. Since plastic strain is a dominant parameter that influences low-cycle fatigue, it was used as a basis for evaluation of solder joint structural integrity. An extensively published and correlated solder joint fatigue life prediction methodology was incorporated by which finite element simulation results were translated into estimated cycles to failure. This study discusses the analysis methodologies as implemented in the ANSYS finite element simulation software tool and the corresponding results for the solder joint fatigue life. Some ANSYS parametric design language commands are included for the benefit of those readers who are familiar with the tool.

Index Terms – chip-scale package, ball grid array package, solder fatigue, finite element modeling.

1. INTRODUCTION

As the demand for smaller, lighter, and more portable consumer electronics increases, more effort is focused on the development of chip-scale packages. Typically, a chip-scale package is defined as one in which the package footprint is within 20% of the size of the die in which it encompasses. The advantage of such a package is that it offers considerable space savings over the traditional full-sized ball grid array or lead-frame package. Furthermore, chip-scale packaging technology offers many of the benefits of known-good-die while also employing much of the previously established manufacturing infrastructure.

Many different chip-scale packaging technologies exist which can further be divided into the following four categories depending on the substrate structure: (1) Flex or Tape; (2) Rigid (i.e. laminate or ceramic); (3) Lead-Frame; and, (4) Wafer Level. For the purposes of this study, only the “flex or tape” based chip-scale package category was investigated.

The effect of temperature cycling on the reliability of microelectronic packages has been the subject of many studies. Because of the difference in the thermal expansion of the multiple materials involved in the construction of a typical package, temperature variations create a mismatch ultimately resulting in solder joint stress. Repeated application of this stress eventually causes solder joint failure, a mechanism commonly known as low cycle fatigue.

To minimize development costs and maximize reliability performance, advanced analysis is a necessity during the design and development phase of a microelectronic package. Analytical computer simulation such as finite element analysis can provide a very detailed description of solder stress/strain distribution and history under a variety of loading conditions, and is a powerful tool for performing design optimization and parametric studies. However, the analyst is typically interested in the cycles to failure that a package design configuration and cyclic loading condition will cause. This requires the utilization of a life prediction methodology in which data typically provided by a finite element solution can be translated into cycles to solder joint failure.

Several finite element based analysis methodologies have been proposed which predict solder joint fatigue life (e.g. Engelmaier [1]; Shine and Fox [2]; Wong et al. [3]; Yamada [4]; Subrahmanyan et al. [5]; Dasgupta et al. [6]; Pao [7]; Clech et al. [8]; Syed [9]; Darveaux et al. [10]; and Darveaux [11]). It should be noted that there is a material limitation inherent to many of these methodologies since they assume the utilization of eutectic 63Sn/37Pb solder or some similar

combination of solder materials (i.e. 62Sn/36Pb/2Ag). Life prediction methodologies for high temperature solder (90Pb/10Sn, 95Pb/5Sn, etc.) or future lead-free based interconnect materials, are almost non-existent due to their low volume use or relative infancy in today's microelectronics packaging industry.

Of all these methodologies, Darveaux's seems to be the most popular due to the ease in its implementation. Darveaux's methodology links laboratory measurements of low-cycle fatigue crack initiation and crack growth rates to the inelastic work of the solder. It is a strain energy based approach, where the work term consists of time-dependent creep and time-independent plasticity. This inelastic behavior is captured in ANSYS using Anand's constitutive model [12]. The modeling methodology utilizes finite element analysis to calculate the viscoplastic strain energy density accumulated per cycle during thermal or power cycling. The strain energy density is then utilized with crack growth data to calculate the number of cycles to initiate a crack, and the number of cycles for the crack to propagate across a solder joints diameter.

Darveaux's methodology has been previously presented in the successful analyses of various electronic assemblies from multiple industry sources (e.g. Amagai [13]; Fusaro and Darveaux [14]; Dougherty et al. [15]; Johnson [16]; and Zahn [17]). Recently, Zahn [18] and Goetz and Zahn [19] extended the methodology to predict both solder ball and solder bump reliability of a multi-chip silicon based system-in-package. In many of these publications, the authors have presented reliability test data that validates the accuracy of Darveaux's methodology within +/-2X, which is considered state of the art for this type of complex physical analysis.

2. TAPE BASED CHIP-SCALE PACKAGE

A 13x13mm, 225-ball (15x15 full ball matrix), 0.80mm pitch chip-scale package was analyzed. The die size was measured at 8.24x9.12mm. The package outline drawing is displayed in Fig. 1. Eight different solder ball via configurations were analyzed. The detail of the eight tape based chip-scale package configurations are outlined in Table 1. All packages consisted of a 1-metal layer tape substrate and incorporated a 0.380mm substrate solder pad diameter with a solder ball via hole opening diameter of 0.280mm at the tape metal layer pad. The stack-up layer thickness information for the printed circuit board (pcb) is provided in Fig. 2.

3. SOLDER BALL FATIGUE MODELS

Viscoplastic finite-element simulation methodologies were utilized to predict solder ball joint reliability of the tape based chip-scale package using eight different ball via configurations created by variations in both package assembly and tape vendors. Due to the complex physics that encompass this type of non-linear transient finite element analysis, only a diagonal slice of the package was modeled in order to facilitate reasonable model run times. The utilization of a diagonal slice assures that a worst-case situation is simulated where the perimeter solder ball is the furthest distance from the package center neutral point. The diagonal slice representing the finite element model is shown by the bold print dashed line in Fig. 1. The resulting diagonal slice model is shown in Fig's 3 and 4 with close-up details of the eight modeled solder ball and via regions shown in Fig's 5 through 12. The entire model utilized a mapped (or structured) finite element mesh that varied from 7035 nodes and 4824 elements to 7428 nodes and 5188 elements depending on the ball via configuration modeled. Typical solution run times were 2.22-2.67 hours (Dual Processor, 800 MHz Pentium III, 1GByte RAM, NT Operating System).

The diagonal slice model passes through the thickness of the package assembly, capturing all major components and a full set of solder joints. The use of a slice model involves a choice on the part of the analyst on the boundary constraints to be applied at the slice plane. The plane is neither a free surface nor a true symmetry plane. The reasonable compromise of coupling the y-displacements of the nodes on the slice plane was chosen. This has the effect that the slice plane is free to move in the y-direction, but that the surface is required to remain planar. Boundary constraints applied to a typical slice model are shown in Fig. 13. Note that for all analyses presented in this paper, the printed circuit board x-dimension (or length) was set at 1.5X that of the modeled package slice x-dimension. The y-dimension (or width) of the slice model is one-half the solder ball pitch. Note that for a diagonal slice model, the ball pitch is the hypotenuse (1.1314mm) of the true ball pitch (0.80mm) as is evident by the ball separation along the bold print dashed line in Fig. 1.

Material Properties & Modified Anand Constants

Linear and non-linear, elastic and plastic, time and temperature independent and dependent material properties were incorporated in the finite element models as displayed in Tables 2 through 6. As an alternative to a rate-independent plasticity approach, Darveaux [11, 20] has presented solder constitutive relations based on Anand's [12] model for rate-dependent plasticity. Anand's constitutive model incorporates viscoplasticity, a time-dependent plasticity phenomenon, where the development of plastic strains is dependent on the rate of loading. Viscoplasticity is defined by unifying plasticity and

creep. Anand's model does not consider rate-independent plasticity. Therefore, Darveaux modified the constants in Anand's constitutive relation to account for both time-dependent and time-independent phenomenon. These modified Anand constants are given in Table 7 [20]. Using ANSYS as the finite element analysis tool, the Anand plasticity data table was activated for the solder ball material and incorporated the constants as given in Table 7. Solder ball materials were meshed in ANSYS using the VISCO107 elements, whereas all other package materials were meshed using SOLID45 elements.

Solder Joint Fatigue Life Prediction Methodology

By measuring the crack growth rate of actual solder joints, Darveaux [20] was able to establish four crack growth correlation constants (K1 through K4) along with two equations by which finite element simulation results could be used to calculate thermal cycles to crack initiation along with crack propagation rate per thermal cycle. However, the methodology is sensitive to the finite element modeling procedure. First, care must be taken in controlling the element thickness at the interface between the eutectic solder and copper pad. Second, element volumetric averaging of the stabilized change in plastic work within this controlled eutectic solder element thickness must be used. This procedure reduces singularity issues whereby the size of the finite element mesh affects plastic work simulation results.

Although equation constants for varying interface element thicknesses are provided by Darveaux [20], the element interface thickness utilized by all models discussed herein was 0.0254mm (1mil). This thickness equates to the first two layers of solder ball material elements at the package substrate and printed circuit board interface joints (see Fig's 5-12). It should also be noted that Darveaux's methodology requires that the solder ball and tape material elements not be joined in the finite element model. This is due to the non-adhesion between solder and tape materials. Given a tape defined solder joint at the package substrate, Darveaux recommends a 0.0127mm (0.5mil) gap between the solder ball and tape material in the finite element model. This gap is visible in Fig's 5 through 12. Corresponding K1 through K4 crack growth correlation constants for a 0.0254mm (1mil) solder joint element thickness are given in Table 8. The equations for the calculation of thermal cycles to crack initiation "N_o" and crack propagation rate per thermal cycle "da/dN" are shown below as (1) and (2) respectively.

$$N_o = K1(\Delta W_{ave})^{K2} \quad (1)$$

$$\frac{da}{dN} = K3(\Delta W_{ave})^{K4} \quad (2)$$

Where "ΔW_{ave}" is the element volumetric average of the stabilized change in plastic work within the controlled eutectic solder element thickness. The characteristic solder joint fatigue life "α" (number of cycles to 63.2% population failure) can then be calculated by summing the cycles to crack initiation with the number of cycles it takes for the crack to propagate across the entire solder joint diameter "a" as shown in equation (3).

$$\alpha = N_o + \frac{a}{da/dN} \quad (3)$$

It should be noted that material intermetallic layers, along with intermetallic spikes directed perpendicular to the intermetallic layers, typically form at the solder pad / solder ball interfaces. The mechanical effects of these intermetallics on the fatigue life of the solder joints are not directly included in the finite element models. However, since the fatigue life prediction methodology developed by Darveaux was derived using measurement data taken from actual solder joints, which presumably contained similar intermetallic structures, their influence is believed to be indirectly incorporated into the predicted results.

ANSYS Solution Methodology

Once the slice model has been completed as displayed in Fig's 3 and 4, and the boundary constraints have been applied as indicated in Fig. 13, the ANSYS solution setup commands are as follows:

```
! SET SOLUTION OPTIONS
/solu                   ! enter soln processor
eqslv,pcg,1.0e-08       ! set solver and tollerance
antype,static,new       ! set analysis type
nlgeom,on               ! set large def and strain
nropt,auto,,off         ! set newton-raphson soln
outres,all,last         ! write data to .rst file
```

The thermal cycle temperature and time variables can be set in ANSYS using variable names and equations as follows:

```
! SET THERMAL CYCLE VARIABLES
hitmp=125+273           ! set hi cycle temp (K)
hirmp=15*60             ! set lo-hi ramp time (sec)
hidwl=15*60             ! set hi dwell time (sec)

lotmp=-40+273           ! set lo cycle temp (K)
lormp=15*60             ! set hi-lo ramp time (sec)
lodwl=15*60             ! set lo dwell time (sec)
```

```
delta=hitmp -lotmp          ! calc delta temp
rmpstp=delta/10             ! calc ramp substeps
```

Note that the analysis will use one substep for every 10 degrees K of temperature change in a thermal ramp load step as suggested by Darveaux [11] and as calculated by the variable "rmpstp" above.

Once the solution setup is complete, two thermal cycles are simulated. The ANSYS zero strain reference temperature is set to the high temperature "hitmp" of the thermal cycle sequence. Each thermal cycle consists of four load steps (ramp low, dwell low, ramp high, and dwell high). Thus a complete simulation of two thermal cycles consists of eight load steps. Other publications that incorporate Darveaux's methodology have indicated the simulation of three thermal cycles (twelve load steps). However, it has been this authors experience that the difference in predicted fatigue life when simulating two thermal cycles, as opposed to three thermal cycles, has been less than 5% and in the conservative direction (i.e. a reduced number of predicted thermal cycles to failure). By only simulating two thermal cycles, simulation run times can be reduced by 30-35%.

The below sequence of ANSYS commands indicates the setting of the zero strain reference temperature along with those required for the first thermal cycle (i.e. first four load steps).

```
tref,hitmp                  ! set zero strain temp

! RAMP LOW (LOAD STEP 1)
autots,off                  ! turn off auto time step
nsubstp,rmpstp              ! set substeps
bf,all,temp,lotmp           ! apply temp to all nodes
kbc,0                       ! linearly ramp loads
time,lormp                  ! set time
solve                       ! solve load step

! DWELL LOW (LOAD STEP 2)
autots,on                   ! turn on auto time step
nsubstp,10,100,1            ! set substeps
bf,all,temp,lotmp           ! apply temp to all nodes
kbc,1                       ! maintain loads
time,lormp+lodwl            ! set time
solve                       ! solve load step

! RAMP HIGH (LOAD STEP 3)
autots,off                  ! turn off auto time step
nsubstp,rmpstp              ! set substeps
bf,all,temp,hitmp           ! apply temp to all nodes
kbc,0                       ! linearly ramp loads
time,lormp+lodwl+hirmp      ! set time
solve                       ! solve load step

! DWELL HIGH (LOAD STEP 4)
autots,on                   ! turn on auto time step
nsubstp,10,100,1            ! set substeps
bf,all,temp,hitmp           ! apply temp to all nodes
kbc,1                       ! maintain loads
time,lormp+lodwl+hirmp+hidwl    ! set time
solve                       ! solve load step
```

To finish the simulation of the second thermal cycle, the above ANSYS command groups for load steps 1 through 4 are repeated. However, the x-value indicating time in the ANSYS "time,x" command for load steps 5 through 8 must be adjusted appropriately. This is easily done by adding a multiplier in front of each of the time constants for load steps 5 though 8 respectively as follows:

```
time,2*lormp+lodwl+hirmp+hidwl          ! LS5
time,2*lormp+2*lodwl+hirmp+hidwl        ! LS6
time,2*lormp+2*lodwl+2*hirmp+hidwl      ! LS7
time,2*lormp+2*lodwl+2*hirmp+2*hidwl    ! LS8
```

Once two thermal cycles (eight load steps) have completed execution, it is necessary to obtain the ΔW_{ave} for the worst-case solder joint. The worst-case solder joint can be identified by plotting the nodal plastic work of the solder ball materials at the end of the eighth load step. Once the worst-case solder joint has been identified, only the 0.0254mm (1mil) thick layer of solder ball material elements at the joint interface are selected using the ANSYS ESEL (element select) command. Once the 0.0254mm thick layer of solder ball material elements which make up the solder joint have been selected within ANSYS, the below sequence of ANSYS commands are then used to calculate ΔW_{ave}.

```
! CALC AVG PLASTIC WORK FOR CYCLE 1
set,4,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
wavg1=sumplwk/sumvolu

! CALC AVG PLASTIC WORK FOR CYCLE 2
set,8,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
wavg2=sumplwk/sumvolu

! CALC DELTA AVG PLASTIC WORK
dwavg=wavg2-wavg1
```

Since Darveaux provides crack growth correlation constants in English units, it is important to

remember to convert the simulated ΔW_{ave} (ANSYS constant "dwavg") from units of MPa to units of psi by multiplying by 6.894757×10^{-3}. Also, the solder joint diameter should be converted from units of mm to units of inches by dividing by 25.4. These values can then be substituted into equations (1) through (3) to obtain cycles to crack initiation, crack propagation rate, and solder joint characteristic fatigue life respectively.

4. FATIGUE MODEL RESULTS

A total of eight package diagonal slice models were created to evaluate the effects of differing ball via configurations due to variations in both package assembly and tape vendors. Table 1 indicates the package configurations investigated which consisted of punched, etched, laser etched, and enhanced re-flow pad area vias. It should be noted that configurations 1 and 7 are identical except for the use of a reduced mold cap and die attach thickness. This is also true for configurations 4 and 8. It should also be noted that configurations 2 and 3 utilize the 3M nickel and copper eVia enhancements respectively. In all simulations it is assumed that a solder paste is pre-applied to the printed circuit board solder ball pads to insure that the package solder ball standoff heights are maintained after 2nd level board re-flow. The original solder ball diameter for all eight tape based chip-scale package configurations was 0.40mm.

Tables 9 and 10 indicate the detailed simulation results for package configurations 1 through 4, and 5 through 8 respectively. Included in these tables is the location of the diagonal slice model failure ball (from model center, including center half ball). Also included is the viscoplastic strain energy density change from simulated thermal cycle 1 to 2 (i.e. Delta Plastic Work/Cycle) which is substituted into Equations (1) and (2) to calculate cycles to crack initiation and crack propagation rate respectively. The solder joint diameter, cycles for the crack to propagate across this diameter, and the characteristic solder joint fatigue life (i.e. 63.2% population failure) are also provided in Tables 9 and 10.

In all ball via configurations evaluated, the solder joint at the package substrate failed first with the exception of package configuration 3 (3M Cu-eVia) where the solder joint at the printed circuit board pad failed first. Package substrate solder joint characteristic fatigue lives ranged from 286cycles (Laser Via/Config. 6) to 1130cycles (3M Cu-eVia/Config. 3). The first failure ball at the package substrate joint consistently occurred at solder ball 7, which is seen to be located just outside the edge of the die in Fig's 3 and 4. One exception to this occurs for package configuration 6 (etched via/reduced thickness mold cap and die) where the first failure joint occurred at solder ball 6, which is just inside of the die edge.

The characteristic fatigue lives at the printed circuit board solder joints ranged from 707cycles (Laser Via/Config. 6) to 994cycles (3M Cu-eVia/Config. 3). The first failure ball at the package substrate consistently occurred at solder ball 8, which is the outside solder joint of the diagonal slice models.

In comparing like package configurations with the reduced mold cap and die thicknesses (i.e. Config's 1/7 & 4/8), it should be noted that the thinner packages performed better with solder joint characteristic fatigue lives at both the package substrate and printed circuit board solder joints which are double that of the thicker package configurations. This is consistent with results seen in a previous study by Zahn [17]. This dramatic improvement in solder joint characteristic fatigue life is believed to be directly related to the increased flexibility of the thinner package configurations, thus reducing the amount of plastic strain absorbed by the solder ball structures during accelerated temperature cycling.

5. SUMMARY

A finite element analysis based methodology for estimating accelerated temperature cycling solder joint characteristic fatigue life has been applied to predict the reliability performance of differing ball via configurations for a tape based chip-scale package due to variations in both package assembly and tape vendors. This included the evaluation of punched, etched, laser etched, and enhanced re-flow pad area vias. The methodology incorporated the ANSYS finite element analysis tool along with Anand's viscoplastic constitutive law. Darveaux's crack growth rate model was applied to calculate solder joint characteristic life using simulated viscoplastic strain energy density results at the package substrate and printed circuit board solder joints.

Eight package configurations were evaluated including the use of the 3M nickel and copper eVia enhanced area solder ball pads. Two sets of package configurations where identical except for the use of reduced mold cap and die thicknesses. Simulations indicate that the 3M Cu-eVia provides the best solder joint characteristic fatigue life performance followed by the 3M Ni-eVia for the standard thickness packages. However, by incorporating a reduced mold cap and die thickness, the solder joint characteristic fatigue life of both the etched and punched solder ball via configurations were able to surpass that of the 3M Ni-eVia. However, the 3M Cu-eVia remained the top performer for all package configurations analyzed as part of this study

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Table 1. Tape Based Chip-Scale Package Configuration Details.

	Config. 1	Config. 2	Config. 3	Config. 4	Config. 5	Config. 6	Config. 7	Config. 8
Mold Cap	0.7mm EME7730	0.7mm EME7730	0.7mm EME7730	0.7mm EME7730	0.7mm EME7730	0.7mm EME7730	0.5mm EME7730	0.5mm EME7730
Die	0.3048mm Silicon	0.3048mm Silicon	0.3048mm Silicon	0.3048mm Silicon	0.3048mm Silicon	0.3048mm Silicon	0.1778mm Silicon	0.1778mm Silicon
Die Attach	0.0445mm 84-3MVB	0.0445mm 84-3MVB	0.0445mm 84-3MVB	0.0445mm 84-3MVB	0.0445mm 84-3MVB	0.0445mm 84-3MVB	0.0445mm 84-3MVB	0.0445mm 84-3MVB
Metal Layer	0.025mm Copper	0.025mm Copper	0.025mm Copper	0.018mm Copper	0.018mm Copper	0.018mm Copper	0.025mm Copper	0.018mm Copper
Adhesive Layer	N/A	N/A	N/A	0.012mm Tomo-X	0.012mm Tomo-X	N/A	N/A	0.012mm Tomo-X
Tape Substrate	0.050mm Kapton-E	0.050mm Kapton-E	0.050mm Kapton-E	0.050mm Upilex-S	0.050mm Upilex-S	0.040mm Espanex	0.050mm Kapton-E	0.050mm Upilex-S
Via Type	Generic Etched	3M Ni - eVia	3M Cu - eVia	Generic Punched	Generic Punched	Generic Laser	Generic Etched	Generic Punched
Via Plug	N/A	0.013mm Nickel	0.040mm Copper	N/A	0.040mm Paste	N/A	N/A	N/A
Via Hole Top Dia.	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm
Via Hole Bottom Dia.	0.4206mm	0.4260mm	0.4260mm	0.2800mm	0.2800mm	0.3180mm	0.4260mm	0.2800mm
Substrate Joint Dia.	0.2800mm	0.3256mm	0.3728mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm
PCB Joint Dia.	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm	0.2800mm
Solder Ball Stdoff. Ht.	0.2860mm	0.2910mm	0.3010mm	0.3094mm	0.3645mm	0.3090mm	0.2860mm	0.3094mm
Solder Ball Ctr. Dia.	0.4640mm	0.4720mm	0.4890mm	0.4112mm	0.4112mm	0.4510mm	0.4640mm	0.4112mm

Solder Ball Stdoff. Ht. = Distance from PCB Pad Top to Tape Substrate Bottom.
Original Ball Dia. = 0.40mm (Solder Paste Pre-Applied to PCB Pads to Insure 2nd Level Re-Flow Ball Standoff)

Table 2. Model Material Properties.

Component (Material)	Elastic Moduli (MPa)	Shear Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)
Ball (63Sn37Pb)	75842-152T	-	$24.5\text{x}10^{-6}$	0.35
Chip (Silicon)	162716	-	$-5.88\text{x}10^{-6}+6.26\text{x}10^{-8}\text{T}$ $-1.6\text{x}10^{-10}\text{T}^2+1.5\text{x}10^{-13}\text{T}^3$	0.28
Conductor (Copper)	128932	-	$13.8\text{x}10^{-6}+9.44\text{x}10^{-9}\text{T}$	0.34
PCB Core (FR4)	27924-37T (XY) 12204-16T (Z)	12600-16.7T (XY) 5500-7.3T (YZ & XZ)	$16.0\text{x}10^{-6}$ (XY) $84.0\text{x}10^{-6}$ (Z)	0.39 (XZ & YZ) 0.11 (XY)
PCB Mask (Dry Film)	4137	-	$30.0\text{x}10^{-6}$	0.40

T = Material Property Temperature in Kelvin

Table 3. Tape Material Properties.

Tape (Kapton-E)				Tape (Upilex-S)			
Temp (K)	Elastic Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)	Temp (K)	Elastic Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)
233	6624	(XY) $1.20\text{x}10^{-5}$ (Z) $3.00\text{x}10^{-5}$	0.35	233	9878	(XY) $1.00\text{x}10^{-5}$ (Z) $2.50\text{x}10^{-5}$	0.26
298	5520		0.34	298	8232		0.25
423	1252		0.33	373	6860		0.23
448	313		0.32	448	5684		0.24

Table 4. Tape Material Properties..

Tape (Espanex)			
Temp (K)	Elastic Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)
293	5900	(XY) 1.20×10^{-5} (Z) 2.00×10^{-5}	
298			0.41
473	3500		

Table 5. Tape Adhesive and Die Attach Material Properties.

Tape Adhesive (Tomoekawa-X)				Die Attach (84-3MVB)			
Temp (K)	Elastic Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)	Temp (K)	Elastic Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)
233	1058	1.69×10^{-4}	0.35	233	12184	4.40×10^{-5}	0.35
298	588		0.35	298	6769		0.35
373		1.70×10^{-4}		353		4.50×10^{-5}	
433		1.85×10^{-4}		363		7.90×10^{-5}	
453	49		0.35	368		8.90×10^{-5}	
473		1.86×10^{-4}		373		9.90×10^{-5}	
				383		1.33×10^{-4}	
				473	207	1.34×10^{-4}	0.35

Table 6. Mold Compound Material Properties.

Mold Compound (EME7730)			
Temp (K)	Elastic Moduli (MPa)	CTE (1/K)	Poisson's Ratio (No Units)
233	28224	9.00×10^{-6}	0.25
298	23520		0.25
403		1.00×10^{-5}	
418		1.70×10^{-5}	
423		2.20×10^{-5}	
428		2.70×10^{-5}	
443		3.40×10^{-5}	
473		3.50×10^{-5}	
513	1764		0.25

Table 7. Darveaux Modified Anand Constants [11, 20].

Constant	Parameter	Value	Definition
C1	S_o (MPa)	12.41	Initial Value of Deformation Resistance
C2	Q/R (1/Kelvin)	9400	Activation Energy/Boltzmann's Constant
C3	A (1/sec)	4.0E-06	Pre-Exponential Factor
C4	ξ (dimensionless)	1.5	Multiplier of Stress
C5	m (dimensionless)	0.303	Strain Rate Sensitivity of Stress
C6	h_o (MPa)	1378.95	Hardening Constant
C7	s (MPa)	13.79	Coeff. of Deformation Resistance Saturation Value
C8	n (dimensionless)	0.07	Deformation Resistance Value
C9	a (dimensionless)	1.3	Strain Rate Sensitivity of Hardening

Table 8. Darveaux K1 through K4 Crack Growth Correlation Constants [20].

Constant	Value
K1	22400 cycles/psi
K2	-1.52
K3	5.86×10^{-7} in/cycle/psi
K4	0.98

Table 9. Detailed Simulation Results – Chip-Scale Package Configurations 1-4.

Data Description	Config. 1	Config. 2	Config. 3	Config. 4
Ball/Substrate Solder Joint				
Failure Joint (From Center)	7	7	7	7
Delta Plastic Work/Cycle (MPa)	0.4987E+00	0.3351E+00	0.1878E+00	0.4566E+00
Delta Plastic Work/Cycle (psi)	72.33	48.60	27.24	66.22
Crack Initiation (cycles)	33	61	147	38
Crack Growth Rate (mm/cycle)	0.9883E-03	0.6694E-03	0.3796E-03	0.9064E-03
Solder Joint Diameter (mm)	0.2800	0.3256	0.3728	0.2800
Crack Propagation (cycles)	283	486	982	309
Characteristic Life (cycles)	317	548	1130	347
Ball/Test Board Solder Joint				
Failure Joint (From Center)	8	8	8	8
Delta Plastic Work/Cycle (MPa)	0.2034E+00	0.1814E+00	0.1686E+00	0.2375E+00
Delta Plastic Work/Cycle (psi)	29.51	26.31	24.46	34.44
Crack Initiation (cycles)	131	155	174	103
Crack Growth Rate (mm/cycle)	0.4104E-03	0.3669E-03	0.3415E-03	0.4776E-03
Solder Joint Diameter (mm)	0.2800	0.2800	0.2800	0.2800
Crack Propagation (cycles)	682	763	820	586
Characteristic Life (cycles)	813	919	994	690
Model Size and Run Time Info.				
Total Model Nodes	7035	7428	7428	7292
Total Model Elements	4824	5188	5188	5008
CPU Run Time (Hrs)	2.49	2.66	2.59	2.78

Table 10. Detailed Simulation Results – Chip-Scale Package Configurations 5-8.

Data Description	Config. 5	Config. 6	Config. 7	Config. 8
Ball/Substrate Solder Joint				
Failure Joint (From Center)	7	7	6	7
Delta Plastic Work/Cycle (MPa)	0.4200E+00	0.5481E+00	0.2412E+00	0.2250E+00
Delta Plastic Work/Cycle (psi)	60.92	79.50	34.99	32.63
Crack Initiation (cycles)	43	29	101	112
Crack Growth Rate (mm/cycle)	0.8352E-03	0.1084E-02	0.4850E-03	0.4530E-03
Solder Joint Diameter (mm)	0.2800	0.2800	0.2800	0.2800
Crack Propagation (cycles)	335	258	577	618
Characteristic Life (cycles)	379	287	678	730
Ball/Test Board Solder Joint				
Failure Joint (From Center)	8	8	8	8
Delta Plastic Work/Cycle (MPa)	0.2254E+00	0.2293E+00	0.1128E+00	0.1237E+00
Delta Plastic Work/Cycle (psi)	32.69	33.26	16.36	17.94
Crack Initiation (cycles)	112	109	320	278
Crack Growth Rate (mm/cycle)	0.4538E-03	0.4615E-03	0.2302E-03	0.2521E-03
Solder Joint Diameter (mm)	0.2800	0.2800	0.2800	0.2800
Crack Propagation (cycles)	617	607	1216	1111
Characteristic Life (cycles)	729	716	1536	1389
Model Size and Run Time Info.				
Total Model Nodes	7292	7035	7035	7292
Total Model Elements	5008	4824	4824	5008
CPU Run Time (Hrs)	2.81	2.60	2.49	2.78

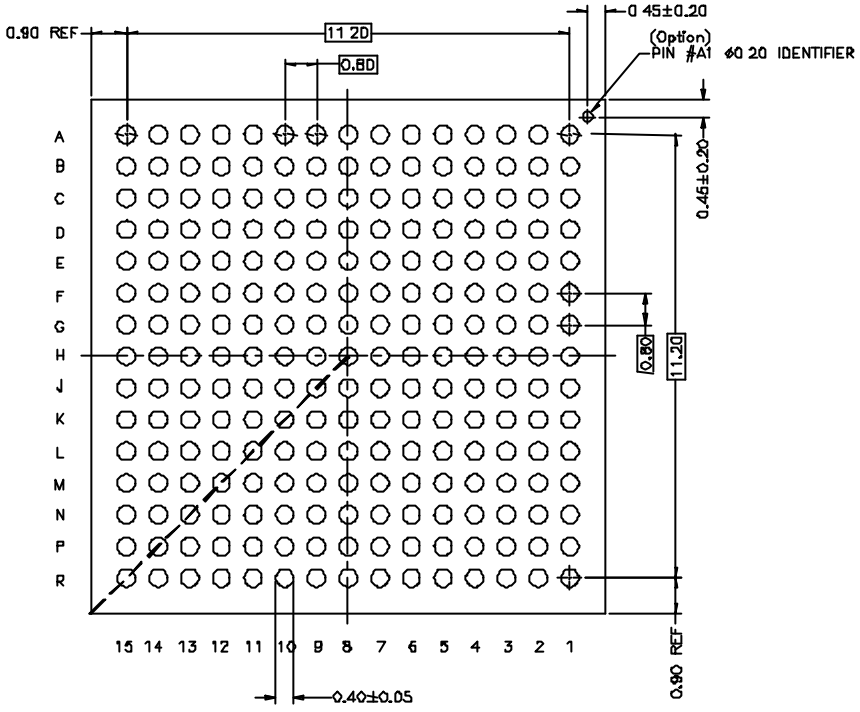

Fig. 1. Package outline drawing.

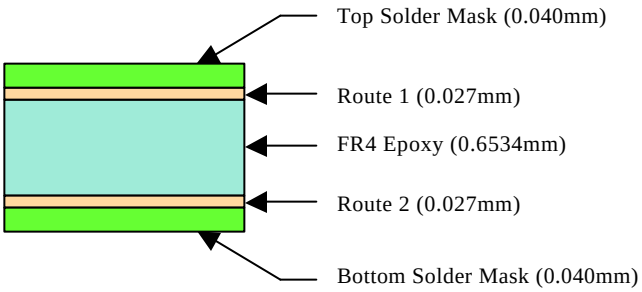

Fig. 2. Layer dimensions of printed circuit board.

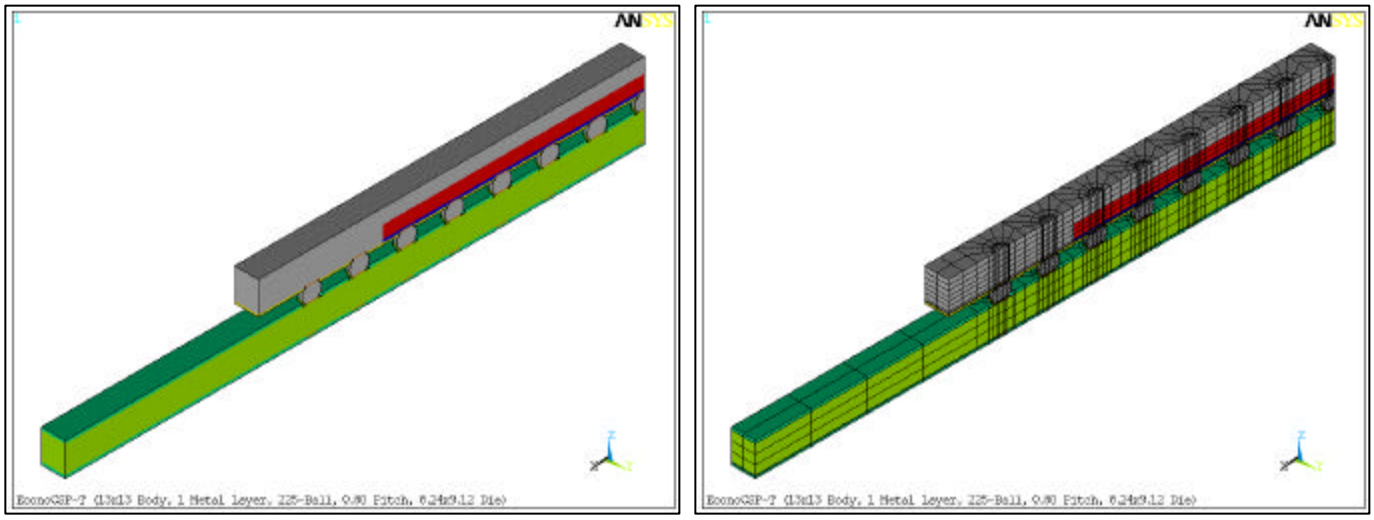

Fig. 3 & 4. Diagonal slice finite element model and resulting mesh.

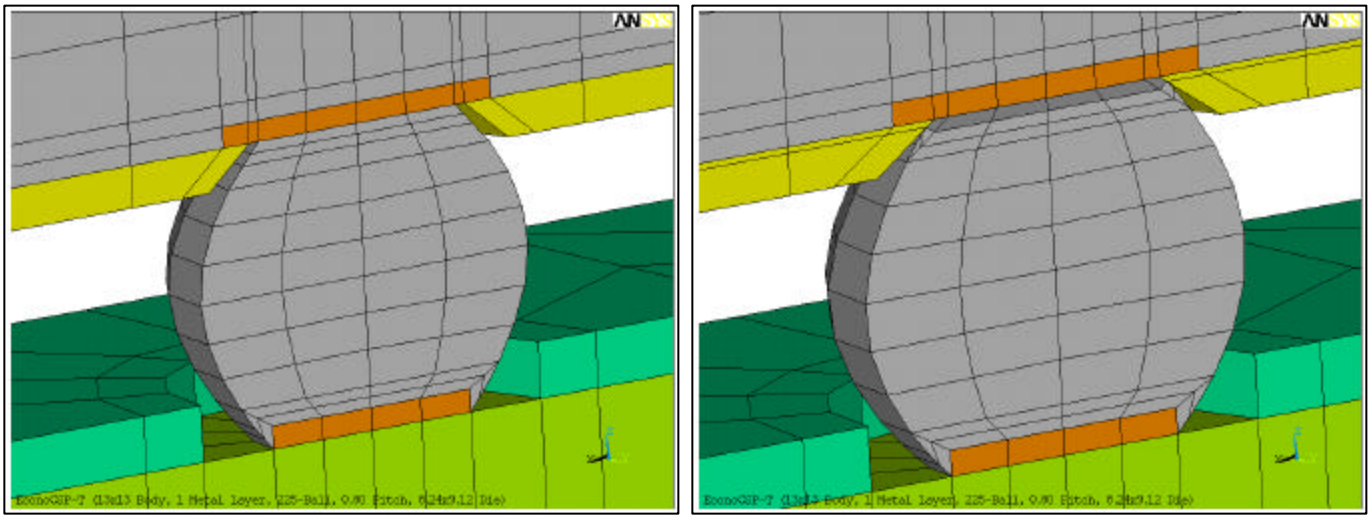

Fig. 5 & 6. Modeled ball and ball via details for Chip-Scale package configurations 1 and 2 respectively.

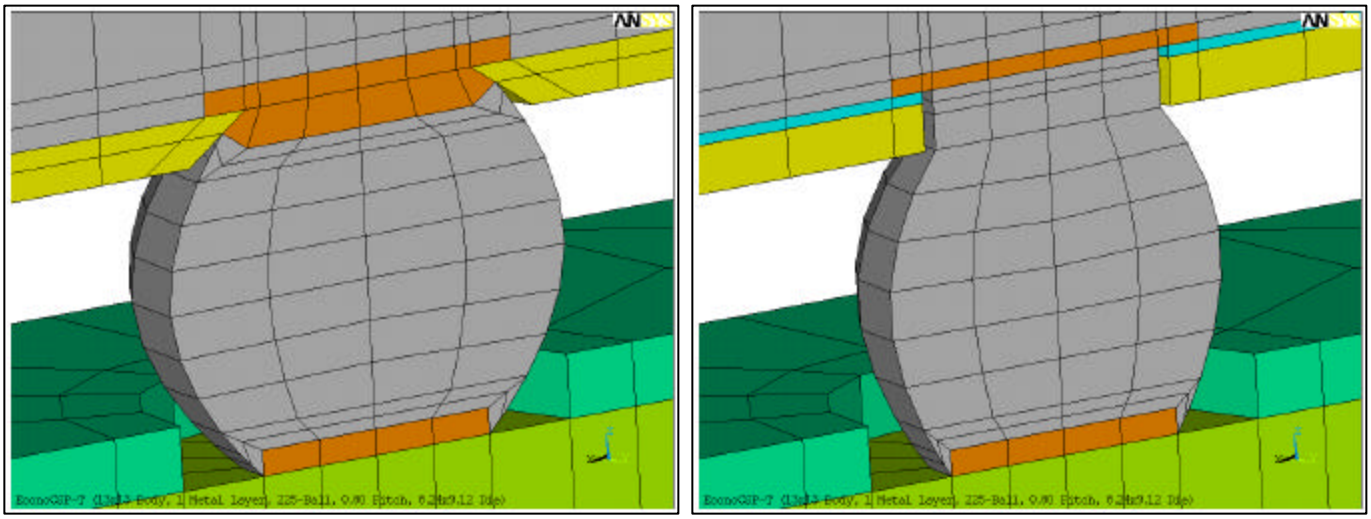

Fig. 7 & 8. Modeled ball and ball via details for Chip-Scale package configurations 3 and 4 respectively.

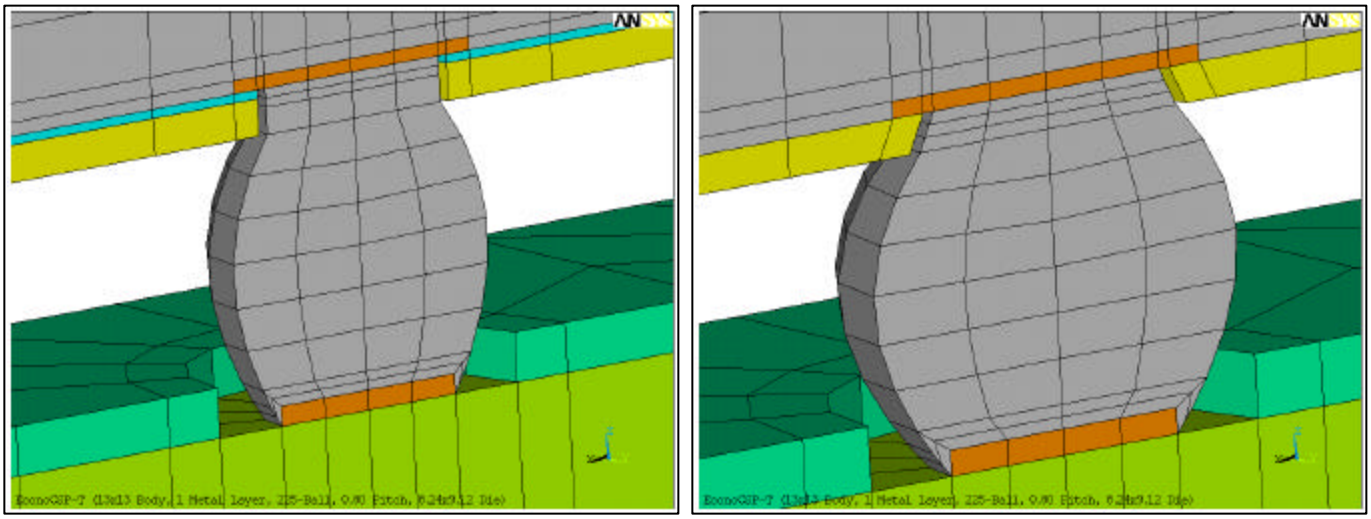

Fig. 9 & 10. Modeled ball and ball via details for Chip-Scale package configurations 5 and 6 respectively.

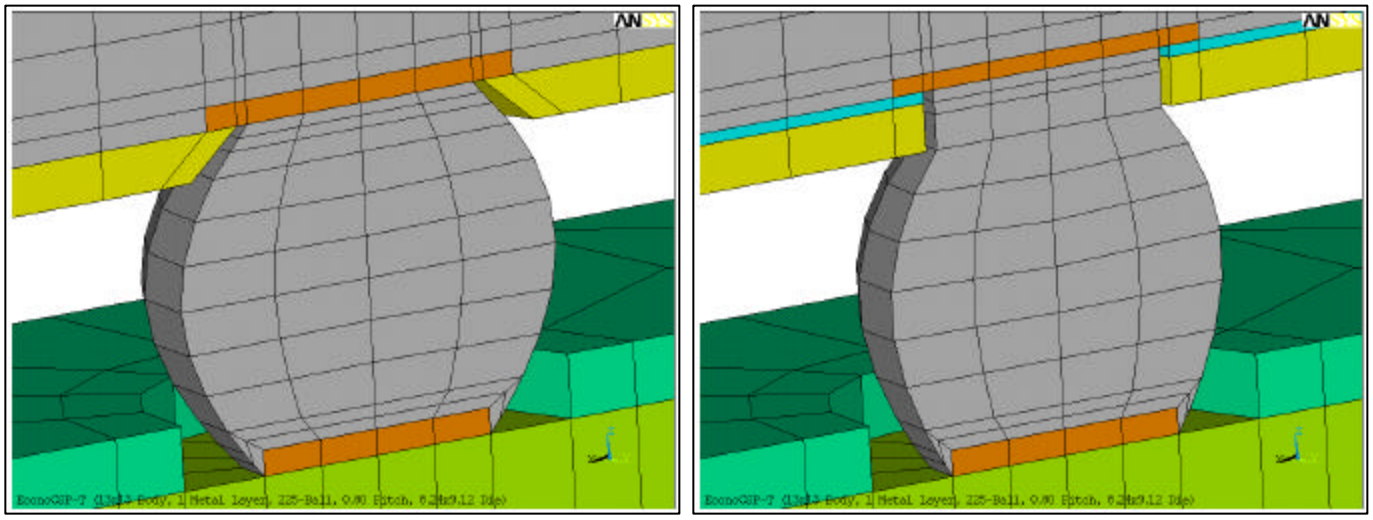

Fig. 11 & 12. Modeled ball and ball via details for Chip-Scale package configurations 7 and 8 respectively.

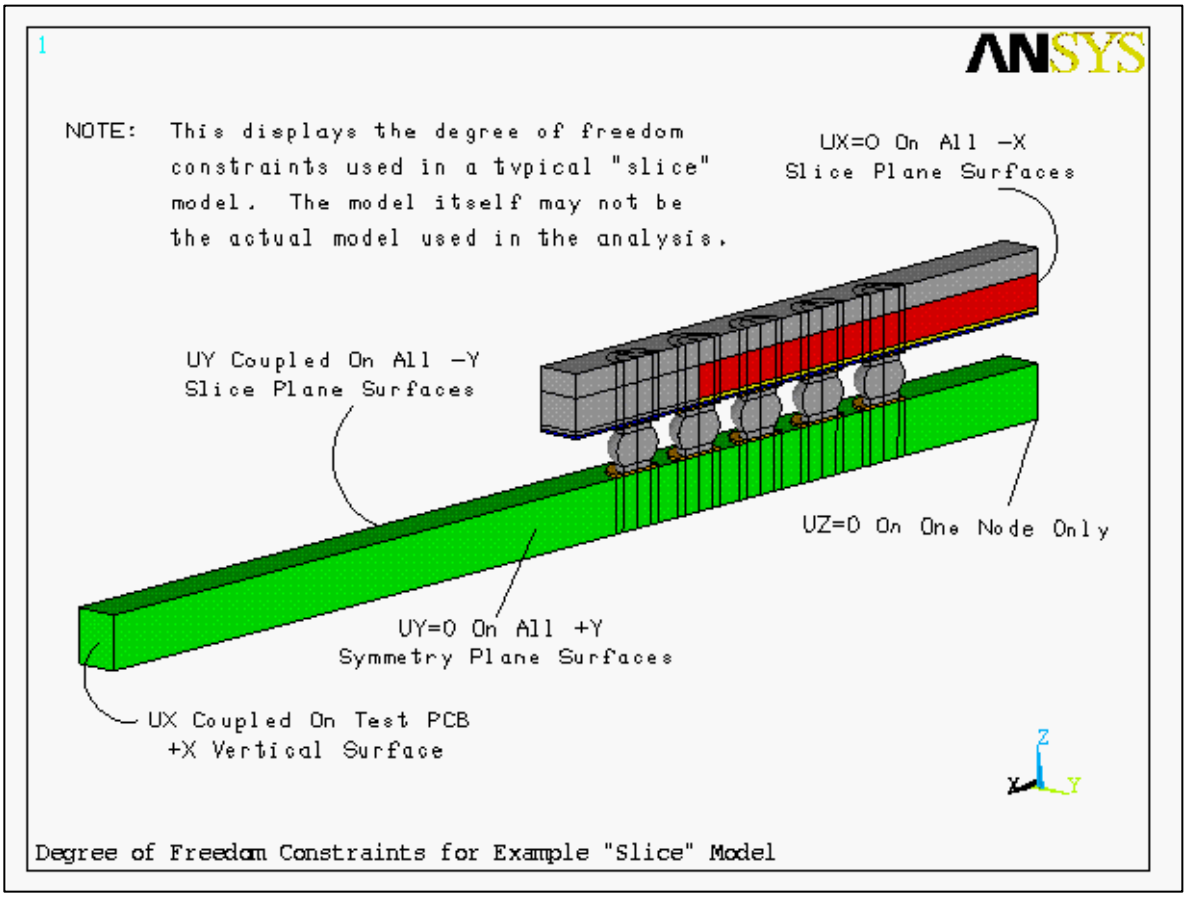

Fig. 13. Boundary constraints applied to a typical slice model.