A Parametric Study of Flip Chip Reliability Based on Solder Fatigue Modelling

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1997 International Electronics Manufacturing Technology Symposium
October 13-15, 1997

Abstract

A solder fatigue model for 63Sn/Pb solder has been developed by combining nonlinear finite element modelling with thermal fatigue data of assorted flip chip assemblies. The model characterizes the creep fatigue phenomena of the solder alloy by correlating the amount of creep strain energy dissipated per thermal cycle with the characteristic Weibull life of the critical solder joint. It has been validated for various die sizes, bump geometries, board materials and thermal profiles. Furthermore, the model has accurately predicted fatigue lives for flip chip assemblies with and without underfill.

The solder fatigue model has been utilized to investigate the reliability of flip chip joints subjected to thermal cycling. In particular, a parametric study had been performed which shows how various flip chip design parameters will affect solder joint fatigue. Finite element models have been developed to analyze the effect of die size, die thickness, solder joint height, cap diameter and underfill properties on solder fatigue. For this investigation, all analyses have been carried out for parts on ceramic substrates. The results for underfilled parts show that while die size does not influence solder joint reliability, the effects of underfill CTE are very important. Non-underfilled parts are significantly influenced by die size, cap size and joint height.

Introduction

The accelerated development and implementation of flip chip technology is an ongoing race between increasing die size, I/O density and cost effectiveness, coupled with constant demands to decrease design cycle time. Moreover, these goals must be realized while maintaining a high level of reliability. The role of materials characterization and finite element modelling is to serve as a valuable aide in the advanced development of flip chip applications. Both may be employed to predict reliability as well as evaluate materials and designs. Their main advantage, however, lies in their ability to measure the influence of design parameters on reliability in a relatively short period of time.

Perhaps the failure mode which receives the most attention, and which potentially has the greatest impact on the reliability of flip chip applications, is solder joint fatigue due to the coefficient of thermal expansion (CTE) mismatch of adjoining materials. A great deal of time and effort has been spent on evaluating thermal fatigue, both experimentally and analytically, with the ultimate goal of generating a means to predict solder joint failure. In general, all successful solder fatigue models correlate the number of thermal cycles to failure with an appropriate and well-defined correlating parameter. This parameter must quantify the damage mechanism which will ultimately lead to a fatigue failure. For solder joints in most microelectronics applications, prominent damage mechanisms may be due to elastic deformation (vibration loads), time-independent plastic deformation (thermal shock), or time-dependent creep deformation (thermal cycle). For flip chip applications in particular, solder fatigue due to thermal cycling is the most prominent fatigue mechanism found in product field failures. Thus, a methodology for generating models characterizing the creep fatigue of solder alloys would prove to be an invaluable tool.

The ability to predict solder fatigue may be used to address three general classes of problems. First and foremost, reliability predictions may be generated for specific flip chip applications subjected to particular thermal profiles. In addition, design evaluations may be made to determine an optimum materials set or geometry. Finally, the

Presented at the 1997 International Electronics Manufacturing Technology Symposium
Austin, Texas, October 13-15, 1997, pp. 299-307

creep fatigue model may be used in parametric studies assessing the influence of flip chip design parameters on solder fatigue. These parametric studies may be used to show trends and develop design rules. While a parametric analysis is the most work-intensive of the applications of the solder fatigue model, it also has the potential to be the most economical, relative to the cost of performing the analysis experimentally. Furthermore, the solder fatigue model allows parametric studies to be performed which are impossible to perform experimentally due to insufficient process controls or unavailable materials.

The following paper presents a creep fatigue model for the 63Sn/Pb solder alloy. The model is generated by combining nonlinear finite element analyses with experimentally measured thermal fatigue lives of various flip chip assemblies. The model is then used to perform a parametric study investigating the influence of certain design parameters on the fatigue life of flip chip solder joints. The study is limited to ceramic applications for this investigation. When appropriate, measured fatigue lives are compared to those predicted in the parametric study.

Experimental Fatigue Data

63Sn/Pb solder fatigue data has been generated by thermal cycling various combinations of flip chip assemblies mounted on organic and ceramic circuit boards, with and without underfill, for various solder joints geometries and die sizes. The tests were performed for a -50/150°C temperature profile with 15 minute dwells and 25 minute ramps, as well as a 60 minute -40/125°C profile (15 minute ramps and dwells). The test vehicles used for these experiments included 0.25 and 0.5 inch square die with 18 mil pitch perimeter bumps, in addition to 0.221 by 0.251 inch die containing 8 mil pitch perimeter bumps. All parts were daisy chained continuity test die, assembled to substrates such that current passed through each bump. The parts were electrically tested at prescribed endpoints during thermal cycling in order to detect the first electrically open flip chip solder joint. An open joint was defined as a 20 percent increase in resistance of the daisy-chained joints, and marked the end of the test for a given flip chip. Typical sample sizes ranged from 35 to 72 parts per flip chip combination.

For each test condition a two-parameter Weibull failure distribution was generated using only data points from confirmed solder fatigue failures. The Weibull distribution has the following form [1]

$$F(x) = 1 - e^{-(x/\theta)^{\beta}} \qquad (1)$$

where F(x) is the probability of failure at x number of cycles, β is the shape parameter or Weibull slope, and θ is the characteristic Weibull life. Note that the Weibull life defines the number of cycles where 63.2 percent of the parts have failed. In all, thirteen flip chip combinations have been tested for this investigation, yielding Weibull lives ranging from 18 to 5300 cycles.

63Sn/Pb Solder Fatigue Model

A general methodology for generating creep fatigue models for solder alloys has been described by Popelar, et al. in [2]. For the present model, the experimentally measured Weibull lives described above are correlated with a damage parameter through nonlinear finite element analyses.

For each type of flip chip assembly tested, a two-dimensional plane strain finite element model was generated and analyzed for the given thermal profile to determine the value of the corresponding damage parameter. The finite element models were generated using the ANSYS™ general purpose finite element software. Two-dimensional models were selected over three-dimensional because more detail of the solder joint could be included and the models could be easily modified for different flip chip geometries. The two-dimensional models have been shown to sufficiently capture the influence of flip chip design parameters on solder fatigue. Thus, the increase in time and computer resources required to utilize three-dimensional models was not justified.

Consider the flip chip schematic shown in Figure 1, consisting of the die, solder joint, substrate and epoxy underfill. All the materials making up these components are assumed to behave linearly, with the exception of the solder. As such, the elastic

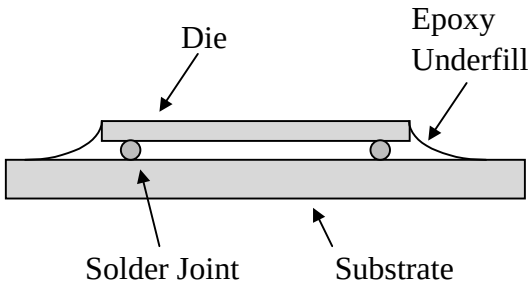

Figure 1. Flip chip schematic.

modulus, CTE and Poisson's ratio are provided as a function of temperature for the finite element models. For the solder, however, an additional constitutive equation is required which describes the nonlinear time-dependent creep phenomena of the solder. This equation may take many forms. For the present investigation, the two-term power law equation described by Wong et al. [3] is employed. This equation relates the steady-state creep strain rate $d\varepsilon_{cr}/dt$ to temperature and applied load σ, and is expressed as

$$\frac{d\varepsilon_{cr}}{dt} = DB_1\left(\frac{\sigma}{E}\right)^{n_1} + DB_2\left(\frac{\sigma}{E}\right)^{n_2} \qquad (2)$$

where

E = Elastic Modulus
D = exp(Q/kT)
T = Absolute Temperature, K
k = 8.63e-5 eV/K

The parameters Q, B_1, B_2, n_1 and n_2 are alloy dependent constants, which must be determined experimentally along with the elastic modulus. These parameters have been measured by Popelar [4] for 63Sn/Pb, and are listed below.

Q = 0.32 eV
B_1 = 1.75e12 sec^{-1}
B_2 = 3.51e54 sec^{-1}
n_1 = 4.08
n_2 = 18.6
E = 12.5 - 0.029T, Msi

The first term in Equation (2) represents the component of creep deformation due to grain boundary sliding, while the second term represents deformation due to matrix creep. Grain boundary sliding will occur at combinations of low stress levels and high temperatures, while matrix creep occurs at high stresses and low temperatures. It should also be pointed out that because the temperature cycles investigated are assumed to be slow enough that the solder has ample time to creep (i.e., relax), the stresses in the solder are assumed to remain low enough such that no significant time-independent plastic deformation occurs. Hence, no plasticity models are considered for the solder in the finite element analyses.

For each finite element analysis performed, a creep hysteresis curve (equivalent stress versus equivalent creep strain) is generated for a single temperature cycle. The stress is defined as the Von Mises equivalent stress, while the equivalent creep strain is defined as

$$\varepsilon_{cr} = \left\{(2/3)\left(\varepsilon_x^2 + \varepsilon_y^2 + \varepsilon_z^2 + 1/2\left(\gamma_{xy}^2 + \gamma_{xz}^2 + \gamma_{yz}^2\right)\right)\right\}^{1/2} \qquad (3)$$

where ε's and γ's denote normal and shear components of creep strain, respectively. The creep hysteresis curve is generated for a 0.5 mil layer of solder at the die/solder joint interface. Failure analyses of fractured flip chip joints show that it is in this region of the solder joint where typical creep fatigue failures occur. The equivalent stress and strain values calculated from finite element analyses represent an area average of the 0.5 mil solder layer. It should be noted that each finite element model contains eight elements through the thickness of the 0.5 mil layer. This approach has been shown to eliminate convergence problems associated with the finite element models and their corresponding mesh densities [5].

Figure 2 shows a creep hysteresis curve for a typical flip chip assembly subjected to a single thermal cycle, generated by a nonlinear finite element analysis. The area within the curve is defined as the creep strain energy or creep energy, dissipated per thermal cycle. It is this parameter which characterizes the amount of creep damage per cycle in the solder joint. Hence, it will be used

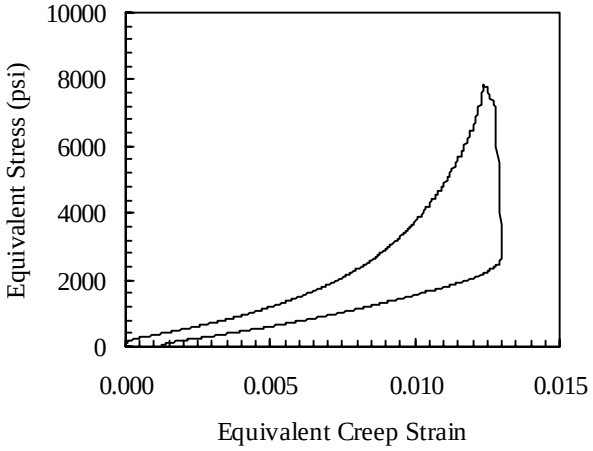

Figure 2. Typical hysteresis curve for a flip chip joint subjected to a single thermal cycle.

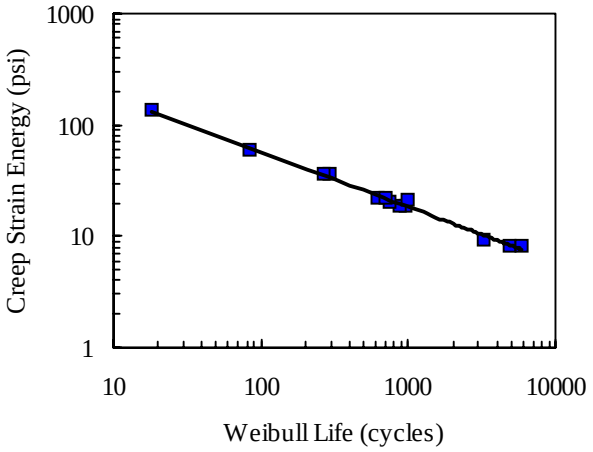

Figure 3. 63Sn/Pb fatigue life correlation.

as the damage parameter in the subsequent solder fatigue correlation.

Figure 3 shows the experimentally measured fatigue lives correlated with the creep energy dissipated per thermal cycle for the 63Sn/Pb solder alloy. For each data point shown, a finite element model was generated for the given flip chip assembly and analyzed for the appropriate thermal profile to determine the creep energy dissipated per thermal cycle. Note that the correlation in Figure 3 is very strong throughout the measured range of fatigue lives. In addition, the correlation holds for flip chips with and without underfill. Without underfill the solder joint is dominated by a shear loading mechanism, with relatively small contributions due to tensile loads. With underfill, however, comparable contributions exist from both shear and normal loads. The fact that the correlation holds for such different loading conditions indicates that the dissipated creep energy is indeed a valid fatigue correlating parameter.

The curve shown in Figure 3 is a power law fit to the data defining the creep fatigue correlation as

$$W_{cr} = 560 N_f^{-0.495} \qquad (4)$$

where W_{cr} is the creep energy dissipated per thermal cycle and N_f is the Weibull life. The fatigue model of Equation (4) characterizes the creep fatigue phenomena of 63Sn/Pb solder subjected to thermal cycling. For a given flip chip application subjected to a specific thermal profile, the amount of creep energy dissipated can be determined using an appropriate finite element analysis. Equation (4) may then be employed to accurately predict the fatigue life of the system.

The fatigue model described above has been used to perform a parametric study of flip chips assembled to ceramic substrates. The following is a detailed discussion of the results of this study.

Parametric Study of Flip Chips on Ceramic

An accurate and flexible solder fatigue model allows one to study the effect of design parameters on fatigue life quickly and inexpensively. Such a parametric study has been carried out for the flip chip on ceramic application. The effect of die size, die thickness, solder joint height and cap diameter has been investigated for underfilled and non-underfilled parts. In addition, the effect of underfill elastic modulus and CTE has been evaluated. There are several caveats listed below which must be taken into account when considering the resulting parametric curves.

- The failure mode for all fatigue life predictions is assumed to be solder fatigue due to accumulated creep damage. Other failure modes such as delamination or die cracking are not considered for the present investigation, but may be present in actual applications.

- It is assumed that a single parameter may be changed without an interacting effect on other parameters. For example, the cap diameter (defined as the diameter of the under bump metallurgy) is varied without considering an accompanying change in solder joint height that would typically be seen in actual applications.
- All fatigue life results are presented in terms of the characteristic Weibull life.
- All results are for a -50/150°C, 80 minute temperature profile with 25 minute ramps and 15 minute dwells.
- All results are for a 35 mil thick Alumina substrate.
- The default values for die size, die thickness, solder joint height and cap diameter are 250 mils square, 25 mils, 3.5 mils and 6 mils, respectively. The default underfill used is Hysol FP4520.

The following section contains parametric curves generated by the fatigue model described above. The open circles in the plots indicate points generated by the model in order to produce smooth continuous curves. The closed squares represent experimentally measured data points, and are included when available.

Results

Figure 4 shows predicted fatigue life as a function of die size. Note that die size is expressed by the distance from the center of the chip to the location of the corner-most bump; i.e., the distance of bump to neutral point (DNP). (A one inch square chip has a DNP of approximately 700 mils.) It is clear from Figure 4 that fatigue life is very sensitive to DNP for the non-underfilled case, but independent of DNP for the underfilled case. This phenomena may be explained through a straightforward mechanical assessment of the solder joint loading mechanisms as follows.

Recall that solder fatigue is induced due to the thermal mismatch of materials joined to the solder. Two types of mismatch must be considered: local and global. Define local mismatch as the mismatch between the solder and the die. This contribution to fatigue is the same for both the underfilled and non-underfilled cases, and is independent of die size. (For the underfilled case, an additional local mismatch exists between the underfill and solder that is not considered in the present discussion, but is nonetheless independent of die size.) For the non-underfilled case, global mismatch refers to the CTE mismatch between the die and the substrate. This mismatch generates shear deformation in the solder joint, and is the primary source of damage. The total shear strain γ in the solder joint is directly proportional to DNP,

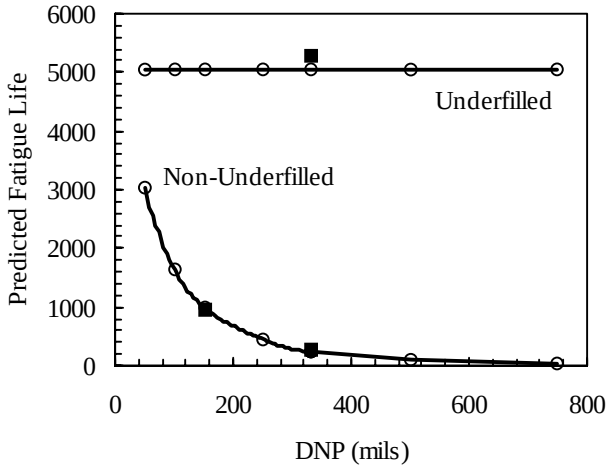

Figure 4. Predicted fatigue life as a function of die size (expressed as DNP).

$$\gamma \propto \frac{DNP}{h}\Delta T\Delta\alpha \qquad (5)$$

where ΔT is the thermal profile, $\Delta\alpha$ is the CTE mismatch between die and substrate, and h is the solder joint height. Clearly, if DNP is increased, the shear deformation increases, and fatigue life decreases.

For the underfilled case, the solder damage due to global mismatch is dominated by tensile deformation generated by out-of-plane expansion of the underfill. Because the effective stiffness of the underfill is so much greater than that of the solder joints, the joints tend to move with the expanding underfill. The total tensile strain ε in the solder is then proportional to the underfill CTE α_{UF} as

$$\varepsilon \propto \Delta T\alpha_{UF} \qquad (6)$$

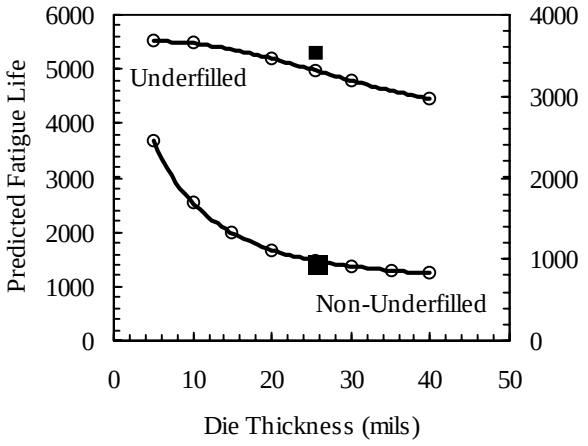

Figure 5. Predicted fatigue life as a function of die thickness.

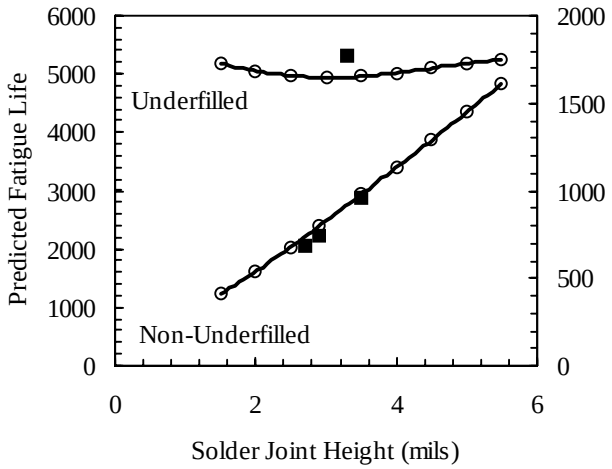

Figure 6. Predicted fatigue life as a function of solder joint height.

The tensile deformation described in Equation (6) is not dependent on die size. Hence, fatigue life is independent of DNP for the underfilled case, as seen in Figure 4.

It should be pointed out that while global mismatch is the primary loading (i.e., damage) mechanism present in the non-underfilled case, comparable (and small) contributions due to global and local mismatch exist in the underfilled case. Coupled with Equations (5) and (6) describing global mismatch, this fact explains the difference in loading conditions between the two cases noted earlier.

Underfilled and non-underfilled fatigue life as a function of die thickness is shown in Figure 5. Note that the underfilled results are plotted against the left axis, while the non-underfilled results are plotted against the right. Consider the non-underfilled case. In general, flexing of the substrate and die dissipates energy that otherwise would be absorbed by the solder joints. Hence, the worst case scenario for a solder joint occurs when the die and substrate each have a relative stiffness such that the amount of flexure in both is minimized. The maximum amount of energy is then absorbed by the solder joint, resulting in the lowest fatigue life. Increasing the die thickness increases the effective stiffness of the die. The resulting decrease in die flexure means more energy is absorbed by the solder joints, yielding lower fatigue life. If the die thickness were further increased it would eventually reach a point where it becomes infinitely stiff relative to the substrate. Fatigue life would then level off at a minimum. This mechanism is demonstrated in Figure 5. For very thin die, fatigue life is high. As die thickness is increased, fatigue life decreases. Beyond a die thickness of 30 mils, however, fatigue life levels off as the die becomes increasingly stiff compared to the substrate. The same phenomena is seen for the underfilled curve. The difference being that the curve has not yet leveled off at a 40 mil die thickness.

It should be noted that for die thickness approaching zero, the non-underfilled fatigue life goes to infinity. That is because both local and global CTE mismatch have been removed. For the underfilled case, a finite fatigue life is still predicted due to the remaining influence of tensile deformation generated by the underfill (see Equation (6)). Obviously these results are of interest only in the academic sense. The reality is that for a typical working range of die thickness, 15-30 mils, predicted fatigue lives vary roughly 20 percent, within experimental variation found in measured fatigue lives.

Predicted fatigue life as a function of solder joint height is shown in Figure 6. Again, underfilled results are plotted against the left axis and non-underfilled against the right. A strong dependence of fatigue life on solder joint height is observed for the non-underfilled case. This is consistent with Equation (5). The amount of shear strain decreases

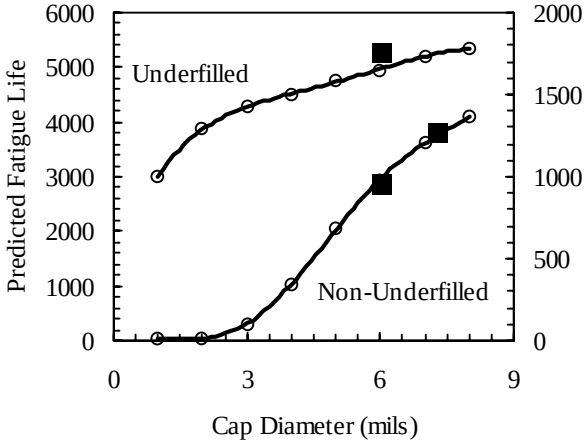

Figure 7. Predicted fatigue life as a function of cap diameter of the die/solder interface.

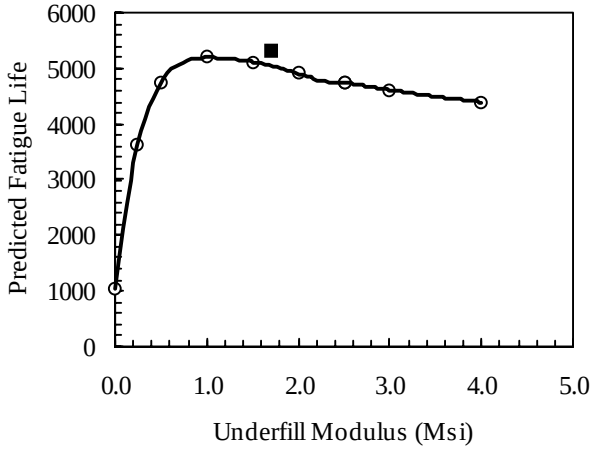

Figure 8. Predicted fatigue life as a function of underfill elastic modulus.

with increasing solder joint height, resulting in greater fatigue life. Equation (6), however, shows no dependence on solder joint height for tensile deformation found in the underfilled case. Indeed, consistent with this observation, Figure 6 shows underfilled fatigue life has little dependence on solder joint height.

Figure 7 shows fatigue life as a function of cap diameter of the die/solder interface, with underfilled and non-underfilled results plotted against the left and right axes, respectively. Recall that the cap diameter is defined as the diameter of the under bump metallurgy. As expected, fatigue life decreases with decreasing cap diameter for both underfilled and non-underfilled cases. However, the influence of cap diameter is much more pronounced for the non-underfilled case, where a change from 3 mil to 6 mil diameter increases fatigue life tenfold. In contrast, an equivalent change in cap diameter for an underfilled part only increases fatigue life approximately 15 percent.

Figures 8 and 9 show the influence on fatigue life of underfill elastic modulus and CTE, respectively. It should be pointed out that it is inaccurate to assume that the elastic modulus of underfill remains constant over temperature. Indeed, the elastic modulus of underfill will significantly vary with temperature, even below the glass transition phase. The modulus of FP4520, as measured from tensile tests, decreases by a factor of six going from -60 to 150°C. Hence, it is hard to

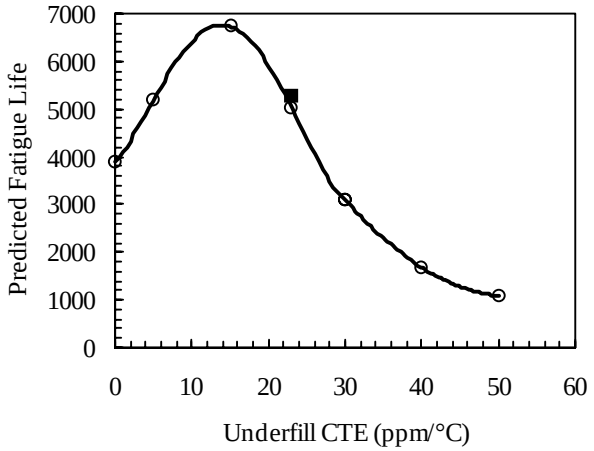

Figure 9. Predicted fatigue life as a function of underfill coefficient of thermal expansion.

capture the influence of such a material property. The modulus values used in Figure 8 should be considered an average value over the temperature -50/150°C profile. For most underfills, the typical elastic modulus measures between 1-2 Msi. As is seen from the curve, fatigue life varies insignificantly in this range.

In contrast to elastic modulus, it is reasonable to expect the underfill CTE to remain constant below the glass transition temperature (Tg). (The Tg for FP4520, for example, is approximately 150°C.) Hence, if it is assumed that the underfill remains below its Tg, then the influence of CTE on fatigue life may be evaluated as shown in Figure 9. Note

that the underfill CTE has a strong influence on fatigue life. This observation is consistent with Equation (6), which describes the tensile deformation generated in the solder joint by the out-of-plane expansion of the underfill. For typical underfills, CTE values range from 20-40 ppm/°C. Predicted fatigue lives decrease roughly by a factor of three over this range. Equation (6) would dictate that fatigue life should continue to increase with decreasing underfill CTE. However, Figure 9 shows an optimum CTE of approximately 14 ppm/°C where fatigue life is maximized. Decreasing CTE further results in a lower fatigue life. This points to an interaction of underfill CTE on the local mismatch of the solder with the silicon and the underfill itself.

Conclusions

A solder fatigue model has been generated for the 63Sn/Pb solder alloy which correlates the amount of creep strain energy dissipated with cycles to failure. The model characterizes the creep fatigue phenomena of the solder due to thermal cycling. The model incorporates nonlinear finite element modelling to generate hysteresis curves from which the dissipated creep energy may be calculated, and correlates these values with experimentally measured fatigue lives of various flip chip assemblies. The resulting fatigue model has been shown to be valid for different die sizes, substrate materials and solder joint geometries. In addition, the model has been validated for flip chips with and without underfill.

The solder fatigue model has been employed in a parametric study looking at the effect of flip chip design parameters on fatigue life. The analyses were carried out for flip chips with and without underfill. When possible, the resulting parametric curves were validated with measured fatigue lives. The results clearly show that the underfilled flip chip has significantly greater fatigue life. The results also show that the fatigue life of non-underfilled flip chips is highly dependent on die size, solder joint height and cap diameter. These effects can be explained by looking at the mechanics of the loading present in the non-underfilled case, and are readily handled by the solder fatigue model.

For underfilled applications, little or no effect on fatigue life was seen for varying die size, die thickness, solder joint height or cap diameter. In fact, underfill CTE appears to be the only parameter studied which will significantly change the fatigue response of a given flip chip application. This would indicate the importance of maintaining operating temperatures below the underfill glass transition phase. Above Tg, elastic modulus decreases an order of magnitude, while CTE can increase by a factor of three, or greater. Figures 8 and 9 show that both these trends adversely effect fatigue life.

It is common practice to match underfill CTE with that of solder, with the belief that fatigue life will be optimized. If one were to consider only global mismatch, Equation (6) could be used to argue for this practice. However, as stated above, an interaction exists bewteen the underfill CTE and local mismatch of the solder. This interaction is strong enough to reduce the optimal CTE to 14 ppm/°C, as seen in Figure 9. (The CTE of 63Sn/Pb solder is approximately 23 ppm/°C.) At an underfill CTE of 14 ppm/°C, the total damage in the solder is minimized, resulting in optimal fatigue life. Optimizing underfill CTE, then, is not just a function of solder alloy, but rather a function of the design of the entire flip chip application.

This investigation has introduced a 63Sn/Pb creep fatigue model, as well as a parametric study of the flip chip on ceramic application. Future work will investigate the influence of solder alloy on creep fatigue, and quantify the influence of design parameters for organic circuit board applications.

Acknowledgments

The author wishes to express gratitude to his Delco Electronics colleagues Curt Erickson and Frank Stepniak for their guidance and unabashed critiques throughout this investigation. Additional acknowledgments go out to Shing Yeh for generating the experimental fatigue data necessary to define the solder fatigue model, and to Paul Staab for generating the tensile properties of the Hysol FP4520 underfill used in the finite element analysis.

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Presented at the 1997 International Electronics Manufacturing Technology Symposium
Austin, Texas, October 13-15, 1997, pp. 299-307