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DESIGN AND MANUFACTURING OF MICRO VIA-IN-PAD SUBSTRATES FOR SOLDER BUMPED FLIP CHIP APPLICATIONS

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A novel and low-cost micro via-in-pad (VIP) substrate for supporting a solder bumped flip chip is presented in this study. Emphasis is placed on the design, materials, process, manufacturing, and reliability of the micro VIP substrate of a chip scale package (CSP), and of the micro VIP CSP printed circuit board (PCB) assembly. Cross-sections of samples are examined for a better understanding of the solder bump, CSP redistribution, VIP, and solder joint. Non-linear finite element analyses are used to determine the stress and strain in the copper VIP and the solder joint. Time-dependent non-linear analysis is used to predict the thermal-fatigue life of the VIP solder joint.

1. Introduction

The past decade witnessed an explosive growth in the research and development efforts devoted to flip chip in a plastic package and flip chip on a printed circuit board (PCB) as a direct result of the higher requirements for package density, performance, and interconnection and the limitations of face-up wire bonding technology. Besides the build-up and micro-via technologies,[1,2] one of the solutions is via-in-pad (VIP). In this study, the design, analysis, assembly, and modeling of a novel VIP substrate for housing a solder bumped flip chip in a CSP (chip scale package) format are presented.

Because of the special design, the substrate consists of a single core of organic material and two-metal layers of copper and is manufactured with the conventional PCB fabrication process at a very low cost. Furthermore, the vias are drilled with laser, thus, very small hole-size (0.15 mm to 0.1 mm) can be achieved.

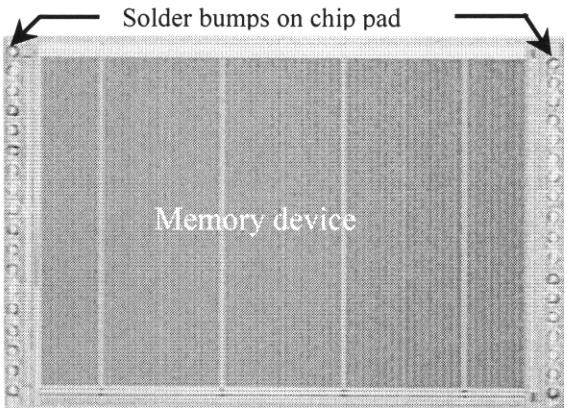
The proposed substrate is used to support a functional 32-pin, low-power, high-speed static random access memory (SRAM). The assembled VIP CSP is soldered on a PCB. Non-linear time-temperature-dependent finite element method is performed for the thermal stress analyses as well as the solder joint life prediction.

2. IC Wafer of the 32-pin SRAM

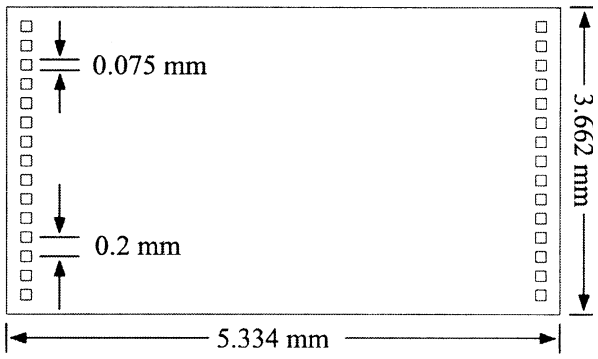
The functional 32-pin SRAM [Figs. 1(a) and 1(b)], is designed and manufactured with very high yield and at a low cost by United Microelectronics Corporation (UMC) on an 8″ wafer. The major function of this SRAM chip is for very high speed and low power applications. The major characteristics of the chip for designing the Cu VIP are listed as follows:

- Chip sizes are 5.334 mm × 3.662 mm;
- Pad sizes are 0.075 mm × 0.075 mm;
- Pad pitch is 0.195 mm (minimum);
- Chip thickness is 0.675 mm;
- Chip pads are distributed along two shorter sides;
- Two pads for ground and two pads for power.

*On sabbatical leave from Hong Kong University of Science & Technology.



(a)



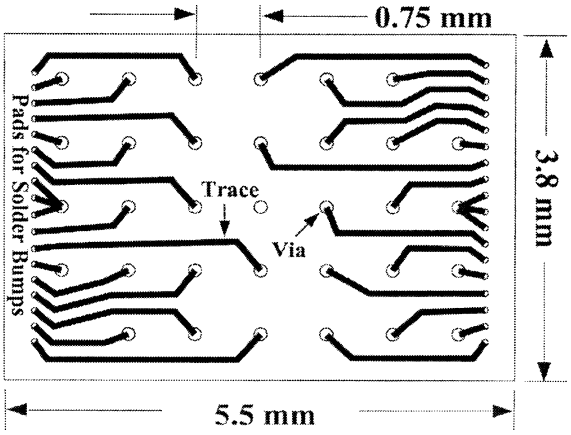
(b)

Fig. 1. (a) SRAM chip with solder bumps, (b) dimensions of the chip.

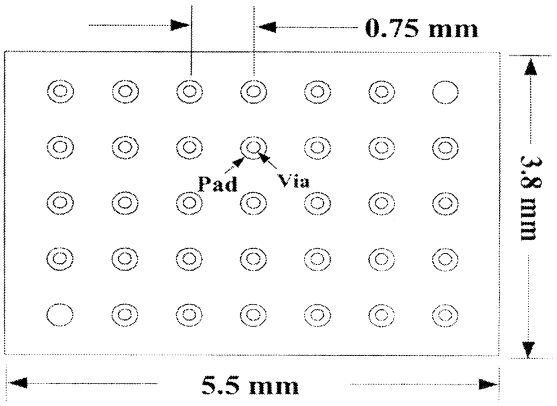
3. VIP Substrate

A novel VIP substrate has been designed for the 32-pin SRAM. Figures 2(a) and 2(b) show, respectively, the top and bottom sides of the substrate, which is a 0.164 mm thick high glass transition temperature organic material. It can be seen from the top-side that the traces from the peripheral pads are redistributed inward (fan-in) and connected to the copper pads on the bottom-side of the package substrate through the μvias. The diameter of the μvias is less than 0.15 mm and the diameter of the copper pads is 0.32 mm. The dimensions of the VIP substrate are: 5.5 mm$\times$3.8 mm$\times$0.164 mm. The pitch of the VIP is 0.75 mm. The VIP substrate designed in this study is manufactured by the key process steps shown in Fig. 3. The raw material is the bismaleimide triazene (BT) HL832 and the core thickness is 0.1 mm. The major process steps are as follows.

Step 1: Use mechanical drill to make holes for handling and referencing.



(a)



(b)

Fig. 2. (a) Top side of the VIP substrate, (b) bottom side of the VIP substrate.

Step 2: Apply a 30 μm thick dry film photoresist on the Cu and open a 150 μm diameter circle for each μvia.

Step 3: Pre-etch the copper foil at positions where μvias are to be formed.

Step 4: Use CO_2 laser to drill holes on the BT substrate.

Step 5: Electroplate copper to 25 ± 5 μm thick.

Step 6: Plug in non-conductive ink (S 500-R01).

Step 7: Apply photoresist and circuit layout mask, then use photolithography technique to make pads, traces, and Cu rings.

Step 8: Inspection.

Step 9: Print and cure solder mask to 15 $+10/-5$ μm thick.

Step 10: Electroless Ni/Au plating.

Step 11: Route the large panel to 172 mm$\times$60 mm panels.

Step 12: Final inspection.

Figures 4(a) and 4(b) show the top and the

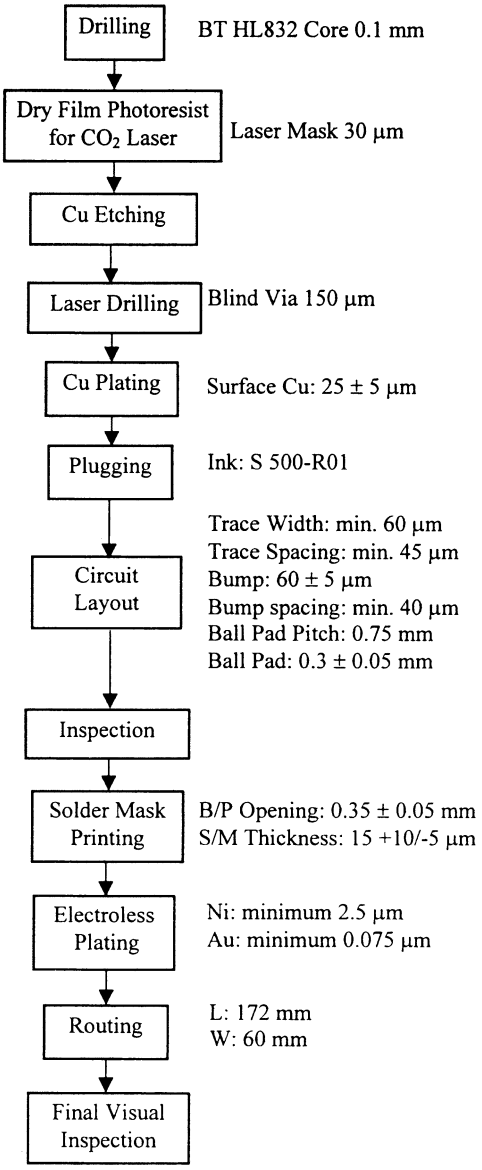
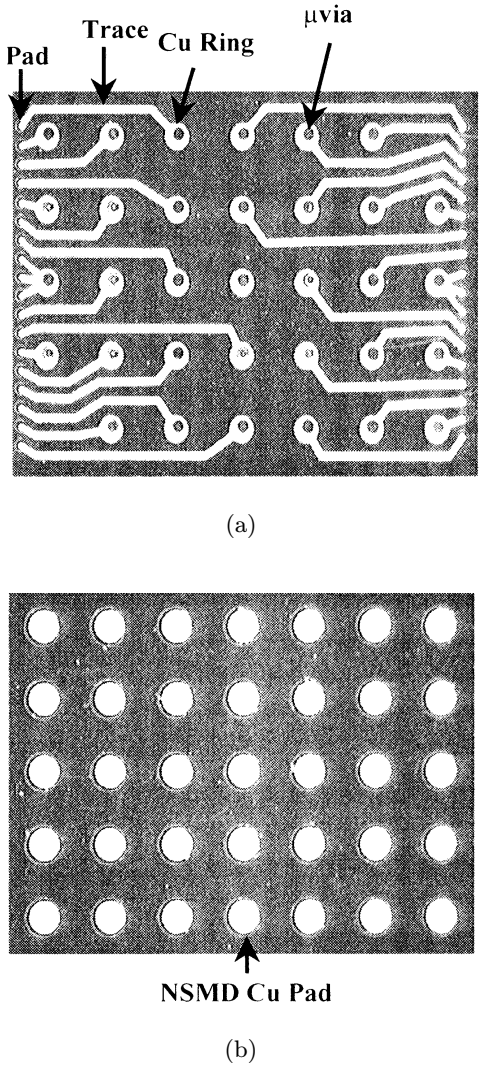


Fig. 3. Key process steps for making the VIP substrate.



(a)

(b)

Fig. 4. (a) Top side of the VIP substrate and (b) bottom side of the substrate.

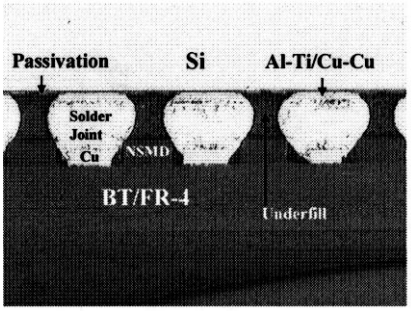
bottom sides of the VIP substrate for the 32-pin solder bumped flip chip SRAM. It can be seen that they are very simple (no dog-bone pads) and, hence, the manufacturing cost is relatively low.

4. Solder Bumped Flip Chip on VIP Substrate

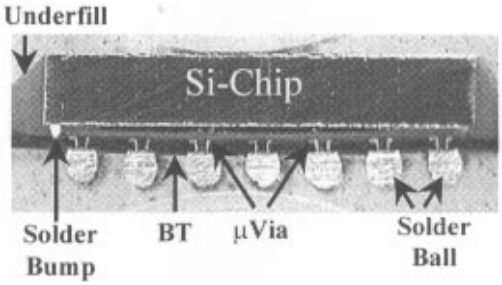
The assembly process of VIP substrate with the 32-pin SRAM is very similar to that of the NuCSP reported in Refs. 3 and 4, except that in this study solder balls are mounted on the VIP substrate. Figures 5(a), 5(b) and 5(c) show the cross sections of the CSP with the present VIP substrate. Figure 5(a) shows the cross section along the chip pads. Figure 5(b) shows the cross section along the VIP, and Fig. 5(c) shows the schematics. Detailed dimensions will be shown in the finite element modeling section.

5. PCB Assembly of the VIP CSP

Figure 6 shows the FR-4 epoxy-glass PCB for this study. It can be seen that there are two different kinds of solder-mask layout on the copper pads. These are solder mask defined (SMD) copper pads and non-solder mask defined (NSMD) copper pads. The assembly process of the VIP CSP on the PCB is very similar to that of the conventional no-clean surface mount technology (SMT).[5–8] In the following sections, some of the major steps are discussed.



(a)



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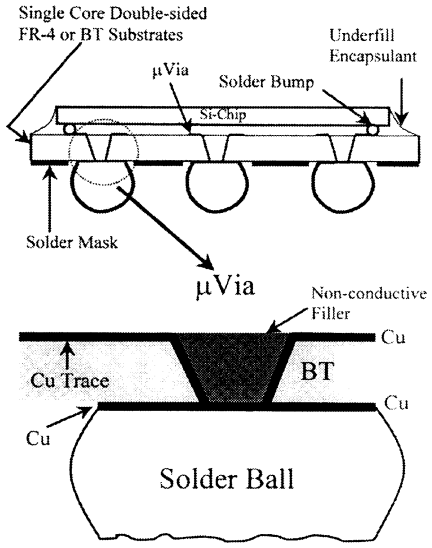


(c)

Fig. 5. VIP CSP cross sections. (a) Along the chip pads, (b) along the VIP, and (c) schematic of the VIP solder joint.

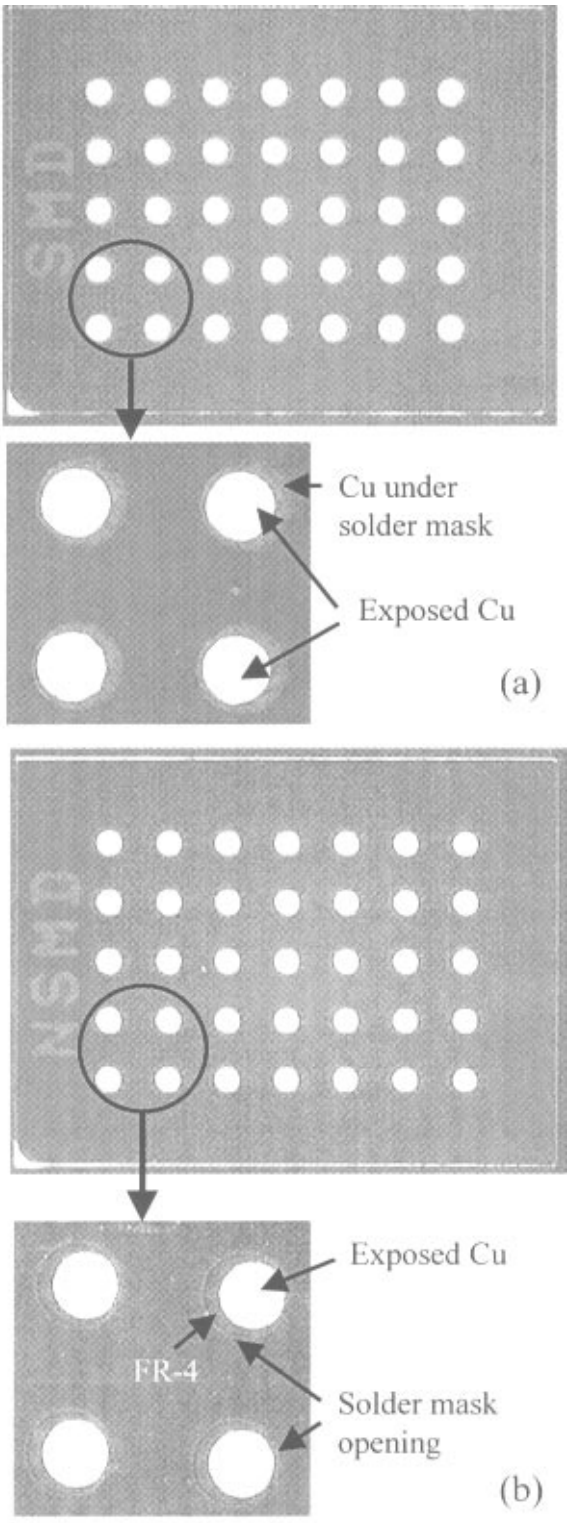
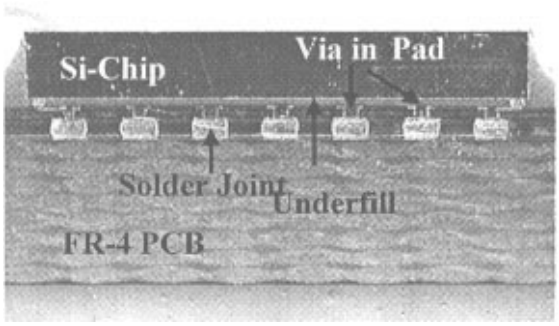


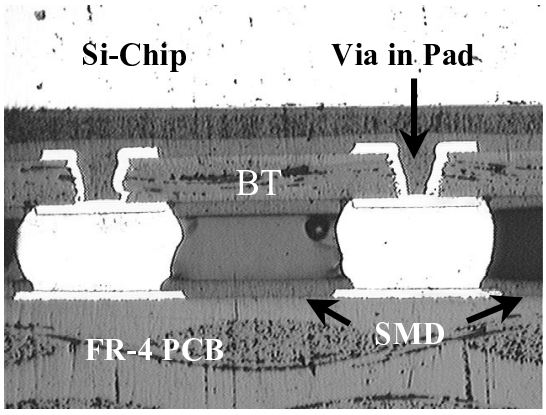
Fig. 6. (a) SMD PCB and (b) NSMD PCB.

Before fluxing and pick-n-place, both the VIP CSP and the PCB are cleaned with isopropanol to reduce particle contamination. In this study, a no-clean flux is applied to the PCB only. The pick-n-place of the chip is performed on an IC mounter with a look-up and look-down camera for alignment. The alignment accuracy is within 12 μm. After alignment, the CSP is put down on the PCB.

After fluxing and pick-n-place, the VIP CSP on PCB is placed on the conveyor belt of a reflow



(a)



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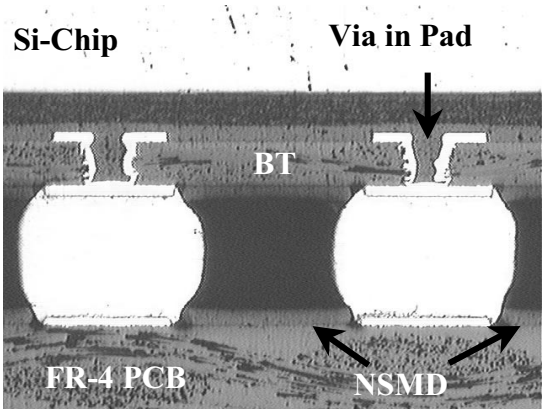

(c)

Fig. 7. (a) Cross section of the VIP CSP PCB assembly, (b) with SMD copper pads, and (c) with NSMD copper pads.

oven. The maximum temperatures of 230 to 237°C are achieved during the reflow process. Also, the time durations above 161 and 183°C for the soldering are, respectively, 132 to 146 sec and 47 to 66 sec. The belt speed is 0.95 m/min.

Figures 7(a), 7(b) and 7(c) show the cross sections of the VIP CSP PCB assembly. Figure 7(b) is with SMD copper pads on the PCB, while Fig. 7(c) is with NSMD copper pads on the PCB. (In this study, the solder balls before reflow in Fig. 7(c) are larger than those shown in Fig. 7(b).) In both cases, it is very easy to do the PCB assembly with very high yield. Figure 8 shows the cross sections of VIP CSP PCB assemblies with both solder bump on the chip and solder joint on the PCB. It can be seen that, since there are no dog-bone pads, the micro VIP design can save plenty of space on the substrate.

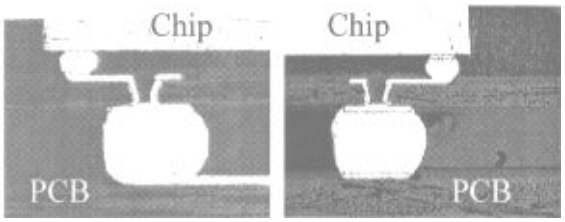

Fig. 8. Cross sections showing the solder bump, copper VIP, and solder joint.

6. Elasto-Plastic Analysis of the VIP

Detailed dimensions of the VIP solder joint are shown in Fig. 9. The commercial finite element code ANSYS version 5.5 is employed in this study. A two-dimensional model is established using the 8-node plane strain elements. It should be noted that all detailed assembly structures such as the chip, underfill, solder mask, BT substrate, Cu VIP, solder joint,

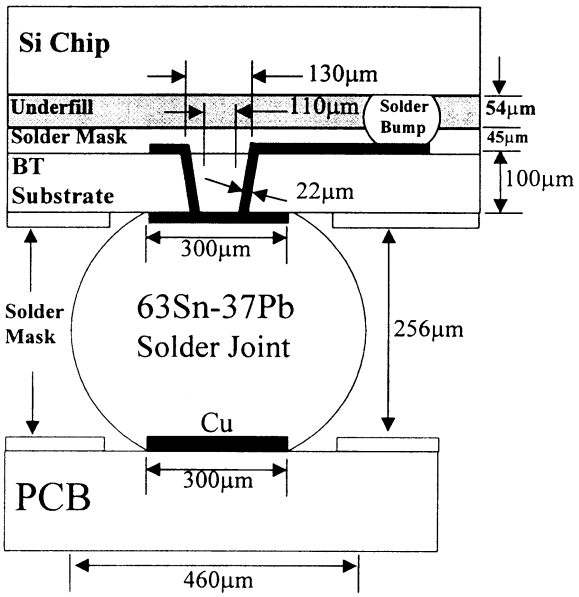

Fig. 9. Details of the VIP solder joint.

Cu pads, and FR-4 PCB are modeled in the finite element analysis. Besides, due to the symmetry in the assembly structure, only one half of the cross-section is considered.

The material properties used in the computational modeling are shown in Table 1. The copper VIP is considered as an elasto-plastic material (yield stress = 54 MPa, yield strain = 0.0007, Young's modulus = 76 GPa, and the slope of the plastic curve is 0.1). The eutectic solder (63Sn-37Pb) is assumed to be a temperature-dependent elasto-plastic materials.[5] All other constituents are considered as linear elastic materials. The temperature cycling condition in this study is shown in Fig. 10. For the present elasto-plastic analysis, a temperature loading of 25°C to 110°C is applied.

Table 1. Material properties of the VIP CSP PBC assembly.

Material Properties	Young's Modulus (GPa)	Poisson's Ratio (ν)	Thermal Expansion Coefficient (α) ppm/°C
FR4 Substrate	22	0.28	18.5
Copper	76	0.35	17
63Sn-37Pb Solder	See note	0.4	21
Underfill	6	0.35	30
Silicon Chip	131	0.3	2.8
Solder Mask	6.9	0.35	19
μvia Filler	7	0.3	35
BT	26	0.39	15

Note: Young's modulus as well as stress-strain relationships of solder are temperature-dependent.

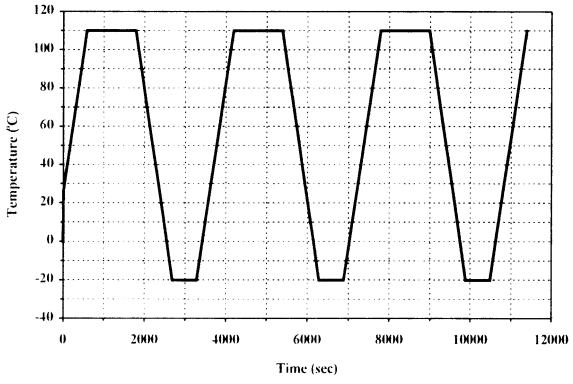

Fig. 10. Temperature profile for modeling.

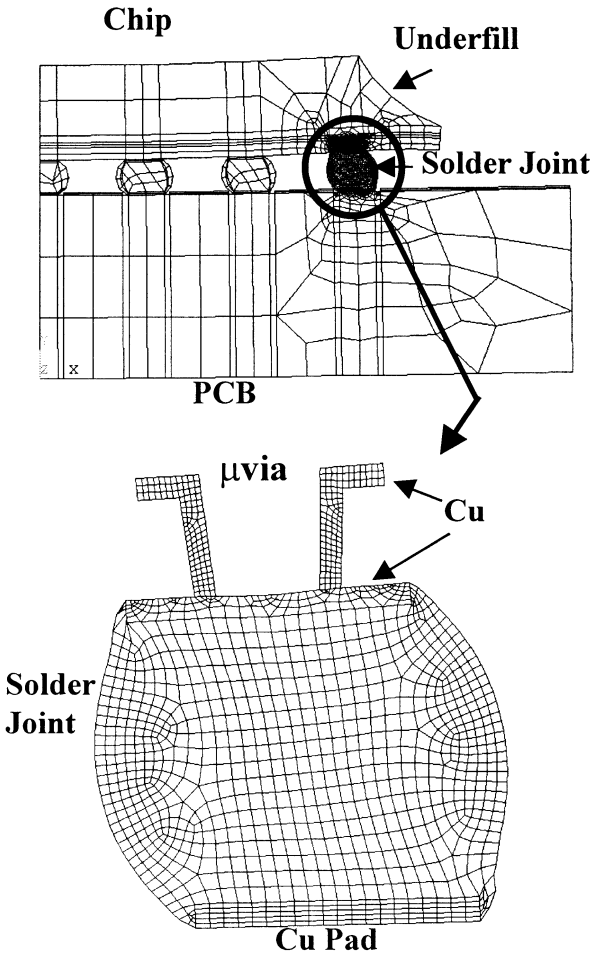

Fig. 11. Deformed shape of the VIP CSP PCB assembly.

A typical deformation of the VIP CSP PCB assembly is shown in Fig. 11. It can be seen that the maximum relative deformation (dominated by shear) appears at the corner VIP solder joint. This is due to the thermal expansion mismatch between the chip-BT substrate, PCB, and a raising temperature loading.

The distribution of von Mises stress and accumulated equivalent plastic strain range at the corner VIP solder joint are shown in Figs. 12 and 13, respectively. It can be seen that the maximum values in the corner VIP solder joint are located at the corner interface between the lower left corner of the Cu VIP and the solder joint. However, these values are very small compared with those of flip chip on board or wafer level CSP assemblies without underfill. This is because the thermal expansion mismatch between the FR-4 PCB and the BT substrate is very small.

The von Mises stress contour distribution in the Cu VIP is shown in Fig. 14. It can be seen that the

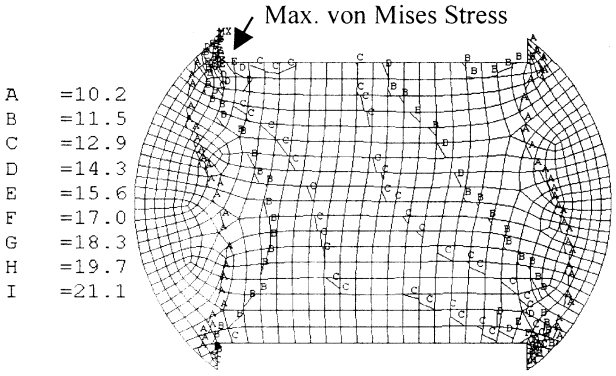

Fig. 12. Maximum von Mises stress in the VIP solder joint.

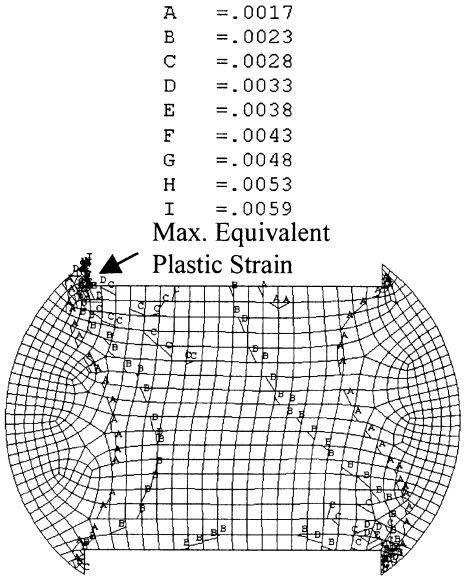

Fig. 13. Maximum equivalent plastic strain in the VIP solder joint.

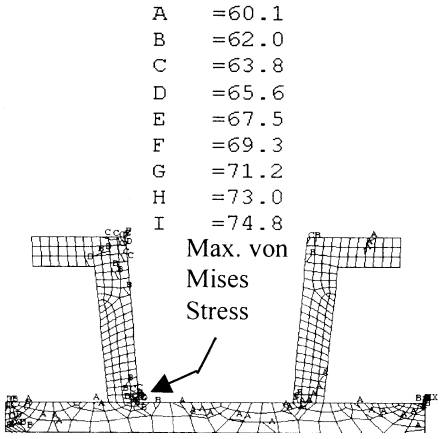

Fig. 14. von Mises stress in the copper VIP.

maximum von Mises stress appears at the lower left inner corner, and is equal to 74.8 MPa. This is much smaller than the strength of Cu, which is in the range of 200 MPa.

7. VIP Solder Joint Reliability with Creep Analysis

The Garofalo-Arrhenius steady-state creep is generally expressed by[8]

$$\frac{d\gamma}{dt} = C\left(\frac{G}{\theta}\right)\left[\sinh\left(\omega\frac{\tau}{G}\right)\right]^n \exp\left(\frac{-Q}{k\theta}\right) \qquad (1)$$

where γ is the steady-state creep shear strain, $d\gamma/dt$ is the steady-state creep shear strain rate, t is the time, C is a material constant, G is the temperature dependent shear modulus, θ is the absolute temperature (K), ω defines the stress level at which the power law stress dependence breaks down, τ is the shear stress, n is the stress exponent, Q is the activation energy for a specific diffusion mechanism, and k is the Boltzmann's constant. For 60Sn–40Pb solder, the creep constitutive equation has been determined by Darveaux and Banerji[8] as shown in Fig. 15.

The temperature loading imposed on the VIP CSP PCB assembly is shown in Fig. 10. It can be seen that for each cycle (60 minutes) the temperature condition is between −20°C and 110°C with 15 minutes ramp, 20 minutes hold at hot, and 10 minutes hold at cold. Three full cycles of analysis are performed.

The deformed shape is very similar to that of the elasto-plastic analysis. Also, the maximum shear stress and creep shear strain responses appear in the corner joint at the corner interface between the lower left corner of the Cu VIP and the solder joint.

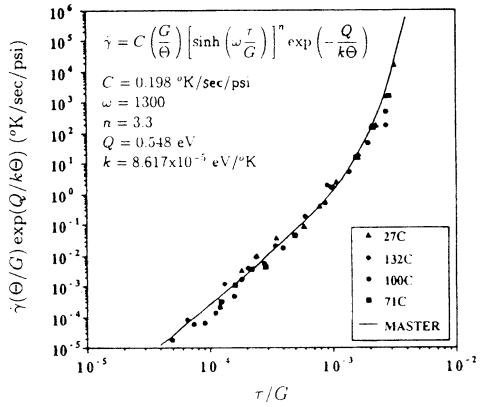

Fig. 15. Creep constitute equation for the 60Sn-40Pb solder.

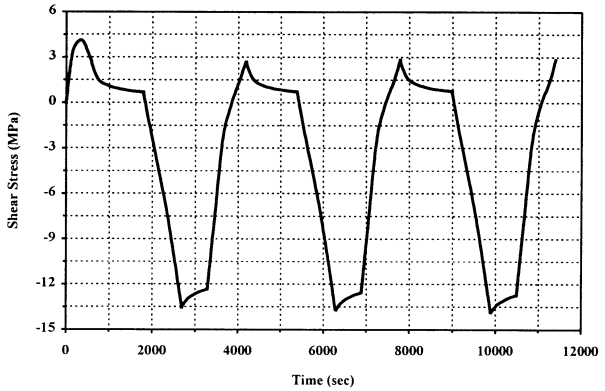

Fig. 16. Time-dependent shear stress at the VIP solder joint's critical location.

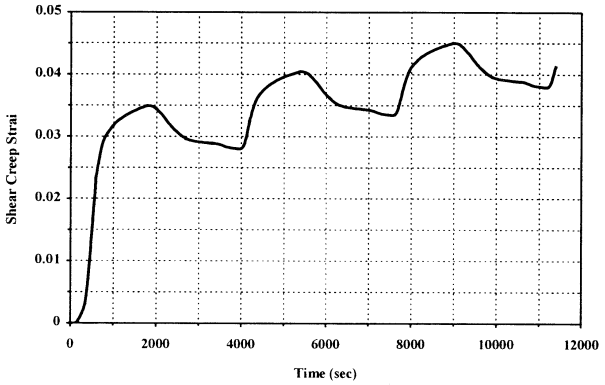

Fig. 17. Time-dependent shear creep strain at the VIP solder joint's critical location.

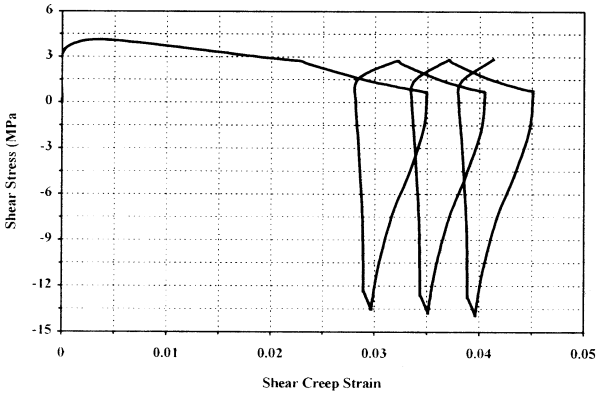

Fig. 18. Hysteresis loops of the shear stress and creep shear strain at the VIP solder joint's critical location.

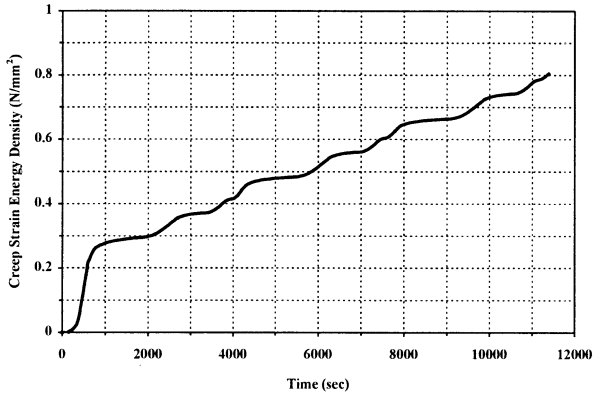

Fig. 19. Time-dependent creep strain energy density at the VIP solder joint's critical location.

For the time dependent analysis, it is important to study the responses for multiple cycles till the hysteresis loops become stabilized. The shear stress and shear creep strain of three cycles at the maximum location are shown in Figs. 16 and 17, respectively. Figure 18 shows the shear stress and shear creep strain hysteresis loops for multiple cycles. It can be seen that the creep shear strain is quite stabilized after the first cycle. Figure 19 shows the time history of creep strain energy density at the VIP solder joints' critical location for three cycles. The average creep strain energy density per cycle (ΔW) can be obtained by averaging the creep strain energy density of the last two cycles, which is $0.189\ \mathrm{N/mm^2} = 27.4$ psi.

Once we have ΔW, the thermal fatigue crack initiation life (N_0) can be estimated from (Darveaux) Equation (13.35) of Ref. 8,

$$N_0 = 7860\Delta W^{-1} = 287 \text{ cycles} \qquad (2)$$

and the thermal fatigue crack propagation life (N) based on the linear fatigue crack growth rate theory can be estimated from (Darveaux) Equation (13.36) of Ref. 8,

$$da/dN = 4.96 \times 10^{-8}\Delta W^{1.13} \qquad (3)$$

or

$$N = N_0 + (a_f - a_0)/(4.96 \times 10^{-8}\Delta W^{1.13}) \qquad (4)$$

where a is the crack length of the solder joint; a_0 is the initial crack length, which is assumed to be zero; and a_f is the final crack length. It can be seen that in order to determine N we need to choose an a_f. For example, if $a_f = 0.347$ mm (solder cracks through near the bottom of the Cu VIP), then $N = 6,842$ cycles. On the other hand, if $a_f = 0.433$ mm (solder cracks through the diagonal of VIP solder joint, i.e., from the corner interface between the lower left corner of the Cu VIP and the solder joint to the lower right corner interface between the upper right corner of the Cu pad on the PCB and the solder joint), then $N = 8,421$ cycles.

It should be pointed out that, due to a numerical integration scheme error in the old version of the finite element code ANSYS, Darveaux' thermal-fatigue life prediction equations may involve errors as high as 16%.[9]

8. Summary

A simple VIP substrate for solder bumped flip chip applications has been presented. It is a single core two-side structure with micro vias in pads to which solder balls are attached. Dog-bone-pad structure is not needed and, thus, there is more space for routing.

The application of the VIP substrate is demonstrated by housing a SRAM device in a CSP format. It is found that the solder bumped SRAM chip is very easy to be assembled on the VIP substrate, and the solder balls are very easy to be mounted on the copper VIP. Also, the VIP CSP is very easy to be assembled on the SMD and NSMD PCB.

The thermal stress in the copper VIP is calculated by a non-linear finite element analysis. It is found that the maximum von Mises stress in the copper VIP is much less than the strength of Cu. Thus, under the thermal loading condition (25°C to 110°C), the copper VIP should be reliable in most of the operating conditions.

The thermal-fatigue life of the VIP solder joint is predicted by a creep analysis and Darveaux's empirical equation. It is found that the average creep strain energy density is very small at the corner solder joint, and thus the VIP solder joints should be reliable.

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