VGA Documentation

Goal is to create synchronization between pixel assignment with framerate and refresh rate by using suitable Hsync, Vsync, and sync pulse with suitable display, front porch and back porch dimensions.

Definitions:

Horizontal Synchronization: HSYNC is a signal given to the monitor telling it to stop drawing the current horizontal line, and start drawing the next line. The amount of time this takes to occur is measured in Hz (Hertz), which is a measure of cycles per second.

Vertical Synchronization: VSYNC will tell the beginning of frame to synchronize frame with refresh rate

Front porch: it is an interval period between the end of picture information and start of horizontal pulse

Back porch: it is the duration between end of horizontal pulse and start of the next line with video information

Sync Pulse: is to maintain synchronism of lines together.

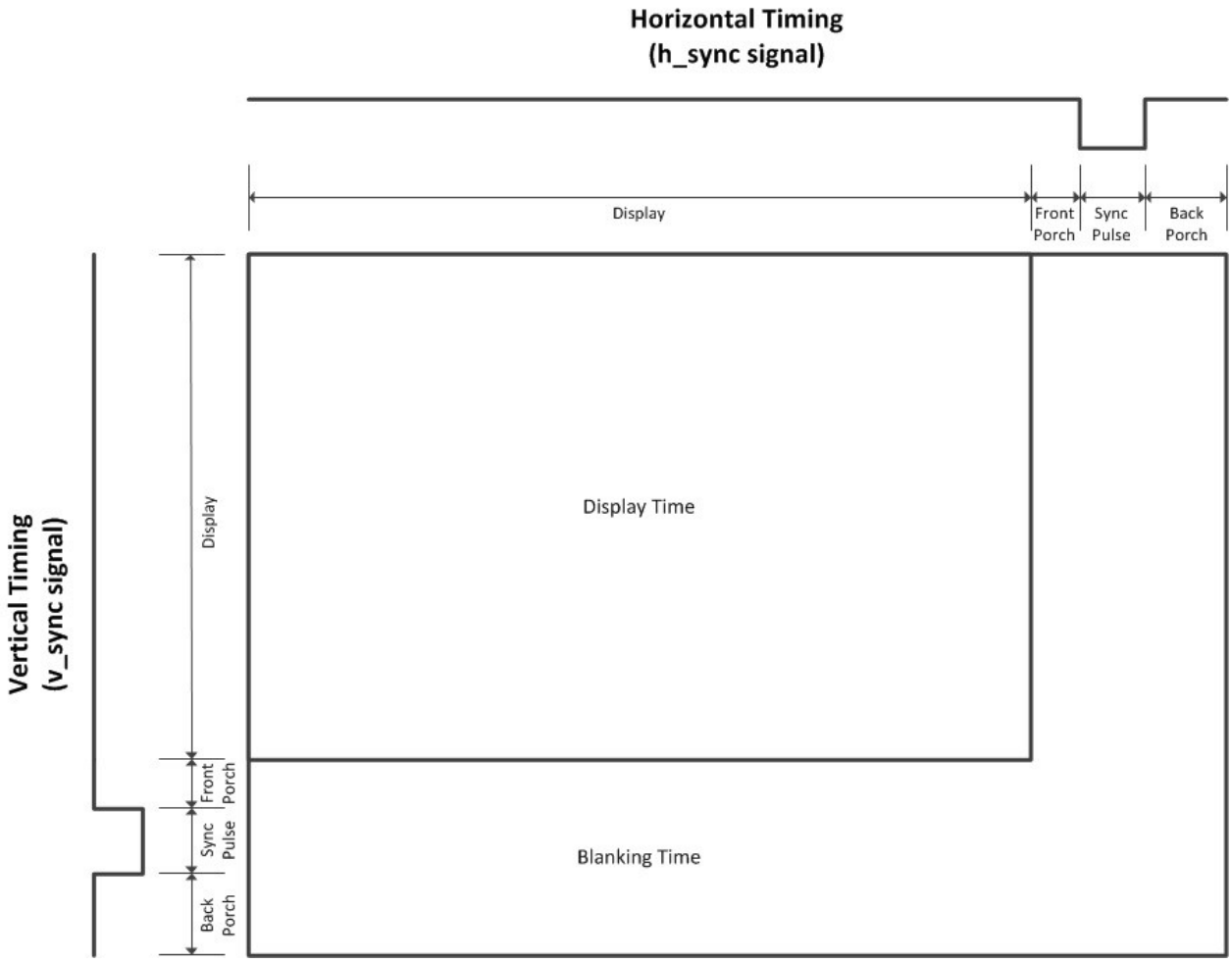
Process:

Pixels are obtained from the Vram. Each pixel is assigned its location by synchronizing its horizontal location with its vertical one, to do so each line of pixels is put till the line reaches the front porch. Once it reaches the front porch the line stops and any incoming signals are erased. There is also the back porch which creates enough time for the pixel to reach its suitable place in the second line for it to start forming. In the same time the synchronization pulse is given to keep everything in sync with each other.

Each monitor has a refresh rate, and the frames created (a display full of pixels) must be aligned and synchronized with the refresh rate. Vsync is done to assure this process goes smoothly.

This is a graphical presentation of the total size to the display size.

Total size = Display + front porch + back porch + sync pulse



Our display is 400x300, however this is not a standard. So the closest standard display is 800x600 at 40 MHZ clock cycle (as shown in the picture below). So if we half the clock cycle given it gives you half the display given which is what is required.

SVGA Signal 800 x 600 @ 6

General timing

Screen refresh rate	60 Hz
Vertical refresh	37.878787878788 kHz
Pixel freq.	40.0 MHz

Horizontal timing (line)

Polarity of horizontal sync pulse is positive.

Scanline part	Pixels	Time [µs]
Visible area	800	20
Front porch	40	1
Sync pulse	128	3.2
Back porch	88	2.2
Whole line	1056	26.4

Vertical timing (frame)

Polarity of vertical sync pulse is positive.

Frame part	Lines	Time [ms]
Visible area	600	15.84
Front porch	1	0.0264
Sync pulse	4	0.1056
Back porch	23	0.6072
Whole frame	628	16.5792

Code Framework (with comments for clarification):

Thursday, March 19, 2020 8:12 PM

vsynchsync.vhd Thu Mar 19 20:12:28 2020

```
 1
 2  LIBRARY ieee;
 3  USE ieee.std_logic_1164.all;
 4
 5  ENTITY vsynchsync IS
 6     GENERIC(
 7        h_pulse  :  INTEGER := 128;      --horiztonal sync pulse
 8        h_bp     :  INTEGER := 88;    --horiztonal back porch (left part of scree
 9        h_pixels :  INTEGER := 800;      --horiztonal display
10        h_fp     :  INTEGER := 40;    --horiztonal front porch (right part of
   screen)
11        h_pol    :  STD_LOGIC := '0';    --horizontal sync pulse polarity (1 =
   positive, 0 = negative)
12        v_pulse  :  INTEGER := 4;        --vertical sync pulse
13        v_bp     :  INTEGER := 23;       --vertical back porch (top part of scree
14        v_pixels :  INTEGER := 600 ;     --vertical display
15        v_fp     :  INTEGER := 1;        --vertical front porch (bottom part of
   screen)
16        v_pol    :  STD_LOGIC := '1');   --vertical sync pulse polarity (1 =
   positive, 0 = negative)
17
18     PORT(
19        pixel_clk   :  IN    STD_LOGIC;  --pixel clock at frequency of VGA mode
   being used
20        reset_n     :  IN    STD_LOGIC;  --active low asycnchronous reset
21        h_sync      :  OUT   STD_LOGIC;  --horiztonal sync pulse
22        v_sync      :  OUT   STD_LOGIC;  --vertical sync pulse
23        disp_ena    :  OUT   STD_LOGIC;  --display enable ('1' = display time,
   '0' = blanking time)
24        column      :  OUT   INTEGER;    --horizontal pixel coordinate
25        row         :  OUT   INTEGER;    --vertical pixel coordinate
26        n_blank     :  OUT   STD_LOGIC;  --direct blacking output to DAC
27        n_sync      :  OUT   STD_LOGIC); --sync-on-green output to DAC
28  END vsynchsync;
29
30  ARCHITECTURE behavior OF vsynchsync IS
31     CONSTANT h_period :  INTEGER := 1056;  --total number of pixel clocks in a r
32     CONSTANT v_period :  INTEGER := 628;  --total number of rows in column
33  BEGIN
34
35     n_blank <= '1';
36     n_sync <= '0';
37
38     PROCESS(pixel_clk, reset_n)
39        VARIABLE h_count  :  INTEGER RANGE 0 TO 1055 := 0;  --horizontal counter
   (counts the columns)
40        VARIABLE v_count  :  INTEGER RANGE 0 TO 627 := 0;  --vertical counter
   (counts the rows)
41     BEGIN
42
43        IF(reset_n = '0') THEN     --reset assert
44           h_count := 0;           --reset horizontal counter
45           v_count := 0;           --reset vertical counter
46           h_sync <= NOT h_pol;    --deassert horizontal sync
```

```
47            v_sync <= NOT v_pol;     --deassert vertical sync
48            disp_ena <= '0';         --disable display
49            column <= 0;             --reset column pixel coordinate
50            row <= 0;                --reset row pixel coordinate
51
52          ELSIF(pixel_clk'EVENT AND pixel_clk = '1') THEN
53
54            --counters
55            IF(h_count <1055) THEN      --horizontal counter (pixels)
56               h_count := h_count + 1;
57            ELSE
58               h_count := 0;
59               IF(v_count < 627) THEN  --veritcal counter (rows)
60                  v_count := v_count + 1;
61               ELSE
62                  v_count := 0;
63               END IF;
64            END IF;
65
66            --horizontal sync signal
67            IF(h_count < h_pixels + h_fp OR h_count >= h_pixels + h_fp + h_pulse)
    THEN
68               h_sync <= NOT h_pol;     --deassert horiztonal sync pulse
69            ELSE
70               h_sync <= h_pol;         --assert horiztonal sync pulse
71            END IF;
72
73            --vertical sync signal
74            IF(v_count < v_pixels + v_fp OR v_count >= v_pixels + v_fp + v_pulse)
    THEN
75               v_sync <= NOT v_pol;     --deassert vertical sync pulse
76            ELSE
77               v_sync <= v_pol;         --assert vertical sync pulse
78            END IF;
79
80            --set pixel coordinates
81            IF(h_count < h_pixels) THEN   --horiztonal display time
82               column <= h_count;         --set horiztonal pixel coordinate
83            END IF;
84            IF(v_count < v_pixels) THEN   --vertical display time
85               row <= v_count;            --set vertical pixel coordinate
86            END IF;
87
88            --set display enable output
89            IF(h_count < h_pixels AND v_count < v_pixels) THEN    --display time
90               disp_ena <= '1';                                  --enable display
91            ELSE                                                 --blanking time
92               disp_ena <= '0';                                  --disable displa
93            END IF;
94
95          END IF;
96       END PROCESS;
97
98    END behavior;
```