Fib.sim with –O0 optimization

Starting at PC 400168
Total number of dynamic instructions: 157
Total number of cycles: 221
  RType: 13
  IType: 143
  JType: 1
Number of Memory Reads: 63
Number of Memory Writes: 45
Number of Register Reads: 288
Number of Register Writes: 163
Number of Forwards:
  From Ex Stage: 35
  From Mem Stage: 53
Branches:
  Forward:
    Taken: 0
    Not taken: 0
  Backward:
    Taken: 10
    Not taken: 1
Branch delay slot:
  Useful instruction: 0
  Not useful instruction: 11
Jump delay slot:
  Useful instruction: 0
  Not useful instruction: 2
Load Use Hazard:
  Has load use stall: 51
  Has load use hazard: 0
  Has no load use hazard: 63
256 byte cache (blocksize 4 bytes): 103 hits, 5 misses (hit rate: 95.3704%)
256 byte cache (blocksize 8 bytes): 105 hits, 3 misses (hit rate: 97.2222%)
256 byte cache (blocksize 16 bytes): 106 hits, 2 misses (hit rate: 98.1481%)
256 byte cache (blocksize 32 bytes): 107 hits, 1 misses (hit rate: 99.0741%)
256 byte cache (blocksize 64 bytes): 107 hits, 1 misses (hit rate: 99.0741%)
256 byte cache (blocksize 128 bytes): 107 hits, 1 misses (hit rate: 99.0741%)
256 byte cache (blocksize 256 bytes): 107 hits, 1 misses (hit rate: 99.0741%)