(Computer Arch)

1) #100; ← unit = nano-second (Timescale ns)

2) $dumpfile ← use to create a file that contains dumped waveform.

3) $dumpvars ← use to define scope of dump.

4) $dumpvcd ← here "vcd" value change dump
It's an ASCII based format for dumpfile generated by EDA logic simulation tools.

5) $finish ← is a verilog system task that tells the simulator to terminate current simulation.

6) $random ← function call returns a 32-bit random num each time it's called.

7) always @* (posedge clk) ← is key to flip-flop generation

8) always @* ← blocks are used to describe events that should happen under certain contains. If
It follows by a set of parentheses, a begin some code, run on end.

9) @(posedge clk) ← always at the possitive edge of the clock.

10) reg ← is a verilog data type that can be synthesized into either sequential/combinational logic depending on how you code it.

11) wire ← elements are simple wires in verilog design. buses of (arbitary width)