...i rupa Bhattacharjee, ROLL NO. 6, DEPT: CSE (2nd Year)

ASSIGNMENT

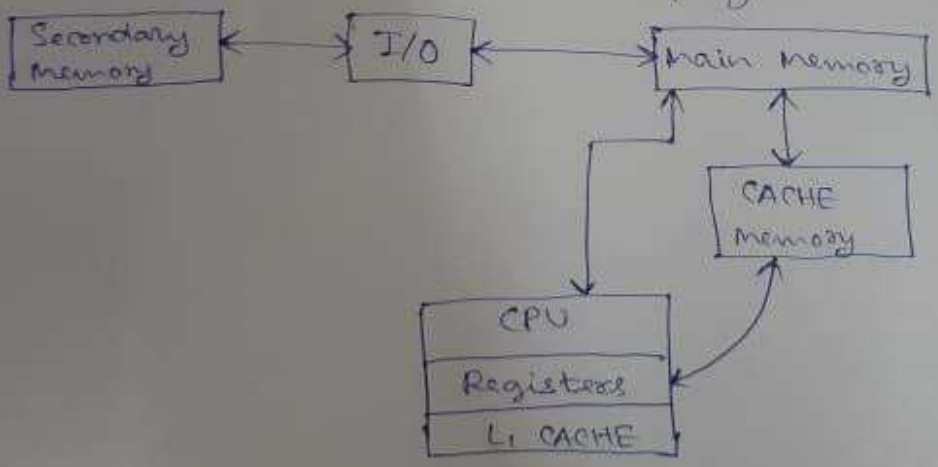
...2022

...scribe the shared memory model of SIMD architecture.

Ans: SIMD (Single Instruction Multiple Data Stream) machines but using shared memory are suited to applications that require frequent exchange of data where one processor acts as the consumer of this data. Each processor executes the same task in sync with the other processors.

2. What is locality of reference?

Ans: Locality of reference refers to a phenomenon in which a computer program tends to access same set of memory locations frequently for a particular time period. It refers to the tendency of accessing instructions whose addresses are near one another. It is mainly exhibited by loops and sub-routine calls in a program.



mainly used to encode and decode the ... representation of subnormal numbers.

3. What is a biased exponent?

Ans: In floating-point arithmetic, a biased exponent is the result of adding some constant (called bias) to the exponent chosen to make the range of the exponent non-negative. They are particularly useful when encoding and decoding the floating-point representation of subnormal numbers.

Assignment

Shilpa Paul
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What is Vector processor and write in application? Explain different types of Vector processor instruction. classify the Vector processor architecture and give brief explanation. What are the different method of Vector processor.

Ans: A Vector processor is a processing unit (CPU) that implements an instruction set where its instruction are designed to operate efficiently and effectively on large one-dimensional array of data called Vectors. So, it is also known as array processor.

Application:

(i) Data analysis
(ii) Weather forcasting
(iii) Aerodynamics
(iv) Medical Dignosis
(v) Space flight simulation

Types of Vector instruction:

- Vector-Vector instruction: One or two Vector operands are fetched from same Vector processor. These instructions are defined by mapping -

$$f_1 : V_i \rightarrow V_j$$
$$f_2 : V_j \times V_k \rightarrow V_i$$

- Vector-Scalar instruction: Vector scalar instruction corresponding to mapping.

$$f_3 : S \times V_i \rightarrow V_j$$

obtained by eqn 2N (2×16 = 32)

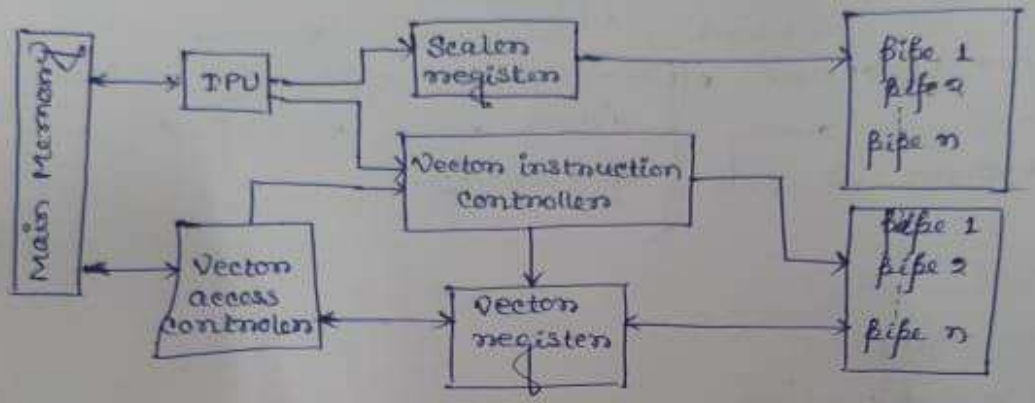
Roll- 21 , year - 3rd

- Vector - memory instruction : This lead to Vector load on Vector store step by step memory (M) register on Vector (V) register.

$f_4 : M \rightarrow V$ Vector load

$f_5 : V \rightarrow M$ Vector store.

Vector processor Architecture :



Functional units of a Vector computer are as follows —

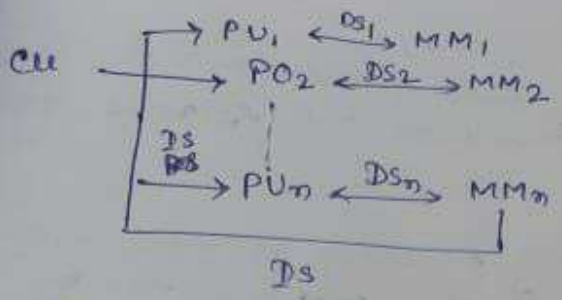
- IPU
- Vector register
- Scalar register
- Scalar processor
- Vector processor
- Vector access controller

So, as it's followed by its classification —

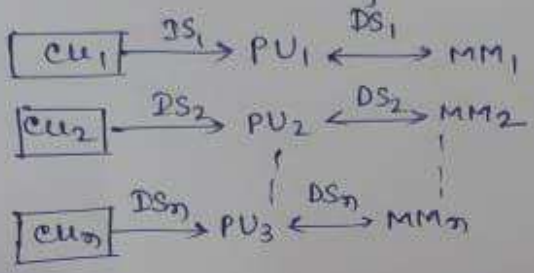
- Register to Register Architecture
- Memory to memory architecture.

- Single Instruction Multiple Data Stream (SIMD)

In SIMD architecture, multiple data streams . one instruction acts on the further instructed multiple Data Streams.



Multiple Instruction Multiple Data stream (MIMD)



In MIMD architecture multiple instruction act on different data streams.

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Sub - Computer Architecture Sem - 4th
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All about Data-hazard :

Introduction : To start the above discussion about "Data-hazard" at first need to learn what is hazard?
A hazard is any source of potential damage, harm or adverse health effects on something. But in the computer architecture, hazards are problems with the instruction pipeline in CPU when the next instruction cannot execute in the following clock cycle and can potentially lead to in correct computation result.

Defination : Data hazard occur when instruction that exhibit data dependence modify data in different stages of a pipeline. Ignoring potential data-hazard can result in conditions (also termed as hare hazards)

Types of that : There are 3 situation in which a data-hazard can occur →
(1) RAW (read-after Write) [a true-dependency]
(2) WAR (Write-after-read) [an anti dependency]
(3) WAW (Write-after-Write) [an output dependency]
(4) RAR (read-after-read) [It's not an hazard case]

Explanations : Now, we can discuss about various types of hazards.

(i) **RAW :** A read after Write data-hazards (RAW) refers to a result that has not yet been calculated or retrieved. This can occur because even though an instruction is executed after a prior instruction, the prior instruction has been processed only partly through the pipeline.

of eqn 2N
(2×16 = 32)

Adrita Bhattacharjee
CSE 05

1) Consider a 64 PE in ILLIAC determine the minimum number of data routing states needed to perform the following inter PE data transfer.

PE$_i$ to PE$_{(i+k) \bmod 64}$ where $0 \le i \le 63$, $0 \le k \le 63$

2) Explain the recirculating networks associated with SIMD computers

Answer

1) Routing information for ILLIAC-1 involves 4 eqns.

$R_{+1}(i) = (i+1) \bmod N$
$R_{-1}(i) = (i-1) \bmod N$
$R_{+r}(i) = (i+r) \bmod N$
$R_{-r}(i) = (i-r) \bmod N$

Since there are 64 processing elements.
we will get 64×4 data routing states
$\therefore$ 256 data routing states are obtained

In 16 bit,
through the routing eqn 64 states are recieved which the max^m no of data routing states.
Min^m number is 32.

$\therefore N = 16$
$r = 4$
64 => 4N data
$\therefore$ Min^m no of routing states is obtained by eqn 2N (2x16 = 32)

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$\therefore N = 23$

$\therefore$ For 64 processing elts $[N = 64]$

min^{m} no of data routing states is $2N = 2 \times 64 = 128$.

2) Hardware implementation of ILLIAC-IV, Cube network and Barrel shifter are analysed.

Recirculating (single stage) network multistage networks of combinational logics and pipelined multistage networks is analysed. An expanded control structure for recirculating structure is introduced. It allows each processor to select its interconnection function independently of the other processors. A multistage shuffle exchange network is presented. This network allows at each stage a ~~straight~~ shuffle followed by an exchange. Finally these networks are examined for this behaviour in partitionable SIMD machines.

Barrel shift network are also known as $\pm 2^i$ network (PM2I)

For eg: If n of PEs is $N = 64$ then $n = 4$ & $r = 4$

The ILLIAC-IV network has 32 direct links & the barrel shift has 58 direct links

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Computer Architecture Exam

Q. Explain the following terminologies in association with SIMD computers.
a) Routing functions for ILIAC network.
b) Cube routing function.
c) Barrell shifting function.
d) Shuffle - exchange function. (4×2)

Q. Calculate the min. number of routing steps from any PE_i to any other PE_{i+k} for the arbitrary distance $1 \leq k \leq 255$. Indicate the upper bound on min. routing steps required in barrell shift network. (2)

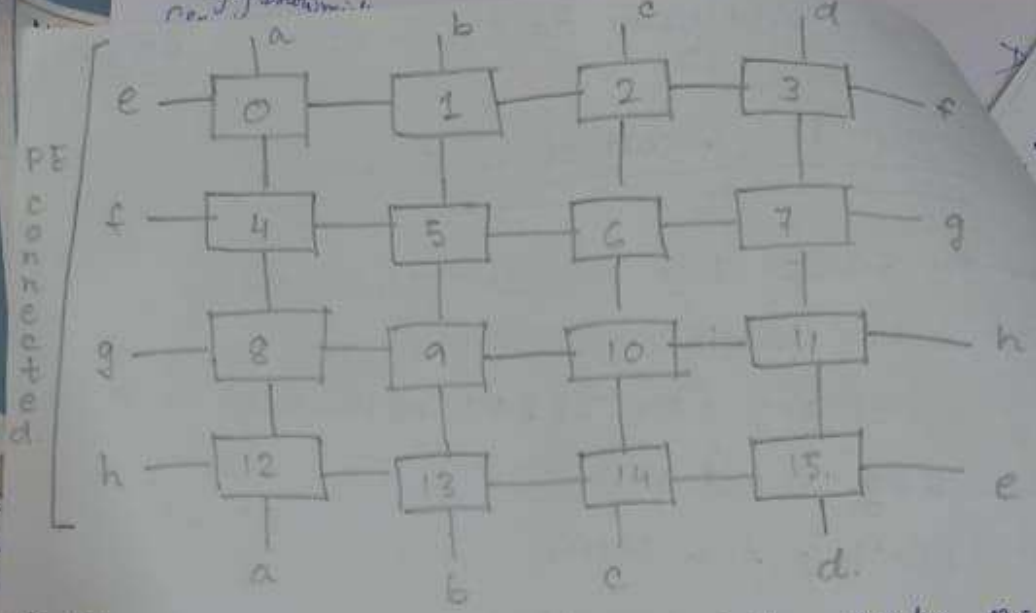
Q. Draw the multi-stage omega network where N = 16. (5).

— X —

1) a). The routing functions used in the ILIAC network are,

$R_{+1}(i) = (i+1) \text{ MOD } N.$
$R_{-1}(i) = (i-1) \text{ MOD } N.$
$R_{+r}(i) = (i+r) \text{ MOD } N.$
$R_{-r}(i) = (i-r) \text{ MOD } N.$

where $r = \sqrt{N}$.
and N = number of PEs =
$0 \leq i \leq N-1$.

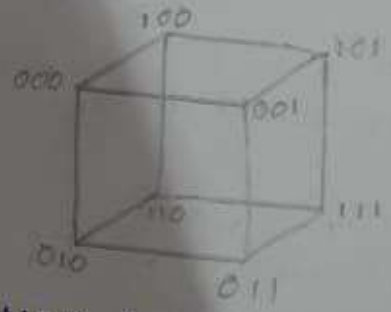


b) The routing function used in cube network is, $C_i = (a_{n-1} \cdots \bar{a}_i \, a_{i-1} \cdots a_1 a_0)$ $n = \log_2 N$.

The Output stage denoted by $OS(t_{n-1} \cdots t_i t_{i-1} \cdots t_1 t_0)$ $0 \le i \le n-1$.

The Input stage denoted by $IS(t_{n-1} \cdots \bar{t}_i t_{i-1} \cdots t_1 t_0)$ $0 \le i \le n-1$

For $N=8$, $n = \log_2 8 = 3$. So we consider only 3-bit numbers.



) The routing functions used in Barrel shift is

$B_{+i}(j) = (j + 2^i) \text{ MOD } N$. $0 \le i \le n-1$. $n = \log_2 N$.

$B_{-i}(j) = (j - 2^i) \text{ MOD } N$ $0 \le j \le N-1$.

$PE_A = a_{n-1} \cdots a_i \cdots a_1 a_0$

Shuffle function,

$\sigma(PE_A) = a_{n-2} \cdots a_i \cdots a_1 a_0 a_{n-1}$

The exchange function,

$E(PE_A) = a_{n-1} \cdots a_i \cdots \bar{a}_0$

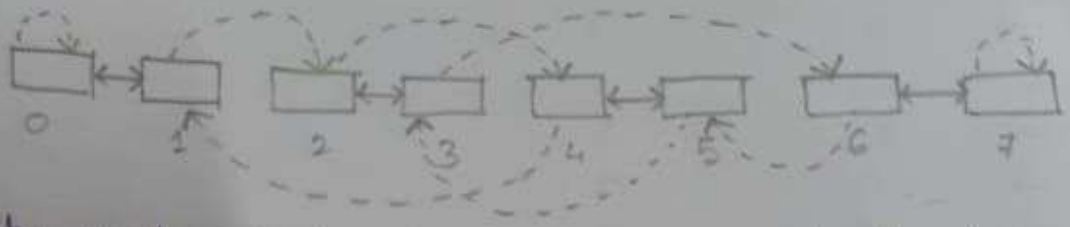
$n = \log_2 N$.

N → number of PEs

We see that $E(PE_A) = C_0(PE_A)$

↓

Cube routing function for $i = 0$.



The exchange functions are denoted by (↔).
and shuffle functions are denoted by (⋯≻).

Shuffle	Exchange
0 → 0	0 → 1
1 → 2.	1 → 0.
2 → 4	2 → 3
3 → 6	3 → 2
4 → 1	4 → 5
5 → 3	5 → 4
6 → 5	6 → 7
7 → 7.	7 → 6.

The minimum number of routing steps is upper bounded by $B \leq \frac{\log_2 N}{2}$.

? minimum number of routing steps from any PE$_i$ to any other PE$_{i+K}$ where $1 \leq K \leq 255$ is

$\frac{\log_2 256}{2} = \frac{8}{2} = 4.$

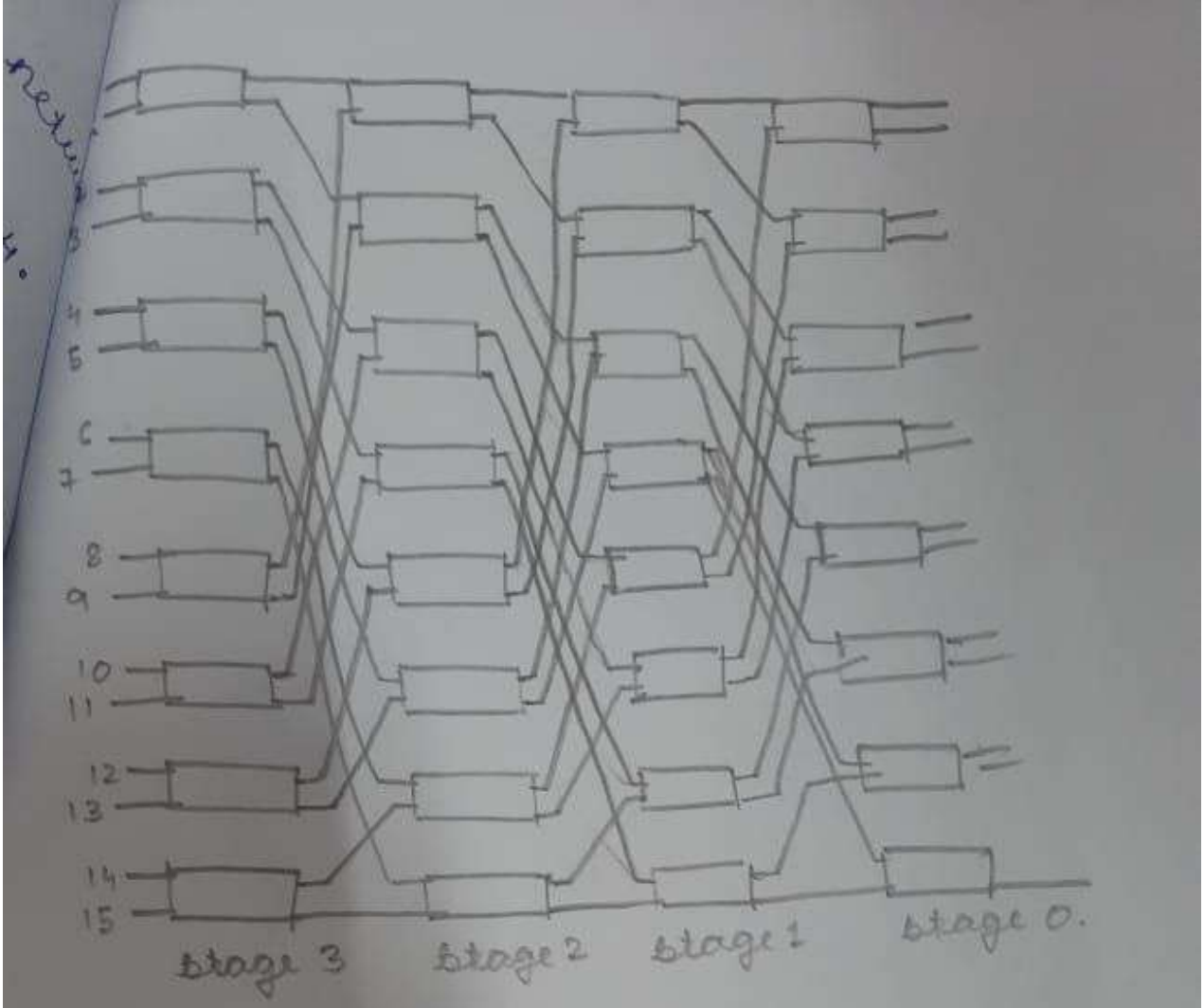
3) For N = 16, the multi-stage omega network is:

$n = \log_2 N = 4.$

$S = a_{n-2} \ldots a_i \ldots a_1 a_0 a_{n-1}$.

$E = a_{n-1} \ldots a_i \ldots \bar{a}_0$

	Shuffle	Exchange
0 →	0	1
1 →	2	0
2 →	4	3
3 →	6	2
4 →	8	5
5 →	10	4
6 →	12	7
7 →	14	6
8 →	1	9
9 →	3	8
10 →	5	11
11 →	7	10
12 →	9	13
13 →	11	12
14 →	13	15
15 →	15	14.


6
7
8
9
10
11
12
13
14
15
stage 3
stage 2
stage 1
stage 0.

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CSE 2nd year Roll 8
Computer Architecture

Date 2nd May 2022

Assignment

Q1) a) How do you calculate optimal performance/cost ratio for a pipelined architecture?

b) How to attain the maximum throughput of a pipelined architecture?

2) Describe the shared memory model of a SIMD architecture.

Ans

1a) The cost of a pipeline can be estimated by $c + \frac{h}{k}$ where c is the cost of the logic stages, h is the cost of the latches in a single stage, and k is the number of stages.

b) Maximum throughput can be obtained:
- → Decreasing clock cycles per instruction by introducing new Hardware.
- → Increasing clock rate by reducing propagation delays
- → Introducing faster circuits

2) SIMD represents Single instruction multiple data streams. The SIMD model of parallel computing includes two parts such as a front-end computer of the usual von Neumann style, and processor array. The processor array is a collection of identical synchronized processing elements adequate for simultaneously implementing the same operation on various data. Each processor in the array has a small amount of local memory where the distributed data resides while it is being processed in parallel.

The processor array is linked to the memory bus of the front end so that the front end can randomly create the local processor memories as if it were another memory.

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ASSIGNMENT

1. What is data flow computer? Differentiate between data flow computer and control flow computer?.

Ans: In computing, dataflow is a broad concept, which has various meanings depending on the application and context. Dataflow architectures have no program counter, in concept. The executability and execution of instructions is solely determined based on the availability of input arguments to the instructions, so that the order of execution is unpredictable i.e. behaviour is non-deterministic.

The key differences between data flow computer and control flow computer are as follows :-

Data Flow Computer	Control Flow Computer
(i) Unlike control flow, multiple components can process data at the same time.	(i) Precedence constraints control the project flow based on task completion, success or failure.
(ii) Smallest unit of the data flow is a component.	(ii) Smallest unit of the control flow is a task.
(iii) Data is moved and manipulated through transformations.	(iii) Control flow does not move data from task to task.
(iv) Data is passed between each component in data flow.	(iv) Tasks are run in in series if connected with precedence or in parallel.

2. Explain the differences between BFS and DFS.

Ans: BFS

(i) It stands for breadth first

2. What are the problems with data flow computers in implementation?

Ans: The problems with data flow computers are as follows :-

(i) Batch Sequential: It has high latency because each batch must be completed to reach to the second batch. It does not avail of the flexibility of interaction between batches.

(ii) Pipes and Filters: It does not support dynamic interaction and there is always the possibility of data transformation overhead between the filters.

(iii) Process Control Architecture: Specifying the time characteristic is a difficult part of this type of architecture. Disturbed responses could not be handled.