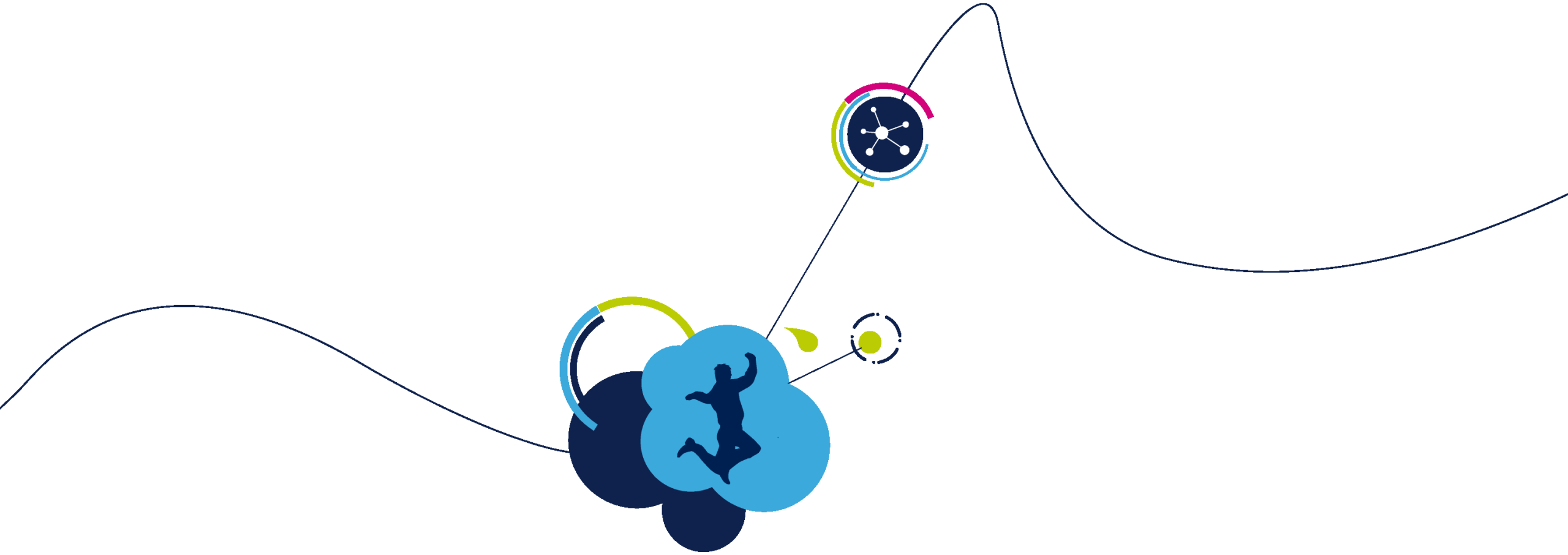

USB over STM32 family

Updated on 22/11/2017

USB over STM32 family

- USB full-speed device available on all STM32 families (not all devices)
  - Low-speed available only for host interface (on some families)
- **Crystal-less** implementation on some devices
  - Internal oscillator HSI48 calibrated to match USB FS specification (±0.25%)
  - Calibration sources:
    - SOF from USB host
    - 32.768 kHz LSE crystal
    - External signal
  - Can’t be used for USB host or HS device (this requires ±0.05%)
- Internal pull-up on D+ line (except for F1/F3/L1 devices)
  - Software disconnect by disabling the pull-up
  - STM32F105/7 – internal pull-up, but VBUS pin must be connected
- High-speed support on high-performance family (F2/F4/F7/H7)
  - Requires external PHY connected via ULPI interface
  - **STM32F7x3 has embedded HS PHY**

STM32 USB comparaison

	Device family	Core	Host/OTG	HS interface	Crystal-less
General purpose	STM32F0x0 (Value line)	Cortex-M0	No	No	No
	STM32F0x2/0x8	Cortex-M0	No	No	Yes
	STM32F102/103	Cortex-M3	No	No	No
	STM32F105/107	Cortex-M3	Yes	No	No
	STM32F3	Cortex-M4	No	No	No
High performance	STM32F2	Cortex-M3	Yes (2x)	ULPI (1x)	No
	STM32F4/F7	Cortex-M4	Yes (2x)	ULPI (1x)	No
	STM32F7x3	Cortex-M7	Yes (2x)	**On-chip PHY**	No
	STM32H7	Cortex-M7	Yes (2x)	ULPI (1x)	Yes
Low power	STM32L0	Cortex-M0+	No	No	Yes
	STM32L1	Cortex-M3	No	No	No
	STM32L4x2/4x3	Cortex-M4	No	No	Yes
	STM32L4x5/4x6	Cortex-M4	Yes	No	From LSE
	STM32L4+	Cortex-M4	Yes	No	Yes

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USB device-only peripheral

- STM32F0/F102/F103/F3 and STM32L0/L1/L4x2/L4x3 devices
- Maximum 8 bidirectional endpoints
  - Including endpoint 0
  - Bidirectional endpoints must have same type
    - e.g. 0x81 (IN) and 0x01 (OUT) are both BULK
- Supports only full-speed
- Dedicated SRAM buffer for transfers
  - Shared with CAN on some devices
  - On F102/F103 device not possible to use with CAN
  - Configurable size per endpoint
  - 16-bit access
- Link power management (LPM) and Battery charging detection (BCD) support on some devices

USB device-only peripheral

Device	Buffer (bytes)	Buffer (with CAN enabled)	LPM	BCD
STM32F0	1024	768	Yes	Yes
STM32F103/105	512	0 (forbidden)	No	No
STM32F303xB/C STM32F358xC STM32F302xB/C	512	512	No	No
STM32F303xD/E STM32F302x6/8	1024	768	Yes	No
STM32L0	1024	1024 (no CAN)	Yes	Yes
STM32L1	512	512 (no CAN)	No	No
STM32L4x2/4x3	1024	1024 (no CAN)	Yes	Yes

USB OTG peripheral

- High-speed supported on some devices (USB_OTG_HS)
  - USB_OTG_HS can still operate in full-speed using internal PHY
  - Dedicated DMA controller for USB_OTG_HS
    - Requires all transmit/receive buffers to be 32-bit aligned
- Supports Device-only, Host-only and OTG mode
- Internal pull-downs for the USB FS host
- Dedicated FIFO
  - Configurable size per endpoint
  - 32-bit access

USB OTG peripheral

Device	USB_OTG_FS			USB_OTG_HS		
	Endpoints *	Pipes (Host)	FIFO size	Endpoints *	Pipes (Host)	FIFO size
STM32F1 STM32F401 STM32F411	4 IN + 4 OUT	8	1.25 K	-		-
STM32F2 STM32F4 (other)	4 IN + 4 OUT	8	1.25 K	6 IN + 6 OUT	12	4 K
STM32F412 STM32F413	6 IN + 6 OUT	12	1.25 K	-		-
STM32F446/469/479 STM32F7	6 IN + 6 OUT	12	1.25 K	8 IN + 8 OUT	18	4 K
STM32H7	**	**	**	8 IN + 8 OUT	18	4 K

* Including endpoint 0

** H7 has two OTG_HS named peripherals with same properties (including DMA), but only one has high-speed capability