ор	R1 = R2 op R3										
ор	R4 = R1 op R2										
		IF	ID	Reg	Ex	Mem	WB				Muxes F1
			IF	ID	Reg	Ex	Mem	WB			
ор	R1 = R2 op R3										
op with CCR depend											
		IF	ID	Reg	Ex	Mem	WB				forward x
			IF	ID	Reg	Ex	Mem	WB			
ор	R1 = R2 op R3										
Х											
op with CCR depend	ence										
		IF	ID	Reg	Ex	Mem	WB				forward y
			X	X	Х	х	Х	Х			
				IF	ID	Reg	Ex	Mem	WB		
ор	R1 = R2 op R3										
X	X										
ор	R4 = R1 op R2										
		IF	ID	Reg	Ex	Mem	WB				Muxes F1
				IF	ID	Reg	Ex	Mem	WB		
R7 =R1 (uncondition	al operation) R2	IF	ID	Reg	Ex	Mem	WB				
			Х	X	х	Х	Х	Х			
				X	х	x	Х	Х	Х		
					х	x	Х	Х	Х	x	
						IF	ID	Reg	Ex	Mem	WB
R3 = R1 op R2		IF	ID	Reg	Ex	Mem	WB				
R7 = R1 op(condition	al) R2		IF	ID	Reg	Ex	Mem	WB			
(next)				Х	Х	Х	X	X	Х		
					X	Х	Х	X	X	X	
				Case 1:		IF	ID	Reg	Ex	Mem	WB

			1
or F2 use a			
or FZ use a			
into ccr			
[			
into ccr			
[			
or F2 use b	Unless X = another o	op conflict, in which case use a.	
	(closest conflict)		
	(Closest conflict)		
	Forward a to PC		
( if the fire	st instruction did not set CCR)		
	• •		

				Case 2:		Х	X	X	X	X	х
							IF	ID	Reg	Ex	Mem
ор	R1 = R2 op R3										
load	R4 = mem(R1 +lm6	5)									
		İF	ID	Reg	Ex	Mem	WB				Muxes F1
			IF	ID	Reg	Ex	Mem	WB			
ор	R1 = R2 op R3										
X	X										
load	R4 = mem(R1 +lm6	5)									
	*	İF	ID	Reg	Ex	Mem	WB				Muxes F1
				IF	ID	Reg	Ex	Mem	WB		
load	R4 = mem(R1 +lm6	5)									
ор	R2 = R4 op R3										
		IF	ID	Reg	Ex	Mem	WB				Muxes F1
	stall		Х	Х	Х	Х	Х				
				IF	ID	Reg	Ex	Mem	WB		
load	R4 = mem(R1 +lm6	:1									
load	R3 = mem(R4 +Im6										
iuau	N3 - IIIBIII(N4 +IIII0	')	IF	ID	Reg	Ex	Mem	WB			Mux F1 ι
		stall	IT'	χ	x	X	x	X			IVIUX F1 (
		Stail		^	IF	ID	Reg	Ex	Mem	WB	
					11	טו	iteg	LA	IVICIII	VVD	
	D4 D2 D2										
op	R1 = R2  op  R3										
store	mem(R4+Im6) = R1						11/5				
		IF	ID	Reg	Ex	Mem	WB				
			IF	ID	Reg	Ex	Mem	WB			Mux F1 u

₩B	(if the first instructi	on did set CCR	(forward	from a)			
F2							
F2 use a							
r F2 use b							
or F2 use c							
		load	load				
		x an	d x load	use just forw	ard, stail is imple	mented by the int	ermediate instri
es c							


ор	R1 = R2 op R3								
store	mem(R1+lm6) = R2								
	IF	ID	Reg	Ex	Mem	WB			
		IF	ID	Reg	Ex	Mem	WB		Mux F1 us
ор	R1 = R2 op R3								
store	mem(R1+Im6) = R1								
	lF	ID	Reg	Ex	Mem	WB			
		IF	ID	Reg	Ex	Mem	WB		Mux F1 uso
									Mux F3 uso
ор	R1 = R2 op R3								
X	x								
store	mem(R1+Im6) = R2								
	IF.	ID	Reg	Ex	Mem	WB			
		X	X	X	Х	X	X		
			IF	ID	Reg	Ex	Mem	WB	Mux F1 us
ор	R1 = R2 op R3								
X	x								
store	mem(R1+Im6) = R1								
	IF.	ID	Reg	Ex	Mem	WB			
		Х	X	X	X	Х	Х		
			IF	ID	Reg	Ex	Mem	WB	
load	R2 = mem(R1+Im6)								
store	mem(R3+Im6) = R2								
	IF.	ID	Reg	Ex	Mem	WB			
		IF	ID	Reg	Ex	Mem	WB		Mux F3 us

ses a					
es a					
es c					
ses b					
Mux F1 uses b					
IVIUX I I USES D					
es c					
		<b></b>	<u> </u>		

	-			
	-			

load	R2 = mem(R1+Im6	)								
store	mem(R2+Im6) = R3									
		IF	ID	Reg	Ex	Mem	WB			
	stall		Х	X	Х	x	Х	X		
				IF	ID	Reg	Ex	Mem	WB	Mux F1 us
load	R2 = mem(R1+Im6	)								
store	mem(R2+Im6) = R2	2								
		IF	ID	Reg	Ex	Mem	WB			
	stall		Х	Х	Х	x	Х	X		
				IF	ID	Reg	Ex	Mem	WB	Mux F1 us
After JAL and J	LR stalls are always require	d.follow	ed by a fo	orward						
JAL	R2 = PC+1	IF	ID	Reg	Ex	Mem	WB			
х	x		Х	Х	Х	X	Х	X		
				IF	ID	Reg	Ex	Mem	WB	Mux F4 us
	R2 = PC+1	IF	ID	D	E.	N/	WB			
JAL		IF	ID	Reg	Ex	Mem				Muxes F1
ор	R3 = R2 op R1		Х	X IF	x ID	x Reg	x Ex	x Mem	WB	Mux F4 us
JAL	R2 = PC+1	IF	ID	Reg	Ex	Mem	WB			
load	R3 = mem(R2 +lm6	5)	X	Χ	X	х	X	Χ		Muxes F1
				IF	ID	Reg	Ex	Mem	WB	Mux F4 us
	D2 DC:4	I.E.	ID	D	F	D.4	WD			
JAL	R2 = PC+1	IF	ID	Reg	Ex	Mem	WB			NA 54
store	mem(R2 +Im6) = F	3	X	X	Х	Х	X	X		Muxes F1

		 1		
es c				
es c				
es d				
or F2 use b				
es d				
or F2 use b				
es d				
	1	J		
	J	]		
or F2 use b				
5. 12 d3C b		1		

				IF	ID	Reg	Ex	Mem	WB	Mu	ıx F4 us
JAL	R2 = PC+1	IF	ID	Reg	Ex	Mem	WB				
store	mem(R2 +lm6) =	R2	х	x	х	х	Х	Χ		Mι	ıxes F1
				IF	ID	Reg	Ex	Mem	WB	Mu	ıx F4 us
JAL		IF	ID	Reg	Ex	Mem	WB				
op R1 = R2+R7			Х	X	X	Х	X	X		use	e g to fo
				IF	ID	Reg	Ex	Mem	WB		- 6
											······
JLR		IF	ID	Reg	Ex	Mem	WB				
			Х	X	Х	Х	Х	Χ			
				Х	Х	х	Х	Х	Х		
					IF	ID	Reg	Ex	Mem	WB	
Note JLR has no erro	or, if followed by R7 o	peration									
Beq											
		IF	ID	Reg	Ex	Mem	WB				
			IF	ID	NOP	NOP	NOP	NOP			
				IF	NOP	NOP	NOP	NOP	NOP		
				Shown	what happ	ens if bran	ch is takeı	n, else brar	nch not take	en, normal with	no NOP
LDW R7		IF	ID	Reg	Ex	Mem	WB				

es d				
or F2 use b				
es d				
C3 u				
rward appropriat	o value of D7			
nwaru appropriati	2 value of R7			
Mux F4 uses e				
flush t	ne first two pipline registers.			
NOP =	ne first two pipline registers. no operation, when IR = 16'b11110000000	000000		
)				

	ļ		

or LDM 1xxxxxxx			х	Х	Х	Х	Х	Х			
				Χ	X	Х	Х	Χ	Х		
					X	Х	X	Х	Х	X	
						X	X	Χ	Х	X	x
							X	Х	Х	X	x
							IF	ID	Reg	Ex	Mem
LHI R7,Im6											
	only one stall										
	forward h to be lo	aded into	PC								
LLU DE Les C		IF	ID.	D	E.	NA o roo	W/D				F
LHI R5,Im6		IF	ID	Reg	Ex	Mem	WB	14/5			Forward i
R1 R2 op R5			IF	ID	Reg	Ex	Mem	WB			
LHI R5,Im6		IF	ID	Reg	Ex	Mem	WB				Forward j
x											آ ا
R1 R2 op R5				IF	ID	Reg	Ex	Mem	WB		

	Forward c to be loaded into PC!			
X				
WB				
o the inputs of ALU				
to the inputs of ALU				