ATLAS NOTE

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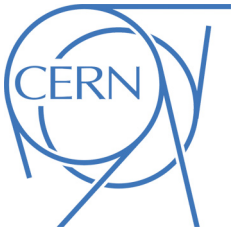

Bench test of VMM2 mini-1 boards

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Abstract

We have investigated the performance of the VMM2 ASIC. Results are presented, some already known and some not.

1 Introduction

We present results of a bench test of the VMM2 readout electronics performed at Harvard. Most of the results have been shared with some of our BNL colleagues who designed the ASIC. They helped us to start on the right foot, contributed to the understanding and resolution of a number of issues we found, and hence we all sign this note.

We begin with a description of the VMM2 architecture. Most details are known to most people working on the NSW upgrade; however, we want this note to be also a *vade mecum* for new students. We did not spend much time probing the VMM2 analog part because it is almost equal to that of the VMM1 which we investigated at length in Refs.[1]. Calibrations of charge and timing for two different VMM2 chips are described in Section 2.

Most of our studies were dedicated to the new VMM2 features, namely the on-board ADCs, the FIFO memories, and the token logic used to extract the stored informations. The new parts have some problems which are described in Secs. 3 to 5.

1.1 VMM2 architecture

The VMM2 is composed of 64 channels, each providing charge and timing information. The functionality of the VMM2 is detailed in Refs. [2] and [3]. Appendix A provides a few additional tips for beginners. A basic logic diagram is shown in Figure 1. For each channel, the chip contains an analog section with

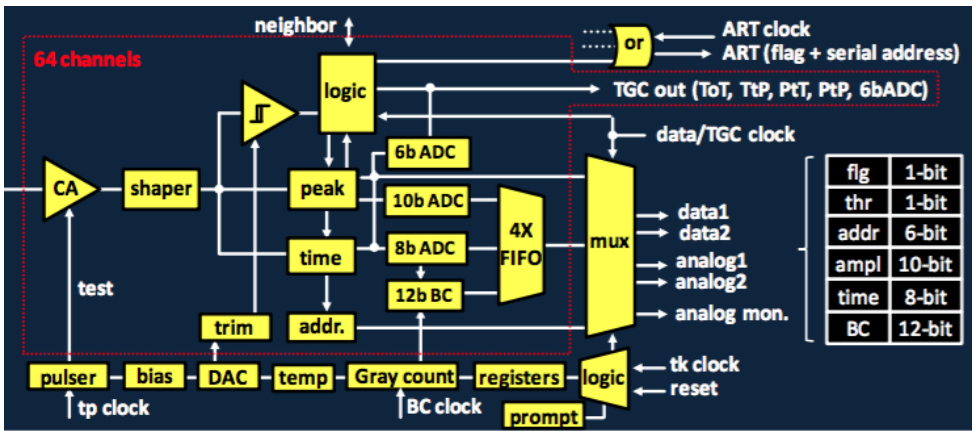


Figure 1: Architecture of the VMM2 ASIC.

a selectable-gain charge preamplifier and a high-order DDF (delayed dissipative feedback) shaper with a peaktime selectable from 25 to 200 ns [1]. The shaping amplifier is followed by a discriminator with a threshold value common to all channels with the additional option of fine trimming the threshold of each channel. The voltage output of the shaping amplifier, referred to as the PDO, goes to a peak detector (armed by the discriminator).

The detection of a peak starts the TAC ramp for this channel. In continuous mode, TAC ramps are stopped by the falling edge of the next pulse of the bunch cross clock, referred to as CKBC [2]. The number of CKBC cycles elapsed till the TAC stop are recorded in a 12-by Gray-code counter. The scale of the TAC ramp is selectable and in our test we use the 500 ns scale. The ASIC can operate in three modes: direct output, two-phase/analog, and continuous/digital. We operate the VMM2 in continuous mode, in which the PDO and TDO signal are digitized by the on-board 10-bit and 8-bit domino ADCs,

[1] The analog output of the shaping amplifiers can be monitored one channel at the time.
[2] TAC ramps are stopped by the falling edge of ENA in two-phase mode.

respectively. At the end of the ADC conversion, the ADC counts are stored in a 4-level deep FIFO together with the channel address, Gray-code counter content and some ancillary information. A timing diagram detailing the storage of a channel information is shown in Fig. 2. The FIFO content is read out

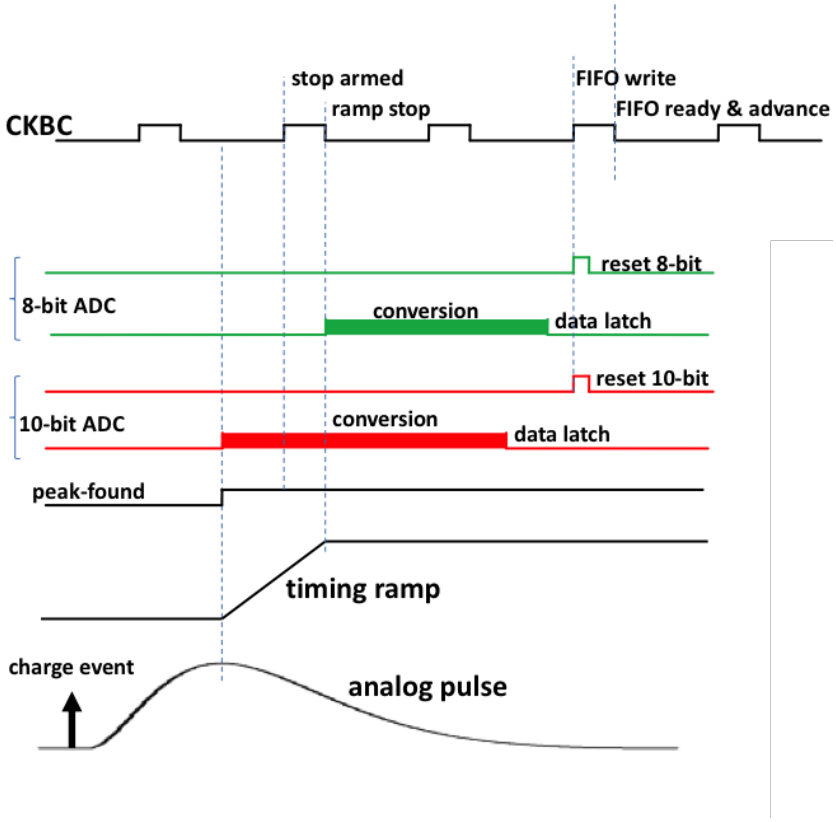


Figure 2: The channel recording scheme.

by the data acquisition system through a token-passing scheme, described Appendix C, which makes use of two clocks: CKTK, which advances the readout token to FIFO elements with data; and CKDT, which clocks out the FIFO content of channels with information.

For data acquisition, we first successfully used a GLIB [4] evaluation board instrumented with an Arizona SF-6 mezzanine card [5]. Later, to be in syntony with BNL colleagues, the test we will describe were performed using the BNL CDAQ board with a Labview GUI. This GUI has two primary pages: the VMM2 Readout page, shown in Fig. 3; and the SPI Write page, shown in Fig. 4. The VMM2 Readout Page provides real time histograms of the PDO, TDO, and hits per channel, and allows the configuration of test pulses. The SPI Write page is used to set the VMM2 configuration.

2 VMM2 Calibration

This section describes our procedure for calibrating the PDO and TDO ADC scale in fC and ns per count, respectively. We tested two VMM2 chips, mounted on mini-1 front-end boards, referred to as VMM2A and VMM2B in the following. For all measurements in this section, we use a TAC slope of 500 ns, gain of 9 mV/fC, peaking time of 200 ns, and coarse threshold DAC of 250.

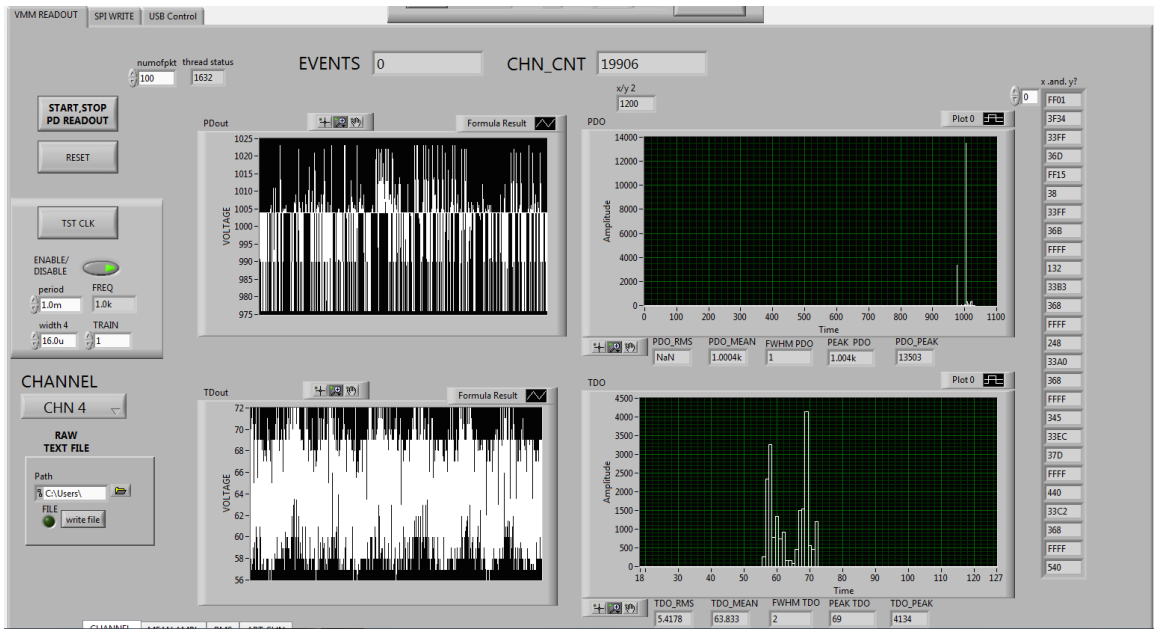


Figure 3: The VMM2 Readout GUI page.

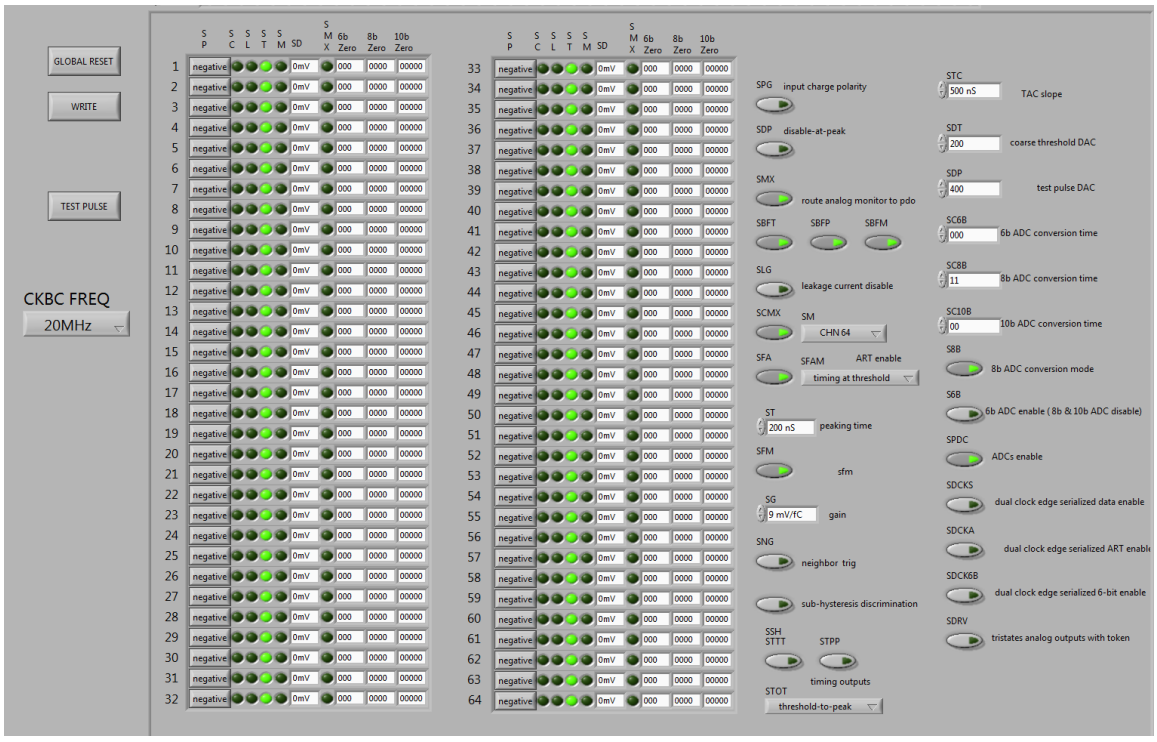


Figure 4: The SPI Write GUI settings used in our tests. Note the S8B=1 setting which makes the 8-bit ADC conversion time shorter than that of the 10-it ADC (see the diagram in Fig. 2).

2.1 Channel Pedestals and Thresholds

The pedestals and thresholds of each individual channel have been measured with an oscilloscope using the monitor channel and the appropriate SPI settings shown in Fig. 4. The DAC step pulse is viewed

on Channel 2, with SCMX and SBFM set low. The measurement of pedestals and thresholds requires SCMX high and SBFM high and low, respectively. The individual channel SMX set low and high for reading pedestals and thresholds, respectively. The pedestals and thresholds are shown in Figs. 5 and 6 for VMM2A, and in Figs. 7 and 8 for VMM2B.

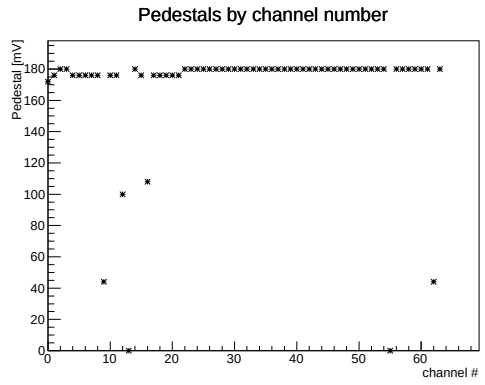


Figure 5: VMM2A pedestals by channel.

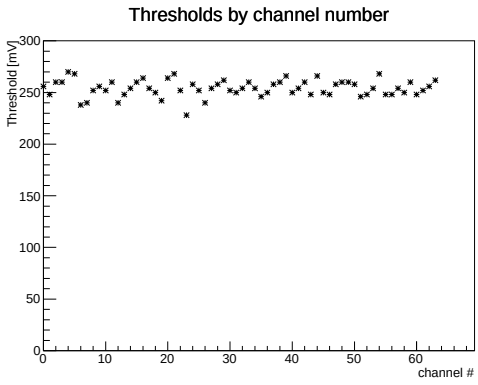


Figure 6: VMM2A thresholds by channel.

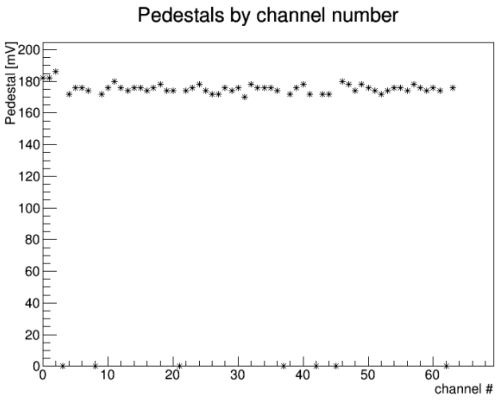


Figure 7: VMM2B pedestals by channel.

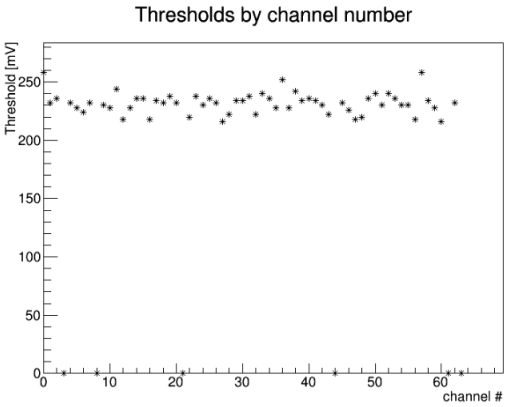


Figure 8: VMM2B thresholds by channel.

The scatter of channel-to-channel values is similar to that of the VMM1 as well as that of the differences between pedestals and thresholds. The range of the threshold fine adjustment is the same as in the VMM1, making it is plausible that the minimal thresholds for MIP will still vary between 2 and 6 fC as it was the case for VMM1 [1].

2.2 DAC Calibration

The charge measurement is calibrated by sending step pulses, the value of which is determined by a DAC, to the charge amplifier via a 1.2 pF capacitor. The VMM1 DAC response is nonlinear. To check the linearity of the DAC output voltage height vs input count, we select several values of the input DAC ranging from 80 to 200 and measure the height in mV of the resulting pulse with an oscilloscope. We then fit a straight line to the resulting graph, and use the fit parameters to convert DAC counts into injected-charge values. These fits are shown in Fig. 9. We note the the DAC response is more linear then in the VMM1; however, the 2 chips respond differently. Because the DAC outputs differ from chip to chip, PDO calibrations in the experiment will be possible only if the DAC output of each chip can

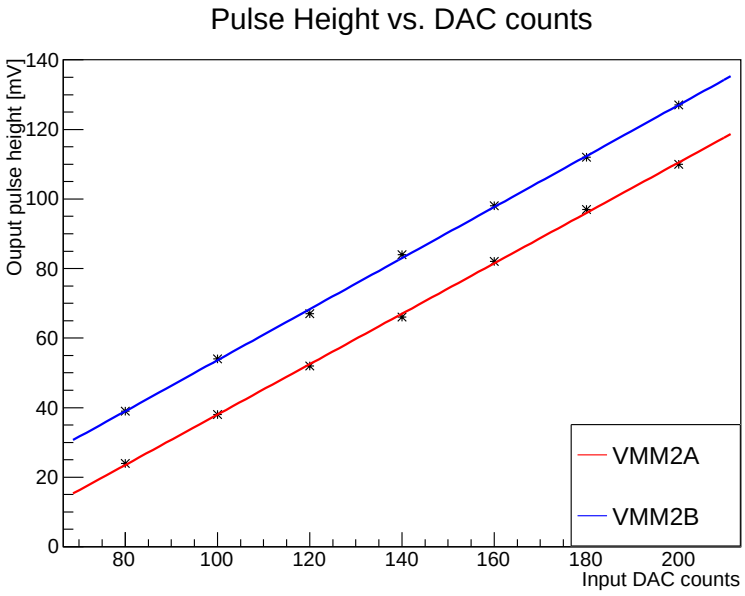


Figure 9: DAC output vs. input.

be re-routed to an external calibrated ADC. In the following sections, we show the results of the 10-bit (PDO) and 8-bit (TDO) calibration for the VMM2A chip.

2.3 PDO Calibration

We send test pulses to all 64 channels using 5 different DAC values (80, 100, 120, 140, and 150). The calibrated DAC output is converted into an injected charge which is then compared to the ADC counts. An example is shown in Fig. 10. Each histogram is fitted with a straight line. The pedestals and slopes

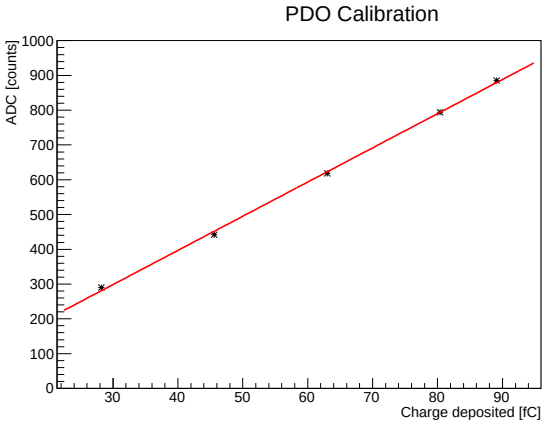
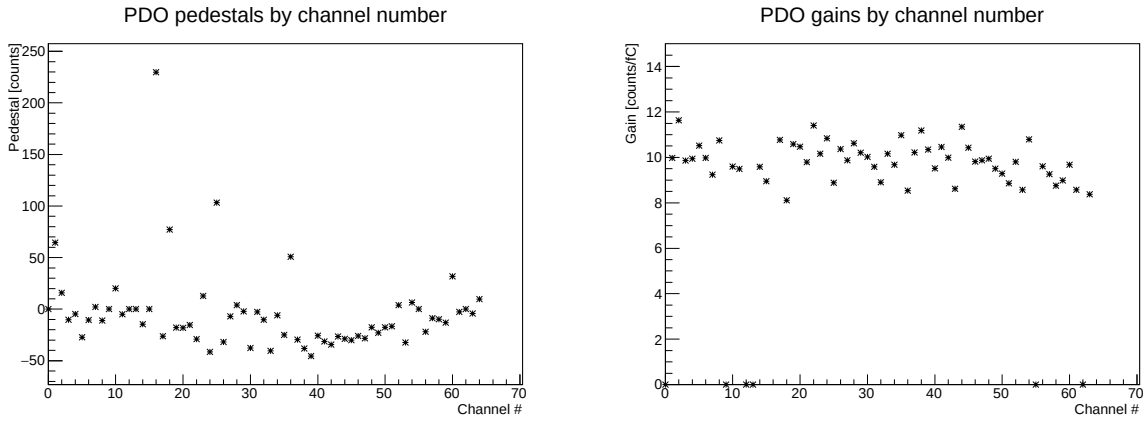


Figure 10: An example of the PDO calibration, for one channel.

of the fits for all working channels are shown in Fig. 11.



(a) (b)

Figure 11: PDO ADC pedestals (a) and slope/gain (b) by channel.

2.4 TDO Calibration

The determination of the arrival time of a micromega pulse is crucial for the μTPC method, and requires an accurate calibration of the 8-bit ADC scale. As far as we know, no attempt has yet been made to calibrate the TAC ramp and the 8-bit ADC. The reason is that, using the VMM in continuous mode, it is hard to delay a test pulse with respect the CKBC clock.

In this first attempt, we use the feature that the TAC ramp is armed at peak found and stopped at the falling edge of the next CKBC pulse. By reducing the CKBC frequency from 20 mHz to 10 and then 5 mHz, we delay the TAC stop by 25 and 75 ns. At the same time, when scaling down the CKBC frequency, one increases the total width of the TDO distribution from 50 to 100, and 200 ns.

We calibrate the 500 ns TAC scale by fitting with a straight line the ADC counts corresponding to the beginning and the end of the time distribution for the 3 different frequencies with respect to the beginning of the 20 mHz distribution set arbitrarily at 25 ns. An example of ADC calibration for 1 channel is shown in Fig. 12. Pedestals and slopes for all channels are shown in Fig.13. The 8-bit ADC is well behaved.

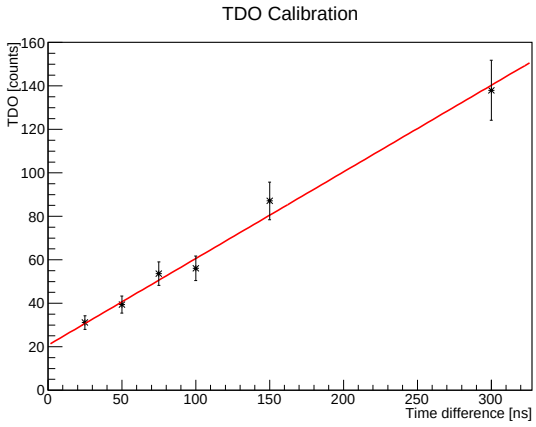
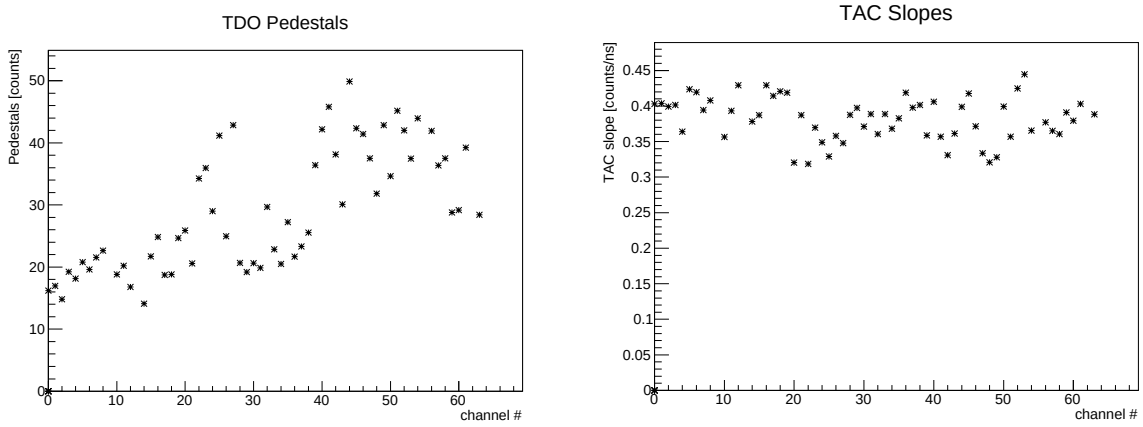


Figure 12: An example of TDO calibration, for one channel. Errors come from the uncertainty in estimating the beginning/end of each TDO distribution.

Since the experiment will use a TAC scale between 32 and 64 ns, a different calibration method is in order, and we are working on this.

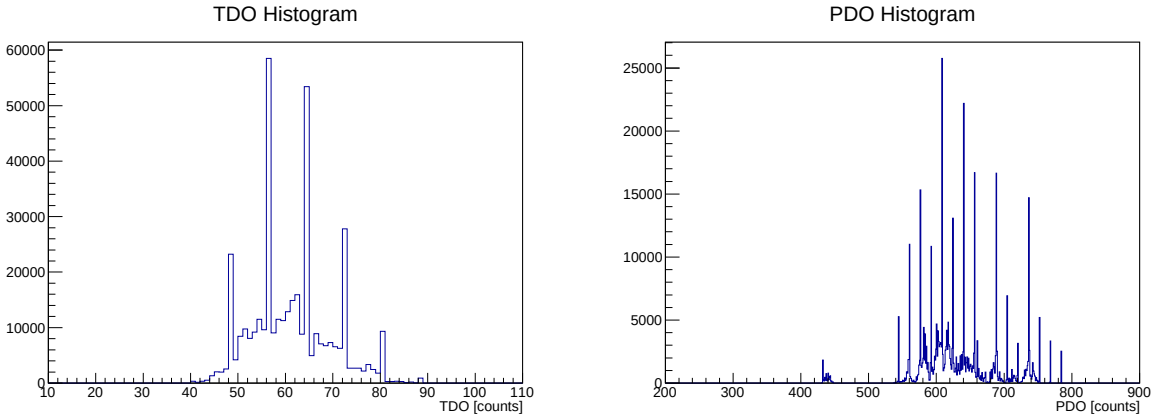


(a) (b)

Figure 13: TDO ADC pedestals (a) and slope (b) by channel.

3 Loss of the ADC LSB

It is a known fact that in some chips or channels the 10-bit and 8-bit ADC lose the least significant bits (4 and 3, respectively) [6]. This effect for VMM2B is illustrated by Fig. 14.



(a) (b)

Figure 14: Distributions of the 10-bit (a) and 8-bt (b) ADC counts when test-pulsing all 64 VMM2B channels. All channels are included in these distributions.

The ADC architecture is described in Appendix A. PDO (TDO) voltages are converted into currents, and compared to reference currents of 6 (5) cells which scan the maximum expected current in 6 (5) steps (MSB) for the 10(8)-bit ADC. Once the signal current is located into a cell, the lower reference current of this cell is subtracted, and the difference is compared to 4 mini-cells (LSB). each a quarter (third) of one main cell. As clearly explained in Ref. [2], at the moment of the subtraction, spikes in the voltage-to-current conversion of the PDO (TDO) force the domino ADC to subtract the reference current of an higher cell thus yielding LSB=0.

4 Corruption of the token-passing logic

It is well known that the VMM readout often outputs replicas of a channel information. However, this issue has not been thoroughly investigated. All VMM chips suffer of this problem which is not endemic, but develops when operating the chip for some time; this time varies from seconds to hours depending on the chip, the chip SPI configuration, or the frequency of the input signal. Figure 15 shows the number of accumulated hits per channel before and after this problem occurs. In this case, we are test pulsing all 64 channels with a 1 Hz frequency. One notes that some channels have extra hits (replicas) but some

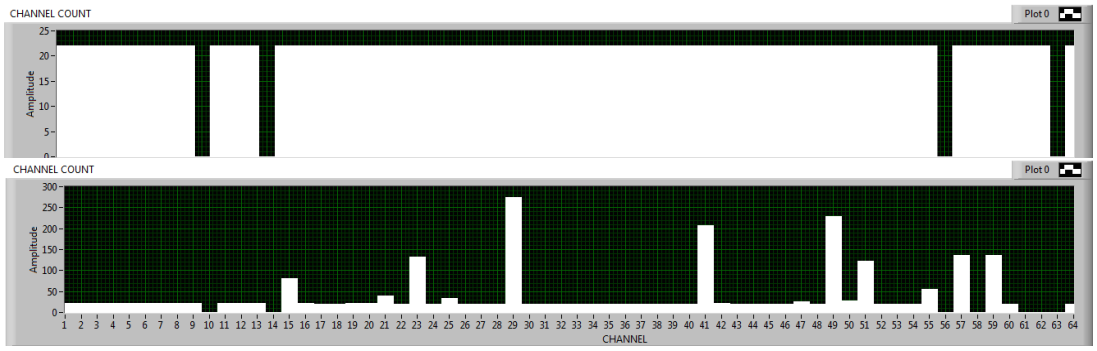


Figure 15: number of hits accumulated in each channel with (top) normal and (bottom) corrupted token logic.

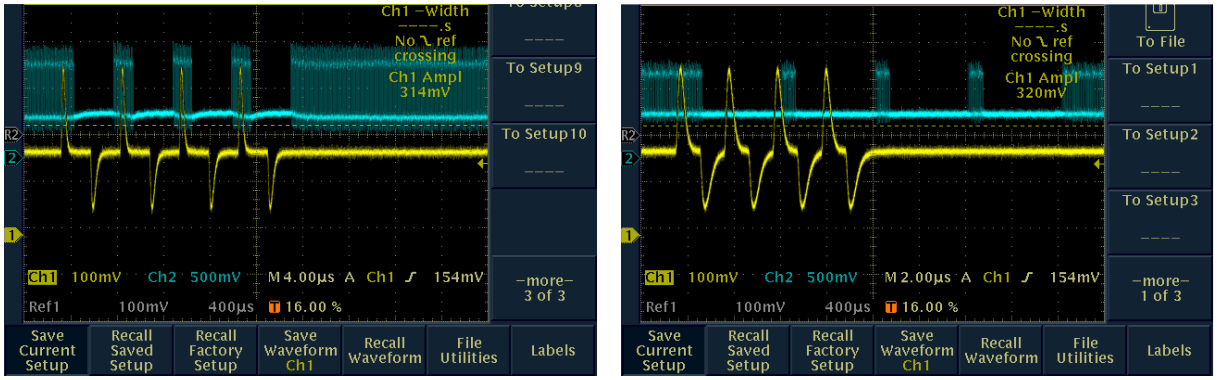
channel lose hits. This is better understood by inspecting the two files of data in Appendix B. The first file shows the 64 channel content when the VMM works properly. The second file is written when the VMM stops working properly. One sees replicas of the same channel which usually - but not always- occur when the token is passed to the previous instead of the next channel, as it should be. One also sees that bunches of channels are read again after many events. Some events consists of only a few channels because, even with a 1 Hz test-pulse frequency, the 4-level FIFO may become completely filled when not read, and information is lost.

This problem is caused by parasitic impedances that drag the phase of the token used to readout the FIFO content. Reference [3] does not describe the token-passing scheme which is detailed in Appendix C. In a few words, the token-passing logic is like a hamster, the token, wheel with 64 steps. The hamster goes around the wheel 10^7 times per second (advanced by the CKTK clock) asking the FIFO of each channel if there are data to read; if there are data, CKTK comes to a screeching halt, data are read out using the CKDT clock, the writing and output points of the FIFO are updated, CKDT ends, and CKTK starts moving the token again. Because of the parasitic impedances the token loses its synchronization with CKTK, and *stuff happens* as shown in Appendix B.

We did notice that re-downloading the SPI configuration re-establishes the token synchronization. Since the token-logic is also regenerated with the so called soft reset, we have modified the FPGA firmware so that, once a channel info is read out, if no data 0 flag appears after 40 CKBC cycles, a soft reset is issued. In other word, we issue a soft reset each time a complete event is read out. This adds the time to read out 1/2 channel to the readout latency. With this simple fix, the VMM chips work for weeks without losing synchronization. The firmware fix has been sent to all interested parties.

5 Update of the FIFO writing point

A problem was discovered when studying the VMM2 response to high rates by test pulsing all 64 channels with increasing frequencies. Actually, the gain sags for frequency higher than 100 kHz, but is not an immediate concern of ours because we will use MMFE-8 boards with cosmics to commission the trigger. During this test, we noticed that, if a second test pulse was coming before the 64 channels were all read out, the non-read channels were overwritten by the second event. We made the test even simpler by firing only one channel with a train of 4 pulses with decreasing spacing, as shown in Fig. 16. In the situation of Fig. 16 (b), the second pulse overwrites the first. As explained in Appendix C, the FIFO writing and output points are updated after after the FIFO is read out. They should be updated when the FIFO is written; this will be fixed in the VMM3 version.



(a) (b)

Figure 16: Scope display of the input test pulses and CKTK when the next test pulse arrives (a) after and (b) before the first pulse has been read out, as indicated by the start of CKTK.

6 Conclusion

We have tested a couple of VMM2 chips mounted on a mini-1 board. The analog part of the new ASIC has not changed much, and we see no improvement or degradation. We mostly studied the response of the new additions, i.e. the on-board ADCs, the 4-level FIFO, and the token-passing circuitry. We rediscovered known issues, such as the loss of the ADC less significant bits and the loss of synchronization of the token-passing logic. However, we found a firmware fix for the latter problem. We also found a bug in the method of updating the FIFO writing and output points.

References

[1] J. Connors *et al.,* ATL-COM-UPGRADE-2013-019, ATL-COM-UPGRADE-2013-023, ATL-COM-UPGRADE-2013-034, K. DiPetrillo *et al.,* ATL-COM-MUON-2014-038.

[2] G. De Geronimo *et al.,* `https://indico.cern.ch/event/287628/session/4/contribution/33/attachments/535406/738187/ACES_2014_VMM2_fin.pdf`.

[3] `https://twiki.cern.ch/twiki/pub/Atlas/NSWelectronics/VMM2_datasheet_v16.pdf`.

[4] `https://espace.cern.ch/project-GBLIB/public`.

[5] The SF6 mezzanine, its firmware as well as the GLIB firmware was kindly provided by K. Johns.

[6] G. De Geronimo, `https://indico.cern.ch/event/447077/VMM_Sept_2015.pptx`.

[7] ATLAS New Small Wheel Technical Design Report, ATLAS-TDR-020, CERN-LHCC-2013-006

[8] T. Alexopoulos *et al.*, *Performance of the first version of VMM front-end ASIC with resistive micromega detectors*, ATL-UPGRADE-PUB-2014-001

7 Appendix A: VMM2 tips

- When reading a mini-1 board through a CDAQ card, download the firmware directly into the fpga, not into the eprom - the latter download does not work.
- The 8 and 10 bit ADCs use a clockless duak-stage-current mode architecture. In a first pass, the 10- and 8-bit ADCs determine the 6 and 5 most significant bits of the peak and time values, repectively. On a second pass, the last LSB (4 and 3, respectively) are determined. The conversion times for the two passes are approximately 200 and 100 ns, respectively. The conversion time allocated to each of the two passes can be increased by 60 ns by setting monostables with the registers sc10b01 and sc10b10 for the 10-bit ADC, and sc801 and sc810 for the 8-bit ADC. It is useful to avoid that the 10-bit ADC reset the data before the 8-bit ADC has latched them into the FIFOs.

  The bit s8b accelerates the 8-bit timing ADC conversion by starting the process at the start of the timing ramp, rather than at its stop to further alleviate the above mentioned problem.
- Page 13 of the ic134 document describes two types of VMM reset:

  The soft (acquisition) reset clears the gray-code counter, the token passing logic, the FIFO control logic, the FIFO content, the channel control and discrimination logic, and the peak detector.

  The hard (global) reset clears the counter memory, the channel data memory (in normal operation both memories are loaded in the FIFO at the completion of each event), and the configuration registers.

8 Appendix B: Examples of data before and after the token loses synchronization

We first show a few events taken with the token logic fully functioning. We test pulse all 64 channels at a frequency of 1 Hz; the string of 64 infos is read out in less than 200 μsec so that when the next test pulse arrives, the FIFO should be empty.

BCID	CH	PDO	TDO
1106	1	528	25 3 12
1111	2	560	29 3 255
1111	3	459	32 3 255
1111	4	464	32 3 255
1106	5	471	31 3 255
1111	6	456	34 3 255
1111	7	438	33 3 255
1111	8	496	33 3 255
1106	10	480	24 3 255
1111	11	448	37 3 255
1111	12	149	32 3 255
1106	14	437	26 3 255
1111	15	428	34 3 255
1111	16	144	38 3 255
1111	17	481	35 3 255
1106	18	480	32 3 255
1106	19	480	32 3 255
1106	20	480	29 3 255
1111	21	454	36 3 255
1111	22	518	48 3 255
1106	23	496	48 3 255
1106	24	469	37 3 255
1111	25	544	48 3 255
1111	26	461	36 3 255
1106	27	463	56 3 255
1111	28	512	32 3 255
1111	29	480	32 3 255
1111	30	437	35 3 255
1111	31	449	32 3 255
1111	32	401	40 3 255
1111	33	439	35 3 255
1111	34	451	29 3 255
1111	35	493	40 3 255
1111	36	464	32 3 255
1111	37	448	34 3 255
1111	38	496	38 3 255
1111	39	447	48 3 255
1111	40	416	56 3 255
1111	41	464	56 3 255
1111	42	439	49 3 255
1111	43	384	43 3 255
1111	44	500	64 3 255
1111	45	464	63 3 255
1111	46	436	64 3 255
1111	47	437	48 3 255
1111	48	448	40 3 255
1111	49	425	56 3 255
1111	50	420	48 3 255
1111	51	400	64 3 255
1111	52	480	56 3 255
1106	53	374	48 3 255
1111	54	512	56 3 255
1111	56	432	56 3 255
1111	57	428	48 3 255
1111	58	405	49 3 255
1111	59	413	45 3 255
1111	60	496	40 3 255
1111	61	402	54 3 255
1111	63	391	42 3 255
1111	0	435	31 3 255
1525	0	432	32 3 12
1527	1	528	27 3 255
1527	2	560	24 3 255
1527	3	454	30 3 255
1527	4	464	32 3 255
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1527	7	439	32 3 255
1527	8	493	32 3 255
1527	10	480	28 3 255
1527	11	446	28 3 255
1525	12	149	35 3 255
1527	14	442	23 3 255
1527	15	426	32 3 255
1525	16	139	43 3 255
1527	17	480	33 3 255
1527	18	480	32 3 255
1527	19	480	34 3 255
1527	20	480	30 3 255
1527	21	448	32 3 255
1525	22	509	48 3 255
1527	23	496	48 3 255
1527	24	470	36 3 255
1525	25	544	51 3 255
1525	26	448	40 3 255
1525	27	464	56 3 255
1527	28	512	30 3 255
1527	29	483	30 3 255
1527	30	432	32 3 255
1527	31	448	28 3 255
1527	32	416	38 3 255
1527	33	439	32 3 255
1527	34	455	30 3 255
1527	35	499	38 3 255
1527	36	464	32 3 255
1527	37	448	35 3 255
1527	38	488	35 3 255
1527	39	442	48 3 255
1525	40	416	56 3 255
1527	41	461	56 3 255
1525	42	437	51 3 255
1527	43	380	40 3 255
1527	44	501	64 3 255
1525	45	464	61 3 255
1525	46	434	64 3 255
1527	47	437	48 3 255
1527	48	453	40 3 255
1527	49	424	56 3 255
1527	50	416	48 3 255
1525	51	400	64 3 255
1525	52	458	58 3 255
1525	53	368	54 3 255
1525	54	512	58 3 255
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3732	3	455	33 3 255
3732	4	464	31 3 255
3733	5	468	29 3 255
3732	6	451	35 3 255
3732	7	448	38 3 255
3732	8	497	37 3 255
3732	10	478	30 3 255
3732	11	447	34 3 255
3732	12	148	32 3 255
3733	14	447	24 3 255
3732	15	418	33 3 255
3732	16	144	40 3 255
3732	17	480	32 3 255
3732	18	465	32 3 255
3732	19	482	38 3 255
3732	20	496	32 3 255
3732	21	448	34 3 255
3732	22	512	48 3 255
3733	23	496	48 3 255
3732	24	470	40 3 255
3732	25	528	48 3 255
3732	26	455	40 3 255
3733	27	448	56 3 255
3732	28	512	35 3 255
3732	29	480	33 3 255
3733	30	432	32 3 255
3732	31	448	32 3 255
3732	32	416	40 3 255
3733	33	434	33 3 255
3732	34	448	32 3 255
3733	35	496	34 3 255
3732	36	464	32 3 255
3732	37	461	35 3 255
3732	38	484	38 3 255
3732	39	444	48 3 255
3732	40	416	56 3 255
3732	41	464	58 3 255
3732	42	443	51 3 255
3732	43	380	40 3 255
3732	44	500	72 3 255
3732	45	464	64 3 255
3732	46	448	64 3 255
3732	47	440	48 3 255
3733	48	448	40 3 255
3732	49	423	56 3 255
3732	50	416	48 3 255
3732	51	400	64 3 255
3732	52	459	56 3 255
3732	53	368	50 3 255
3732	54	512	56 3 255
3732	56	432	56 3 255
3732	57	429	48 3 255
3732	58	404	48 3 255
3732	59	410	43 3 255
3732	60	480	40 3 255
3732	61	400	53 3 255
3732	63	392	42 3 255

The next file contains about 30 events acquired after the token-passing logic is no more synchronized with the clocks CKTK and CKDT. One sees events containing replicas of the same channel, but one can also see events in which a bunch of channels is read out multiple times after successive events events were processed, and events in which most data are lost because the FIFO are full even if test-pulsing with a 1 Hz frequency.

Data flow from top to bottom, left to right columns, and into the next page. For each string of data, the first number is the BCID which is equal within a few counts for all 64 channels fired at the same time; the second is the channel number; and the third and fourth numbers are the PDO and TDO values. The symbols * and r indicate channels read out correctly and replicas, respectively. We mark the first few events.


```
2501 43 384 43 3  14 * ev 1
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 42 384 43 3 255 r
2501 63 391 42 3 255 *
2501 0 433 32 3 255  *
2501 1 544 32 3 255  *
2501 2 560 29 3 255  *
2501 3 456 25 3 255  *
2501 4 464 28 3 255  *
2501 5 471 36 3 255  *
2501 6 451 33 3 255  *
2501 7 447 29 3 255  *
2501 8 499 32 3 255  *
2501 8 499 32 3 255  r
2501 8 499 32 3 255  r
2501 12 149 32 3 255 *
2501 14 444 24 3 255 *
2501 14 444 24 3 255 r
2501 16 144 40 3 255 *
2501 16 144 40 3 255 r
2501 18 479 32 3 255 *
2501 19 483 37 3 255 *
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r

2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r
2501 18 483 37 3 255 r


2181 18 483 37 3 255 r ev 2

2501 18 483 37 3 255 r ev 1

2181 18 483 33 3 255 r ev 2
2181 18 483 33 3 255 r
2181 18 483 32 3 255 r
2181 18 483 33 3 255 r
2181 18 481 32 3 255 r

133 18 483 32 3 255  r ev 3
133 18 480 32 3 255  r

102 35 493 40 3 29  * ev 4
103 36 464 32 3 255 *
103 38 489 40 3 255 *
102 39 444 48 3 255 *
102 40 416 56 3 255 *
103 41 448 56 3 255 *
102 42 443 50 3 255 *
102 43 379 46 3 255 *
102 44 499 72 3 255 *
103 45 464 56 3 255 *
102 46 437 64 3 255 *
103 47 435 48 3 255 *
103 48 454 40 3 255 *
102 49 424 56 3 255 *
102 50 416 50 3 255 *
102 51 400 61 3 255 *
103 52 480 56 3 255 *
103 53 374 48 3 255 *
103 52 374 48 3 255 r
103 56 432 56 3 255 *
103 57 431 48 3 255 *
103 56 431 48 3 255 r
103 56 431 48 3 255 r
102 60 480 45 3 255 *
103 61 405 48 3 255 *
103 63 392 39 3 255 *
103 0 435 25 3 255  *
103 1 528 32 3 255  *
103 2 560 24 3 255  *
103 3 459 25 3 255  *
103 4 463 24 3 255  *
103 5 471 32 3 255  *
103 6 458 32 3 255  *
102 7 439 38 3 255  *
103 8 496 32 3 255  *
103 10 480 24 3 255 *
103 11 446 27 3 255 *
102 12 149 35 3 255 *
103 14 443 25 3 255 *
102 15 420 36 3 255 *
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102 16 144 40 3 255 *
103 17 481 32 3 255 *
103 18 480 32 3 255 *
103 19 480 40 3 255 *
103 20 480 32 3 255 *
103 21 448 32 3 255 *
103 22 513 40 3 255 *
103 23 496 48 3 255 *
103 24 465 40 3 255 *
103 25 528 48 3 255 *
103 26 448 32 3 255 *
101 27 464 56 3 255 *
103 28 512 32 3 255 *
103 29 484 31 3 255 *
102 30 432 35 3 255 *
102 31 450 35 3 255 *
103 32 416 40 3 255 *
103 33 436 31 3 255 *
102 34 451 34 3 255 *

684 35 496 35 3 255 * ev 5
684 36 464 33 3 255 *
677 37 448 35 3 255 *
684 38 496 34 3 255 *
677 40 416 56 3 255 *
677 41 459 56 3 255 *
677 42 436 50 3 255 *
684 44 510 64 3 255 *
677 45 464 60 3 255 *
677 46 437 64 3 255 *
684 47 480 48 3 255 *
684 48 453 40 3 255 *
684 49 424 56 3 255 *
677 50 416 50 3 255 *
677 51 400 64 3 255 *
677 52 463 58 3 255 *
684 53 370 48 3 255 *
684 52 370 48 3 255 r
684 56 432 56 3 255 *
684 57 429 48 3 255 *
684 56 429 48 3 255 r
684 56 429 48 3 255 r
677 60 480 44 3 255 *
684 61 400 48 3 255 *
684 10 480 28 3 255 *
677 11 448 36 3 255 *
677 15 429 40 3 255 *
677 17 480 36 3 255 *
684 20 480 32 3 255 *
677 21 448 36 3 255 *
684 22 512 43 3 255 *
684 23 496 48 3 255 *
677 24 465 41 3 255 *
677 25 544 49 3 255 *
677 26 461 40 3 255 *
684 27 464 56 3 255 *
677 28 512 36 3 255 *
684 29 481 29 3 255 *
677 30 432 36 3 255 *
677 31 448 35 3 255 *
684 32 416 40 3 255 *
684 33 434 32 3 255 *
684 34 457 31 3 255 *

2501 35 496 40 3 255 * ev 1
2501 36 464 32 3 255 *
2501 37 456 38 3 255 *
2501 38 496 37 3 255 *
2501 39 432 48 3 255 *
2501 40 418 56 3 255 *
2501 41 464 56 3 255 *
2501 42 433 48 3 255 *
2501 44 510 64 3 255 *
2501 45 464 56 3 255 *
2501 46 448 48 3 255 *
2501 47 438 48 3 255 *
2501 48 448 40 3 255 *
2501 49 424 56 3 255 *
2501 50 416 48 3 255 *
2501 51 400 64 3 255 *
2501 52 463 56 3 255 *
2501 53 370 48 3 255 *
2501 52 370 48 3 255 r
2501 56 432 56 3 255 *
2501 57 429 48 3 255 *
2501 56 429 48 3 255 r
2501 56 429 48 3 255 r
2501 60 480 41 3 255 *
2501 61 400 51 3 255 *
2501 10 480 31 3 255 *
2501 11 448 32 3 255 *
2501 15 422 38 3 255 *
2501 17 480 32 3 255 *
2501 20 480 32 3 255 *
2501 21 448 34 3 255 *
2501 22 513 43 3 255 *
2501 23 496 48 3 255 *
2501 24 465 40 3 255 *
2501 25 528 48 3 255 *
2501 26 448 39 3 255 *
2501 27 464 56 3 255 *
2501 28 512 33 3 255 *
2501 29 484 33 3 255 *
2501 30 432 32 3 255 *
2501 31 448 30 3 255 *
2501 32 416 40 3 255 *
2501 33 439 35 3 255 *
2501 34 448 31 3 255 *

102 35 493 40 3 255 * ev 4
103 36 464 32 3 255 *
103 37 456 32 3 255 *
103 38 489 40 3 255 *
102 39 432 48 3 255 *
102 40 418 56 3 255 *
103 41 464 56 3 255 *
102 42 435 50 3 255 *
102 44 499 72 3 255 *
103 45 464 56 3 255 *
102 46 448 64 3 255 *
103 47 435 48 3 255 *
103 48 448 40 3 255 *
102 49 424 56 3 255 *
102 50 416 50 3 255 *
102 51 400 61 3 255 *
103 52 463 56 3 255 *
103 53 374 48 3 255 *
103 52 374 48 3 255 r
103 56 432 56 3 255 *
103 57 431 48 3 255 *
103 56 431 48 3 255 r
103 56 431 48 3 255 r
102 60 480 45 3 255 *
103 61 405 48 3 255 *
103 10 480 24 3 255 *
103 11 448 27 3 255 *
102 15 429 36 3 255 *
103 17 481 32 3 255 *
103 20 480 32 3 255 *
103 21 448 32 3 255 *
103 22 513 40 3 255 *
103 23 496 48 3 255 *
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103 24 465 40 3 255 *
103 25 528 48 3 255 *
103 26 461 32 3 255 *
101 27 464 56 3 255 *
103 28 512 32 3 255 *
103 29 484 31 3 255 *
102 30 432 35 3 255 *
102 31 450 35 3 255 *
103 32 416 40 3 255 *
103 33 436 31 3 255 *
102 34 448 34 3 255 *
102 34 448 34 3 255 *
102 34 448 34 3 255 *
102 34 448 34 3 255 *

2819 0 434 27 3 25   * ev 6
2819 1 544 32 3 255  *
2819 2 560 31 3 255  *
2819 3 453 31 3 255  *
2822 4 464 28 3 255  *
2819 5 472 39 3 255  *
2819 6 454 34 3 255  *
2819 7 448 37 3 255  *
2819 8 496 33 3 255  *
2819 8 496 33 3 255  r
2819 8 496 33 3 255  r
2819 12 151 32 3 255 *
2819 14 443 31 3 255 *
2819 14 443 31 3 255 r
2819 16 144 40 3 255 *
2819 16 144 40 3 255 r
2819 18 480 32 3 255 *
2819 19 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
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2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 18 488 40 3 255 r
2819 43 383 42 3 255 *
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2819 42 383 42 3 255 r
2822 54 496 56 3 255 *
2822 54 496 56 3 255 r
2822 54 496 56 3 255 r
2819 58 402 48 3 255 *
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2819 58 402 48 3 255 r
2819 58 402 48 3 255 r
2819 58 402 48 3 255 r
2819 63 394 42 3 255 *

2501 54 512 56 3 255 * ev 1
2501 54 512 56 3 255 r
2501 54 512 56 3 255 r
2501 58 404 48 3 255 *
2501 58 404 48 3 255 r
2501 58 404 48 3 255 r
2501 58 404 48 3 255 r

102 54 512 58 3 255 * ev 4
102 54 512 58 3 255 r
102 54 512 58 3 255 r
103 58 404 44 3 255 *
103 58 404 44 3 255 r
103 58 404 44 3 255 r
103 58 404 44 3 255 r

2822 54 512 56 3 255 ev 6
2822 54 512 56 3 255
2822 54 512 56 3 255
2819 58 406 48 3 255
2819 58 406 48 3 255
2819 58 406 48 3 255
2819 58 406 48 3 255

547 43 383 40 3 12   ev 8
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
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547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255
547 42 383 40 3 255  r
547 63 392 41 3 255  *
545 0 432 32 3 255   *
547 1 528 30 3 255   *
547 2 560 27 3 255   *
547 3 457 30 3 255   *
547 4 464 32 3 255   *
547 5 471 32 3 255   *
547 6 457 33 3 255   *
547 7 437 32 3 255   *
547 8 498 32 3 255   *
547 8 498 32 3 255   r
547 8 498 32 3 255   r
547 12 149 24 3 255  *
547 14 432 29 3 255  *
547 14 432 29 3 255  r
547 16 143 32 3 255  *
547 16 143 32 3 255  r
547 18 480 35 3 255  *
547 19 486 56 3 255  *
547 18 486 56 3 255  r
547 18 486 56 3 255
547 18 486 56 3 255
547 18 486 56 3 255
547 18 486 56 3 255
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547 18 486 56 3 255
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547 18 486 56 3 255
547 18 486 56 3 255
547 18 486 56 3 255
547 18 486 56 3 255
547 18 486 56 3 255
547 18 486 56 3 255  r

3904 43 378 43 3 14  * ev 9
3904 42 378 43 3 255 r
3904 42 378 43 3 255 r
3904 42 378 43 3 255 r
3904 42 378 43 3 255
3904 42 378 43 3 255
3904 42 378 43 3 255
3904 42 378 43 3 255
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3904 42 378 43 3 255
3904 42 378 43 3 255
3904 42 378 43 3 255
3904 42 378 43 3 255 r
3904 63 390 40 3 255
3904 0 432 29 3 255 *
3905 1 528 27 3 255 *
3905 2 544 27 3 255 *
3904 3 451 32 3 255 *
3904 4 464 31 3 255 *
3904 5 464 37 3 255 *
3904 6 448 34 3 255 *
3904 7 448 32 3 255 *
3904 8 496 35 3 255 *
3904 8 496 35 3 255 r
3904 8 496 35 3 255 r
3904 12 148 30 3 255 *
3904 14 447 29 3 255 *
3904 14 447 29 3 255 r
3904 16 143 40 3 255 *
3904 16 143 40 3 255 r
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3904 18 464 34 3 255 *
3904 19 480 34 3 255 *
3904 18 480 34 3 255 r
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
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3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255
3904 18 480 34 3 255 r

3840 18 480 34 3 255 ev 10

3904 18 480 34 3 255 ev 9

3840 18 480 32 3 255  ev 10
3840 18 480 32 3 255

2816 18 480 32 3 255 ev 11
2816 18 480 32 3 255
2816 18 480 32 3 255

768 18 480 32 3 255  ev 12
768 18 480 32 3 255

1185 35 487 35 3 14     ev 13
1185 36 464 38 3 255
1185 37 448 33 3 255
1185 38 480 40 3 255
1185 39 441 48 3 255
1185 40 416 56 3 255
1185 41 457 56 3 255
1185 42 443 48 3 255
1185 43 377 46 3 255
1185 44 499 64 3 255
1185 45 464 56 3 255
1185 46 432 64 3 255
1185 47 432 50 3 255
1185 48 447 42 3 255
1185 49 416 56 3 255
1185 50 416 48 3 255
1185 51 398 64 3 255
1185 52 455 56 3 255
1185 53 368 54 3 255
1185 52 368 54 3 255
1185 56 428 56 3 255
1185 57 428 48 3 255
1185 56 428 48 3 255
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1185 56 428 48 3 255
1185 60 480 44 3 255
1185 61 400 48 3 255
1185 63 387 44 3 255
1185 0 432 32 3 255
1185 1 528 27 3 255
1185 2 560 24 3 255
1185 3 451 30 3 255
1185 4 464 32 3 255
1185 5 466 34 3 255
1185 6 448 27 3 255
1185 7 439 32 3 255
1185 8 493 32 3 255
1185 10 472 26 3 255
1185 11 446 31 3 255
1185 12 146 27 3 255

1248 14 432 24 3 255 ev 14

1185 15 422 31 3 255 ev 13
1185 16 144 42 3 255
1185 17 483 32 3 255
1185 18 477 32 3 255
1185 19 479 39 3 255
1185 20 480 34 3 255
1185 21 448 32 3 255
1185 22 512 43 3 255
1185 23 496 48 3 255
1185 24 470 36 3 255
1185 25 528 48 3 255
1185 26 458 32 3 255
1185 27 457 56 3 255
1185 28 512 36 3 255
1185 29 482 30 3 255
1185 30 432 34 3 255
1185 31 448 28 3 255
1185 32 411 42 3 255
1185 33 432 37 3 255
1185 34 448 33 3 255

547 35 496 37 3 255 * ev 8
545 36 464 38 3 255 *
547 37 448 32 3 255 *
547 38 496 35 3 255 *
547 39 448 48 3 255 *
545 40 416 56 3 255 *
547 41 463 56 3 255 *
545 42 436 49 3 255 *
545 44 510 64 3 255 *
547 45 464 56 3 255 *
547 46 436 48 3 255 *
547 47 440 48 3 255 *
547 48 457 40 3 255 *
545 49 427 56 3 255 *
547 50 422 46 3 255 *
545 51 400 64 3 255 *
545 52 461 59 3 255 *
547 53 375 48 3 255 *
547 52 375 48 3 255 *
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547 57 430 48 3 255 *
547 56 430 48 3 255 r
547 56 430 48 3 255 r
547 60 480 40 3 255 *
547 61 400 48 3 255 *
547 10 480 24 3 255 *
547 11 448 32 3 255 *
547 15 431 34 3 255 *
547 17 480 29 3 255 *
547 20 480 32 3 255 *
547 21 448 32 3 255 *
547 22 512 43 3 255 *
547 23 496 48 3 255 *
547 24 470 36 3 255 *
547 25 544 48 3 255 *
545 26 458 40 3 255 *
547 27 464 56 3 255 *
545 28 512 35 3 255 *
545 29 485 35 3 255 *
545 30 432 35 3 255 *
547 31 448 30 3 255 *
547 32 415 40 3 255 *
547 33 446 31 3 255 *
547 34 454 32 3 255 *

3905 35 496 40 3 255 *  ev 9
3904 36 464 33 3 255 *
3904 37 448 35 3 255 *
3904 38 496 38 3 255 *
3904 39 447 48 3 255 *
3904 40 416 56 3 255 *
3904 41 464 56 3 255 *
3904 42 436 48 3 255 *
3904 44 510 64 3 255 *
3904 45 464 56 3 255 *
3904 46 448 64 3 255 *
3904 47 432 48 3 255 *
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3904 49 421 56 3 255 *
3904 50 416 48 3 255 *
3904 51 400 64 3 255 *
3904 52 462 56 3 255 *
3904 53 375 48 3 255 *
3904 52 375 48 3 255 r
3904 56 432 56 3 255 *
3904 57 426 48 3 255 *
3904 56 426 48 3 255 r
3904 56 426 48 3 255 r
3904 60 480 41 3 255 *
3904 61 400 51 3 255 *
3905 10 480 24 3 255 *
3904 11 446 32 3 255 *
3904 15 427 38 3 255 *
3904 17 480 32 3 255 *
3904 20 480 32 3 255 *
3904 21 456 33 3 255 *
3904 22 514 47 3 255 *
3905 23 496 48 3 255 *
3904 24 470 38 3 255 *
3904 25 544 48 3 255 *
3904 26 448 39 3 255 *
3904 27 464 56 3 255 *
3904 28 512 33 3 255 *
3904 29 485 32 3 255 *
3904 30 432 32 3 255 *
3905 31 448 31 3 255 *
3904 32 411 40 3 255 *
3904 33 439 35 3 255 *
3905 34 454 27 3 255 *

1185 35 496 35 3 255  ev 13
1185 36 464 38 3 255
1185 37 448 33 3 255
1185 38 480 40 3 255
1185 39 441 48 3 255
1185 40 416 56 3 255
1185 41 464 56 3 255
1185 42 443 48 3 255
1185 44 504 64 3 255
1185 45 464 56 3 255
1185 46 436 64 3 255
1185 47 432 50 3 255
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1185 48 448 42 3 255
1185 49 422 56 3 255
1185 50 416 48 3 255
1185 51 398 64 3 255
1185 52 462 56 3 255
1185 53 368 54 3 255
1185 52 368 54 3 255
1185 56 432 56 3 255
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1185 60 480 44 3 255
1185 61 400 48 3 255
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1185 15 431 31 3 255
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1185 20 480 34 3 255
1185 21 448 32 3 255
1185 22 512 43 3 255
1185 23 496 48 3 255
1185 24 470 36 3 255
1185 25 528 48 3 255
1185 26 458 32 3 255
1185 27 457 56 3 255
1185 28 512 36 3 255
1185 29 480 30 3 255
1185 30 432 34 3 255
1185 31 448 28 3 255
1185 32 411 42 3 255
1185 33 432 37 3 255
1185 34 455 33 3 255
1185 34 455 33 3 255
1185 34 455 33 3 255
1185 34 455 33 3 255

1155 0 432 27 3 14    ev 15
1155 1 528 32 3 255
1153 2 528 29 3 255
1155 3 450 32 3 255
1155 4 464 33 3 255
1155 5 464 35 3 255
1155 6 453 38 3 255
1155 7 442 38 3 255
1155 8 496 37 3 255
1155 8 496 37 3 255
1155 8 496 37 3 255
1155 12 149 32 3 255
1155 14 437 28 3 255
1155 14 437 28 3 255
1155 16 143 40 3 255
1155 16 143 40 3 255
1155 18 480 32 3 255
1155 19 480 34 3 255
1155 18 480 34 3 255
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1153 42 378 40 3 255
1153 42 378 40 3 255
1155 54 512 56 3 255
1155 54 512 56 3 255
1155 54 512 56 3 255
1155 58 406 48 3 255
1155 58 406 48 3 255
1155 58 406 48 3 255
1155 58 406 48 3 255
1155 63 389 42 3 255

3904 54 512 56 3 255 * ev 9
3904 54 512 56 3 255 r
3904 54 512 56 3 255 r
3904 58 400 48 3 255 *
3904 58 400 48 3 255 r
3904 58 400 48 3 255 r
3904 58 400 48 3 255 r

1185 54 512 59 3 255 ev 13
1185 54 512 59 3 255
1185 54 512 59 3 255
1185 58 400 43 3 255
1185 58 400 43 3 255
1185 58 400 43 3 255
1185 58 400 43 3 255

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Not reviewed, for internal circulation only

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3929 1 544 32 3 255
3929 2 560 25 3 255
3929 3 463 28 3 255
3929 4 464 30 3 255
3929 5 471 36 3 255
3929 6 455 36 3 255
3929 7 447 32 3 255
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3929 8 498 36 3 255
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1881 18 488 32 3 255  ev 33

1353 18 488 32 3 255  ev 34

1881 18 488 32 3 255  ev 33

1353 18 488 32 3 255  ev 34
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1353 18 488 32 3 255
1353 18 488 32 3 255
1353 18 488 32 3 255
1353 18 480 32 3 255

571 35 491 41 3 29    ev 35
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571 37 448 31 3 255
570 38 484 40 3 255
571 39 442 48 3 255
570 40 416 56 3 255
571 41 464 56 3 255
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571 43 378 40 3 255
571 44 501 64 3 255
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571 46 434 48 3 255
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571 48 456 40 3 255
571 49 419 56 3 255
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571 4 464 30 3 255
571 5 472 32 3 255
571 6 448 32 3 255
571 7 441 32 3 255
571 8 493 32 3 255
570 10 472 31 3 255
571 11 448 31 3 255
571 12 149 25 3 255
571 14 447 29 3 255
571 15 425 32 3 255
570 16 143 43 3 255
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570 18 480 34 3 255
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571 21 448 32 3 255
571 22 512 43 3 255
570 23 496 49 3 255
571 24 471 38 3 255
571 25 528 48 3 255
570 26 448 40 3 255
570 27 464 56 3 255
571 28 512 32 3 255
571 29 480 28 3 255
570 30 432 37 3 255
570 31 448 34 3 255
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570 34 451 33 3 255

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1273 36 464 38 3 255  ev 31
1273 37 449 40 3 255

1256 38 496 35 3 255 ev 30
1256 39 444 48 3 255

1273 40 417 56 3 255  ev 31
1273 41 464 56 3 255
1273 42 438 49 3 255

1256 44 508 64 3 255  ev 30
1256 45 464 56 3 255
1256 46 448 64 3 255
1256 47 448 48 3 255
1256 48 448 40 3 255
1256 49 425 56 3 255

1273 50 416 50 3 255  ev 31
1273 51 400 64 3 255
1273 52 460 56 3 255

1256 53 375 48 3 255  ev 30
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1256 61 402 48 3 255  ev 30
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1256 17 481 30 3 255  ev 30

1273 20 496 36 3 255  ev 31

1256 21 455 36 3 255  ev 30
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1273 23 496 48 3 255 ev 31

1256 24 470 38 3 255 ev 30
1256 25 528 48 3 255
1256 26 464 36 3 255
1256 27 464 56 3 255

1273 28 512 36 3 255 ev 31

1256 29 480 27 3 255 ev 30

1273 30 432 34 3 255 ev 31

1257 31 448 32 3 255 ev 30
1256 32 416 40 3 255
1256 33 442 32 3 255
1256 34 453 33 3 255
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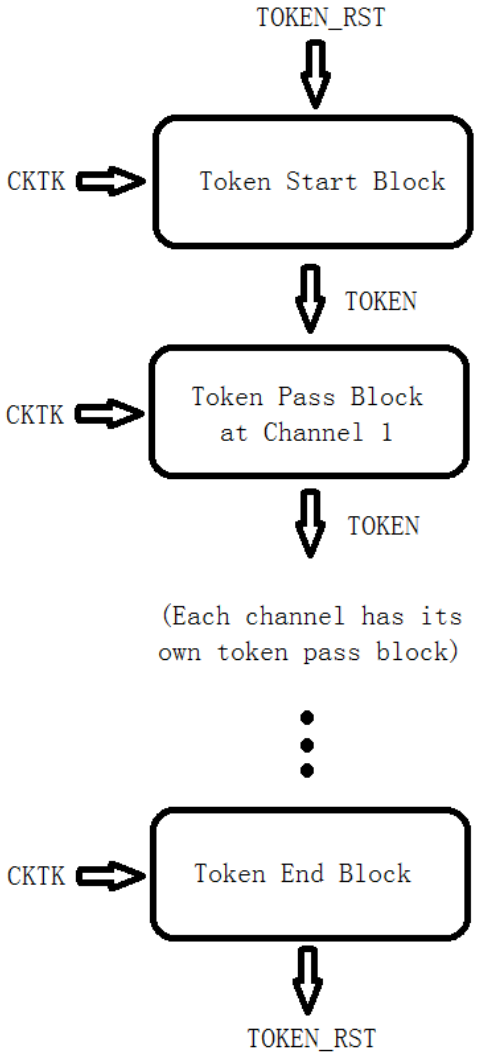
9 Appendix C: The token-passing scheme

Concise introduction to the FIFO and token logic

The 38-bit information of each VMM channel is stored into a FIFO memory. Each FIFO can store up to 4 events. There are 64 FIFOs, one for each of the 64 VMM channels. When a channel's info is stored in its FIFO, an additional flag – called flgsetrst – is asserted in the FIFO. This flag is set if at least one of the FIFO level is filled. The FIFO content is read out by a FPGA – such as the Virtex on the MMFE-8 board, or the ALTERA on the CDAQ board- which sends 2 clocks (CKTK and CKDT) to the VMM FIFO and token logic. The token logic consists, as explained in detail below, of a circular array of 64 token blocks –one for each FIFO- which are advanced by the CKTK cycle. When a token block is addressed, it checks if the flagsetrst of its corresponding channel is asserted. If not, the token passes to the next block on the CKTK cycle. If yes, the FIFO is interrogated, and sends a flag on the data0 line to the FPGA. The FPGA stops the CKTK clock and starts the CKDT clock which is used to empty the oldest FIFO info of this channel. When the 38-bit is read out, the flgsetrst is cleared unless the FIFO contains additional data. Once the 38-bit info is acquired, the writing and output point of the FIFO are updated. This results in overwriting events in the FIFO if the next happens before the first has been read out (see main text). Once the FPGA has read the 38-bit info, CKTK starts again, the token block moves to the next channels, and stops where a flagsetrst is asserted. Once the token block arrives to the end of the 64 channels, it goes back to the beginning

Diagram of Token Generation and Transfer

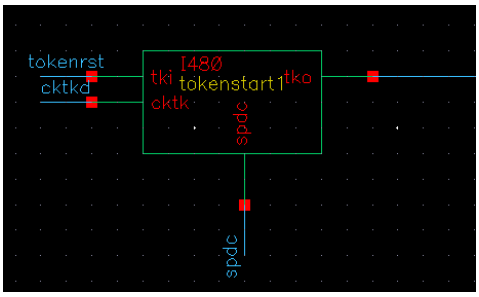


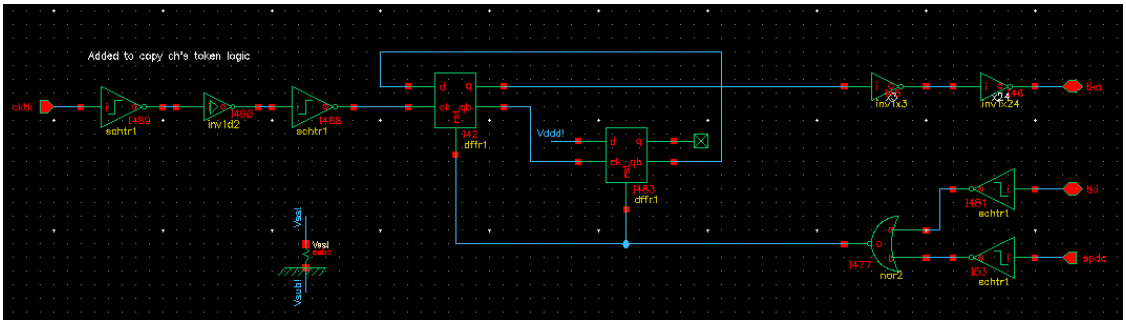
The above diagram shows the token generation and transfer scheme. The token system consists of three parts: one token start block, 64 identical token pass blocks, and one token end block. The “Token start block” generates the intial token at the rising edge of CKTK, which is passed to the token pass block at channel 1. As shown in the following section, there is a two-input multiplexer at the token pass block. One input is directly connected to the output of token start block, while the other one is connected to a D flip-flop. The multiplexer is controlled by a flag called “flgsetrst” which indicates whether there are data not read in the 4-depth FIFO. If there is no new data in channel-1 FIFO, the multiplexer makes channel 1 transparent to the token. If there are data not-yet read out in the channel-1 FIFO, the multiplexer chooses the second input so that the token stops at channel 1. However, when it stops at channel 1, the token will be regenerated at the following CKTK’s rising edge and the block behaves as a token start block.

The token is passed to the token pass block of channel 2. If channel 2 has no data, it is transparent to the token. The token will stop at the channel whose "flagsetrst" is asserted. If channel 2 has data, it will be emptied as channel 1 . In this way, the token is passed to channels which contain unread data. In the end, when the cycle arrives at token end block, the token end block send the token reset signal to the token start block. The token start block generates a new transfer round.

The following section describes the schematics of each block. Note: the schematics consists of basic logic blocks of inverts, D flip flops, NOR gates, and transmission gates as the symbols indicate. Although there are different types of inverts, they're all inverts logically. D flip flops resets at low; when rst=0, q=0 and qb=1; D flip flop triggers at the clock's falling edge; At clock's falling edge, q= d and qb=invert(d) .

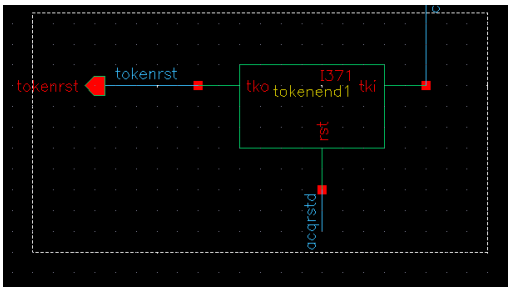
Token Start Block's Schematic

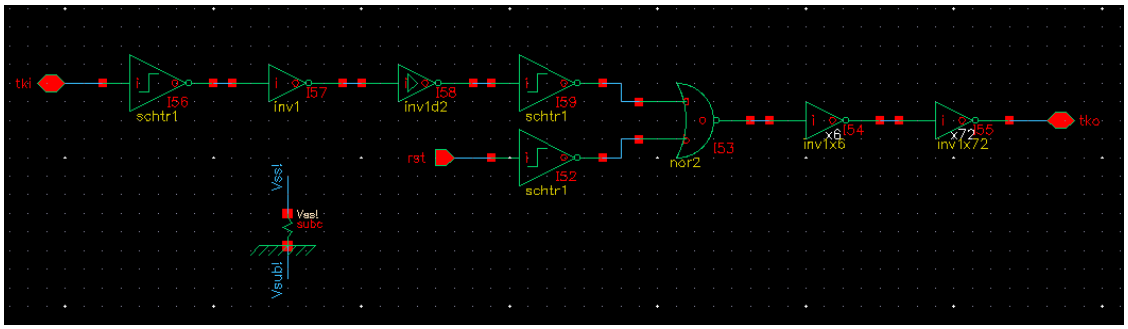




As shown, the token reset signal generated from the token end block is sent to the token start block through the tokenrst wire. It resets the two D flip flops in the token start block and sets the token to be low. At the first CKTK's rising edge after the reset, the token will be set to high - thus a token is generated. On the following CKTK's rising edge before the next reset, the tko port will stay low. Thus, no additional token is generated.

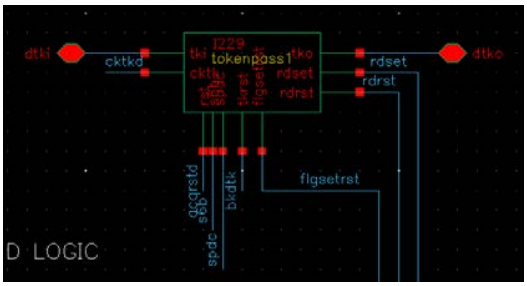
Token End Block's Schematics

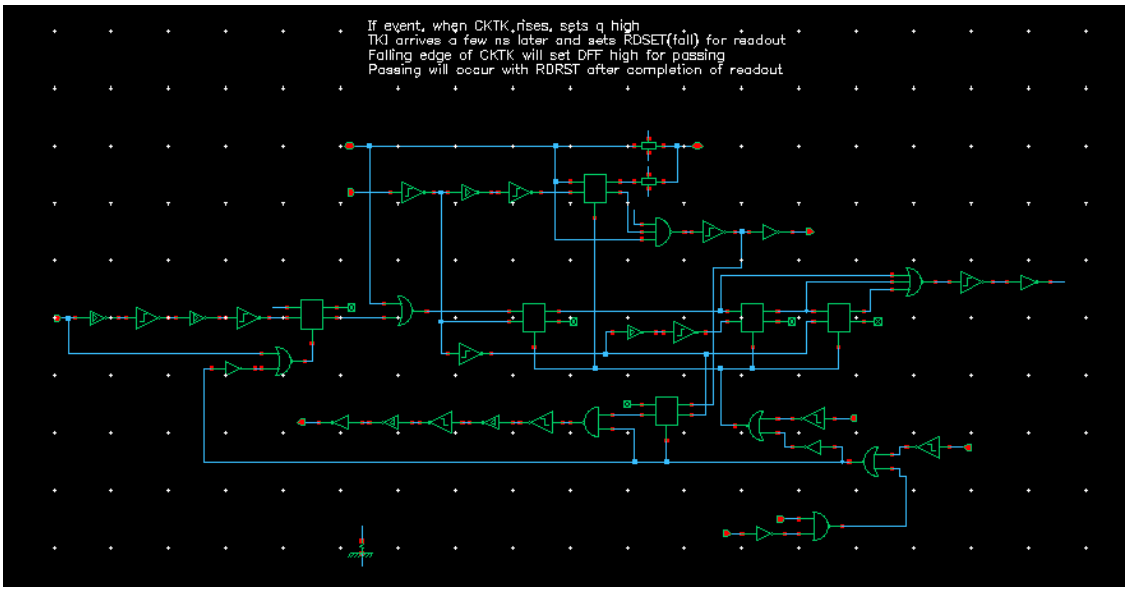




As shown, the token end block is an inverter with a long delay. As said previously, it is the termination of the token wheel. If the token stops at one channel, the tki port will always be low. Thus, the tko port which sends the token reset signal will stay high. When the token finally arrives at the token end block, the tko port becomes low, the reset signal is sent, and the token start block is reset. However, as shown in the following token pass block section, the token reset signal will not keep high all the time, since the previous token pass block will pull the token line down to be low in the following CKTK rising edge.

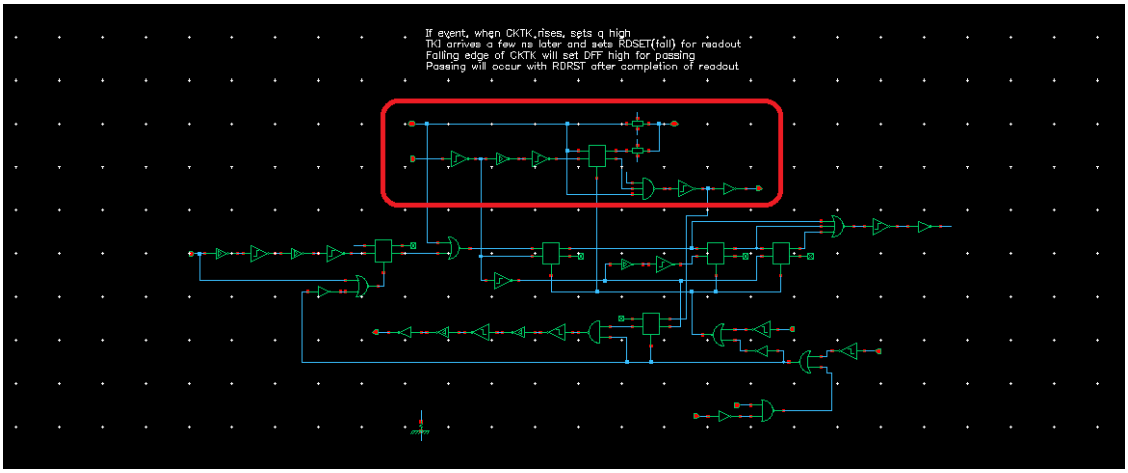
Token Pass Block's Schematic

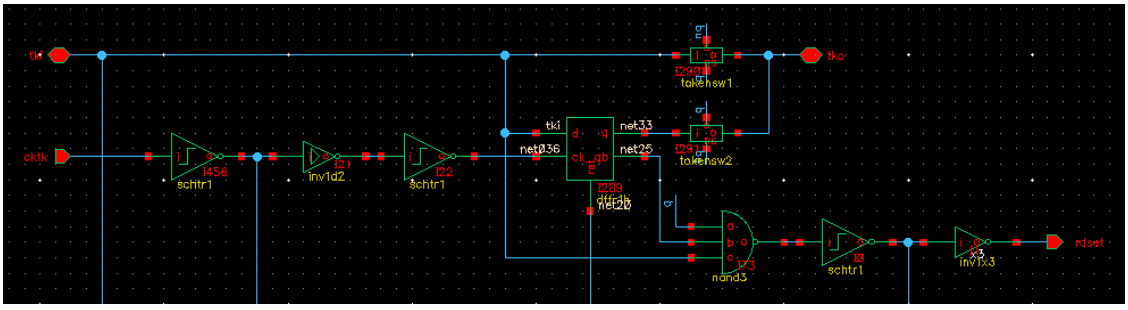




The token pass block is a bit complex. Its schematics is too complicated to be shown in one snapshot. So we divide it into two relevent parts which are separately described.

Token Pass Block's Schematic – Part 1

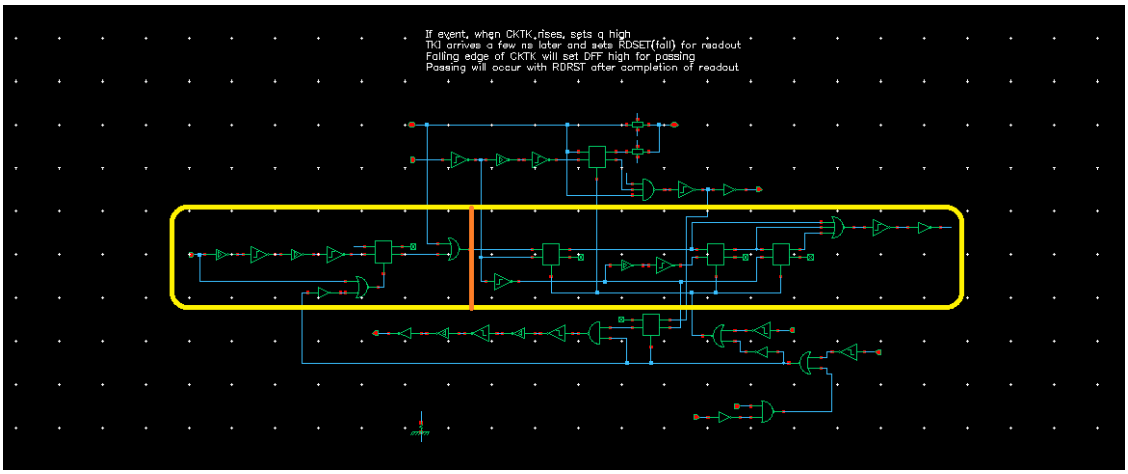


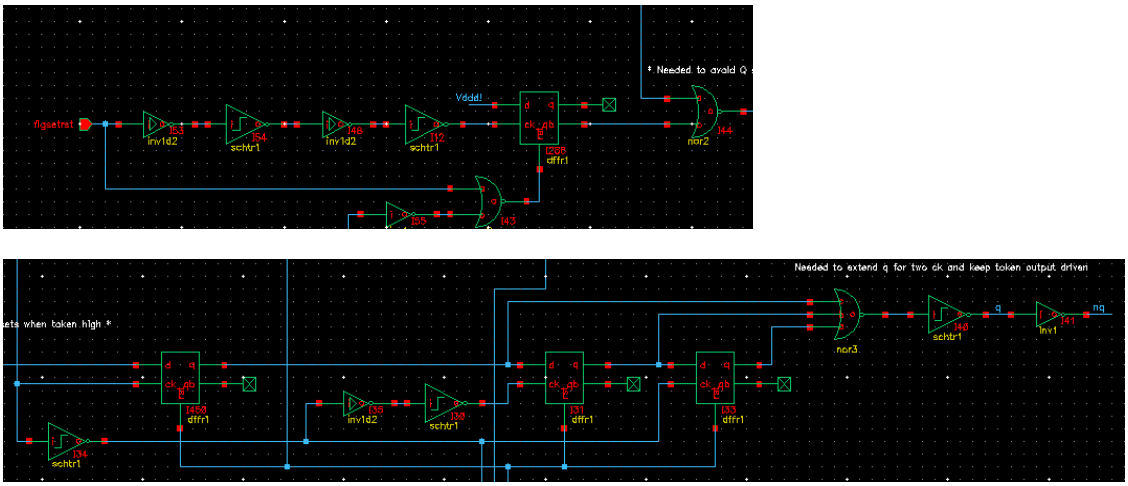


Part 1 is the upper section of the token pass block's schematic. It shows the token pass paths. The tki port receives the token signal generated from the token start block or the previous token pass block. Tokensw1 and tokensw2 form the two input multiplexer previously mentioned. They are swithes controlled by signal q and its invert nq, which will be described in part 2. One input of the multiplexer is the tki port; another input is the output of a D flip flop. When q=0 and nq=1, the first input is chosen. It's the situation where there are no data in the channel's FIFO. When q=1 and nq=0, the second input is chosen. It's the situation where there are data in the channel's FIFO. When the token doesn't arrive at a channel or the token already passed a channel, the tki port is low (Note: it becomes clear after the following explanation.). As the schematic shows, the D flip flop also outputs tki in the CKTK's rising edge. So no matter which path is chosen, the tko port is always low, which means the tki of the next token pass block is also low. When the token arrives at a channel which has data in the FIFO, the second path is chosen.

For example, the token is just generated from the token start block in one CKTK rising edge and channel 1 has data. Because of the delay in passing the toke to channel-1 tki-port, the channel-1 tko-port will still output a low signal in the same CKTK rising edge. Before the next CKTK rising edge, channel-1's tki-port will remain high; the token stops at channe 1. When the next CKTK rising edge arrives, the token is forwared to the following blocks by the D flip flop, and the channel-1 tki-port is pulled low by the token start block. That's how the token is transferred from channel to channel. The following part explains how the tokenl stops at channels which contain data in their FIFO.

Token Pass Block's Schematic – Part 2





Part 2 illustrates the middle section of the token-pass block's schematics. It's too large to be shown in a single snapshot. So it's divided into two parts. When there are data in one channel's FIFO, the flgsetrst signal is low (Note: it will stay low until all the data in the 4-depth FIFO is read out). In this situation, the nor2 gate is like an inverter whose input is the tki port. When the token doesn't arrive at a given channel or the token has already passed it, the D flip flop diffr1 will output a high signal, which means that q=1 and nq=0. As said above, the second input of the multiplexer is chosen. Thus, the token stops at this channel when it arrives.