



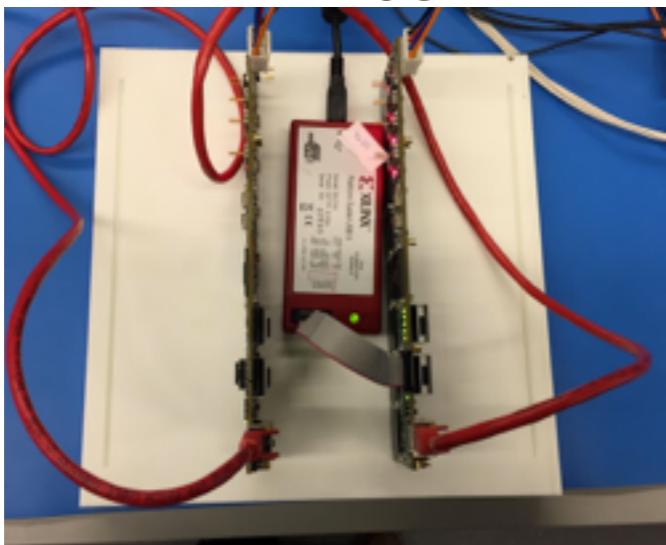
Status of the Harvard Micromegas Octuplet

NSW Electronics Meeting
September 9, 2016

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J. Huth, C. Rogan, S. Sussman, A. Tuna, A. Wang, N. Wuerfel

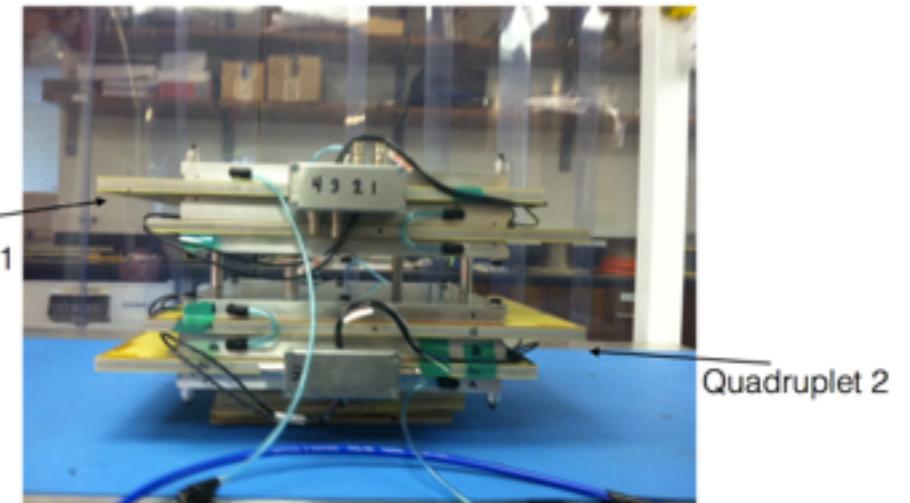
Overview

MMFE8s



+

MM Octuplet



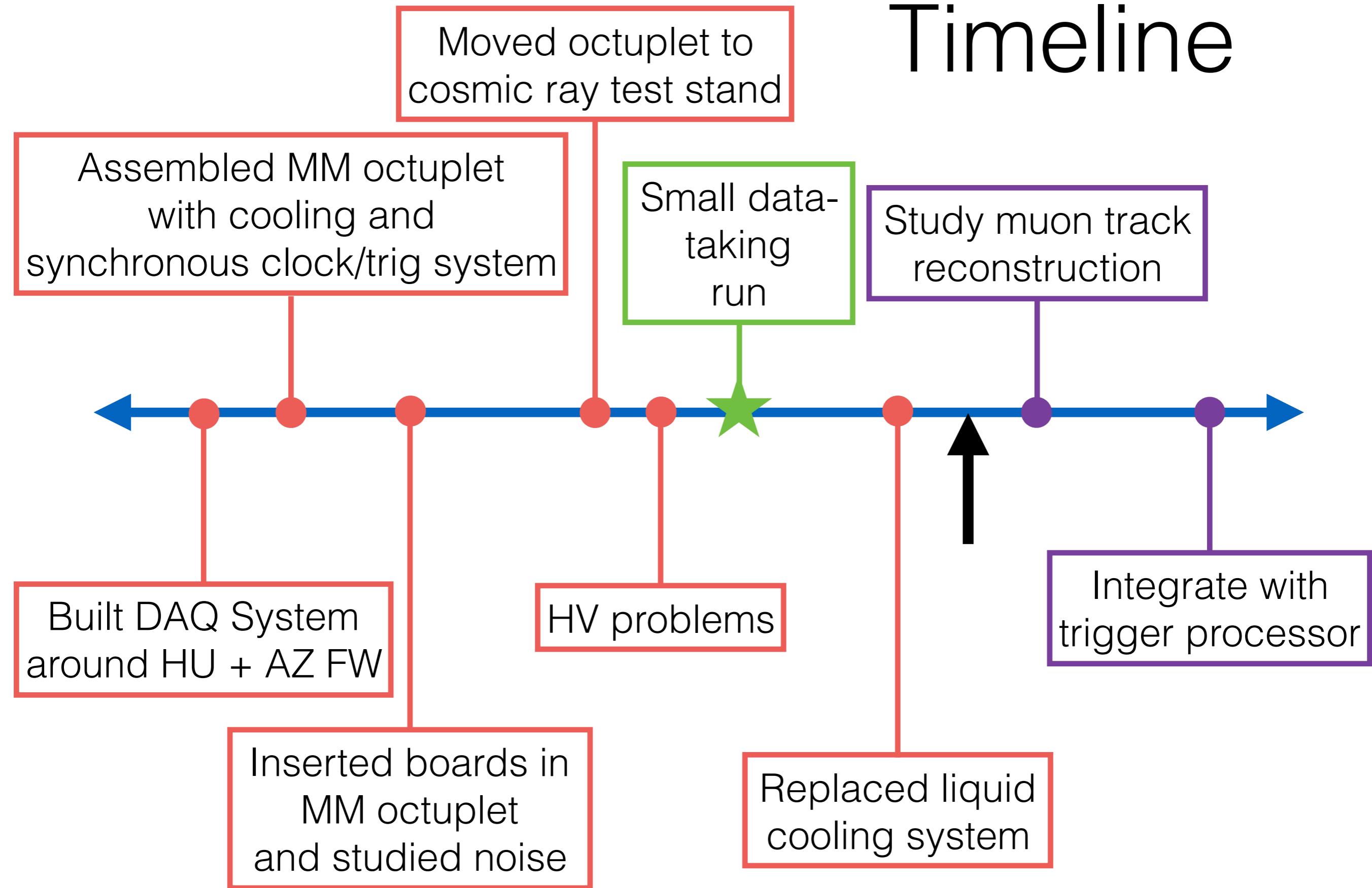
Trigger Processor

+



Putting together a system with 8 micromegas chambers,
MMFE8s, and trigger processor

Timeline



Outline

A. MMFE8s:

- Firmware
- Data taking software
- Calibration System

B. Octuplet Setup

- Cooling System
- Clock and Trigger Distributor

C. Integration

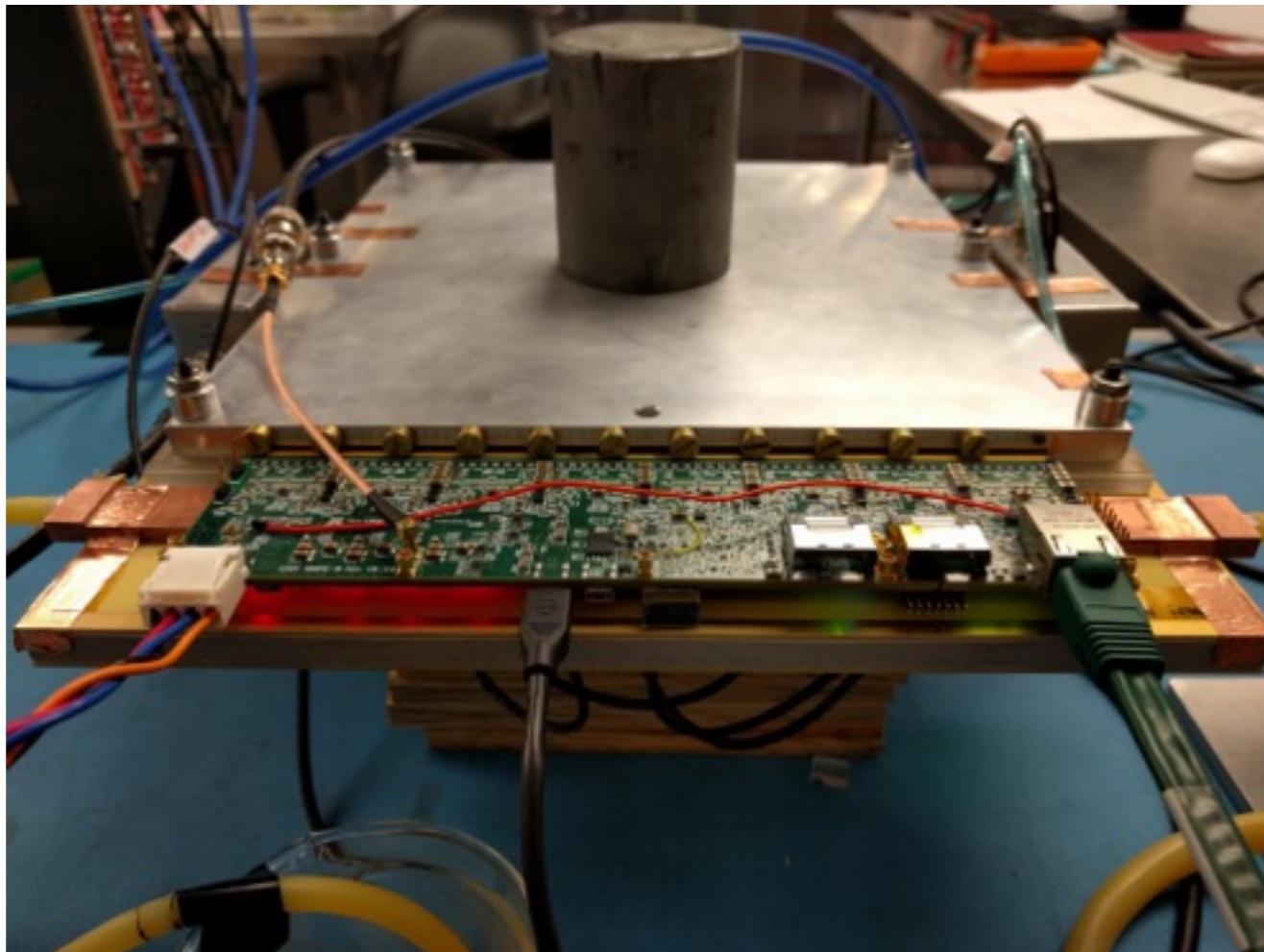
- Calibration of MMFE8 boards inside chambers
- **Noise issues**

D. Octuplet Goes to 38 Oxford

- **High voltage issues**
- Small mechanical issues

E. Current Status

MMFE8 Status



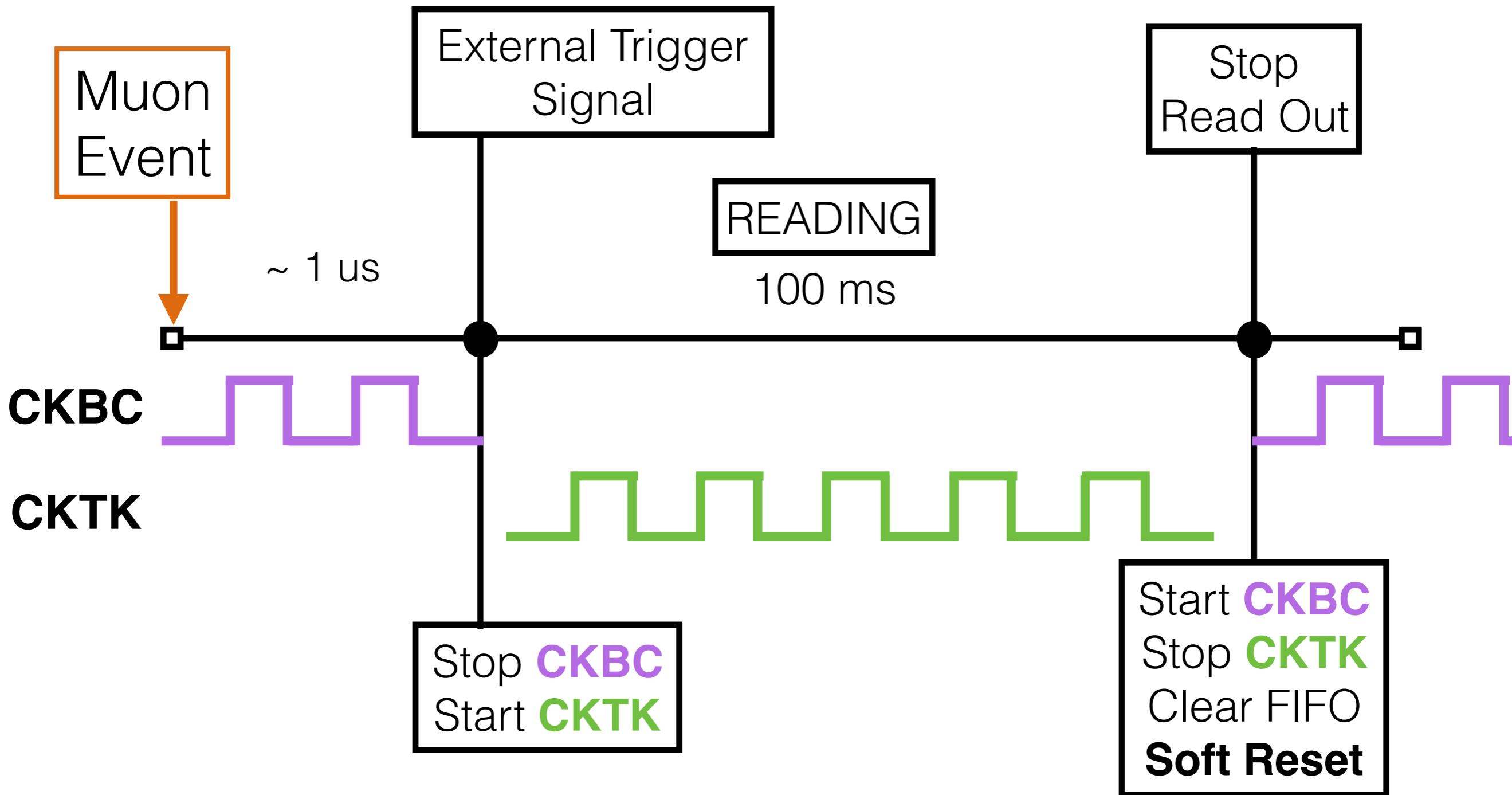
- Have been using Rev C + Rev D boards
- Have firmware + software DAQ system that is able to handle multiple MMFE8s with 8 VMMs each
- Before testing the octuplet, we have been testing boards on the bench as well as in a single chamber with HV

MMFE8 DAQ System

- Firmware, software is based on the HU+AZ firmware and GUI
- We implemented several additions:
 - We have incorporated a full Xilinx Vivado **license** (so there are no dropped ethernet connections with SDK after ~8-10 hours)
 - We have programmed **flash memory** of boards with the BIT + ELF files so we don't need the JTAG connector
 - All boards use a common input mother clock and external trigger signal for **synchronicity**

MMFE8 DAQ System

- The logic of the system presented in 12 February NSW elx meeting: <https://indico.cern.ch/event/496030/>, now we have added a few modifications
- For every event, we read out the **VMM data** from the FPGA FIFO, as well as (1) the **number of CKBC** preceding the event trigger and (2) the total **number of event triggers** that received
- If we don't see an event in 4096 BC's, we send a soft reset and a FIFO reset, otherwise we acquire the event and we send the resets at the end of the readout

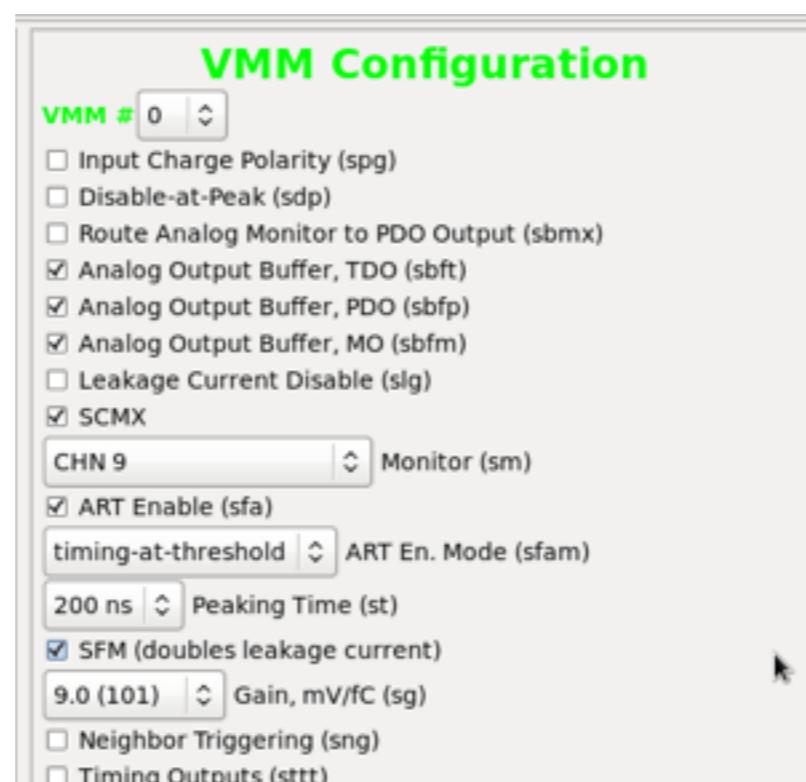


- CKTK is **starts** 1 us after the event to ensure that the event information has been transferred to the VMM FIFO
- When we acquired data with CKTK always running, we found that if the CKTK token was interrogating a VMM FIFO while it is being filled, we would get a string of nonsense data (often zeros)
- We informed Gianluigi of the problem and the fix
- With this fix, we are a 1-hit system since the channels FIFOs can be overwritten until they are read out by the FPGA

MMFE8 DAQ System



- Data-taking software:
 - GUI based on AZ original code for 1 board
 - We added the ability to configure multiple MMFE8s with 8 VMMs each



	SP	SC	SL	ST	SM	SMX	SD	SZ10b	SZ8b	SZ6b
*	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
01	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
02	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
03	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
04	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
05	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
06	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
07	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
08	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
09	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns
10	n	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0 mv	<input type="checkbox"/>	0 ns	<input type="checkbox"/>	0 ns

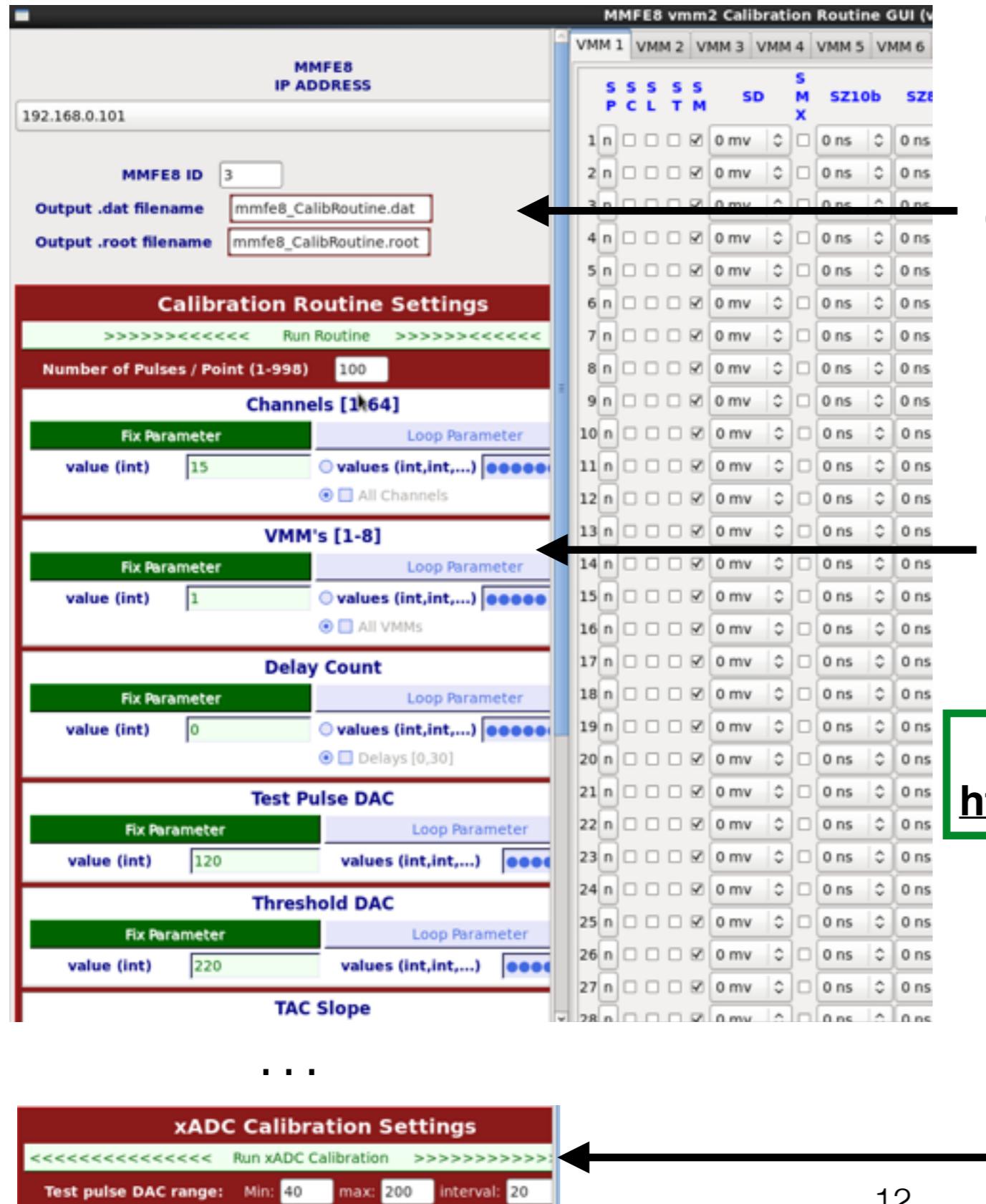
MMFE8 DAQ System

- We prepared a python script to write the MMFE8 data to a file:
 - It checks one board continuously for an FPGA bit set by the external trigger
 - If the bit is high, it reads out FIFO of all 8 boards in sequence through ethernet
 - Firmware allots 100 ms for reading out, which is enough time to read ~50 events per board

MMFE8 Calibration Program

- Based on AZ GUI, Chris developed a python program for the fast calibration of a MMFE8 board
- The program send pulses to each channel selected and reads out data
- has customizable parameters:
 - Peaktime, input DAC value for step pulse, Channels, VMM, Time delay of CKTP with respect to CKBC, # pulses sent
- It can be analyzed with **VMM2_Calibration** package which fits and output TDO, PDO calibration values
- It also collects xADC calibration data, where we use the MMFE8 FPGA ADC to calibrate the input test pulse

MMFE8 Calibration Program

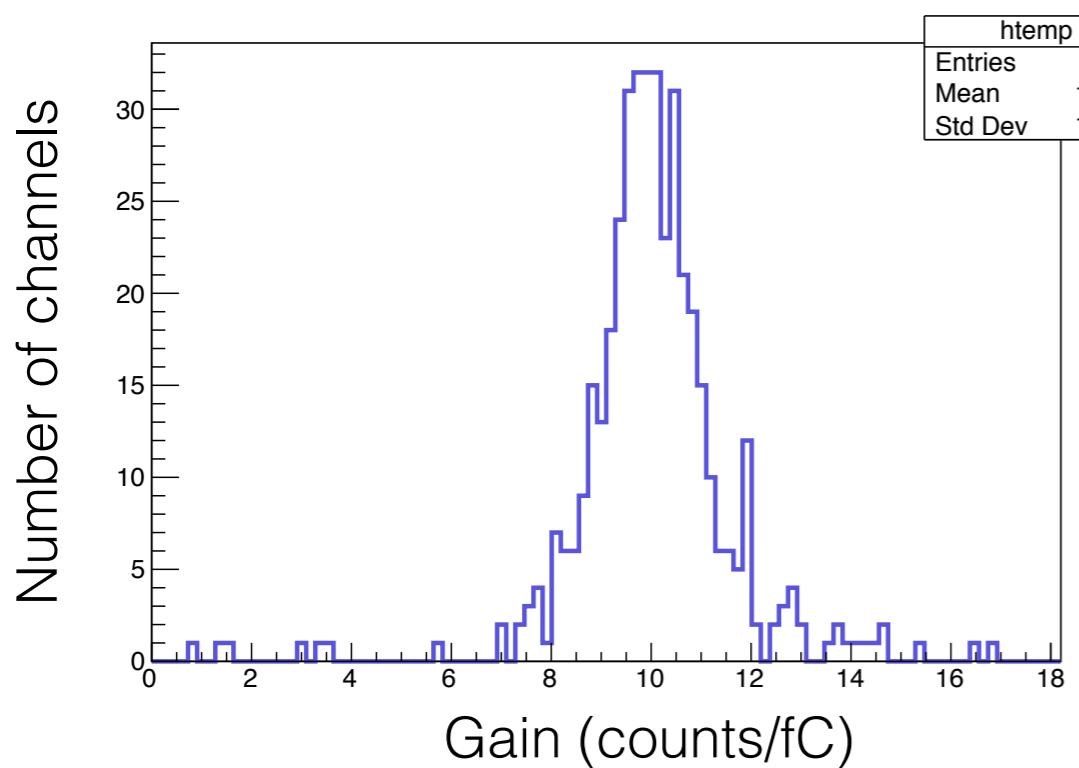


data files: either .dat or .root

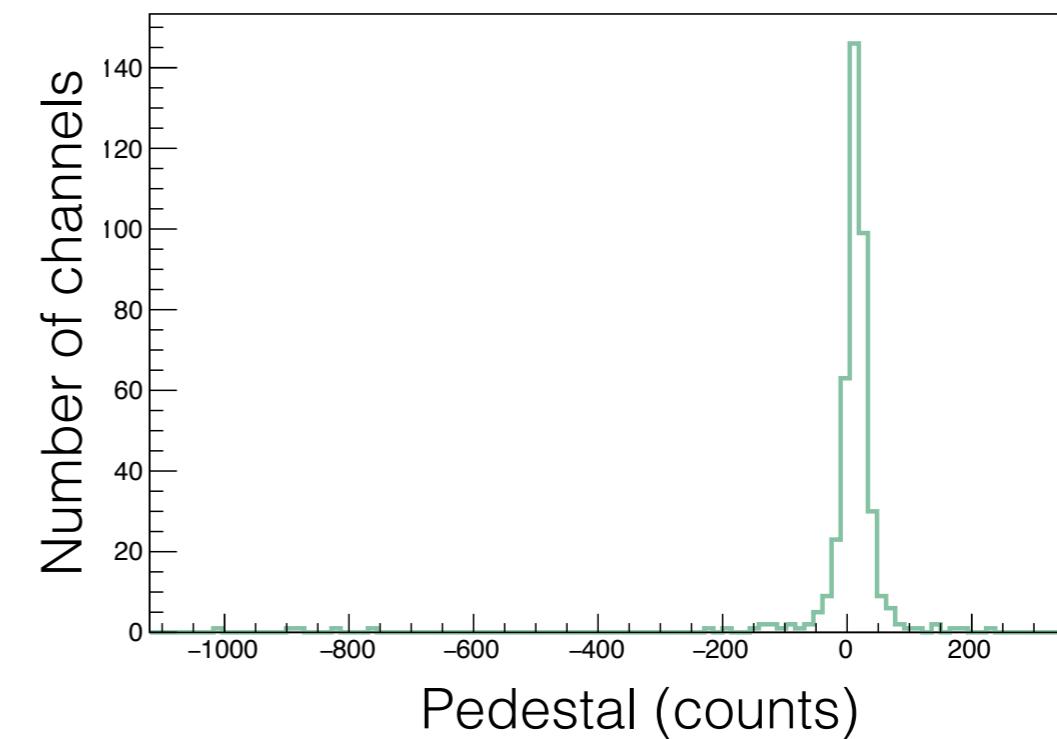
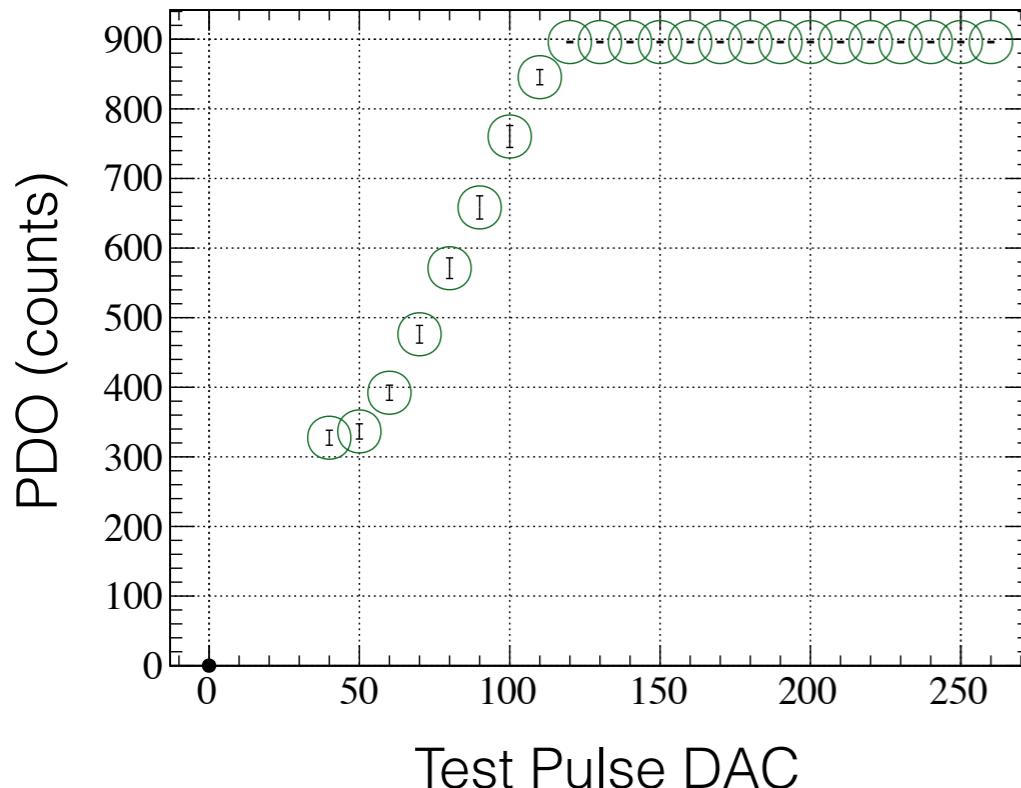
customizable settings

Refer to:
https://github.com/crogan/VMM2_Calibration

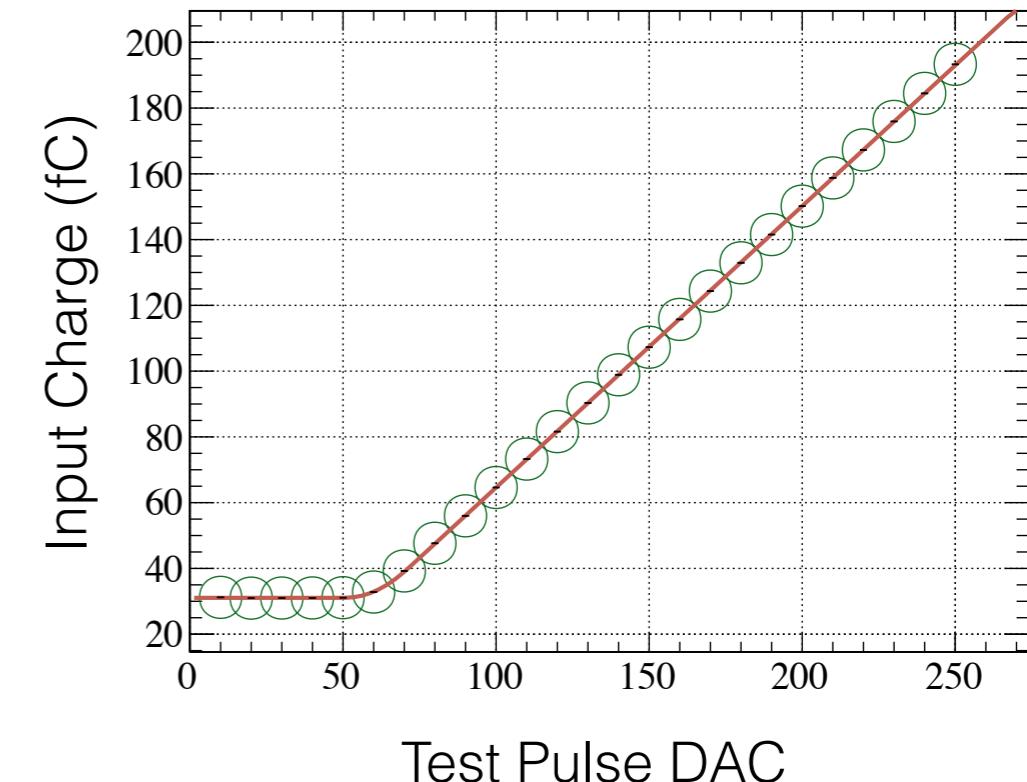
xADC calibration



ATLAS Internal - MMFE8+VMMBoard #102, VMM #0 , CH #12



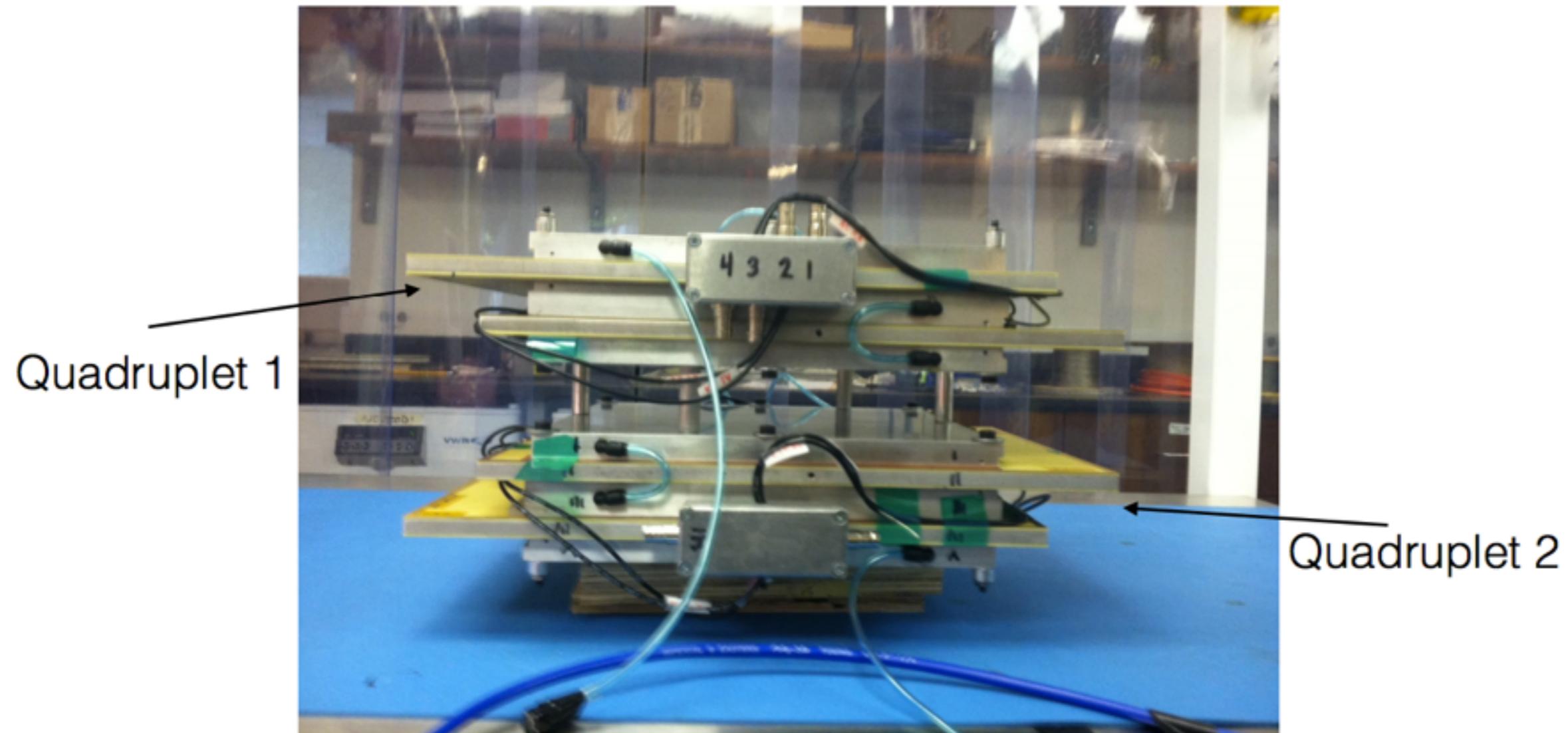
ATLAS Internal - MMFE8+VMMBoard #102, VMM #0



Example calibration plots

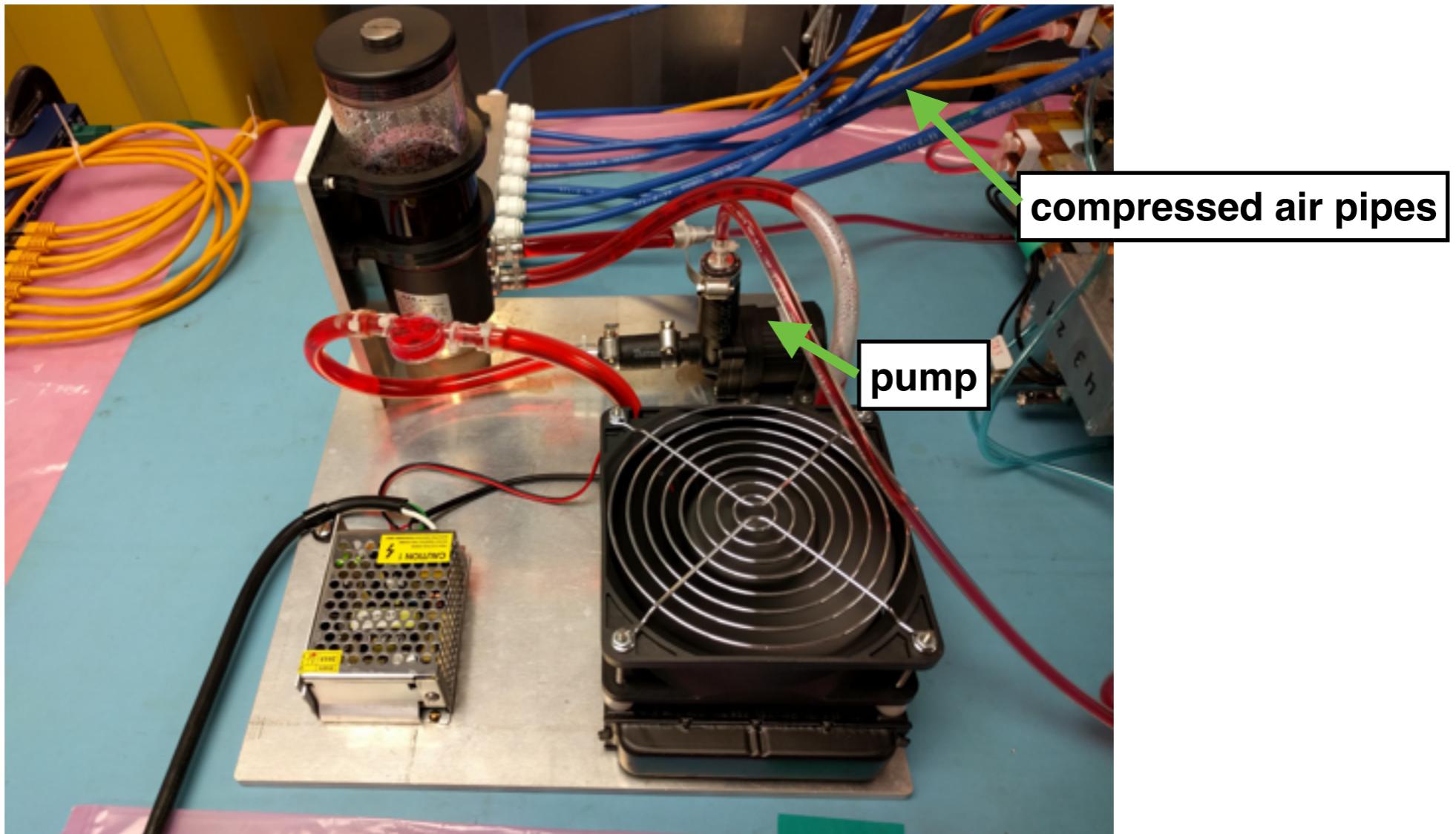
*Will give more details in a future talk

Our Octuplet



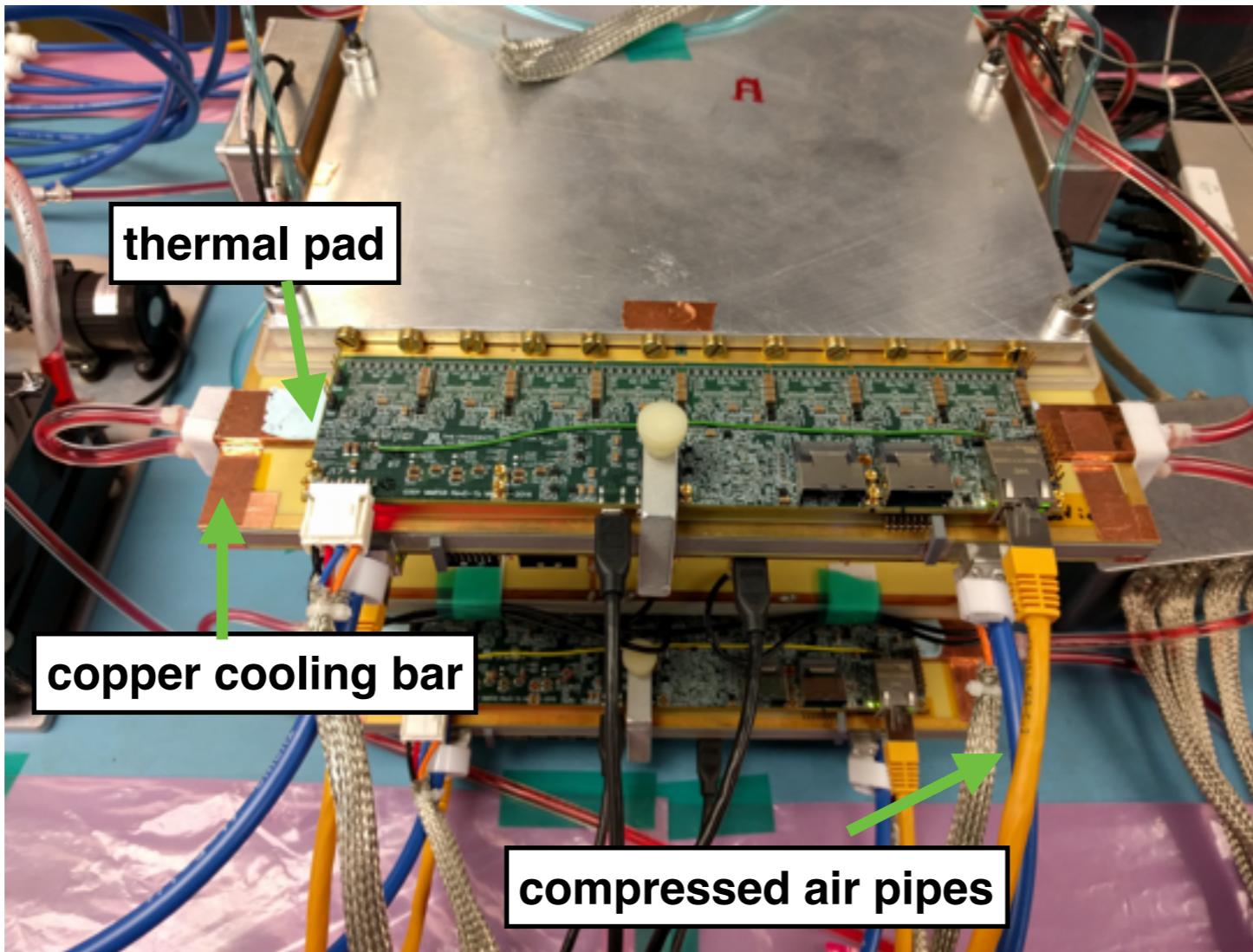
- Bare octuplet
- 20 x 20 cm chambers

Cooling System (v1)



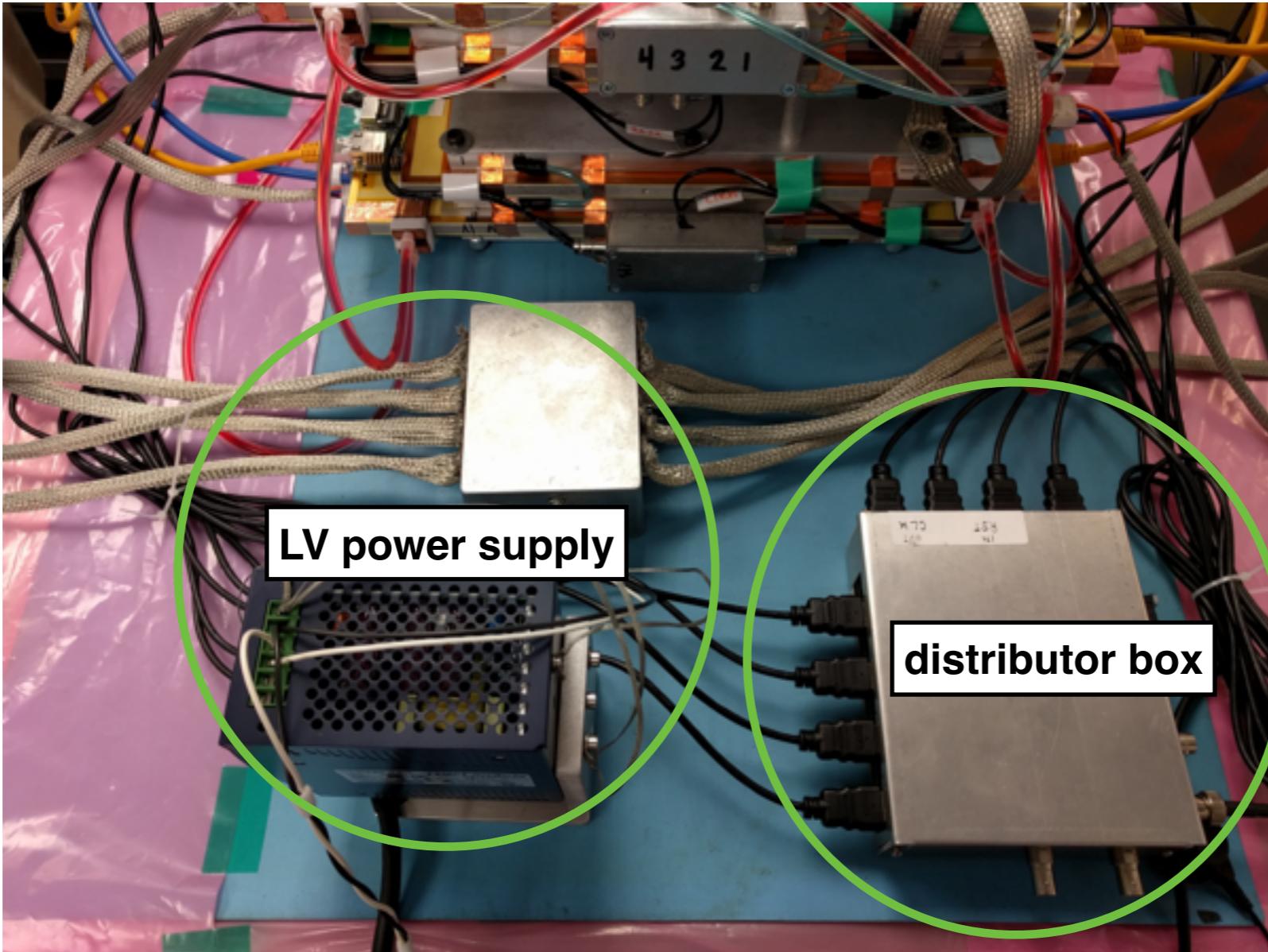
- Liquid cooling system to cool the VMMs
- Coolant is pumped through a 4mm thick copper plate, which is thermally connected to the VMMs through a 1 mm silicone pad (compressible to ~ 0.5 mm), heat dissipated through a fan

Cooling System (v1)



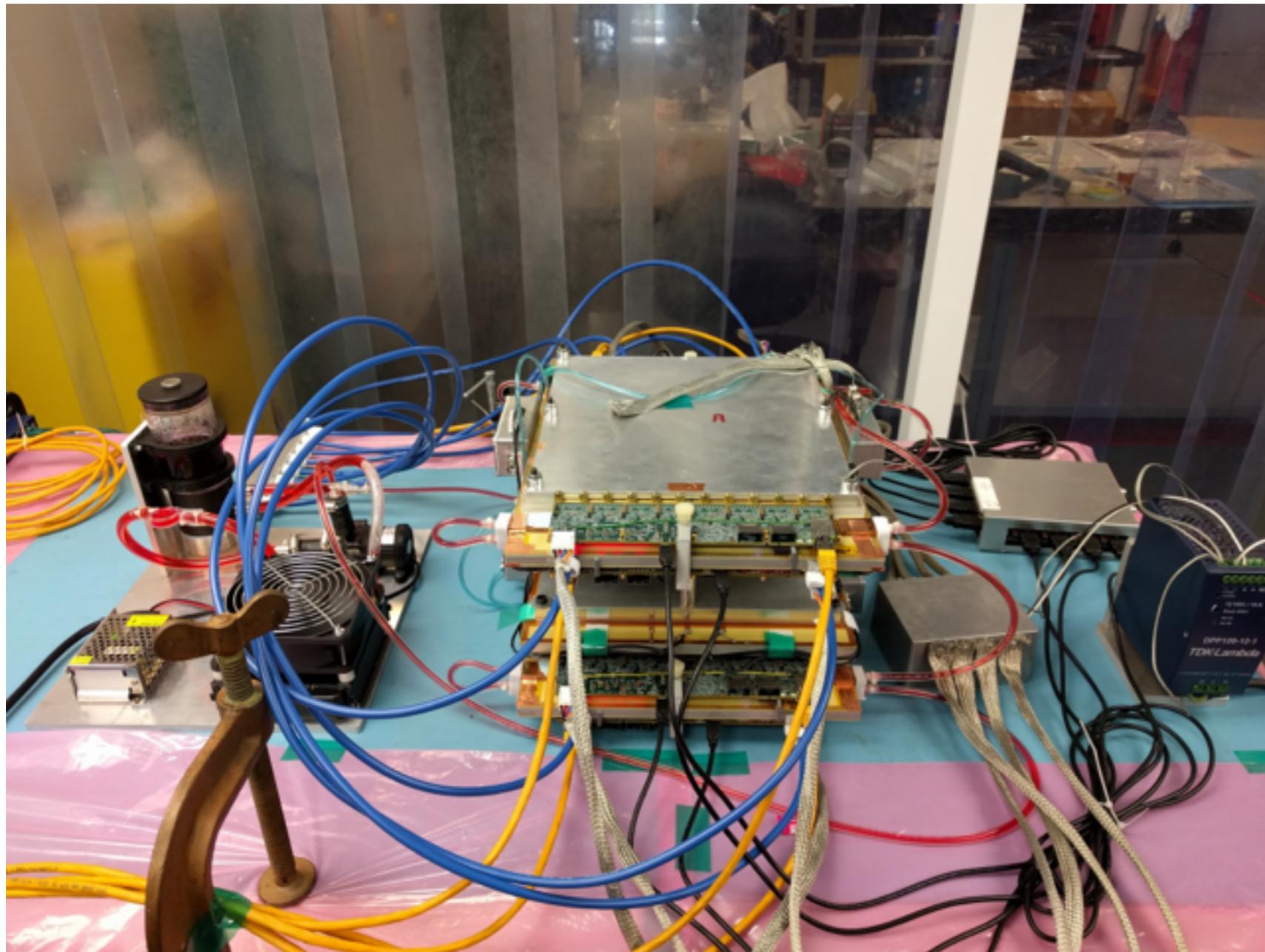
- The heat generated by the DCDC converters isn't well dissipated
- Measured the temperature of the DCDC converter cases to be up to 60 degrees C for a board in the octuplet using a thermistor
- Thus we added compressed air to cool this

Clock and Trigger Signal distributor



- Distributor box (designed by M. Bledsoe & J. Grotto) relays an external trigger signal and a 40 MHz clock to 8 MMFE8 boards through a HDMI → microHDMI cable
- Use J8 HDMI input on MMFE8 board, J7 connects to an FPGA port that isn't suitable for a clock input

Full Octuplet Setup



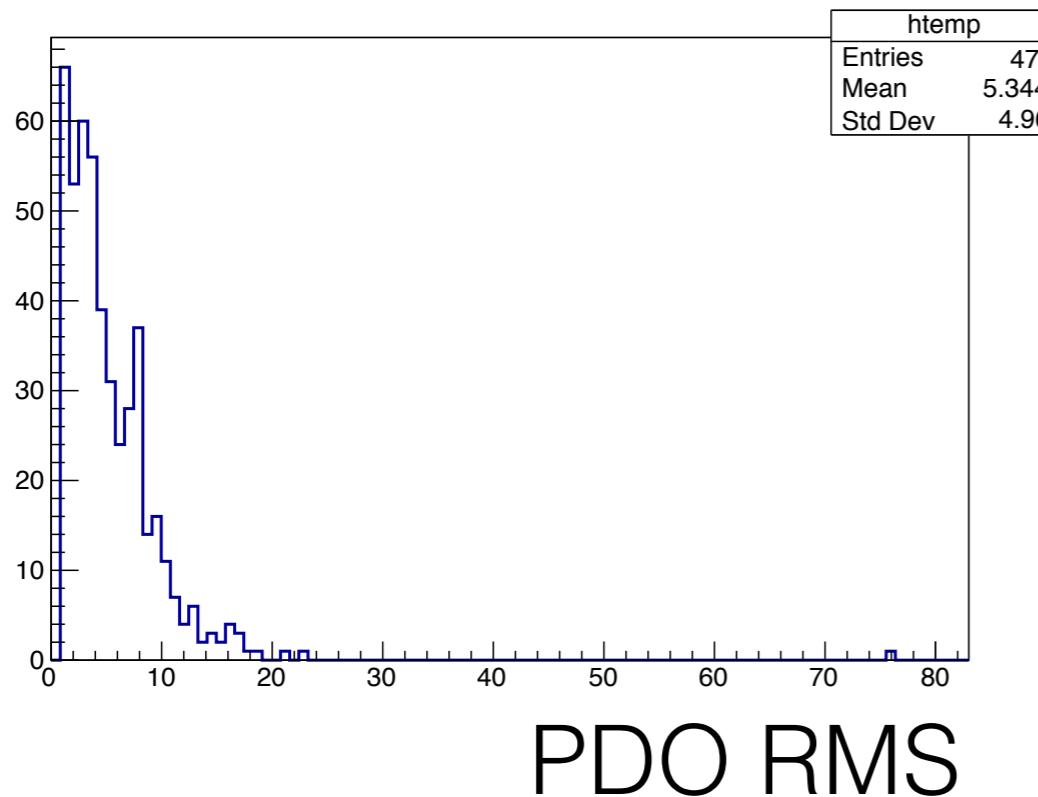
- **blue pipes** = compressed air
- **shielded cables** = LV power supply
- **yellow cords** = ethernet cables

Noise issues - Recap

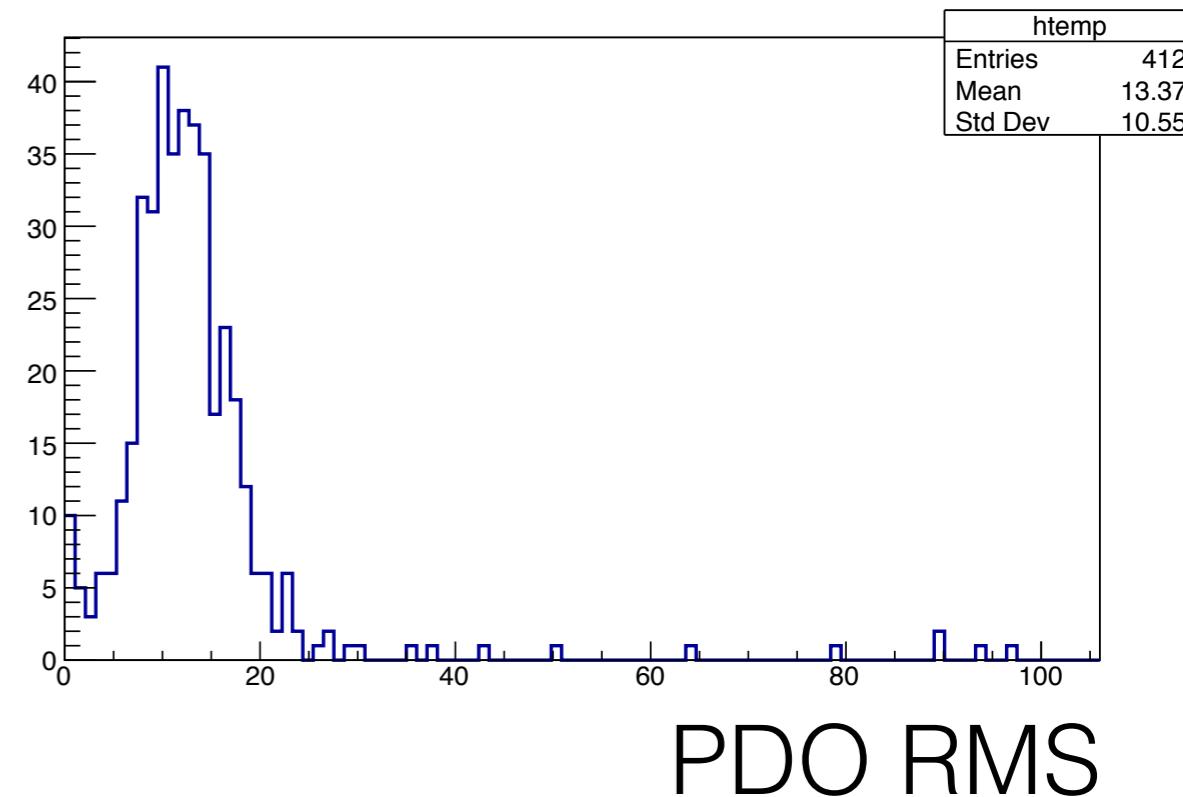
- We have studied noise before, but we have always been working on **small statistics** with poor diagnostics
- With the VMM1 and Mini-1, we studied the boards on the bench and connected to a chamber - noise was negligible in both cases
- Then, G. Iakovidis and S. Jones reported noise when they put a MMFE8 board in the chamber
- We tested a MMFE8 RevC board with 2 working VMMs inside the chamber last year -> we saw noise at first, but after fortifying the zebra holder to improve the zebra contact, it disappeared
- However, we only looked at a **few** channels with 2 VMMs

Noise issues

Example of board with no noise



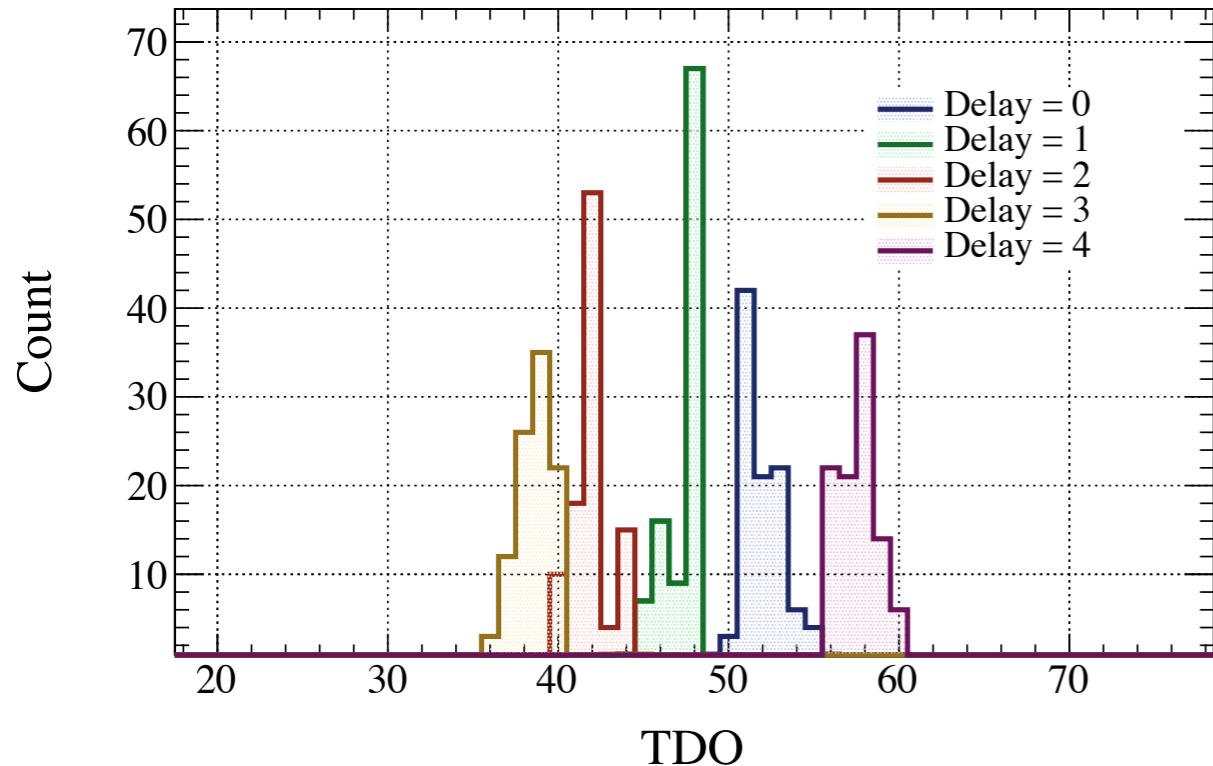
Example of board with noise



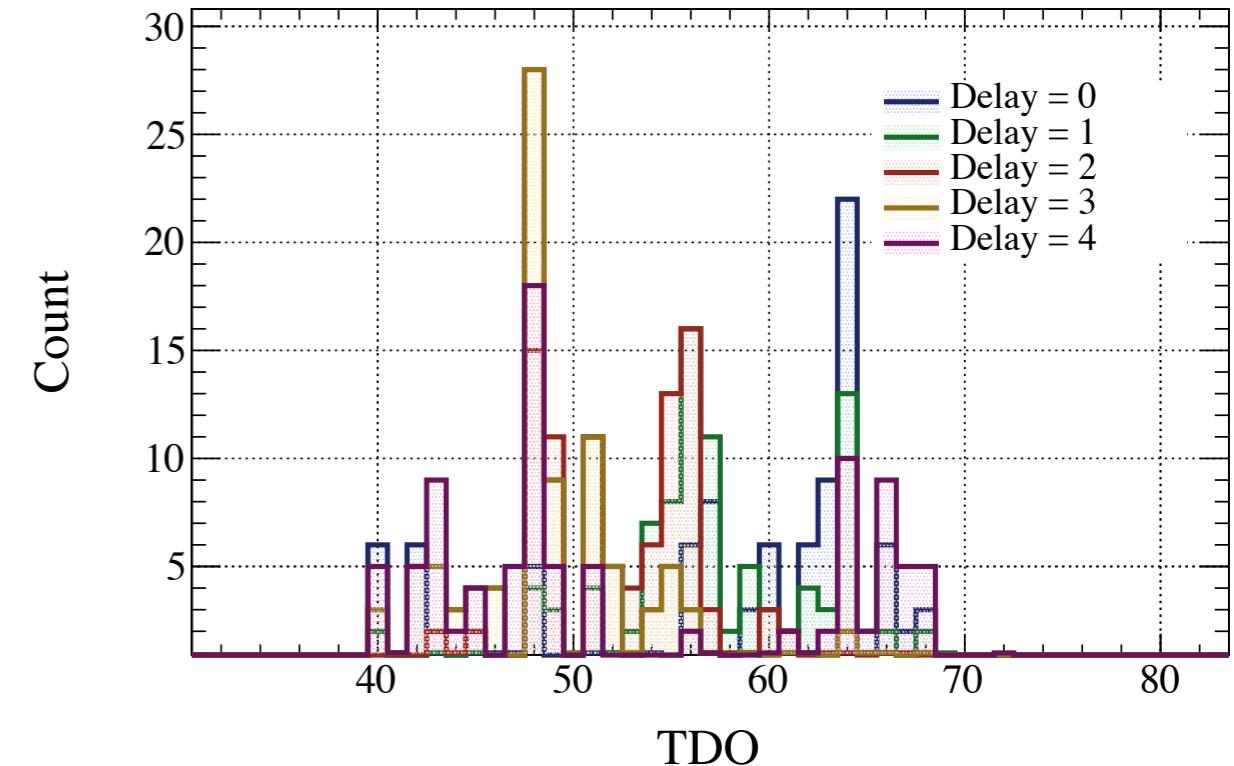
- With a board **on the bench**, there is **no noise** (have looked at 10+ boards)
- As soon as we put in MMFE8 boards into a chamber, we began to notice that the PDO RMS was larger than on the bench - easy to detect because we have high statistics and an automated calibration program

Effect of Noise on TDO

ATLAS Internal - MMFE8+VMM2 Board #105, VMM #4 , CH #22



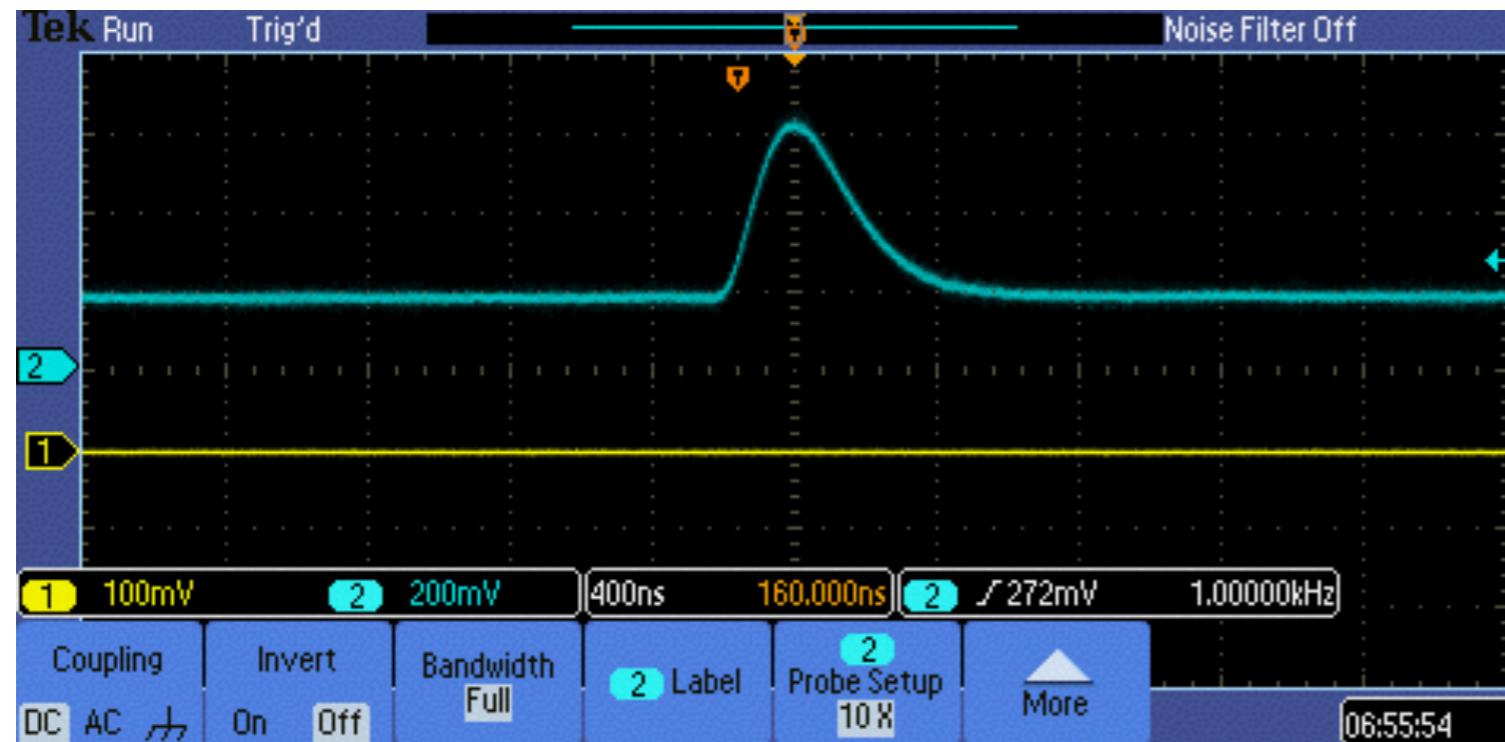
ATLAS Internal - MMFE8+VMM2 Board #105, VMM #4 , CH #31



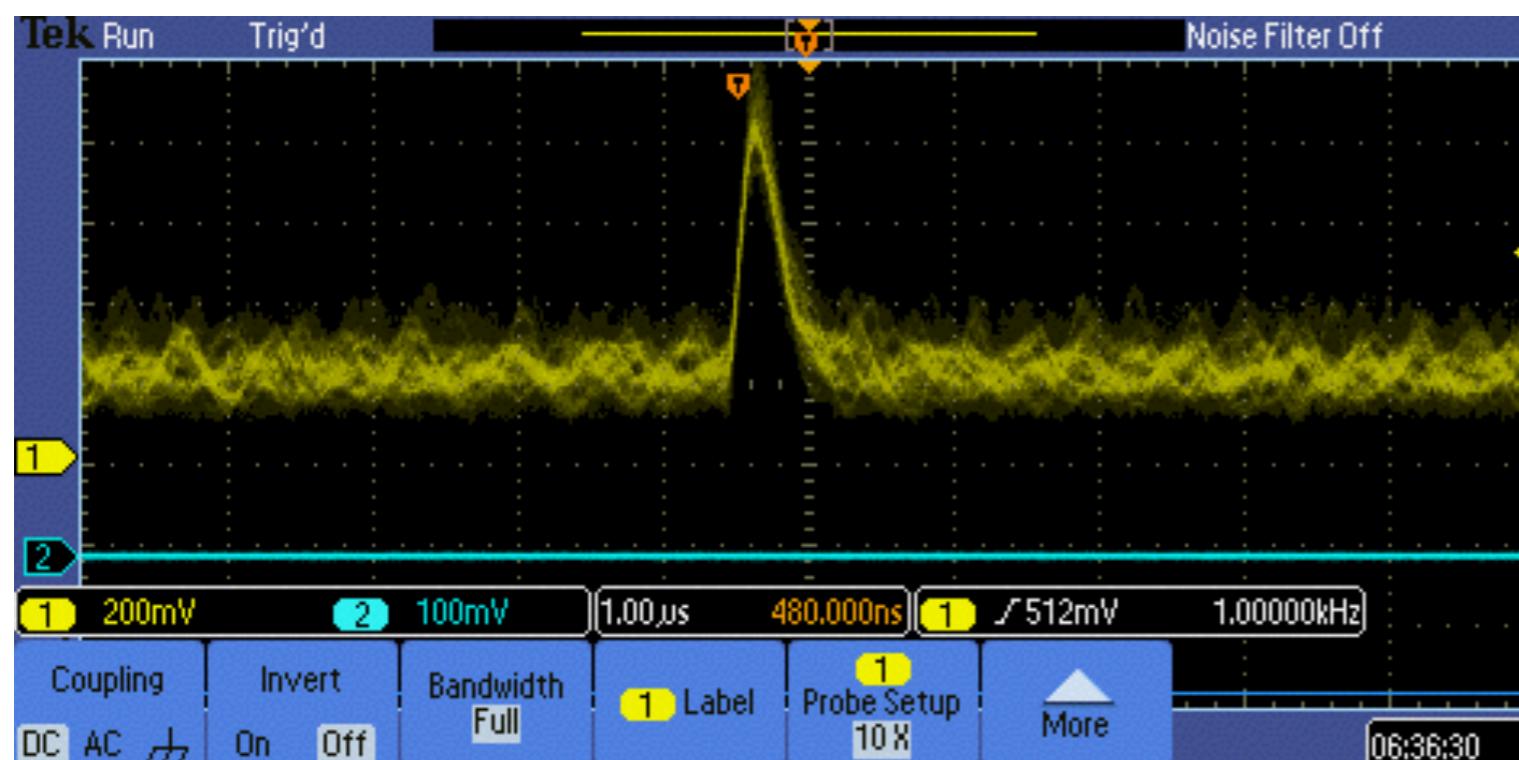
*saturated PDO

- If we try to calibrate the TDO while the MMFE8 boards are in the chambers, we cannot get calibration parameters for many channels
- For these channels, you can't distinguish differences in 25 ns due to the noise, so the TDO information is useless
- Right now, we are running at a high threshold and using only the PDO data

Looking at the test pulse on the monitor output

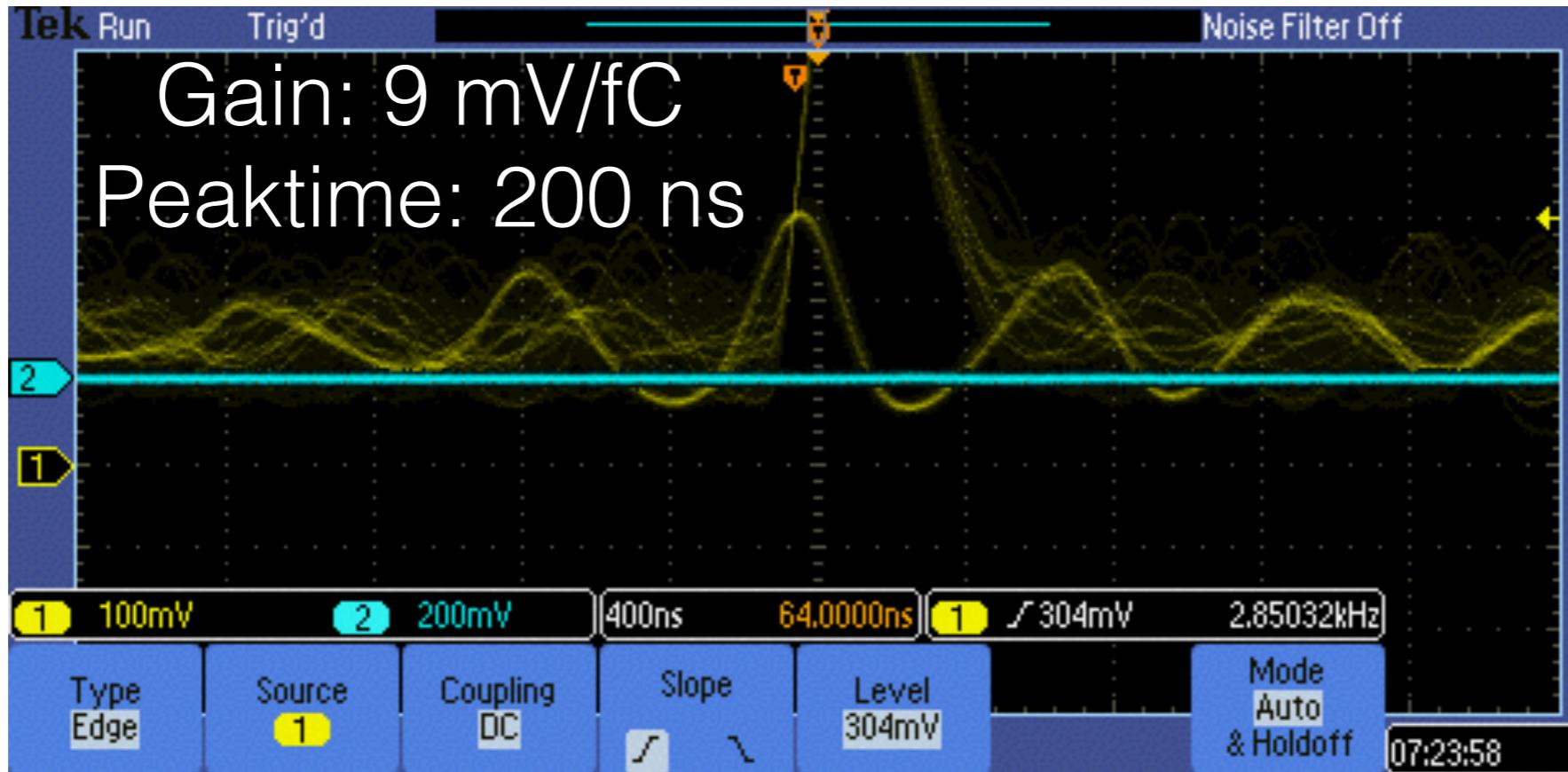


example of a
noiseless channel



example of a noisy
channel

Expanded view of the noise



- We see up to ~ 200 mV of noise above the pedestal
- The main frequency is at **~1.2 MHz**, and the amplitude varies with the VMM gain and peaktim
- Looking at other signals such as the threshold or the step pulse on the monitor output, these signals do not exhibit this noise
- Not all VMMs in a board are noisy, and not all channels in a VMM are noisy. Often a noisy channel neighbors a noiseless channel
- Thus the noise is not on the board, it is an oscillation at the VMM input
- Overall noise level **increases** when we add more MMFE8 boards to the octuplet

Noise issues

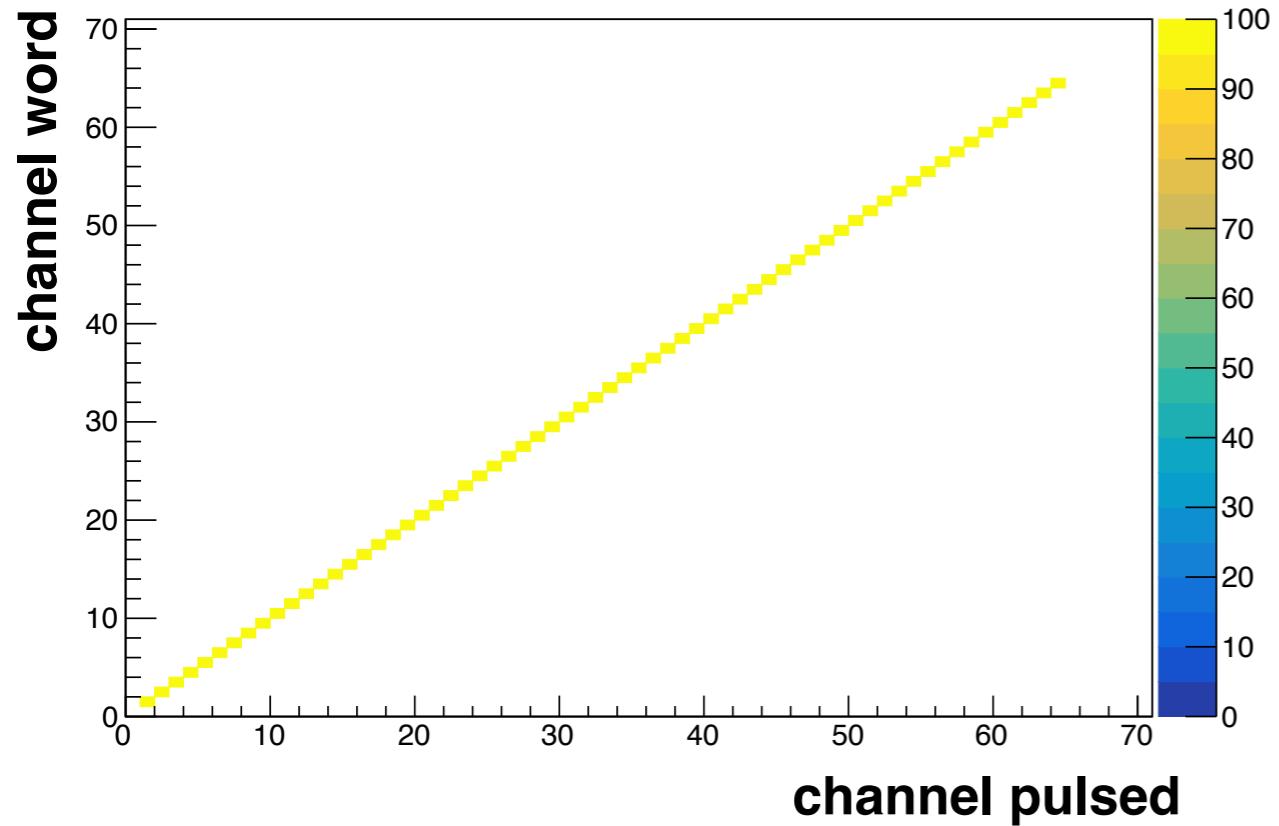
- Other facts:
 - We used a special board to connect a 142C ORTEC charge amplifier to a zebra connector (256 strips) -> in this case, we did not see this type of noise, which excludes most mundane causes of noise
 - We thought the oscillation was induced by the DCDC converters because they operate at a 1.2 MHz frequency and have a large 100-300 mV ripple. We also noticed that the noisiest VMMs are usually the two closest to the DCDC converter (0 and 1)
 - Arizona modified a board for us with reduced ripple and a lower frequency of operation (~500 kHz)
 - This board has the same level of noise and the frequency **is still** 1.2 MHz

Noise issues

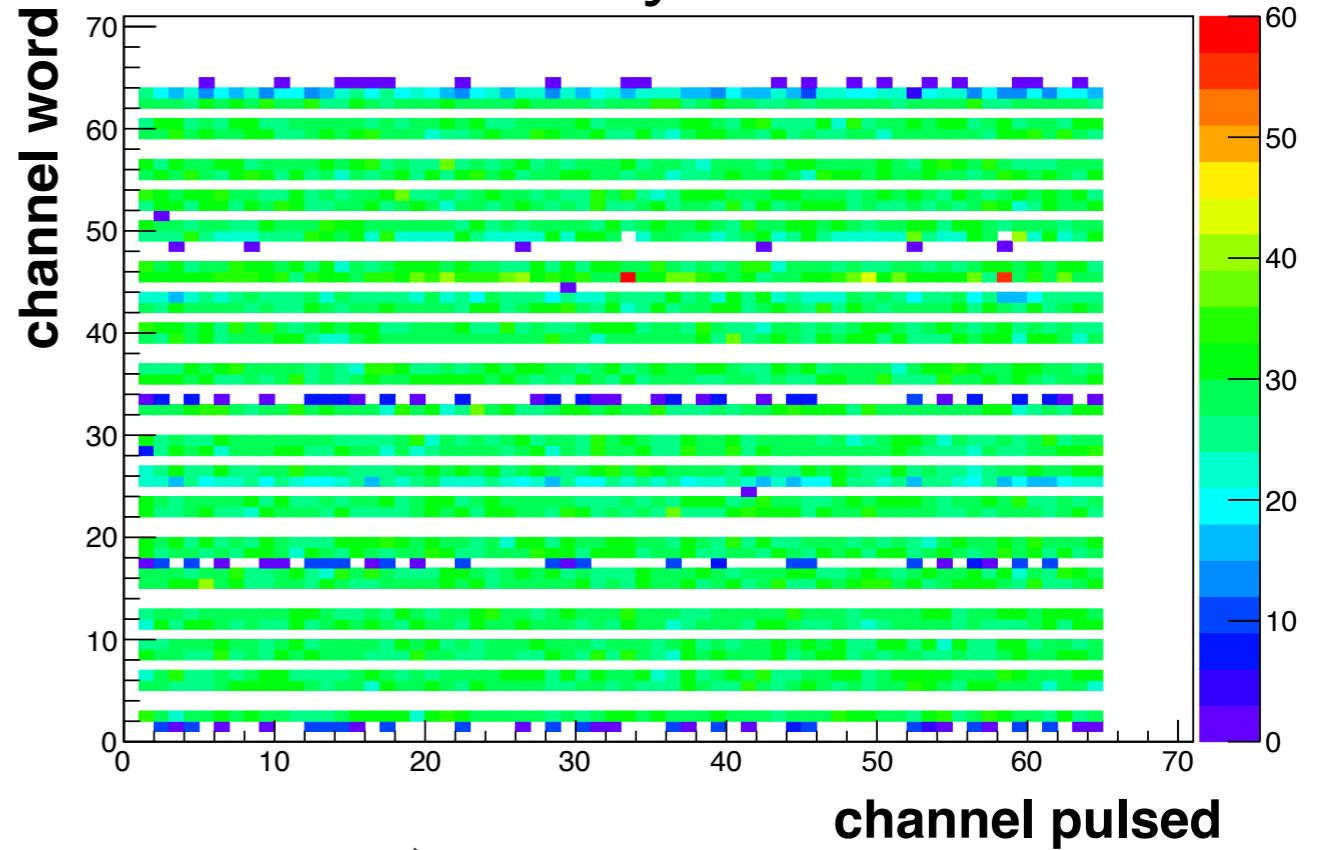
- Other facts (continued):
 - The analog ground, digital ground, and power supply ground of the MMFE8 board are all the same (they were supposed to be separated)
 - When pressing the board on the zebra with the cams, the MMFE8 ground is connected to the octuplet cage, which in turn is connected to the chamber mesh and the HV ground
 - In this situation we don't know which ground is returning which current
 - For example, we measured the difference between the ground of the power supply and the ground of each MMFE8 board
 - There is a relative ~10-15 mV increase in voltage going from the top to the bottom board of the octuplet, which means that the 12 V power supply current sent to a board is returned by other boards through the cams and the aluminum frame

Noise issues

noiseless VMM



noisy VMM



- The upper right plot shows that a pair of noisy channels on a VMM alternate with a pair of adjacent noiseless channels
- Consecutive pairs of VMM inputs lie on opposite sides of a board
- We look forward to verification of our results

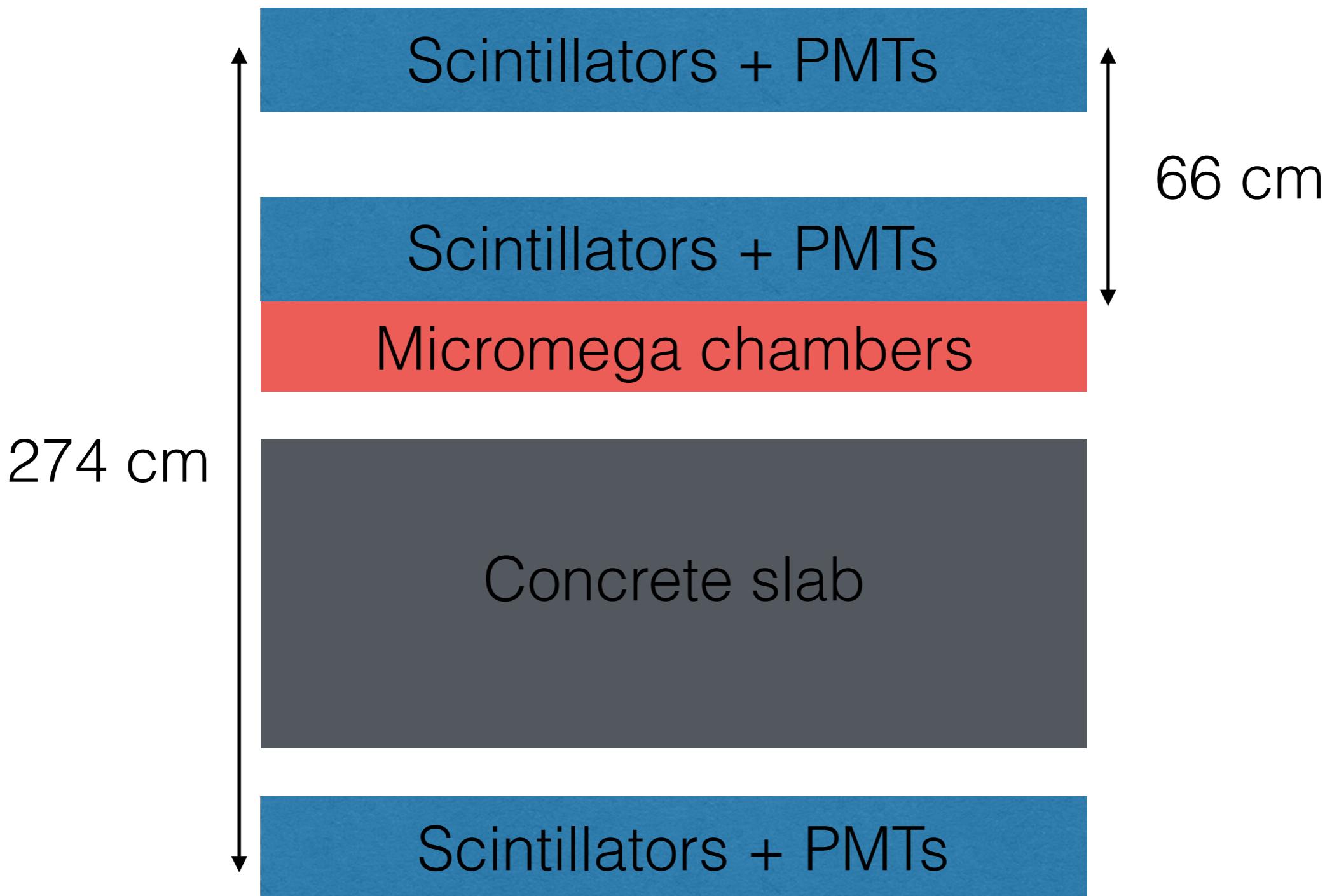
Here, it is so noisy that we don't get any data from the channel being pulsed, the FIFO is filled by noisy channels.

Move to 38 Oxford



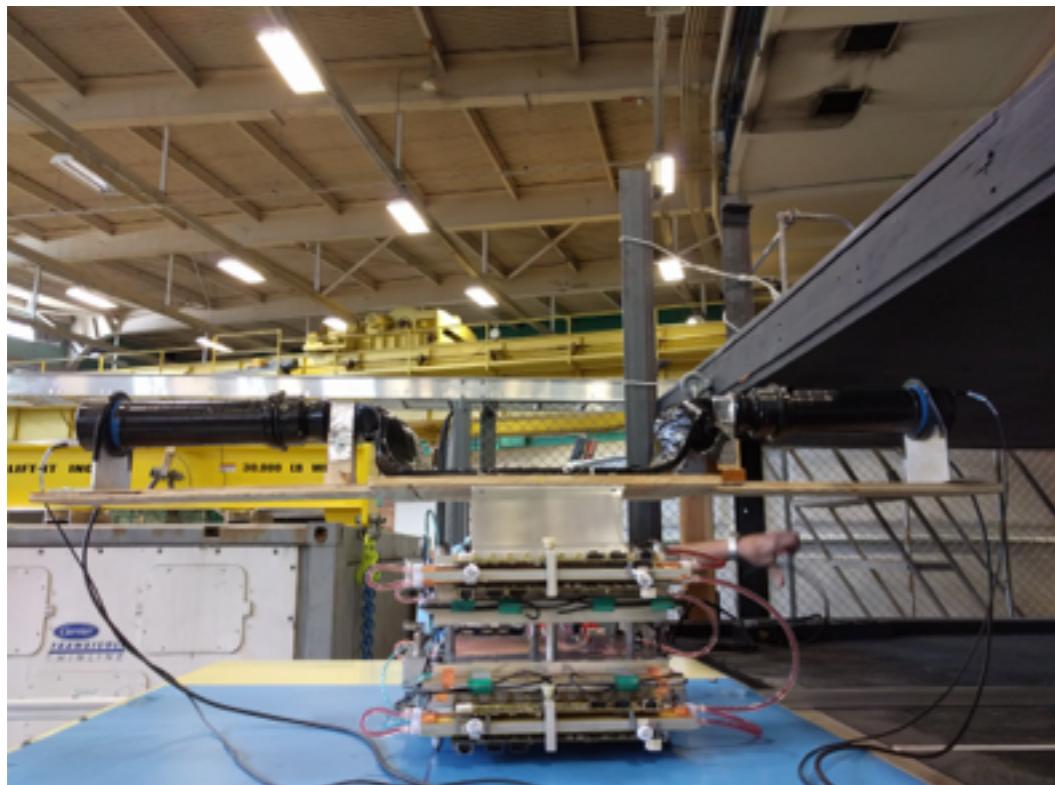
- After assembling, we moved the whole system to the cosmic ray test stand

Cosmic ray test stand setup



- Maximum angle of muon track: -13 to 23 degrees

Cosmic ray test stand setup



High Voltage Issues

- When we studied the noise on a **MMFE8 RevC board with 2 VMMs** last year, we lost a VMM to HV. We paid no attention because that board lost 5 VMMs in a week just sitting on the bench
- We also tested a **MMFE8 RevC board with 8 VMMs** with HV on the chamber and we didn't notice any channels/VMMs dying, but we did not do a systematic check of all the channels
- After we turned on high voltage for the first time on the **octuplet**, we lost a large number of channels on several **RevD cards**, around ~1000 channels in ~4000!

High Voltage Issues

- After these channels died, we took a closer look the worst affected board
- Input impedance of killed channels is about $200\ \Omega$, the impedance of healthy channels is $\sim 500\ k\Omega$
- To understand whether we zapped the protection diode or the VMM input FET, we took out two VMMs and measured the impedance of the protection diodes
- We found that diodes were not broken. When testing the diodes, we discovered (our ignorance) that they clamp the voltage to 8.5-9.5 V, and many do not clamp the voltage at all
- According to Gianluigi, the SOA of the VMM FET is 2 V DC, but a transient of 1.6 V for 20 s can seriously damage the FET (ballpark estimate and the SOA must have a distribution)

High Voltage Issues

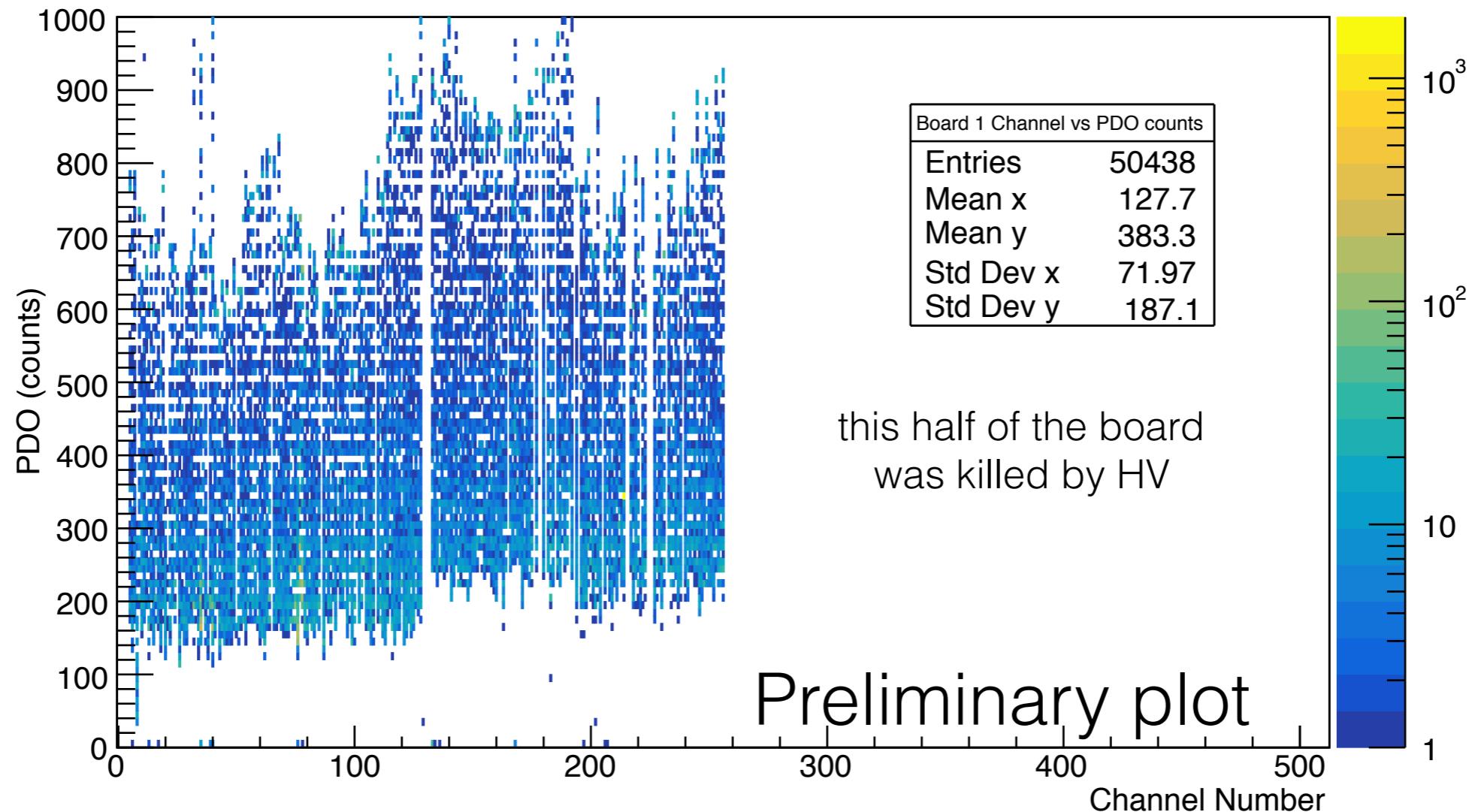
- Based on this information, we performed a number of controlled experiments using the **surviving boards**
- We ramped with various different speeds between 5 V/s and 100 V/s over several days and scanned the channels each time
- We only saw 3 more channels die, this happened first three times we ramped up and down using 5 V/s
- While we ramped up the voltage, we looked at the test pulse on the monitor output. During ramps at > 10 V/s, **test pulse disappears**

High Voltage Issues

- We also measured the voltage on top of the zebras during ramping, which was about 2 V for a HV ramping speed of 50 V/s
- We replaced the killed boards with three new boards (2 RevC, 1 RevD). Ramping up @ 25 V/s, we lost ~ 10 channels on these three boards
- Conclusion: The VMM input is not protected enough, ramping zaps the FETs which are at the tail of the SOA distribution. It remains a mystery why we lost so many channels in four boards, while in the other boards we just lost a few channels

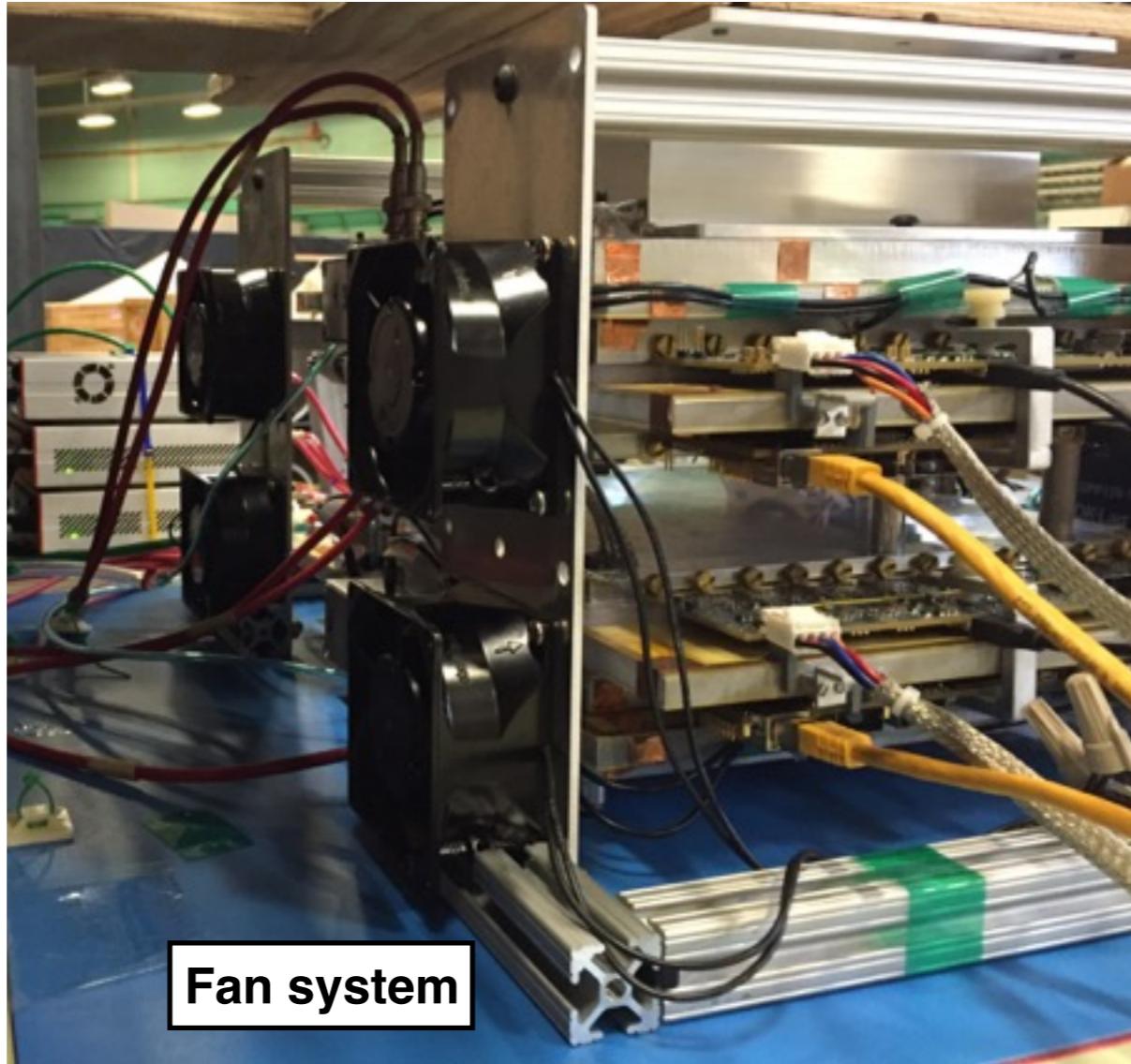
Preliminary data taking

Board 1 Channel vs PDO counts



- We managed to take a small data run of ~80,000 events with the damaged boards, with 7 MMFE8 boards in total
- Drift Voltage = -250 V, Resistive strips = +540 V

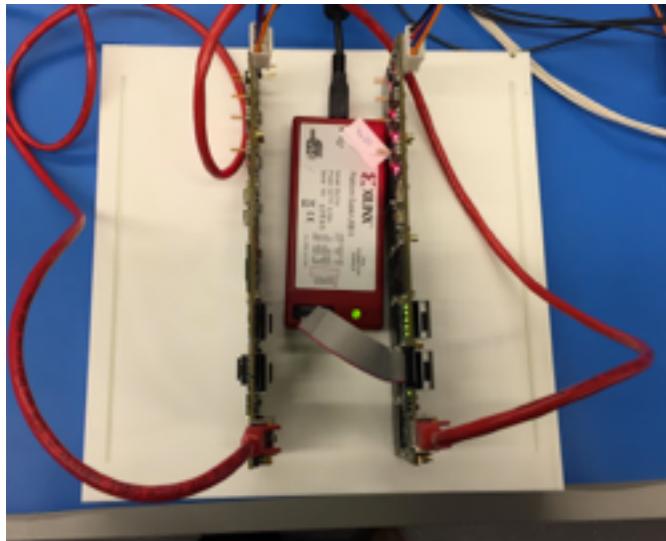
Current status



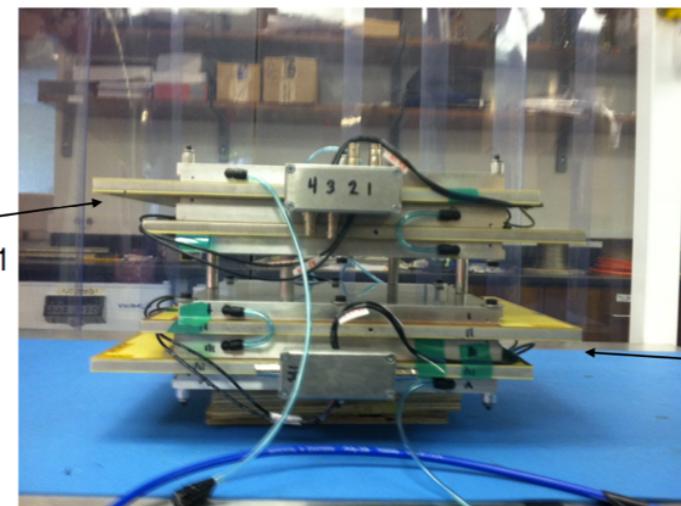
- After replacing so many boards, the liquid cooling system started leaking, so we replaced it with a series of large fans

Conclusion

MMFE8s



MM Octuplet



Trigger Processor



- We have an integrated setup of MMFE8 boards and the MM octuplet with the cosmic ray test stand, seems to be running smoothly now :)
- We will take ~ 1 million events with 8 boards and analyze the data
- Then, we will bring in the ADDC and the trigger processor to test the trigger system

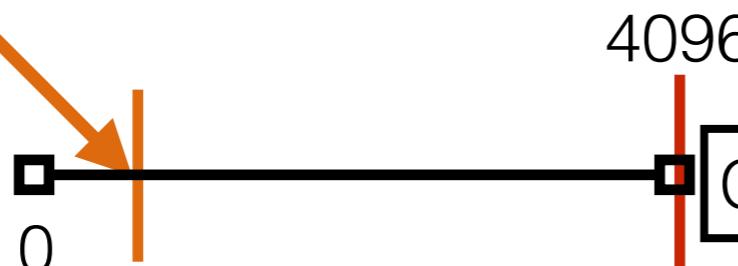
Backup

Miscellaneous mechanical issues

- Miscellaneous lessons from the assembly:
 - >1 ethernet connector broke off, they are weakly attached so we now glue all of them onto the board to reinforce them
 - Our liquid cooling system began to leak, was very fragile in design but we learned some general lessons:
 - Some capacitors on the board are higher than the VMM chip, which resulted in the board having an angle when pushed down on the copper plate
 - Removing the card connected to the copper plate required a significant amount of force and was difficult on the cosmic test stand platform
 - Moving the card also results in small pieces of the silicone pad breaking off and sometimes getting into the zebra area

VMM Synchronization

Ext Trig



- (1) Stop CKBC, inhibit Ext Trig, enable CKTK
- (2) Wait Δt to drain VMM FIFOs
- (3) Set reg signaling that trigger happened, wait 100 ms for data readout
- (4) Soft Reset, disable CKTK
- (5) Start CKBC, allow Ext Trig

(1) External Trigger

microblaze

reg

if 1 then GUI
pulls data
from FPGA

GUI

2 counters
+ FIFO content

- (1) Stop CKBC
- (2) Soft Reset
- (3) Start CKBC

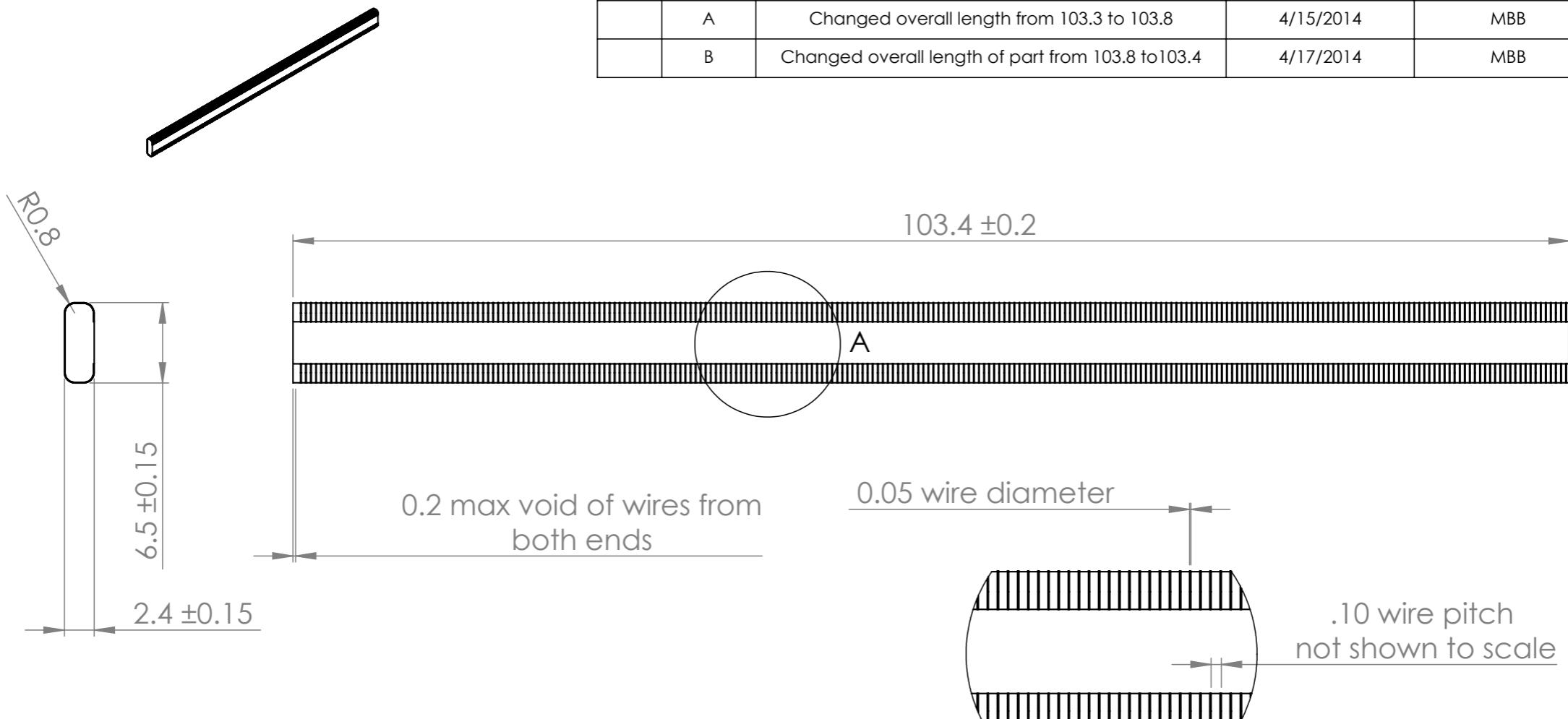
4096

Counter A

(2) No External Trigger

Zebra Connector Specifications

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	Changed overall length from 103.3 to 103.8	4/15/2014	MBB
	B	Changed overall length of part from 103.8 to 103.4	4/17/2014	MBB



Notes:

Core Material:
Zsil-1

Conductors:
Material C2
Plating Z5

Substrate:
11L

Z-Axis Connector Co.
345 Ivyland Rd. Warminster PA 18974
267-803-9000

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UNLESS OTHERWISE SPECIFIED:

DIMENSIONS ARE IN mm
TOLERANCES:
FRACTIONAL \pm n/a
ANGULAR: MACH ± 1 BEND ± 1
TWO PLACE DECIMAL $\pm .25$
THREE PLACE DECIMAL $\pm .127$

INTERPRET GEOMETRIC
TOLERANCING PER:

MATERIAL see note

FINISH

DO NOT SCALE DRAWING

DETAIL A

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TITLE:

Elastomeric Connector

SIZE	DWG. NO.	REV
A	Zwrap-314	B
SCALE: 1:2	WEIGHT:	SHEET 1 OF 1