VMM2 (ic134)

rev. 16, 4/21/2015

Updated information on power dissipation

Architecture and Functionality

Fig. 1 shows the architecture VMM2, which is an evolution of VMM1 [1], but with a much higher complexity and functionality as described in the following paragraphs. The step-up can be appreciated from the increase in layout size (from 5.9×8.4 mm² to 13.5×8.4 mm²) and transistor count (from ~ 500k to ~ 5 million).

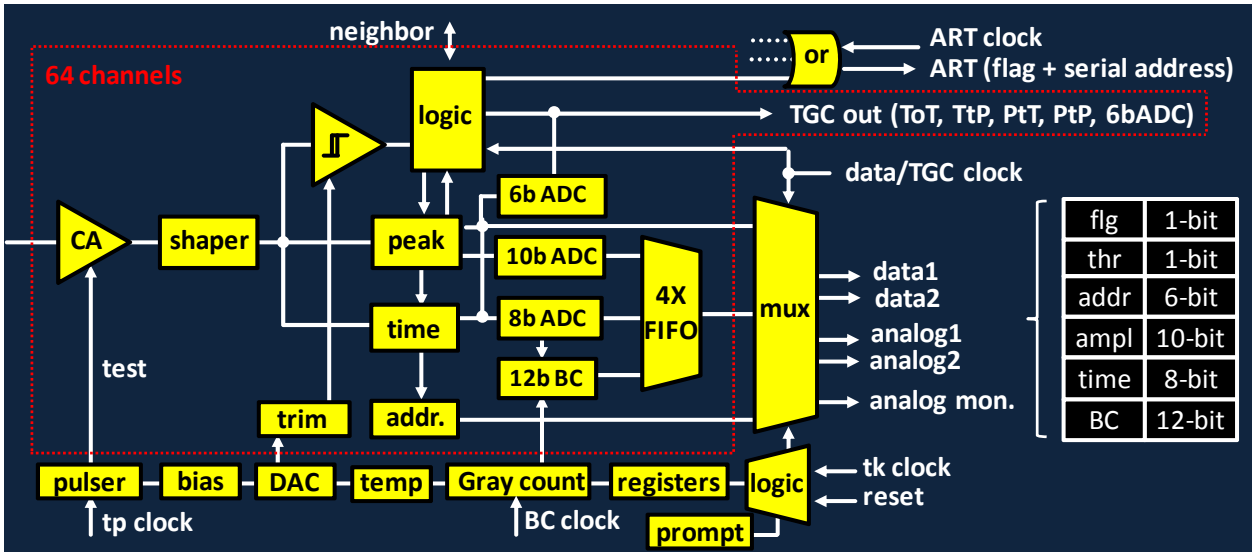


Fig. 1 – Architecture of VMM2

VMM2 is composed of 64 linear front-end channels with inputs at pins *i0* through *i63*. Each channel integrates a low-noise charge amplifier (CA) with adaptive feedback, test capacitor (enabled with channel bit *st*) and adjustable polarity (to process either positive or negative charge, set with global bit *spg* and channel bit *sp*), optimized for a capacitance of 200pF and a peaking time of 25 ns. The input MOSFET is a p-channel with gate area L x W = 180 nm x 10 mm (200 fingers, 50 µm each) biased at a drain current I_D = 2 mA; this corresponds to an inversion coefficient IC ≈ 0.22, a transconductance g_m ≈ 50 mS, and a gate capacitance C_g ≈ 11 pF. The filter (shaper) is a third-order designed in delayed dissipative feedback (DDF) [2], has adjustable peaking time in four values (25, 50, 100, and 200 ns) and stabilized band-gap referenced baseline. The DDF architecture offers higher analog dynamic ranges, making possible a relatively high resolution at input capacitance much smaller than 200 pF. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).

Next to the shaper are the sub-hysteresis discriminator [1] with neighboring and trimming, the peak detector and the time detector. The sub-hysteresis function, enabled with the bit *ssh*, allows discrimination of pulses smaller than the hysteresis of the comparator circuit. The threshold is adjusted with the global DAC bits *sdp0:sdp9* and the channel DAC trimming bits *sd0:sd3*. The neighboring function, enabled with the bit *sng*, forces the measurements of channels neighbor to a triggered one,

even if the channel belongs to a neighbor chip. The inter-chip communication occurs through the bi-directional pins *sett* and *setb*. The peak detector measures the peak amplitude and stores it in an analog memory. The time detector measures the peak timing using a time-to-amplitude converter (TAC), i.e. a voltage ramp that starts at the time of the peak and stops either when *ena* is lowered or at a clock cycle of the BC clock, depending on the mode of operation as described below. The TAC value is stored in an analog memory and the ramp duration is adjustable in four values (125ns 250ns 500ns, 1µs). The peak and time detectors are followed by a set of three low-power ADCs (a 6-bit, a 10-bit, and a 8-bit), characterized by a domino architecture [3] but of new concept. These ADC are enabled depending on the selected mode of operation.

The ASIC can operate in three modes: *direct-outputs* (bit *sttt* high and either bit *spdc* low or bit *spdc* high and bit *s6b* high), *two-phase* or *analog* (bit *spdc* low, bit *sttt* low) and *continuous* or *digital* (bit *spdc* high, bit *sttt* low, bit *s6b* low). Note: due to reset conflicts, VMM2 cannot operate the direct-outputs when in continuous mode. This feature will be integrated in the next version VMM3.

In *direct-output* mode the 64 channel digital outputs *ttp* are activated and provide one of four different timing pulses: time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold (PtT), or a 10ns pulse occurring at peak (PtP), and can be set using the global bits *stot* and *stpp*. The channel self resets at the end of the timing pulse, thus providing continuous and independent operation of all 64 channels. Alternatively, if the bits *spdc* and *s6b* are both set high, the peak detector converts the voltage into a current that is routed to the 6-bit ADC. The 6-bit ADC provides a low-resolution A/D conversion of the peak amplitude in a conversion time of about 25 ns from the peak time. The conversion time and the baseline (zeroing) are adjustable using the global bit set *sc6b* (the conversion time is the number of data clocks set by the *sc6b* bits) and the channel bit set *sz6b* respectively. The serialized 6-bit data is made available at the channel output immediately after an event flag which occurs at the peak time. The flag is lowered at the next clock cycle of the data clock, and the 6-bit ADC data is shifted out after that, either at each clock cycle or at each clock edge of the data clock depending on the global bit *sdck6b*. The channel reset occurs after the last bit has been shifted out.

In *two-phase* (*analog*) mode, which is the mode originally implemented in VMM1, the ASIC operates in two separate phases: acquisition with *ena* high and readout with *ena* low. During the acquisition phase the events are processed and stored in the analog memories of the peak and time detectors. As soon as a first event is processed, a flag is raised at the digital output *data0*. Once the acquisition is complete the ASIC can be switched to the readout phase and the readout proceeds injecting a token at the token input *tki*. The first set of amplitude and time voltages is made available at the analog outputs *pdo* and *tdo*. Analog buffers can be enabled using the bits *sbfp* and *sbft*. The address of the channel is serialized and made available at the output *data0* using six data clocks. The next channel is read out by advancing the token with the token clock. The token is sparse, passed only among those channels with valid events. If, after the token clock occurs, the data0 gets low, the readout is complete and the token is routed to the output tko for the readout of the next chip. This allows daisy-chain readout with a single token input.

In *continuous* (*digital*) mode (bit *spdc* high, bit *sttt* low, bit *s6b* low) the peak and time detectors convert the voltages into currents that are routed to the 10-bit ADC and 8-bit ADC respectively. The 10-bit ADC provides a higher resolution A/D conversion of the peak amplitude in a conversion time of about 200 ns from the occurrence of the peak. The conversion time and baseline (zeroing) are adjustable using the global bit set *sc10b* (the conversion time is a ~200ns base plus a 60 ns increment for the MSB and LSB phases, set by the *sc10b* bits) and the channel bit set *sz10b* respectively. The 8-bit ADC provides the

A/D conversion of the peak timing (measured using the TAC) from the time of the peak to a stop signal. The bit *s8b* allows using two different conversion modes which will be described elsewhere. The TAC stop signal occurs at a next clock cycle of a shared 12-bit Gray-code counter which is incremented using the external clock signal BC. The counter value at the TAC stop time is latched into a local 12-bit memory, thus providing a total of 20-bit deep timestamp with a nanosecond resolution. The conversion time and baseline (zeroing) are adjustable using the global bit set *sc8b* (the conversion time is a ~100ns base plus a 60 ns increment for the MSB and LSB phases, set by the *sc8b* bits) and the channel bit set *sz8b* respectively. The channel is reset once both the 8-bit and 10-bit conversions are complete and the digital values are latched in digital memories.

Thus, in *continuous* (*digital*) mode a total of 38 bits are generated for each event. The first bit is used as a readout flag, the second is the threshold crossing indicator (allows discrimination between above-threshold and neighbor events). Next is a 6 bits word for the channel address, followed by 10 bits associated with the peak amplitude, and 20 bits associated with the timing. The 38-bit word is stored in a 4-events deep derandomizing FIFO (there is one such FIFO per channel) and it is read out using a token-passing scheme where the token is passed first-come first-serve only among those FIFOs that contain valid events. The first token is internally generated as needed (i.e. the *tki* and *tko* IOs are not used) and advanced with the token clock. The data in the FIFOs is thus sequentially multiplexed to the two digital outputs *data0* and *data1*. The first output *data0* is also used as a flag, indicating that events need to be read out from the chip. The external electronics releases a sync signal using the token clock as well (i.e. the token clock provides both advancement and data output synchronization), after which the 38-bit data is shifted out in parallel to the *data0* and *data1* outputs using either 19 clock cycles or 19 clock edges of the external data clock, depending on the global bit *sdcks*.

Along with the described channel-level processing, the ASIC also provides, at a single dedicated digital output *art*, the address of the first on-chip above-threshold event, called address in real time (ART). The ART mode is enabled with the bit *sfa*. Either at the pulse threshold crossing (bit *sfam* low) or at the pulse peak (bit *sfam* high) a flag is released at the *art* output. The flag is followed by the serialized address of the event. Also in this case the address is released either at each clock cycle or at each clock edge of the external ART clock, depending on the global bit *sdcka*.

The ASIC integrates global and acquisition resets, an adjustable pulse generator connected to the injection capacitor of each channel, adjustable with a global 10-bit DAC, and triggered with the external clock *tp*, a threshold generator adjustable with a global 10-bit DAC, a band-gap reference circuit, a temperature sensor. It also integrates analog monitor capability to directly measure the global DACs, the band-gap reference, a temperature sensor, the analog baseline, the analog pulse, and the channel threshold (after trimming). An analog buffer can be enabled using the bits *sbfm*. The monitor is controlled with global register bits *scmx, sm0-sm5* and channel register bit *smx*. The analog monitor can be routed to the *pdo* output using the register bit *sbmx*.

All digital IOs are low-voltage differential signals (LVDS) with a 600mV baseline and +/- 150mV swing. They are voltage driven devices and the maximum current they can drive is 15mA. The neighboring chips communicate using bi-directional LVDS IOs.

The power dissipation ranges from 500 mW to 800 mW depending on the selected functionalities and mode of operation. The worst case current required from the supplies are 150 mA for Vddp, 450 mA for Vdd, 200mA for Vddad, and 25mA for Vddd.

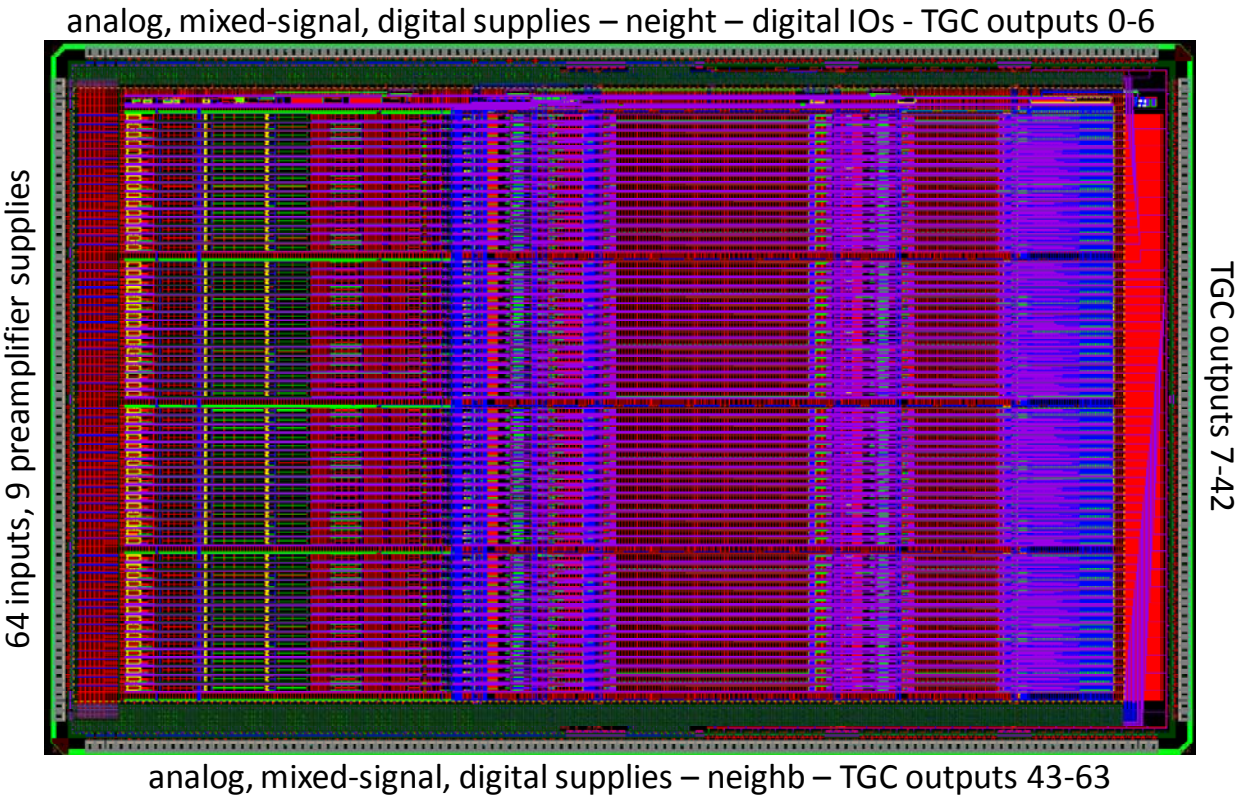


Fig. 2 – Physical layout of VMM2, size 13.5×8.4 mm² pad count 392.

Fig. 2 shows the physical layout of VMM2. It measures 13.5×8.4 mm² and it has 392 bonding pads. To the left are 64 inputs and 9 charge amplifier supplies, connected to the sources of the p-channel input MOSFETs. To the top are 60 analog supplies, 16 LVDS IOs, 16 mixed signal (ADC) and digital supplies, and the first 7 direct LVDS timing outputs. To the bottom are 63 analog supplies, 1 LVDS IO and the last 21 direct LVDS timing outputs. To the right are one digital ground and the remaining 35 LVDS timing outputs. A detailed ASIC pinout is reported later in this document.

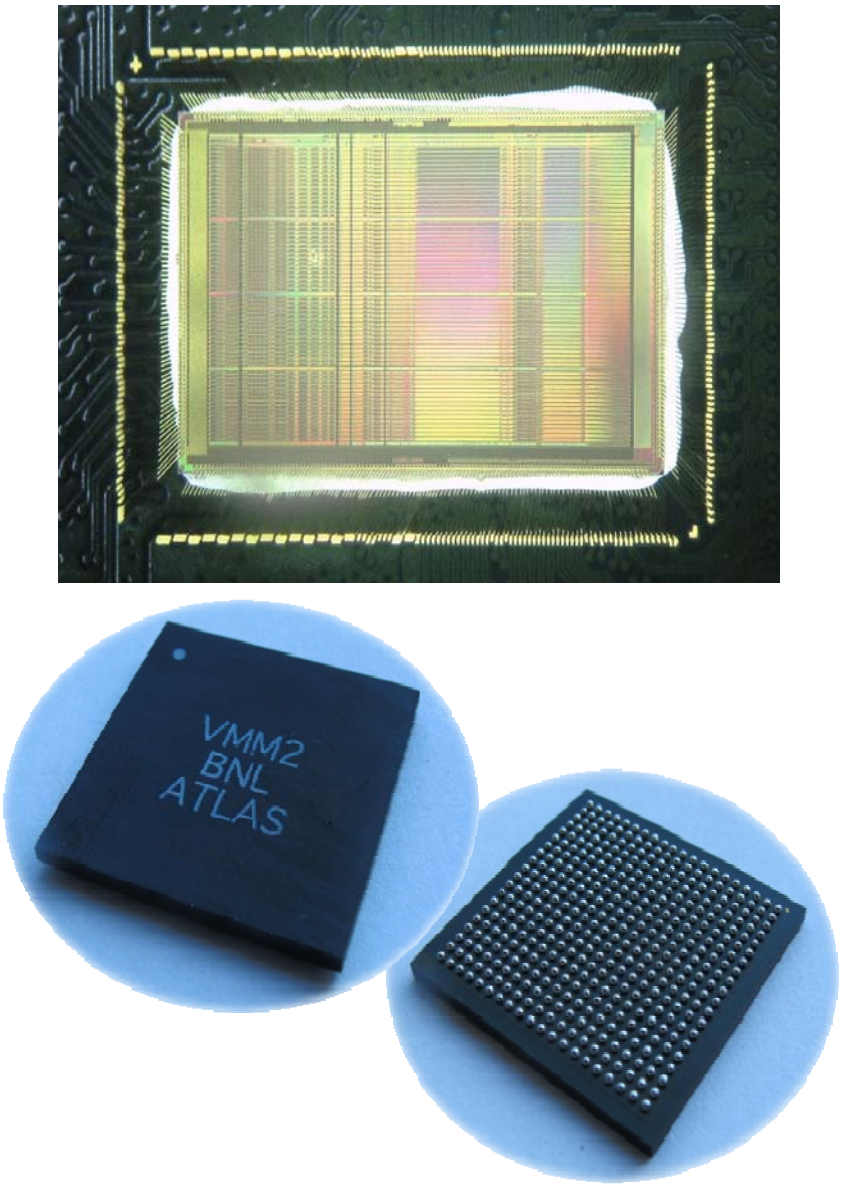


Fig. 3 – Die wire-bonded to substrate and BGA package, size 21 x 21 mm², pin count 400.

The ASIC is designed and fabricated using the 130nm 1.2V 8-metal CMOS technology from IBM. The ASIC is packaged in a custom 21 x 21 mm² 400-pin BGA package developed by i2a. Fig. 3 shows a picture of the package, characterized by a pin pitch of 1 mm. A detailed BGA package pinout is reported later in this document.

[1] G. De Geronimo, J. Fried, S. Li, J. Metcalfe, N. Nambiar, E. Vernon, and V. Polychronakos, "VMM1 – An ASIC for micropattern detectors", *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 2314-2321, 2013.
[2] G. De Geronimo and S. Li, "Shaper design in CMOS for high dynamic range", IEEE Trans. Nucl. Sci., vol. 58, no. 5, pp. 2382-2390, 2011.
[3] G. De Geronimo, J. Fried, G. C. Smith, B. Yu, E. Vernon, C. L. Britton, W. L. Bryan, L. G. Clonts, and S. S. Frank, "ASIC for small angle neutron scattering experiments at the SNS", IEEE Trans. Nucl. Sci., vol. 54, pp. 541-548, 2007.

Front-end and Signal Processing

- **Analog front-end**
  - sensor capacitance: optimized for 200pF, can operate from sub pF to 1nF, optimization for >30pF with channel register bit *sc*
  - input MOSFET: 10mm, 2mA, 11pF
  - input charge polarity: positive and negative, controlled with global register bit spg and channel register bit *sp*
  - shaper: 3rd order DDF with complex conjugate poles
  - band-gap referenced baseline stabilizer
  - peaking time: 25, 50, 100, 200 ns, controlled with global register bits *st0,st1*
  - gain: 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (maximum charge 2, 1, 0.33, 0.22, 0.17, 0.11, 0.08, 0.06 pC), controlled with global register bits *sg0,sg1,sg2*
  - channel mask, enabled with channel register bit *sm*
  - test capacitor ~ 1.2pF, enabled with channel register bit *st*
  - input leakage generator (required for continuous reset), enabled with channel register bit *sl*
  - pulse generator, common to all channels, 10-bit adjustable, ~1mV steps, with global bit registers *sdp0-sdp9,* strobe with *tp* input

- **Signal processing**
  - amplitude discriminator capable of processing sub-hysteresis signals, sub-hysteresis enabled with global register bit *ssh*
  - discrimination threshold adjustable with 10-bit global DAC, ~1mV steps, global register bits *sdt0-sdt9* and 4-bit channel DAC, ~1mV steps, channel register bits *sd0-sd3*
  - option of disabling discrimination once the first peak is detected, enabled with global register bits *sdp*
  - force-neighbor signal processing for above-threshold events: when an event exceeds the threshold, the neighbor channels (in neighbor chips if desired) are forced to peak/time detection; enabled with global register bit *sng*; first and last channels communicate with associated channels in neighbor chips through bi-directional pins *sett, setb*
  - peak detector with peak-found signal for accurate timing (multi-phase: track, peak-detect, hold&buffer)
  - 10-bit peak amplitude conversion available for each channel and controlled with global register bits *sttt, spdc, s6b, sc010b, sc110b, sdcks,* and channel register bits *sz010b, sz110b, sz210b* providing offset adjustment in LSB units.
  - time detector at peak-found with time-to-amplitude conversion implementing voltage ramp with adjustable duration: 0.125, 0.25, 0.5, 1 μs, controlled with global register bits *stc0,stc1*; ramp starts at peak-found from peak detector and stops either at falling edge of *ena* input or at next BC clock, controlled with global register bit *spdc*
  - 8-bit timing conversion available for each channel and controlled with global register bits *sttt, spdc, s6b, s8b, sc08b, sc18b, sdcks,* and channel register bits *sz08b, sz18b, sz28b* providing offset adjustment in LSB units.
  - address in real time (ART) available at output *art* either at threshold crossing or at peak found with flag indicator followed by serialized address, enabled and controlled with global register bits *sfa, sfam*

- time-over-threshold, threshold-to-peak, peak-to-threshold, pulse-at-peak available for each channel at dedicated outputs *ttp* and controlled with global register bits *sttt, stot, stpp*
- 6-bit peak amplitude conversion available for each channel at dedicated outputs *ttp* and controlled with data clock and global register bits *sttt, spdc, s6b, sc06b, sc16b, sc26b, sdck6b,* and channel register bits *sz06b, sz16b, sz26b* providing offset adjustment in LSB units.

Configuration and Registers

- **Configuration**
  - when in configuration mode (*wen* high, *ena* low), the configuration registers are accessible through the token clock *cktk* and the data input *di* inputs; the written configuration is available at the *do* output for daisy-chain configuration.
  - global register: 80 bits (5 reserved, 12 not used), channel register: 24-bits (2 not used)

- **Global bits (defaults are 0)**
  - *spg [0 1]*: input charge polarity (*[0]* negative, *[1]* positive)
  - *sdp*: disable-at-peak
  - *sbmx*: routes analog monitor to pdo output
  - *sbft [0 1],sbfp [0 1],sbfm [0 1]*: analog output buffers enable *[1]* (*tdo*, *pdo*, *mo*)
  - *slg*: leakage current disable *[0=enabled]*
  - *sm5-sm0, scmx*: monitor multiplexing
    - common monitor: *scmx, sm5-sm0 [0 000001 to 000100]*, pulser DAC (after pulser switch), threshold DAC, band-gap reference, temperature sensor
    - channel monitor: *scmx, sm5-sm0 [1 000000 to 111111]*, channels 0 to 63
  - *sfa [0 1], sfam [0 1]*: ART enable (*sfa [1]*) and mode (*sfam [0]* timing at threshold, *[1]* timing at peak)
  - *st1,st0 [00 01 10 11]*: peaktime (200, 100, 50, 25 ns)
  - *sfm [0 1]*: doubles the leakage current
  - *sg2,sg1,sg0 [000:111]*: gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)
  - *sng*: neighbor (channel and chip) triggering enable
  - *stot [0 1]*: timing outputs control 1
    - stpp,stot[00,01,10,11]: TtP,ToT,PtP,PtT
    - TtP: threshold-to-peak
    - ToT: time-over-threshold
    - TpP: pulse-at-peak (10ns)
    - PtT: peak-to-threshold
  - *sttt [0 1]*: timing outputs enable
  - *ssh [0 1]*: sub-hysteresis discrimination enable *[1]*
  - *stc1,stc0 [00 01 10 11]*: TAC slope adjustment (125, 250, 500, 1000 ns)
  - *sdt9-sdt0 [0:0 through 1:1]*: coarse threshold DAC
  - *sdp9-sdp0 [0:0 through 1:1]*: test pulse DAC
  - *sc010b,sc110b*: 10-bit ADC conversion time
  - *sc08b,sc18b*: 8-bit ADC conversion time
  - *sc06b,sc16b,sc26b*: 6-bit ADC conversion time
  - *s8b*: 8-bit ADC conversion mode
  - *s6b*: 6-bit ADC enable (10-bit and 8-bit disable)
  - *spdc*: ADCs enable
  - *sdcks*: dual clock edge serialized data enable
  - *sdcka*: dual clock edge serialized ART enable
  - *sdck6b*: dual clock edge serialized 6-bit enable
  - *sdrv*: tristates analog outputs with token, used in analog mode
  - *stpp [0 1]*: timing outputs control 2

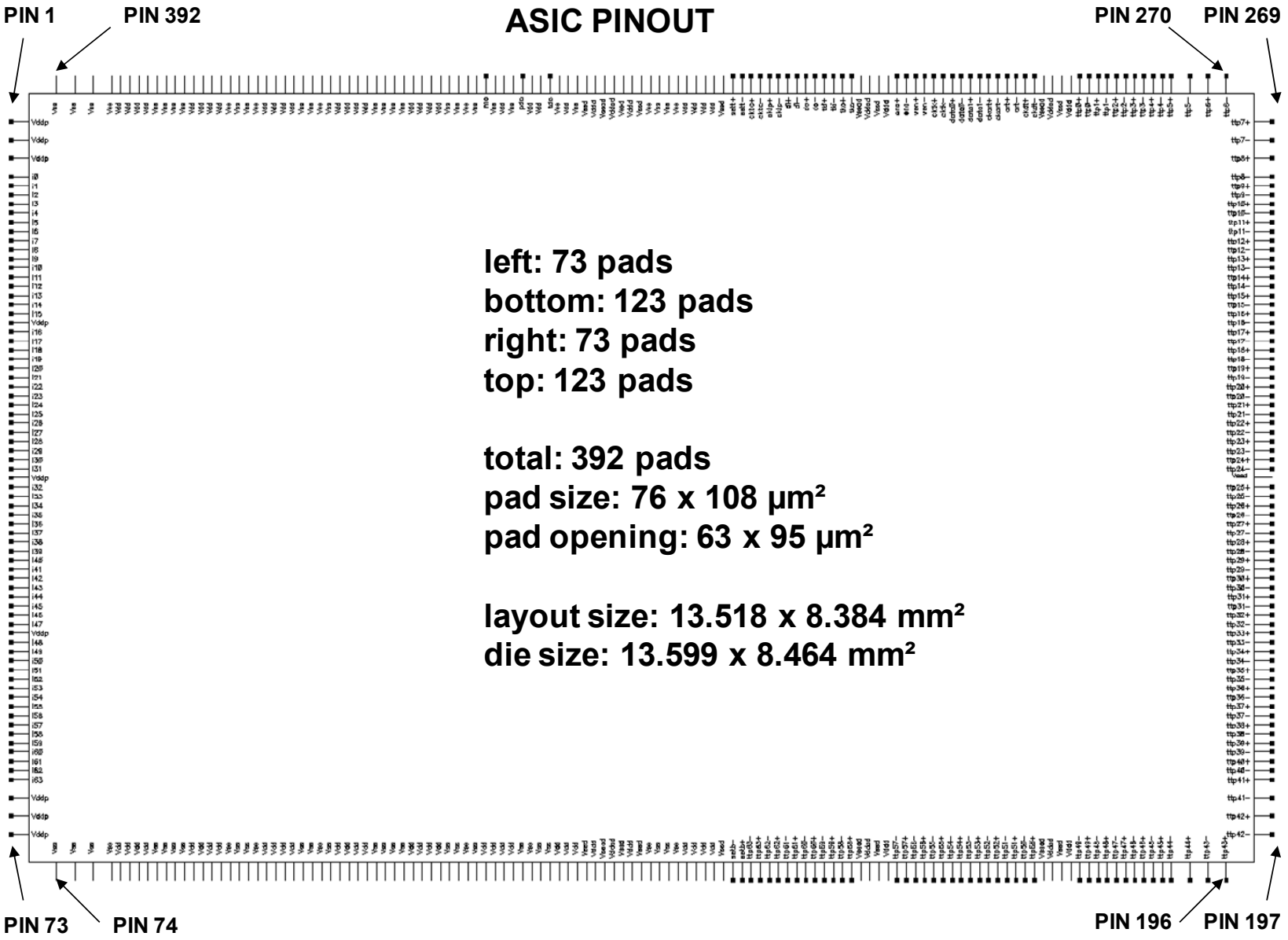
- **Channel bits (defaults are 0)**
  - *sp [0 1]*: input charge polarity (*[0]* negative, *[1]* positive)
  - *sc [0 1]*: large sensor capacitance mode (*[0]* <~30pF, *[1]* >~30pF)
  - *sl [0 1]*: leakage current disable *[0=enabled]*
  - *st [0 1]*: 1.2pF test capacitor enable *[1]*
  - *sm [0 1]*: mask enable *[1]*
  - *sd0-sd3 [0:0 through 1:1]*: trim threshold DAC, 1mV step (*[0:0]* trim 0V, *[1:1]* trim –15mV)
  - *smx [0 1]*: channel monitor mode (*[0]* analog output, *[1]* trimmed threshold)
  - *sz010b,sz110b,sz210b,sz310b,sz410b*: 10-bit ADC zero
  - *sz08b,sz18b,sz28b,sz38b*: 8-bit ADC zero
  - *sz06b,sz16b,sz26b*: 6-bit ADC zero

- **Bit order and configuration process**
  - enabled with *wen* high, data shifted at falling edge of *ck*, latched at *wen* low
  - single string, 80+24x64=1616 bit
  - global register:
    - [spg *sdp sbmx sbft sbfp sbfm slg sm5:sm0 scmx sfa sfam st1:0 sfm sg2:0 sng stot sttt ssh stc1:0 sdt9:0 sdp9:0 sc010b:sc110b sc08b:sc18b sc06b:sc26b s8b s6b spdc sdcks sdcka sdck6b sdrv stpp res00 res0 res1 res2 res3 nu nu nu nu nu nu nu nu nu nu nu nu*]
  - channel register (64x):
    - [*sp sc sl st sm sd0:sd3 smx sz010b:sz410b sz08b:sz38b sz06b:sz26b nu nulast*]
  - first bit to write: channel 63 last bit
  - last bit to write: *spg*

Unpackaged ASIC Pinout

- 392 pins (73 left and right, 123 top and bottom)
- *Vdd,Vss (123 total)*: analog supplies 1.2V and grounds 0V - max current ~ 400mA
- *Vddad, Vssad (12 total)*: mixed-signal (ADC) supplies 1.2V and grounds 0V - max current ~ 200mA
- *Vddd, Vssd (21 total)*: digital supplies 1.2V and grounds 0V
- *Vddp (9 total)*: charge amplifier supplies 1.2V - max current ~ 150mA
- *i0-i63*: analog inputs, ESD protected
- *mo*: monitor multiplexed analog output
- *pdo*: peak detector multiplexed analog output
- *tdo*: time detector multiplexed analog output
- *sett*: ch0 neighbor trigger
- *ckbc*: BC clock (timestamp Gray-code counter advance)
- *cktp*: test pulse clock
- *di*: configuration data input
- *do*: configuration data output
- *tki*: token input (in analog mode)
- *tko*: token output (in analog mode)
- *ena*: acquisition start/stop
    - *ena* high, *wen* low: acquisition is enabled
        - internally enabled after 40ns from *ena* high
        - in *two-phase* (*analog*) mode is acquisition
        - in *continuous* (*digital*) mode is acquisition and readout
    - *ena* low, *wen* low: in *two-phase* mode is readout
    - *ena* pulse, *wen* high: global reset (acquisition and registers)
- *wen*: configuration enable
    - *wen* high: configuration mode
    - *wen* pulse: acquisition reset (also resets BC counter)
- *cktk*: token and configuration clock
- *data0*: flag and first data line (flag and address in analog mode)
- *data1*: second data line
- *ckart*: ART clock
- *art*: ART output
- *ckdt*: data output and 6-bit ADC clock
- *ttp0-ttp63*: direct digital outputs
- *setb*: ch63 neighbor trigger

ASIC PINOUT

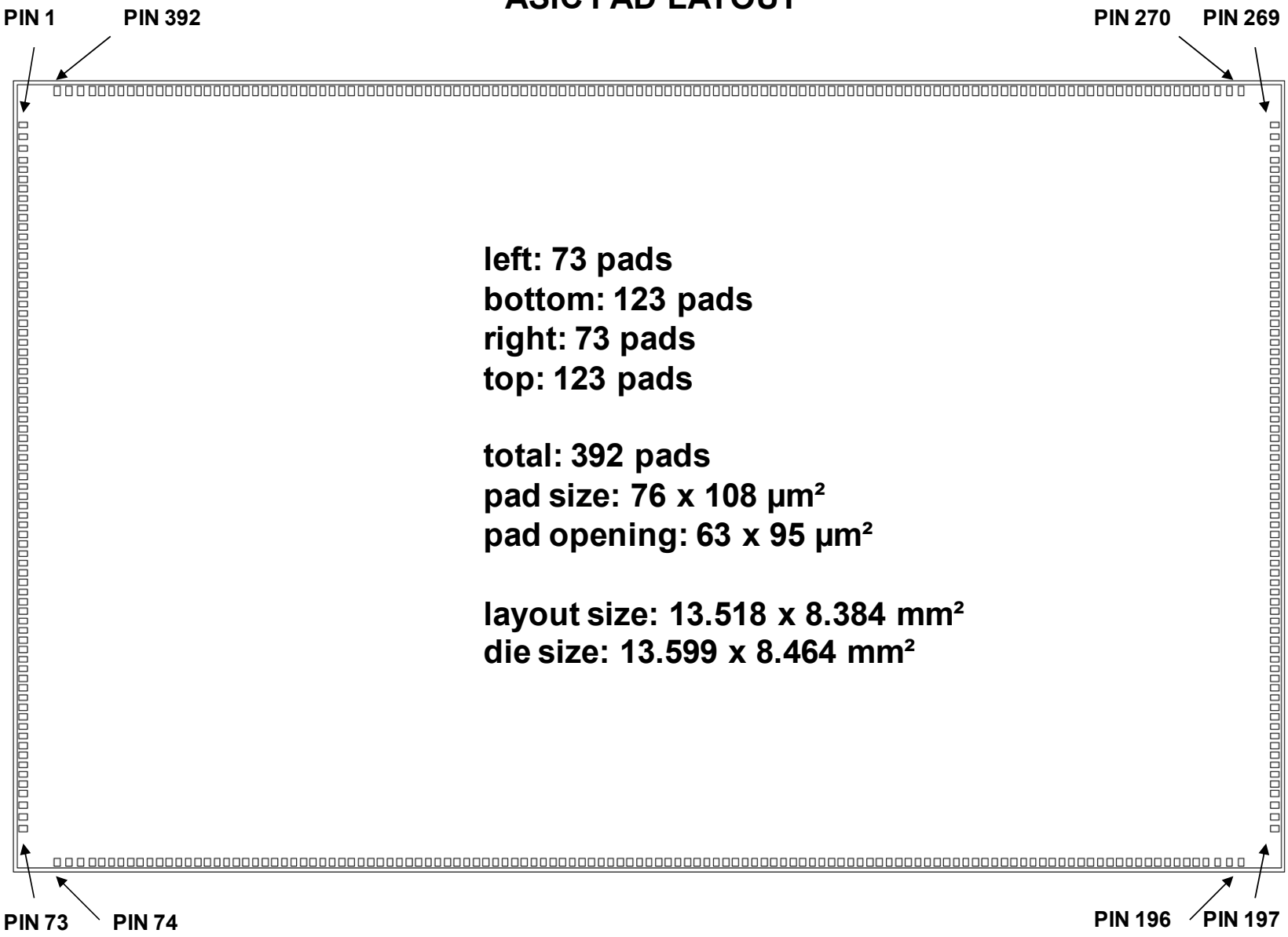


left: 73 pads
bottom: 123 pads
right: 73 pads
top: 123 pads

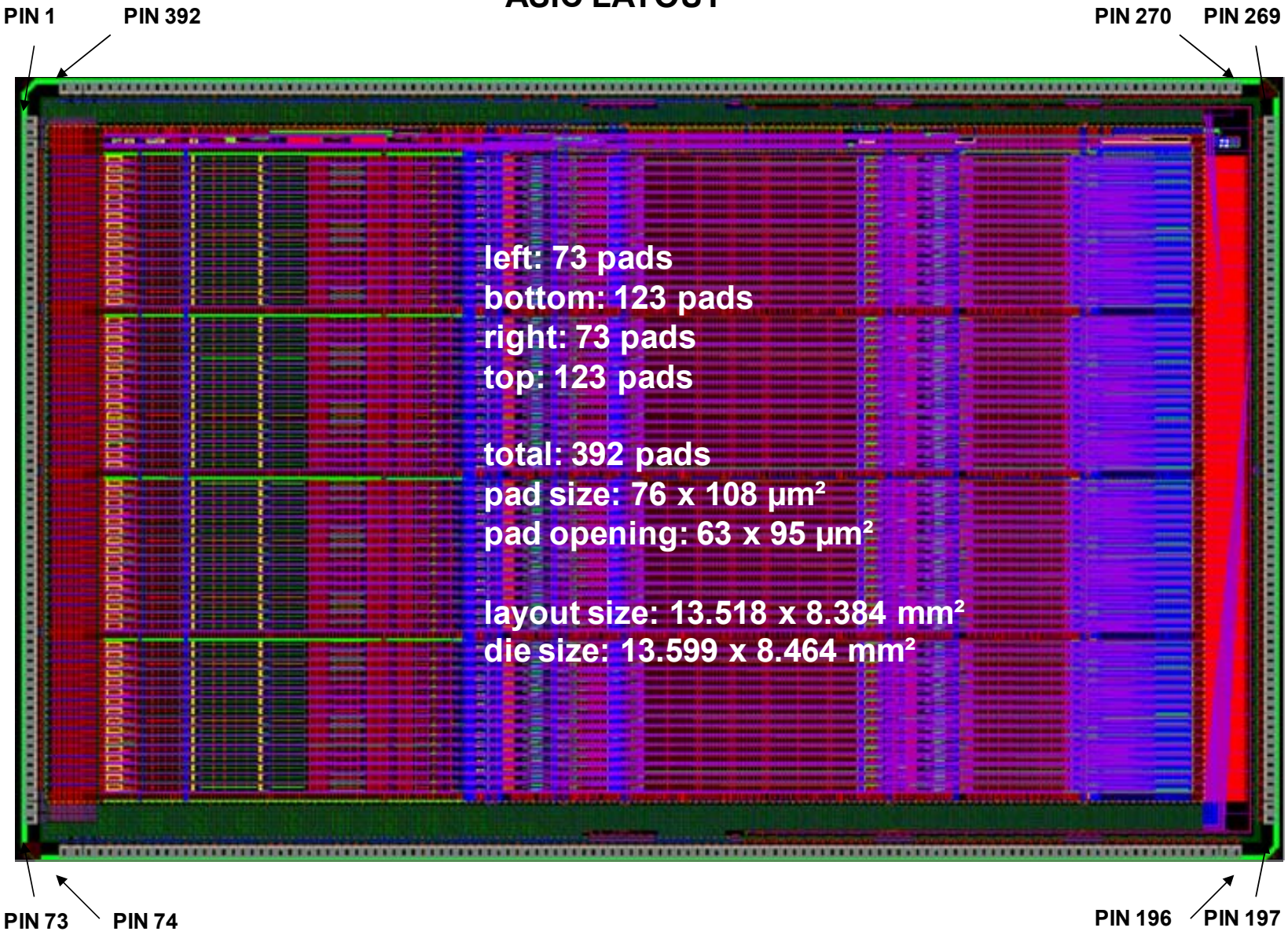
total: 392 pads
pad size: 76 x 108 µm²
pad opening: 63 x 95 µm²

layout size: 13.518 x 8.384 mm²
die size: 13.599 x 8.464 mm²

ASIC PAD LAYOUT



ASIC LAYOUT

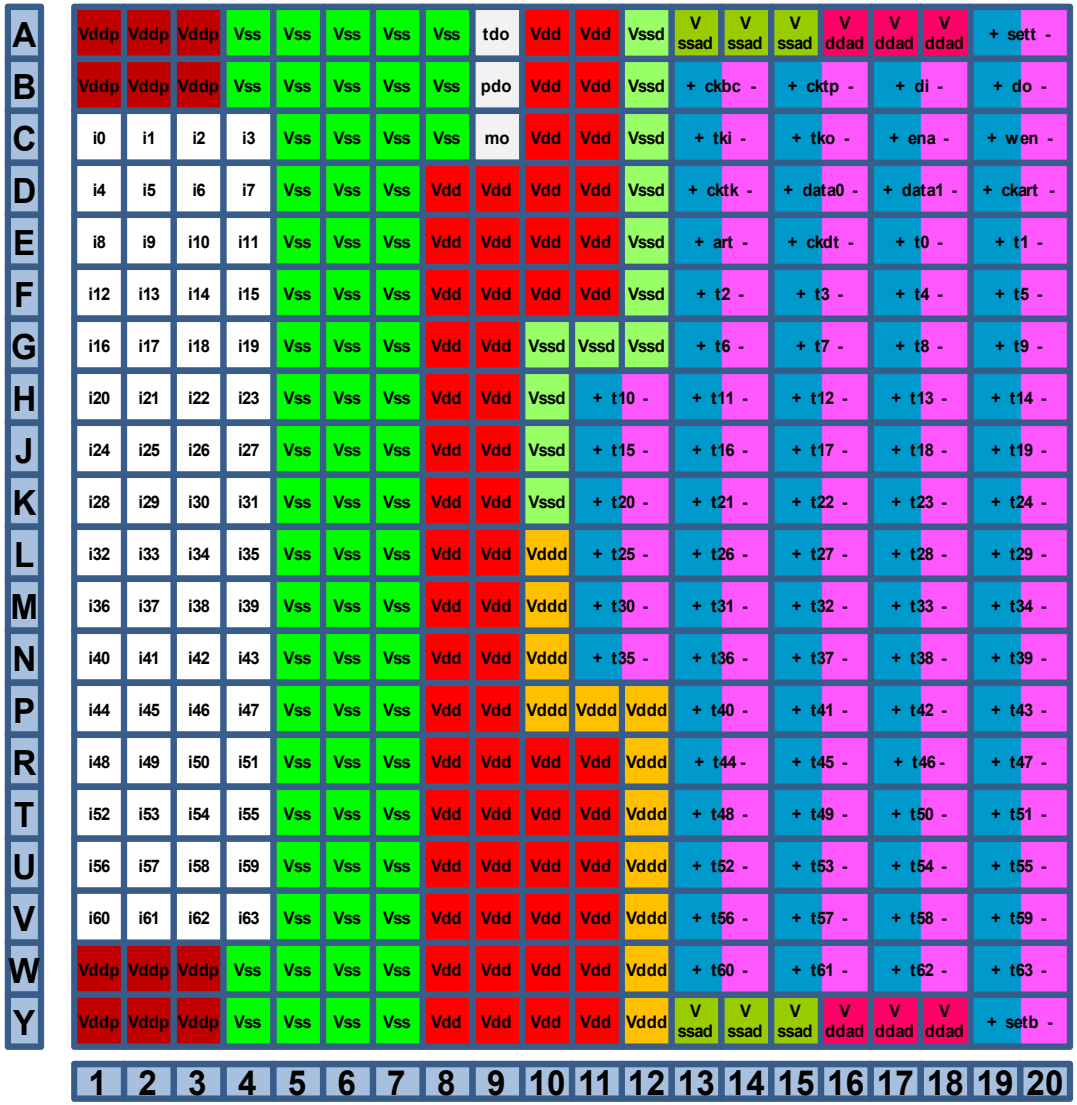

PIN 1
PIN 392
PIN 270
PIN 269
left: 73 pads
bottom: 123 pads
right: 73 pads
top: 123 pads
total: 392 pads
pad size: 76 x 108 µm²
pad opening: 63 x 95 µm²
layout size: 13.518 x 8.384 mm²
die size: 13.599 x 8.464 mm²
PIN 73
PIN 74
PIN 196
PIN 197

BGA-Packaged ASIC Pinout

Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vss	tdo	Vdd	Vdd	Vssd	Vssad	Vssad	Vssad	Vddad	Vddad	Vddad	sett	nsett
Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vss	pdo	Vdd	Vdd	Vssd	ckbc	nckbc	cktp	ncktp	di	ndi	do	ndo
i0	i1	i2	i3	Vss	Vss	Vss	Vss	mo	Vdd	Vdd	Vssd	tki	ntki	tko	ntko	ena	nena	wen	nwen
i4	i5	i6	i7	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	cktk	ncktk	data0	ndata0	data1	ndata1	ckart	nckart
i8	i9	i10	i11	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	art	nart	ckdt	nckdt	t0	nt0	t1	nt1
i12	i13	i14	i15	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	t2	nt2	t3	nt3	t4	nt4	t5	nt5
i16	i17	i18	i19	Vss	Vss	Vss	Vdd	Vdd	Vssd	Vssd	Vssd	t6	nt6	t7	nt7	t8	nt8	t9	nt9
i20	i21	i22	i23	Vss	Vss	Vss	Vdd	Vdd	Vssd	t10	nt10	t11	nt11	t12	nt12	t13	nt13	t14	nt14
i24	i25	i26	i27	Vss	Vss	Vss	Vdd	Vdd	Vssd	t15	nt15	t16	nt16	t17	nt17	t18	nt18	t19	nt19
i28	i29	i30	i31	Vss	Vss	Vss	Vdd	Vdd	Vssd	t20	nt20	t21	nt21	t22	nt22	t23	nt23	t24	nt24
i32	i33	i34	i35	Vss	Vss	Vss	Vdd	Vdd	Vddd	t25	nt25	t26	nt26	t27	nt27	t28	nt28	t29	nt29
i36	i37	i38	i39	Vss	Vss	Vss	Vdd	Vdd	Vddd	t30	nt30	t31	nt31	t32	nt32	t33	nt33	t34	nt34
i40	i41	i42	i43	Vss	Vss	Vss	Vdd	Vdd	Vddd	t35	nt35	t36	nt36	t37	nt37	t38	nt38	t39	nt39
i44	i45	i46	i47	Vss	Vss	Vss	Vdd	Vdd	Vddd	Vddd	Vddd	t40	nt40	t41	nt41	t42	nt42	t43	nt43
i48	i49	i50	i51	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	t44	nt44	t45	nt45	t46	nt46	t47	nt47
i52	i53	i54	i55	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	t48	nt48	t49	nt49	t50	nt50	t51	nt51
i56	i57	i58	i59	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	t52	nt52	t53	nt53	t54	nt54	t55	nt55
i60	i61	i62	i63	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	t56	nt56	t57	nt57	t58	nt58	t59	nt59
Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	t60	nt60	t61	nt61	t62	nt62	t63	nt63
Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	Vssad	Vssad	Vssad	Vddad	Vddad	Vddad	setb	nsetb

BGA PINOUT

TOP VIEW



Vddp preamp +1.2V

Vdd analog +1.2V

Vss analog 0V

V ddad mixed +1.2V

V ssad mixed 0V

Vddd digital +1.2V

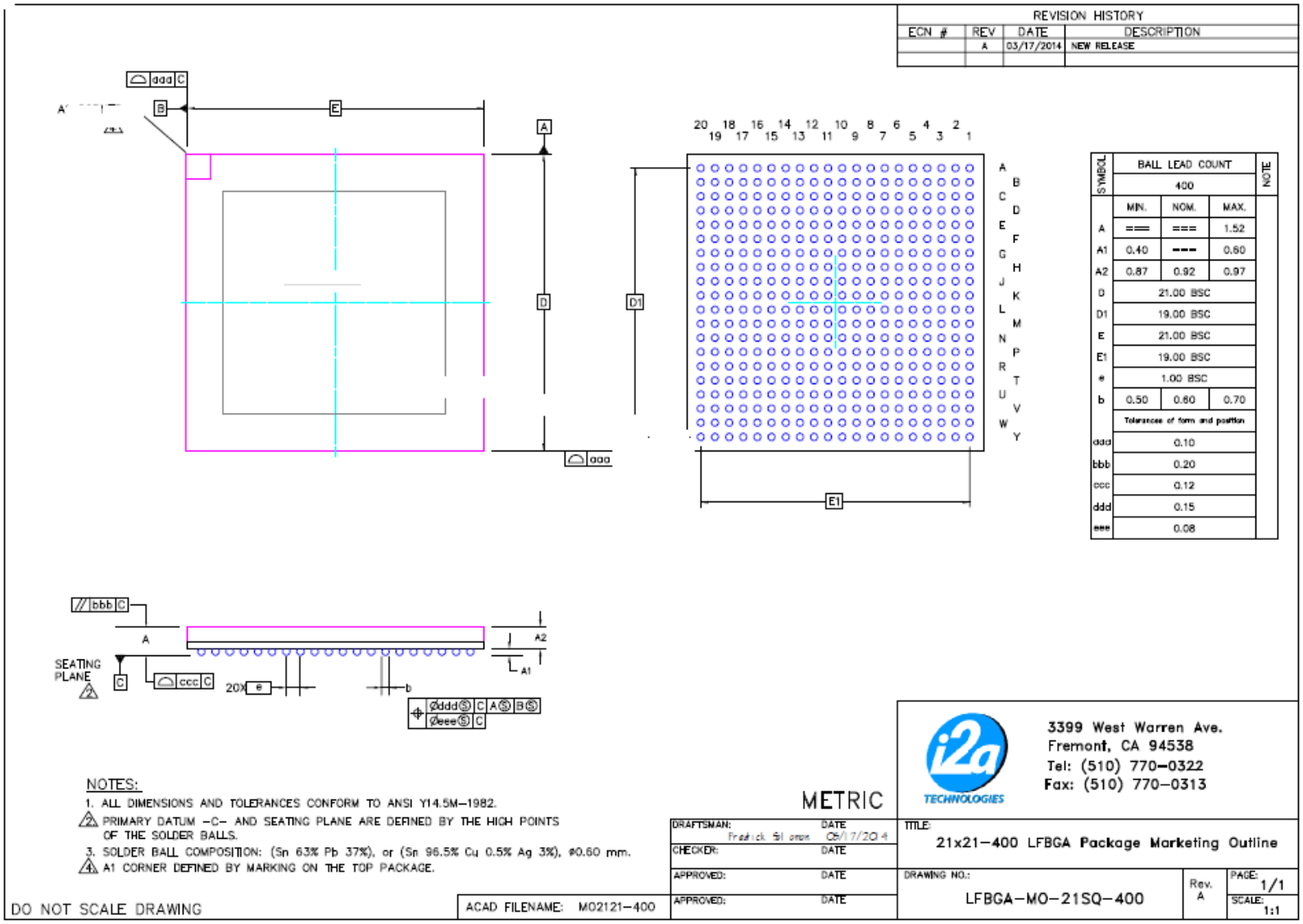
Vssd digital 0V

analog in

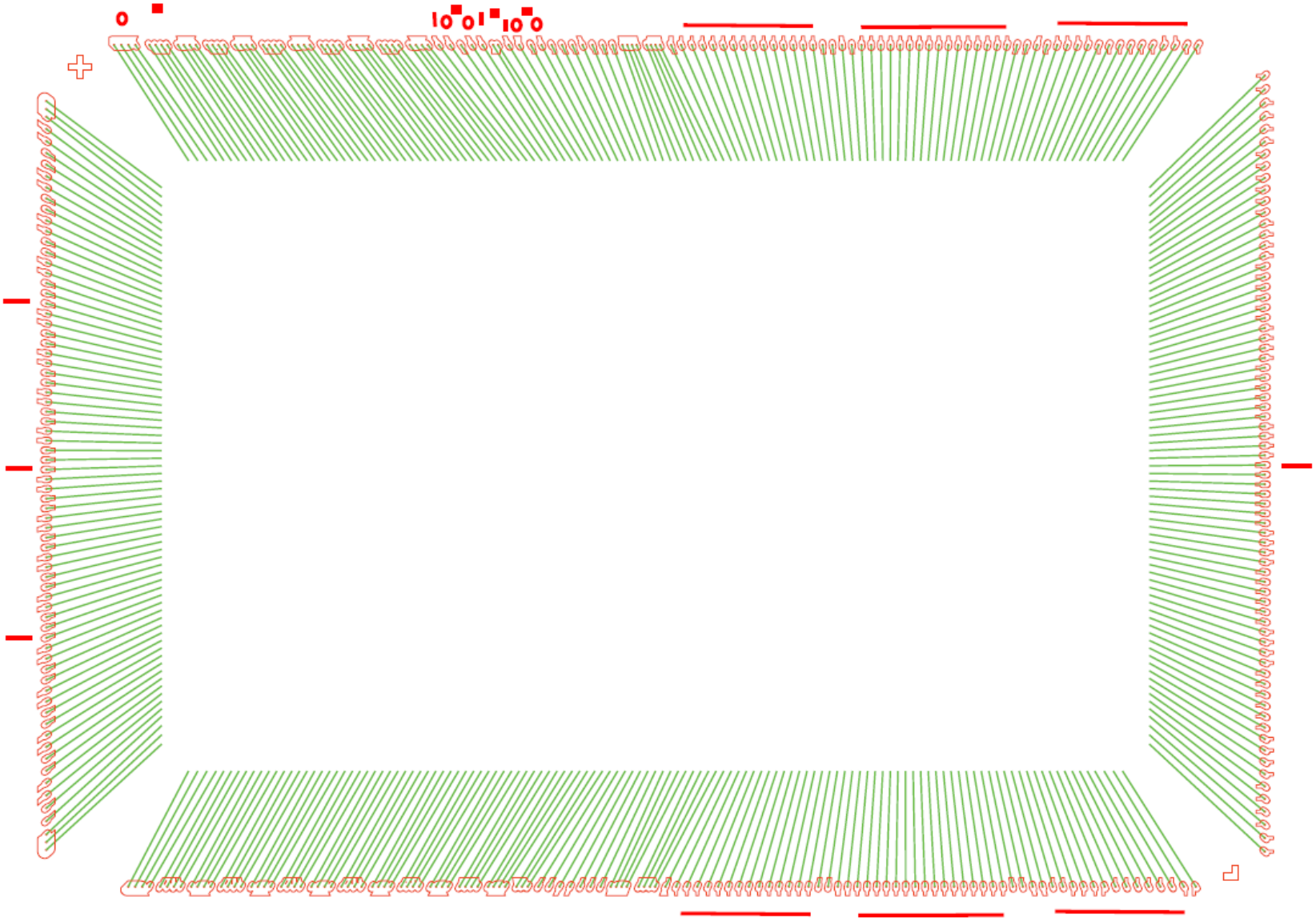
analog out

+ xxx - LVDS IO

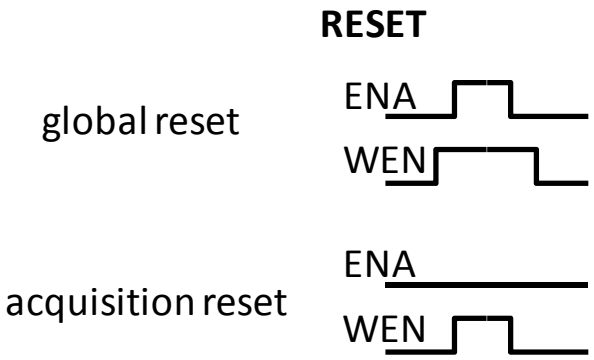
Package Outline Drawing



Bonding Diagram

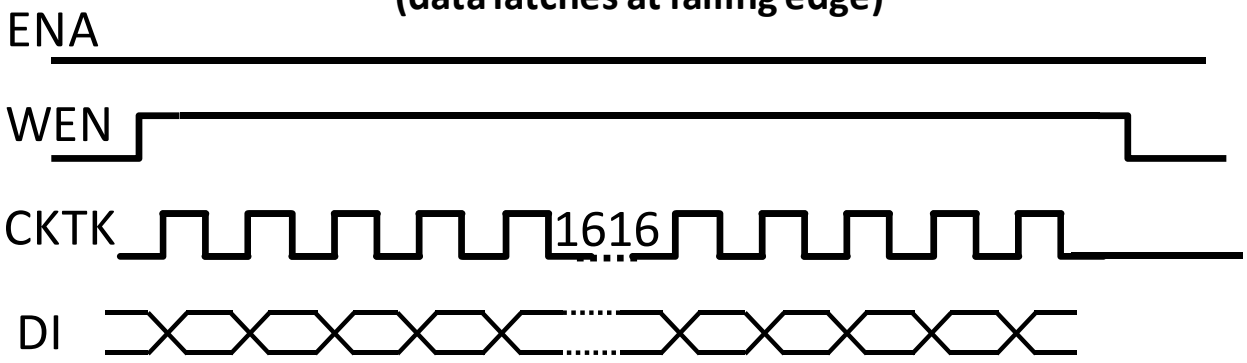


Timing Diagrams

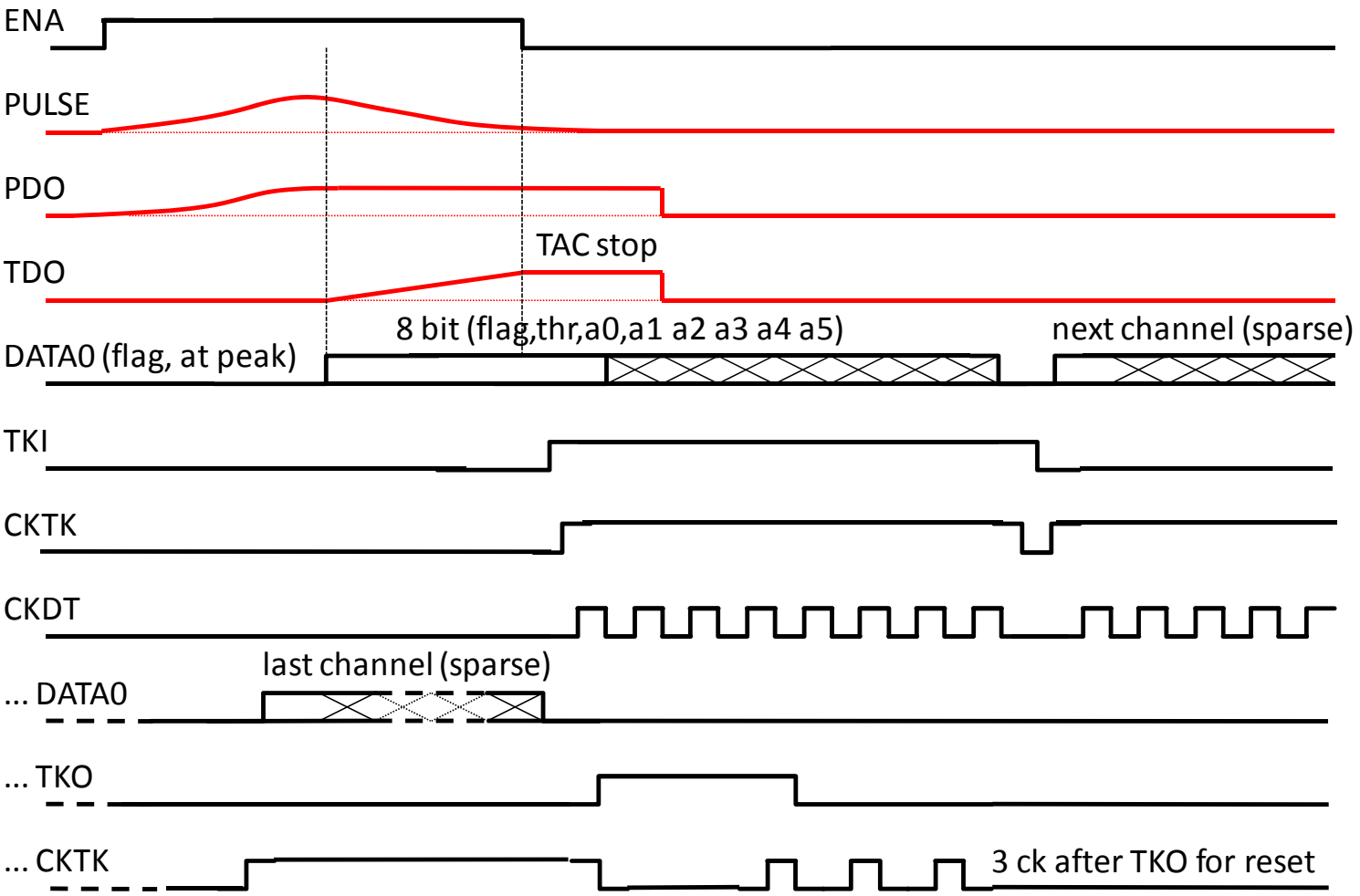


CONFIGURATION

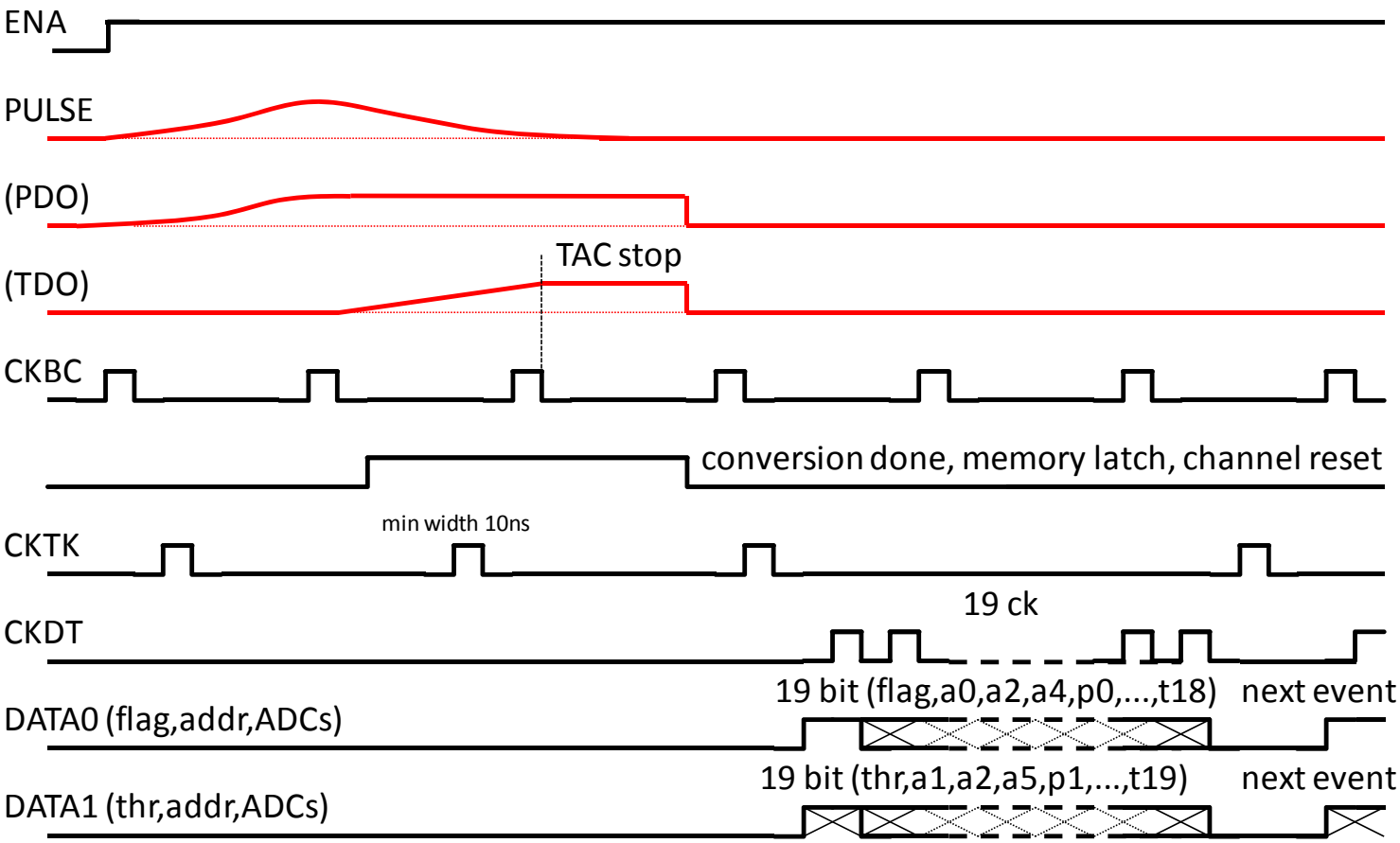
(data latches at falling edge)



DATA READOUT with PDO,TDO and external ADC (2-phase mode)

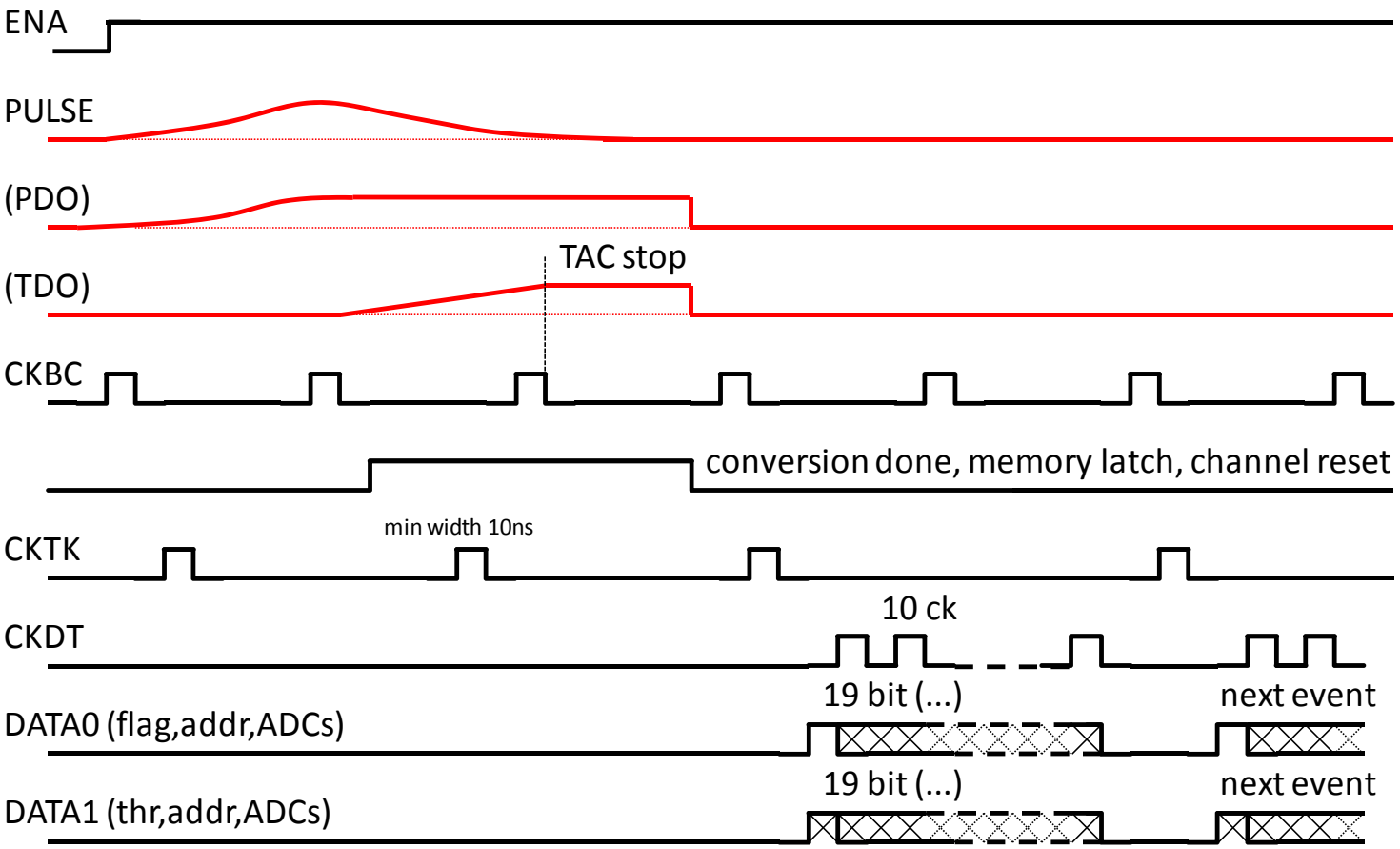


DATA READOUT with ADCs (continuous mode, 1bit/ck)



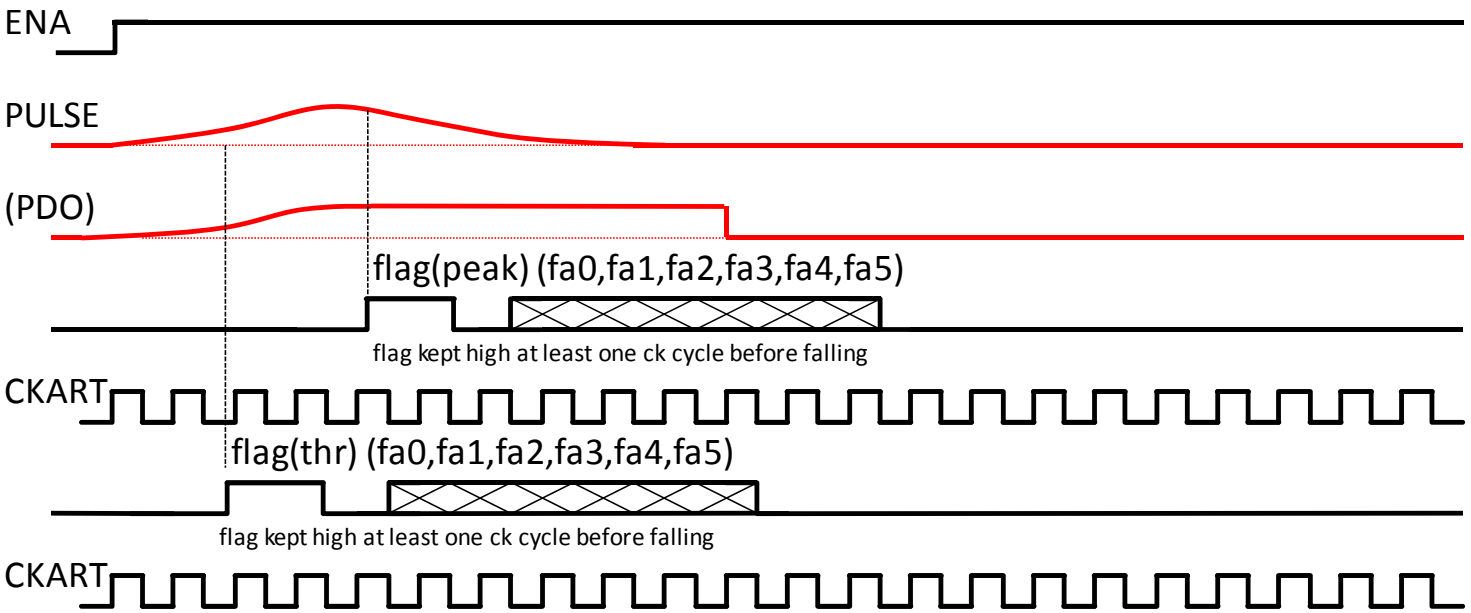
Notes: - enabled with bit SPDC high and S6B low
- data mode (1bit/ck or 2/bit/ck) set with bit sdcks

DATA READOUT with ADCs (continuous mode, 2bit/ck)



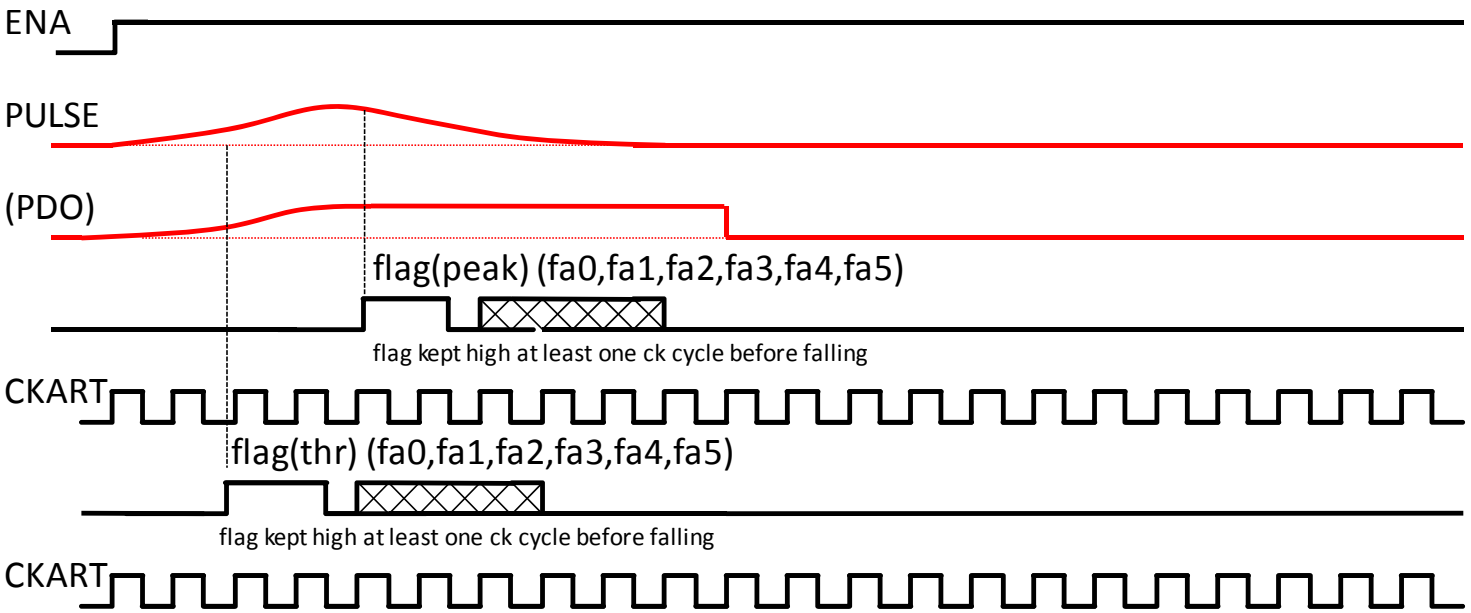
Notes: - enabled with bit SPDC high and S6B low
- data mode (1bit/ck or 2/bit/ck) set with bit sdcks

ART READOUT (1bit/ck data)



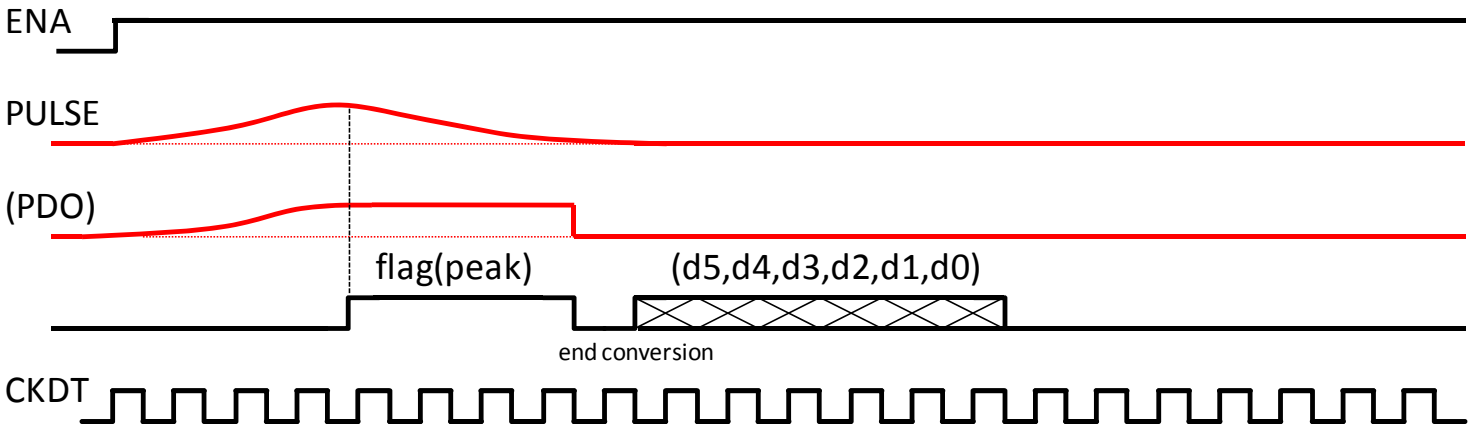
Notes:
- ART enabled with bit SFA
- flag mode (threshold or peak) set with bit SFAM
- data mode (1bit/ck or 2/bit/ck) set with bit sdcka

ART READOUT (2bit/ck data)



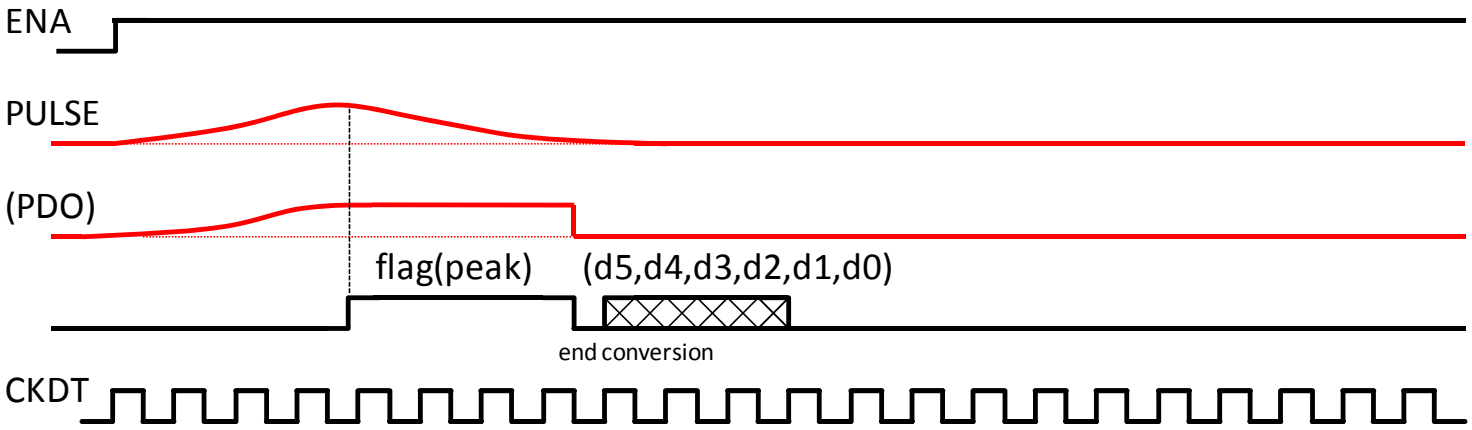
Notes:
- ART enabled with bit SFA
- flag mode (threshold or peak) set with bit SFAM
- data mode (1bit/ck or 2/bit/ck) set with bit sdcka

CHANNEL (6-bit) READOUT (1bit/ck data)



Notes: - enabled with bits SPDC and S6B
- conversion time programmable in CKDT units with bits sc06b,sc16b,sc26b
- data mode (1bit/ck or 2/bit/ck) set with bit sdck6b

CHANNEL (6-bit) READOUT (2bit/ck data)



Notes: - enabled with bit SPDC and S6B
- conversion time programmable in CKDT units with bits sc06b,sc16b,sc26b
- data mode (1bit/ck or 2/bit/ck) set with bit sdck6b