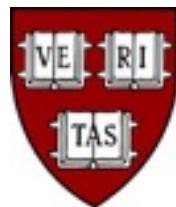


# VMM studies with the Harvard Micromegas Octuplet

M. Bledsoe, N. Felt, M. Franklin, B. Garber,  
P. Giromini, J. Grotto, J. Huth, **C. Rogan**,  
S. Sussman, A. Tuna, A. Wang, N. Wuerfel



HARVARD  
UNIVERSITY



ATLAS Muon Week - Chios, Greece - September 28, 2016

# Talk Outline

- Harvard Micromega Octuplet
  - Project goals and scope
  - Experimental setup
  - Data acquisition and calibration
- Preliminary data-taking results
- Lessons learned and open issues
  - Chamber noise
  - High Voltage protection and effects
  - Zebra connector studies
  - Duplicate channels in data
- Next steps and outlook

# Scope and Goals

**Primary Goal:** Integrate 8 MM chambers, with readout using 8 MMFE8's, with MM trigger processor in cosmic ray telescope



**MMFE8s**

- MMFE8 firmware and readout software **DONE**
- Amplitude and timing calibration with on-board test-pulse and xADC

**DONE** ▪ 8 MMFE8 readout and DAQ software

**DONE** ▪ External trigger and clock inputs for synchronicity

**DONE** ▪ Cooling system for boards

**DONE** ▪ Integration into test-stand



**MM Octuplet**

- Readout ADDC and trigger processor with octuplet input
- Communicate trigger processor accept signal to octuplet (via L1DDC)

**IN PROGRESS**

**FUTURE**

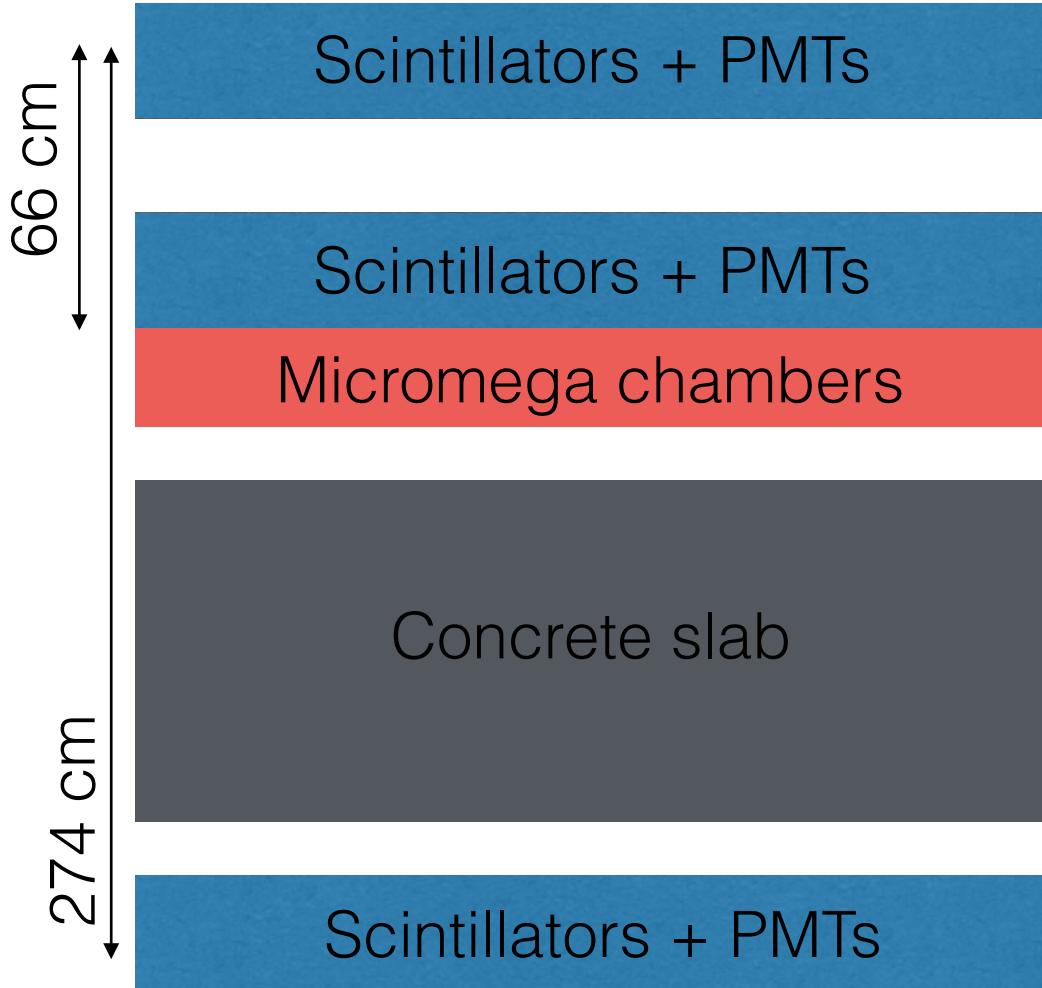
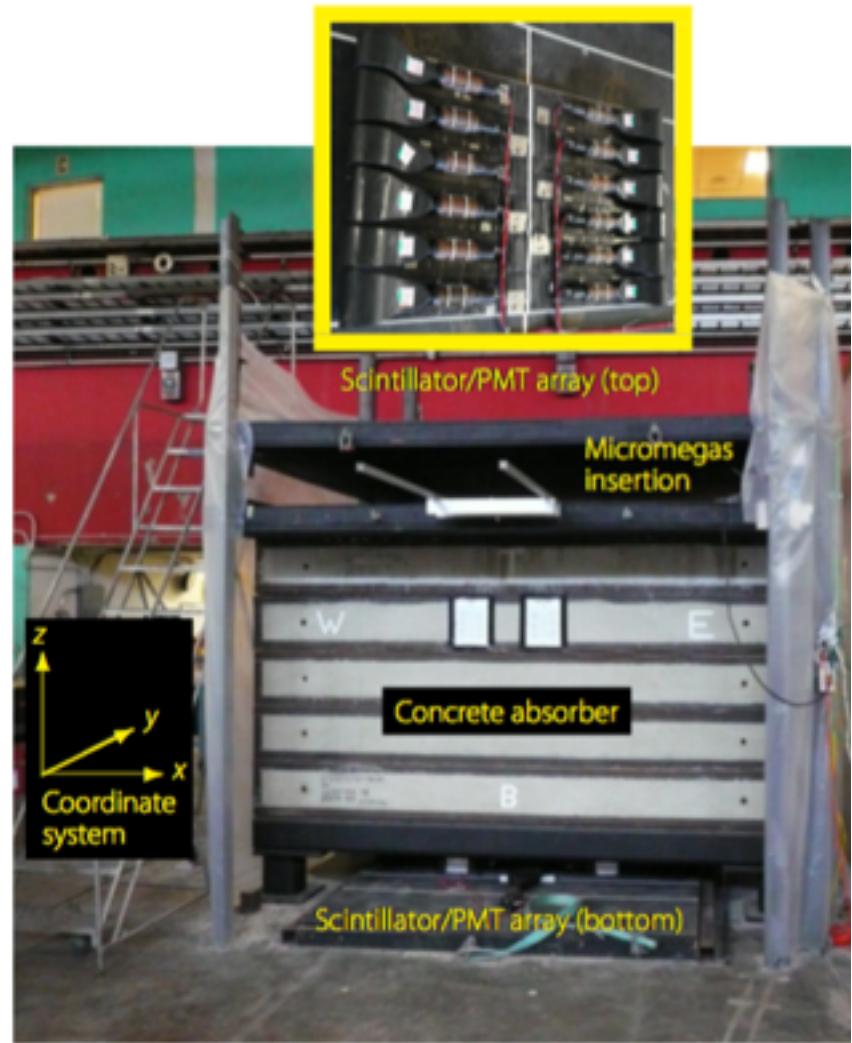


**Trigger Processor**



# Harvard cosmic-ray test stand

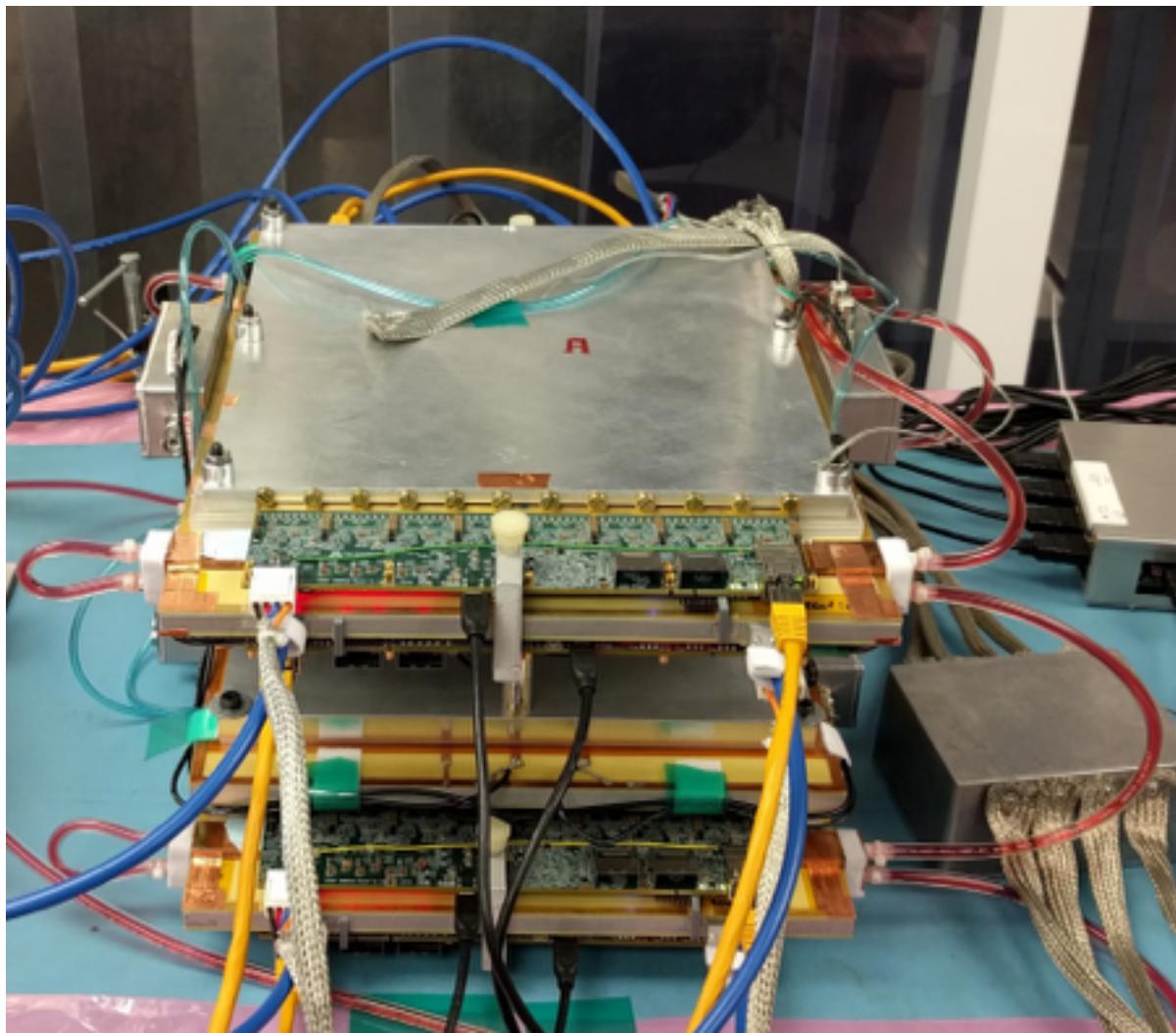
Maximum angle of muon track -13 to 23 degrees



# Micromega Octuplet Setup

- 8 20 x 20 cm Micromega chambers

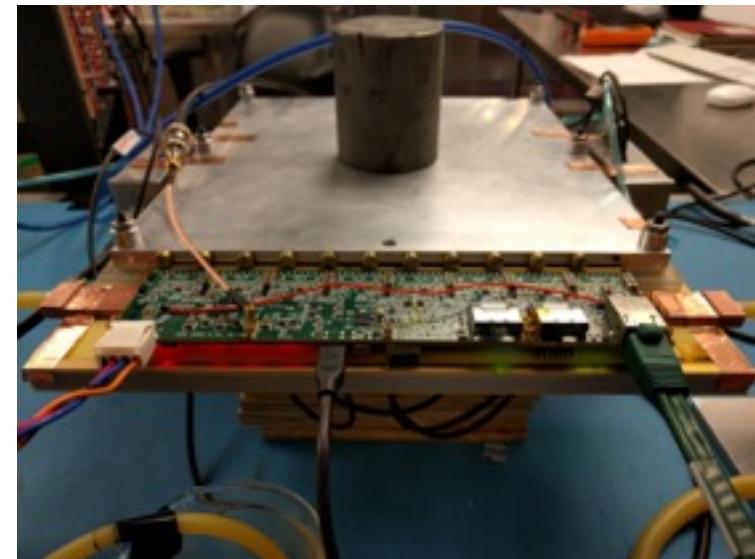
- **blue pipes**  
compressed air
- **shielded cables**  
LV power supply
- **yellow cords**  
ethernet cables





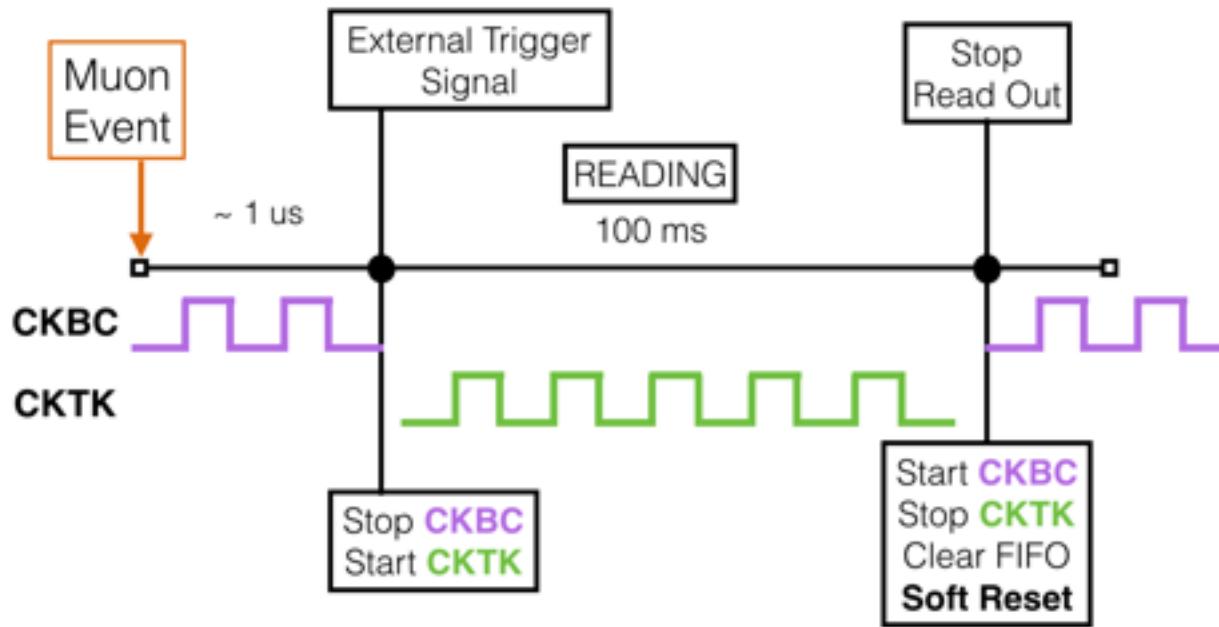
# MMFE8 Readout

- Using Rev. C + Rev D MMFE8 boards
- Have firmware + software DAQ system that is able to handle multiple MMFE8s with 8 VMMs each
- Extensive bench tests of noise, readout, and calibration, for many boards
- Firmware and readout software is based on the HU+AZ firmware and GUI, with several additions
  - Incorporated a full Xilinx Vivado **license** (no longer dropped ethernet connections with SDK after ~8-10 hours)
  - Programmed FPGA **flash memory** of boards with the BIT + ELF files for operation without JTAG connector
  - All boards use a common input mother clock and external trigger signal for **synchronicity**



**Single Micromega chamber with MMFE8 on bench**

- Logic of DAQ system presented in 12 February NSW elx meeting (<https://indico.cern.ch/event/496030/>) now with a few modifications:
- For every event, we read out the **VMM data** from the FPGA FIFO, as well as
  - the **number of CKBC** preceding the event trigger (trigger BCID)
  - the total **number of event triggers** that received (event number)
- Soft reset and a FIFO reset sent every 4096 BC's, unless event is acquired and resets are sent after readout



- Currently, CKTK only enabled after receiving an external trigger signal ( $1 \mu\text{s}$  after event)
- We found that CKTK token interrogating VMM FIFO while it is being filled could result in data corruption and duplicates
- Operating as a 1-hit system, with FIFOs being overwritten until read out by FPGA
- In 100 ms, currently can read out up to 50 hits per board

# MMFE8 DAQ System



- GUI based on AZ original code for 1 board, with the added ability to configure multiple MMFE8s with 8 VMMs each
- Library of masked channels and thresholds for each board for test-stand configuration
- Python-based DAQ reads out boards when first board indicates external trigger

**VMM Configuration**

VMM #

Input Charge Polarity (spg)  
 Disable-at-Peak (sdp)  
 Route Analog Monitor to PDO Output (sbmx)  
 Analog Output Buffer, TDO (sbt)  
 Analog Output Buffer, PDO (sbfp)  
 Analog Output Buffer, MO (sbfm)  
 Leakage Current Disable (slg)  
 SCMX  
 CHN 9   
 ART Enable (sfa)  
 timing-at-threshold  ART En. Mode (sfam)  
 200 ns  Peaking Time (st)  
 SFM (doubles leakage current)  
 9.0 (101)  Gain, mV/fC (sg)  
 Neighbor Triggering (sng)  
 Timing Outputs (sts)

**Channel Configuration**

	SP	SC	SL	ST	SM	SMX	SD	SZ10b	SZ8b	SZ6b
*	<input type="button" value="n"/>									
01	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
02	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
03	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
04	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
05	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
06	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
07	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
08	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
09	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns
10	n	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	<input type="button" value="n"/>	0 mv	<input type="button" value="n"/>	0 ns	0 ns	0 ns

# VMM2 Calibration

- Automated calibration program

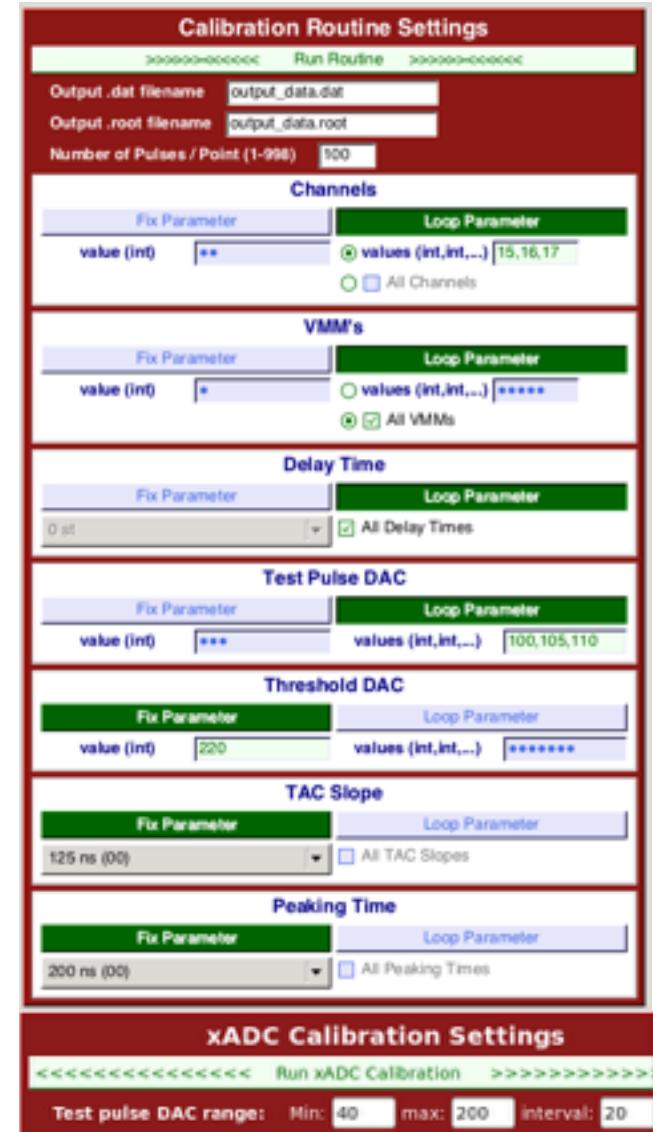
- GUI interface for configuration
- Useful for board/VMM diagnostics

- Program sends pulses to selected channels and reads out data, while varying one or more customizable parameters:

- Peaktiming, input DAC value for step pulse, Channels, VMM, Time delay of CKTP with respect to CKBC, # pulses sent

- Also collects xADC calibration data, using the MMFE8 FPGA ADC to calibrate the test pulse

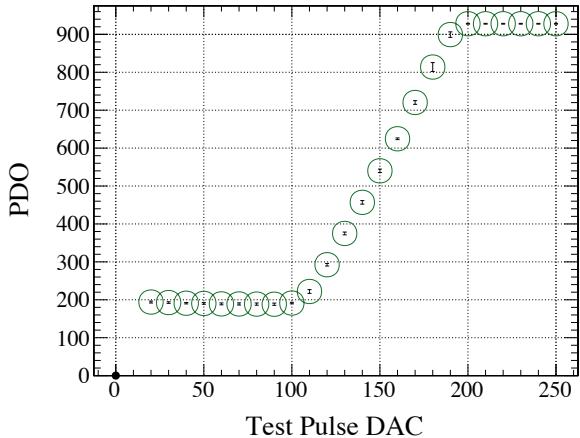
- Use **VMM2\_Calibration** package ([https://github.com/crogan/VMM2\\_Calibration](https://github.com/crogan/VMM2_Calibration)), automates fits of PDO and TDO output, provides databases of calibration factors



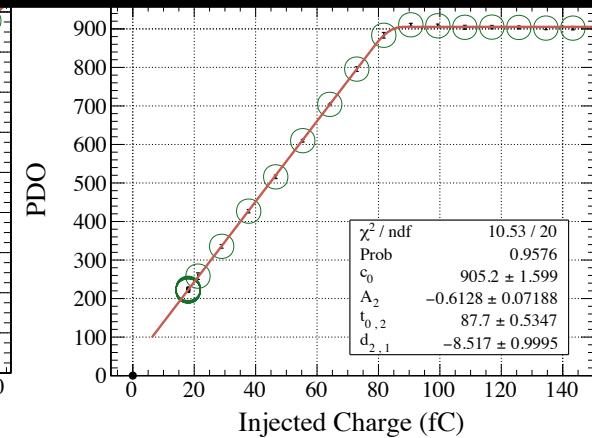
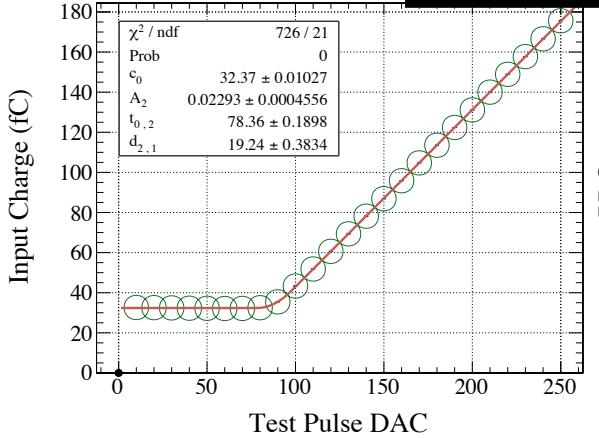
# VMM2 Calibration

## Example calibration plots

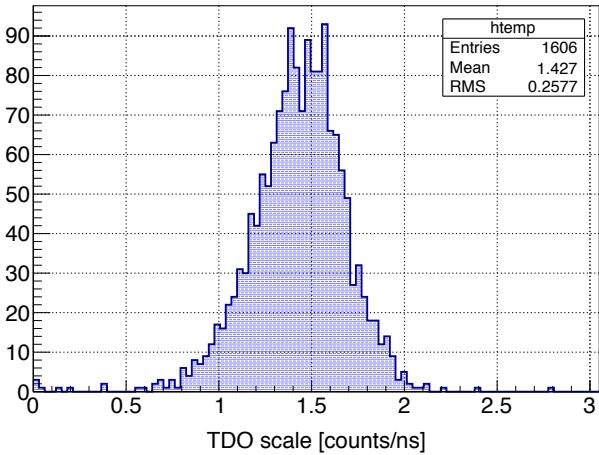
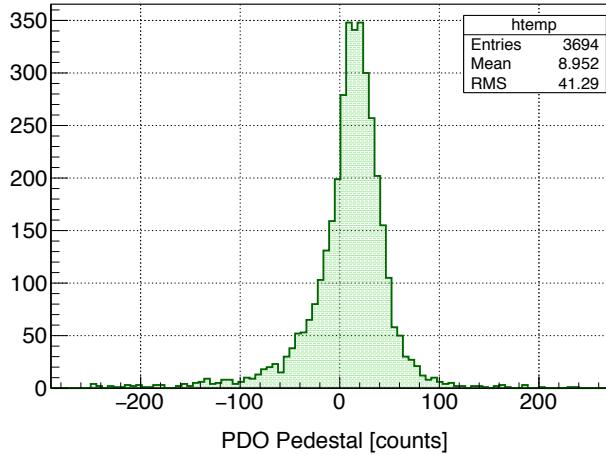
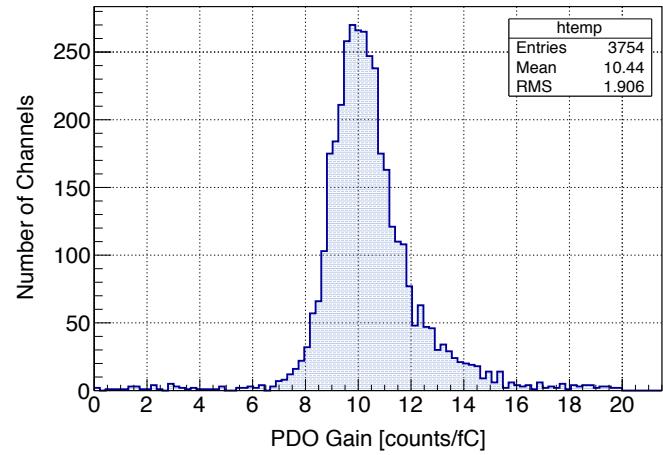
ATLAS Internal - MMFE8+VMM2 Board #111, VMM #1 , CH #60



ATLAS Internal - MMFE8+VMM2 Board #111

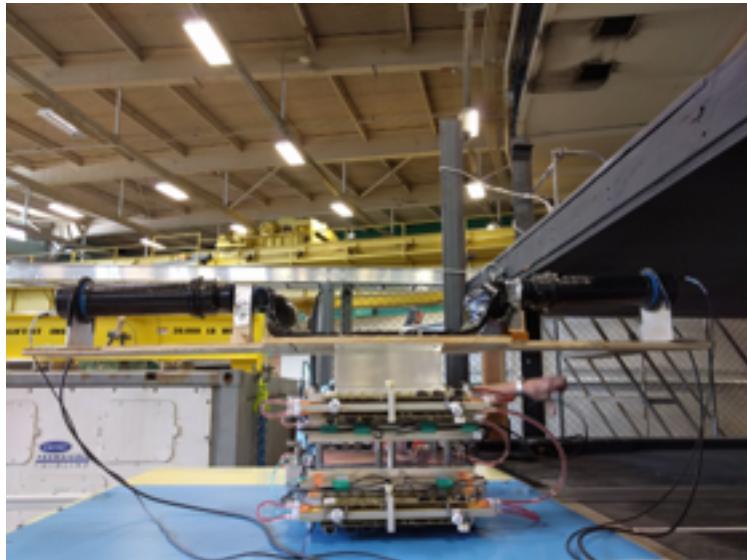
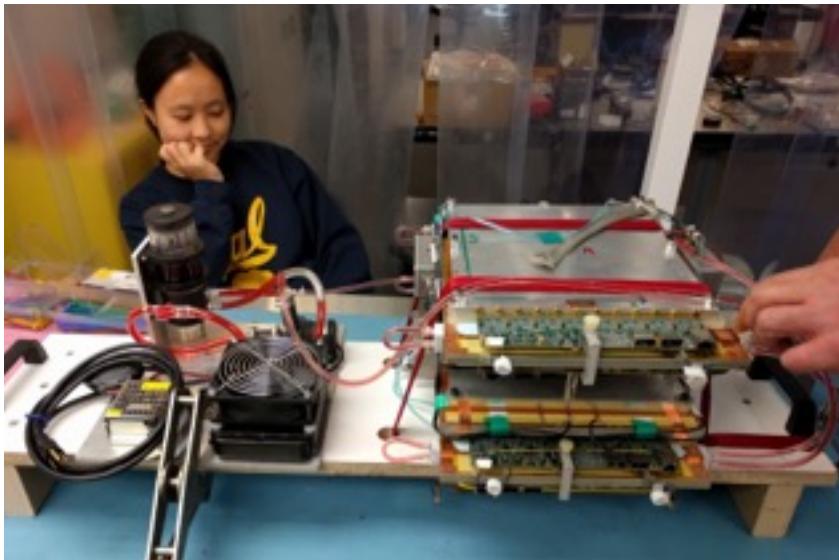


channel-by-channel calibration factors (see backup for more details)





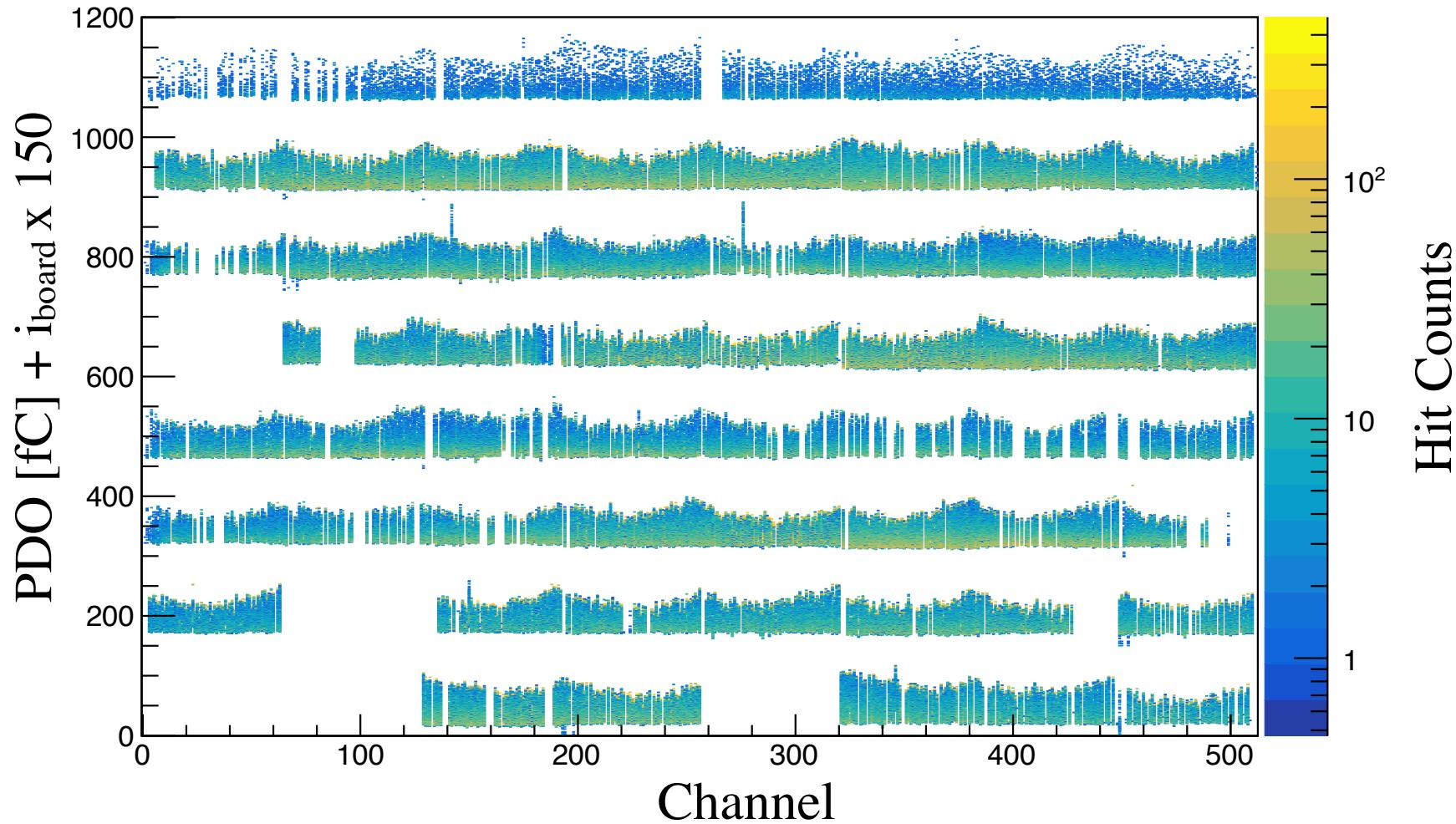
# From bench to test-stand



- Data-taking in test-stand since mid-August
- > 1 M events recorded

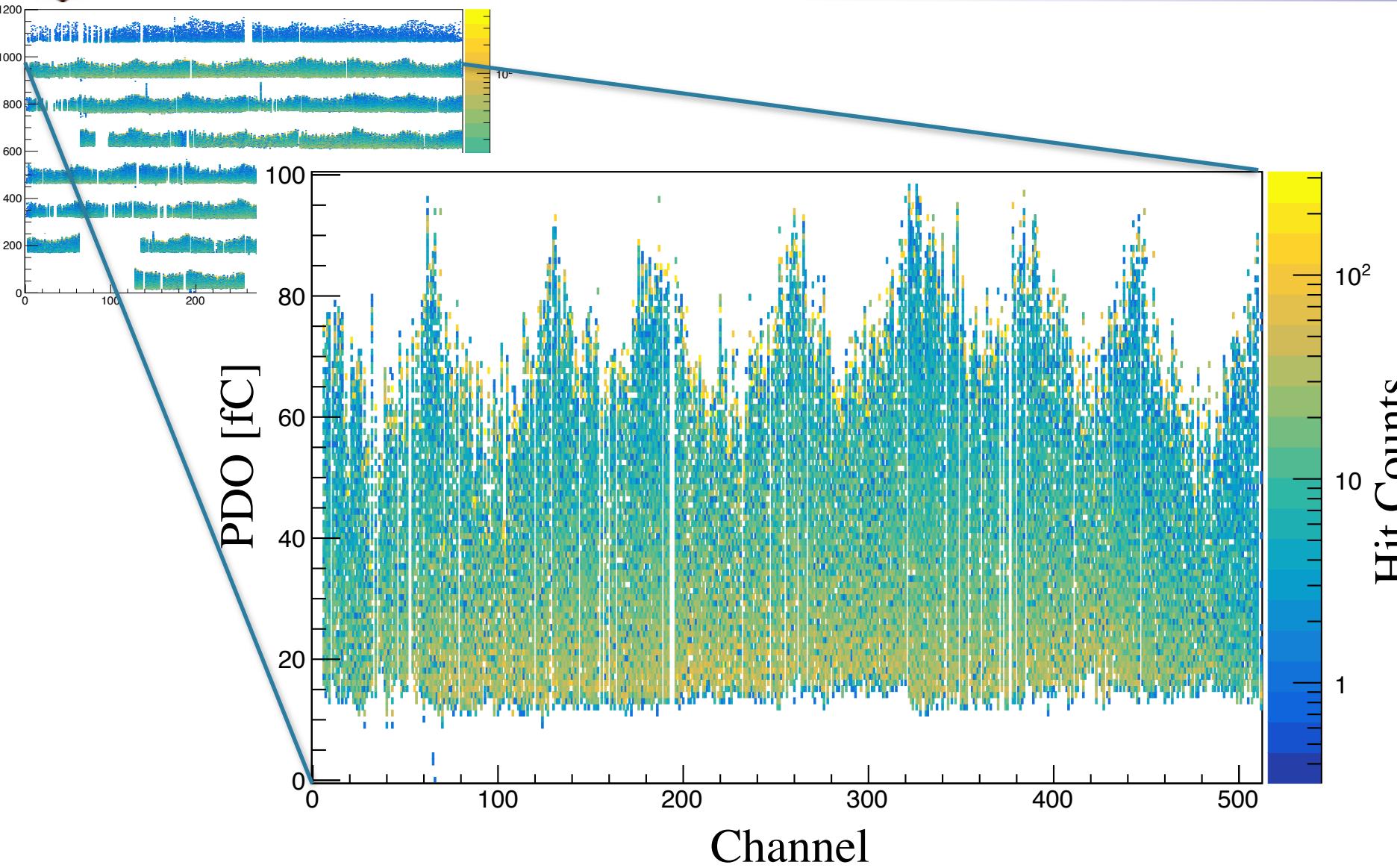
# Preliminary data taking

- Running w/ Drift Voltage = -250 V, Resistive strips = +540-570 V, gain @ 9 mV/fC, peaktime 200 ns, varying thresholds



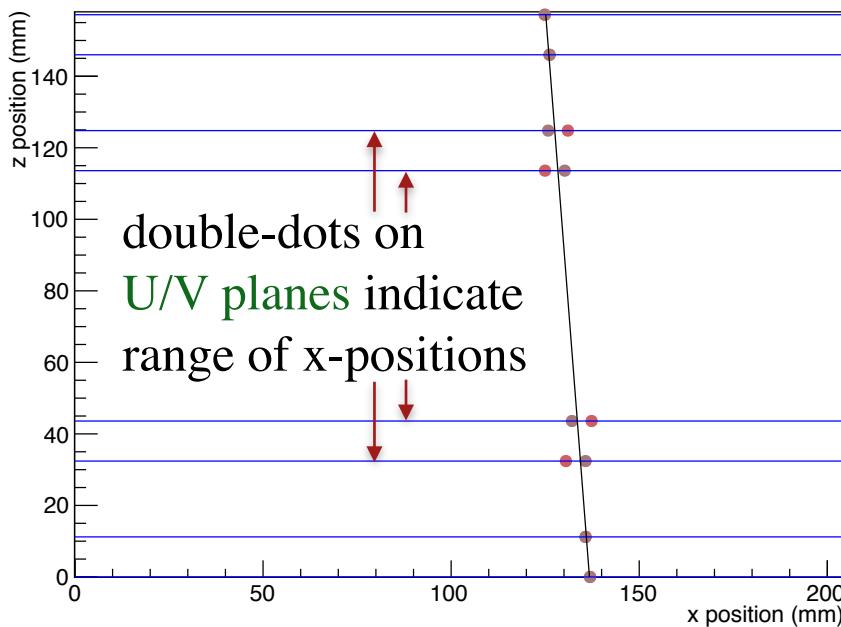


# Preliminary data taking



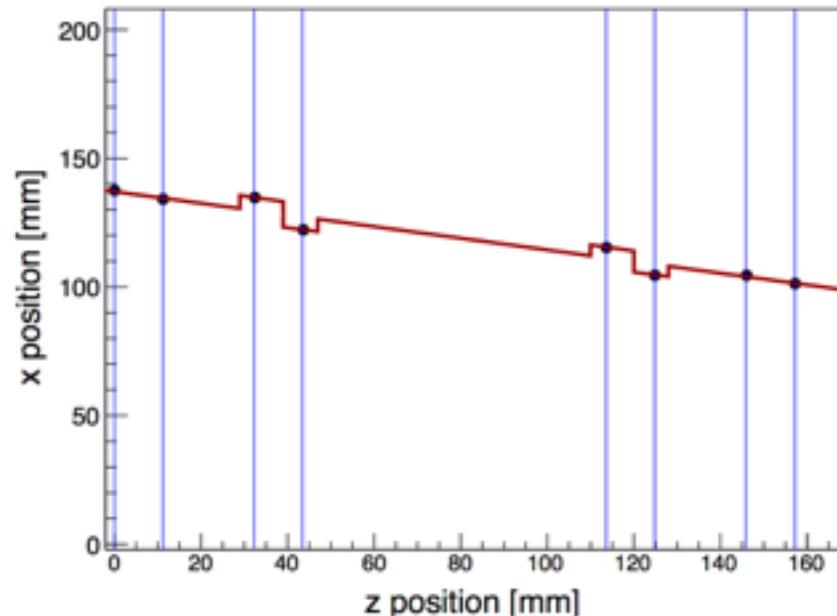


# Preliminary data taking



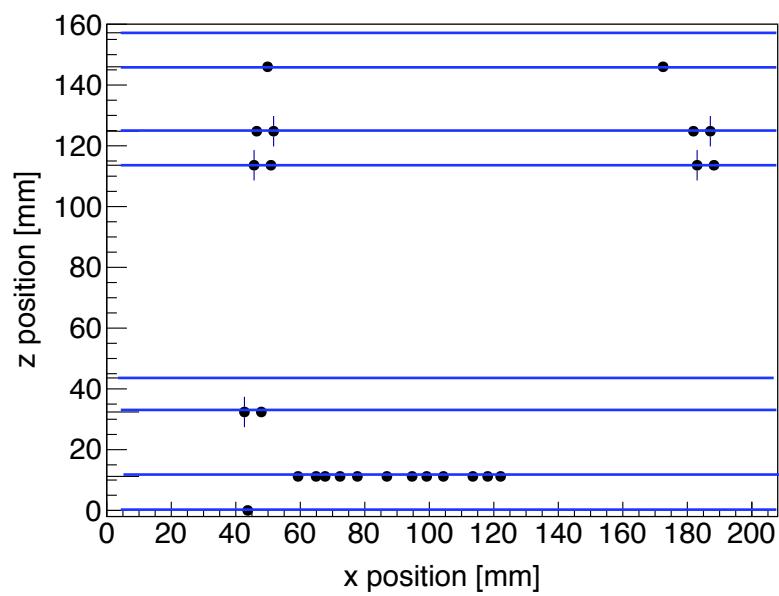
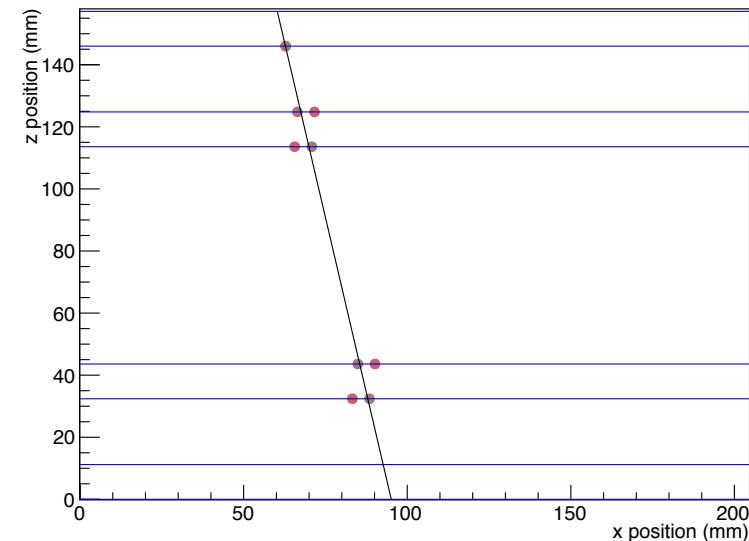
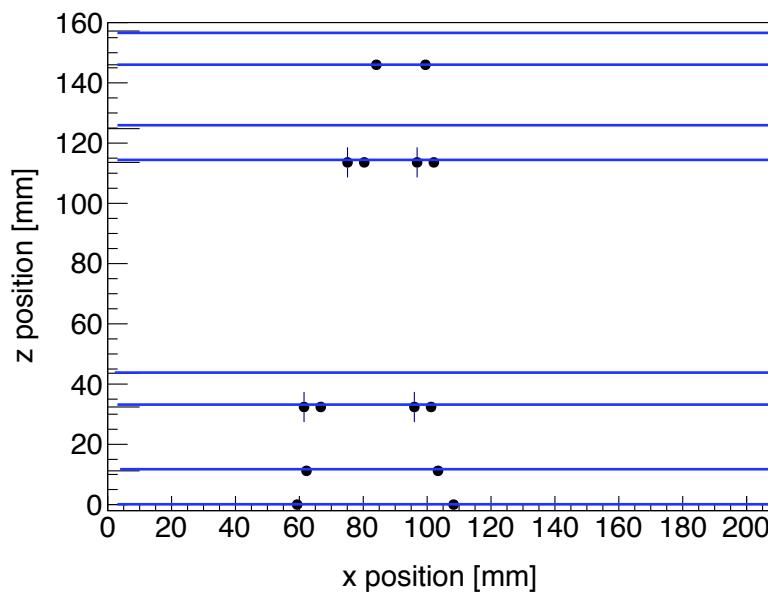
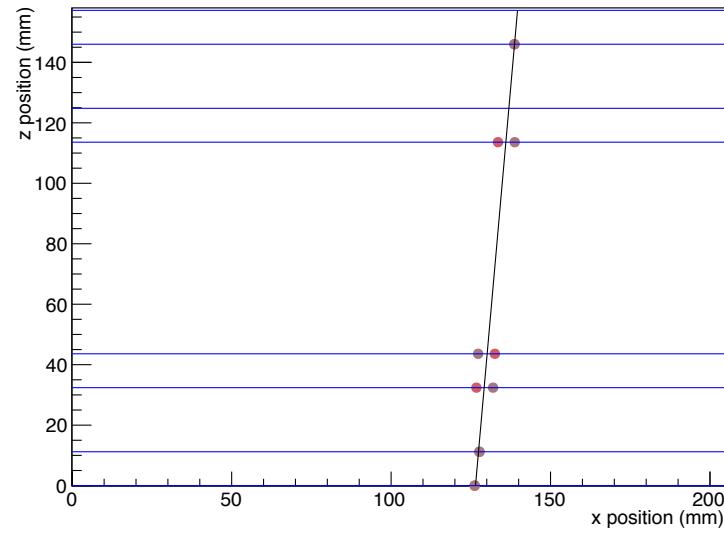
Here, explicitly showing  
x-dependence on “y”-coordinate  
(parallel to electrodes) in U/V planes

- Pacman clustering algorithm applied to MM hits on each board
- Highest charge cluster on each board used in track fit





# Preliminary data taking



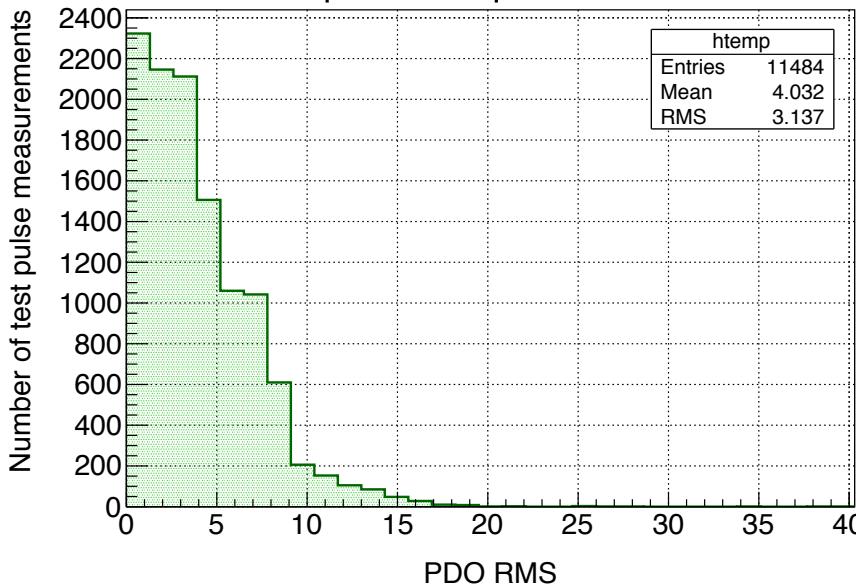


# Open Issues

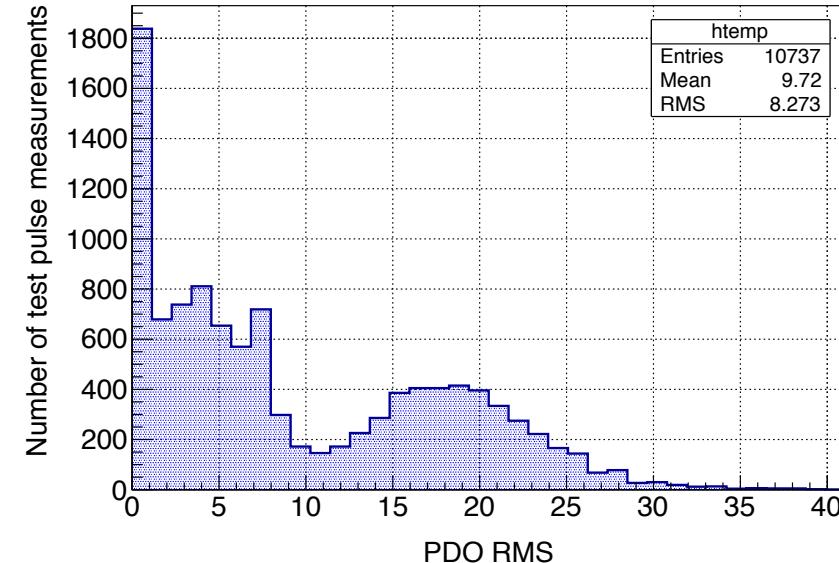
# Observed Noise

- Have tested 10+ boards **on the bench**, and have observed **no noise**
- After putting MMFE8 boards into a chamber noticed a **large increase in noise**
- Identifiable by running the automated calibration routine and observing large increases in PDO measurement RMS:

Example of quiet board



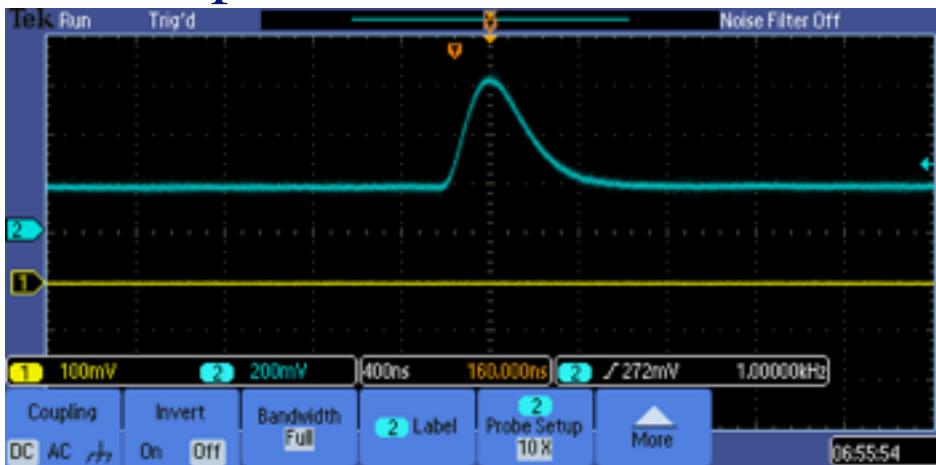
Example of noisy board



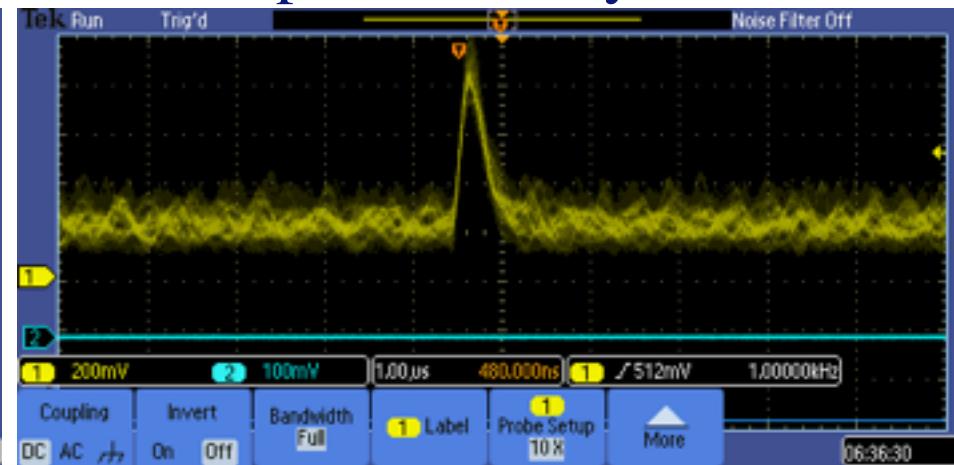


## Noise on monitor output

example of a noise-less channel



example of a noisy channel



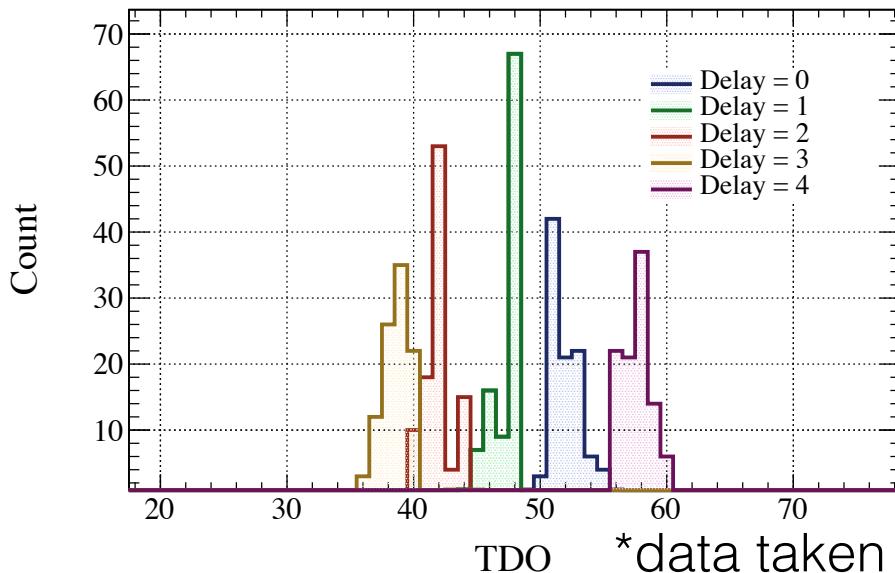
- Up to  $\sim 200$  mV of noise @  $\sim 1.2$  MHz
- Increased noise with more boards in chamber contact and powered
- Large variations between VMM's and even between channels on VMM
- See backup slides for detailed discussion of noise characterization, investigations, and other studies



## Noise effects on TDO

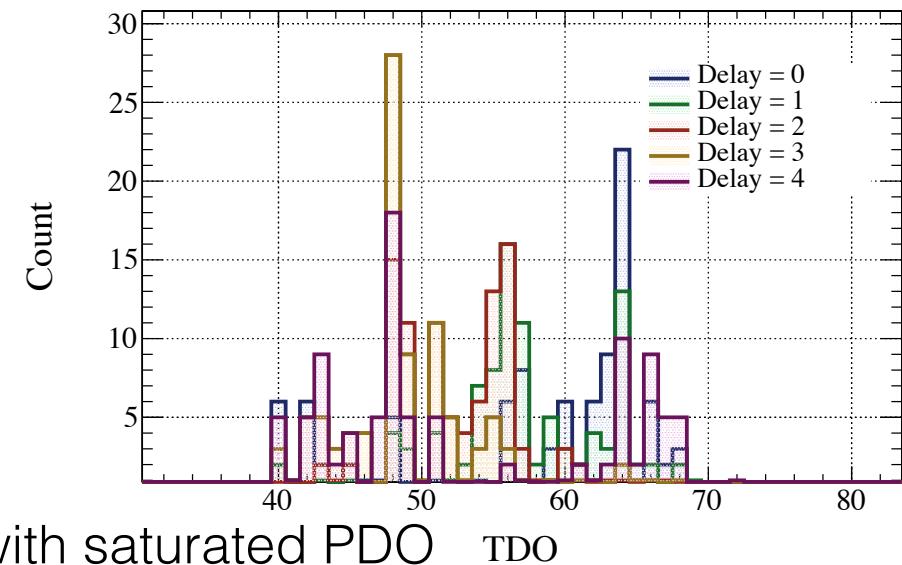
noise-less channel

ATLAS Internal - MMFE8+VMM2 Board #105, VMM #4 , CH #22



noisy channel

ATLAS Internal - MMFE8+VMM2 Board #105, VMM #4 , CH #31

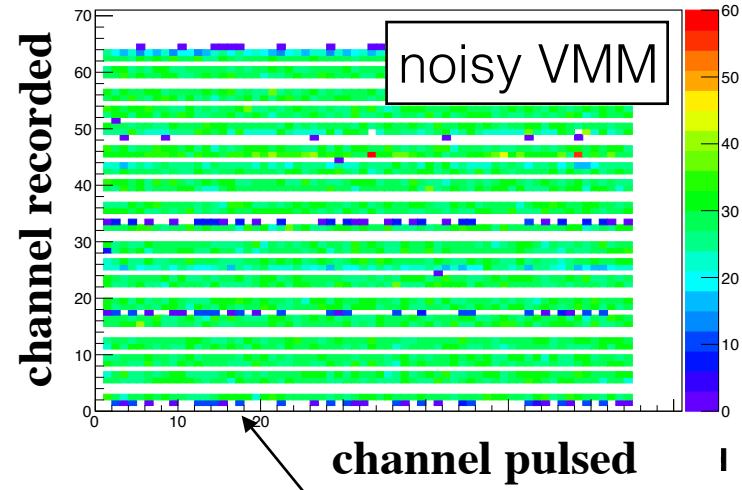
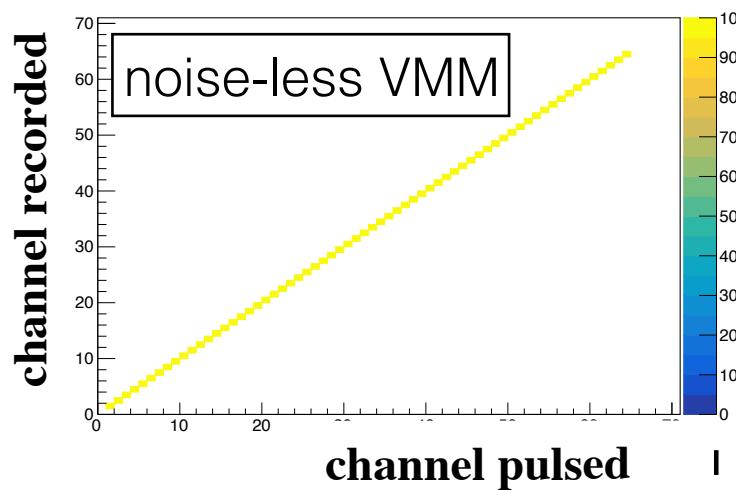


- For noisy channels, unable to resolve 5 ns shifts in TDO applied for time calibration
  - $\Rightarrow$  Unable to determine time calibration parameters for these channels
  - $\Rightarrow$  TDO measurement is generally poor
- Currently, we are mitigating noise effects by running at a high threshold and using only the PDO (amplitude) data



# Noise Pattern

- On boards analogue, digital, and power supply grounds are all the same (different from original design)
- With board pressed against zebra, these grounds are connected to octuplet cage, which is connected to chamber mesh and HV ground  
⇒ Don't know which ground is returning which current  
(ex. 10-15 mV / board voltage increase between top/bottom of quadruplet)



- We observe that a pair of noisy channels on a VMM alternate with a pair of adjacent noiseless channels (upper right plot)
- Adjacent pairs of VMM inputs lie on opposite sides of board
- We look forward to verification of this observation

Here, it is so noisy that we don't get any data from the channel being pulsed, the FIFO is filled by noisy channels.

# High Voltage Issues

- After turning on HV for the first time on the **octuplet**, we lost a large number of channels on several **RevD cards**  
⇒ lost ~1000 channels in ~4000!
- See backup for more details of HV studies.  
**Currently, not observing additional lost channels**
- Investigating protective diodes revealed clamping @ 8.5-9.5 V
- According to Gianluigi, the SOA of the VMM FET is 2 V DC, but a transient of 1.6 V for 20s can seriously damage the FET (estimate, SOA likely has distribution)
- Measured voltage on top of the zebras during ramping  
⇒ ~2 V for a HV ramping speed of 50 V/s
- **Conclusion:** need additional protection for VMM  
⇒ currently under expert discussion

# Zebra Connector Studies

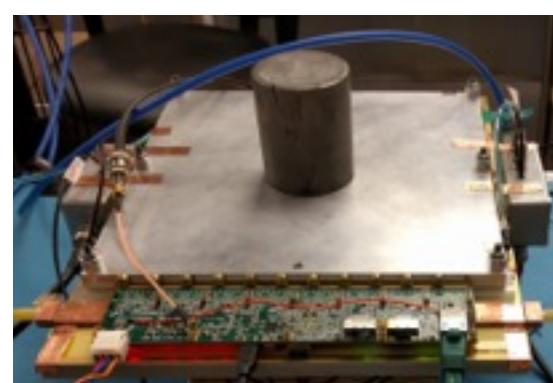
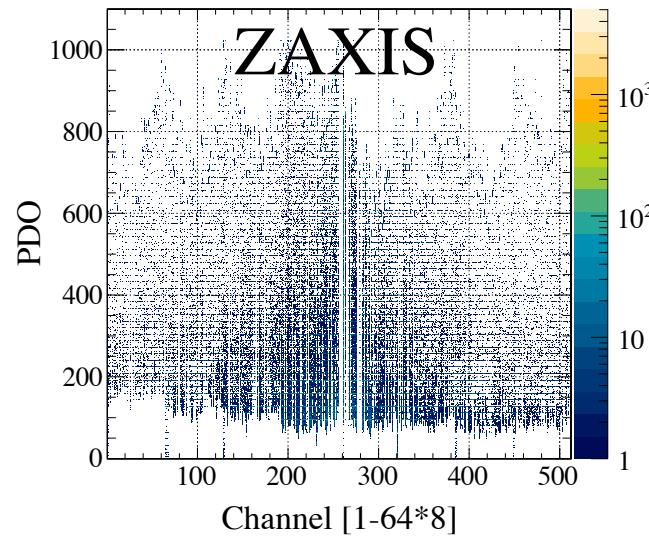
ZAXIS zebra connector

FUJIPOLY zebra connector



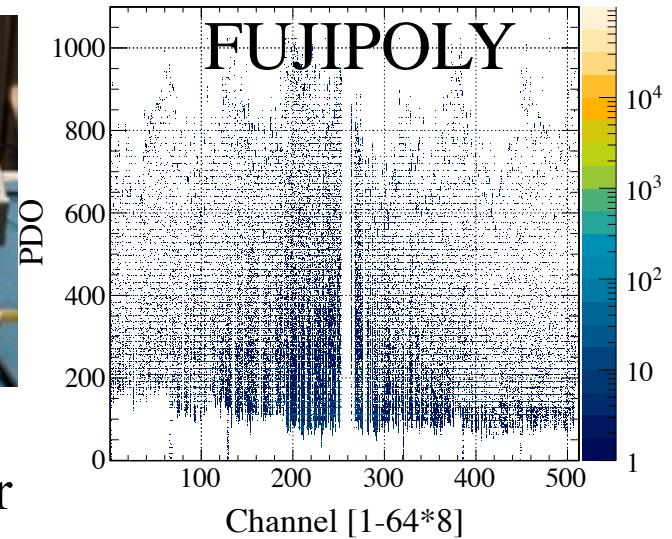
- Performed bench tests on a single chamber comparing ZAXIS zebra connector (what we are currently using) with FUJIPOLY
- Examined channel yields with Fe-55 source on center of chamber

ATLAS Internal - MMFE8+VMM2 Harvard chamber Run 5



Fe-55 source placed  
near center of chamber

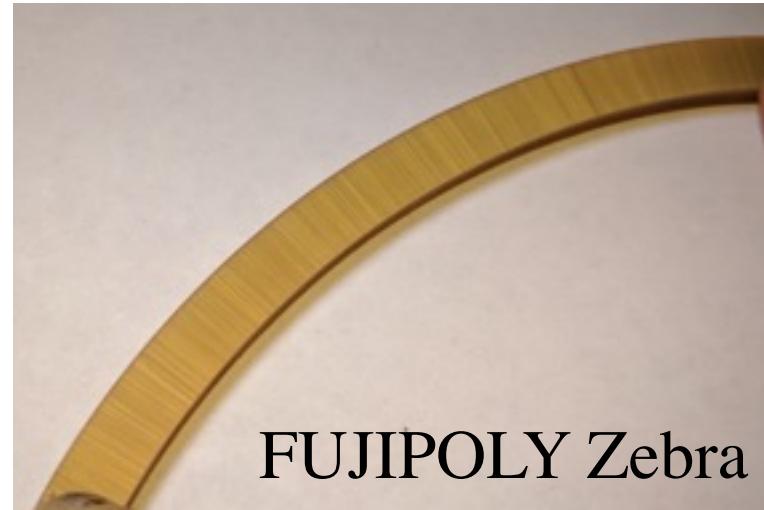
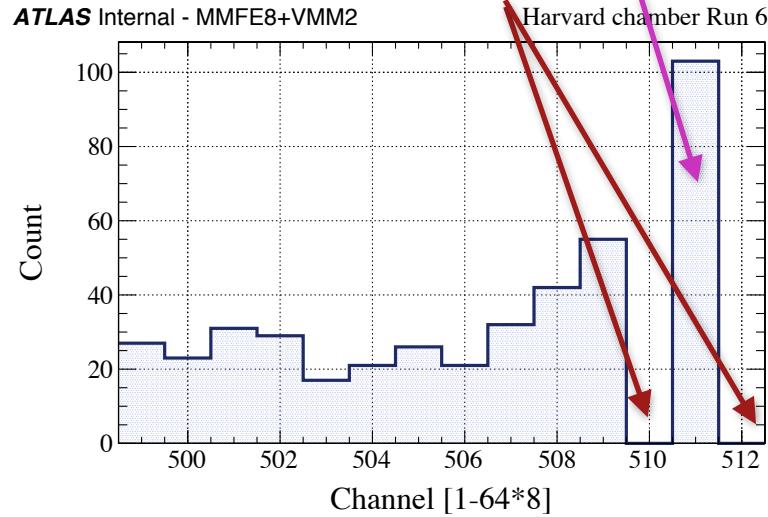
ATLAS Internal - MMFE8+VMM2 Harvard chamber Run 6



- Observed missing and ringing/noisy channels FUJIPOLY



Zoomed plot for missing/noisy channels for FUJIPOLY Zebra

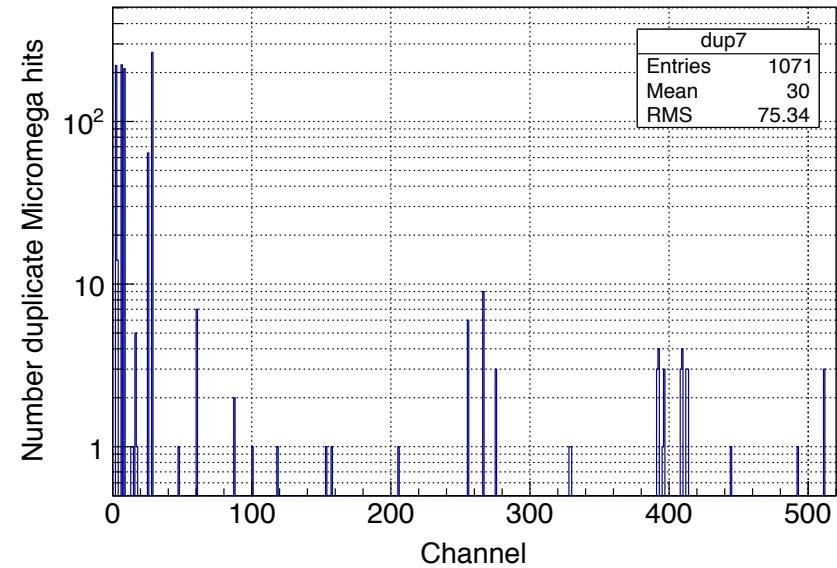
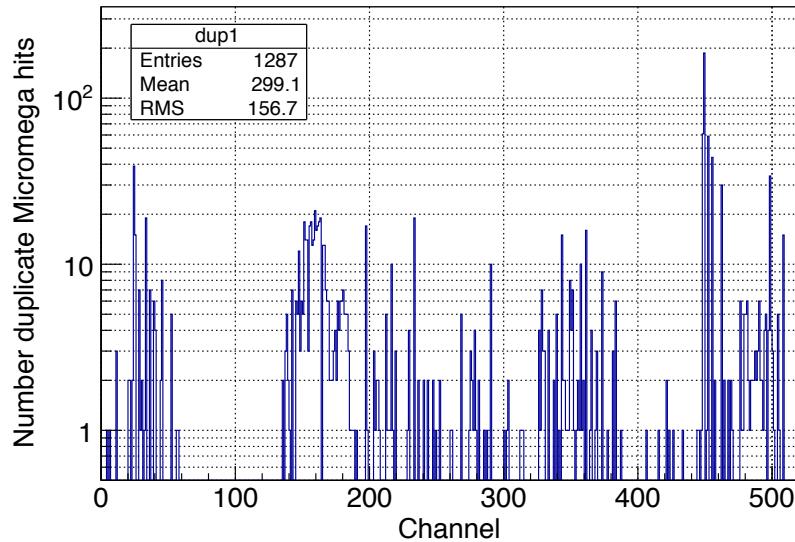


FUJIPOLY Zebra

- After Theo's investigations, we have verified that shorting channel inputs can cause missing/oscillating channels (recovered with removal of short)
- Due to malleability of FUJIPOLY zebra, compressing connector into contact with board appears to produces these shorts (often near the end of zebra connector)
- May want to review zebra connector choice

# Duplicate Events

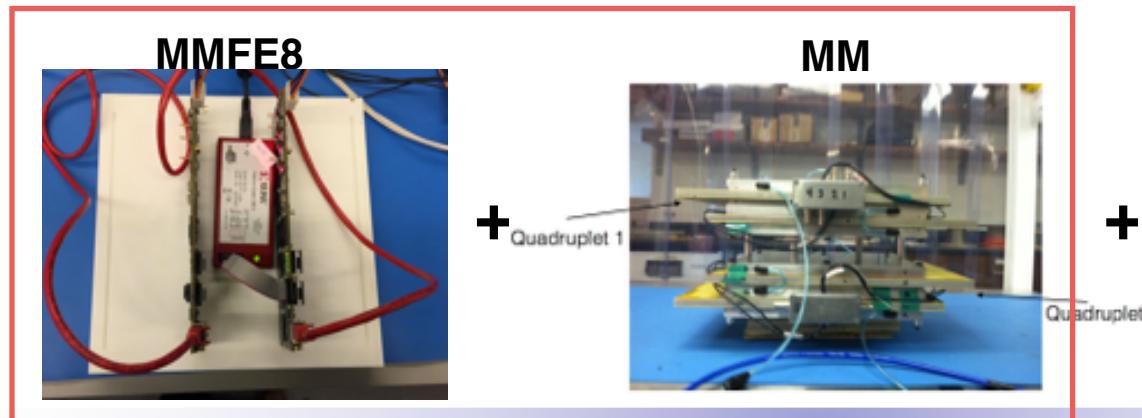
- Still observing duplicate events in data (two example boards below):



- Previous sources of duplicates were mitigated with:
  - soft resets  $\Rightarrow$  prevents token logic from sticking
  - enabling CKTK only after data received  
 $\Rightarrow$  no token reading during data writing
  - with these changes VMM2 is emulating VMM3 in these respects
- Remaining duplicate source still under investigation

# Outlook

- We have an integrated setup of MMFE8 boards and the Micromega octuplet with the cosmic ray test stand  
⇒ smooth data-taking for over a month
- Continuing data-taking/analysis for another ~week
- Work to incorporate ADDC and the trigger processor in test-stand to test the trigger system ongoing now

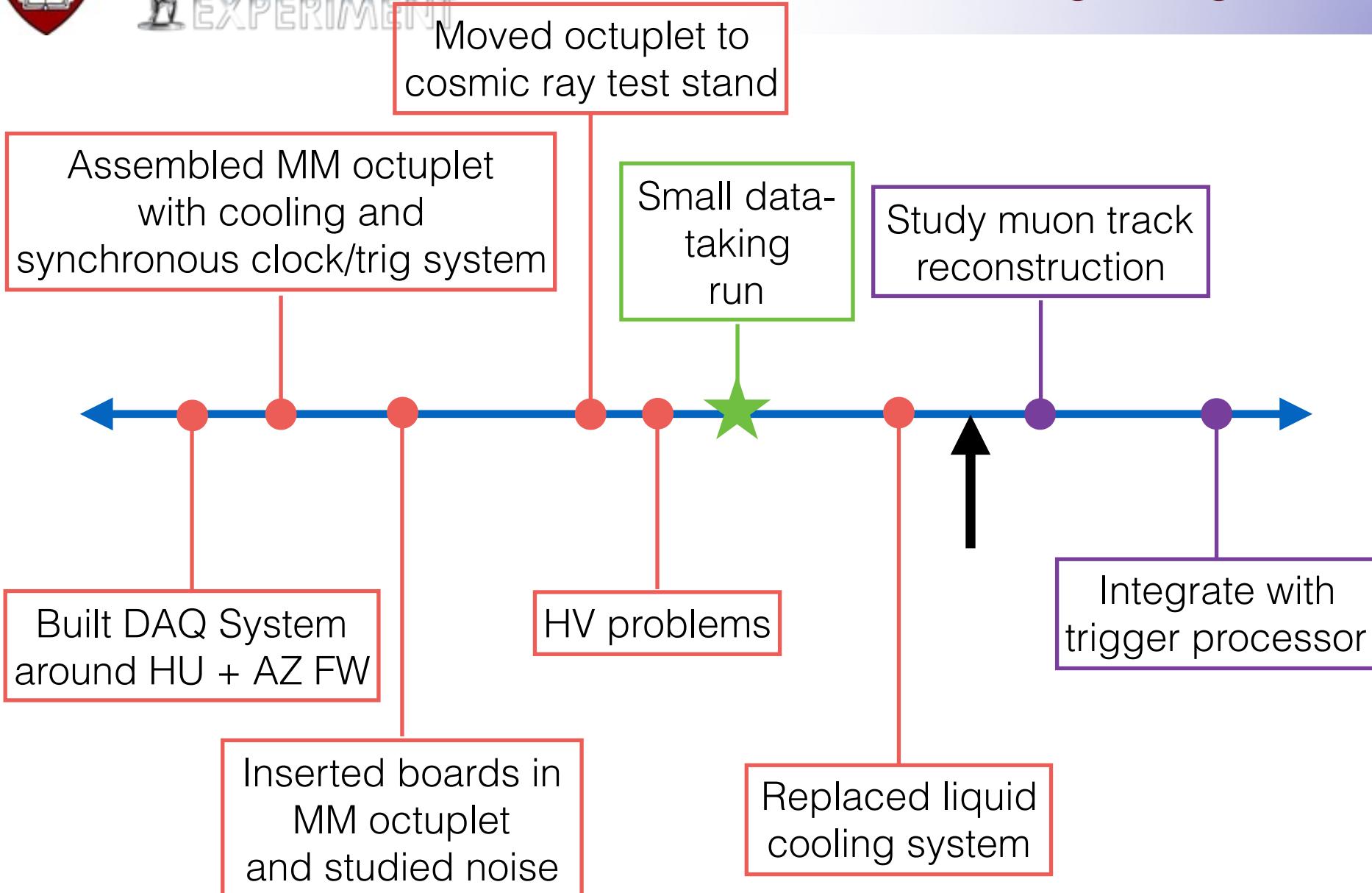




# Backup Slides



# Timeline

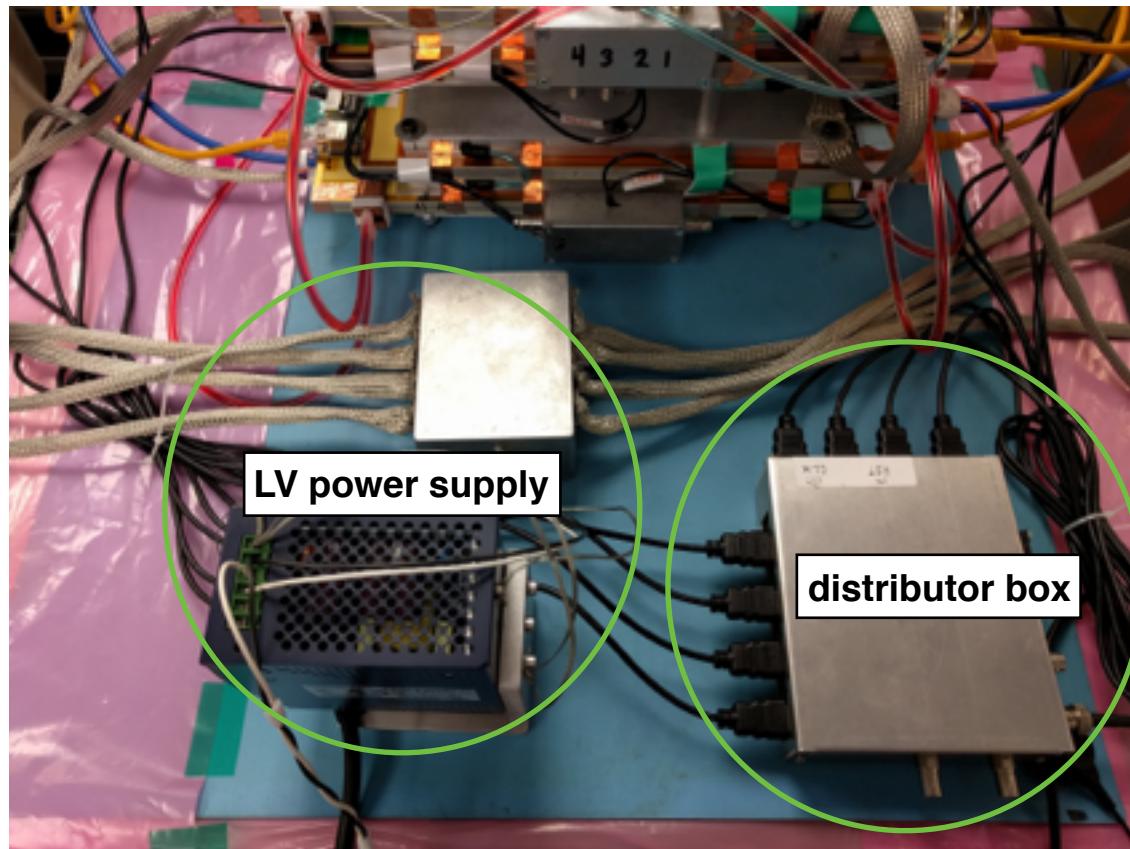


- We prepared a python script to write the MMFE8 data to a file:
  - It checks one board continuously for an FPGA bit set by the external trigger
  - If the bit is high, it reads out FIFO of all 8 boards in sequence through ethernet
  - Firmware allots 100 ms for reading out, which is enough time to read ~50 events per board



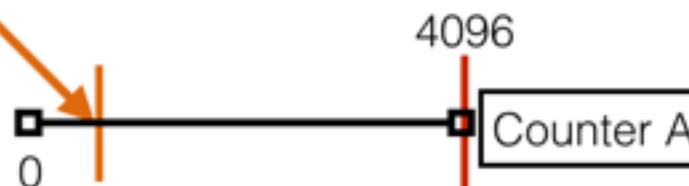
# Clock and trigger distributor

- Distributor box (designed by undergrads M. Bledsoe & J. Grotto) relays an external trigger signal and a 40 MHz clock to 8 MMFE8 boards through a HDMI →microHDMI cable
- Use J8 HDMI input on MMFE8 board (J7 connects to an FPGA port that isn't suitable for a clock input)





Ext Trig

**(1) External Trigger**

- (1) Stop CKBC, inhibit Ext Trig, enable CKTK
- (2) Wait  $\Delta t$  to drain VMM FIFOs
- (3) Set reg signaling that trigger happened, wait 100 ms for data readout
- (4) Soft Reset, disable CKTK
- (5) Start CKBC, allow Ext Trig

microblaze



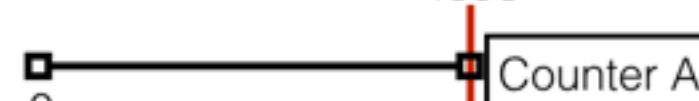
if 1 then GUI  
pulls data  
from FPGA

2 counters  
+ FIFO content

GUI

- (1) Stop CKBC
- (2) Soft Reset
- (3) Start CKBC

4096

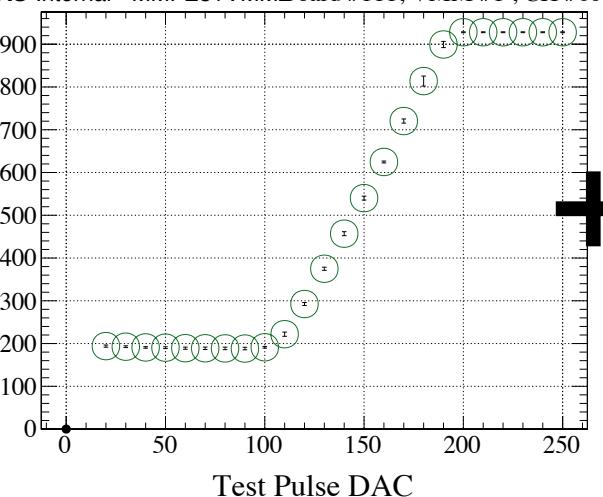
**(2) No External Trigger**



# VMM2 Calibration

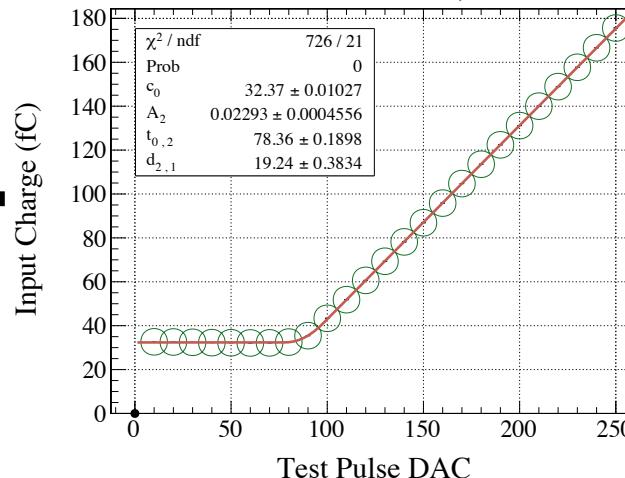
amplitude  
calibration

PDO



PDO response measured  
as a function of test pulse  
DAC for each channel

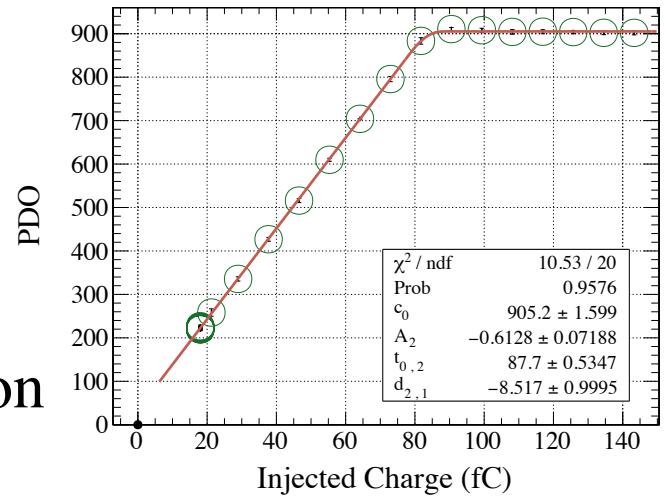
ATLAS Internal - MMFE8+VMMBoard #111, VMM #3



xADC calibration  
for each VMM  
using FPGA ADC

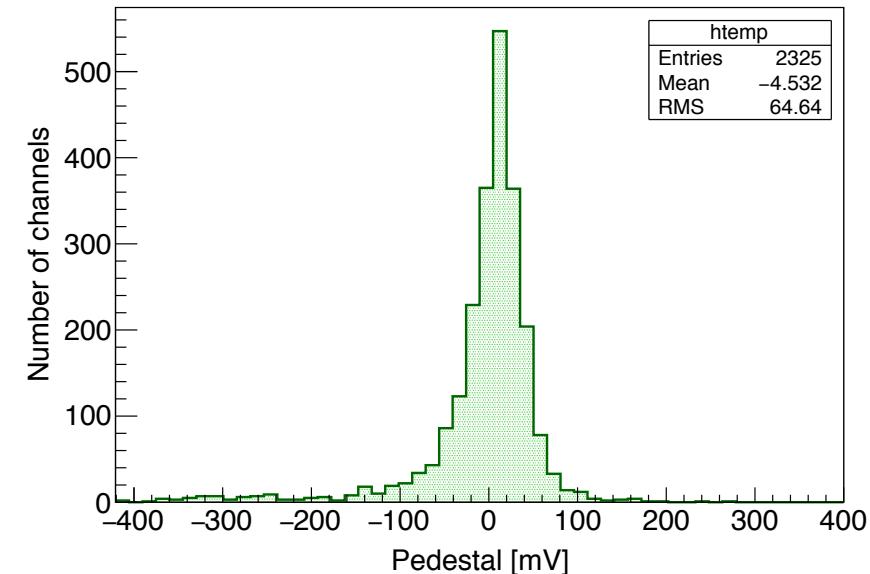
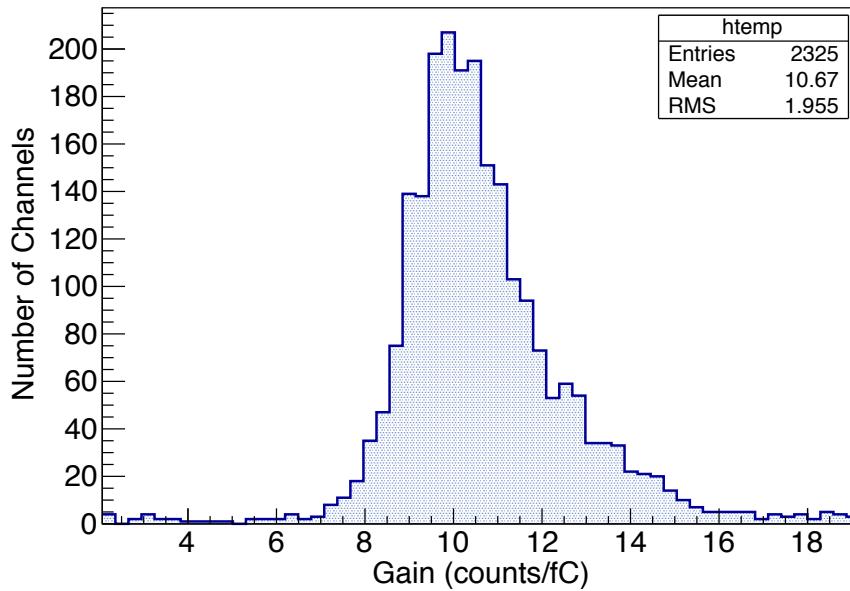
=

ATLAS Internal - MMFE8+VMMBoard #111, VMM #1 , CH #9



Combining measurements give  
channel-by-channel PDO calibration

# VMM2 Calibration



**Channel-by-channel amplitude calibration**  
 (run in 9 mV/fC gain setting)

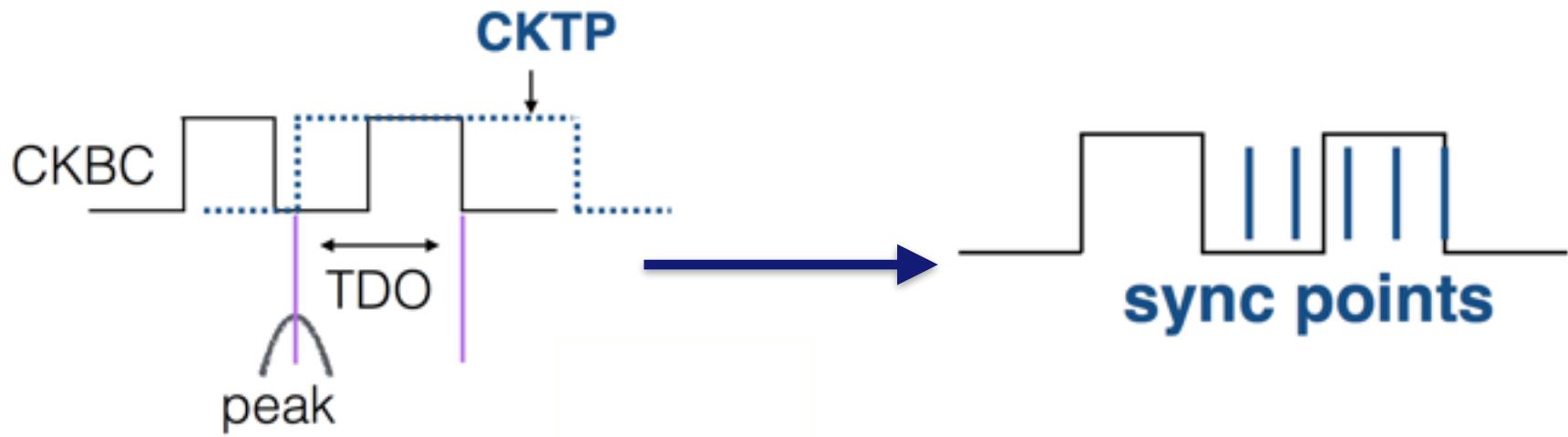


# TDO calibration

Timing (TDO) measurement calibration through varying timing delay by:

- Synchronizing CKTP to CKBC
- Delaying CKTP relative to CKBC by N “delay counts” on 200 MHz mother clock (5 ns steps)

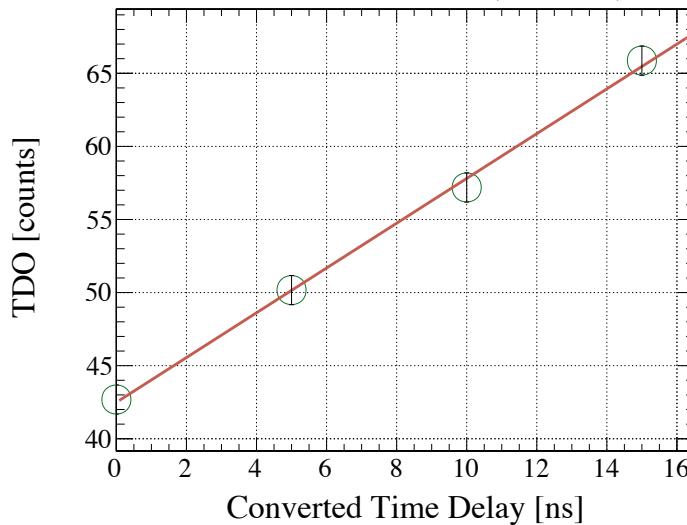
See Ann Wang’s talk for more details:  
[\(https://indico.cern.ch/event/496030/\)](https://indico.cern.ch/event/496030/)





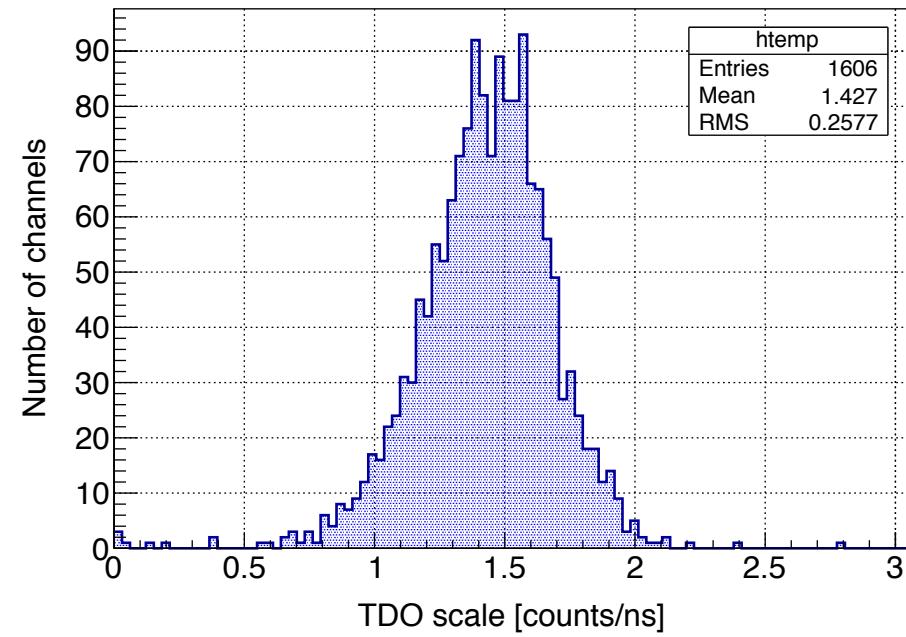
# VMM2 Calibration

ATLAS Internal - MMFE8+VMM2 Board #105, VMM #7 , CH #57



**timing calibration** by varying test pulse phase w.r.t. CKBC  
(see previous slide)  
TDO response measured for each channel

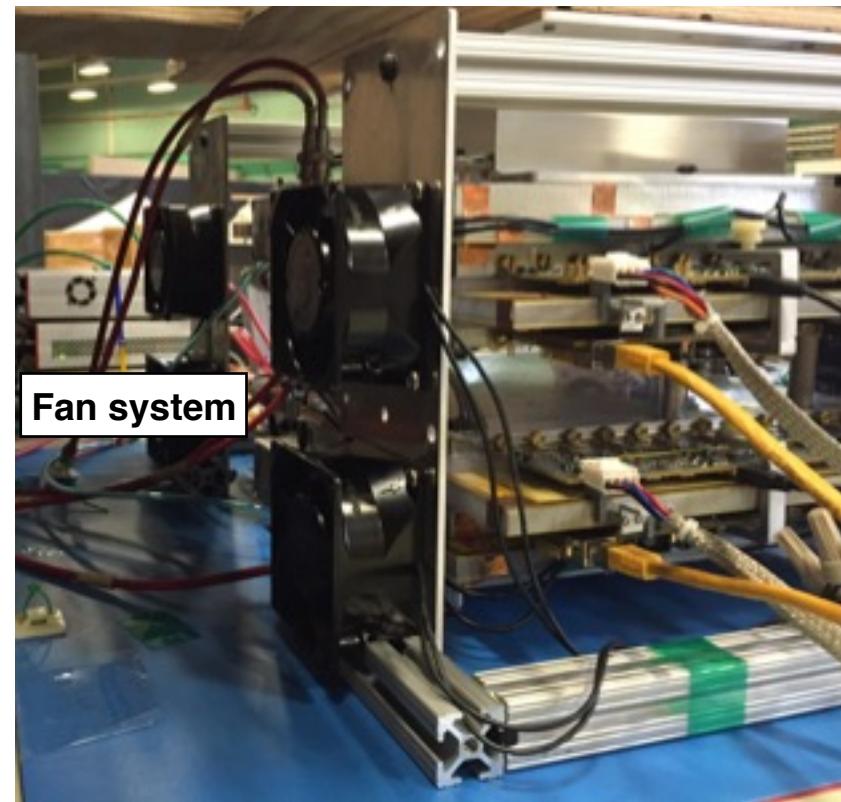
In principle, channel-by-channel TDO calibrations, but TDO measurements with large noise are problematic (see noise discussion in these slides)





## Board cooling

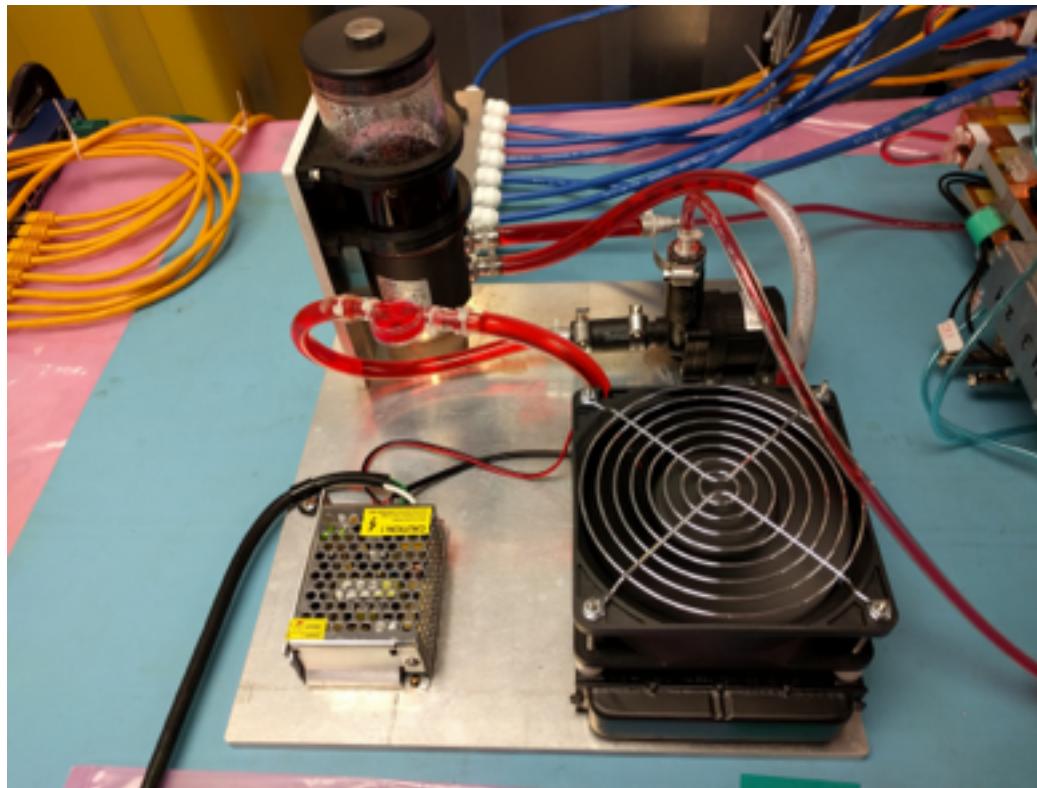
- Currently, 8 large fans mounted next to boards provide cooling
- Original liquid cooling system exhibited leaks



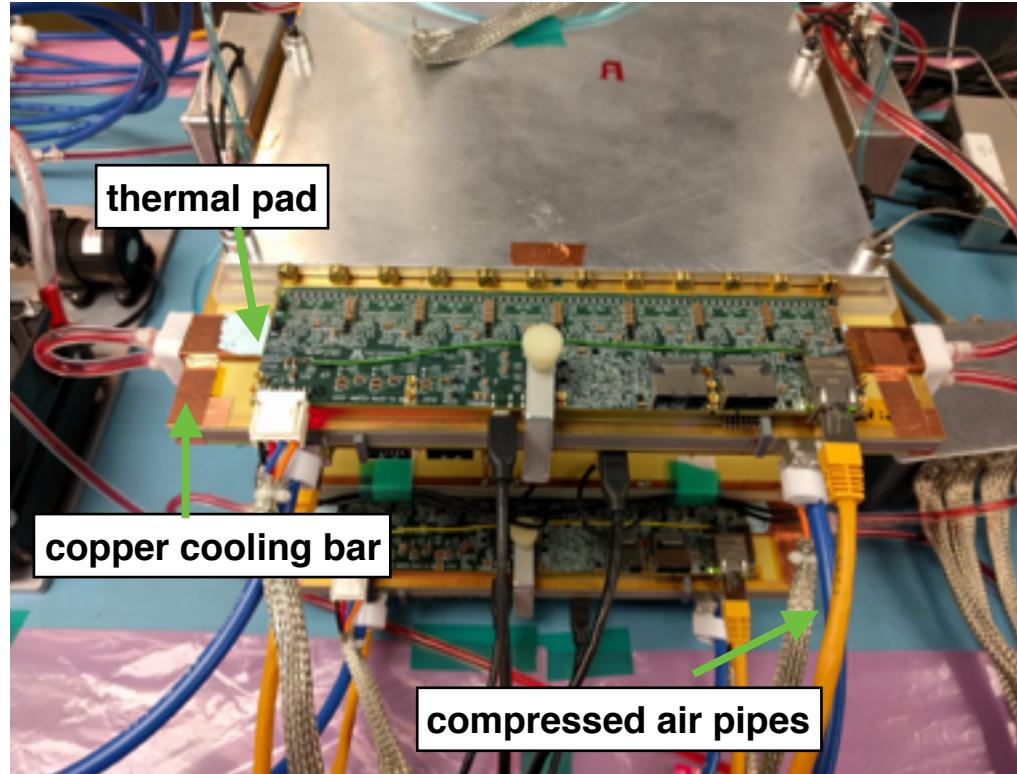


# Cooling System (v0)

- Liquid cooling system to cool the VMMs
- Coolant is pumped through a 4mm thick copper plate, which is thermally connected to the VMMs through a 1 mm silicone pad (compressible to  $\sim 0.5$  mm), heat dissipated through a fan



# Cooling System (v0)



- The heat generated by the DCDC converters isn't well dissipated
- Measured the temperature of the DCDC converter cases to be up to 60 degrees C for a board in the octuplet using a thermistor
- Thus we added compressed air to cool this



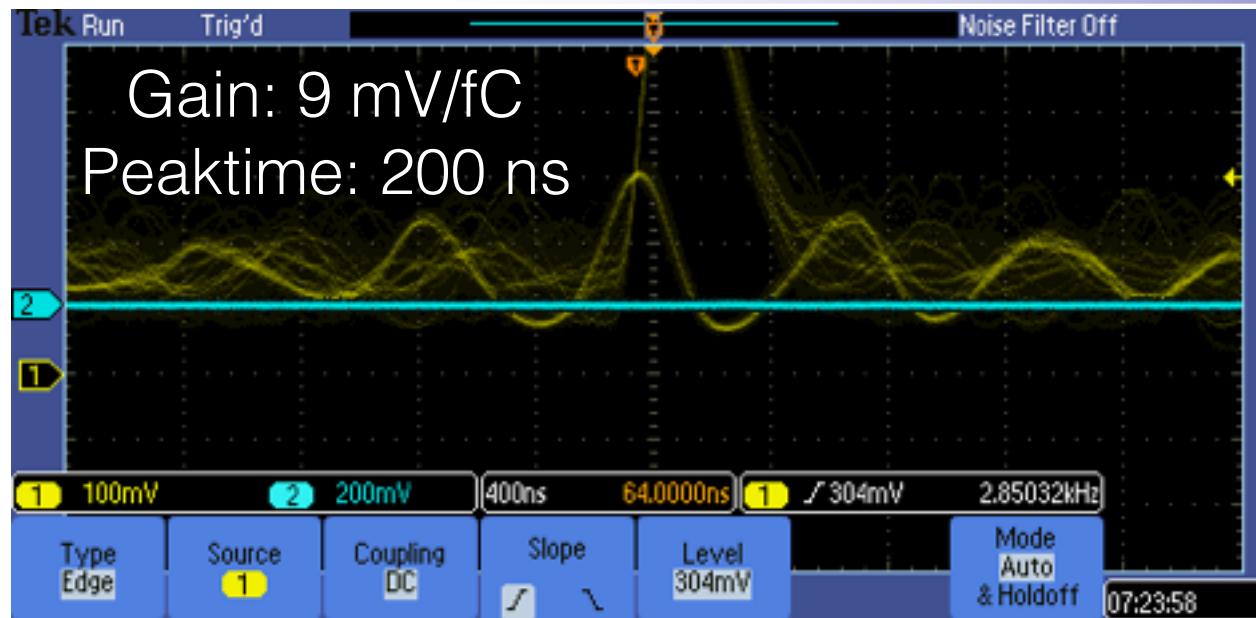
- Miscellaneous lessons from the assembly:
  - >1 ethernet connector broke off, they are weakly attached so we now glue all of them onto the board to reinforce them
  - Our liquid cooling system began to leak, was very fragile in design but we learned some general lessons:
  - Some capacitors on the board are higher than the VMM chip, which resulted in the board having an angle when pushed down on the copper plate
  - Removing the card connected to the copper plate required a significant amount of force and was difficult on the cosmic test stand platform
  - Moving the card also results in small pieces of the silicone pad breaking off and sometimes getting into the zebra area

# Noise issues - Recap

- We have studied noise before, but we have always been working on **small statistics** with poor diagnostics
- With the VMM1 and Mini-1, we studied the boards on the bench and connected to a chamber ⇒ noise was negligible in both cases
- Then, G. Iakovidis and S. Jones reported noise when they put a MMFE8 board in the chamber
- We tested a MMFE8 RevC board with 2 working VMMs inside the chamber last year ⇒ we saw noise at first, but disappeared after fortifying the zebra holder to improve contact
- However, we only looked at a **few** channels with 2 VMMs

# Noise Characterization

- Up to  $\sim 200$  mV of noise above the pedestal
- Main frequency is at  **$\sim 1.2$  MHz**
- Amplitude varies with the VMM gain and peaktimes
- Other signals, such as the threshold or the step pulse on the monitor output, do not exhibit this noise
- Not all VMMs in a board are noisy, and not all channels in a VMM are noisy. Often a noisy channel neighbors a noiseless channel  $\Rightarrow$  appears noise is not on the board, it is an oscillation at the VMM input
- Overall noise level **increases** when we add more MMFE8 boards to the octuplet



# Noise Investigations

- Used a special board to connect a 142C ORTEC charge amplifier to a zebra connector (256 strips)  $\Rightarrow$  did not see this type of noise, which excludes most mundane causes of noise
- Hypothesized the oscillation was induced by the DCDC converters (because they operate at a 1.2 MHz frequency and have a large 100-300 mV ripple). We also noticed that the noisiest VMMs are usually the two closest to the DCDC converter (0 and 1)
- Arizona modified a board for us with reduced ripple and a lower frequency of operation ( $\sim$ 500 kHz)  $\Rightarrow$  This board has the same level of noise and the frequency **is still** 1.2 MHz

# Noise Considerations

- The analog ground, digital ground, and power supply ground of the MMFE8 board are all the same (they were supposed to be separated)
- When pressing the board on the zebra with the cams, the MMFE8 ground is connected to the octuplet cage, which in turn is connected to the chamber mesh and the HV ground
- In this situation we don't know which ground is returning which current
- For example, we measured a difference between the ground of the power supply and the ground of each MMFE8 board
- There is a relative  $\sim$ 10-15 mV increase in voltage going from the top to the bottom board of the octuplet, which means that the 12 V power supply current sent to a board is returned by other boards through the cams and the aluminum frame

# High Voltage Issues

- When we studied the noise on a **MMFE8 RevC board with 2 VMMs** last year, we lost a VMM to HV. We paid no attention because that board lost 5 VMMs in a week just sitting on the bench
- We also tested a **MMFE8 RevC board with 8 VMMs** with HV on the chamber and we didn't notice any channels/VMMs dying, but we did not do a systematic check of all the channels
- After we turned on high voltage for the first time on the **octuplet**, we lost a large number of channels on several **RevD cards**, around  $\sim 1000$  channels in  $\sim 4000$ !

# High Voltage Issues

- After these channels died, we took a closer look the worst affected board
- Input impedance of killed channels is about  $200\ \Omega$ , the impedance of healthy channels is  $\sim 500\ k\Omega$
- To understand whether we zapped the protection diode or the VMM input FET, we took out two VMMs and measured the impedance of the protection diodes
- We found that diodes were not broken. When testing the diodes, we discovered (our ignorance) that they clamp the voltage to 8.5-9.5 V, and many do not clamp the voltage at all
- According to Gianluigi, the SOA of the VMM FET is 2 V DC, but a transient of 1.6 V for 20 s can seriously damage the FET (ballpark estimate and the SOA must have a distribution)

# High Voltage Issues

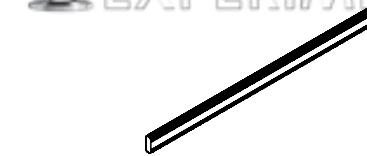
- Based on this information, we performed a number of controlled experiments using the **surviving boards**
- We ramped with various different speeds between 5 V/s and 100 V/s over several days and scanned the channels each time
- We only saw 3 more channels die, this happened first three times we ramped up and down using 5 V/s
- While we ramped up the voltage, we looked at the test pulse on the monitor output. During ramps at  $> 10$  V/s, **test pulse disappears**

# High Voltage Issues

- We also measured the voltage on top of the zebras during ramping, which was about 2 V for a HV ramping speed of 50 V/s
- We replaced the killed boards with three new boards (2 RevC, 1 RevD). Ramping up @ 25 V/s, we lost ~ 10 channels on these three boards
- **Conclusion:** The VMM input is not protected enough, ramping zaps the FETs which are at the tail of the SOA distribution. It remains a mystery why we lost so many channels in four boards, while in the other boards we just lost a few channels



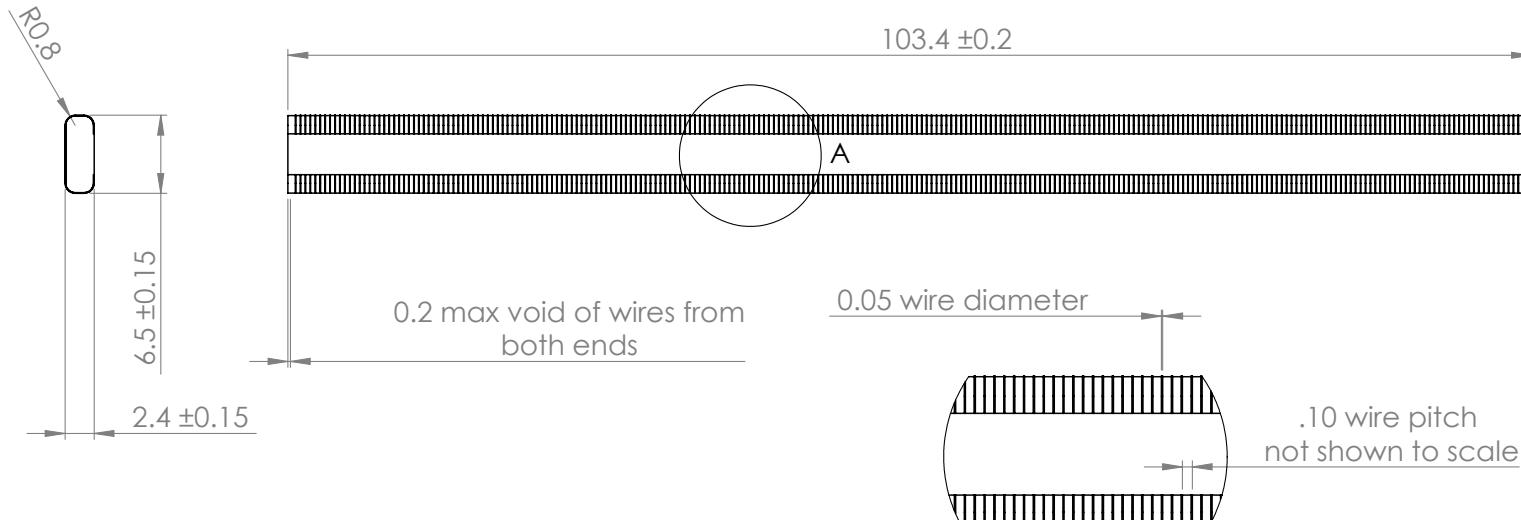
**ATLAS**  
**EXPERIMENT**



# Zebra Connector Specifications

## REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	Changed overall length from 103.3 to 103.8	4/15/2014	MBB
	B	Changed overall length of part from 103.8 to 103.4	4/17/2014	MBB



## Notes:

Core Material:  
Zsil-1

Conductors:  
Material C2  
Plating Z5

Substrate:  
11L

DETAIL A

Z-Axis Connector Co. 345 Ivyland Rd, Warminster PA 18974 267-803-9000	UNLESS OTHERWISE SPECIFIED:	DRAWN CHECKED ENG APPR. MFG APPR. Q.A.	NAME MBB DS DS BH GG	DATE 4/17/2014 4/21/2014 4/21/2014 4/21/2014 4/21/2014	ZAXISCONNECTOR.COM
	DIMENSIONS ARE IN mm TOLERANCES: FRACTIONAL ± n/a ANGULAR: MACH ± 1 BEND ± 1 TWO PLACE DECIMAL ± .25 THREE PLACE DECIMAL ± .127				TITLE: Elastomeric Connector
PROPRIETARY AND CONFIDENTIAL  THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF Z-AXIS CONNECTOR COMPANY. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF Z-AXIS CONNECTOR COMPANY IS PROHIBITED.	INTERPRET GEOMETRIC TOLERANCING PER:	MATERIAL see note	COMMENTS:	SIZE A	DWG. NO. Zwrap-314
	FINISH				REV B
DO NOT SCALE DRAWING		SCALE: 1:2		WEIGHT:	SHEET 1 OF 1

5

4

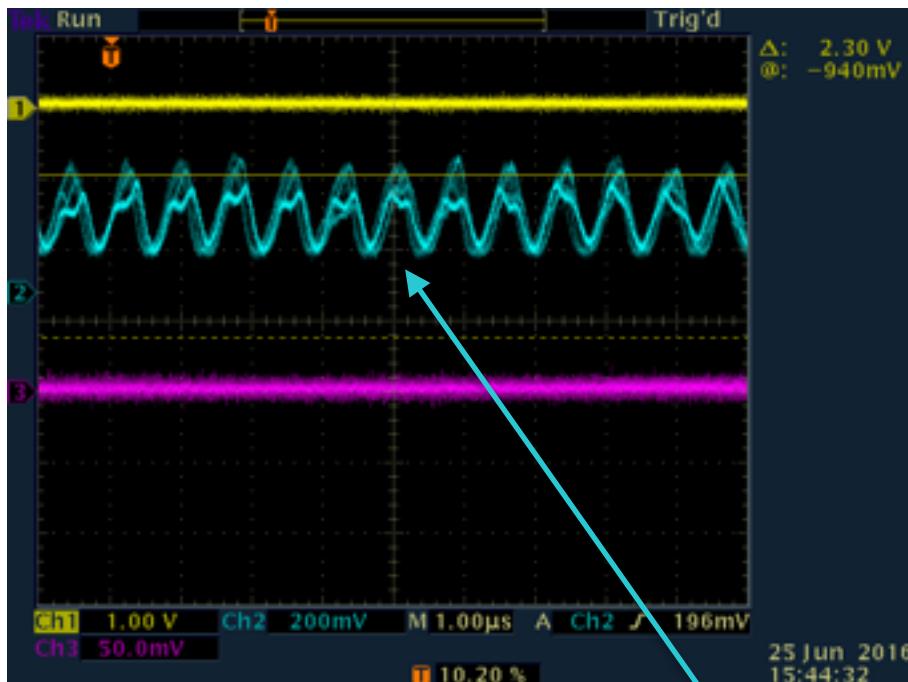
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2

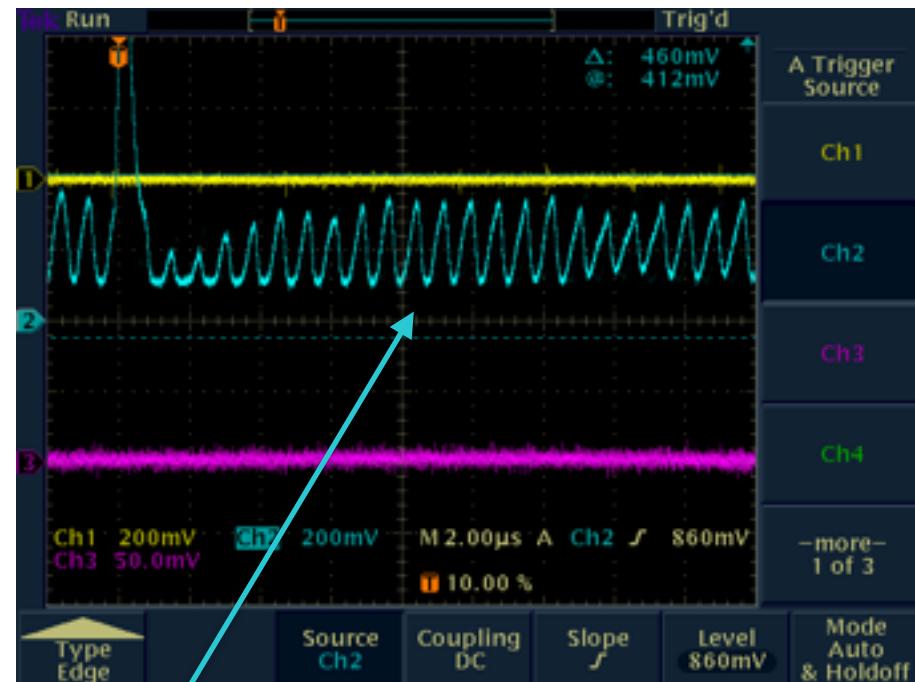
1



VMM 3, channel 62



VMM 3, channel 63



Sometimes noisy channels appeared with FUJI POLY zebra near the end of the connector

In this case, CH 62 & 63 masked on VMM 3