CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

- OD This input signal is open drain.
- TTL This input signal may be at TTL logic levels.
- Z This input may be at High Impedance.
- Z* This input (local to this board) may be at High Impedance.

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Note: the shading patterns below are in colour, and not distinguishable on black & white hard copies.

Circuits in need of improvement are marked like this.

Circuits known to be incorrect are marked like this.

Obsolete sections or circuits are marked like this.

Changes from previous revision are marked like this.

D	Title: front-panel-revF-DEB-board1
	Revision: Rev B
	Last Change: 25 Jun 2016 18:54:00
	Drawn by: Alexios 1/11
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

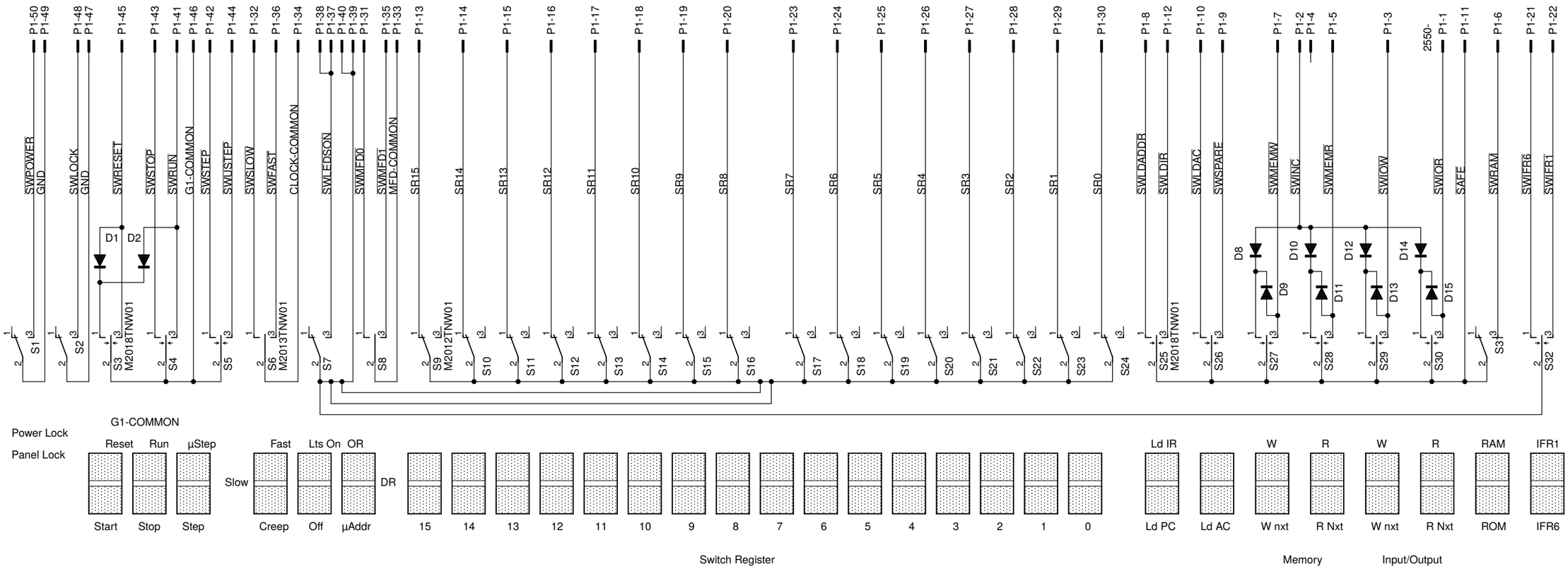
Switch Wiring

Left switch actuation truth table

	SWRESET	SWRUN	SWSTOP	SWSTEP	SWUSTEP
Reset	L				
Start	L	L			
Run		L			
Stop			L		
Step				L	
uStep					L

Right switch actuation truth table

	SWMEMR	SWMEMW	SWIOR	SWIOW	SWINC
Memory Read	L				
Memory Read Next	L	L			L
Memory Write		L			
Memory Write Next			L		L
I/O Read			L		
I/O Read Next				L	L
I/O Write				L	
I/O Write Next					L



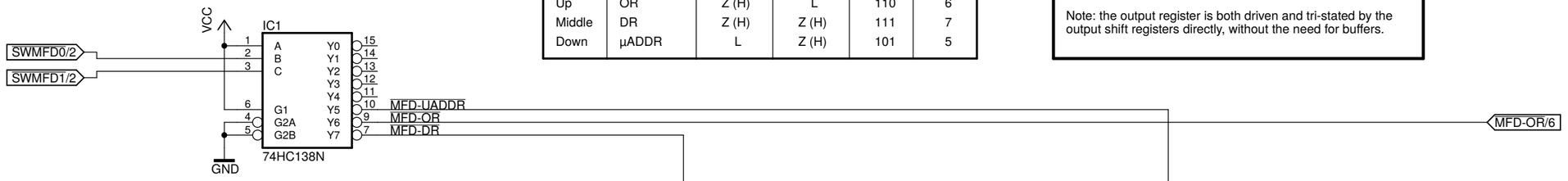
D	Title: front-panel-revF-DEB-board1
	Revision: Rev D
	Last Change: 25 Jun 2016 18:54:00
	Drawn by: Alexios 2/11
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

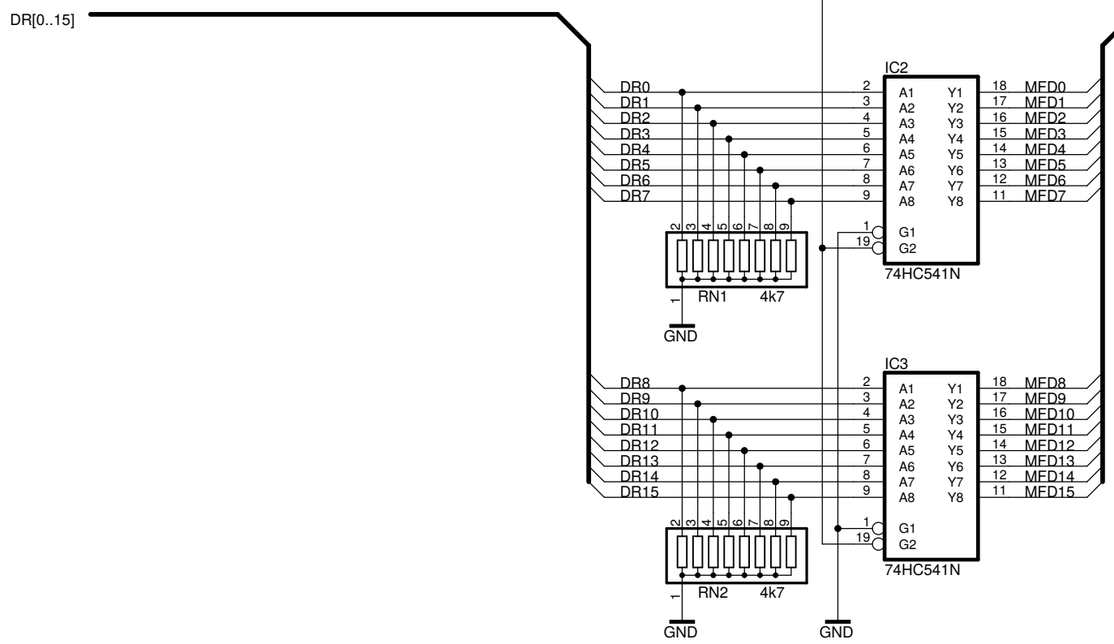
Front Panel: Multi-Function Display

Switch	MFD Shows	$\overline{SWMFD0}$	$\overline{SWMFD1}$	Vector	Output
Up	OR	Z (H)	L	110	6
Middle	DR	Z (H)	Z (H)	111	7
Down	µADDR	L	Z (H)	101	5

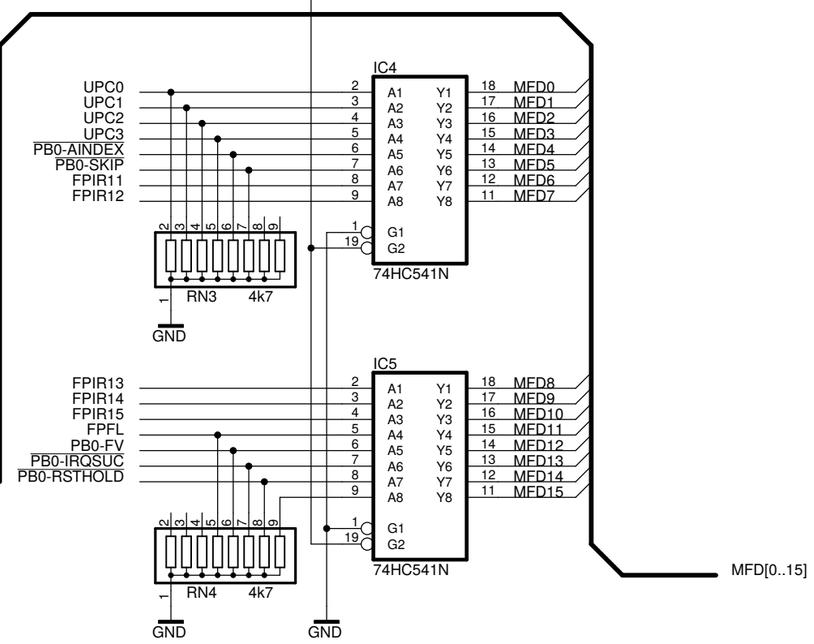
Note: the output register is both driven and tri-stated by the output shift registers directly, without the need for buffers.



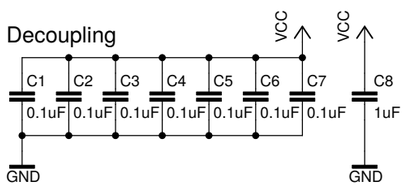
Data Register (DR)



µADDR Vector



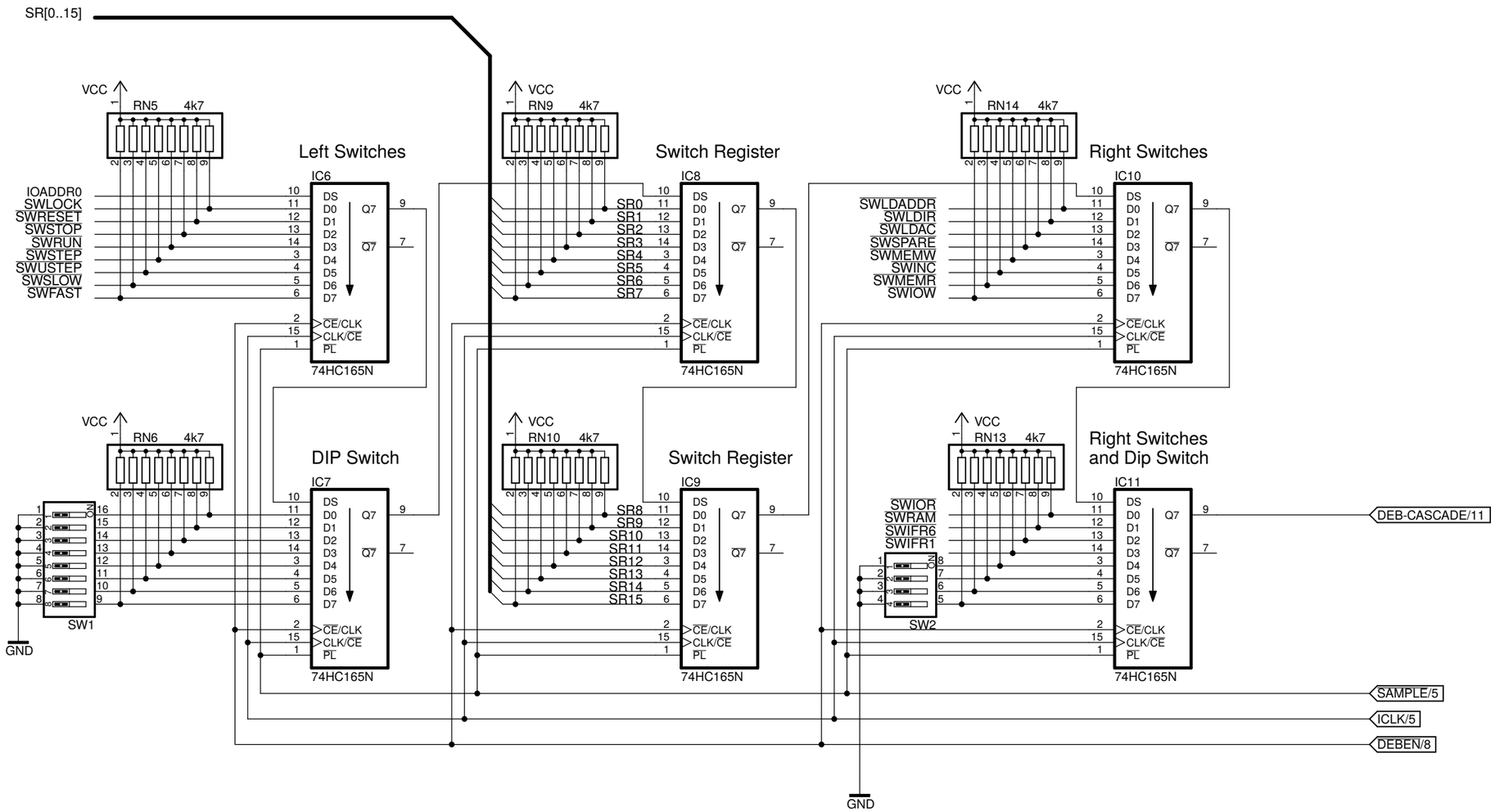
Note: active-low signals in the µADDR vector are not inverted. The aim is to show the micro-instruction address in ROM, and inverted bits would confuse the matter. The front panel legend shows this.



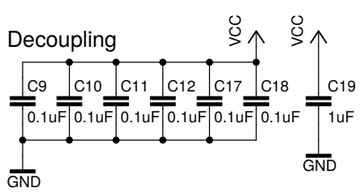
D	Title: front-panel-revF-DEB-board1
	Revision: Rev D
	Last Change: 25 Jun 2016 18:54:00
	Drawn by: Alexios — 3/11
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Input Shift Registers, switches and computer buses



Decoupling



D	Title: front-panel-revF-DEB-board1
	Revision: Rev D
	Last Change: 25 Jun 2016 18:54:00
	Drawn by: Alexios 4/11
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Input shift registers, processor state

FPIR[0..15]
FPPC[0..15]
FPAC[0..15]

AC

IC16

IOADDR0 10
FPAC0 11
FPAC1 12
FPAC2 13
FPAC3 14
FPAC4 3
FPAC5 4
FPAC6 5
FPAC7 6

74HC165N

IC17

FPAC8 11
FPAC9 12
FPAC10 13
FPAC11 14
FPAC12 3
FPAC13 4
FPAC14 5
FPAC15 6

74HC165N

PC

IC18

FPPC0 11
FPPC1 12
FPPC2 13
FPPC3 14
FPPC4 3
FPPC5 4
FPPC6 5
FPPC7 6

74HC165N

IC19

FPPC8 11
FPPC9 12
FPPC10 13
FPPC11 14
FPPC12 3
FPPC13 4
FPPC14 5
FPPC15 6

74HC165N

IR

IC20

FPIR0 11
FPIR1 12
FPIR2 13
FPIR3 14
FPIR4 3
FPIR5 4
FPIR6 5
FPIR7 6

74HC165N

IC21

FPIR8 11
FPIR9 12
FPIR10 13
FPIR11 14
FPIR12 3
FPIR13 4
FPIR14 5
FPIR15 6

74HC165N

Microcode vector

IC22

PB0-RUNIT0 11
PB0-RUNIT1 12
PB0-RUNIT2 13
PB0-RUNIT3 14
WUNIT0 3
WUNIT1 4
WUNIT2 5
FPOPIF0 6

74HC165N

IC23

PB0-OPIF1 11
PB0-OPIF2 12
PB0-OPIF3 13
CPL 14
CLL 3
STI 4
CLI 5
INCPC 6

74HC165N

Microcode vector / Misc

VCC

IC24

STPDR 11
STPAC 12
DEC 13
IO 14
MEM 3
4
5
END 6

74HC165N

IC25

BFNEG 11
BFZERO 12
PB0-FV 13
BFIRQ 14
FPFL 3
WAIT 4
CB-WEN 5
R 6

74HC165N

VPIN/8

SAMPLE/8
ICLK/8
VPEN/8

ICLK/4

Note: unless otherwise specified, all input signals are pulled up or down to avoid CMOS floating inputs.

IC21: FPIR11-15 already pulled down by MFD.
IC25: PB0-FV, FPFL pulled down by MFD.

Decoupling

VCC

C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF

GND

VCC

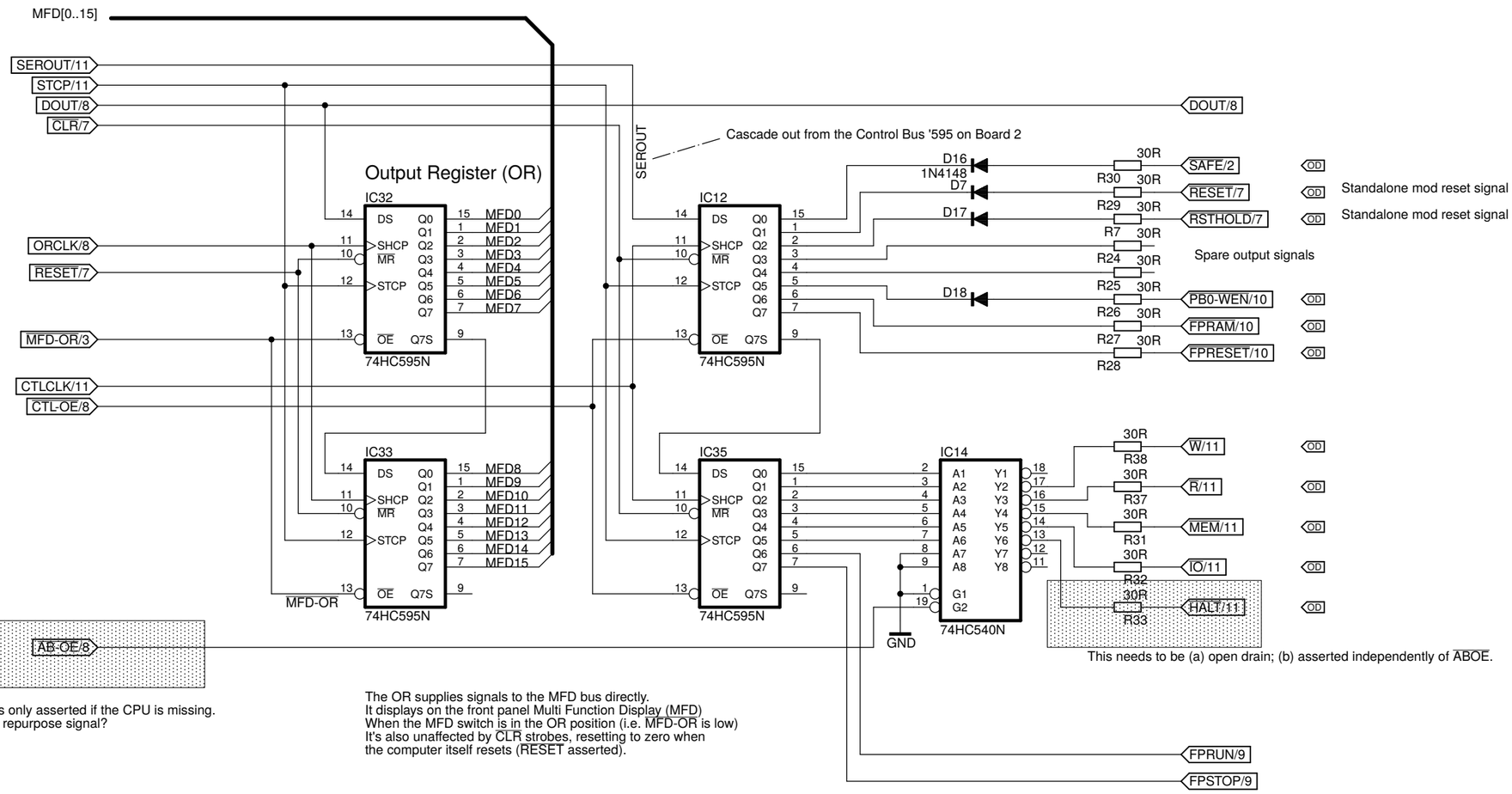
C30 1uF

GND

D	
Title: front-panel-revF-DEB-board1	
Revision: Rev D	
Last Change: 25 Jun 2016 18:54:00	
Drawn by: Alexios	5/11
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

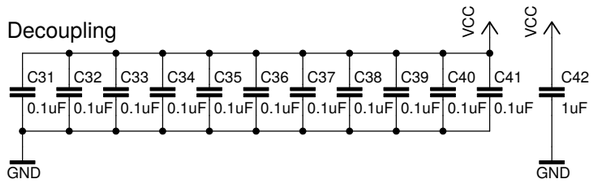
CFT Mini-Computer

Output shift registers



ABOE is only asserted if the CPU is missing.
Possibly repurpose signal?

The OR supplies signals to the MFD bus directly.
It displays on the front panel Multi Function Display (MFD)
When the MFD switch is in the OR position (i.e. MFD-OR is low)
It's also unaffected by CLR strobes, resetting to zero when
the computer itself resets (RESET asserted).



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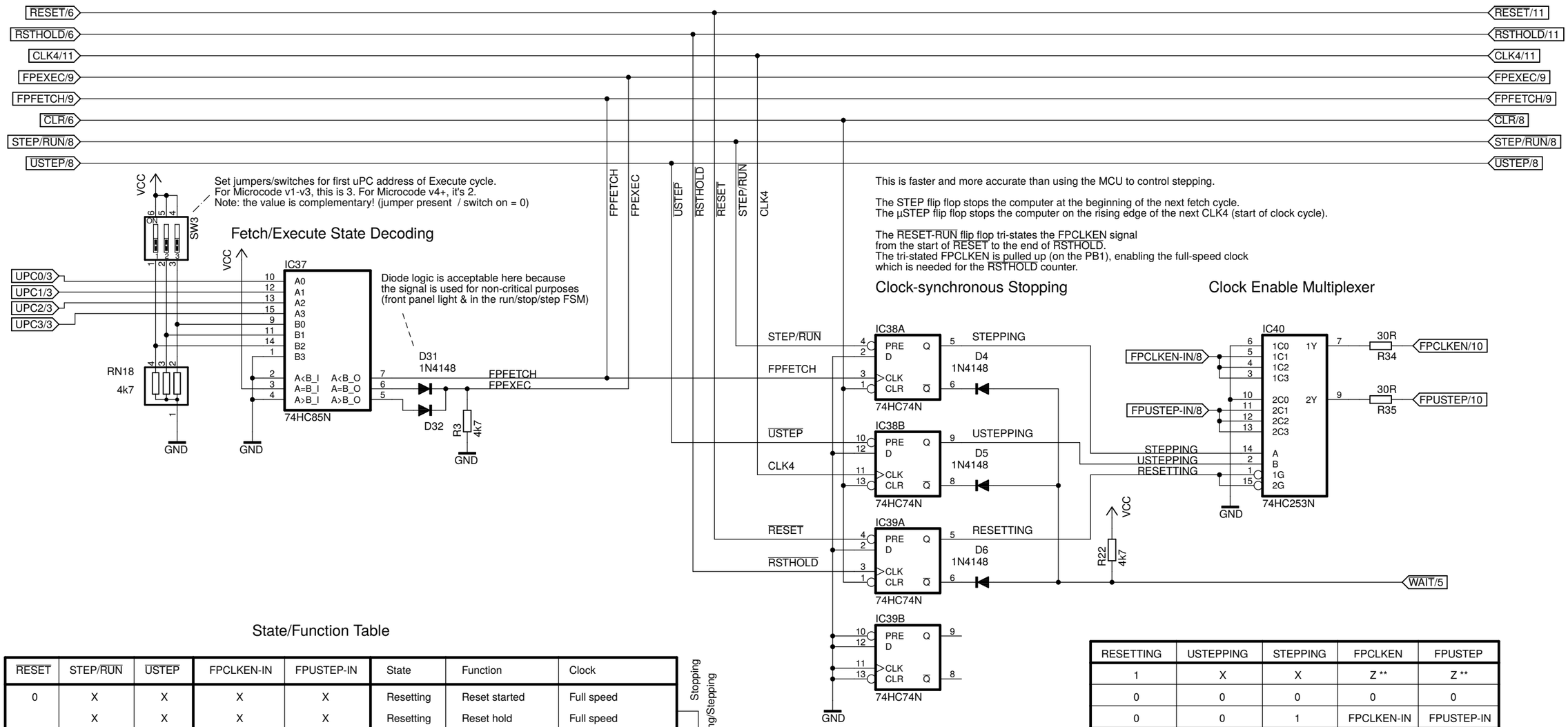
CFT Mini-Computer

Front Panel: Fetch/Execute Decoding, Synchronous Stopping



State/Function Table

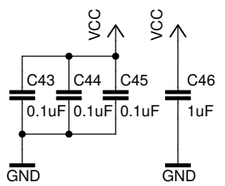
RESET	STEP/RUN	USTEP	FPCLKEN-IN	FPUSTEP-IN	State	Function	Clock
0	X	X	X	X	Resetting	Reset started	Full speed
	X	X	X	X	Resetting	Reset hold	Full speed
1	0	X	1	X	Running	Normal operation	Full speed
1	0	X	0	Strobing	Running	Normal operation	Slow (FPUSTEP-IN)
1	/	X	1	X	Stepping	Step Initiated	Full speed
1	/	X	0	Strobing	Stepping	Step Initiated	Slow (FPUSTEP-IN)
1	1	/	1	X	µStepping	µStep Initiated	Full speed
1	1	/	0	Strobing	µStepping	µStep Initiated	Slow (FPUSTEP-IN)
1	1	1	1	X	Stopping	Stopping/Stopped	N/A
1	1	1	0	Strobing	Stopping	Stopping/Stopped	N/A
1	1	1	0	0	Stopped	Stopped	N/A

Stopping
Starting/Stepping

RESETTING	USTEPPING	STEPPING	FPCLKEN	FPUSTEP
1	X	X	Z **	Z **
0	0	0	0	0
0	0	1	FPCLKEN-IN	FPUSTEP-IN
0	1	0	FPCLKEN-IN	FPUSTEP-IN
0	1	1	FPCLKEN-IN	FPUSTEP-IN

** PB0 pulls up FPCLKEN, enabling the clock when the output is in the high impedance state. Resets always happen at full speed, so the reset timing is (a) always identical, (b) fast (a reset at slow speeds could take over an hour to complete).

Decoupling



D

Title:	front-panel-revF-DEB-board1
Revision:	Rev D
Last Change:	25 Jun 2016 18:54:00
Drawn by: Alexios	7/11
Simulation filename:	To be coded
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

Front Panel: System Device

AB[0..15]

AB[0..15]

PFP-SEL/11

Decodes I/O 0100-011F (32 addresses)

IC42

74HC138N

AB5 AB6 AB7

IODEV1XX/11

30R R23

Edge detector

IC13A

74HC112N

PFP-SEL

Wait state generator

IC13B

74HC112N

D3 1N4148

WS/11

IOCMD

CLR-WS

VCC GND

RN19 4k7

RN20 4k7

MEGA168

IC41

RESET-MCU

4k7 R8

PC6(/RESET)

AREF AVCC VCC

PC0(ADC0) PC1(ADC1) PC2(ADC2) PC3(ADC3) PC4(ADC4/SDA) PC5(ADC5/SCL)

PD0(RXD) PD1(TXD) PD2(INT0) PD3(INT1) PD4(XCK/T0) PD5(T1) PD6(AIN0) PD7(AIN1)

PB0(ICP) PB1(OC1A) PB2(SS/OC1B) PB3(MOSI/OC2) PB4(MISO) PB5(SCK)

PB6(XTAL1/TOSC1) PB7(XTAL2/TOSC2)

C49 22pF C50 22pF Q2

C55 0.1uF C56 0.1uF

R1 R2 R9 R10 R11 R12 R16 R17 R18 R19 R20 R21 30R

R14 R15 R13 30R

R4 4k7 R5 4k7 R6 4k7

DEB-IN-BOARD2 VPIN ICLK DOUT CMD0 CMD1

RXD TXD

IOCMD DB-OE AB-OE IBUS-OE CTI-OE COUT

CLR-WS FPCLKEN-IN FPUSTEP-IN

MOSI MISO SCK

IOADDR0 IOADDR1 IOADDR2

DEB-IN-BOARD2/11 VPIN/5 ICLK/11 DOUT/11 IOCMD DB-OE/11 AB-OE/11 IBUS-OE/11 COUT/11 FPCLKEN-IN/7 FPUSTEP-IN/7 CMD1/11 IOADDR0/11 IOADDR1/11 IOADDR2/11

VPEN and DEBEN must NEVER be enabled simultaneously!

IC43 74HC259N

IC45 74HC540N

COUT IOADDR0 IOADDR1 IOADDR2 CMD0 CLR

ORCLK/6 SAMPLE/11 VPEN/5 DEBEN/11 STEP/RUN/7 USTEP/7 CLR/11

R36 4k7

CLR feeds back to clear itself. The pulse width is ~ 23ns, long enough to reset registers.
The pull down activates CLR by default (and on power on).

Notes on Bus Communication

Accessing the PFP/DEB port range immediately sets a wait state.
The wait state persists until the board has latched the address
(and, for write cycles, the data).
This is done because the PFP is considerably slower than the processor.

Reset behaviour: if the FF starts off cleared, all's good.
If the FF starts off set, $\overline{Q}$ will be low, which will clear the FF.
The MCU should clear the Wait State generator FF explicitly on initialisation.

Decoupling

C47 C48 C51 C52 C53 0.1uF

C54 1uF

In-Circuit Programming

CON1

MISO SCK RESET MOSI +5 GND

USB Serial

JP1

RTS TXD RXD FTDIVCC CTS

RXD TXD

Made for an FTDI USB to 3.3V TTL cable
For a 5V FTDI USB cable, do not fit R2 and R3.

TODO:

* DRC

D

Title:	front-panel-revF-DEB-board1
Revision:	Rev D
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Drawn by: Alexios	8/11
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CFT Mini-Computer

Front Panel Light Connections

Module 1	Module 2	Module 3	Module 4	Module 5	Module 6	Module 7	Module 8
Columns 1-4	Columns 5-9	Columns 10-13	Columns 14-17	Columns 18-21	Columns 22-25	Columns 26-29	Columns 30-33

SWLEDSON/2

Row 1

µAddr — JP26 — GND — JP33 — GND

	2550-		2550-		2550-		2534-	2550-	
END	P11-1	IO	P11-6	INCPC	P12-1	CPL	P12-6	FPOPIF0	P13-1	PB0-RUNIT3	P13-6	X1-1	P14-1	X1-5	P14-6
WEN	P11-2	DEC	P11-7	CLI	P12-2	PB0-OPIF3	P12-7	WUNIT2	P13-2	PB0-RUNIT2	P13-7	X1-2	P14-2	X1-6	P14-7
R	P11-3	STPAC	P11-8	STI	P12-3	PB0-OPIF2	P12-8	WUNIT1	P13-3	PB0-RUNIT1	P13-8	X1-3	P14-3	X1-7	P14-8
MEM	P11-4	STPDR	P11-9	CLL	P12-4	PB0-OPIF1	P12-9	WUNIT0	P13-4	PB0-RUNIT0	P13-9	X1-4	P14-4	X1-8	P14-9
	P11-5		P11-10		P12-5		P12-10		P13-5		P13-10		P14-5		P14-10

Row 2

Address — JP27 — GND — JP34 — GND

BAEXT7	P11-11	BAEXT3	P11-16	FPPC15	P12-11	FPPC11	P12-16	FPPC7	P13-11	FPPC3	P13-16	X1-9	P14-11	X1-13	P14-16
BAEXT6	P11-12	BAEXT2	P11-17	FPPC14	P12-12	FPPC10	P12-17	FPPC6	P13-12	FPPC2	P13-17	X1-10	P14-12	X1-14	P14-17
BAEXT5	P11-13	BAEXT1	P11-18	FPPC13	P12-13	FPPC9	P12-18	FPPC5	P13-13	FPPC1	P13-18	X1-11	P14-13	X1-15	P14-18
BAEXT4	P11-14	BAEXT0	P11-19	FPPC12	P12-14	FPPC8	P12-19	FPPC4	P13-14	FPPC0	P13-19	X1-12	P14-14	X1-16	P14-19
	P11-15		P11-20		P12-15		P12-20		P13-15		P13-20		P14-15		P14-20

Row 3

Flags — JP28 — JP31 — GND — JP35 — GND

MBEN	P11-21	PB0-FV	P11-26	FPAC15	P12-21	FPAC11	P12-26	FPAC7	P13-21	FPAC3	P13-26	X1-17	P14-21	X1-21	P14-26
	P11-22	BFIRQ	P11-27	FPAC14	P12-22	FPAC10	P12-27	FPAC6	P13-22	FPAC2	P13-27	X1-18	P14-22	X1-22	P14-27
BFNEG	P11-23	FPFL	P11-28	FPAC13	P12-23	FPAC9	P12-28	FPAC5	P13-23	FPAC1	P13-28	X1-19	P14-23	X1-23	P14-28
BFZERO	P11-24		P11-29	FPAC12	P12-24	FPAC8	P12-29	FPAC4	P13-24	FPAC0	P13-29	X1-20	P14-24	X1-24	P14-29
	P11-25		P11-30		P12-25		P12-30		P13-25		P13-30		P14-25		P14-30

Row 4

Accumulator State — JP29 — JP32 — MFD — GND — JP36 — GND

FPRST	P11-31	FPFETCH	P11-36	MFD15	P12-31	MFD11	P12-36	MFD7	P13-31	MFD3	P13-36	X1-25	P14-31	X1-29	P14-36
FPRUN	P11-32	FPEXEC	P11-37	MFD14	P12-32	MFD10	P12-37	MFD6	P13-32	MFD2	P13-37	X1-26	P14-32	X1-30	P14-37
FPSTOP	P11-33	FPINT	P11-38	MFD13	P12-33	MFD9	P12-38	MFD5	P13-33	MFD1	P13-38	X1-27	P14-33	X1-31	P14-38
FPWS	P11-34		P11-39	MFD12	P12-34	MFD8	P12-39	MFD4	P13-34	MFD0	P13-39	X1-28	P14-34	X1-32	P14-39
	P11-35		P11-40		P12-35		P12-40		P13-35		P13-40		P14-35		P14-40

Row 5

Instruction — JP30 — GND

	P11-41	PB0-UCB2	P11-46	FPIR15	P12-41	FPIR11	P12-46	FPIR7	P13-41	FPIR3	P13-46		P14-41		P14-46
	P11-42	PB0-UCB1	P11-47	FPIR14	P12-42	FPIR10	P12-47	FPIR6	P13-42	FPIR2	P13-47		P14-42		P14-47
	P11-43	PB0-UCB0	P11-48	FPIR13	P12-43	FPIR9	P12-48	FPIR5	P13-43	FPIR1	P13-48		P14-43		P14-48
PB0-UCB3	P11-44		P11-49	FPIR12	P12-44	FPIR8	P12-49	FPIR4	P13-44	FPIR0	P13-49		P14-44		P14-49
	P11-45		P11-50		P12-45		P12-50		P13-45		P13-50		P14-45		P14-50

X1-33
X1-34

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Drawn by: Alexios	9/11
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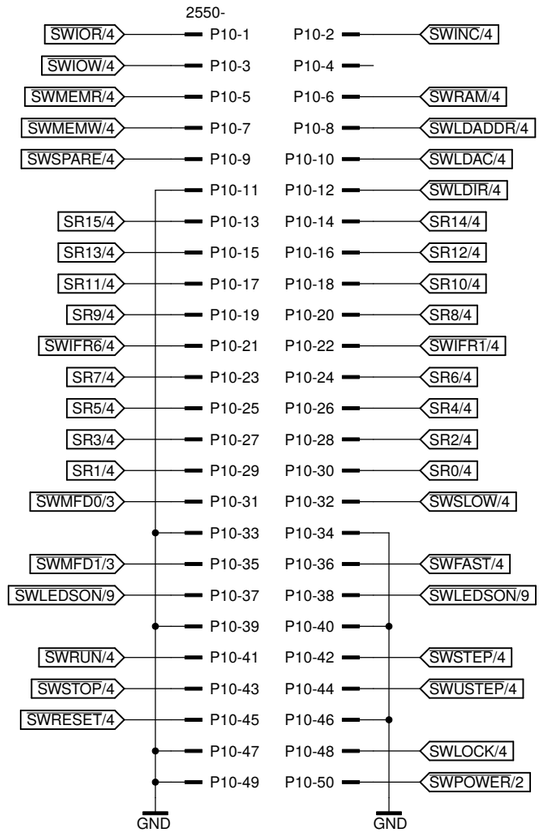
D

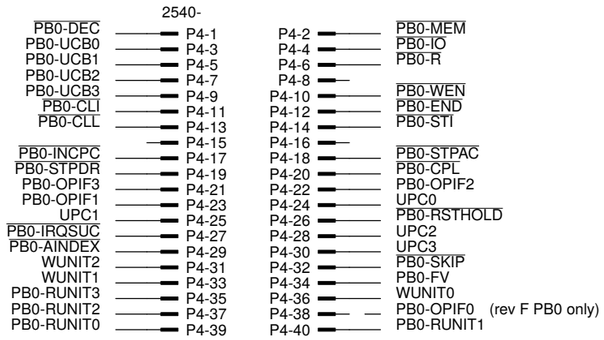
CFT Mini-Computer

Connectors

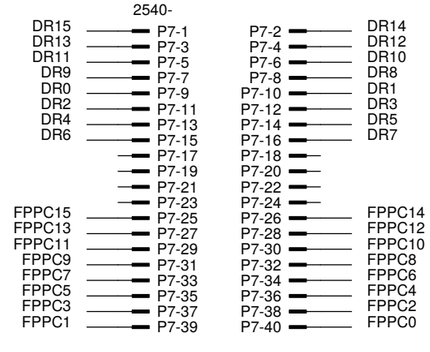
Switch Assembly



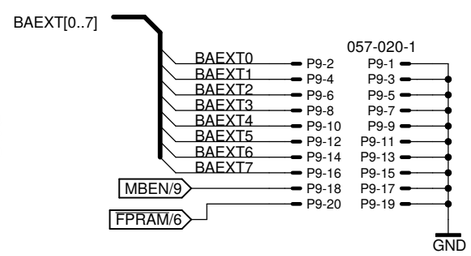
Processor Board 0



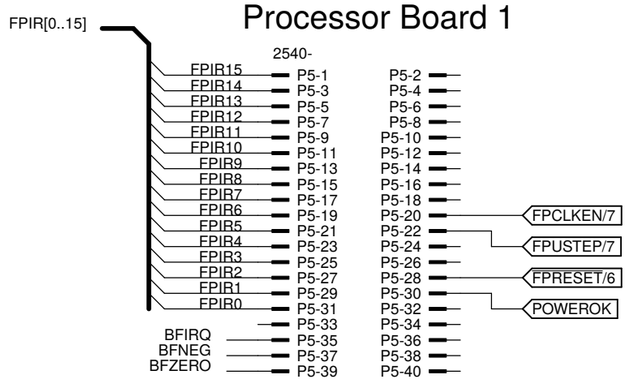
Processor Board 2 (left)



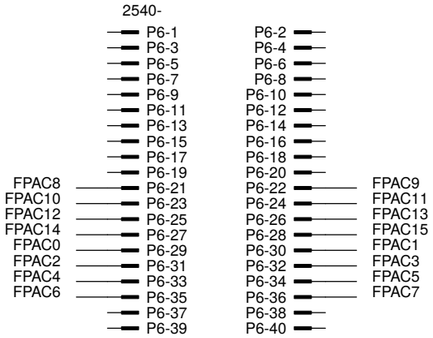
Processor Board 3 (MBU)



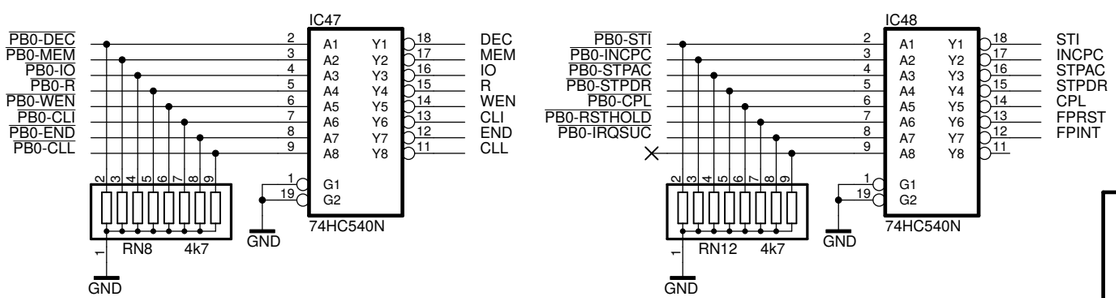
Processor Board 1



Processor Board 2 (right)

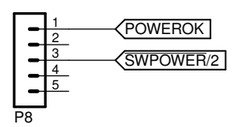


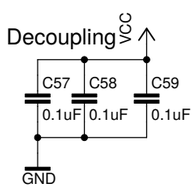
Signal Inversion



Power Supply

From power supply loom

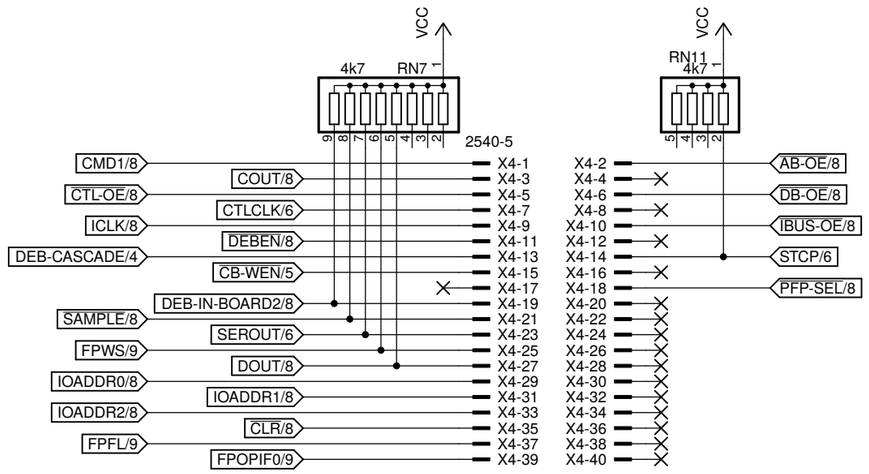




D	Title: front-panel-revF-DEB-board1
	Revision: Rev D
	Last Change: 25 Jun 2016 18:54:00
	Drawn by: Alexios 10/11
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

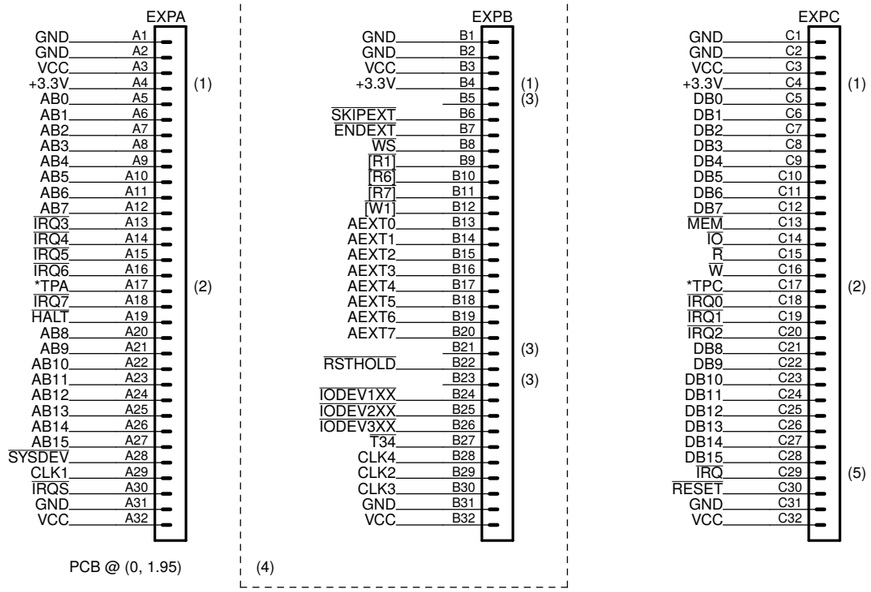
CFT Mini-Computer

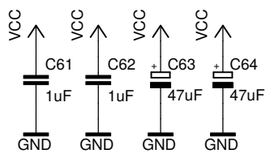
Bus Connectors



Board 2 connects all even unused pins to ground.
These pins are unconnected here to avoid ground loops.

Expansion Bus (computer bus)





Notes

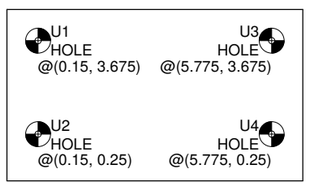
(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it.
It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) IRQ is provided for systems which lack an interrupt controller (IRQ0-7)



[PCB Logo]

[QR Code http://www.bedroomlan.org/cft (shortened)]

open hardware

J	
Title: front-panel-revF-DEB-board1	
Revision: Rev J	
Last Change: 25 Jun 2016 18:54:00	
Drawn by: Alexios	11/11
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	