CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic.
All ICs are through-hole DIP packages.

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Circuits in need of improvement are marked like this.

Circuits known to be incorrect are marked like this.

D	Title: cft
	Revision: Rev B
	Last Change: 25 Feb 2012 18:44:25
	Drawn by: Alexios 1/38
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Clock generation & control, Reset, Power & indicators

Run Indicator (optional)

330R R5 LED1 GND

VCC R1 4k7

The '253 implements a function of CLKEN and FPUSTEP to allow either clocked operation of manual stepping.

f(CLKEN,FPUSTEP): (CLK/2, $\overline{CLK/2}$)

f(0,0) = (0, 1)
f(0,1) = (1, 0)
f(1,X) = (CLKIN/2, $\overline{CLKIN/2}$)

NB: CLK/2, $\overline{CLK/2}$ and CLK/4, $\overline{CLK/4}$ are critical paths.

FPCLKEN/28 → FPCLKEN/28

RESET/4 → $\overline{RESET}$/4

FPUSTEP/28 → FPUSTEP/28

R2 4k7 GND

Clock Control (run/stop/step)

IC2A 74HC112N: PRE, J, Q, CLK, K, $\overline{Q}$, CLR

CLKIN/2, $\overline{CLKIN/2}$

IC5 74HC253N: 1C0–1C3, 1Y, 2C0–2C3, 2Y, A, B, 1G, 2G

CLK/2, $\overline{CLK/2}$

Raw clock Selector MUX

SLOWCLK/3

TESTCLK/3

IC1 74HC253N: 1C0–1C3, 1Y, 2C0–2C3, 2Y, A, B, 1G, 2G

RAWCLK

R3 4k7

FPFAST/28

FPSLOW/28

R4 4k7

GND

Divide by 2, generate 2 phases

Divide by 2, generate 4 phases

IC6A, IC6B 74HC112N: PRE, J, Q, CLK, K, $\overline{Q}$, CLR

Raw clock is divided by 4 using 2 FF stages

TP3 → CLK3/38

TP4 → CLK1/5

TP5 → CLK4/38

TP6 → CLK2/38

TP7 → CLK5/7

IC4C 74HC00N

$\overline{GUARD}$ phase difference selector

74HC00: 7ns delay per gate, 14ns delay per jumper setting

IC3A, IC7D, IC7C, IC7B, IC7A, IC4B, IC4A, IC3D, IC3C, IC3B — 74HC00N

TP8

JP1

Install exactly ONE jumper.

GUARD/7

$\overline{GUARD}$ avoids IBUS contention between processor units of different speed by inhibiting unit decoding immediately before/after CLK rising edges.
The delay mechanism will have to be readjusted if the clock speed changes.

Clock Source Selector

Fast: FPFAST=1, FPSLOW=0 (#2)
Slow 1: FPFAST=0, FPSLOW=0 (#0)
Slow 2: FPFAST=0, FPSLOW=1 (#1)
With no front panel, pull-up/down always selects FASTCLK.

Full-Speed (Fast) Clock Oscillator

C11 0.1uF

XTAL1 16.000MHz: VCC, NC/TS, GND, OUT

FASTCLK

Oscillator is 4x system clock speed.
16 MHz is a hopeful maximum. Testing required.
Oscillator frequency could drop to 4 MHz if the system is unstable.

Decoupling

C1–C9 0.1uF, C10 1uF

IC2B 74HC112N

IC4D 74HC00N

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U

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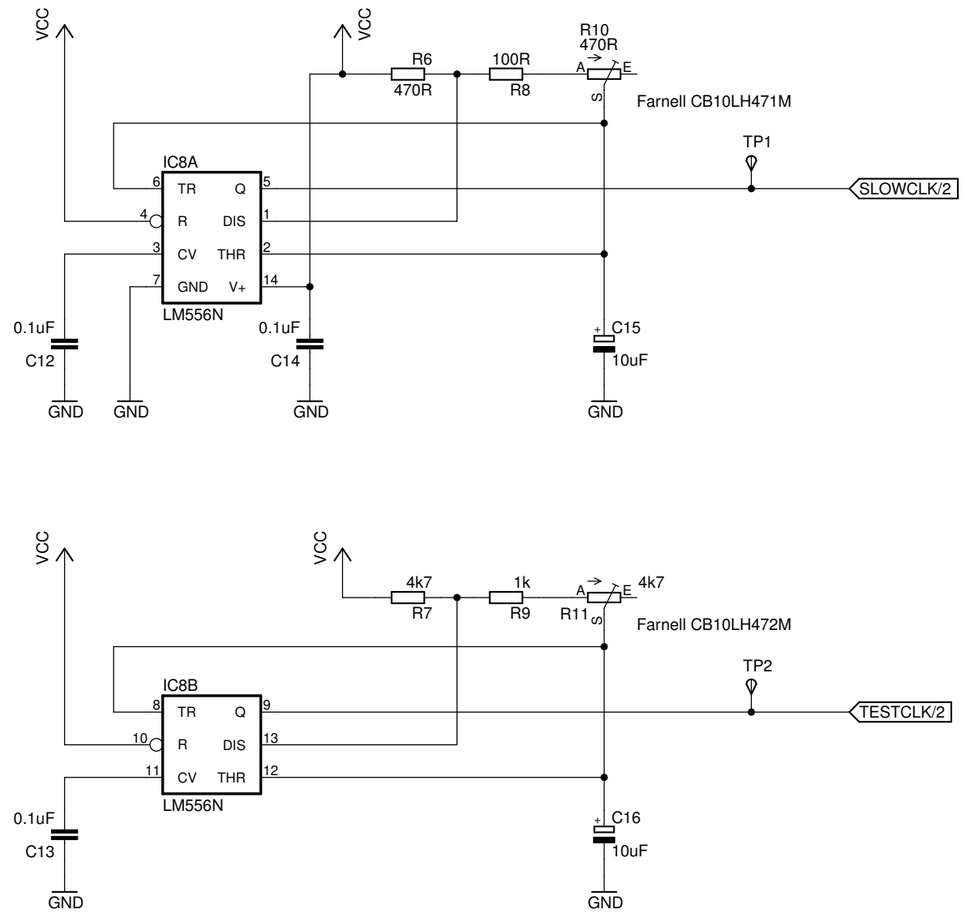
Slow Clock Generator

Slow and Test Clock Generators



TODO:

* Bill of Materials
* DRC

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Reset Handling and Sequencing

On RESET, the reset timer drives RSTHOLD down for 255 CLK pulses.
Using a 16 MHz oscillator, this will assert RSTHOLD for 31.875 us.
Using the slow clock (~400 Hz raw), this will pulse for 1.275 seconds.
Finally, with the testing clock (~40 Hz raw), RSTHOLD will last 12.75 seconds.
NB: CLKIN/2 is RAWCLK divided by 2 (obviously).

RESET/2
RSTHOLD/5
CLKIN/2/2
RESET/5
RSTHOLD/5
TP9
IBUS[0..15]

VCC
R17 4k7
R18 4k7

Reset Sources

VCC
R14 4k7
R16 4k7

FPRESET/29
POWEROK/34

IC10A 74HC05N
IC10B 74HC05N
IC10C 74HC05N
IC10D 74HC05N

NB: Open Collector gate

330R R13
LED2
Power LED
GND

NB: Open Drain gates

RESET

POWEROK comes from the ATX PSU via the front panel.
The PSU holds POWEROK low at power-up (or during brown-outs), until power stabilises. The computer is expected to reset when POWEROK is low.

Reset Button (optional)

JP2
S1
R12 50k
C23 10nF
IC9A '1G14
R15 4k7
VCC
GND

If the reset button and debouncing circuit is installed, this resistor may be left out.

Reset timer

CLKIN/2
RESET

IC13 74HC590N
CLK CCKEN CCLR RCK G
QA QB QC QD QE QF QG QH RCO
RSTHOLD

IC10E 74HC05N
NB: Open Drain gate

System Reset Vector (FFF0)

IC11 74HC541N
IC12 74HC541N
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
RSTHOLD
IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15
IBUS[0..15]

Outputs binary 1111'1111'1111'0000 to the IBUS while RSTHOLD is asserted.
This value is picked up by other units of the processor, including the Program Counter, and becomes the computer's boot address.

Decoupling

C17 C18 C19 C20 C21 0.1uF
C22 1uF
VCC
GND

IC10F 74HC05N
NB: Open Drain gate

TODO:

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U

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Microcode Sequencer

Notes

32k x 8 (2x256) ICs required for Microcode v4.
512k x 8 ICs are cheaper and easier to come by, though,
so this schematic uses these. Smaller ICs can be substituted.

ROMS to be socketed for easy reprogramming.

Use 70ns or 50ns chips.

Vertical microcode (unit selectors RUNIT, WUNIT and OPIF) are pulled low because a value of zero selects no unit.

$\overline{WS}$: indicates a wait state. Inhibits the uPC counter.
$\overline{HALT}$: halts the processor. The control unit's outputs are at High-Z. Consequently, the processor is disconnected from all busses. Control signals are active low and pulled up, so other units (like the front panel) may operate them with the processor halted.

$\overline{RESET}$: while $\overline{RESET}$ is active (low), the microcode ROMs are deselected and their outputs tri-stated to avoid bus contention with units resetting uncleanly.

Nota Bene: this sequencer can only run Microcode v.4!

AINDEX/6
SKIP/6
FL/6
FV/6
IRQS/6
RSTHOLD/4

AINDEX
SKIP
FL
FV
IRQS
RSTHOLD
END

Microcode PC

VCC
4k7 R19
4k7 R20
IC15
74HC161
P1 P2 P3 P4 Q1 Q2 Q3 Q4 CLK CO LD PE TE CL
UPC0 UPC1 UPC2 UPC3
CLK1/2
WS
HALT/36
CLK1
END
WS
HALT
RSTHOLD
GND

Microcode ROMs

RN2 4k7
RN4 4k7

UROM1
UROM2
UROM3
29F040
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
D0 D1 D2 D3 D4 D5 D6 D7
$\overline{CE}$ $\overline{OE}$ $\overline{WE}$

IR11/6
IR12/6
IR13/6
IR14/6
IR15/6

UPC0 UPC1 UPC2 UPC3 AINDEX SKIP IR11 IR12 IR13 IR14 IR15 FL FV IRQS RSTHOLD

RUNIT0 RUNIT1 RUNIT2 RUNIT3 WUNIT0 WUNIT1 WUNIT2 OPIF0
OPIF1 OPIF2 OPIF3 INCAC CPL CLL STI CLI
INCPC INCDR UINSTR18 MEM IO R W END

4k7 RN1
4k7 RN3

C30 1uF
C31 1uF
C32 1uF

HALT/36
RESET/4
IC14A
74HC08

ROM image: microcode-00
ROM image: microcode-01
ROM image: microcode-02

RUNIT0/6 RUNIT1/6 RUNIT2/6 RUNIT3/6
WUNIT0/6 WUNIT1/6 WUNIT2/6
OPIF0/6 OPIF1/6 OPIF2/6 OPIF3/6
CPL/6 CLL/6 STI/6 CLI/6
INCAC/6 INCPC/6 INCDR/6
UINSTR18/6 MEM/6 IO/6 R/6 W/6 END/6

$\overline{UCE}$ is used by the unit decoders to ensure no units are selected when either $\overline{HALT}$ or $\overline{RESET}$ are inactive.

UCE/7

Decoupling

C24 C25 C26 C27 C28 0.1uF
IC15P
VDD VSS
C29 1uF

74HC08

IC14B IC14C IC14D

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U

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Microcode Sequencer Front Panel Connections

UPC0/5
UPC1/5
UPC2/5
UPC3/5
AINDEX/5
SKIP/5
IR11/5
IR12/5
IR13/5
IR14/5
IR15/5
FL/5
FV/5
IRQS/5
RSTHOLD/5

IR[0..15] is sent to the Front Panel separately.

RUNIT0/5
RUNIT1/5
RUNIT2/5
RUNIT3/5
WUNIT0/5
WUNIT1/5
WUNIT2/5
OPIF0/5
OPIF1/5
OPIF2/5
OPIF3/5
CPL/5
CLL/5
STI/5
CLI/5
INCAC/5
INCPC/5
INCDR/5
UINSTR18/5
MEM/5
IO/5
R/5
W/5
END/5
FZERO/8
FNEG/8

IC16 — 74HC541N

UPC0	2	18	BUPC0
UPC1	3	17	BUPC1
UPC2	4	16	BUPC2
UPC3	5	15	BUPC3
AINDEX	6	14	BAINDEX
SKIP	7	13	BSKIP
FL	8	12	BFL
FV	9	11	BFV

IC17 — 74HC541N

IRQS	2	18	BIRQS
RSTHOLD	3	17	BRSTHOLD
RUNIT0	4	16	BRUNIT0
RUNIT1	5	15	BRUNIT1
RUNIT2	6	14	BRUNIT2
RUNIT3	7	13	BRUNIT3
WUNIT0	8	12	BWUNIT0
WUNIT1	9	11	BWUNIT1

IC18 — 74HC541N

FZERO	2	18	BFZERO
FNEG	3	17	BFNEG
	4	16	
WUNIT2	5	15	BWUNIT2
OPIF0	6	14	BOPIF0
OPIF1	7	13	BOPIF1
OPIF2	8	12	BOPIF2
OPIF3	9	11	BOPIF3

IC19 — 74HC540N

INCAC	2	18	BINCAC
CPL	3	17	BCPL
CLL	4	16	BCLL
STI	5	15	BSTI
CLI	6	14	BCLI
INCPC	7	13	BINCPC
INCDR	8	12	BINCDR
UINSTR18	9	11	BUINSTR18

IC20 — 74HC540N

MEM	2	18	BMEM
IO	3	17	BIO
R	4	16	BR
W	5	15	BW
END	6	14	BEND

JP3

BUPC0	1	2	BMEM
BUPC1	3	4	BIO
BUPC2	5	6	BR
BUPC3	7	8	BW
BAINDEX	9	10	BEND
BSKIP	11	12	BINCAC
BFL	13	14	BCPL
BFV	15	16	BCLL
BIRQS	17	18	BSTI
BRSTHOLD	19	20	BCLI
BRUNIT0	21	22	BINCPC
BRUNIT1	23	24	BINCDR
BRUNIT2	25	26	BUINSTR18
BRUNIT3	27	28	BOPIF0
BWUNIT0	29	30	BOPIF1
BWUNIT1	31	32	BOPIF2
BWUNIT2	33	34	BOPIF3
FZERO	35	36	FNEG
	37	38	
	39	40	

TODO:

* Bill of Materials
* DRC

U

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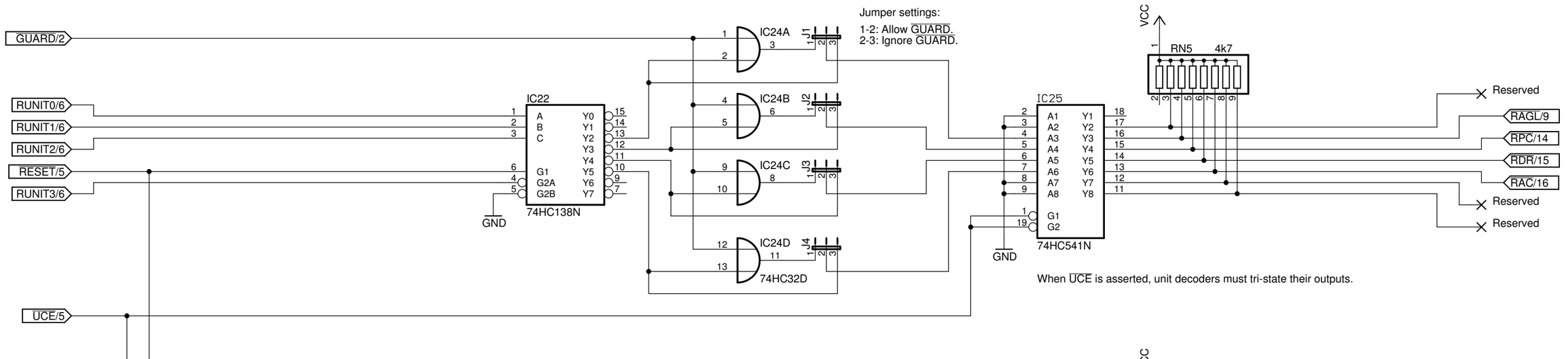
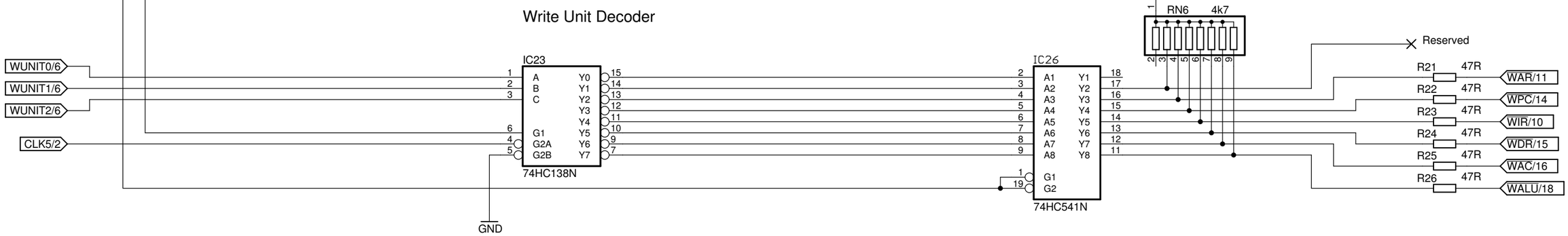
CFT Mini-Computer

Read & Write Unit Decoding

Read Unit Decoder (partial)



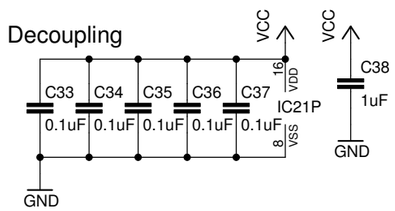
Write Unit Decoder



TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

Decoupling



Write Unit Decoder:

000 = Idle
001 = Reserved
010 = Write AR (WAR)
011 = Write PC (WPC)
100 = Write IR (WIR)
101 = Write DR (WDR)
110 = Write AC & ALU Port A (WAC)
110 = Write ALU Port B (WALU)
111 = Reserved

RUNIT is decoded partially: only 0xxx values are decoded here.
ALU Operation decoding (RUNIT=1xxx) is done on the ALU board.

0000 = Idle
0001 = Reserved
0010 = Read from AGL (RAGL)
0011 = Read from PC (RPC)
0100 = Read from DR (RDR)
0101 = Read from AC (RAC)
0110 = Reserved
0111 = Reserved
1XXX = ALU operation or Constant

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CFT Mini-Computer

Skip/Branch Logic

IR[0..15]

OPIF[0..3]

FNEG/6

FZERO/6

FL/6

FV/6

Microcode v.4 OPIF field

OPIF = 0000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 0001: IF3 ($\overline{SKIP}$ = IR3)
OPIF = 0010: IF4 ($\overline{SKIP}$ = IR4)
OPIF = 0011: IF5 ($\overline{SKIP}$ = IR5)
OPIF = 0100: IF6 ($\overline{SKIP}$ = IR6)
OPIF = 0101: IF7 ($\overline{SKIP}$ = IR7)
OPIF = 0110: IF8 ($\overline{SKIP}$ = IR8)
OPIF = 0111: IF9 ($\overline{SKIP}$ = IR9)

OPIF = 1000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1001: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1010: IFV ($\overline{SKIP}$ = IFV, skip if V=0)
OPIF = 1011: IFL ($\overline{SKIP}$ = IFL, skip if L=0)
OPIF = 1100: IFZERO ($\overline{SKIP}$ = IFZERO, skip if Z=0)
OPIF = 1101: IFNEG ($\overline{SKIP}$ = FNEG, skip if N=0)
OPIF = 1110: IFROLL ($\overline{SKIP}$ = IR0 + IR1 + IR2)
OPIF = 1111: IFBRANCH Logic

IC28B 74AC08N — SV = FV · IR0
IC28A 74AC08N — SL = FL · IR1
IC28D 74AC08N — SZ = FZERO · IR2
IC28C 74AC08N — SN = FNEG · IR3
IC27A 74AC32N
IC27B 74AC32N
IC27C 74AC32N
IC29A 74AC86N — OP1_BRANCH = (SV + SL + SZ + SN) XOR IR4

Worst case propagation delay: 3 x 8.5ns + 9.5ns = 35ns

OP1 Branch Logic (IR0..IR4)

IC30A 74AC32N
IC30B 74AC32N

OP2_ROLL

OP2 Roll detection (IR0..IR3)

Condition Multiplexing

IC32 74AC251D — 0000-0111
IC33 74AC251D — 1000-1111

IR3 IR4 IR5 IR6 IR7 IR8 IR9
OPIF0 OPIF1 OPIF2 OPIF3
FV FL FZERO FNEG OP2_ROLL OP1_BRANCH

SKIPMUXLO = Low = Skip
SKIPMUXHI = Low = Skip

IC31A 74AC00N — OPIF3 = OPIF0 · OPIF1 · OPIF2 · OPIF3
IC31B 74AC00N
IC31C 74AC00N

VCC
4k7 R28
4k7 R27

This generates glitches, but the Skip Flag Register filters them out.

Skip flag register

IC34 74AC175D

SKIP0 → SKIP/6

CLK1/5

RESET/7

GND

Decoupling

C39 C40 C41 C42 C43 C44 C45 C46 — 0.1uF
C47 — 1uF

IC30D 74AC32N
IC30C 74AC32N
IC29B 74AC86N
IC29C 74AC86N
IC29D 74AC86N
IC27D 74AC32N
IC31D 74AC00N

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U

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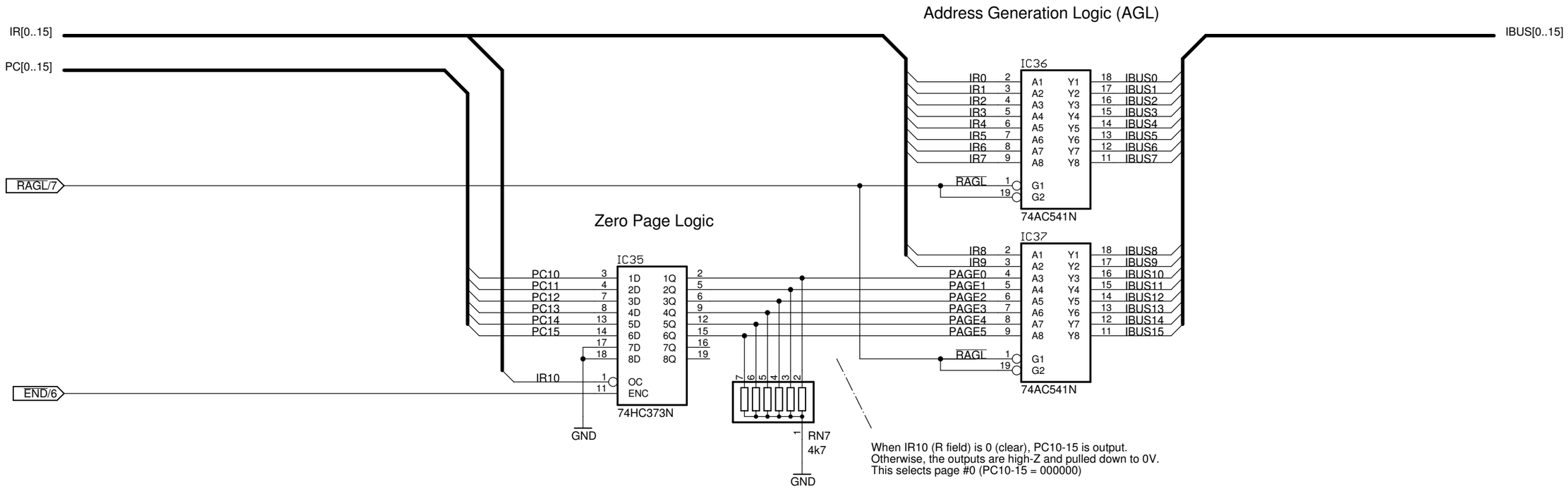
Address Generation Logic



Notes

The value of the PC is clocked into the D-Flip Flop on the rising edge of $\overline{\text{END}}$.
At that point, the PC holds the value of the instruction about to be fetched.

If this registering doesn't take place, by the time the AGL is read, the PC will have been incremented (at the end of the fetch cycle), and pointing to the next instruction.

Thus, the AGL would generate addresses for PC+1. This works as the user expects for the first 1023 page offsets, and fails on the 1024th, where the AGL produces an address for the next page.

This would make programming with page-relative modes much less intuitive.

TODO:

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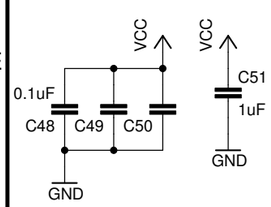
Decoupling



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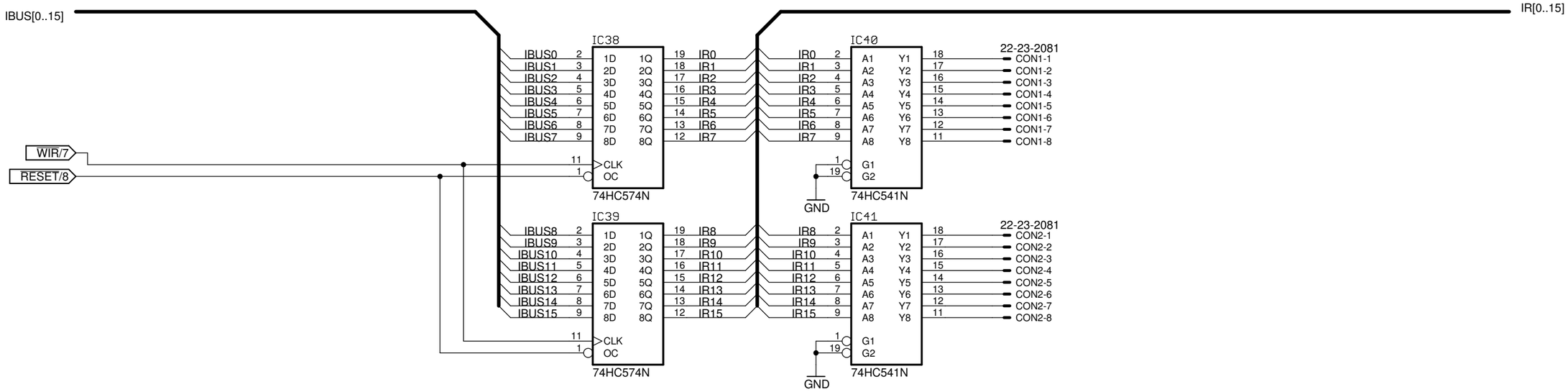
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

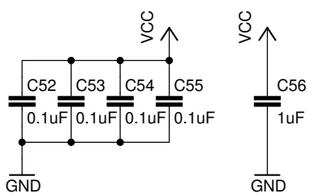
Instruction Register

Instruction Register (IR)

Front Panel Buffers & Connectors



Decoupling



TODO:

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Address Register, Address Bus Drivers & Termination, Autoindex Logic, Device Decoder

MEM/6
IO/6
IC42A
74HC08N
ABEN

IBUS[0..15]

Address Register (AR)

IC43 — 74HC273N
IC44 — 74HC273N
WAR/7
RESET/10
WAR
RESET
CLK
CLR

Address Bus Drive Logic

IC45 — 74HC541N
IC46 — 74HC541N
ABEN
G1
G2

Address Bus Hold

IC48 — 74HC541N
IC49 — 74HC541N
GND

AB[0..15]

RN8A 10k — AB0
RN8B 10k — AB1
RN8C 10k — AB2
RN8D 10k — AB3
RN8E 10k — AB4
RN8F 10k — AB5
RN8G 10k — AB6
RN8H 10k — AB7
RN9A 10k — AB8
RN9B 10k — AB9
RN9C 10k — AB10
RN9D 10k — AB11
RN9E 10k — AB12
RN9F 10k — AB13
RN9G 10k — AB14
RN9H 10k — AB15

TODO:

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Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.

CLK1/8
END/9
IO

Notes (Autoindex Logic)

This evaluates the function:

$\overline{AINDEX} = \overline{AR == 0000'0000'1XXX'XXXX}$

It is necessary to register $\overline{AINDEX}$ because AR is changed during execution of an indirect mode instruction.

The flag is cleared at the end of the instruction, when $\overline{END}$ is asserted.

Autoindex Logic

IC47 — 74HC688N
VCC
GND
AR7 AR8 AR9 AR10 AR11 AR12 AR13 AR14 AR15
P0 P1 P2 P3 P4 P5 P6 P7 P=Q
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 G

IC50 — 74HC175N
D1 D2 D3 D4 CLK CLR
Q1 Q2 Q3 Q4
AINDEX/23

I/O Device Address Decoder

IC52 — 74HC138N
A B C G1 G2A G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
SYSDEV/21
IODEV1XX
IODEV2XX
IODEV3XX

IC51 — 74HC688N
AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15
P0 P1 P2 P3 P4 P5 P6 P7 P=Q
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 G
IO

Decodes I/O addresses 0n00-0nFF to simplify interfacing.

For n = 0, $\overline{SYSDEV}$ is asserted.
For n = 1, $\overline{IODEV1XX}$ is asserted.
For n = 2, $\overline{IODEV2XX}$ is asserted.
For n = 3, $\overline{IODEV3XX}$ is asserted.

Other devices must be decoded ad hoc.

Decoupling

C57 C58 C59 C60 C61 C62 C63 C64 C65 — 0.1uF
C66 — 1uF
VCC
GND

IC42D IC42B IC42C — 74HC08N

U	Title: cft		
	Revision: Rev A		
	Last Change: 25 Feb 2012 18:44:25		
	Drawn by: Alexios	11/38	
	Simulation filename:		
	More Info: http://www.bedroomlan.org/cft		

CFT Mini-Computer

Interrupt State Machine

RESET/11
STI/6
CLI/6
END/11

VCC
R29
4k7
IRQ/22

IRQ should be drive by open-drain gates.
It is pulled up here.

RESET
END

RESET/14

Interrupts Enabled light (optional)

LED-5MM-GREEN
LED3
330
R30
GND

Interrupt Flag (Asynchronous)

STI
RESET
CLI
IC53A
74HC08N
RESET_OR_CLI

IC55A
PRE
J
CLK
K
CLR
Q
74HC112N
GND
FINT

FINT

Masking and State (Synchronous)

FINT
IRQ
IC54A
74HC32N

IC56B
MASKEDIRQ
RESET_OR_CLI
74HC112N
GND

FIRQ
Note: for testing purposes.

Interrupt Seen light (optional)

LED-5MM-GREEN
LED4
330
R31
GND

Interrupt Request Register FF
(Instruction-synchronous)

IC57A
VCC
FIRQ
END
RESET
74HC112N

IRQS/20

Interrupt Flag Waveforms

RESET
STI
CLI
FINT

Masking and IRQ Waveforms

RESET
CLI
FINT
IRQ
FIRQ

Masking and IRQ Waveforms (Instruction-synchronous)

END
RESET
CLI
FIRQ
IRQS

Notes

The Interrupt flag denotes our disposition to handle incoming interrupts (allow or ignore).
At RESET time, interrupts are cleared and further interrupts are masked (ignored).
The falling edge of CLI or RESET clears the interrupt flag, ignoring interrupts.
The falling edge of STI sets the flag, allowing interrupts.

When the interrupt flag is set, the falling edge of IRQ triggers an interrupt (FIRQ high).

This is ignored until the end of the current instruction (falling edge of END).
At that point, the register FF clocks FIRQ in, asserting IRQS to the microcode sequencer.
The K input of the flip flop is held constantly high. With FIRQ high, this is a toggle action.

At the next instruction (falling edge of END), IRQS would toggle again.
Before this happens, the interrupt microprogram asserts CLI, clearing FIRQ, so no further toggling takes place. Instead, with K low and J high, IRQS is deasserted, resuming normal excecution.

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

Decoupling

VCC
C67 0.1uF
C68 0.1uF
C69 0.1uF
C70 0.1uF
C71 0.1uF
C72 1uF
GND

IC53B
IC53C
74HC08N

IC53D
IC54B
74HC32N

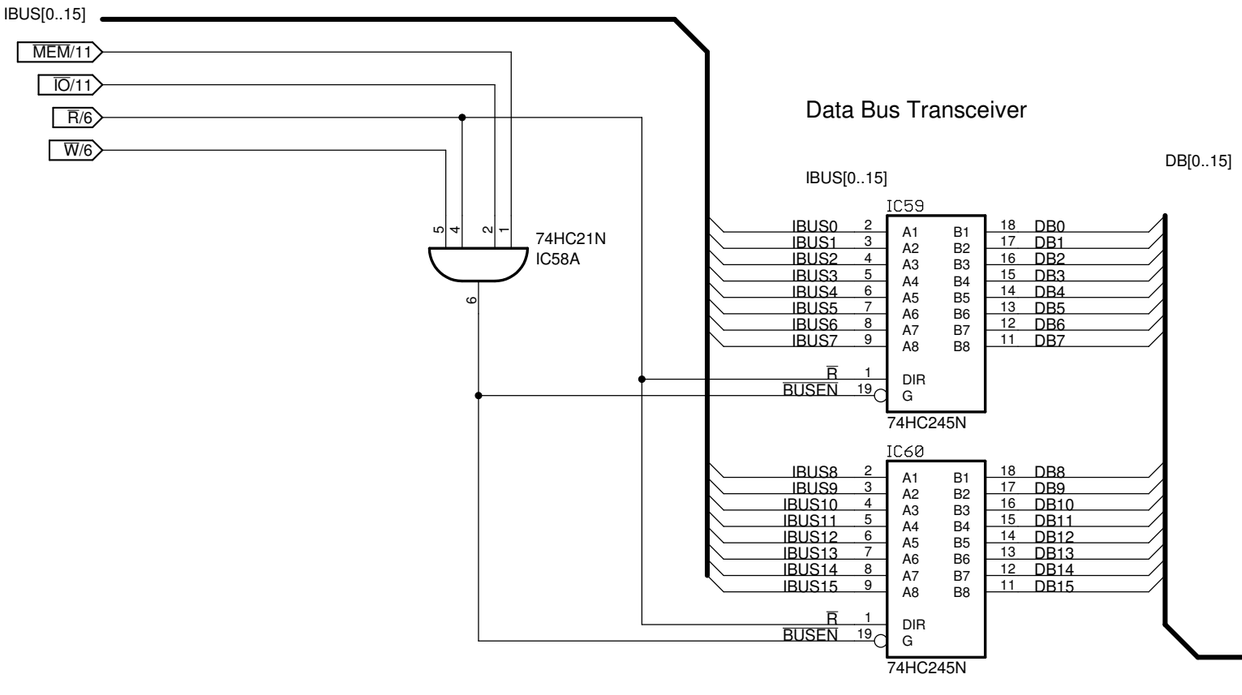
IC54C
IC54D
74HC32N

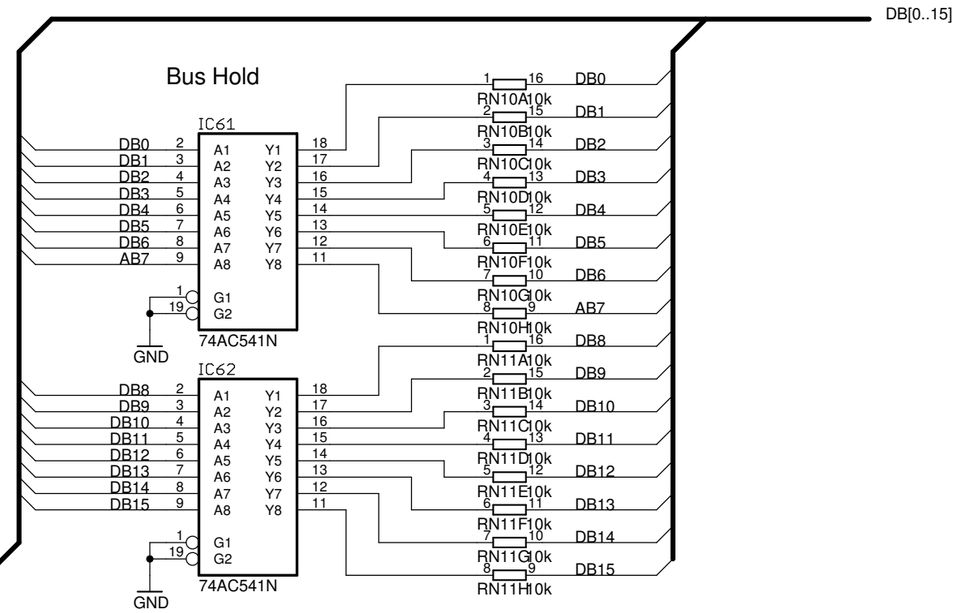
IC57B
74HC112N

U	Title: cft
	Revision: Rev B
	Last Change: 25 Feb 2012 18:44:25
	Drawn by: Alexios 12/38
	Simulation filename: int.v
	More Info: http://www.bedroomlan.org/cft

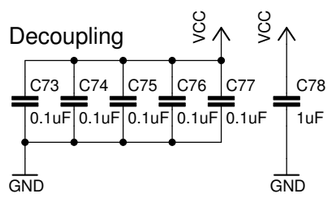
CFT Mini-Computer

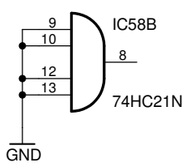
Data Bus Driver & Bus Termination





Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.





TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	13/38
Simulation filename: control_unit.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Major Registers: Program Counter (PC)

RPC/7
WPC/7
INCPC/6
RESET/12
IBUS[0..15]

NB: this is RESET inverted, fed to all 3 major registers' CLEAR signals ('193).

RESET/15
IBUS[0..15]

74ACT06N IC63A

Register & Increment

IC64 74HC193N
IC65 74HC193N
IC66 74HC193N
IC67 74HC193N

Pins: A B C D QA QB QC QD LOAD BORROW CARRY UP DOWN CLEAR
WPC INCPC RESET GND

Tri-State Buffering

IC68 IC69 74HC541N

Pins: A1..A8 Y1..Y8 G1 G2

Front Panel Buffers & Connectors

IC70 IC71 74HC541N
22-23-2081

CON3-1 CON3-2 CON3-3 CON3-4 CON3-5 CON3-6 CON3-7 CON3-8
CON4-1 CON4-2 CON4-3 CON4-4 CON4-5 CON4-6 CON4-7 CON4-8

PC[0..15]

Decoupling

C79 C80 C81 C82 C83 C84 C85 C86 0.1uF
C87 1uF
VCC VCC GND GND

IC63B 74ACT06N
IC63C IC63D IC63E IC63F

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	14/38
Simulation filename: register.v#inc_reg16	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Major Registers: Data Register (DR)

RDR/7
WDR/7
INCDR/6
RESET/14
IBUS[0..15]

NB: this is $\overline{\text{RESET}}$ inverted.

RESET/16
IBUS[0..15]

Register & Increment

IC72 — 74HC193N
IC73 — 74HC193N
IC74 — 74HC193N
IC75 — 74HC193N

	A	B	C	D	QA	QB	QC	QD	LOAD	BORROW	UP	CARRY	DOWN	CLEAR
IC72	IBUS0	IBUS1	IBUS2	IBUS3	DR0	DR1	DR2	DR3	WDR		INCDR			RESET
IC73	IBUS4	IBUS5	IBUS6	IBUS7	DR4	DR5	DR6	DR7	WDR		INCDR			RESET
IC74	IBUS8	IBUS9	IBUS10	IBUS11	DR8	DR9	DR10	DR11	WDR		INCDR			RESET
IC75	IBUS12	IBUS13	IBUS14	IBUS15	DR12	DR13	DR14	DR15	WDR		INCDR			RESET

All: GND

Tri-State Buffering

IC76 — 74HC541N
IC77 — 74HC541N

	A1	A2	A3	A4	A5	A6	A7	A8	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	G1	G2
IC76	DR0	DR1	DR2	DR3	DR4	DR5	DR6	DR7	IBUS0	IBUS1	IBUS2	IBUS3	IBUS4	IBUS5	IBUS6	IBUS7		
IC77	DR8	DR9	DR10	DR11	DR12	DR13	DR14	DR15	IBUS8	IBUS9	IBUS10	IBUS11	IBUS12	IBUS13	IBUS14	IBUS15		

All: G1 = G2 = GND

Front Panel Buffers & Connectors

IC78 — 74HC541N
IC79 — 74HC541N

	A1	A2	A3	A4	A5	A6	A7	A8	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	G1	G2
IC78	DR0	DR1	DR2	DR3	DR4	DR5	DR6	DR7	22-23-2081 CON5-1	CON5-2	CON5-3	CON5-4	CON5-5	CON5-6	CON5-7	CON5-8		
IC79	DR8	DR9	DR10	DR11	DR12	DR13	DR14	DR15	22-23-2081 CON6-1	CON6-2	CON6-3	CON6-4	CON6-5	CON6-6	CON6-7	CON6-8		

All: G1 = G2 = GND

DR[0..15]

Decoupling

	C88	C89	C90	C91	C92	C93	C94	C95	C96
	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	1uF

VCC, GND

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev C	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	15/38
Simulation filename: register.v#inc_reg16	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Accumulator (AC), Zero Flag & Negative Flag

RAC/7
WAC/7
INCAC/6
RESET/15
IBUS[0..15]

Register & Increment

IC80 — 74HC193N
IC81 — 74HC193N
IC82 — 74HC193N
IC83 — 74HC193N

Each 74HC193N: A, B, C, D, LOAD, UP, DOWN, CLEAR, BORROW, CARRY, QA, QB, QC, QD

IC80: IBUS0 IBUS1 IBUS2 IBUS3 → AC0 AC1 AC2 AC3
IC81: IBUS4 IBUS5 IBUS6 IBUS7 → AC4 AC5 AC6 AC7
IC82: IBUS8 IBUS9 IBUS10 IBUS11 → AC8 AC9 AC10 AC11
IC83: IBUS12 IBUS13 IBUS14 IBUS15 → AC12 AC13 AC14 AC15

WAC
INCAC
RESET
GND

Tri-State Buffering

IC84 — 74HC541N: AC0–AC7 → IBUS0–IBUS7
IC85 — 74HC541N: AC8–AC15 → IBUS8–IBUS15

G1, G2

Zero Flag

IC86 — 74HC688N: AC8–AC15, P=Q
IC87 — 74HC688N: AC0–AC7, P=Q

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

Front Panel Buffers & Connectors

IC88 — 74HC541N: AC0–AC7 → 22-23-2081 CON7-1 … CON7-8
IC89 — 74HC541N: AC8–AC15 → 22-23-2081 CON8-1 … CON8-8

AC15 = FNEG → FNEG/23
FZERO/23
INCCPL — Asynchronous toggle of L
AC[0..15]

Decoupling

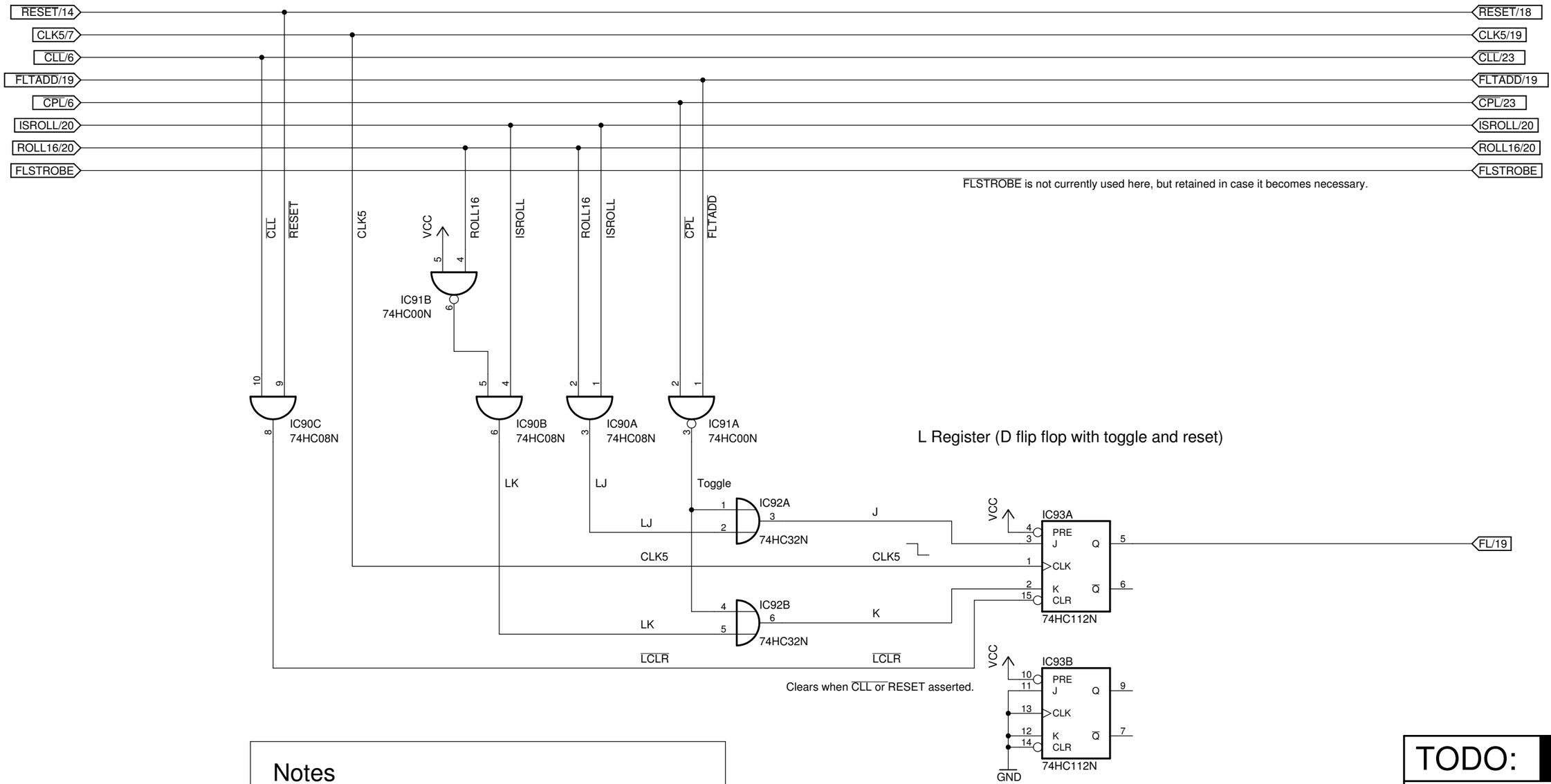
C97 C98 C99 C100 C101 C102 C103 C104 C105 C106 — 0.1uF
C107 — 1uF
VCC, GND

Title:	cft
Revision:	Rev C
Last Change:	25 Feb 2012 18:44:25
Drawn by:	Alexios
	16/38
Simulation filename:	register.v#inc_reg16
More Info:	http://www.bedroomlan.org/cft

U

CFT Mini-Computer

The L Register



Notes

Clock is the falling edge of CLK5 (the 'write' clock), so all inputs have had time to settle.

Since FLTADD is registered on the rising edge of CLK5, this implies that ADD carry out will toggle L one clock period after the addition itself.

Clear sources (asynchronous):

CLL resets it (L=0)
RESET resets it. (L=0)

Data out from a roll instruction sets the L register explicitly when L_LATCH is high.

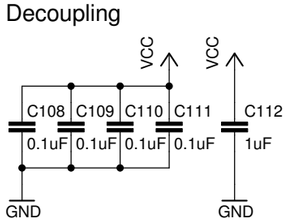
Toggle Sources (synchronous, to avoid glitches):

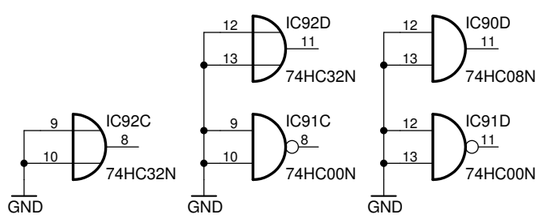
ALU carry out (FLD)
CPL toggles it (L=L)

TODO:

* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Decoupling





U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	17/38
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Arithmetic/Logic Unit: Decoding Logic

RUNIT[0..3]
IR[0..15]
IBUS[0..15]
AC[0..15]
WALU/7
RSTHOLD/6
RESET/17
GUARD/7

IBUS[0..15]
AC[0..15]
WALU/23
RSTHOLD/25
RESET/19
GUARD/38

WALU
IBUS[0..15]
RUNIT0
RUNIT1
IR0
IR2
GUARD
RESET
RSTHOLD
RUNIT3
RUNIT2

ALU Port B Buffer

B[0..15]

IC94 — 74HCT574N

IBUS0	2	19	B0
IBUS1	3	18	B1
IBUS2	4	17	B2
IBUS3	5	16	B3
IBUS4	6	15	B4
IBUS5	7	14	B5
IBUS6	8	13	B6
IBUS7	9	12	B7
	11		CLK
	1		OC

GND

IC95 — 74HCT574N

IBUS8	2	19	B8
IBUS9	3	18	B9
IBUS10	4	17	B10
IBUS11	5	16	B11
IBUS12	6	15	B12
IBUS13	7	14	B13
IBUS14	8	13	B14
IBUS15	9	12	B15
	11		CLK
	1		OC

GND

Unary Operation Decoder

IR0 ROLLOP0
RUNIT0
IR2 ROLLOP2
RUNIT1

IC96A — 74HC32N

IC97 — 74HC253N

	6	1C0	1Y 7 UOP0
	5	1C1	
	4	1C2	
	3	1C3	
	10	2C0	2Y 9 UOP1
	11	2C1	
	12	2C2	
	13	2C3	
	14	A	
	2	B	
	1	1G	
	15	2G	

GND

UOP2
UOP[0..2]

ALU Operation ROM selector (unary/binary)

IC98 — 74HCT138N

RUNIT2	1	A	Y0 15
RUNIT3	2	B	Y1 14
RSTHOLD	3	C	Y2 13
			Y3 12
			Y4 11
RESET	6	G1	Y5 10
GUARD	4	G2A	Y6 9 BOE/19
	5	G2B	Y7 7 UOE/20

GND

B[0..15]

Decoupling

VCC
C113 C114 C115 C116 0.1uF 0.1uF 0.1uF 0.1uF
C117 1uF
GND

74HC32N — IC96B, IC96C, IC96D

IC96D	11		
	12	13	IC96B
		4	
		5	74HC32N
		9	IC96C
		10	8
			6 74HC32N

GND

U	Title: cft
	Revision: Rev B
	Last Change: 25 Feb 2012 18:44:25
	Drawn by: Alexios — 18/38
	Simulation filename: alu.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

ALU Binary Operators

B[0..15]
AC[0..15]
RUNIT[0..3]
RESET/18
CLK5/17
BOE/18
FL/17

RESET/20
CLK5/20
BOE/18
FL/20

ALU Binary Operator ROMs

IC99 — 29F040
B0 12, B1 11, B2 10, B3 9, B4 8, B5 7, AC0 6, AC1 5, AC2 27, AC3 26, AC4 23, AC5 25, FL 4, RUNIT0 28, RUNIT1 29, 3, 2, 30, 1, 22 (CE), 24 (OE), 31 (WE), A0–A18
D0 13 IBUS0, D1 14 IBUS1, D2 15 IBUS2, D3 17 IBUS3, D4 18 IBUS4, D5 19 IBUS5, D6 20 CO1, D7 21
VCC, C124 1uF, GND, BOE

ROM image: alu-binary-6bit-00

IC100 — 29F040
B6 12, B7 11, B8 10, B9 9, B10 8, B11 7, AC6 6, AC7 5, AC8 27, AC9 26, AC10 23, AC11 25, CO1 4, RUNIT0 28, RUNIT1 29, 3, 2, 30, 1, 22 (CE), 24 (OE), 31 (WE), A0–A18
D0 13 IBUS6, D1 14 IBUS7, D2 15 IBUS8, D3 17 IBUS9, D4 18 IBUS10, D5 19 IBUS11, D6 20 CO2, D7 21
VCC, C125 1uF, GND, BOE

ROM image: alu-binary-6bit-00

IC101 — 29F040
B12 12, B13 11, B14 10, B15 9, AC12 6, AC13 5, AC14 27, AC15 26, CO2 4, RUNIT0 28, RUNIT1 29, 3, 2, 30, 1, 22 (CE), 24 (OE), 31 (WE), A0–A18
D0 13 IBUS12, D1 14 IBUS13, D2 15 IBUS14, D3 17 IBUS15, D4 18, D5 19 FLATCH, D6 20 ALUCPI, D7 21 FVOUT
VCC, C126 1uF, GND, BOE

ROM image: alu-binary-4bit-00

CLK5, RESET

VCC, RN12 4k7 (1, 2, 3, 4)

IC102A 74HC08N (1, 2, 3)

FLSTROBE

IC103B 74HC74N — PRE 10, D 12, CLK 11, CLR 13, Q 9, Q̄ 8
FV/23

RESET

IC103A 74HC74N — PRE 4, D 2, CLK 3, CLR 1, Q 5, Q̄ 6
FLTADD/17

CLK5

IBUS[0..15]

Decoupling

VCC, GND
C118 0.1uF, C119 0.1uF, C120 0.1uF, C121 0.1uF, C122 0.1uF, C123 1uF

74HC08N IC102B (5, 6, 4)
74HC08N IC102C (10, 8, 9)
74HC08N IC102D (13, 11, 12)
GND

TODO:

* Bill of Materials
* DRC

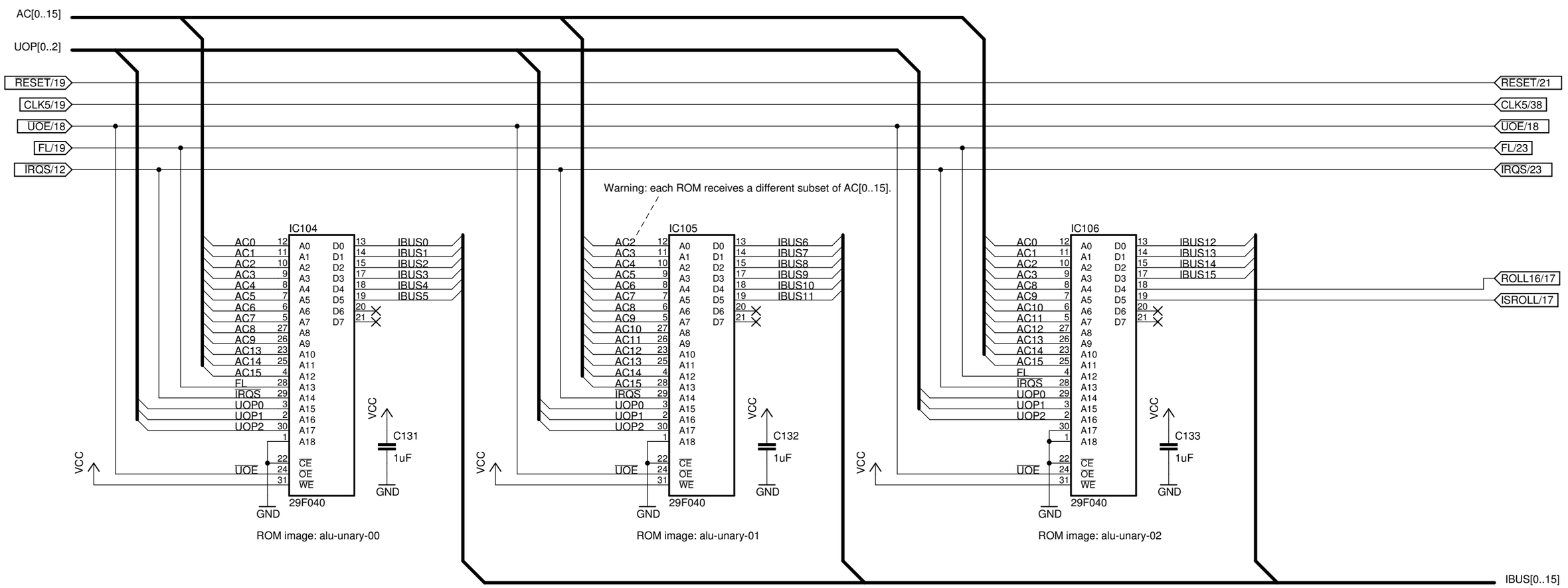
U

Title: cft	
Revision: Rev A	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	19/38
Simulation filename: alu.v	
More Info: http://www.bedroomlan.org/cft	

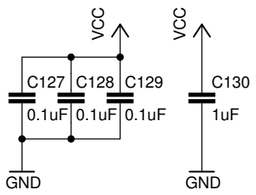
CFT Mini-Computer

ALU Unary Operators and Constant Store

Unary Operations and Constant Store



Decoupling



Notes

ROMs to be socketed for easy re-programming.

TODO:

* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	20/38
Simulation filename: alu.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

8 kW Bank Switching Memory Controller

AB[0..15]

DB[0..15]

RESET/20 → RESET/22

MEM/13 → MEM/24

W/13 → W/22

SYSDEV/11 → SYSDEV/22

Bank Register I/O address decoding

IC108 74HC138N

AB2 AB3 AB4 → A B C

AB5 → G1

AB6 → IC107A (74HC32N) → G2A

W → IC107A (74HC32N)

AB7 → IC107D (74HC32N) → G2B

SYSDEV → IC107D (74HC32N)

Y0 → BANKW0

Y1 → BANKW1

Decodes addr: 0000 0000 0010 0nnn

OUT &0020: Set Bank #0
OUT &0021: Set Bank #1
...
OUT &0027: Set Bank #7

IC109 74HC138N

AB15 → C

VCC → B

MEM → G2A

GND → G2B

Y0 → BANKR0

Y1 → BANKR1

Bank Register Read Select (on MEM access)

8 16-bit Bank Registers

IC112 IC113 IC116 IC117 74HC670N

DB0 DB1 DB2 DB3 → D1 D2 D3 D4

DB4 DB5 DB6 DB7 → D1 D2 D3 D4

AB0 AB1 AB13 AB14 → WA WB RA RB

BANKW0 → GW

BANKR0 → GR

BANKW1 → GW

BANKR1 → GR

Q1 Q2 Q3 Q4 → AE'0 AE'1 AE'2 AE'3

Q1 Q2 Q3 Q4 → AE'4 AE'5 AE'6 AE'7

AB[13..15] select bank register to read.
AB[15] selects which bank register file to access.
AB[14..13] select one of four registers in that file.

The 3 bits AB[13..15] map to 8 bits of extended addresses. This gives 16 - 3 + 8 = 21 bits of addressable memory.

IC114 IC115 IC118 74HC541N

AB13 AB14 → A1 A2

AE'0 AE'1 AE'2 AE'3 AE'4 AE'5 AE'6 AE'7 → A1 A2 A3 A4 A5 A6 A7 A8

AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5 AEXT6 AEXT7 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8

AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5 AEXT6 AEXT7 → A1 A2 A3 A4 A5 A6 A7 A8

BANK0 BANK1 BANK2 BANK3 BANK4 BANK5 BANK6 BANK7 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8

GND → G1 G2

BNK/LNR → G1 G2

BANK[0..7]

AEXT[0..7]

Front Panel Buffer

IC110A 74HC08N

AB15 → 1

FPRAM/28 → 2

3 → AB15RAM

AB15RAM → BNK/LNR

LED-5MM-GREEN R32 330R LED5 → GND

IC111A 74HC112N

BANKW1 → PRE

RESET → CLR

J → Q

CLK

K → Q̄

Q → BNK/LNR

Q̄ → BNK/LNR

BNK/LNR = BANKING → BANKING/30

Writing to bank registers 4-7 enables full banking.
(cancels reset defaults)

The 64 kW address space is split into 8 banks of 8 kW each.

The banking scheme allows page 0 to be swapped for other pages, although since page 0 has special significance, this should probably not be done normally. This leaves 7 banks and 56 kW available for switching.

Decoupling

VCC

C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 — 0.1uF

C146 — 1uF

GND

IC111B 74HC112N

IC110B IC110C IC110D 74HC08N

IC107B IC107C 74HC32N

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

Title:	cft
Revision:	Rev B
Last Change:	25 Feb 2012 18:44:25
Drawn by:	Alexios — 21/38
Simulation filename:	memory.v
More Info:	http://www.bedroomlan.org/cft

U

CFT Mini-Computer

Interrupt Controller

DB[0..15]
AB[0..15]
W/21
SYSDEV/21
RESET/21
W/24
SYSDEV/25
RESET/38

Interrupt Status Register

Interrupt Enable Register

Front Panel Buffers & Connectors

IC120 74HC138N

W, AB5, AB6, AB4, AB7, SYSDEV → A, B, C, G1, G2A, G2B
Y0 → IERW, Y1 → ISRR

Decodes addr: 0000 0000 0001 XXnn

OUT &0010-&001F: write to IER
IN &0010-&001F: read from ISR

IRF[0..7]

IC122 74HC540N

IRF0..IRF7 → A1..A8
Y1..Y8 → DB0..DB7
ISRR → G1, G2

IC126 74HC574N

DB0..DB7 → 1D..8D
1Q..8Q → IEN0..IEN7
IERW → CLK, OC

IC123A 74HC112N

IERW → CLK
RESET → CLR
GND

IEN[0..7]

IC128 74HC541N

IEN0..IEN7 → A1..A8
Y1..Y8 → 22-23-2081 CON9-1..CON9-8
G1, G2 → GND

IC130 74HC541N

IRF[0..7] → A1..A8
Y1..Y8 → 22-23-2081 CON10-1..CON10-8
G1, G2 → GND

IEN[0..7] → 330R RN14A..RN14H → LED-5MM-GREEN LED6..LED13 → GND

IRF[0..7] → 330R RN15A..RN15H → LED-5MM-RED LED14..LED21 → GND

LED Displays (Optional)

IEN[0..7] → RN13 4k7 → GND

Interrupt registers

IRQ[0..7]
IEN[0..7]

IC119A, IC121A, IC124A, IC125A 74HC112N

PRE, J, CLK, K, CLR, Q
IEN0..IEN3 → J
IRQ0..IRQ3 → K
VCC → PRE
Q → IRF0..IRF3
GND → CLR

IRF[0..7]
IEN[0..7]
IRQ[0..7]

IC119B, IC121B, IC124B, IC125B 74HC112N

IEN4..IEN7 → J
IRQ4..IRQ7 → K
Q → IRF4..IRF7

IRF[0..7]

IRQ Generator

IRF0..IRF7 → IC127A, IC127B, IC127C, IC127D 74HC08N
IC129B, IC129C → IC129A 74HC08N → IRQ/25

Note: if the Interrupt Controller is installed, IRQ is always driven.
Nothing else may drive IRQ, not even open drain outputs.

Decoupling

C147..C158 0.1uF, C159 1uF
VCC, GND

IC129D 74HC08N

IC123B 74HC112N

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

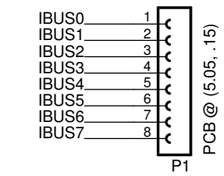
U

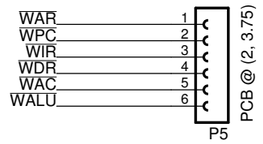
Title: cft	
Revision: Rev A	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	22/38
Simulation filename: to be coded	
More Info: http://www.bedroomlan.org/cft	

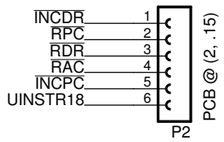
CFT Mini-Computer

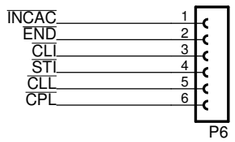
Control Bus Connectors

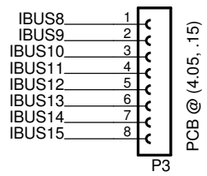
Control Bus Connectors

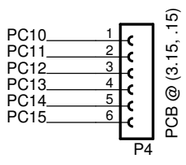


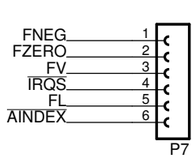












Notes

This is only useful for building the processor on separate cards.

U

Title: cft	
Revision: Rev H	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	23/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Memory (up to 512kW RAM, 512kW ROM)

AB[0..15]
AEXT[0..7]
DB[0..15]
MEM/21
R/13
W/22

AB[0..15]
AEXT[0..7]
DB[0..15]
MEM/37
R/25
W/25

RAM/ROM chip select

AEXT7=0: RAM. AEXT7=0: ROM.

IC131 74HCT138N
AEXT6 AEXT7 MEM VCC GND
A B C G1 G2A G2B Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
RAMEN0 RAMEN1 ROMEN0 ROMEN1

JP4
VCC
ROMUPG

Jumper 1-2: normal operation.
Jumper 2-3: allow in-system ROM upgrade.

JP5
ROMEN1
ROMEN
ROMEN0

Jumper 1-2: ROM at &18000-&1FFFF
Jumper 2-3: ROM at &10000-&1FFFF

JP6
RAMEN1
RAMEN
RAMEN0

Jumper 1-2: RAM at &08000-&0FFFF
Jumper 2-3: RAM at &00000-&0FFFF

Low ROM

IC132 29F040
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
D0 D1 D2 D3 D4 D5 D6 D7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
ROMEN R ROMUPG
CE OE WE
VCC C167 1uF GND

High ROM

IC134 29F040
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
D0 D1 D2 D3 D4 D5 D6 D7
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15
ROMEN R ROMUPG
CE OE WE
VCC C169 1uF GND

Optional LED Display

IC136 74HC540N
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
GND
R33 330R LED-5MM-RED LED22
R34 330R LED-5MM-GREEN LED23
R35 330R LED-5MM-GREEN LED24
R36 330R LED-5MM-GREEN LED25
GND

Low RAM

IC133 AS6C4008
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
D0 D1 D2 D3 D4 D5 D6 D7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
RAMEN R W
CE OE WE
VCC C168 1uF GND

High RAM

IC135 AS6C4008
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
D0 D1 D2 D3 D4 D5 D6 D7
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15
RAMEN R W
CE OE WE
VCC C170 1uF GND

Decoupling

VCC
C160 C161 C162 C163 C164 C165 0.1uF
C166 1uF
GND

TODO:

* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	24/38
Simulation filename: memory.v#banked_memory	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

RS-232 Ports

DB[0..15]
AB[0..15]
RSTHOLD/18
R/24
W/24
SYSDEV/22
RSTHOLD/26
R/26
W/26
SYSDEV/26

Addresses Decoding:

0000'0000'0110'XXXX (&006X) -> Chip #0 (UARTs 0, 1)
0000'0000'0111'XXXX (&007X) -> Chip #1 (UARTs 2, 3)

IC137 74HC138N
AB4 AB5 AB6 AB7 SYSDEV
&000a &001a &002a &003a &004a &005a &006a &007a
CEN0 CEN1

IC138 SC26C92C1N
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
R W CEN0 AB0 AB1 AB2 AB3 RSTHOLD INTRN0 RSCLK
RDN WRN CEN A0 A1 A2 A3 RESET INTRN X1/CLK X2
TXDA RXDA TXDB RXDB
OP0/RTSAN OP1/RTSBN OP2/TXCA/RXCA OP3/CTO/TXCB/RXCB OP4/RXRDY/FFULLA OP5/RXRDY/FFULLB OP6/TXRDYA OP7/TXRDYB
IP0/CTSAN IP1/CTSBN IP2 IP3/TXCA IP4/RXCA IP5/TXCB IP6/RXCB

IC139 SC26C92C1N
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
R W CEN1 AB0 AB1 AB2 AB3 RSTHOLD INTRN1 RSCLK
RDN WRN CEN A0 A1 A2 A3 RESET INTRN X1/CLK X2
TXDA RXDA TXDB RXDB
OP0/RTSAN OP1/RTSBN OP2/TXCA/RXCA OP3/CTO/TXCB/RXCB OP4/RXRDY/FFULLA OP5/RXRDY/FFULLB OP6/TXRDYA OP7/TXRDYB
IP0/CTSAN IP1/CTSBN IP2 IP3/TXCA IP4/RXCA IP5/TXCB IP6/RXCB
TXD3 RXD3 CTS3

IRQ[0..7]
IRQ/22
SV1 SV2
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ
INTRN0 INTRN1

XTAL2 3.6864MHz
C173 0.1uF

C171 100nF
C172 1uF
C174 1uF
C175 1uF

IC140 MAX232
C176 1uF
C177 1uF
C182 1uF
C185 1uF
C188 10uF
C1+ C1- C2+ C2- V+ V- T1IN T2IN R1OUT R2OUT T1OUT T2OUT R1IN R2IN
TXD0 RTS0 RXD0 CTS0

UART0
CON11 G1
CD RXD0 TXD0 DTR GND DSR RTS0 CTS0 RI G2
1M R37
DTE
EARTH

IC141 MAX232
C178 1uF
C179 1uF
C183 1uF
C186 1uF
C189 10uF
TXD1 RTS1 RXD1 CTS1

UART1
CON12 G1
CD RXD1 TXD1 DTR GND DSR RTS1 CTS1 RI G2
1M R38
DTE
EARTH

IC142 MAX232
C180 1uF
C181 1uF
C184 1uF
C187 1uF
C190 10uF
TXD2 RTS2 RXD2 CTS2

UART2
CON13 G1
CD TXD2 RXD2 DTR GND DSR CTS2 RTS2 RI G2
1M R39
DCE
EARTH

FT232 Serial cable pinout

SV3
DTR
RXI (INPUT TTL to USB)
TXO (OUTPUT USB to TTL)
3V3/5V Power input
CTS
TXD3 RXD3 CTS3

TTL (e.g FT232 5V cable)

TODO:
* Bill of Materials
* DRC

D	Title: cft
	Revision: Rev A
	Last Change: 25 Feb 2012 18:44:25
	Drawn by: Alexios — 25/38
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

IDE Bus Interface

AB[0..15]
DB[0..15]
R/25
W/25
RSTHOLD/25
SYSDEV/25
IRQ/25

R/27
W/27
RSTHOLD/38
SYSDEV/27
IRQ/27

Address Decoder (8-port blocks)

IC143 74HC138N

AB4 1 A
AB5 2 B
AB6 3 C
AB7 6 G1
AB3 4 G2A
SYSDEV 5 G2B

Y0 15 &00AX CS1A
Y1 14
Y2 13 &00BX CS3A
Y3 12
Y4 11 &00CX CS1B
Y5 10 &00DX CS3B
Y6 9
Y7 7

Address Decoding:

0000'0000'1aaa'0XXX

0000'0000'1010'0XXX -> &00A0-A7 Port 1 CS1
0000'0000'1011'0XXX -> &00B0-B7 Port 1 CS3

0000'0000'1100'0XXX -> &00C0-C7 Port 2 CS1
0000'0000'1101'0XXX -> &00D0-D7 Port 2 CS3

IRQ[0..7]

SV4
IRQ5 8 7
IRQ6 6 5
IRQ7 4 3
IRQ 2 1

74HCT05N IC144A
VCC R40 4k7
2 1 INTA

SV5
IRQ5 8 7
IRQ6 6 5
IRQ7 4 3
IRQ 2 1

74HCT05N IC144B
VCC R41 4k7
4 3 INTB

DD[0..15]

VCC RN16
1 2 3 4 5 6 7 8 9

IC145 74HCT245N

DB0 2 A1 B1 18 DD0
DB1 3 A2 B2 17 DD1
DB2 4 A3 B3 16 DD2
DB3 5 A4 B4 15 DD3
DB4 6 A5 B5 14 DD4
DB5 7 A6 B6 13 DD5
DB6 8 A7 B7 12 DD6
DB7 9 A8 B8 11 DD7

R 1 DIR
19 G
GND

VCC RN17
1 2 3 4 5 6 7 8 9

IC146 74HCT245N

DB8 2 A1 B1 18 DD8
DB9 3 A2 B2 17 DD9
DB10 4 A3 B3 16 DD10
DB11 5 A4 B4 15 DD11
DB12 6 A5 B5 14 DD12
DB13 7 A6 B6 13 DD13
DB14 8 A7 B7 12 DD14
DB15 9 A8 B8 11 DD15

R 1 DIR
19 G
GND

CFT-to-IDE bus buffers. Could possibly be replaced with HC parts. Could possibly be left out altogether, though they protect the CFT bus from potential problems on the IDE side.

AB[0..15]

VCC CON14 IDE-CONNECTOR

DAA 39 DASP
CS1A 37 CS1FX
CS3A 38 CS3FX
AB0 35 DA0
AB1 33 DA1
AB2 36 DA2
R 25 DIOR
W 23 DIOW
29 DMACK
21 DMARQ
INTA 31 INTRQ
RSTHOLD 1 RESET
34 PDIAG

DD0 17 DD0
DD1 15 DD1
DD2 13 DD2
DD3 11 DD3
DD4 9 DD4
DD5 7 DD5
DD6 5 DD6
DD7 3 DD7
DD8 4 DD8
DD9 6 DD9
DD10 8 DD10
DD11 10 DD11
DD12 12 DD12
DD13 14 DD13
DD14 16 DD14
DD15 18 DD15
IOCS16 32
IORDY 27
CSEL 28
GND

VCC CON15 IDE-CONNECTOR

DAB 39 DASP
CS1B 37 CS1FX
CS3B 38 CS3FX
AB0 35 DA0
AB1 33 DA1
AB2 36 DA2
R 25 DIOR
W 23 DIOW
29 DMACK
21 DMARQ
INTB 31 INTRQ
RSTHOLD 1 RESET
34 PDIAG

DD0 17 DD0
DD1 15 DD1
DD2 13 DD2
DD3 11 DD3
DD4 9 DD4
DD5 7 DD5
DD6 5 DD6
DD7 3 DD7
DD8 4 DD8
DD9 6 DD9
DD10 8 DD10
DD11 10 DD11
DD12 12 DD12
DD13 14 DD13
DD14 16 DD14
DD15 18 DD15
IOCS16 32
IORDY 27
CSEL 28
GND

DD[0..15]

DAA
JP7 1 2
LED-5MM-RED LED26 R42 330R VCC

DAB
JP8 1 2
LED-5MM-RED LED27 R43 330R VCC

For external LEDs (e.g. MISCn on the front panel), remove jumper shunt and connect pin 1 to external LED.

VCC
C191 1uF
C192 100nF
C193 100nF
C194 100nF
C195 100nF
C196 1uF
GND

74HCT05N IC144C
74HCT05N IC144D
IC144F 74HCT05N
IC144E 74HCT05N
GND

TODO:

* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials

D	
Title: cft	
Revision: Rev A	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	26/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Clock, Timers & NVRAM

Real Time Clock & NVRAM

Six Programmable Counters

Address Decoder (8-port blocks)

Address Decoder (4-port blocks)

Addresses Decoding:

0000'0000'1000'XXXX (&008X) -> 16 bytes of NVRAM/clock data

0000'0000'1001'00xx (&0090-93) -> NVRAM addr offset (bits 4-10). Clock = &7F

0000'0000'1001'01xx (&0094-97) -> Timer #1
0000'0000'1001'10xx (&0098-9B) -> Timer #2
0000'0000'1001'11xx (&009C-9F) -> Timer Control Register (16 bits)

Interrupt Selection Jumpers

32,768 Hz clock

Interrupt Mask Reg

Counter Interrupt Enables

Counter Clock Select MUXes

Gate/Output Expansion

TODO:

* Bill of Materials
* DRC

Title: cft	
Revision: Rev A	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	27/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

D

CFT Mini-Computer

Front Panel: Switch Register and Switches 1/2

FPCLKEN/2 → FPCLKEN/36

Switch Register

S2, S3, S4, S5, S6, S7, S8, S9 → 22-23-2081 CON16-1 … CON16-8

S10, S11, S12, S13, S14, S15, S16, S17 → 22-23-2081 CON17-1 … CON17-8

All switches: pin 2 → GND

Power Key Switch

Position 1: 2-1, 5-4 (off)
Position 2: 2-3, 5-4 (on, panel lock)
Position 3: 2-3, 5-6 (on, panel unlock)

ATX Power Supply Unit assumed.

S18: pin 2 → GND; pin 3 → FPPWRON/34; pin 5 → GND; pin 6 → FPLOCK/29

Keeps power on when a break-before-make key switch moves between ON & PANEL positions.

Activates the Power Supply Unit, turning the computer on.

Disables the panel switches.

C229 1uF

Verbose / Quiet — S19: pin 2 → GND; pin 3 → FPLEDSON/30

Disables many debugging lights to avoid visual overload.

C230 1uF

ROM High — S20: pin 2 → GND; pin 3 → FPROM/34

RAM High — S20: pin 2 → GND; pin 3 → FPRAM/34

FPROM & FPRAM are not debounced because they are handled off-board by a clocked J-K flip-flop.

Fast (10) — S21: pin 2 → GND; pin 3 → FPFAST/34

Slow 1 (11) — S21: pin 5 → GND; pin 6 → FPSLOW/34

Slow 2 (01) — S21: pin 5 → GND; pin 6 → FPSLOW/34

Fast: FPFAST=1, FPSLOW=0
Slow 1: FPFAST=0, FPSLOW=0
Slow 2: FPFAST=0, FPSLOW=1

Microstep — S22: pin 2 → GND; pin 3 → FPSTEP/34

Step Instruction — S22: pin 2 → GND; pin 3 → FPUSTEP/34

SAFE

SAFE/29

RN19 10k

RN20A 50k

RN20B 50k

RN20C 50k

RN20D 50k

C223 +1uF

C224 1uF

C225 +1uF

C226 1uF

IC165D 74HCT00N

IC161A 74HC14N

IC164A 74HC04N

IC161B 74HC14N

IC164B 74HC04N

IC161C 74HC14N

IC164C 74HC04N

IC161D 74HC14N

IC164D 74HC04N

IC166 74HC373N

OC, ENC → GND

Clock speed latch: clock speed may be changed only when the clock is stopped (CLKEN is high)

FPSTEP-IN

IC165B 74HCT00N

Auto-repeat for Step switch

FPSTEP-IN

TW = 0.25 x R KOhms x C pF (1 + 0.7/R kOhms)

R48 200k

C222 100uF

D2 1N4148

47k = 1.19s

IC162A 74LS123N

IC165A 74HCT00N

NB: MUST be HCT (TTL inputs)

IC163 LM555N

C227 22nF

C228 4.7uF

R50 1k

R49 180k

R51 200k

CAUTION: autorepeat freq must be <= 1Hz
or STEP mechanism may fail under autorepeat conditions.
180k in-series resistor ensures minimum period is ~1s.

Decoupling

C215 C216 C217 C218 C219 C220 0.1uF each

C221 1uF

IC165C 74HCT00N

IC162B 74LS123N

Note: some gates shared with next sheet.

TODO:

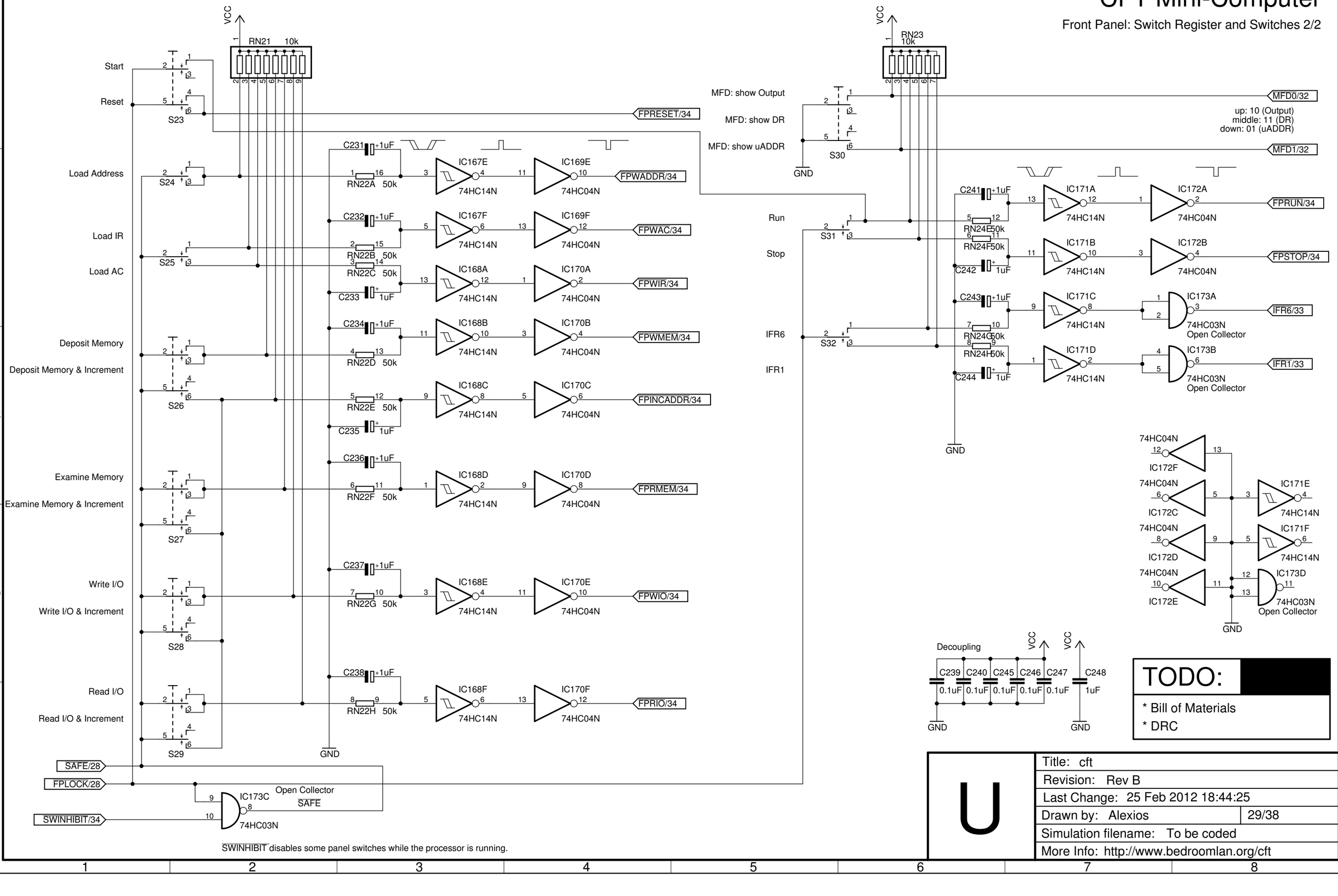
* Bill of Materials
* DRC

Title:	cft
Revision:	Rev B
Last Change:	25 Feb 2012 18:44:25
Drawn by: Alexios	28/38
Simulation filename:	To be coded
More Info:	http://www.bedroomlan.org/cft

U

CFT Mini-Computer

Front Panel: Switch Register and Switches 2/2



SWINHIBIT disables some panel switches while the processor is running.

TODO:

* Bill of Materials
* DRC

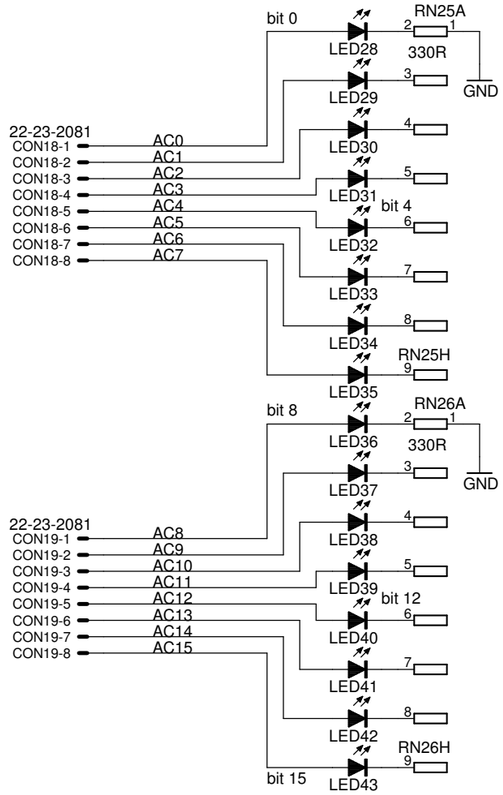
U	Title: cft
	Revision: Rev B
	Last Change: 25 Feb 2012 18:44:25
	Drawn by: Alexios — 29/38
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

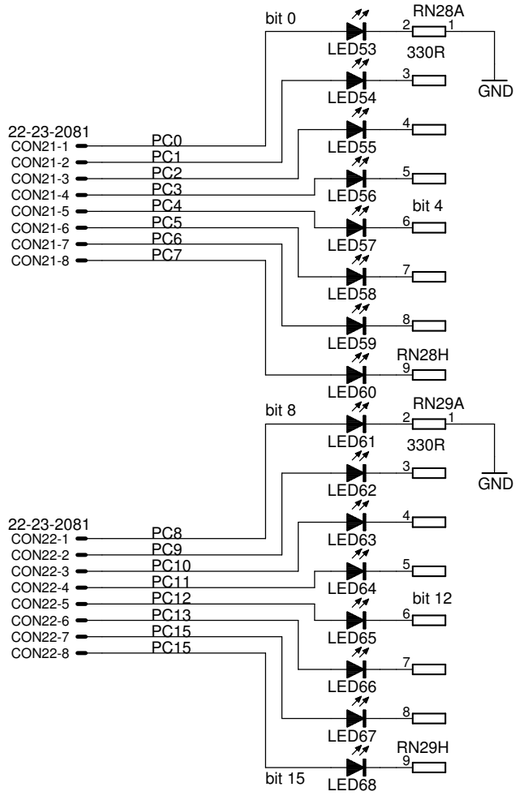
Front Panel: LEDs 1

FPLEDSON/28

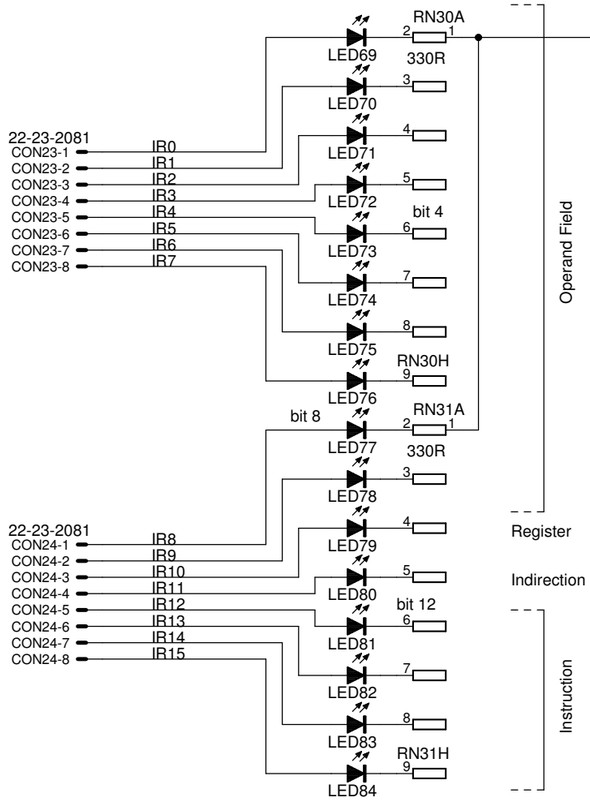
Accumulator Display



Program Counter Display



Instruction Register Display

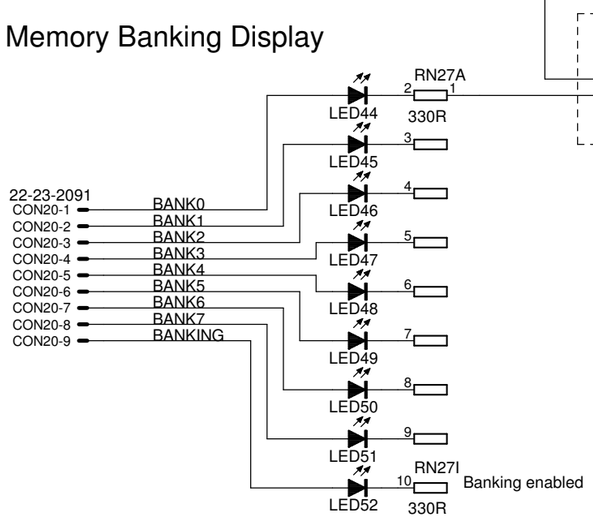


JP10

Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

Memory Banking Display



JP9

Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

TODO:

* DRC

U	Title: cft
	Revision: Rev B
	Last Change: 25 Feb 2012 18:44:25
	Drawn by: Alexios — 30/38
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Front Panel: LEDs 2

FPLEDSON/30 → FPLEDSON/33
FPRUN/34 → FPRUN/34
FPSTOP/34 → FPSTOP/34
FPFETCH/32 → FPFETCH/32
FPEXEC/32 → FPEXEC/32
BIRQS/6 → BIRQS/32

Microcode Vector Display

RN32A 150R: LED85, LED86, LED87, LED88, LED89, LED90, LED91, LED92
RN33A 330R: LED93, LED94, LED95, LED96, LED97, LED98, LED99, LED100
RN34A 330R: LED101, LED102, LED103, LED104, LED105, LED106, LED107, LED108
RN32H: LED92
RN33H: LED100
RN34H: LED108

Read Unit (green): BRUNIT0, BRUNIT1, BRUNIT2, BRUNIT3
Write Unit (red): BWUNIT0, BWUNIT1, BWUNIT2, BOPIF0
OPIFn (amber): BOPIF1, BOPIF2, BOPIF3, BINCAC, BCPL, BCLL, BSTI, BCLI

INCAC, CPL, CLL, STI, CLI, INCPC, INCDR, UINSTR18, MEM, IO, R, W, END

BINCPC, BINCDR, BUINSTR18, BMEM, BIO, BR, BW, BEND

JP12 — Terse mode configuration jumper.
Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

JP11 — Terse mode configuration jumper.
Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

Flag Display

RN35A 330R: LED109, LED110, LED111, LED112, LED113
RN35H

BFNEG, BFZERO, BFV, BIRQS, BFL

N, Z, V, I, L

State & Miscellaneous lights

RN36A 330R:

FPRUN	LED114	Run (green)
FPSTOP	LED115	Stop (red)
FPFETCH	LED116	Fetch (orange)
FPEXEC	LED117	Execute (orange)
INTERRUPT	LED118	Interrupt (orange)
MISC1	LED119	Misc light 1 (green)
MISC2	LED120	Misc light 2 (green)
MISC3	LED121	Misc light 3 (green)

RN36H

IC174A / IC174B: 74LS123N
BIRQS, R52 330k, C249 1uF
VCC
SV10
GND

TODO:

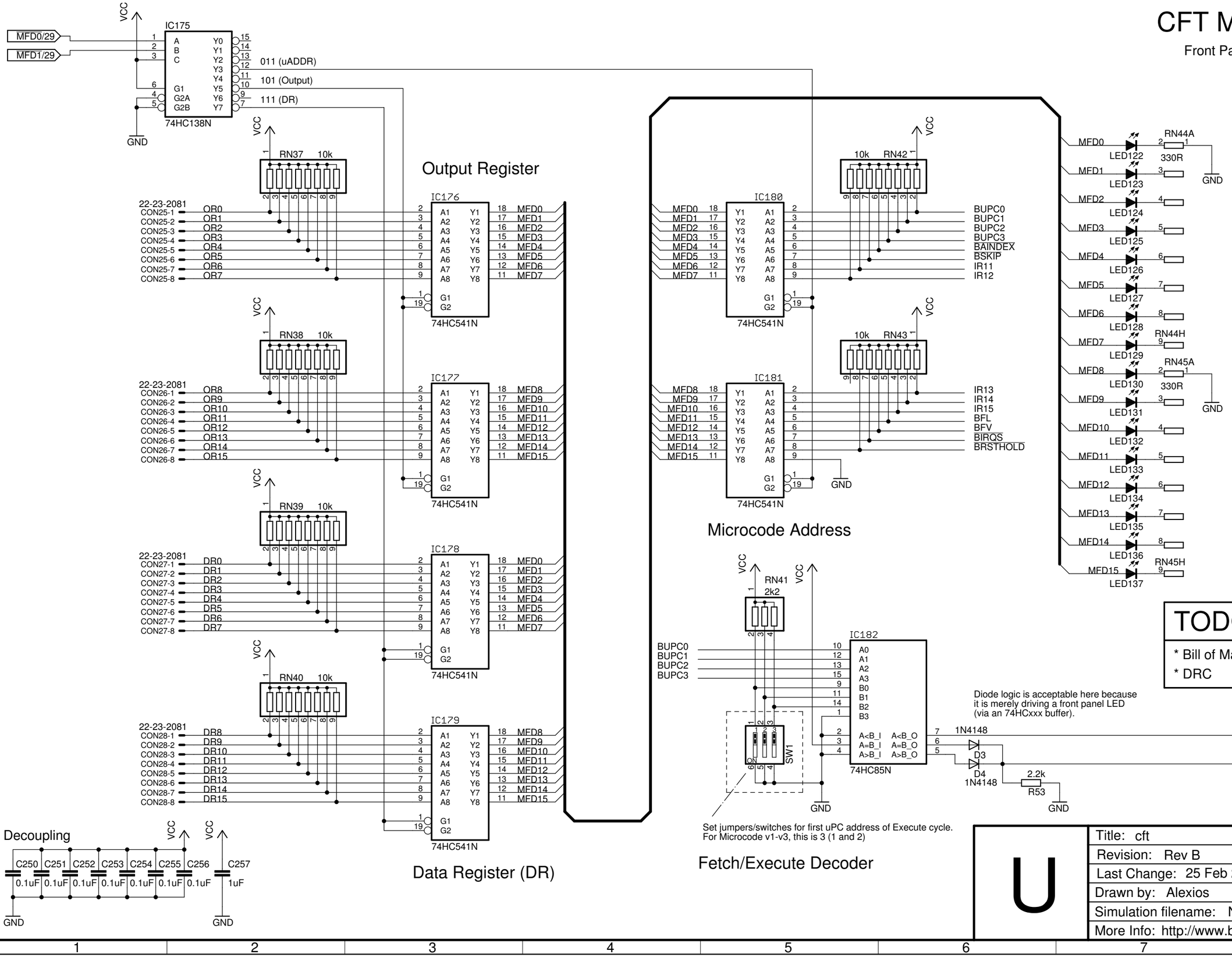
* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	31/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Multi-Function Display



TODO:

* Bill of Materials
* DRC

U	Title: cft
	Revision: Rev B
	Last Change: 25 Feb 2012 18:44:25
	Drawn by: Alexios — 32/38
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Front Panel: Interrupt LEDs

FPLEDSON/31

Interrupt Status Display

22-23-2081
CON29-1 IFR0
CON29-2 IFR1
CON29-3 IFR2
CON29-4 IFR3
CON29-5 IFR4
CON29-6 IFR5
CON29-7 IFR6
CON29-8 IFR7

VCC

R54 330k, C263 1uF, IC183A
R55 330k, C264 1uF, IC183B
R56 330k, C265 1uF, IC184A
R57 330k, C266 1uF, IC184B
R58 330k, C267 1uF, IC185A
R59 330k, C268 1uF, IC185B
R60 330k, C269 1uF, IC186A
R61 330k, C270 1uF, IC186B

74LS123N

GND

JP13

Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled on Verbose mode.
No shunt: always off.

Common cathode tri-colour LEDs may be used here.

LED-5MM-RED LED138 LED139 LED140 LED141 LED142 LED143 LED144 LED145
LED-5MM-GREEN LED146 LED147 LED148 LED149 LED150 LED151 LED152 LED153

bit 0 ... bit 0

330R RN46A, RN46B, RN46C, RN46D, RN46E, RN46F, RN46G, RN46H
330R RN47A, RN47B, RN47C, RN47D, RN47E, RN47F, RN47G, RN47H

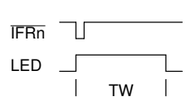
22-23-2081
IEN0 CON30-1
IEN1 CON30-2
IEN2 CON30-3
IEN3 CON30-4
IEN4 CON30-5
IEN5 CON30-6
IEN6 CON30-7
IEN7 CON30-8

Red
Green

LED legend

Off: interrupt line disabled, no activity
Red: interrupt line disabled but activity seen
Steady green: interrupt line enabled, no activity
Green with yellow/orange flashes: enabled interrupt activity

IFRn pulses are not normally visible to the naked eye.
'123 Dual Monostable Vibators produce pulses for IRQ signals.



TW (ns) = 0.25 x R KOhms x C pF (1 + 0.7/R kOhms)

R=330k, C=1uF: ~0.08s delay

Decoupling

VCC
C258 0.1uF, C259 0.1uF, C260 0.1uF, C261 0.1uF
C262 1uF
GND

TODO:

* Bill of Materials
* DRC

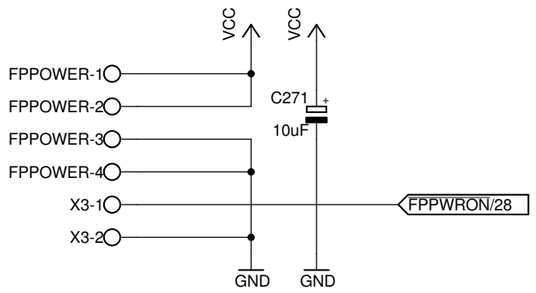
U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	33/38
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

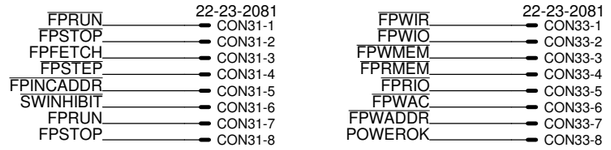
Front Panel: Connectors

Front Panel Power Input



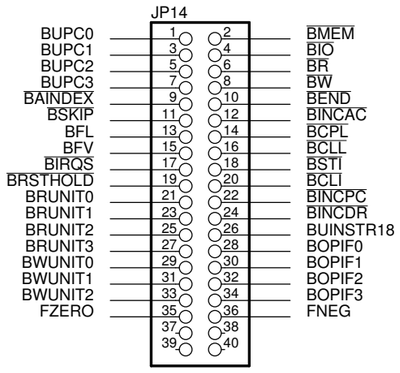
Assumes ATX power supply.

Front Panel Controller Connections

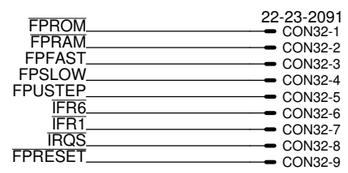


Connector to Front Panel Controller Card.

Sequencer



Connections to Other Cards



TODO:

* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	34/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: System Device

AB[0..15]
DB[0..15]

FPWADDR/34
FPWAC/34
FPWIR/34
FPWMEM/34
FPWIO/34
R/27
W/27

FPWADDR/37
FPWAC/37
FPWIR/37
FPWMEM/37
FPWIO/37
R/37
W/37

IC187 — 74HC138N

Decodes I/O 0008-000F

AB4, AB5, AB6, AB3, AB7, SYSDEV/27

IC190 — 74HC138N

AB0, AB1, AB2, R

IN &0008
IN &0009 (dip switches)

IC191 — 74HC138N

AB0, AB1, AB2, W

OUT &0008 (OR)
OUT &000F (HALT) → FPHALT/36

IC194A — 74HC21N

IC195B — 74HC21N

RN48 2k2
RN49 2k2
RN50 2k2
RN51 2k2

Dip Switch Register (optional)

SW2 (Bit 0 … Bit 7)
SW3 (Bit 8 … Bit 15)

IC188 — 74HC541N

IC189 — 74HC541N

TP20

Output Register

IC192 — 74HCT574N

CON34-1 … CON34-8

IC193 — 74HCT574N

CON35-1 … CON35-8

Switch Register

IC196 — 74HC541N

CON36-1 … CON36-8

IC197 — 74HC541N

CON37-1 … CON37-8

TP22

GND, VCC

Decoupling

C272 C273 C274 C275 C276 C277 C278 C279 C280 C281 — 0.1uF
C282 — 1uF

TODO:

* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	35/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Run/Stop State Machine

HALT/5
FPRUN/34
FPSTOP/34
FPFETCH/34
FPSTEP/34
FPHALT/35
POWEROK/34
CLK1/27

HALT/38
FPRUN/34
FPSTOP/34
FPFETCH/34
FPSTEP/34
FPHALT/35
POWEROK/34
CLK1/38

FPFETCH
FPSTEP
FPHALT
FPSTOP
POWEROK
CLK1

Falling edge detection

IC198C 74HC00N
IC198A 74HC00N
IC198D 74HC00N
IC198B 74HC00N
IC202D 74HC00N

Both CLKEN and HALT are driven low when the processor is stopped.
CLKEN stops the clock. HALT tristates the Control Unit so the front
panel can drive the processor's control signals.
Since other units could also assert HALT, CLKEN is the only way
we have of knowing we've stopped the processor.

To Clock Generator
FPCLKEN/28
TP23

STOP line goes high whenever HALT is active (including wait states,
since HALT is open collector.

HALT (pulled up by Control Unit)

IC202A 74HC00N
Front Panel LED
FPSTOP/34

IC199A 74HC112N
IC200A 74HC01N
Open Collector
IC201A 74HC00N

CLK1
STOP
POWEROK
GND

IC202B 74HC00N
IC202C 74HC00N
Front Panel LED
FPRUN/37

The POWEROK pulse makes the computer power on halted.

VCC
IC199B 74HC112N
STEP/
FETCH/
GND

Disable Front Panel Switches while running
SWINHIBIT/34
TP21

ISRUN = ISRUN1 + IRSUN2
HALT = ISRUN = ISRUN1 + IRSUN2
HALT = RUN = IRSUN1 + IRSUN2
HALT = ISRUN1 NAND ISRUN2

ISSTOP = ISRUN = HALT

Decoupling
VCC
C283 0.1uF
C284 0.1uF
C285 0.1uF
C286 0.1uF
C287 0.1uF
C288 1uF
GND

IC201C 74HC00N
IC201D 74HC00N
Open Collector
IC200C 74HC01N
IC201B 74HC00N
Open Collector
IC200B 74HC01N
IC200D 74HC01N
Open Collector

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	36/38
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Sequencer

The '125 buffers act as purposefully slow open collector buffers.
When the FP input is high, the buffer is tri-stated. When it is low,
the buffer drives, but only low (inputs connected to GND).
In addition, the tPZL delay (typical 15ns) acts as a delay circuit
that gives time for the switch register enables to be decoded
and the switch register value put on the IBUS.

FPINCADDR/34
FPRMEM/34
FPRIO/34
FPWADDR/35
FPWAC/35
FPWIR/35
FPWMEM/35
FPWIO/35
FPRUN/36

FPWADDR
FPWAC
FPWIR

IC209A 74HC125N → WPC/23
IC209C 74HC125N → WDR/23
IC209D 74HC125N → WAC/23
IC210A 74HC125N → WIR/23

Sequencer: MCSTART, MC0, MC1, MC2, MC3

Write Cycle: MCSTART, WAR, RPC, MEM / IO, INCPC, RAC, W

Read Cycle: MCSTART, WAR, RPC, MEM / IO, INCPC, R, WAC

IC209B 74HC125N, R62 2k2, VCC

74HC21N IC203A: FPWIO, FPWMEM, FPRIO, FPRMEM
74HC08N IC206B: FPWIO, FPRIO
74HC08N IC206A: FPWMEM, FPRMEM
74HC08N IC206D: FPRIO, FPRMEM
74HC08N IC206C: FPWIO, FPWMEM

MCSTART

These ICs receive input from the 74LS123 chips
and must be TTL compatible.

IC207A 74HCT32N: FPMEM, MC2
IC208A 74HCT32N: FPIO, MC2
IC207D 74HCT32N: FPR, MC2
IC208D 74HCT32N: FPW, MC3
IC207B 74HCT32N: FPINCADDR, MC2
IC208B 74HCT32N: MC1, MC0
IC208C 74HCT32N: FPW, MC2
IC207C 74HCT32N: FPR, MC3

IC211 74HCT541N
A1 A2 A3 A4 A5 A6 A7 A8 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1, G2

Y1 → MEM/38
Y2 → IO/38
Y3 → R/38
Y4 → W/38
Y5 → INCPC/23
Y6 → RPC/23
Y7 → WAR/23
Y8 → RAC/23

IC210B 74HC125N: WAC

GND

As long as the processor is halted and the control unit tri-stated,
the front panel controller will not introduce contention.
Also, contention between the FPWAC signal and cycle sequencer
cannot happen because even if multiple switches are operated
simultaneously, WAC is either tri-stated or driven low.

IC210C 74HC125N
IC210D 74HC125N
74HC21N IC203B

GND

Decoupling

C289 C290 C291 C292 C293 C294 C295 C296 C297 C298 0.1uF
C299 1uF
VCC
GND

TW = ~20-45us: R63 1k, C300 100nF, IC204A 74LS123N, TP16, MC0
TW = ~94-211us: R64 4k7, C301 100nF, IC204B 74LS123N, TP17, MC1
TW = ~94-211us: R65 4k7, C302 100nF, IC205A 74LS123D, TP18, MC2
TW = ~20-45us: R66 1k, C303 100nF, IC205B 74LS123D, TP19, MC3

TW = 0.25 x R KOhms x C pF (1 + 0.7/R kOhms)

TODO:

* Write & Verify Verilog Model
* Bill of Materials
* DRC

U	Title: cft
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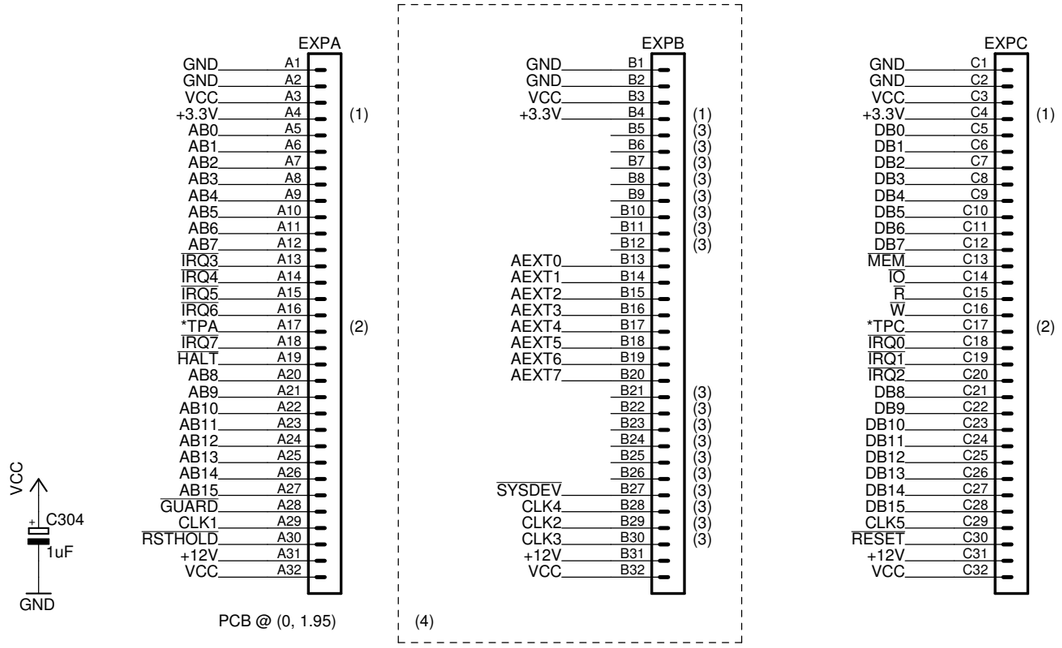
	Drawn by: Alexios — 37/38
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Bus Connectors

Expansion Bus (computer bus)



Notes

(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it. It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) Bit18 of the microinstruction field. Currently unused, reserved for future expansion.

H1 HOLE	@ (.175, 3.675)
H2 HOLE	@ (5.8, 3.675)
H3 HOLE	@ (5.8, .225)
H4 HOLE	@ (.175, .225)

U

Title: cft	
Revision: Rev B	
Last Change: 25 Feb 2012 18:44:25	
Drawn by: Alexios	38/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	