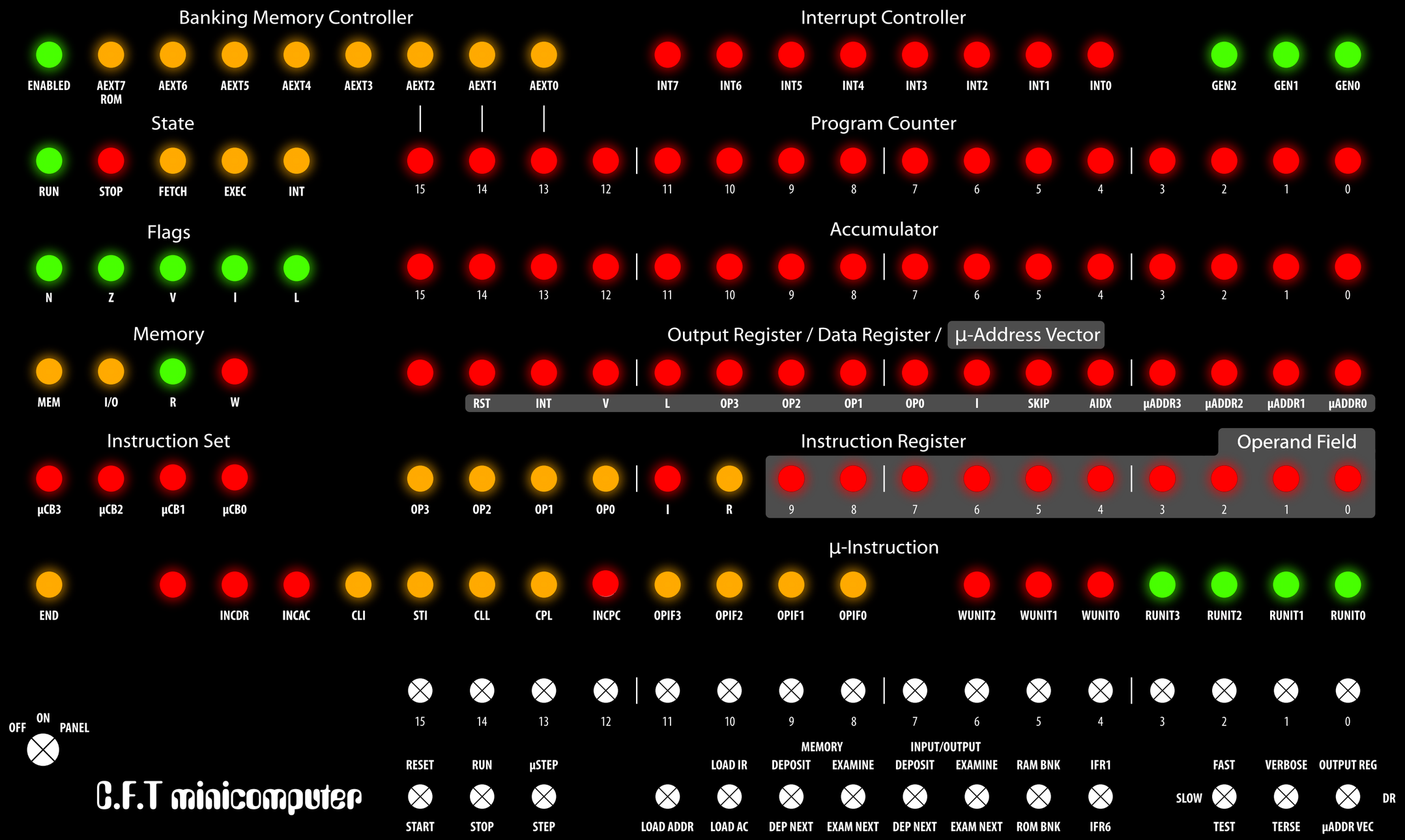
Banking Memory Controller
ENABLED
AEXT7 ROM
AEXT6
AEXT5
AEXT4
AEXT3
AEXT2
AEXT1
AEXT0
Interrupt Controller
INT7
INT6
INT5
INT4
INT3
INT2
INT1
INT0
GEN2
GEN1
GEN0
State
RUN
STOP
FETCH
EXEC
INT
Program Counter
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Flags
N
Z
V
I
L
Accumulator
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Memory
MEM
I/O
R
W
Output Register / Data Register / µ-Address Vector
RST INT V L OP3 OP2 OP1 OP0 I SKIP AIDX µADDR3 µADDR2 µADDR1 µADDR0
Instruction Set
µCB3
µCB2
µCB1
µCB0
OP3
OP2
OP1
OP0
I
R
Instruction Register
Operand Field
9 8 7 6 5 4 3 2 1 0
µ-Instruction
END
INCDR
INCAC
CLI
STI
CLL
CPL
INCPC
OPIF3
OPIF2
OPIF1
OPIF0
WUNIT2
WUNIT1
WUNIT0
RUNIT3
RUNIT2
RUNIT1
RUNIT0
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OFF
ON
PANEL
RESET
RUN
µSTEP
START
STOP
STEP
LOAD ADDR
LOAD IR
LOAD AC
MEMORY
DEPOSIT
EXAMINE
DEP NEXT
EXAM NEXT
INPUT/OUTPUT
DEPOSIT
EXAMINE
RAM BNK
IFR1
DEP NEXT
EXAM NEXT
ROM BNK
IFR6
FAST
SLOW
VERBOSE
OUTPUT REG
DR
TEST
TERSE
µADDR VEC
C.F.T minicomputer