CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

- OD This input signal is open drain.
- TTL This input signal may be at TTL logic levels.
- Z This input may be at High Impedance.
- Z* This input (local to this board) may be at High Impedance.

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Note: the shading patterns below are in colour, and not distinguishable on black & white hard copies.

Circuits in need of improvement are marked like this.

Circuits known to be incorrect are marked like this.

Obsolete sections or circuits are marked like this.

Changes from previous revision are marked like this.

D

Title: front-panel-revC	
Revision: Rev B	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	1/13
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Switch Wiring

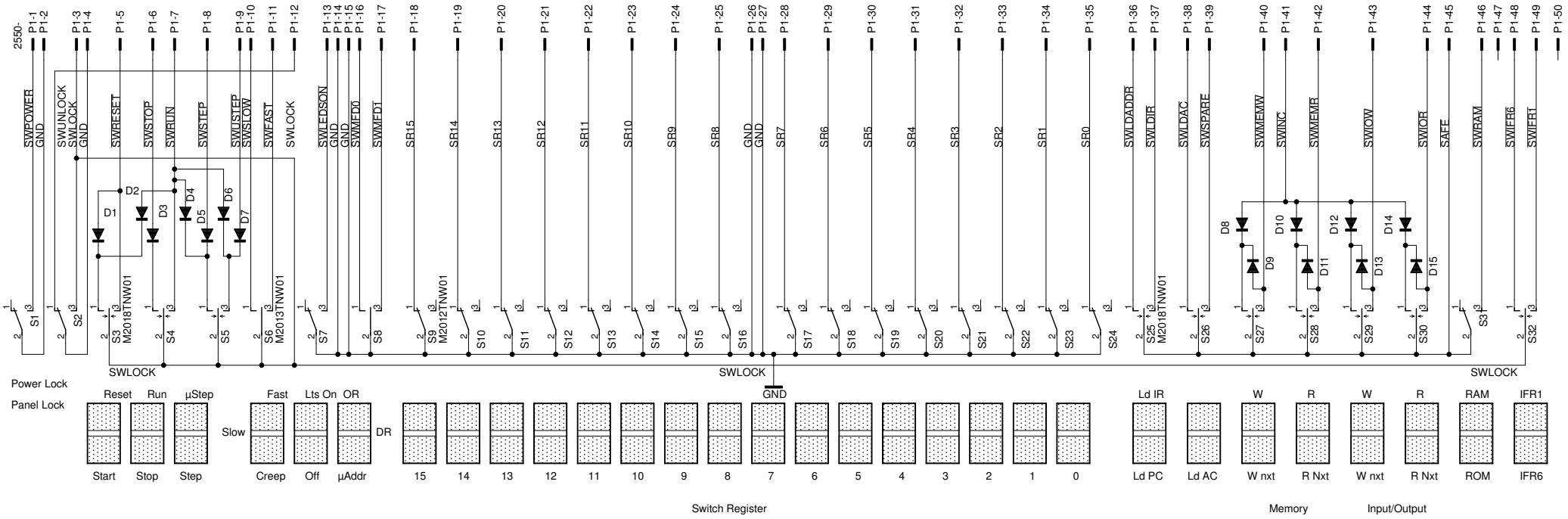
Left switch actuation truth table

	SWRESET	SWRUN	SWSTOP	SWSTEP	SWUSTEP
Reset	L				
Start	L	L			
Run		L			
Stop			L		
Step		L **		L	
uStep		L **			L

* The machine is temporarily set to the RUN state during stepping.

Right switch actuation truth table

	SWMEMR	SWMEMW	SWIOR	SWIOW	SWINC
Memory Read	L				
Memory Read Next	L	L			L
Memory Write		L			
Memory Write Next			L		L
I/O Read			L		
I/O Read Next				L	L
I/O Write				L	
I/O Write Next					L



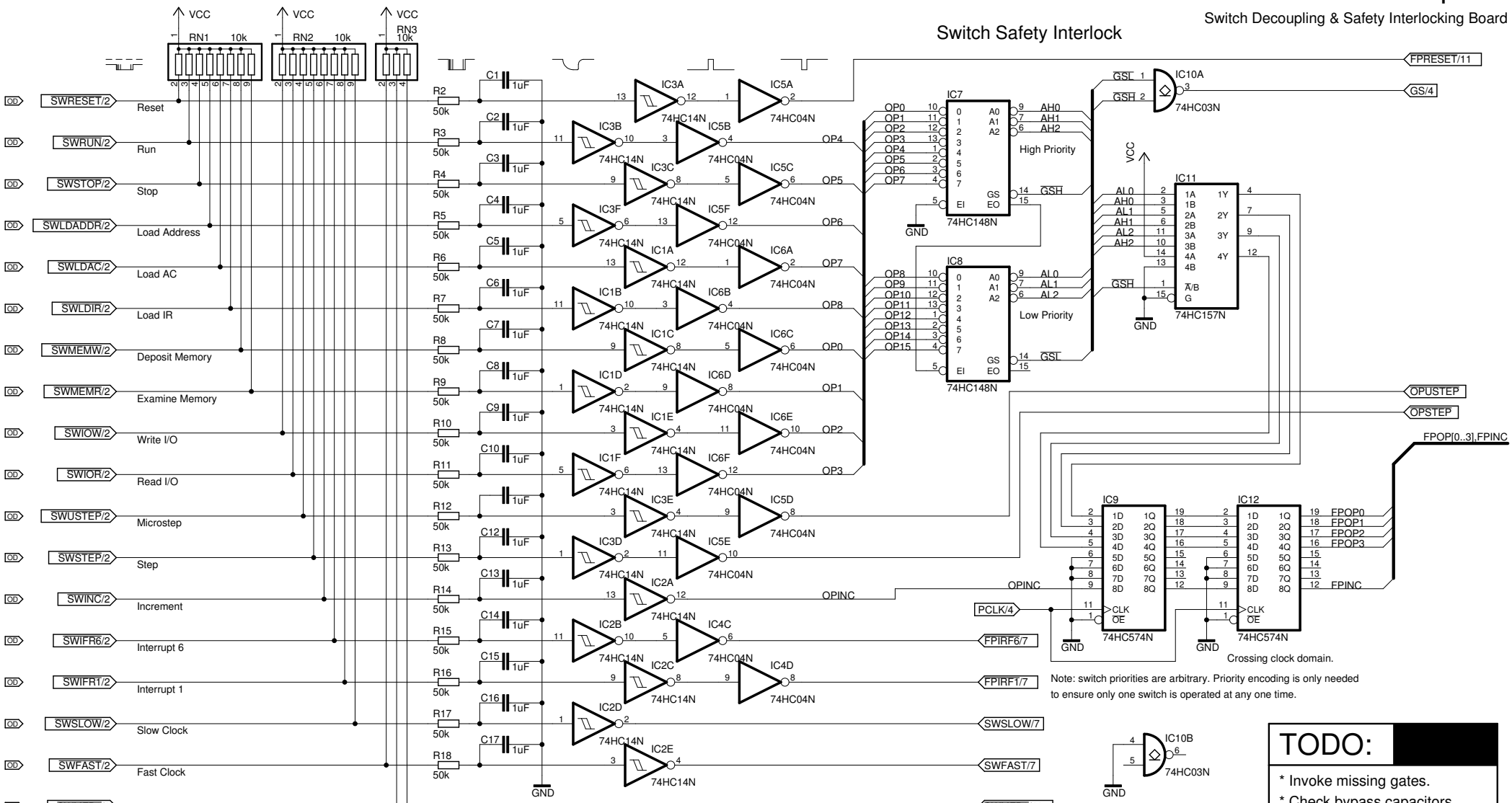
U	Title: front-panel-revC
	Revision: Rev D
	Last Change: 15 Oct 2013 11:01:55
	Drawn by: Alexios 2/13
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

All inputs from switch board are 'open drain'.
(no drains involved, just switches; they're either at Z or L states)

CFT Mini-Computer

Switch Decoupling & Safety Interlocking Board

Switch Safety Interlock



TODO:

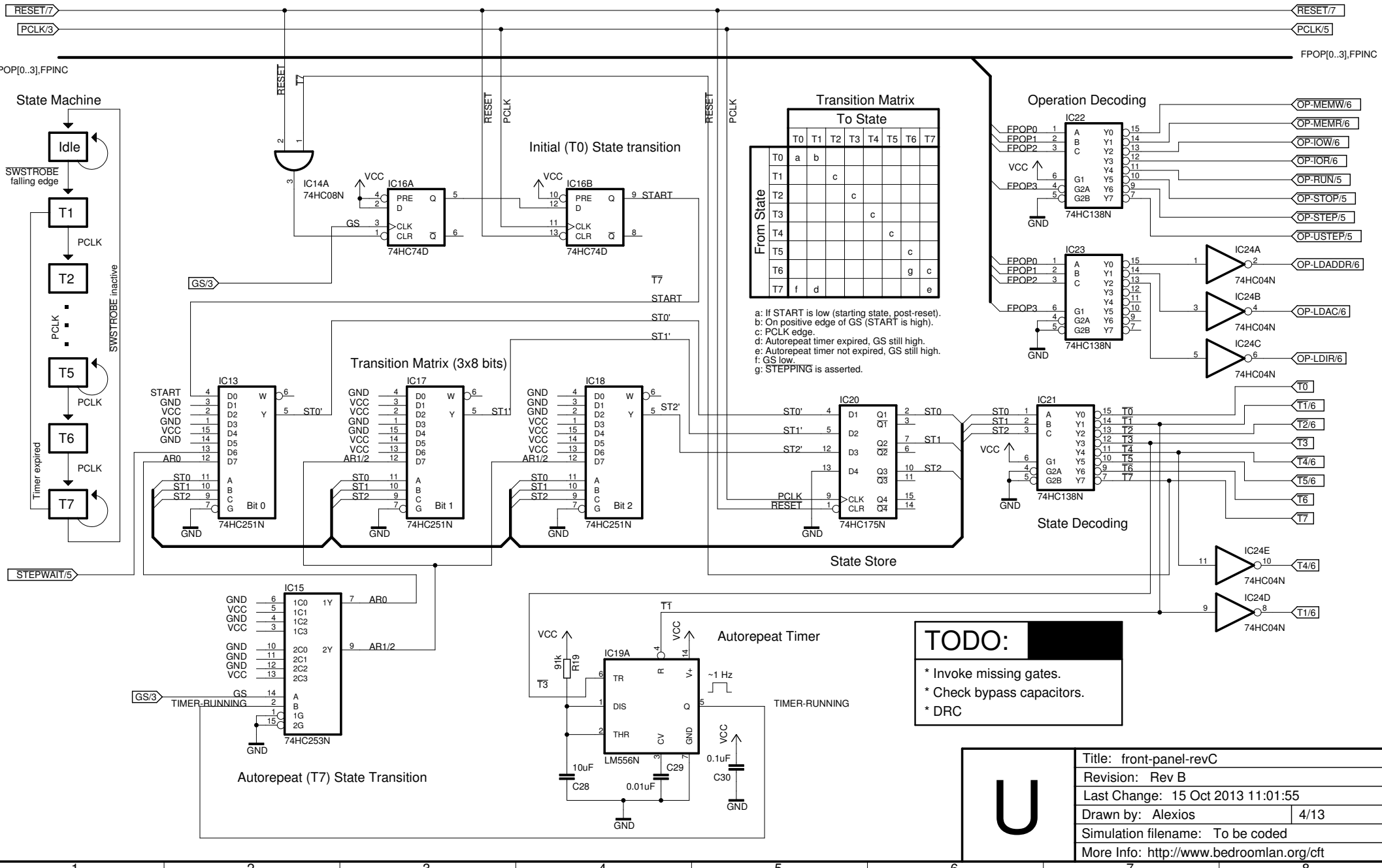
- * Invoke missing gates.
- * Check bypass capacitors.
- * DRC

U

Title: front-panel-revC	
Revision: Rev B	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	3/13
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

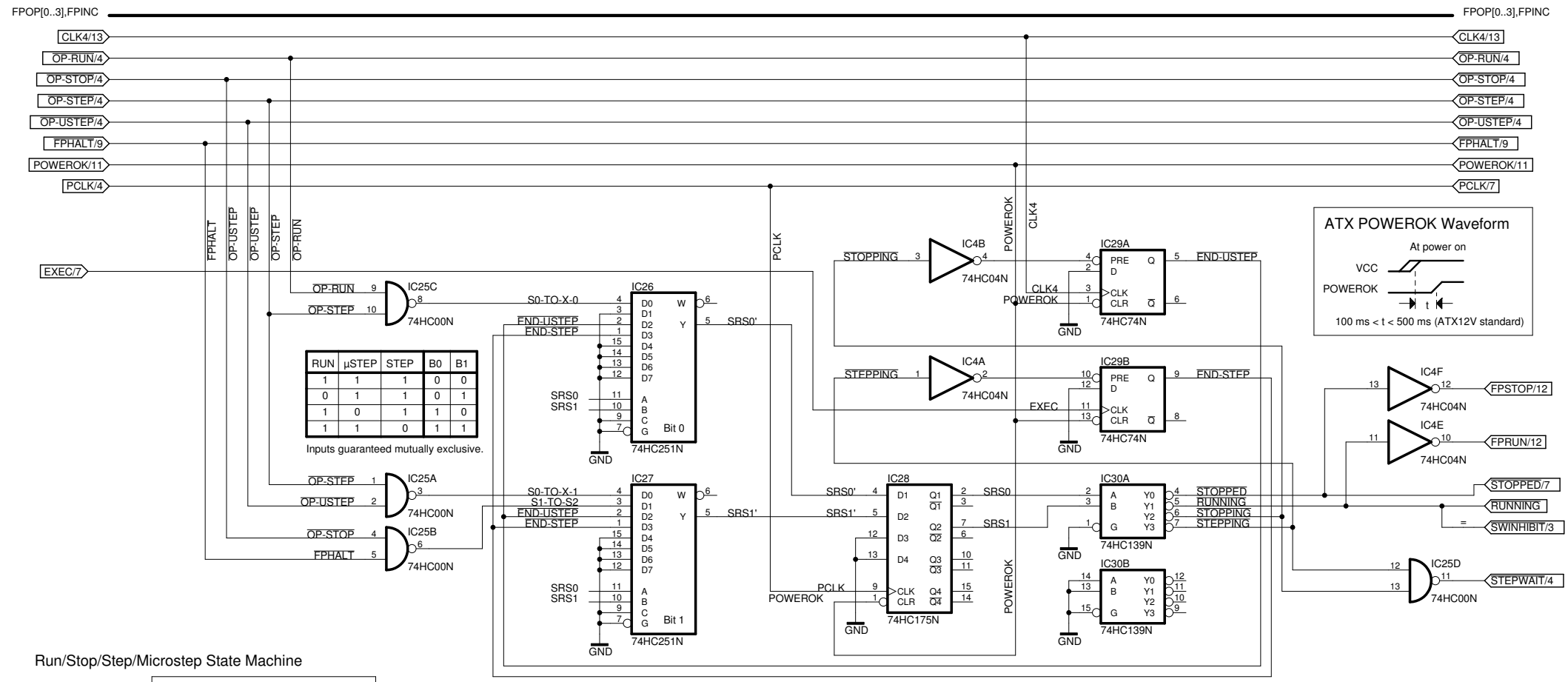
CFT Mini-Computer

Front Panel: Switch State Machine



CFT Mini-Computer

Front Panel: Start/Stop/Step State Machine



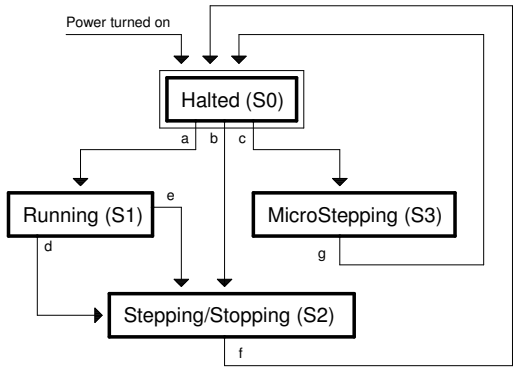
RUN	µSTEP	STEP	B0	B1
1	1	1	0	0
0	1	1	0	1
1	0	1	1	0
1	1	0	1	1

Inputs guaranteed mutually exclusive.

ATX POWEROK Waveform

100 ms < t < 500 ms (ATX12V standard)

Run/Stop/Step/Microstep State Machine



Step: run the processor until it enters the next execute state.
Stop synchronously to a processor clock cycle.
Microstep (µStep): run the processor until the beginning of the next clock cycle.
Stop synchronously to a processor clock cycle.
Stop: halt the processor after the next instruction is fetched
but before it is executed (onset of fetch cycle).

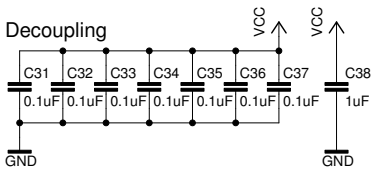
Transition Matrix

From State \ To State	S0	S1	S2	S3
S0		a	b	c
S1			d,e	
S2	f			
S3	g			

S0: Halted
S1: Running
S2: Microstepping/Stopping
S3: Stepping

a: RUN actuated (OP-RUN low).
b: µSTEP actuated (OP-USTEP low).
c: STEP actuated (OP-STEP low).
d: STOP actuated (OP-STOP low).
e: FPHALT asserted (low).
f: CLK4 rising edge.
d: FETCH rising edge.

Decoupling



TODO:

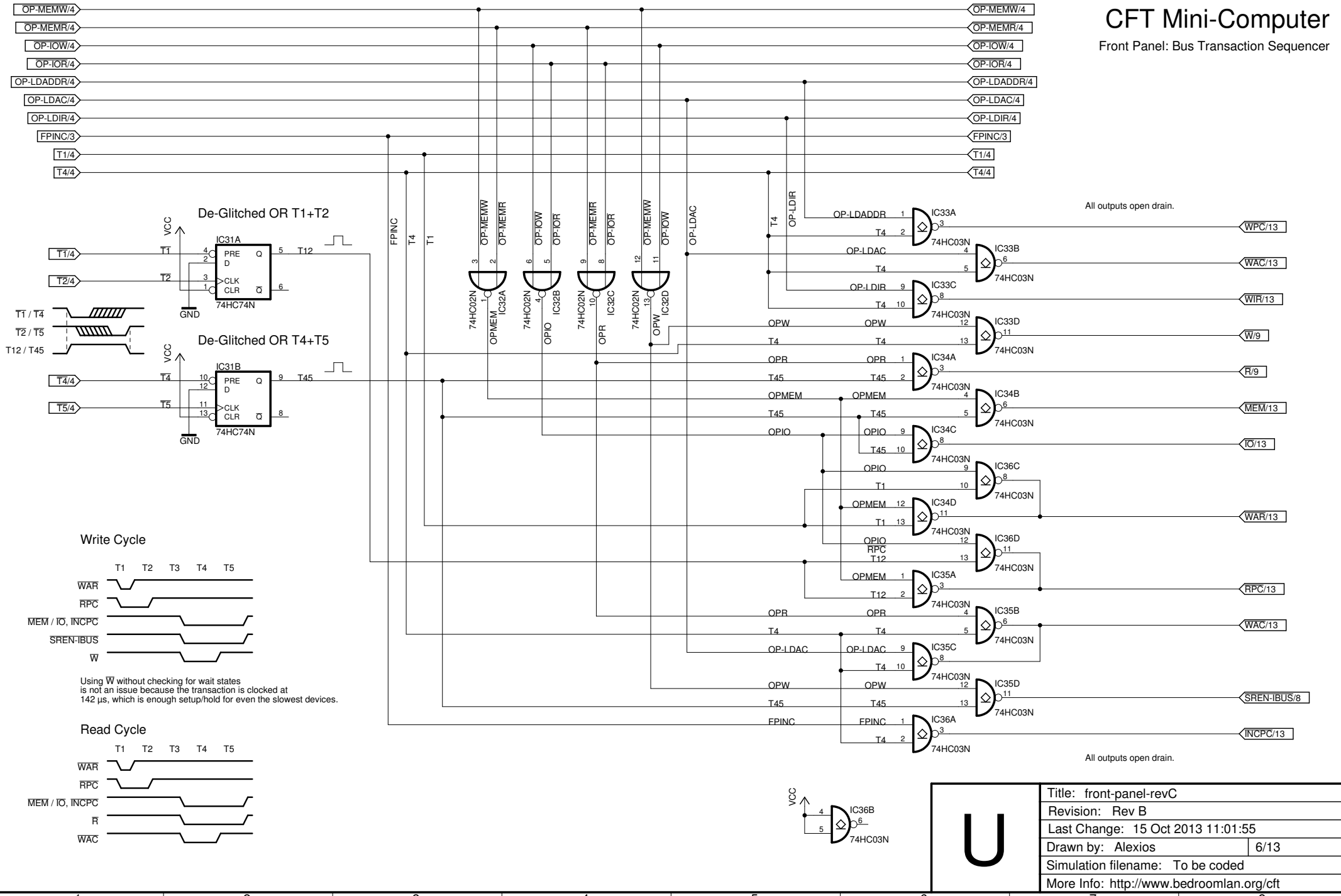
* Invoke missing gates.
* Check bypass capacitors.
* DRC

U

Title: front-panel-revC	
Revision: Rev B	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	5/13
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Bus Transaction Sequencer

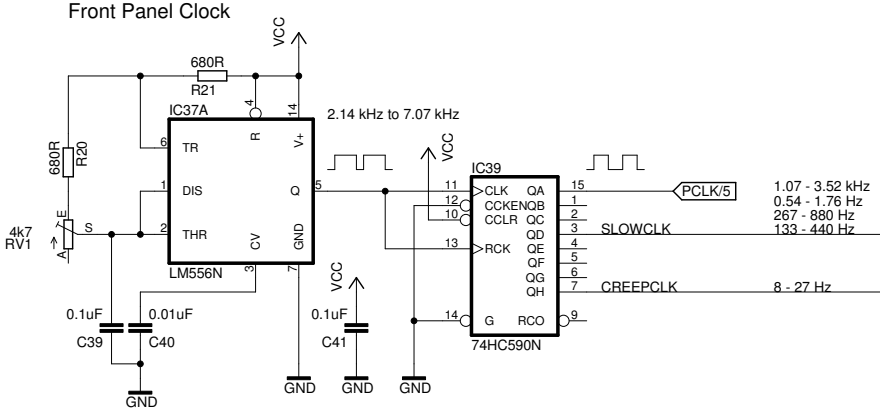


U	Title: front-panel-revC
	Revision: Rev B
	Last Change: 15 Oct 2013 11:01:55
	Drawn by: Alexios 6/13
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

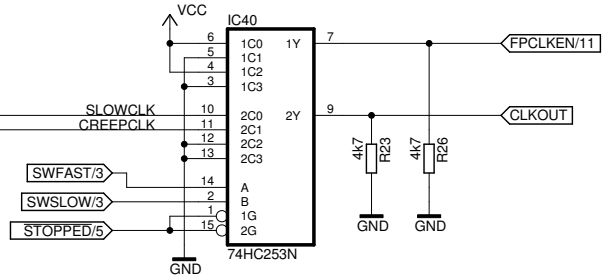
CFT Mini-Computer

Bus Connectors

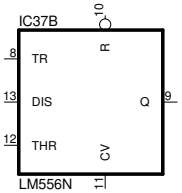
Front Panel Clock



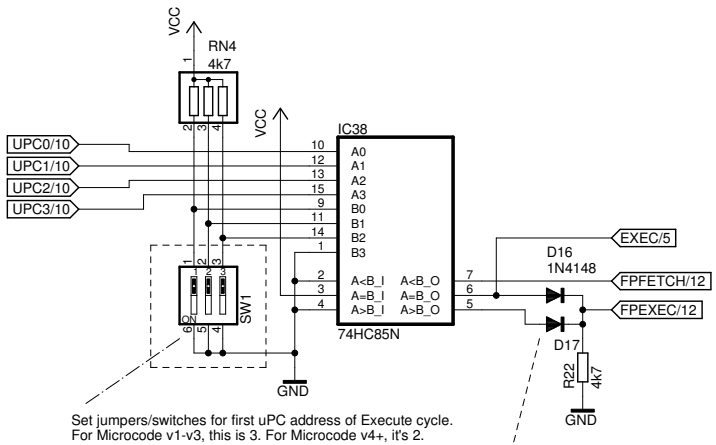
Clock Selector



Switch	Clock	SWFAST	SWSLOW	AB	FPCLKEN
Up	Full speed	H	L	10	1
Middle	~200 Hz	L	L	00	0
Down	~20 Hz	L	H	01	0



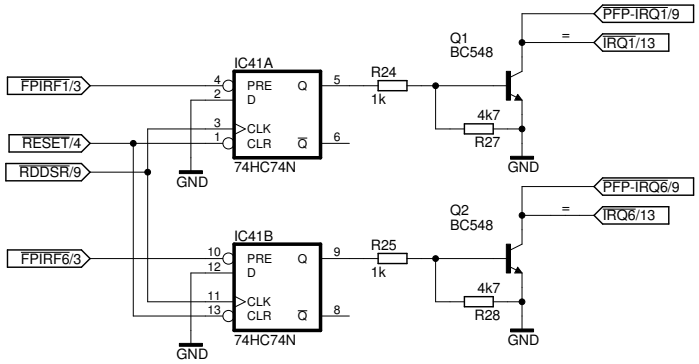
Fetch/Execute State Decoding



Set jumpers/switches for first uPC address of Execute cycle.
For Microcode v1-v3, this is 3. For Microcode v4+, it's 2.

Diode logic is acceptable here because it is merely driving a front panel LED (via an 74HCxxx buffer).

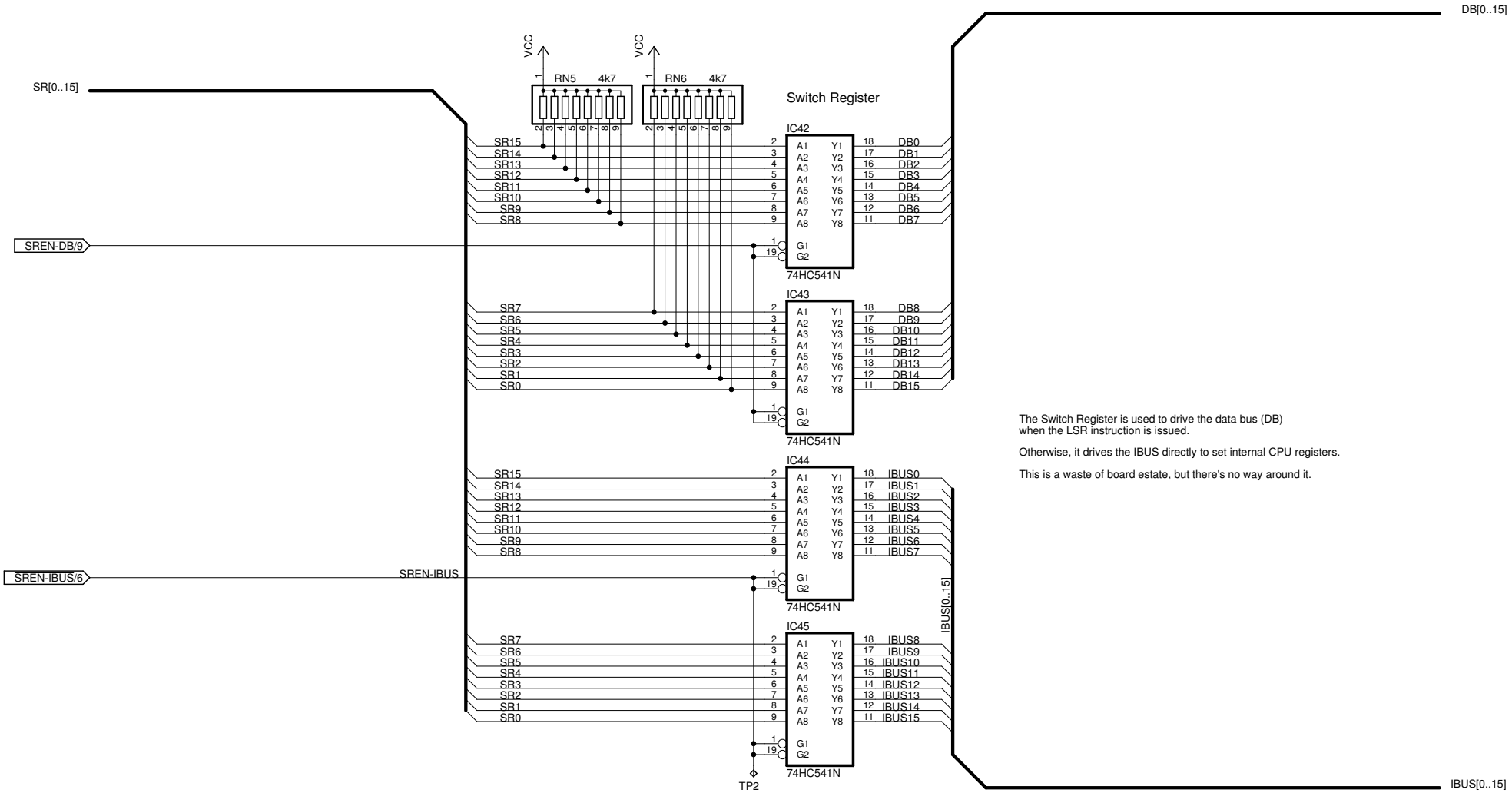
Interrupt Generation (IFR1/6 Switches)



U	Title: front-panel-revC
	Revision: Rev J
	Last Change: 15 Oct 2013 11:01:55
	Drawn by: Alexios 7/13
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Front Panel: Switch Register



The Switch Register is used to drive the data bus (DB) when the LSR instruction is issued.

Otherwise, it drives the IBUS directly to set internal CPU registers.

This is a waste of board estate, but there's no way around it.

TODO:

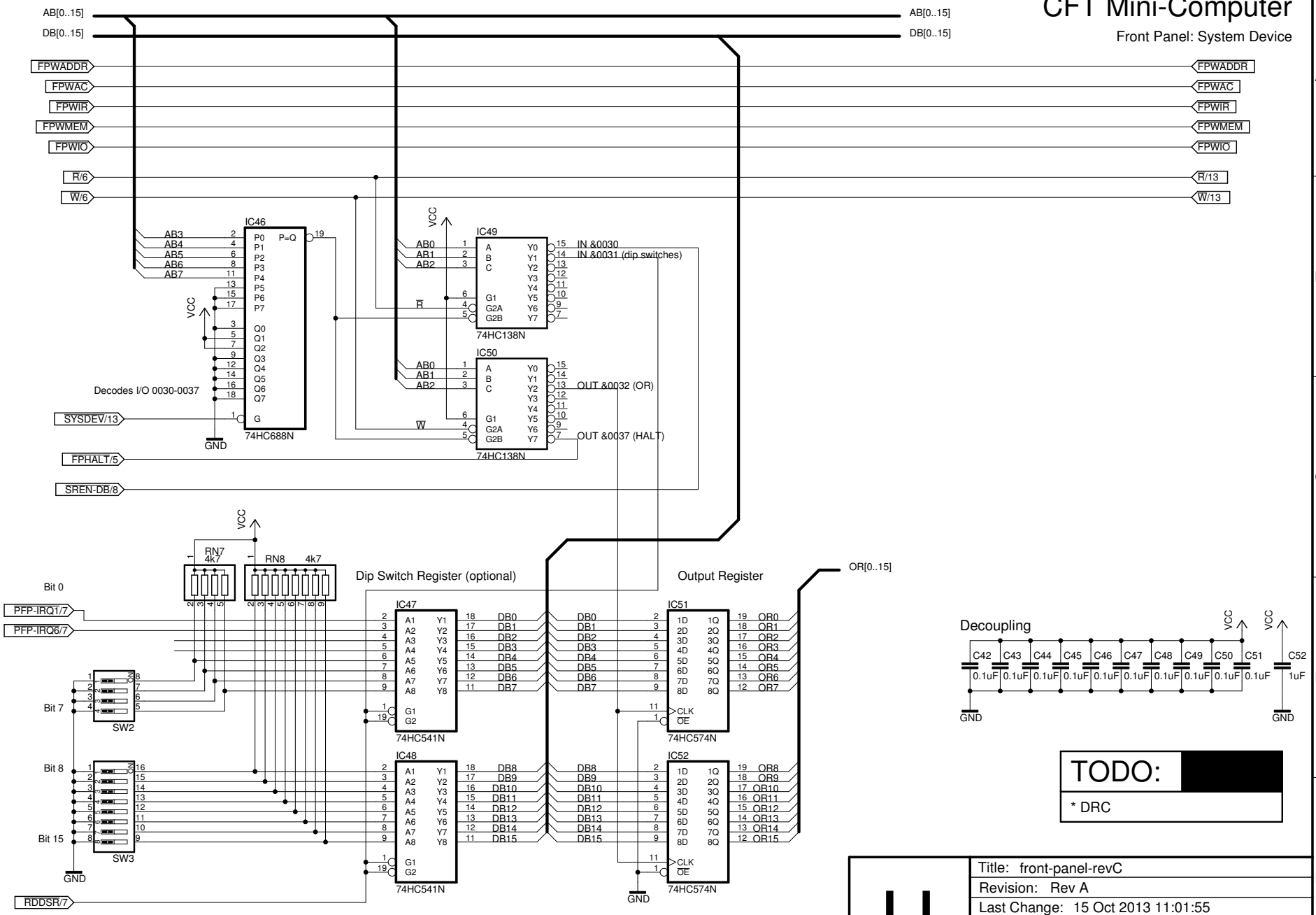
* DRC

U

Title: front-panel-revC	
Revision: Rev A	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	8/13
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: System Device



Decoupling

TODO:

* DRC

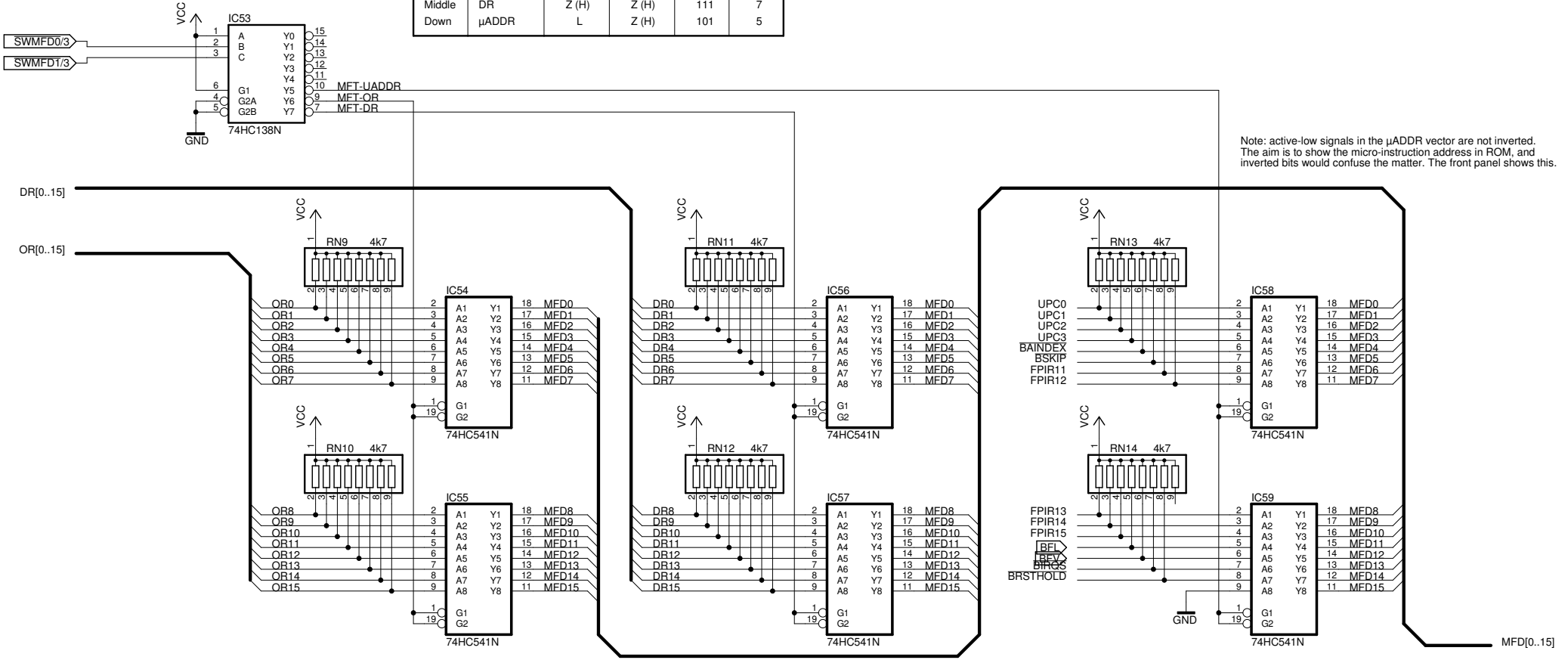
Title: front-panel-revC	
Revision: Rev A	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	9/13
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

U

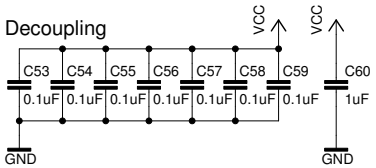
CFT Mini-Computer

Front Panel: Multi-Function Display

Switch	MFD Shows	$\overline{SWMFD0}$	$\overline{SWMFD1}$	Vector	Output
Up	OR	Z (H)	L	110	6
Middle	DR	Z (H)	Z (H)	111	7
Down	µADDR	L	Z (H)	101	5



Note: active-low signals in the µADDR vector are not inverted. The aim is to show the micro-instruction address in ROM, and inverted bits would confuse the matter. The front panel shows this.



TODO:

* DRC

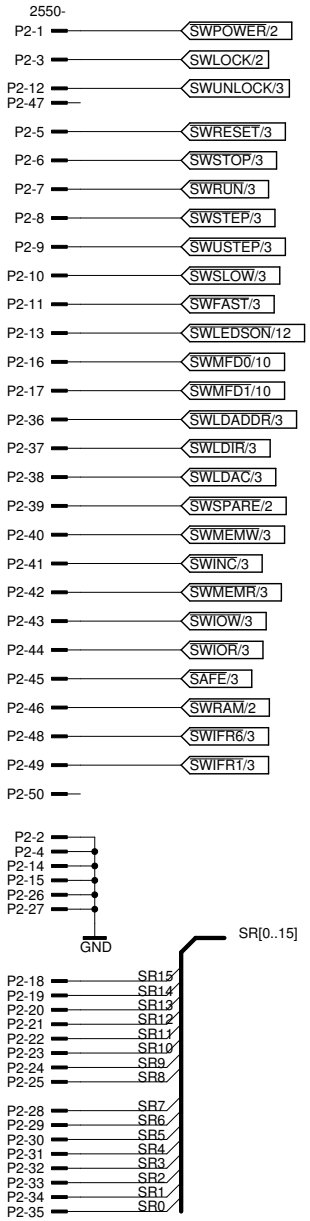
U

Title: front-panel-revC	
Revision: Rev C	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	10/13
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

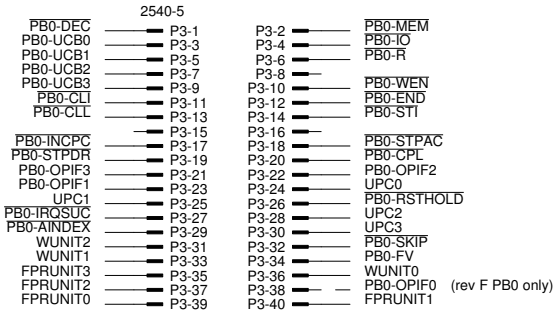
CFT Mini-Computer

Connectors

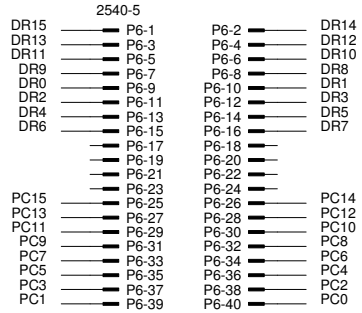
Switch Assembly



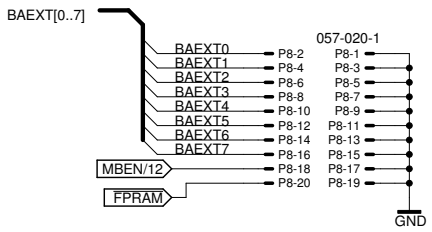
Processor Board 0



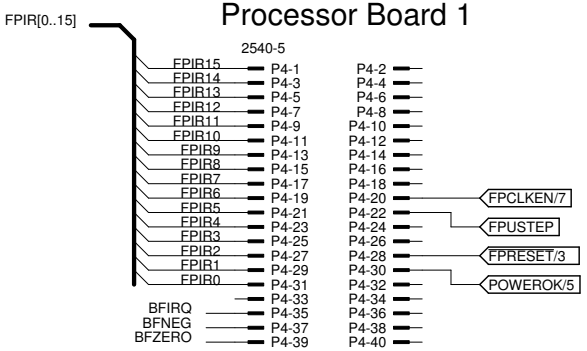
Processor Board 2



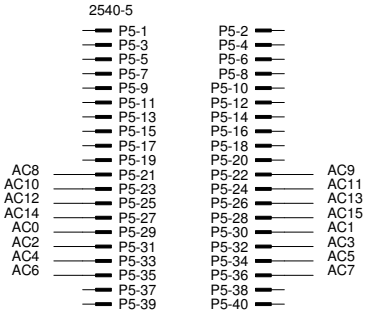
Processor Board 3 (MBU)



Processor Board 1



Processor Board 2



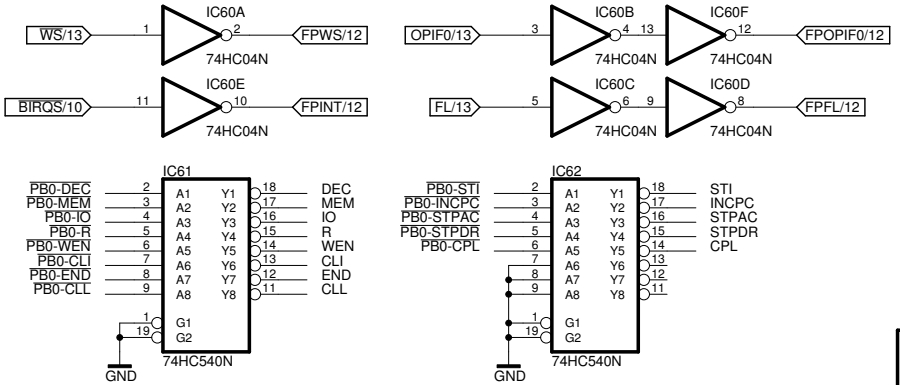
Signal Renaming

PB0-UCB0	=	UCB0
PB0-UCB1	=	UBC1
PB0-UCB2	=	UCB2
PB0-UCB3	=	UCB3
PB0-OPIF3	=	OPIF3
PB0-OPIF2	=	OPIF2
PB0-OPIF1	=	OPIF1
PB0-WUNIT2	=	WUNIT2
PB0-WUNIT1	=	WUNIT1
PB0-WUNIT0	=	WUNIT0
PB0-RUNIT3	=	RUNIT3
PB0-RUNIT2	=	RUNIT2
PB0-RUNIT1	=	RUNIT1
PB0-RUNIT0	=	RUNIT0

Microcode Address signals are NOT inverted.

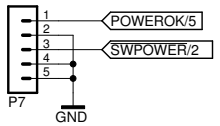
PB0-IRQSUC	=	BIRQS
PB0-SKIP	=	BSKIP
PB0-RSTHOLD	=	BRSTHOLD
PB0-AINDEX	=	BAINDEX

Signal Inversion



Power Supply

From power supply loom

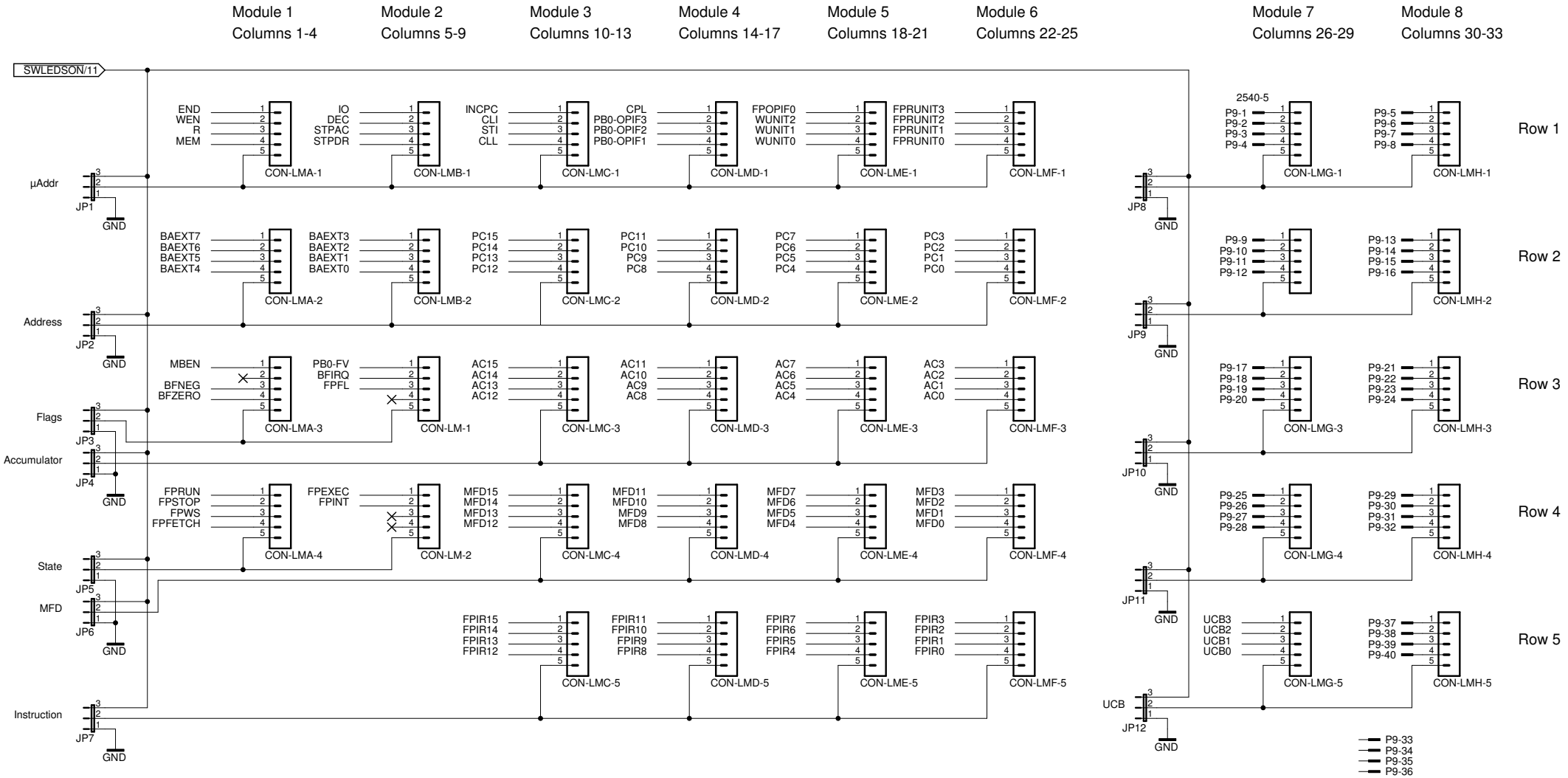


T

Title: front-panel-revC	
Revision: Rev C	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	11/13
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel Light Connections

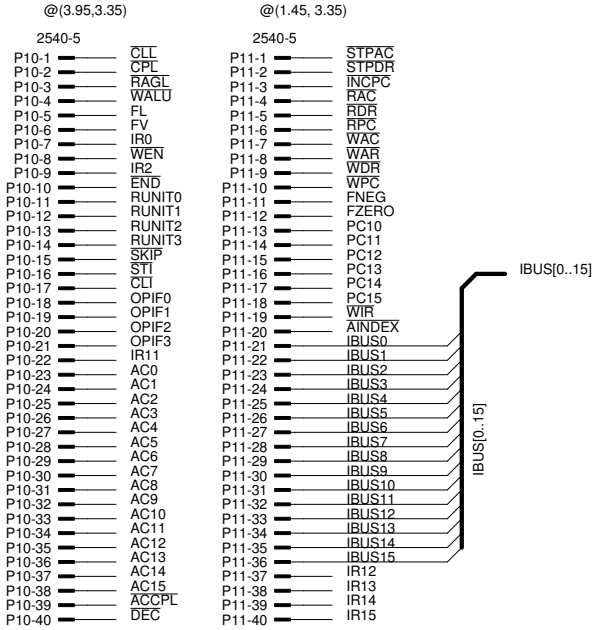


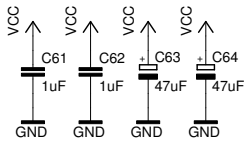
U	Title: front-panel-revC
	Revision: Rev A
	Last Change: 15 Oct 2013 11:01:55
	Drawn by: Alexios 12/13
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

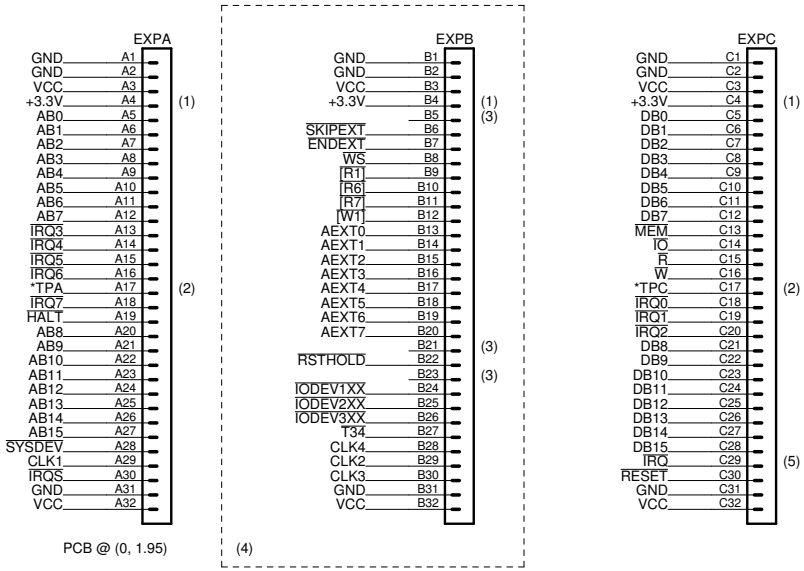
Bus Connectors

Control Bus (processor bus)





Expansion Bus (computer bus)



Notes

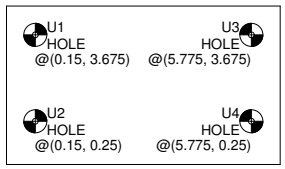
(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it. It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) $\overline{\text{IRQ}}$ is provided for systems which lack an interrupt controller ($\overline{\text{IRQ0-7}}$)



[PCB Logo]

[QR Code http://www.bedroomlan.org/cft (shortened)]

open hardware

J

Title: front-panel-revC	
Revision: Rev J	
Last Change: 15 Oct 2013 11:01:55	
Drawn by: Alexios	13/13
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	