CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Circuits in need of improvement are marked like this.

Circuits known to be incorrect are marked like this.

D	Title: cft
	Revision: Rev B
	Last Change: 4 Mar 2012 16:42:11
	Drawn by: Alexios 1/38
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Clock generation & control, Reset, Power & indicators

Run Indicator (optional)

330R R5 LED1 LED-5MM-GREEN GND

VCC R1 4k7

The '253 implements a function of CLKEN and FPUSTEP
to allow either clocked operation of manual stepping.

f(CLKEN,FPUSTEP): (CLK/2, $\overline{CLK/2}$)

f(0,0) = (0, 1)
f(0,1) = (1, 0)
f(1,X) = (CLKIN/2, $\overline{CLKIN/2}$)

NB: CLK/2, $\overline{CLK/2}$ and CLK/4, $\overline{CLK/4}$ are critical paths.

FPCLKEN/28 → FPCLKEN/28
RESET/4 → RESET/4
FPUSTEP/28 → FPUSTEP/28

R2 4k7 GND

Clock Control (run/stop/step)

IC2A 74HC112N: PRE J Q CLK K $\overline{Q}$ CLR
CLKIN/2, $\overline{CLKIN/2}$

IC5 74HC253N: 1C0 1C1 1C2 1C3 2C0 2C1 2C2 2C3 A B 1G 2G → 1Y 2Y
CLK/2, $\overline{CLK/2}$

Divide by 2, generate 4 phases

IC6A, IC6B 74HC112N

Raw clock is divided by 4 using 2 FF stages

TP3 CLK3/38
TP4 CLK1/4
TP5 CLK4/38
TP6 CLK2/38
TP7 CLK5/7

Raw clock Selector MUX

SLOWCLK/3
TESTCLK/3

IC1 74HC253N → RAWCLK

Divide by 2, generate 2 phases

R3 4k7 FPFAST/28
R4 4k7 FPSLOW/28

$\overline{GUARD}$ phase difference selector

74HC00: 7ns delay per gate, 14ns delay per jumper setting

IC4C 74HC00N

IC3A, IC7D, IC7C, IC7B, IC7A, IC4B, IC4A, IC3D, IC3C, IC3B 74HC00N

TP8

JP1: Install exactly ONE jumper.

GUARD/7

GUARD avoids IBUS contention between processor units of different speed
by inhibiting unit decoding immediately before/after CLK rising edges.
The delay mechanism will have to be readjusted if the clock speed changes.

Currently, the middle jumper seems right for a 16 MHz raw clock.

Clock Source Selector

Fast: FPFAST=1, FPSLOW=0 (#1)
Slow 1: FPFAST=0, FPSLOW=0 (#0)
Slow 2: FPFAST=0, FPSLOW=1 (#2)
With no front panel, pull-up/down always selects FASTCLK.

Full-Speed (Fast) Clock Oscillator

XTAL1 16.000MHz, C11 0.1uF → FASTCLK

Oscillator is 4x system clock speed.
16 MHz is a hopeful maximum. Testing required.
Oscillator frequency could drop to 4 MHz if
the system is unstable.

Decoupling

C1–C9 0.1uF, C10 1uF

IC2B 74HC112N, IC4D 74HC00N

TODO:

* Write & Verify Verilog Model
* DRC

U

Title: cft	
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More Info: http://www.bedroomlan.org/cft	

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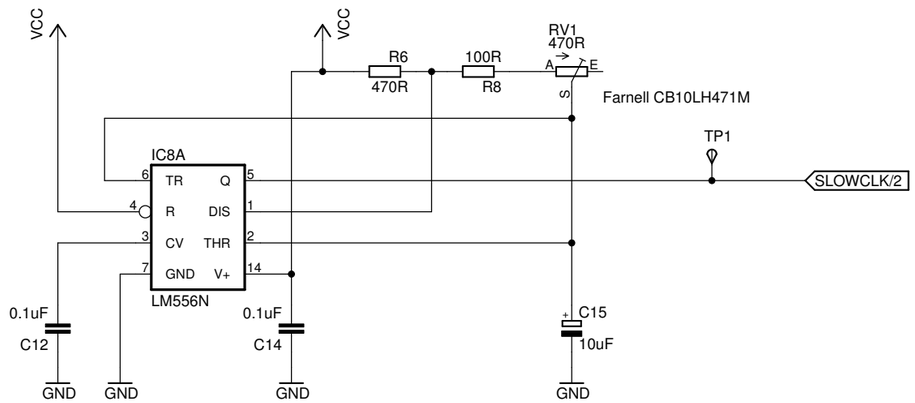
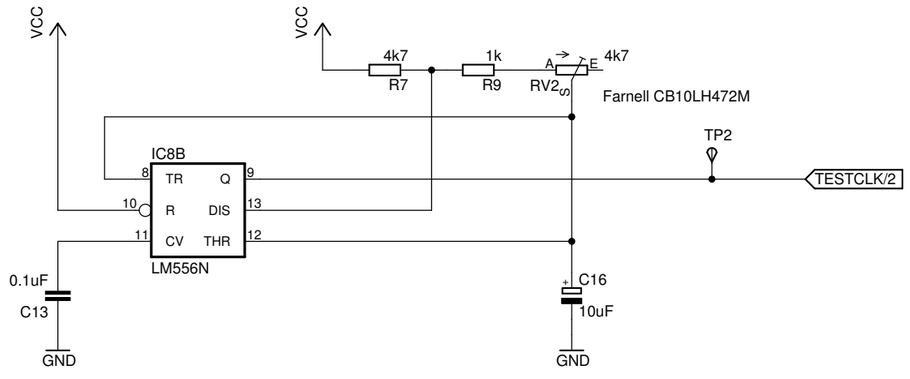
Slow Clock Generator

Slow and Test Clock Generators





TODO:

* DRC

U

Title: cft	
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Drawn by: Alexios	3/38
Simulation filename: clock.v#slow_clock_generator	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Reset Handling and Sequencing

On $\overline{\text{RESET}}$, the reset timer drives $\overline{\text{RSTHOLD}}$ down for 255 CLK pulses.
Using a 16 MHz oscillator, this will assert $\overline{\text{RSTHOLD}}$ for 31.875 us.
Using the slow clock (~400 Hz raw), this will pulse for 1.275 seconds.
Finally, with the testing clock (~40 Hz raw), $\overline{\text{RSTHOLD}}$ will last 12.75 seconds.
NB: CLKIN/2 is RAWCLK divided by 2 (obviously).

RESET/2
CLK1/2
RESET/5
RSTHOLD/5
IBUS[0..15]

VCC
R16 4k7

Reset Sources

VCC
R12 4k7
VCC
R14 4k7

FPRESET/29
POWEROK/34

74HC14N
IC9C
IC9B
74HC14N

IC10A
74HC05N
IC10C
74HC05N
IC10D
74HC05N

NB: Open Collector gate

LED-5MM-GREEN
LED2
330R
R11
Power LED
GND

RESET

NB: Open Drain gates

POWEROK comes from the ATX PSU via the front panel.
The PSU holds POWEROK low at power-up (or during brown-outs), until power stabilises. The computer is expected to reset when POWEROK is low.

Reset Button (optional)

JP2
S1
VCC
R10 50k
C23 0.1uF
IC9A
74HC14N
VCC
R13 4k7

If the reset button and debouncing circuit is installed, this resistor may be left out.

GND

CLK1
RESET

Reset timer

VCC
R15 4k7
RSTHOLD

IC13
CLK QA
CCKEN QB
CCLR QC
QD
RCK QE
QF
QG
QH
G RCO
74HC590N

JP16
2ms
4ms
8ms
16ms
32ms

GND

Install exactly ONE jumper.

Reset delay selector. Times shown for 4 MHz processor clock.

System Reset Vector (FFF0)

VCC
GND

IC11
IC12
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
74HC541N

IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15

RSTHOLD

IBUS[0..15]

Outputs binary 1111'1111'1111'0000 to the IBUS while $\overline{\text{RSTHOLD}}$ is asserted.
This value is picked up by other units of the processor, including the Program Counter, and becomes the computer's boot address.

Decoupling

VCC
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
VCC
C22 1uF
GND
GND

IC10E
IC10F
74HC05N
74HC05N
IC10B
74HC05N
IC9D
74HC14N
IC9E
74HC14N
IC9F
74HC14N
GND
GND

NB: Open Drain gate

TODO:

* Write & Verify Verilog Model
* DRC

U

Title: cft	
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Simulation filename: reset.v	
More Info: http://www.bedroomlan.org/cft	

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Microcode Sequencer

Notes

32k x 8 (2x256) ICs required for Microcode v4.
512k x 8 ICs are cheaper and easier to come by, though,
so this schematic uses these. Smaller ICs can be substituted.

ROMS to be socketed for easy reprogramming.

Use 70ns or 50ns chips.

Vertical microcode (unit selectors RUNIT, WUNIT and OPIF) are pulled low because a value of zero selects no unit.

$\overline{WS}$: indicates a wait state. Inhibits the uPC counter.
$\overline{HALT}$: halts the processor. The control unit's outputs are at High-Z. Consequently, the processor is disconnected from all busses. Control signals are active low and pulled up, so other units (like the front panel) may operate them with the processor halted.

$\overline{RESET}$: while $\overline{RESET}$ is active (low), the microcode ROMs are deselected and their outputs tri-stated to avoid bus contention with units resetting uncleanly.

Nota Bene: this sequencer can only run Microcode v.4!

AINDEX/6 → AINDEX
SKIP/6 → SKIP
FL/6 → FL
FV/6 → FV
IRQS/6 → IRQS
RSTHOLD/4 → RSTHOLD
END

Microcode PC

VCC, 4k7 R17, 4k7 R18
IC15 74HC161: P1–P4 / Q1–Q4 → UPC0, UPC1, UPC2, UPC3; CO → 15
CLK1/4 → CLK1
END → LD
WS → PE
HALT → TE
RSTHOLD → CL
GND

Microcode ROMs

END → $\overline{END}$

IC16 29F010:
UPC0–UPC3, AINDEX, SKIP, IR11–IR15, FL, FV, IRQS, RSTHOLD → A0–A16
D0–D7 → RUNIT0, RUNIT1, RUNIT2, RUNIT3, WUNIT0, WUNIT1, WUNIT2, OPIF0
4k7 RN1, VCC, C30 1uF, GND
$\overline{CE}$, $\overline{OE}$, $\overline{WE}$ → GND

IC17 29F010:
UPC0–UPC3, AINDEX, SKIP, IR11–IR15, FL, FV, IRQS, RSTHOLD → A0–A16
D0–D7 → OPIF1, OPIF2, OPIF3, $\overline{INCAC}$, $\overline{CPL}$, $\overline{CLL}$, $\overline{STI}$, $\overline{CLI}$
VCC, RN3 4k7, 4k7 RN2, C31 1uF, GND
$\overline{CE}$, $\overline{OE}$, $\overline{WE}$ → GND

IC18 29F010:
UPC0–UPC3, AINDEX, SKIP, IR11–IR15, FL, FV, IRQS, RSTHOLD → A0–A16
D0–D7 → $\overline{INCPC}$, $\overline{INCDR}$, UINSTR18, $\overline{MEM}$, $\overline{IO}$, $\overline{R}$, $\overline{WEN}$, $\overline{END}$
VCC, RN4 4k7, C32 1uF, GND
$\overline{CE}$, $\overline{OE}$, $\overline{WE}$ → GND

Note: $\overline{W}$ is $\overline{WEN}$ · CLK5.

IR11/6, IR12/6, IR13/6, IR14/6, IR15/6

HALT/36, RESET/4 → IC14A 74HC08N → VCC, GND

ROM image: microcode-00
ROM image: microcode-01
ROM image: microcode-02

RUNIT0/6, RUNIT1/6, RUNIT2/6, RUNIT3/6
WUNIT0/6, WUNIT1/6, WUNIT2/6
OPIF0/6, OPIF1/6, OPIF2/6, OPIF3/6
CPL/6, CLL/6, STI/6, CLI/6
INCAC/6, INCPC/6, INCDR/6
UINSTR18/6
MEM/6, IO/6, R/6, WEN/6, END/6

$\overline{UCE}$ is used by the unit decoders to ensure no units are selected when either $\overline{HALT}$ or $\overline{RESET}$ are inactive.

$\overline{UCE}$/7

Decoupling

VCC, C24 0.1uF, C25 0.1uF, C26 0.1uF, C27 0.1uF, C28 0.1uF, IC15P (VDD 16, VSS 8), GND
VCC, C29 1uF, GND

74HC08N: IC14B, IC14C, IC14D, GND

TODO:

* Write & Verify Verilog Model
* DRC

U

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Microcode Sequencer Front Panel Connections

UPC0/5
UPC1/5
UPC2/5
UPC3/5
AINDEX/5
SKIP/5
IR11/5
IR12/5
IR13/5
IR14/5
IR15/5
FL/5
FV/5
IRQS/5
RSTHOLD/5

IR[0..15] is sent to the Front Panel separately.

RUNIT0/5
RUNIT1/5
RUNIT2/5
RUNIT3/5
WUNIT0/5
WUNIT1/5
WUNIT2/5
OPIF0/5
OPIF1/5
OPIF2/5
OPIF3/5
CPL/5
CLL/5
STI/5
CLI/5
INCAC/5
INCPC/5
INCDR/5
UINSTR18/5
MEM/5
IO/5
R/5
WEN/5
END/5
FZERO/8
FNEG/8

IC19 — 74HC541N

UPC0	2	18	BUPC0
UPC1	3	17	BUPC1
UPC2	4	16	BUPC2
UPC3	5	15	BUPC3
AINDEX	6	14	BAINDEX
SKIP	7	13	BSKIP
FL	8	12	BFL
FV	9	11	BFV

IC20 — 74HC541N

IRQS	2	18	BIRQS
RSTHOLD	3	17	BRSTHOLD
RUNIT0	4	16	BRUNIT0
RUNIT1	5	15	BRUNIT1
RUNIT2	6	14	BRUNIT2
RUNIT3	7	13	BRUNIT3
WUNIT0	8	12	BWUNIT0
WUNIT1	9	11	BWUNIT1

IC21 — 74HC541N

FZERO	2	18	BFZERO
FNEG	3	17	BFNEG
	4	16	
WUNIT2	5	15	BWUNIT2
OPIF0	6	14	BOPIF0
OPIF1	7	13	BOPIF1
OPIF2	8	12	BOPIF2
OPIF3	9	11	BOPIF3

IC22 — 74HC540N

INCAC	2	18	BINCAC
CPL	3	17	BCPL
CLL	4	16	BCLL
STI	5	15	BSTI
CLI	6	14	BCLI
INCPC	7	13	BINCPC
INCDR	8	12	BINCDR
UINSTR18	9	11	BUINSTR18

IC23 — 74HC540N

MEM	2	18	BMEM
IO	3	17	BIO
R	4	16	BR
WEN	5	15	BW
END	6	14	BEND
	7	13	
	8	12	
	9	11	

JP3

BUPC0	1	2	BMEM
BUPC1	3	4	BIO
BUPC2	5	6	BR
BUPC3	7	8	BW
BAINDEX	9	10	BEND
BSKIP	11	12	BINCAC
BFL	13	14	BCPL
BFV	15	16	BCLL
BIRQS	17	18	BSTI
BRSTHOLD	19	20	BCLI
BRUNIT0	21	22	BINCPC
BRUNIT1	23	24	BINCDR
BRUNIT2	25	26	BUINSTR18
BRUNIT3	27	28	BOPIF0
BWUNIT0	29	30	BOPIF1
BWUNIT1	31	32	BOPIF2
BWUNIT2	33	34	BOPIF3
FZERO	35	36	FNEG
	37	38	
	39	40	

Note: $\overline{BW}$ is really the buffered version of $\overline{WEN}$, but the $\overline{WEN}$ strobe counter-intuitive.

TODO:

* DRC

U

Title: cft	
Revision: Rev F	
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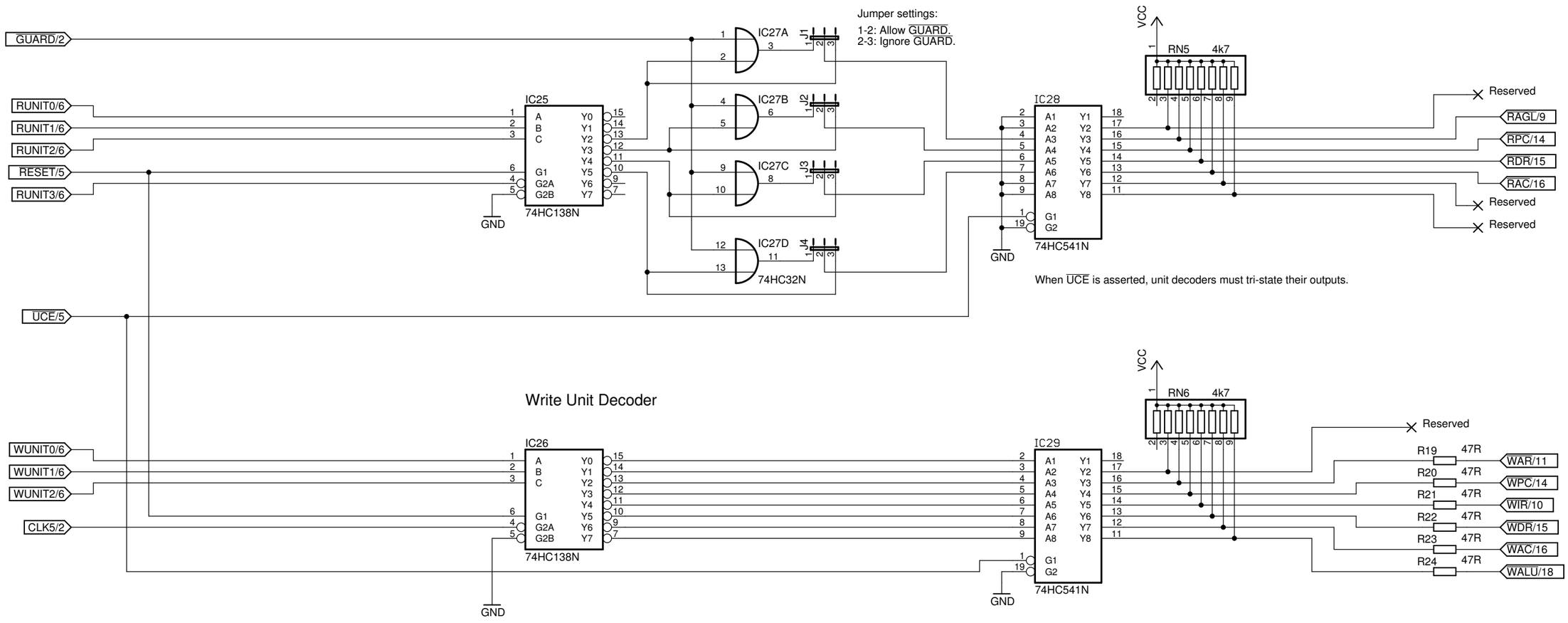
Drawn by: Alexios	6/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Read & Write Unit Decoding

Read Unit Decoder (partial)



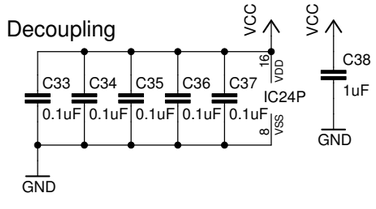
Write Unit Decoder

Write Unit Decoder:

000 = Idle
001 = Reserved
010 = Write AR (WAR)
011 = Write PC (WPC)
100 = Write IR (WIR)
101 = Write DR (WDR)
110 = Write AC & ALU Port A (WAC)
110 = Write ALU Port B (WALU)
111 = Reserved

RUNIT is decoded partially: only 0xxx values are decoded here.
ALU Operation decoding (RUNIT=1xxx) is done on the ALU board.

0000 = Idle
0001 = Reserved
0010 = Read from AGL (RAGL)
0011 = Read from PC (RPC)
0100 = Read from DR (RDR)
0101 = Read from AC (RAC)
0110 = Reserved
0111 = Reserved
1XXX = ALU operation or Constant



TODO:

* Write & Verify Verilog Model
* DRC

U

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Drawn by: Alexios	7/38
Simulation filename: unit_decoder.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Skip/Branch Logic

IR[0..15]

OPIF[0..3]

FNEG/6

FZERO/6

FL/6

FV/6

FNEG/16

FZERO/16

FL/17

FV/19

OP1 Branch Logic (IR0..IR4)

74HC08N: IC31B (SV), IC31A (SL), IC31D (SZ), IC31C (SN)

IC30A 74HC32N, IC30B 74HC32N, IC30C 74HC32N

IC33A 74HC32N, IC33B 74HC32N

OP1_BRANCH = (SV + SL + SZ + SN) XOR IR4

74HC86N IC32A

Worst case propagation delay: 3 x 8.5ns + 9.5ns = 35ns

OP1_BRANCH

OP2 Roll detection (IR0..IR3)

OP2_ROLL

Condition Multiplexing

IC35 74HC251N

IR3, IR4, IR5, IR6, IR7, IR8, IR9 → D0–D7

OPIF0, OPIF1, OPIF2, OPIF3 → A, B, C, G

SKIPMUXLO (Low = Skip)

0000-0111

IC36 74HC251N

FV, FL, FZERO, FNEG, OP2_ROLL, OP1_BRANCH → D0–D7

OPIF0, OPIF1, OPIF2 → A, B, C, G

SKIPMUXHI (Low = Skip)

1000-1111

IC34A 74HC00N: OPIF3 → $\overline{OPIF3}$

IC34B 74HC00N

IC34C 74HC00N

4k7 R26, 4k7 R25

SKIP0

This generates glitches, but the Skip Flag Register filters them out.

Skip flag register

IC37 74HC175D

SKIP0 → D1; D2, D3, D4 → GND; CLR → VCC; CLK → CLK1/5

Q1 → SKIP/6

RESET/7

Microcode v.4 OPIF field

OPIF = 0000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 0001: IF3 ($\overline{SKIP}$ = IR3)
OPIF = 0010: IF4 ($\overline{SKIP}$ = IR4)
OPIF = 0011: IF5 ($\overline{SKIP}$ = IR5)
OPIF = 0100: IF6 ($\overline{SKIP}$ = IR6)
OPIF = 0101: IF7 ($\overline{SKIP}$ = IR7)
OPIF = 0110: IF8 ($\overline{SKIP}$ = IR8)
OPIF = 0111: IF9 ($\overline{SKIP}$ = IR9)

OPIF = 1000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1001: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1010: IF$\overline{V}$ ($\overline{SKIP}$ = IFV, skip if V=0)
OPIF = 1011: IF$\overline{L}$ ($\overline{SKIP}$ = IFL, skip if L=0)
OPIF = 1100: IF$\overline{ZERO}$ ($\overline{SKIP}$ = IFZERO, skip if Z=0)
OPIF = 1101: IF$\overline{NEG}$ ($\overline{SKIP}$ = FNEG, skip if N=0)
OPIF = 1110: IFROLL ($\overline{SKIP}$ = IR0 + IR1 + IR2)
OPIF = 1111: IFBRANCH Logic

Decoupling

C39–C46: 0.1uF; C47: 1uF

IC33D 74HC32N, IC32B 74HC86N, IC32D 74HC86N, IC34D 74HC00N

TODO:

* DRC

U

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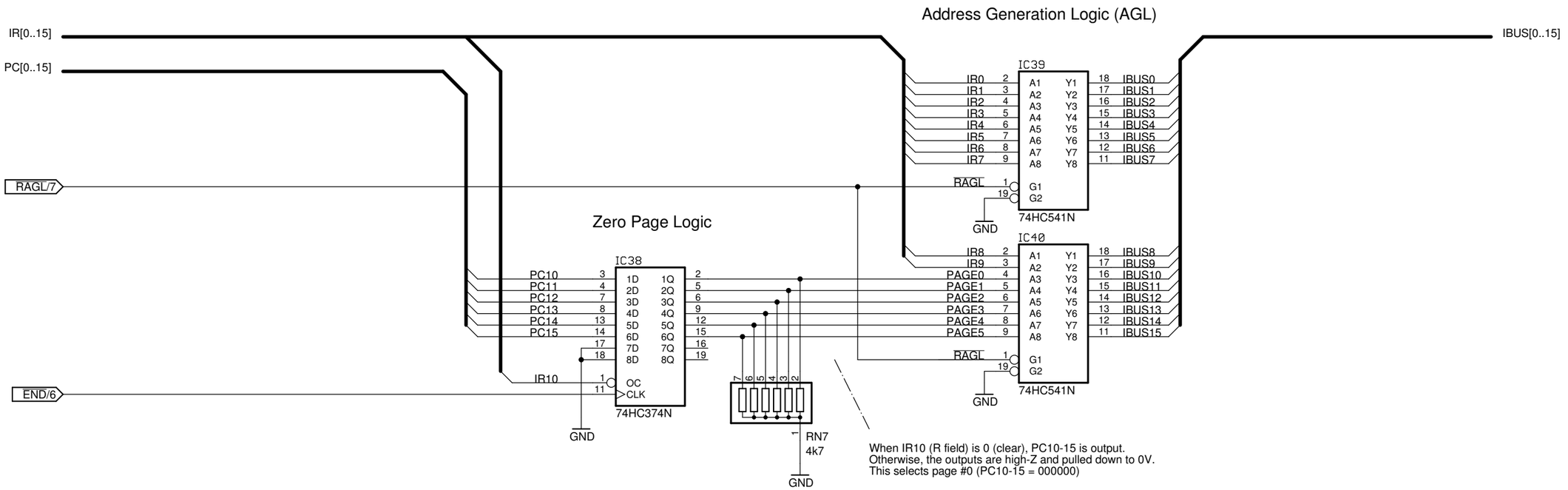
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Address Generation Logic



Notes

The value of the PC is clocked into the D-Flip Flop on the rising edge of $\overline{\text{END}}$.
At that point, the PC holds the value of the instruction about to be fetched.

If this registering doesn't take place, by the time the AGL is read, the PC will have been incremented (at the end of the fetch cycle), and pointing to the next instruction.

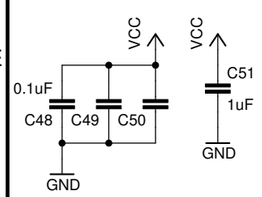
Thus, the AGL would generate addresses for PC+1. This works as the user expects for the first 1023 page offsets, and fails on the 1024th, where the AGL produces an address for the next page.

This would make programming with page-relative modes much less intuitive.

TODO:

* DRC

Decoupling



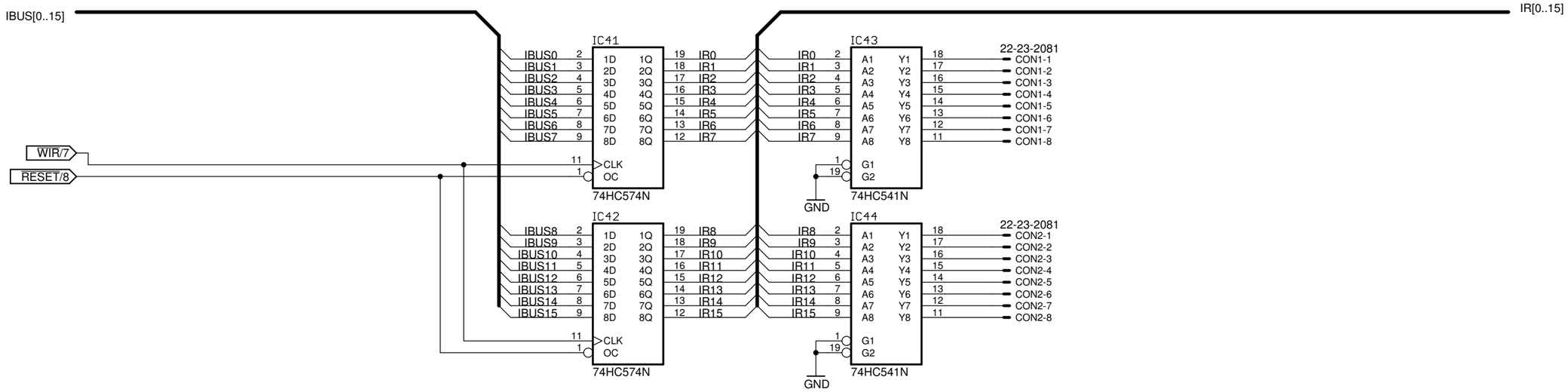
U	Title: cft
	Revision: Rev B
	Last Change: 4 Mar 2012 16:42:11
	Drawn by: Alexios — 9/38
	Simulation filename: agl.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

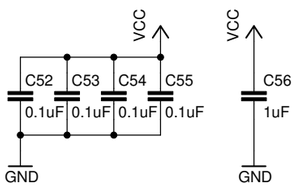
Instruction Register

Instruction Register (IR)

Front Panel Buffers & Connectors



Decoupling



TODO:

* DRC

U

Title: cft	
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Simulation filename: ir.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Address Register, Address Bus Drivers & Termination, Autoindex Logic, Device Decoder

MEM/6, IO/6 → IC45A (74HC08N) → ABEN

IBUS[0..15]

Address Register (AR)

IC46 (74HC273N): IBUS0..IBUS7 → AR0..AR7; WAR, RESET/10 → CLK, CLR

IC47 (74HC273N): IBUS8..IBUS15 → AR8..AR15; WAR, RESET/10 → CLK, CLR

Address Bus Drive Logic

IC48 (74HC541N): AR0..AR7 → AB0..AB7; ABEN → G1, G2; GND

IC49 (74HC541N): AR8..AR15 → AB8..AB15; ABEN → G1, G2; GND

Address Bus Hold

AB[0..15]

IC51 (74HC541N): AB0..AB7 → AB0..AB7; GND

IC52 (74HC541N): AB8..AB15 → AB8..AB15; GND

RN8A 10k: AB0, AB1
RN8B 10k: AB2, AB3
RN8C 10k: AB4, AB5
RN8D 10k: AB6, AB7
RN8E 10k: AB8, AB9
RN8F 10k: AB10, AB11
RN8G 10k: AB12, AB13
RN8H 10k: AB14, AB15
RN9A 10k
RN9B 10k
RN9C 10k
RN9D 10k
RN9E 10k
RN9F 10k
RN9G 10k
RN9H 10k

Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.

TODO:

* DRC

END/9 → END, IO

Autoindex Logic

IC50 (74HC688N): AR7..AR14 → P0..P7; P=Q → IC215A PRE; AR15 → G; VCC; GND

IC215A (74HC112N): PRE ← IC50 P=Q; J ← Q; CLK ← IO; K ← END; CLR ← END; Q̄ → AINDEX/23; GND

Notes (Autoindex Logic)

This evaluates the function:

$\overline{AINDEX} = \overline{AR} == 0000'0000'1XXX'XXXX$

It is necessary to register $\overline{AINDEX}$ because AR is changed during execution of an indirect mode instruction.

The flag is cleared at the end of the instruction, when $\overline{END}$ is asserted.

I/O Device Address Decoder

IC54 (74HC688N): AB11..AB15 → P0..P4; P=Q → IC55 G1; P5..P7 → GND; IO → G; GND

IC55 (74HC138N): AB8..AB10 → A, B, C; G1 ← IC54 P=Q; G2A, G2B → GND; VCC; Y0 → SYSDEV/21; Y1 → IODEV1XX; Y2 → IODEV2XX; Y3 → IODEV3XX; Y4..Y7 unused

Decodes I/O addresses 0n00-0nFF to simplify interfacing.

For n = 0, $\overline{SYSDEV}$ is asserted.
For n = 1, $\overline{IODEV1XX}$ is asserted.
For n = 2, $\overline{IODEV2XX}$ is asserted.
For n = 3, $\overline{IODEV3XX}$ is asserted.

Other devices must be decoded ad hoc.

Decoupling

C57–C65: 0.1uF; C66: 1uF; VCC; GND

IC45D, IC45B, IC45C (74HC08N); GND

IC215B (74HC112N): PRE, J, CLK, K, CLR, Q, Q̄; GND

U	
Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	11/38
Simulation filename: addressing.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Interrupt State Machine

RESET/11
STI/6
CLI/6
END/11

VCC
R27
4k7
IRQ/22

IRQ should be driven by open-drain gates.
It is pulled up here.

RESET
END

Interrupt Flag (Asynchronous)

STI
RESET 1
CLI 2
IC56A
3 RESET_OR_CLI
74HC08N

IC58A
PRE 4, J 3, CLK 1, K 2, CLR 15, Q 5, Q̄ 6
74HC112N
GND
FINT

Masking and State (Synchronous)

FINT 1
IRQ 2
IC57A
3
74HC32N

IC59B
PRE 10, J 11, CLK 13, K 12, CLR 14, Q 9, Q̄ 7
74HC112N
GND
MASKEDIRQ
RESET_OR_CLI

RESET/14
FINT
Note: for testing purposes.

Interrupts Enabled light (optional)

LED-5MM-GREEN
LED3
330R
R28
GND

Safe Interrupt Signalling

IRQ
Interrupt Microprogram Running
IRQS

Assert IRQ, wait for IRQS, deassert IRQ.

FIRQ
Note: for testing purposes.

Interrupt Request Register FF (Instruction-synchronous)

VCC
IC60A
PRE 4, J 3, CLK 1, K 2, CLR 15, Q 5, Q̄ 6
74HC112N
FIRQ
END
RESET
IRQS/20
This is also the interrupt acknowledge signal.

Interrupt Seen light (optional)

LED-5MM-GREEN
LED4
330R
R29
GND

Interrupt Flag Waveforms

RESET
STI
CLI
FINT

Masking and IRQ Waveforms

RESET
CLI
FINT
IRQ
FIRQ

Masking and IRQ Waveforms (Instruction-synchronous)

END
RESET
CLI
FIRQ
IRQS

Notes

The Interrupt flag denotes our disposition to handle incoming interrupts (allow or ignore).
At RESET time, interrupts are cleared and further interrupts are masked (ignored).
The falling edge of CLI or RESET clears the interrupt flag, ignoring interrupts.
The falling edge of STI sets the flag, allowing interrupts.

When the interrupt flag is set, the falling edge of IRQ triggers an interrupt (FIRQ high).

This is ignored until the end of the current instruction (falling edge of END).
At that point, the register FF clocks FIRQ in, asserting IRQS to the microcode sequencer.
The K input of the flip flop is held constantly high. With FIRQ high, this is a toggle action.

At the next instruction (falling edge of END), IRQS would toggle again.
Before this happens, the interrupt microprogram asserts CLI, clearing FIRQ, so no further toggling takes place. Instead, with K low and J high, IRQS is deasserted, resuming normal excecution.

TODO:

* DRC

Decoupling

VCC
C67 0.1uF, C68 0.1uF, C69 0.1uF, C70 0.1uF, C71 0.1uF, C72 1uF
GND

IC56B 4 5 6, IC56C 9 10 8 — 74HC08N
IC56D 12 13 11, IC57B 4 5 6 — 74HC08N
IC57C 9 10 8, IC57D 12 13 11 — 74HC32N
IC60B — 74HC112N

U	Title: cft
	Revision: Rev B
	Last Change: 4 Mar 2012 16:42:11
	Drawn by: Alexios — 12/38
	Simulation filename: int.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Data Bus Driver & Bus Termination

IBUS[0..15]

MEM/11

IO/11

R/6

CLK5/7

WEN/6

IC53A
74HC32N

74HC08N

IC61A

W

Data Bus Transceiver

IBUS[0..15]

IC62

IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7

R
BUSEN

DIR
G

74HC245N

IC63

IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15

R
BUSEN

DIR
G

74HC245N

DB[0..15]

DB[0..15]

Bus Hold

IC64

DB0 DB1 DB2 DB3 DB4 DB5 DB6 AB7

G1
G2

74HC541N

GND

IC65

DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

G1
G2

74HC541N

GND

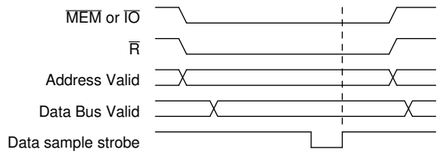
DB[0..15]

RN10A 10k — DB0, DB1
RN10B 10k — DB2, DB3
RN10C 10k — DB4, DB5
RN10D 10k — DB6, AB7
RN10E 10k — DB8, DB9
RN10F 10k — DB10, DB11
RN10G 10k — DB12, DB13
RN10H 10k — DB14, DB15

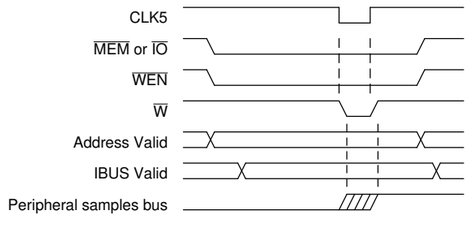
Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.

W/21

Memory or I/O Space Read Waveforms



Memory or I/O Space Write Waveforms



Decoupling

VCC

C73 C74 C75 C76 C77 — 0.1uF each

C78 — 1uF

GND

IC53D 74HC32N
IC61B 74HC08N
IC61C 74HC08N
IC53B 74HC32N
IC53C 74HC32N
IC61D 74HC08N

GND

TODO:

* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	13/38
Simulation filename: control_unit.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Major Registers: Program Counter (PC)

RPC/7
WPC/7
INCPC/6
RESET/12
IBUS[0..15]

NB: this is RESET inverted, fed to all 3 major registers' CLEAR signals ('193).

RESET/15
IBUS[0..15]

74HC04N IC66A

Register & Increment

IC67 74HC193N
IBUS0 IBUS1 IBUS2 IBUS3 → A B C D → QA QB QC QD → PC0 PC1 PC2 PC3
WPC → LOAD
INCPC → UP
RESET → CLEAR
BORROW, CARRY
GND

IC68 74HC193N
IBUS4 IBUS5 IBUS6 IBUS7 → A B C D → QA QB QC QD → PC4 PC5 PC6 PC7
WPC → LOAD
RESET → CLEAR
UP = BORROW, CARRY
GND

IC69 74HC193N
IBUS8 IBUS9 IBUS10 IBUS11 → A B C D → QA QB QC QD → PC8 PC9 PC10 PC11
WPC → LOAD
RESET → CLEAR
UP = BORROW, CARRY
GND

IC70 74HC193N
IBUS12 IBUS13 IBUS14 IBUS15 → A B C D → QA QB QC QD → PC12 PC13 PC14 PC15
WPC → LOAD
RESET → CLEAR
UP = BORROW, CARRY
GND

Tri-State Buffering

IC71 74HC541N
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 → A1 A2 A3 A4 A5 A6 A7 A8 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
G1, G2 → GND

IC72 74HC541N
PC8 PC9 PC10 PC11 PC12 PC13 PC14 PC15 → A1 A2 A3 A4 A5 A6 A7 A8 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15
G1, G2 → GND

PC[0..15]

Front Panel Buffers & Connectors

IC73 74HC541N
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 → A1 A2 A3 A4 A5 A6 A7 A8 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → 22-23-2081 CON3-1 CON3-2 CON3-3 CON3-4 CON3-5 CON3-6 CON3-7 CON3-8
G1, G2 → GND

IC74 74HC541N
PC8 PC9 PC10 PC11 PC12 PC13 PC14 PC15 → A1 A2 A3 A4 A5 A6 A7 A8 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → 22-23-2081 CON4-1 CON4-2 CON4-3 CON4-4 CON4-5 CON4-6 CON4-7 CON4-8
G1, G2 → GND

Decoupling

VCC
C79 C80 C81 C82 C83 C84 C85 C86 0.1uF
C87 1uF
GND

74HC04N IC66C, IC66B, IC66E, IC66D, IC66F
GND

TODO:
* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	14/38
Simulation filename: register.v#reg_pc	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Major Registers: Data Register (DR)

RDR/7
WDR/7
INCDR/6
RESET/14
IBUS[0..15]

NB: this is $\overline{\text{RESET}}$ inverted.

RESET/16
IBUS[0..15]

Register & Increment

IC75 — 74HC193N
IBUS0 15, IBUS1 1, IBUS2 10, IBUS3 9 → A, B, C, D
QA 3 → DR0, QB 2 → DR1, QC 6 → DR2, QD 7 → DR3
$\overline{\text{WDR}}$ 11 → LOAD
$\overline{\text{INCDR}}$ 5 → UP
RESET 14 → CLEAR
DOWN 4 → GND
BORROW 13, CARRY 12

IC76 — 74HC193N
IBUS4 15, IBUS5 1, IBUS6 10, IBUS7 9 → A, B, C, D
QA 3 → DR4, QB 2 → DR5, QC 6 → DR6, QD 7 → DR7
$\overline{\text{WDR}}$ 11 → LOAD
5 → UP
RESET 14 → CLEAR
DOWN 4 → GND
BORROW 13, CARRY 12

IC77 — 74HC193N
IBUS8 15, IBUS9 1, IBUS10 10, IBUS11 9 → A, B, C, D
QA 3 → DR8, QB 2 → DR9, QC 6 → DR10, QD 7 → DR11
$\overline{\text{WDR}}$ 11 → LOAD
5 → UP
RESET 14 → CLEAR
4 → DOWN → GND
BORROW 13, CARRY 12

IC78 — 74HC193N
IBUS12 15, IBUS13 1, IBUS14 10, IBUS15 9 → A, B, C, D
QA 3 → DR12, QB 2 → DR13, QC 6 → DR14, QD 7 → DR15
$\overline{\text{WDR}}$ 11 → LOAD
5 → UP
RESET 14 → CLEAR
4 → DOWN → GND
BORROW 13, CARRY 12

Tri-State Buffering

IC79 — 74HC541N
DR0 2, DR1 3, DR2 4, DR3 5, DR4 6, DR5 7, DR6 8, DR7 9 → A1, A2, A3, A4, A5, A6, A7, A8
Y1 18 → IBUS0, Y2 17 → IBUS1, Y3 16 → IBUS2, Y4 15 → IBUS3, Y5 14 → IBUS4, Y6 13 → IBUS5, Y7 12 → IBUS6, Y8 11 → IBUS7
1, 19 → G1, G2

IC80 — 74HC541N
DR8 2, DR9 3, DR10 4, DR11 5, DR12 6, DR13 7, DR14 8, DR15 9 → A1, A2, A3, A4, A5, A6, A7, A8
Y1 18 → IBUS8, Y2 17 → IBUS9, Y3 16 → IBUS10, Y4 15 → IBUS11, Y5 14 → IBUS12, Y6 13 → IBUS13, Y7 12 → IBUS14, Y8 11 → IBUS15
1, 19 → G1, G2

Front Panel Buffers & Connectors

IC81 — 74HC541N
DR0 2, DR1 3, DR2 4, DR3 5, DR4 6, DR5 7, DR6 8, DR7 9 → A1, A2, A3, A4, A5, A6, A7, A8
Y1 18 → CON5-1, Y2 17 → CON5-2, Y3 16 → CON5-3, Y4 15 → CON5-4, Y5 14 → CON5-5, Y6 13 → CON5-6, Y7 12 → CON5-7, Y8 11 → CON5-8
22-23-2081
1, 19 → G1, G2
GND

IC82 — 74HC541N
DR8 2, DR9 3, DR10 4, DR11 5, DR12 6, DR13 7, DR14 8, DR15 9 → A1, A2, A3, A4, A5, A6, A7, A8
Y1 18 → CON6-1, Y2 17 → CON6-2, Y3 16 → CON6-3, Y4 15 → CON6-4, Y5 14 → CON6-5, Y6 13 → CON6-6, Y7 12 → CON6-7, Y8 11 → CON6-8
22-23-2081
1, 19 → G1, G2
GND

DR[0..15]

Decoupling

VCC
C88 0.1uF, C89 0.1uF, C90 0.1uF, C91 0.1uF, C92 0.1uF, C93 0.1uF, C94 0.1uF, C95 0.1uF
VCC
C96 1uF
GND

TODO:

* DRC

U

Title: cft	
Revision: Rev C	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	15/38
Simulation filename: register.v#reg_dr	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Accumulator (AC), Zero Flag & Negative Flag

RAC/7
WAC/7
INCAC/6
RESET/15
IBUS[0..15]

IBUS[0..15]

Register & Increment

IC83 74HC193N
IC84 74HC193N
IC85 74HC193N
IC86 74HC193N

IBUS0 IBUS1 IBUS2 IBUS3 → AC0 AC1 AC2 AC3
IBUS4 IBUS5 IBUS6 IBUS7 → AC4 AC5 AC6 AC7
IBUS8 IBUS9 IBUS10 IBUS11 → AC8 AC9 AC10 AC11
IBUS12 IBUS13 IBUS14 IBUS15 → AC12 AC13 AC14 AC15

WAC
INCAC
RESET
LOAD
UP
DOWN
CLEAR
BORROW
CARRY
GND

Tri-State Buffering

IC87 74HC541N
IC88 74HC541N

AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7 → IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
AC8 AC9 AC10 AC11 AC12 AC13 AC14 AC15 → IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15

A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2

Zero Flag

IC90 74HC688N
IC89 74HC688N

AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7
AC8 AC9 AC10 AC11 AC12 AC13 AC14 AC15
P0 P1 P2 P3 P4 P5 P6 P7
P=Q
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
G
GND

Front Panel Buffers & Connectors

IC91 74HC541N
IC92 74HC541N

AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7 → CON7-1 CON7-2 CON7-3 CON7-4 CON7-5 CON7-6 CON7-7 CON7-8
AC8 AC9 AC10 AC11 AC12 AC13 AC14 AC15 → CON8-1 CON8-2 CON8-3 CON8-4 CON8-5 CON8-6 CON8-7 CON8-8

22-23-2081

AC15 = FNEG → FNEG/23

IC216A 74HC04N
FZERO/23

INCCPL
Asynchronous toggle of L

AC[0..15]

Decoupling

VCC
C97 C98 C99 C100 C101 C102 C103 C104 C105 C106 0.1uF
C107 1uF
GND

IC216B IC216C IC216D IC216E IC216F 74HC04N

TODO:

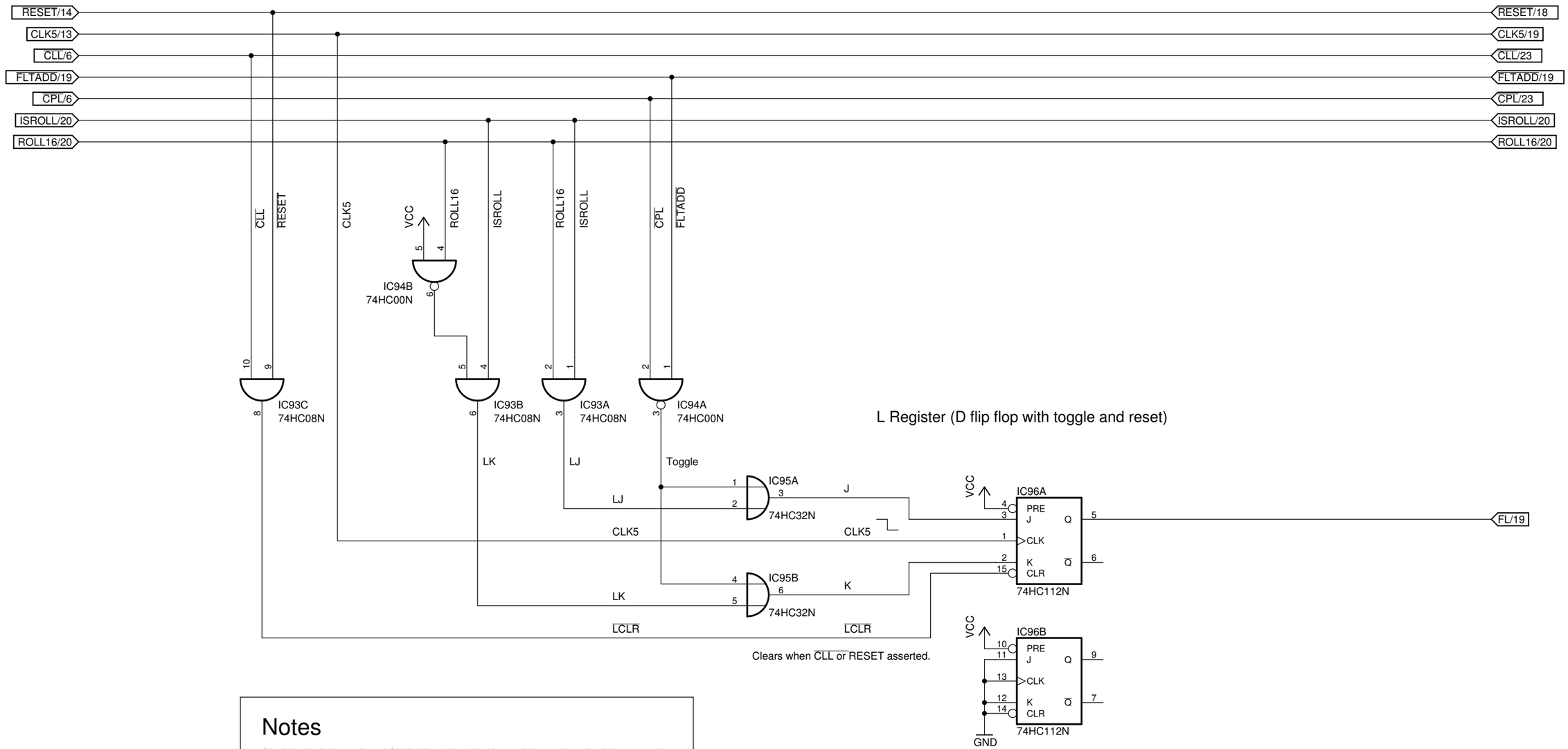
* DRC

U

Title: cft	
Revision: Rev C	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	16/38
Simulation filename: register.v#reg_ac	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

The L Register



Notes

Clock is the falling edge of CLK5 (the 'write' clock), so all inputs have had time to settle.

Since FLTADD is registered on the rising edge of CLK5, this implies that ADD carry out will toggle L one clock period after the addition itself.

Clear sources (asynchronous):

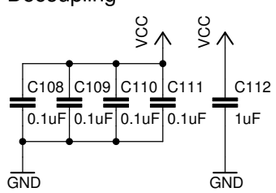
CLL resets it (L=0)
RESET resets it. (L=0)

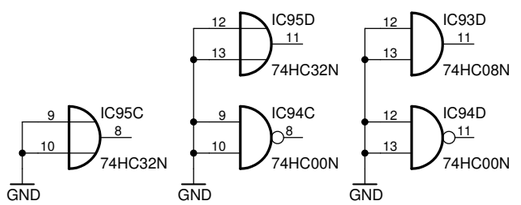
Data out from a roll instruction sets the L register explicitly when L_LATCH is high.

Toggle Sources (synchronous, to avoid glitches):

ALU carry out (FLD)
CPL toggles it (L=L)

Decoupling





TODO:

* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	17/38
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Arithmetic/Logic Unit: Decoding Logic

RUNIT[0..3]
IR[0..15]
IBUS[0..15]
WALU/7
RSTHOLD/6
RESET/17
GUARD/7

IBUS[0..15]
WALU/23
RSTHOLD/25
RESET/19
GUARD/38

WALU
IBUS[0..15]
RUNIT0
RUNIT1
IR0
IR2
GUARD
RESET
RSTHOLD
RUNIT3
RUNIT2

ALU Port B Buffer

B[0..15]

IC97
IBUS0 2 — 1D 1Q — 19 B0
IBUS1 3 — 2D 2Q — 18 B1
IBUS2 4 — 3D 3Q — 17 B2
IBUS3 5 — 4D 4Q — 16 B3
IBUS4 6 — 5D 5Q — 15 B4
IBUS5 7 — 6D 6Q — 14 B5
IBUS6 8 — 7D 7Q — 13 B6
IBUS7 9 — 8D 8Q — 12 B7
11 CLK
1 OC
74HC574N
GND

IC98
IBUS8 2 — 1D 1Q — 19 B8
IBUS9 3 — 2D 2Q — 18 B9
IBUS10 4 — 3D 3Q — 17 B10
IBUS11 5 — 4D 4Q — 16 B11
IBUS12 6 — 5D 5Q — 15 B12
IBUS13 7 — 6D 6Q — 14 B13
IBUS14 8 — 7D 7Q — 13 B14
IBUS15 9 — 8D 8Q — 12 B15
11 CLK
1 OC
74HC574N
GND

Unary Operation Decoder

UOP2
UOP0
UOP1

IR0 ROLLOP0
RUNIT0
IR2 ROLLOP2
RUNIT1

IC100
1C0 1C1 1C2 1C3 — 1Y
2C0 2C1 2C2 2C3 — 2Y
A B 1G 2G
6 5 4 3 — 7
10 11 12 13 — 9
14 2 1 15

IC99A
1 2 3
74HC32N

74HC253N
GND

ALU Operation ROM selector (unary/binary)

IC101
RUNIT2 1
RUNIT3 2
RSTHOLD 3
RESET 6
A B C — Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
G1 G2A G2B
15 14 13 12 11 10 9 7
4 5

BOE/19
UOE/20

JP15
3 2 1
GND
GND

1-2: Ignore GUARD
2-3: Inhibit on GUARD

Due to carry propagation, the ALU ROM could take up to 210ns to produce results,
so GUARD may need to be ignored here.
Alternatively, the AND microprogram could be modified to include a wait state.

UOP[0..2]
B[0..15]

Decoupling

VCC
C113 C114 C115 C116 0.1uF
C117 1uF
GND

74HC32N
IC99D — 13 12 11
IC99B — 4 5 6
IC99C — 9 10 8
74HC32N
74HC32N
GND

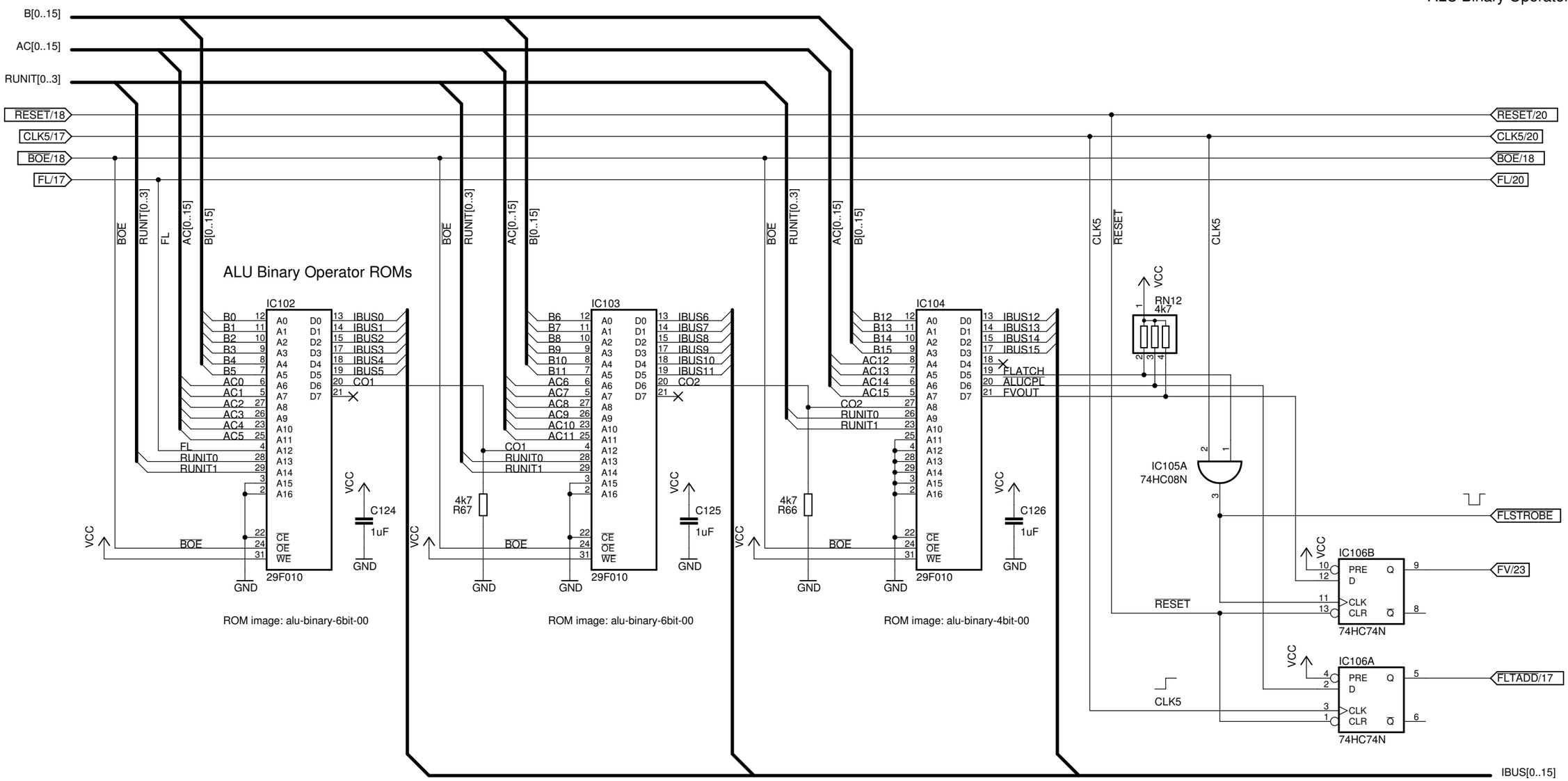
U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	18/38
Simulation filename: alu.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

ALU Binary Operators

ALU Binary Operator ROMs

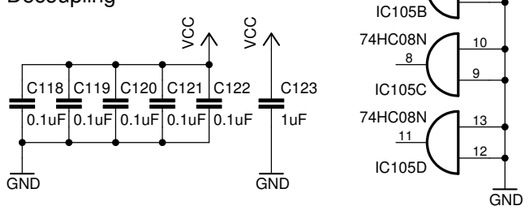


ROM image: alu-binary-6bit-00

ROM image: alu-binary-6bit-00

ROM image: alu-binary-4bit-00

Decoupling



TODO:

* DRC

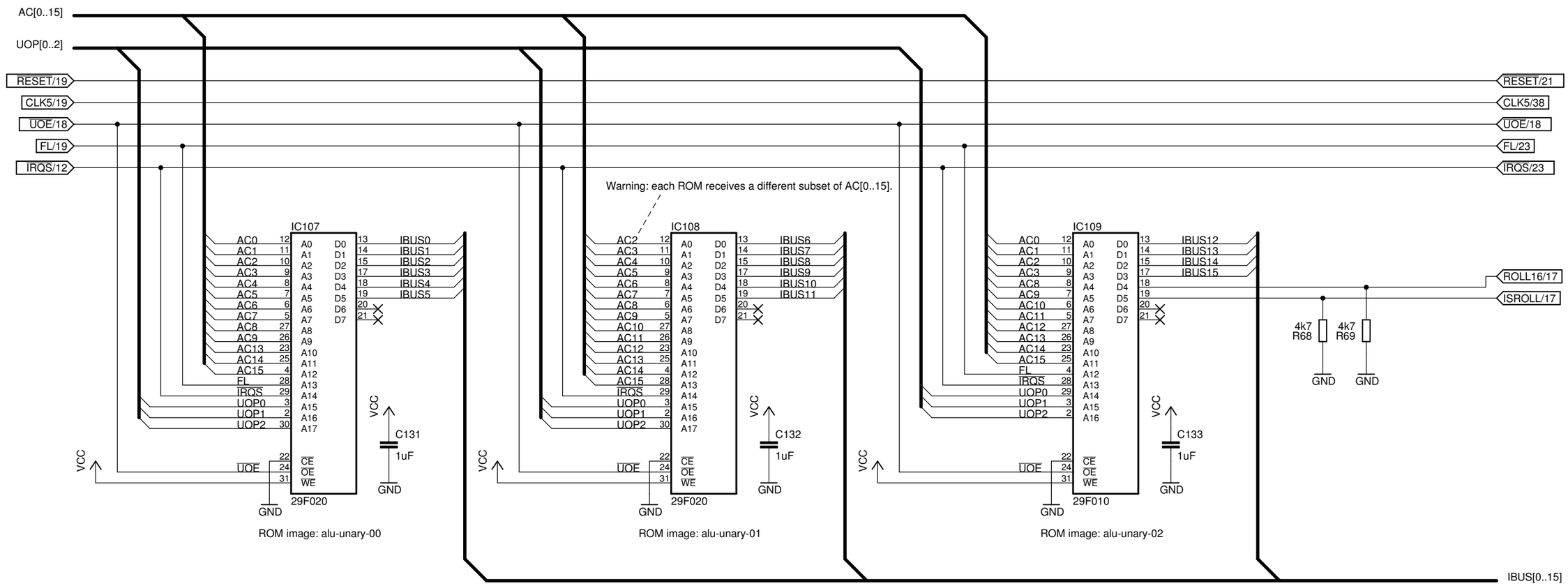
U

Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	19/38
Simulation filename: alu.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

ALU Unary Operators and Constant Store

Unary Operations and Constant Store

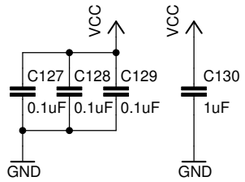


ROM image: alu-unary-00

ROM image: alu-unary-01

ROM image: alu-unary-02

Decoupling



Notes

ROMs to be socketed for easy re-programming.

TODO:

* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	20/38
Simulation filename: alu.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

8 kW Bank Switching Memory Controller

AB[0..15]

DB[0..15]

RESET/20 → RESET/22

MEM/13 → MEM/24

W/13 → W/22

SYSDEV/11 → SYSDEV/22

Bank Register I/O address decoding

IC111 74HC138N

AB2 AB3 AB4 AB5 AB6 W SYSDEV AB7

IC110A 74HC32N

IC110D 74HC32N

Decodes addr: 0000 0000 0010 0nnn

OUT &0020: Set Bank #0
OUT &0021: Set Bank #1
...
OUT &0027: Set Bank #7

IC112 74HC138N

AB15 MEM VCC GND

BANKW0 BANKW1 BANKR0 BANKR1

Bank Register Read Select (on MEM access)

8 16-bit Bank Registers

IC115 IC116 IC119 IC120 74HC670N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

AB0 AB1 AB13 AB14 BANKW0 BANKR0 BANKW1 BANKR1

WA WB RA RB GW GR

AE'0 AE'1 AE'2 AE'3 AE'4 AE'5 AE'6 AE'7

AB[13..15] select bank register to read.
AB[15] selects which bank register file to access.
AB[14..13] select one of four registers in that file.

The 3 bits AB[13..15] map to 8 bits of extended addresses. This gives 16 - 3 + 8 = 21 bits of addressable memory.

IC117 IC118 IC121 74HC541N

AB13 AB14 AB15 FPRAM/28

IC113A 74HC08N

AB15RAM

BNK/LNR

AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5 AEXT6 AEXT7

BANK0 BANK1 BANK2 BANK3 BANK4 BANK5 BANK6 BANK7

BANK[0..7]

AEXT[0..7]

Front Panel Buffer

LED-5MM-GREEN R30 330R LED5

IC114A 74HC112N

BANKW1 RESET

BNK/LNR

BNK/LNR = BANKING → BANKING/30

Writing to bank registers 4-7 enables full banking.
(cancels reset defaults)

The 64 kW address space is split into 8 banks of 8 kW each.

The banking scheme allows page 0 to be swapped for other pages, although since page 0 has special significance, this should probably not be done normally. This leaves 7 banks and 56 kW available for switching.

Decoupling

C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 0.1uF

C146 1uF

VCC GND

IC114B 74HC112N

IC113B IC113C IC113D 74HC08N

IC110B IC110C 74HC32N

TODO:

* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	21/38
Simulation filename: memory.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Interrupt Controller

DB[0..15]
AB[0..15]
W/21
SYSDEV/21
RESET/21
W/24
SYSDEV/25
RESET/38

IC123 74HC138N

W AB5 AB6 AB4 AB7 SYSDEV
G1 G2A G2B
A B C
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
IERW ISRR

Decodes addr: 0000 0000 0001 XXnn

OUT &0010-&001F: write to IER
IN &0010-&001F: read from ISR

Interrupt Status Register

IRF[0..7]

IC125 74HC540N

IRF0 IRF1 IRF2 IRF3 IRF4 IRF5 IRF6 IRF7
ISRR
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

Interrupt Enable Register

IC129 74HC574N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
IERW
CLK OC
IEN0 IEN1 IEN2 IEN3 IEN4 IEN5 IEN6 IEN7

IC126A 74HC112N

IERW
RESET
PRE J CLK K CLR Q Q̄
GND

Front Panel Buffers & Connectors

IC131 74HC541N

IEN0 IEN1 IEN2 IEN3 IEN4 IEN5 IEN6 IEN7
G1 G2
GND
22-23-2081
CON9-1 CON9-2 CON9-3 CON9-4 CON9-5 CON9-6 CON9-7 CON9-8

IC133 74HC541N

IRF0 IRF1 IRF2 IRF3 IRF4 IRF5 IRF6 IRF7
22-23-2081
CON10-1 CON10-2 CON10-3 CON10-4 CON10-5 CON10-6 CON10-7 CON10-8

IEN[0..7]
IRF[0..7]

LED-5MM-GREEN
IEN0 LED6
IEN1 LED7
IEN2 LED8
IEN3 LED9
IEN4 LED10
IEN5 LED11
IEN6 LED12
IEN7 LED13
RN14 330R

LED-5MM-RED
IRF0 LED14
IRF1 LED15
IRF2 LED16
IRF3 LED17
IRF4 LED18
IRF5 LED19
IRF6 LED20
IRF7 LED21
RN15 330R

LED Displays (Optional)

RN13 4k7

Interrupt registers

IEN[0..7]
IRQ[0..7]

IC122A IC124A IC127A IC128A
IEN0 IEN1 IEN2 IEN3
IRQ0 IRQ1 IRQ2 IRQ3
VCC
PRE J CLK K CLR Q Q̄
74HC112N
GND
IRF0 IRF1 IRF2 IRF3

IRF[0..7]

IC122B IC124B IC127B IC128B
IEN4 IEN5 IEN6 IEN7
IRQ4 IRQ5 IRQ6 IRQ7
IRF4 IRF5 IRF6 IRF7

IRQ Generator

IC130A IC130B IC130C IC130D 74HC08N
IRF0 IRF1 IRF2 IRF3 IRF4 IRF5 IRF6 IRF7

IC132A IC132B IC132C IC132D 74HC08N
IRQ/25

Note: if the Interrupt Controller is installed, IRQ is always driven.
Nothing else may drive IRQ, not even open drain outputs.

Decoupling

VCC
C147 C148 C149 C150 C151 C152 C153 C154 C155 C156 C157 C158 C159
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 1uF
GND

IC126B 74HC112N

TODO:

* Write & Verify Verilog Model
* DRC

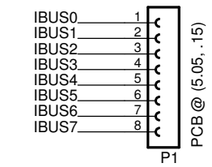
U

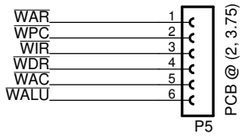
Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	22/38
Simulation filename: to be coded	
More Info: http://www.bedroomlan.org/cft	

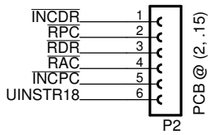
CFT Mini-Computer

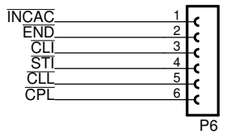
Control Bus Connectors

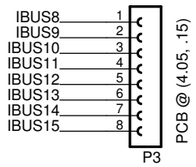
Control Bus Connectors

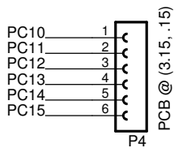


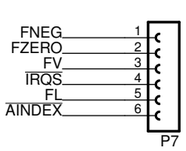












Notes

This is only useful for building the processor on separate cards.

U

Title: cft	
Revision: Rev H	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	23/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Memory (up to 512kW RAM, 512kW ROM)

AB[0..15]
AEXT[0..7]
DB[0..15]
MEM/21
R/13
W/22

AB[0..15]
AEXT[0..7]
DB[0..15]
MEM/37
R/25
W/25

RAM/ROM chip select

AEXT7=0: RAM. AEXT7=0: ROM.

IC134 74HC138N

AEXT6
AEXT7
MEM
VCC
GND

A B C G1 G2A G2B Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

RAMEN0
RAMEN1
ROMEN0
ROMEN1

JP4
ROMUPG

Jumper 1-2: normal operation.
Jumper 2-3: allow in-system ROM upgrade.

JP5
ROMEN1
ROMEN
ROMEN0

Jumper 1-2: ROM at &18000-&1FFFF
Jumper 2-3: ROM at &10000-&1FFFF

JP6
RAMEN1
RAMEN
RAMEN0

Jumper 1-2: RAM at &08000-&0FFFF
Jumper 2-3: RAM at &00000-&0FFFF

Low ROM

IC135 29F040

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12
AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
ROMEN R ROMUPG
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
CE OE WE
D0 D1 D2 D3 D4 D5 D6 D7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

VCC C167 1uF GND

IC136 AS6C4008

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12
AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
RAMEN R W
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
CE OE WE
D0 D1 D2 D3 D4 D5 D6 D7
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

VCC C168 1uF GND

Low RAM

High ROM

IC137 29F040

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12
AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
ROMEN R ROMUPG
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
CE OE WE
D0 D1 D2 D3 D4 D5 D6 D7
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

VCC C169 1uF GND

IC138 AS6C4008

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12
AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5
RAMEN R W
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
CE OE WE
D0 D1 D2 D3 D4 D5 D6 D7
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

VCC C170 1uF GND

High RAM

Optional LED Display

IC139 74HC540N

A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
GND

R31 330R LED-5MM-RED LED22
R32 330R LED-5MM-GREEN LED23
R33 330R LED-5MM-GREEN LED24
R34 330R LED-5MM-GREEN LED25

Decoupling

VCC
C160 0.1uF
C161 0.1uF
C162 0.1uF
C163 0.1uF
C164 0.1uF
C165 0.1uF
C166 1uF
GND

TODO:

* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	24/38
Simulation filename: memory.v#banked_memory	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

RS-232 Ports

DB[0..15]
AB[0..15]
RSTHOLD/18
R/24
W/24
SYSDEV/22
RSTHOLD/26
R/26
W/26
SYSDEV/26

Addresses Decoding:

0000'0000'0110'XXXX (&006X) -> Chip #0 (UARTs 0, 1)
0000'0000'0111'XXXX (&007X) -> Chip #1 (UARTs 2, 3)

IC140 74HC138N
AB4 AB5 AB6 AB7 SYSDEV
&000a &001a &002a &003a &004a &005a &006a &007a CEN0 CEN1

IRQ[0..7]
IRQ/22
SV1 SV2
INTRN0 INTRN1

IC141 IC142 SC26C92C1N
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
R W CEN0 CEN1 RSTHOLD RSCLK INTRN0 INTRN1
AB0 AB1 AB2 AB3
TXDA RXDA TXDB RXDB
OP0/RTSAN OP1/RTSBN OP2/TXCA/RXCA OP3/CTO/TXCB/RXCB OP4/RXRDY/FFULLA OP5/RXRDY/FFULLB OP6/TXRDYA OP7/TXRDYB
IP0/CTSAN IP1/CTSBN IP2 IP3/TXCA IP4/RXCA IP5/TXCB IP6/RXCB
TXD3 RXD3 CTS3

XTAL2 3.6864MHz
C173 0.1uF
C174 C175 1uF

Decoupling
C171 0.1uF
C172 1uF

IC143 IC144 IC145 MAX232
C176 C177 C178 C179 C180 C181 1uF
C182 C183 C184 C185 C186 C187 1uF
C188 C189 C190 10uF
T1IN T2IN R1OUT R2OUT T1OUT T2OUT R1IN R2IN
TXD0 RTS0 RXD0 CTS0
TXD1 RTS1 RXD1 CTS1
TXD2 RTS2 RXD2 CTS2

UART0 UART1 UART2
CON11 CON12 CON13
CD RXD TXD DTR GND DSR RTS CTS RI
DB9 male or 2x5 pin header.
DB9 female or 2x5 pin header.
R35 R36 R37 1M
EARTH
GND DTE DCE

Attention: DCE wiring!

FT232 Serial cable pinout
SV3
DTR
RXI (INPUT TTL to USB)
TXO (OUTPUT USB to TTL)
3V3/5V Power input
CTS
TTL (e.g FT232 5V cable)

TODO:
* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	25/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

IDE Bus Interface

AB[0..15]
DB[0..15]

R/25
W/25
RSTHOLD/25
SYSDEV/25
IRQ/25

R/27
W/27
RSTHOLD/25
SYSDEV/27
IRQ/27

Address Decoder (8-port blocks)

IC146 74HC138N

AB4 AB5 AB6 AB7 AB3 SYSDEV

&00AX CS1A
&00BX CS3A
&00CX CS1B
&00DX CS3B

Address Decoding:

0000'0000'1aaa'0XXX

0000'0000'1010'0XXX -> &00A0-A7 Port 1 CS1
0000'0000'1011'0XXX -> &00B0-B7 Port 1 CS3

0000'0000'1100'0XXX -> &00C0-C7 Port 2 CS1
0000'0000'1101'0XXX -> &00D0-D7 Port 2 CS3

IRQ[0..7]

SV4 SV5

IRQ5 IRQ6 IRQ7 IRQ

74HC05N IC147A INTA
74HC05N IC147B INTB

R38 4k7
R39 4k7

VCC

DD[0..15]

RN16 4k7
RN17 4k7

IC148 IC149 74HC245N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8

DIR G R GND

DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7
DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15

CFT-to-IDE bus buffers. Could possibly be replaced with HC parts. Could possibly be left out altogether, though they protect the CFT bus from potential problems on the IDE side.

AB[0..15]

CON14 CON15 IDE-CONNECTOR

DAA CS1A CS3A AB0 AB1 AB2 R W INTA RSTHOLD
DAB CS1B CS3B AB0 AB1 AB2 R W INTB RSTHOLD

DASP CS1FX CS3FX DA0 DA1 DA2 DIOR DIOW DMACK DMARQ INTRQ RESET PDIAG
IOCS16 IORDY CSEL

GND

LED-5MM-RED LED26 R40 330R
LED-5MM-RED LED27 R41 330R
JP7 JP8

For external LEDs (e.g. MISCn on the front panel), remove jumper shunt and connect pin 1 to external LED.

Decoupling

C191 C192 C193 C194 C195 0.1uF
C196 1uF

74HC05N IC147C IC147D IC147E IC147F

TODO:

* Write & Verify Verilog Model

U

Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	26/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Clock, Timers & NVRAM

Real Time Clock & NVRAM

IC159 M48T02

AB[0..15]
DB[0..15]
R/26
W/26
SYSDEV/26

Address Decoder (8-port blocks)

IC151 74HC138N

AB4	1	A
AB5	2	B
AB6	3	C
AB7	6	G1
SYSDEV	4	G2A
	5	G2B

Y0	15	&008a NVRAM
Y1	14	&009a TIMERSEL
Y2	13	&00Aa
Y3	12	&00Ba
Y4	11	&00Ca
Y5	10	&00Da
Y6	9	&00Ea
Y7	7	&00Fa

IC152 74HC374N

DB1	3	1D	1Q 2
DB2	4	2D	2Q 5
DB3	7	3D	3Q 6
DB4	8	4D	4Q 9
DB5	13	5D	5Q 12
DB6	14	6D	6Q 15
DB7	17	7D	7Q 16
	18	8D	8Q 19
	1	OC	
	11	CLK	

AB0	8	OFS4 4
AB1	7	OFS5 3
AB2	6	OFS6 2
AB3	5	OFS7 1
		OFS8 23
		OFS9 22
		OFS10 19
W	21	
NVRAM	18	
R	20	

A0	DQ0	9 DB0
A1	DQ1	10 DB1
A2	DQ2	11 DB2
A3	DQ3	13 DB3
A4	DQ4	14 DB4
A5	DQ5	15 DB5
A6	DQ6	16 DB6
A7	DQ7	17 DB7
A8		
A9		
A10		
W		
E		
G		

VCC C214 1uF D1 1N5817-B GND

74HC32N IC156A

	3	
W	2	
	1	

Address Decoder (4-port blocks)

IC153 74HC138N

AB2	1	A
AB3	2	B
	3	C
	6	G1
	4	G2A
	5	G2B

Y0	15	&0090-&0093 NVRAMOFS
Y1	14	&0094-&0097 TSEL0
Y2	13	&0098-&009B TSEL1
Y3	12	&009C-&009F
Y4	11	
Y5	10	
Y6	9	
Y7	7	

VCC GND

74HC32N IC156B

	5	
	6	
W	4	

Addresses Decoding:

0000'0000'1000'XXXX (&008X) -> 16 bytes of NVRAM/clock data
0000'0000'1001'00xx (&0090-93) -> NVRAM addr offset (bits 4-10). Clock = &7F
0000'0000'1001'01xx (&0094-97) -> Timer #1
0000'0000'1001'10xx (&0098-9B) -> Timer #2
0000'0000'1001'11xx (&009C-9F) -> Timer Control Register (16 bits)

Six Programmable Counters

IC162 82C54

DB0	8	D0
DB1	7	D1
DB2	6	D2
DB3	5	D3
DB4	4	D4
DB5	3	D5
DB6	2	D6
DB7	1	D7
AB0	19	A0
AB1	20	A1
W	23	WR
R	22	RD
TSEL0	21	CS

CLK0	9	CSELA
GATE0	11	TG0
OUT0	10	TO0
CLK1	15	CSELA
GATE1	14	TG1
OUT1	13	TO1
CLK2	18	CSELB
GATE2	16	TG2
OUT2	17	TO2

IC163 82C54

DB0	8	D0
DB1	7	D1
DB2	6	D2
DB3	5	D3
DB4	4	D4
DB5	3	D5
DB6	2	D6
DB7	1	D7
AB0	19	A0
AB1	20	A1
W	23	WR
R	22	RD
TSEL1	21	CS

CLK0	9	CSELC
GATE0	11	TG3
OUT0	10	TO3
CLK1	15	CSELC
GATE1	14	TG4
OUT1	13	TO4
CLK2	18	CSELD
GATE2	16	TG5
OUT2	17	TO5

VCC RN18 4k7

TG0 TG1 TG2 TG3 TG4 TG5 → SV8

TO0 TO1 TO2 TO3 TO4 TO5 → SV9

Gate/Output Expansion

IRQ[0..7]
IRQ/26

SV6

IRQ0	8	7
IRQ1	6	5
IRQ2	4	3
IRQ	2	1

SV7

IRQ0	8	7
IRQ1	6	5
IRQ2	4	3
IRQ	2	1

Interrupt Selection Jumpers

VCC C197 1uF

C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 0.1uF GND

VCC R44 4k7

74HC03N IC157C

Counter Interrupt Enables

VCC R45 4k7

74HC03N IC157A

74HC03N IC157B

Interrupt Mask Reg

74HC03N IC157D

74HC32N

IC158A IC158B IC158C IC158D IC156D IC156C

32,768 Hz clock

IC150A 74HC14N

R42 10M R43 300k

XTAL3 32.768kHz

C212 22pF C213 22pF GND

32KHZ

IC154 74HC374N

DB0	3	1D	1Q 2
DB1	4	2D	2Q 5
DB2	7	3D	3Q 6
DB3	8	4D	4Q 9
DB4	13	5D	5Q 12
DB5	14	6D	6Q 15
DB6	17	7D	7Q 16
DB7	18	8D	8Q 19
TCRSEL	1	OC	
	11	CLK	

IC155 74HC374N

DB8	3	1D	1Q 2
DB9	4	2D	2Q 5
DB10	7	3D	3Q 6
DB11	8	4D	4Q 9
DB12	13	5D	5Q 12
DB13	14	6D	6Q 15
DB14	17	7D	7Q 16
DB15	18	8D	8Q 19
TCRSEL	1	OC	
	11	CLK	

TO0 TO1 TO2 TO3 TO4 TO5 32KHZ CLK1

IC160 74HC153N

CLK1	6	1C0
32KHZ	5	1C1
TO3	4	1C2
TO4	3	1C3
CLK1	10	2C0
32KHZ	11	2C1
TO4	12	2C2
TO5	13	2C3
	14	A
	2	B
	1	1G
	15	2G

1Y	7	CSELA
2Y	9	CSELB

IC161 74HC153N

CLK1	6	1C0
32KHZ	5	1C1
TO0	4	1C2
TO1	3	1C3
CLK1	10	2C0
32KHZ	11	2C1
TO1	12	2C2
TO2	13	2C3
	14	A
	2	B
	1	1G
	15	2G

1Y	7	CSELC
2Y	9	CSELD

Counter Clock Select MUXes

IC150B 74HC14N

	11	
	10	
IC150C	9	
	8	
IC150D	1	
	2	
IC150E	3	
	4	
IC150F	5	
	6	

GND

TODO:

* DRC

U

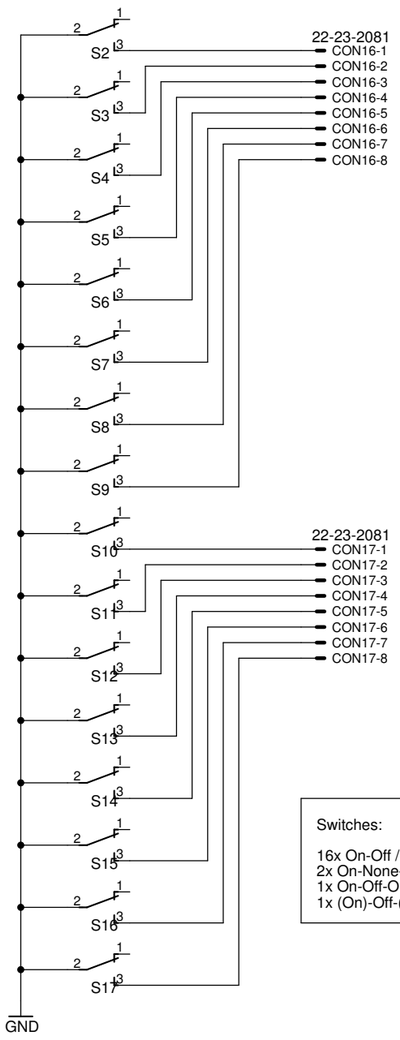
Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	27/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CLK1/8

CFT Mini-Computer

Front Panel: Switch Register and Switches 1/2

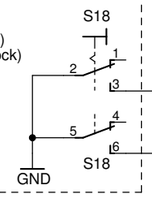
Switch Register

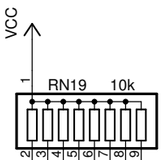


Power Key Switch

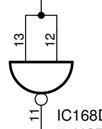
Position 1: 2-1, 5-4 (off)
Position 2: 2-3, 5-4 (on, panel lock)
Position 3: 2-3, 5-6 (on, panel unlock)

ATX Power Supply Unit assumed.





Keeps power on when a break-before-make key switch moves between ON & PANEL positions.



FPCLKEN/2

FPCLKEN/36

Activates the Power Supply Unit, turning the computer on.

FPPWRON/34

C229 1uF

Disables the panel switches.

FPLOCK/29

Verbose

Quiet

S19

GND

Disables many debugging lights to avoid visual overload.

FPLEDSON/30

C230 1uF

GND

ROM High

RAM High

S20

FPROM/34

FPRAM/34

FPROM & FPRAM are not debounced because they are handled off-board by a clocked J-K flip-flop.

Fast (10)

Slow 1 (11)

Slow 2 (01)

S21

SAFE

C223 +1uF

RN20A 50k

IC164A

74HC14N

IC167A

74HC04N

IC169

74HC373N

FPFAST/34

Fast: FPFAST=1, FPSLOW=0
Slow 1: FPFAST=0, FPSLOW=0
Slow 2: FPFAST=0, FPSLOW=1

RN20B 50k

C224 1uF

IC164B

74HC14N

IC167B

74HC04N

FPSLOW/34

Clock speed latch: clock speed may be changed only when the clock is stopped (CLKEN is high)

C225 +1uF

RN20C 50k

RN20D 50k

C226 1uF

IC164C

74HC14N

IC167C

74HC04N

FPSTEP-IN

IC168B

74HCT00N

FPSTEP/34

Microstep

Step Instruction

S22

IC164D

74HC14N

IC167D

74HC04N

FPUSTEP/34

Auto-repeat for Step switch

FPSTEP-IN

TW = 0.25 x R KOhms x C pF (1 + 0.7/R kOhms)

CAUTION: autorepeat freq must be <= 1Hz
or STEP mechanism may fail under autorepeat conditions.
180k in-series resistor ensures minimum period is ~1s.

R46 200k

C222 100uF

D2 1N4148

47k = 1.19s

IC165A

74LS123N

IC168A

74HCT00N
NB: MUST be HCT (TTL inputs)

IC166

LM555N

C227 22nF

C228 4.7uF

1k R48

R47 180k

R49 200k

Switches:

16x On-Off / On-On / On-None-Off / On-None-On
2x On-None-On / On-On
1x On-Off-On DP
1x (On)-Off-(On)

SAFE/29

Decoupling

C215 C216 C217 C218 C219 C220 0.1uF

C221 1uF

IC168C

74HCT00N

IC165B

74LS123N

Note: some gates shared with next sheet.

TODO:

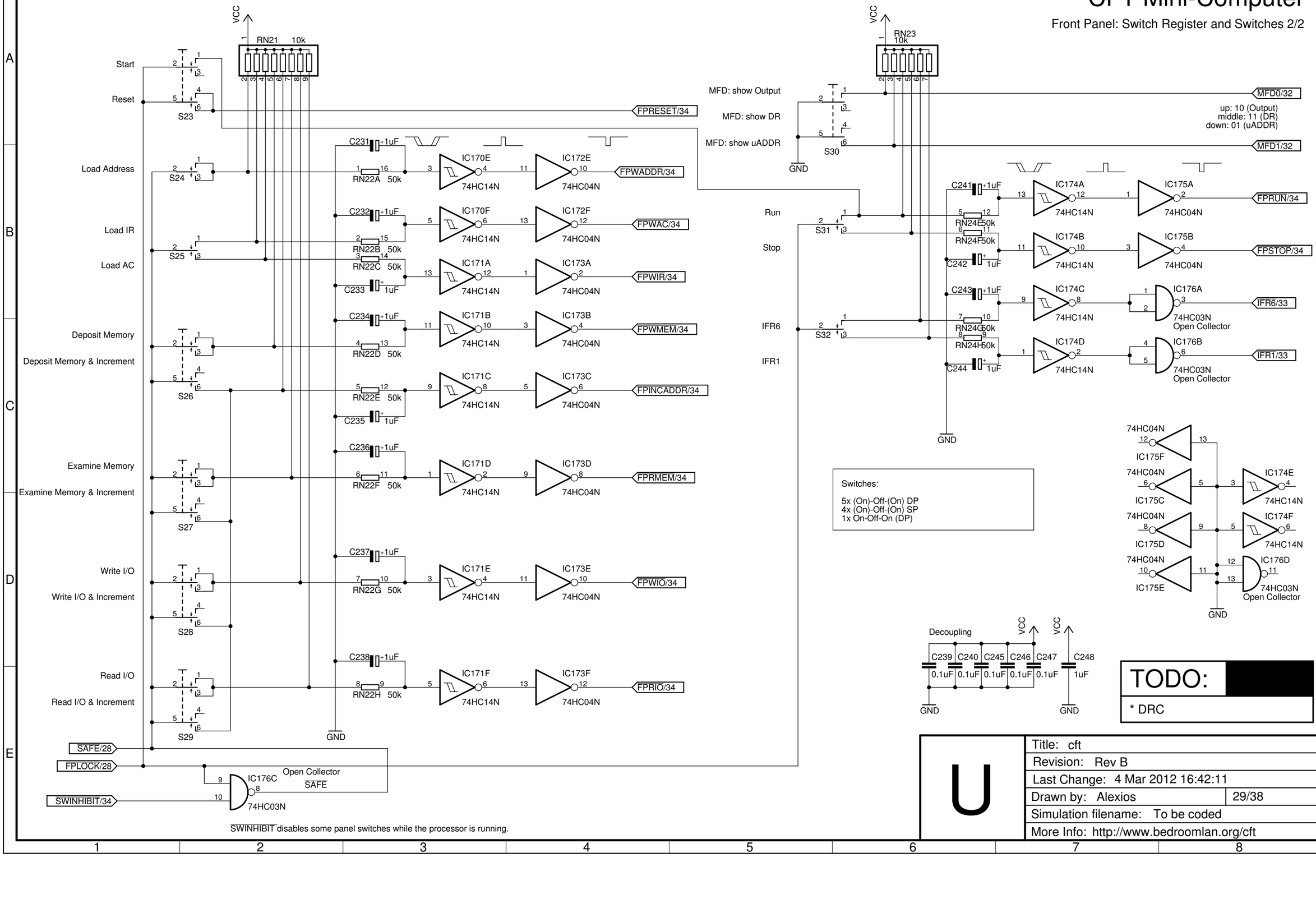
* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	28/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Switch Register and Switches 2/2



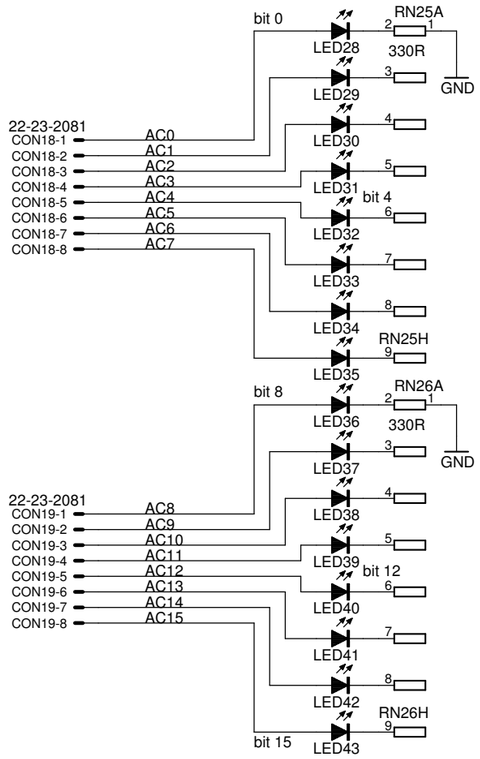
U	Title: cft
	Revision: Rev B
	Last Change: 4 Mar 2012 16:42:11
	Drawn by: Alexios — 29/38
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

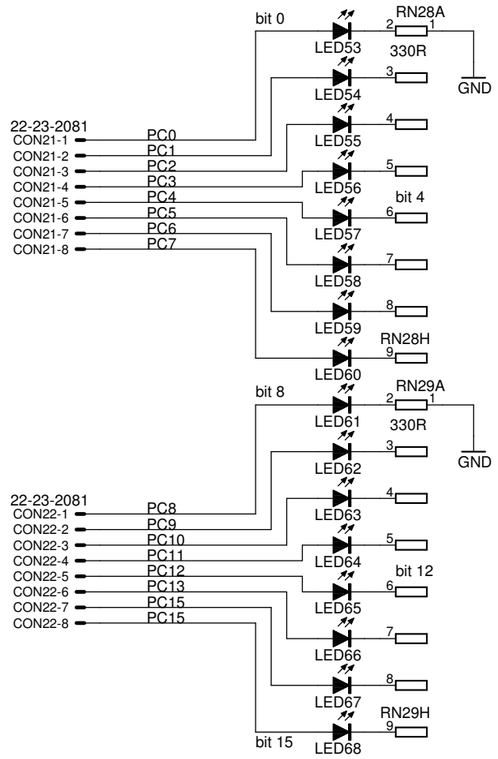
Front Panel: LEDs 1

FPLEDSON/28

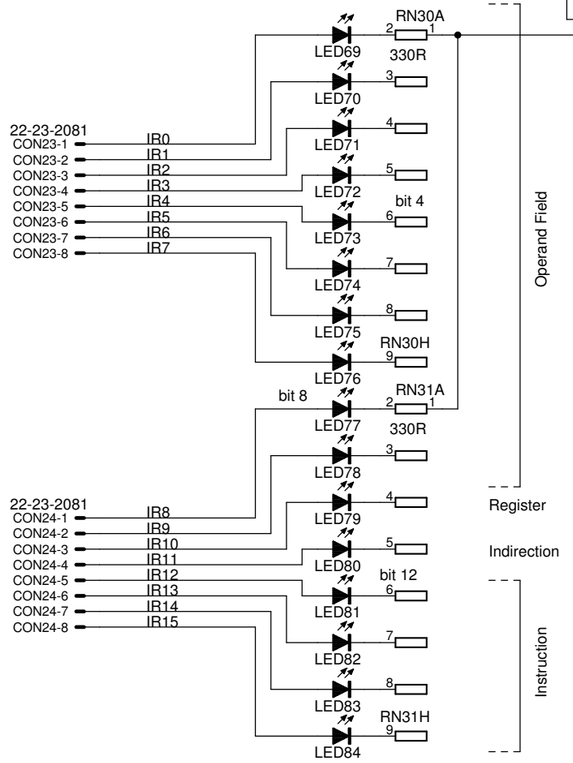
Accumulator Display



Program Counter Display



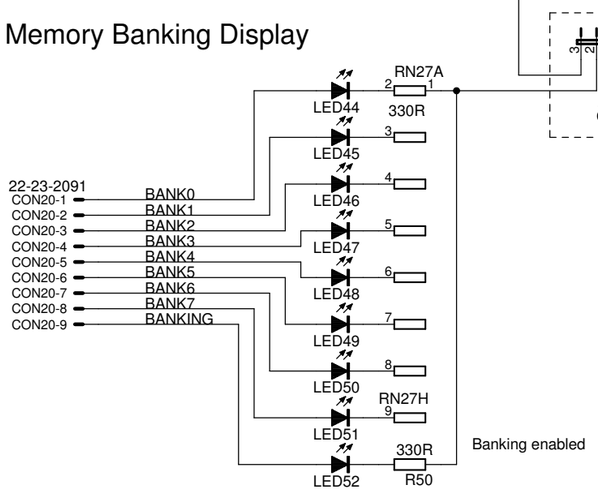
Instruction Register Display

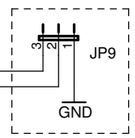


Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

Memory Banking Display





Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

TODO:

* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	30/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: LEDs 2

FPLEDSON/30 → FPLEDSON/33
FPRUN/34 → FPRUN/34
FPSTOP/34 → FPSTOP/34
FPFETCH/32 → FPFETCH/32
FPEXEC/32 → FPEXEC/32
BIRQS/6 → BIRQS/32

Microcode Vector Display

BRUNIT0, BRUNIT1, BRUNIT2, BRUNIT3, BWUNIT0, BWUNIT1, BWUNIT2, BOPIF0 → RN32A (150R) → LED85–LED92 — Read Unit (green), Write Unit (red)

BOPIF1, BOPIF2, BOPIF3, BINCAC, BCPL, BCLL, BSTI, BCLI → RN33A (330R) → LED93–LED100 — OPIFn (amber)

BINCPC, BINCDR, BUINSTR18, BMEM, BIO, BR, BW, BEND → RN34A (330R) → LED101–LED108

INCAC	
CPL	
CLL	
STI	
CLI	
INCPC	
INCDR	
UINSTR18	
MEM	
IO	
R	
W	
END	

JP12: 3-pin jumper, pin 1 → GND

Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled in Verbose mode.
No shunt: always off.

JP11: 3-pin jumper, pin 1 → GND

Flag Display

BFNEG, BFZERO, BFV, BIRQS, BFL → RN35A (330R) → LED109–LED113

N	
Z	
V	
I	
L	

RN35H: 9 → GND

State & Miscellaneous lights

FPRUN	LED114	Run (green)
FPSTOP	LED115	Stop (red)
FPFETCH	LED116	Fetch (orange)
FPEXEC	LED117	Execute (orange)
INTERRUPT	LED118	Interrupt (orange)
MISC1	LED119	Misc light 1 (green)
MISC2	LED120	Misc light 2 (green)
MISC3	LED121	Misc light 3 (green)

RN36A (330R): 2 → GND; RN36H: 9

IC177A (74LS123N): BIRQS → 1; R51 300k → 14; C249 1uF → 3; A, B, C, R/C, CLR, Q (13), Q̄ (4)

IC177B (74LS123N): A, B, C, R/C, CLR, Q (5), Q̄ (12); GND

VCC

SV10: 2, 4, 6 / 1, 3, 5

TODO:

* DRC

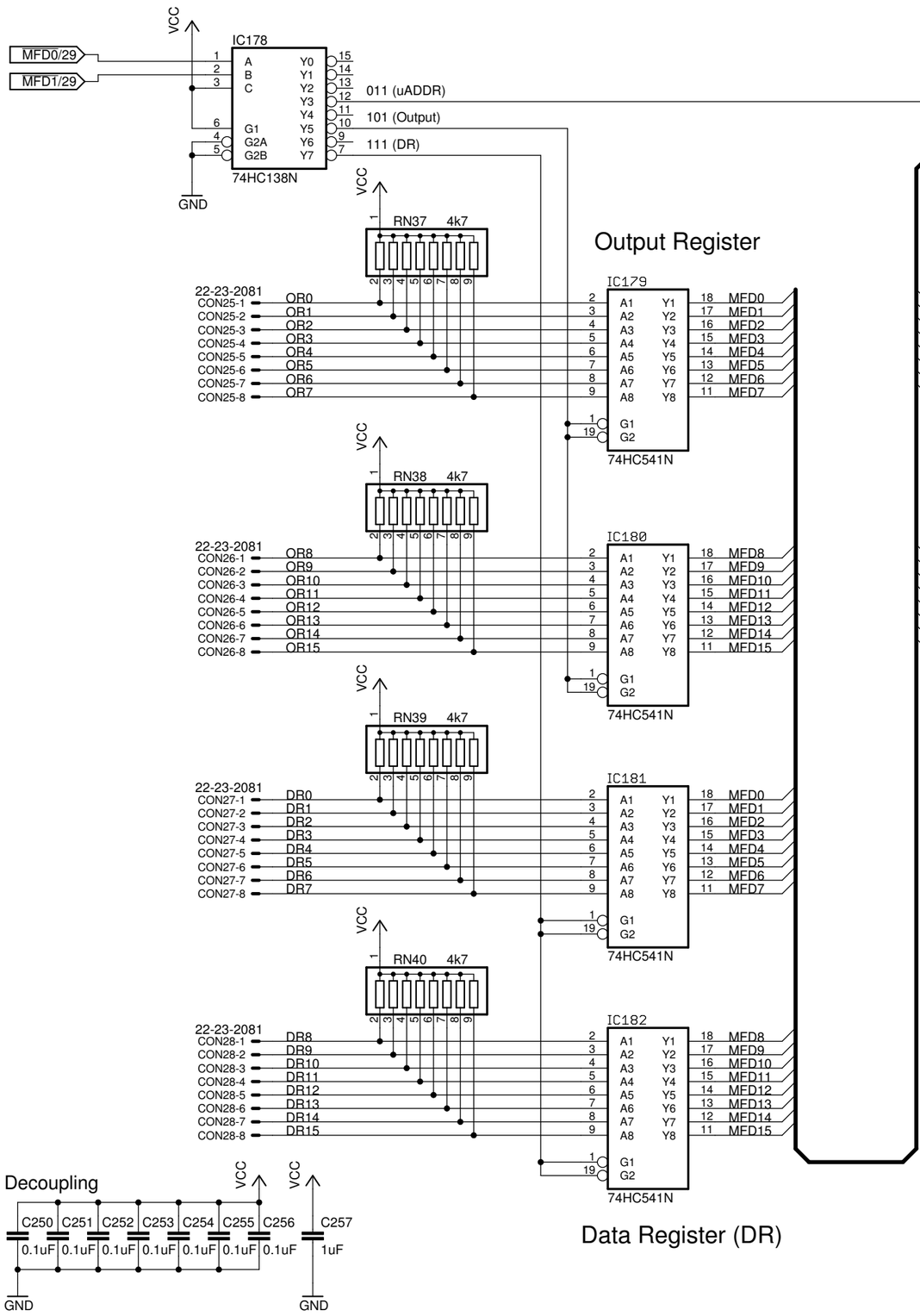
U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	31/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

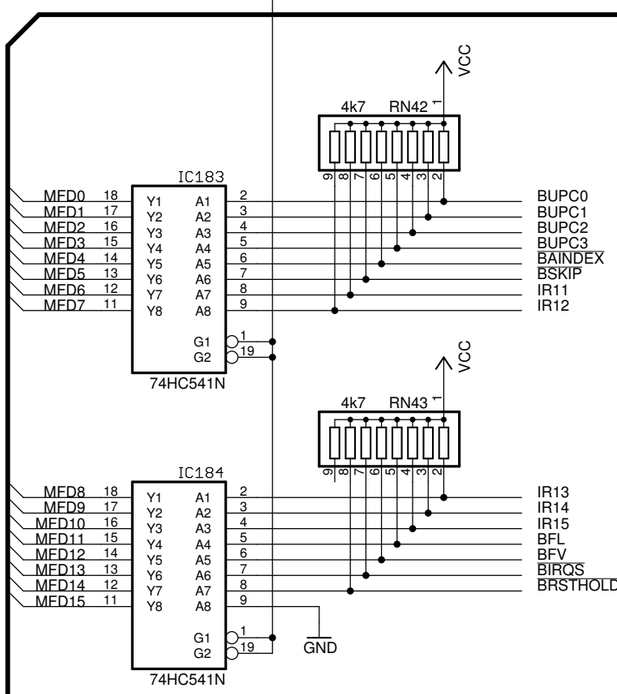
CFT Mini-Computer

Front Panel: Multi-Function Display

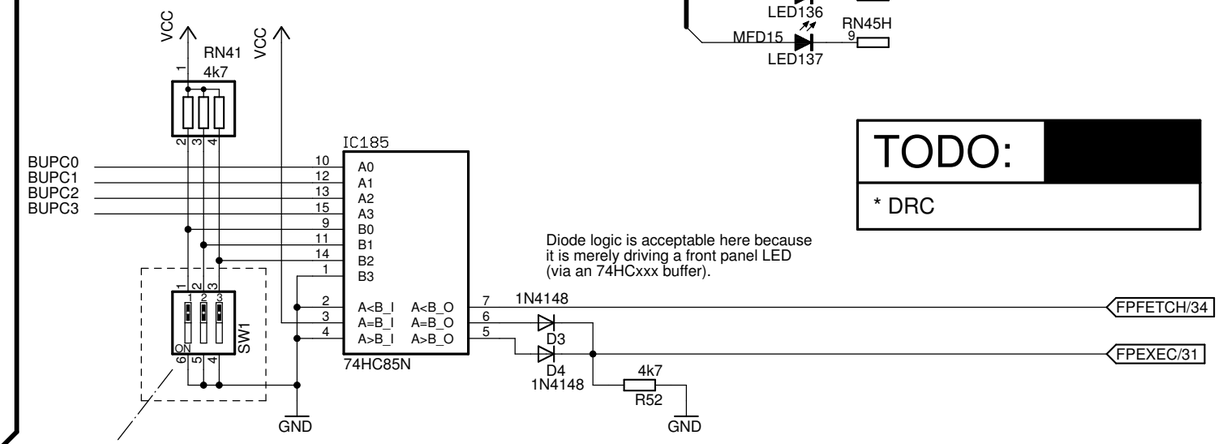
Output Register



Data Register (DR)

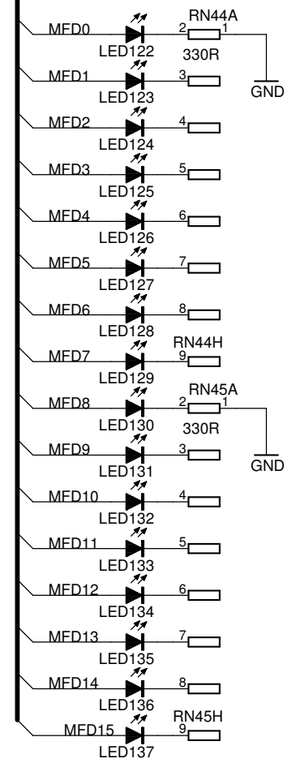


Microcode Address



Set jumpers/switches for first uPC address of Execute cycle.
For Microcode v1-v3, this is 3 (1 and 2)

Fetch/Execute Decoder



Decoupling

TODO:

* DRC

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	32/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

U

CFT Mini-Computer

Front Panel: Interrupt LEDs

FPLEDSON/31

JP13

Terse mode configuration jumper.

Shunt on 1-2: always enabled.
Shunt on 2-3: enabled on Verbose mode.
No shunt: always off.

GND

Interrupt Status Display

22-23-2081
CON29-1 IFR0
CON29-2 IFR1
CON29-3 IFR2
CON29-4 IFR3
CON29-5 IFR4
CON29-6 IFR5
CON29-7 IFR6
CON29-8 IFR7

VCC

IC186A
IC186B
IC187A
IC187B
IC188A
IC188B
IC189A
IC189B
74LS123N

R53 300k C263 1uF
R54 300k C264 1uF
R55 300k C265 1uF
R56 300k C266 1uF
R57 300k C267 1uF
R58 300k C268 1uF
R59 300k C269 1uF
R60 300k C270 1uF

GND

Common cathode tri-colour LEDs may be used here.

330R RN46
330R RN47

LED-5MM-RED bit 0
LED138
LED139
LED140
LED141
LED142
LED143
LED144
LED145

Red

LED-5MM-GREEN bit 0
LED146
LED147
LED148
LED149
LED150
LED151
LED152
LED153

Green

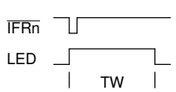
IEN0 IEN1 IEN2 IEN3 IEN4 IEN5 IEN6 IEN7

22-23-2081
CON30-1
CON30-2
CON30-3
CON30-4
CON30-5
CON30-6
CON30-7
CON30-8

LED legend

Off: interrupt line disabled, no activity
Red: interrupt line disabled but activity seen
Steady green: interrupt line enabled, no activity
Green with yellow/orange flashes: enabled interrupt activity

IFRn pulses are not normally visible to the naked eye.
'123 Dual Monostable Vibators produce pulses for IRQ signals.



TW (ns) = 0.25 x R KOhms x C pF (1 + 0.7/R kOhms)

R=330k, C=1uF: ~0.08s delay

Decoupling

VCC

C258 0.1uF C259 0.1uF C260 0.1uF C261 0.1uF C262 1uF

GND

TODO:

* DRC

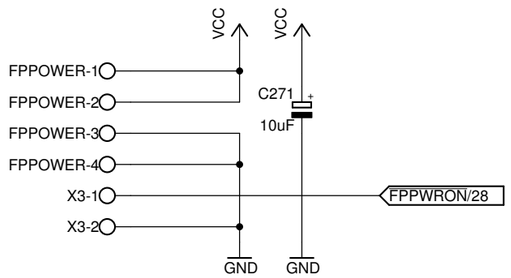
U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	33/38
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

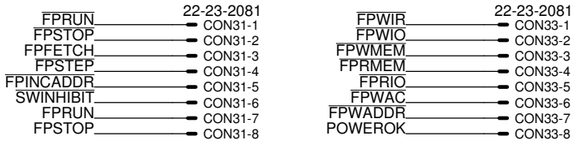
Front Panel: Connectors

Front Panel Power Input



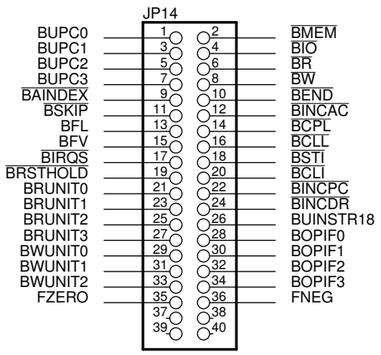
Assumes ATX power supply.

Front Panel Controller Connections

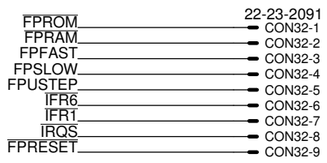


Connector to Front Panel Controller Card.

Sequencer



Connections to Other Cards



TODO:

* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	34/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: System Device

AB[0..15]
DB[0..15]
FPWADDR/34
FPWAC/34
FPWIR/34
FPWMEM/34
FPWIO/34
R/27
W/27
SYSDEV/27

IC190 74HC138N — Decodes I/O 0008-000F
AB4, AB5, AB6, AB3, AB7

IC193 74HC138N
AB0, AB1, AB2, R
IN &0008
IN &0009 (dip switches)

IC194 74HC138N
AB0, AB1, AB2, W
OUT &0008 (OR)
OUT &000F (HALT) → FPHALT/36

RN48 4k7, RN49 4k7

Dip Switch Register (optional)

SW2: Bit 0 … Bit 7
SW3: Bit 8 … Bit 15

IC191 74HC541N
IC192 74HC541N
DB0 … DB15

TP20

Output Register

IC195 74HC574N
IC196 74HC574N
CON34-1 … CON34-8
CON35-1 … CON35-8

GND

IC197A 74HC21N
IC198B 74HC21N

FPWADDR/37
FPWAC/37
FPWIR/37
FPWMEM/37
FPWIO/37
R/37
W/38

RN50 4k7, RN51 4k7

Switch Register

DB[0..15]

IC199 74HC541N
IC200 74HC541N
CON36-1 … CON36-8
CON37-1 … CON37-8

TP22

Decoupling

C272 C273 C274 C275 C276 C277 C278 C279 C280 C281 — 0.1uF
C282 — 1uF
VCC, GND

TODO:

* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	35/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Run/Stop State Machine

HALT/5
FPRUN/34
FPSTOP/34
FPFETCH/34
FPSTEP/34
FPHALT/35
POWEROK/34
CLK1/27

HALT/38
FPRUN/34
FPSTOP/34
FPFETCH/34
FPSTEP/34
FPHALT/35
POWEROK/34
CLK1/38

FPFETCH
FPSTEP
FPHALT
FPSTOP
POWEROK
CLK1

Falling edge detection

IC201C 74HC00N
IC201A 74HC00N
IC201D 74HC00N
IC201B 74HC00N
IC205D 74HC00N

Both CLKEN and HALT are driven low when the processor is stopped.
CLKEN stops the clock. HALT tristates the Control Unit so the front panel can drive the processor's control signals.
Since other units could also assert HALT, CLKEN is the only way we have of knowing we've stopped the processor.

To Clock Generator FPCLKEN/28

TP23

STOP line goes high whenever HALT is active (including wait states, since HALT is open collector.

IC205A 74HC00N

Front Panel LED FPSTOP/34

HALT (pulled up by Control Unit)

IC203A 74HC01N

Open Collector

IC204A 74HC00N

IC202A 74HC112N

CLK1
STOP
POWEROK

GND

IC205B 74HC00N

IC205C 74HC00N

Front Panel LED FPRUN/37

The POWEROK pulse makes the computer power on halted.

VCC

IC202B 74HC112N

STEP/
FETCH/

GND

TP21

Disable Front Panel Switches while running SWINHIBIT/34

ISRUN = ISRUN1 + IRSUN2
HALT = ISRUN = ISRUN1 + IRSUN2
HALT = RUN = IRSUN1 + IRSUN2
HALT = ISRUN1 NAND ISRUN2

ISSTOP = ISRUN = HALT

Decoupling

C283 0.1uF
C284 0.1uF
C285 0.1uF
C286 0.1uF
C287 0.1uF
C288 1uF

VCC
GND

IC204C 74HC00N
IC204D 74HC00N
IC203C 74HC01N
IC204B 74HC00N
IC203B 74HC01N
IC203D 74HC01N

Open Collector

TODO:

* Write & Verify Verilog Model
* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	36/38
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Sequencer

The '125 buffers act as purposefully slow open collector buffers. When the FP input is high, the buffer is tri-stated. When it is low, the buffer drives, but only low (inputs connected to GND). In addition, the tPZL delay (typical 15ns) acts as a delay circuit that gives time for the switch register enables to be decoded and the switch register value put on the IBUS.

FPINCADDR/34
FPRMEM/34
FPRIO/34
FPWADDR/35
FPWAC/35
FPWIR/35
FPWMEM/35
FPWIO/35
FPRUN/36

FPWADDR
FPWAC
FPWIR

Sequencer: MCSTART, MC0, MC1, MC2, MC3

Write Cycle: MCSTART, WAR, RPC, MEM / IO, INCPC, RAC, WEN

Note: Due to the WEN to W conversion, numerous W strobes will be generated.

Read Cycle: MCSTART, WAR, RPC, MEM / IO, INCPC, R, WAC

VCC
R61 4k7
IC212B 74HC125N
MCSTART

74HC21N: FPWIO, FPWMEM
IC206A: FPRIO, FPRMEM
74HC08N: FPWIO, FPRIO — IC209B: FPIO
74HC08N: FPWMEM, FPRMEM — IC209A: FPMEM
74HC08N: FPRIO, FPRMEM — IC209D: FPR
74HC08N: FPWIO, FPWMEM — IC209C: FPW

IC212A 74HC125N → WPC/23
IC212C 74HC125N → WDR/23
IC212D 74HC125N → WAC/23
IC213A 74HC125N → WIR/23

These ICs receive input from the 74LS123 chips and must be TTL compatible.

IC210A 74HCT32N: FPMEM, MC2
IC211A 74HCT32N: FPIO, MC2
IC210D 74HCT32N: FPR, MC2
IC211D 74HCT32N: FPW, MC3
IC210B 74HCT32N: FPINCADDR, MC2
IC211B 74HCT32N: MC1, MC0
IC211C 74HCT32N: FPW, MC2
IC210C 74HCT32N: FPR, MC3

IC214 74HCT541N: A1–A8 ← MEM/38, IO/38, R/38, WEN/13, INCPC/23, RPC/23, WAR/23, RAC/23; Y1–Y8 → MCSTART, MC0, MC1, MC2, MC3, FPINCADDR, WAC, GND

IC213B 74HC125N: WAC → GND

As long as the processor is halted and the control unit tri-stated, the front panel controller will not introduce contention. Also, contention between the FPWAC signal and cycle sequencer cannot happen because even if multiple switches are operated simultaneously, WAC is either tri-stated or driven low.

IC213C 74HC125N
IC213D 74HC125N
74HC21N: IC206B
GND

Decoupling: C289–C298 0.1uF, C299 1uF; VCC; GND

IC207A 74LS123N: R62 1k, C300 100nF, TW = ~20-45us → TP16 → MC0
IC207B 74LS123N: R63 4k7, C301 100nF, TW = ~94-211us → TP17 → MC1
IC208A 74LS123N: R64 4k7, C302 100nF, TW = ~94-211us → TP18 → MC2
IC208B 74LS123N: R65 1k, C303 100nF, TW = ~20-45us → TP19 → MC3

TW = 0.25 x R KOhms x C pF (1 + 0.7/R kOhms)

TODO:

* Write & Verify Verilog Model
* DRC

Title: cft	
Revision: Rev A	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	37/38
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

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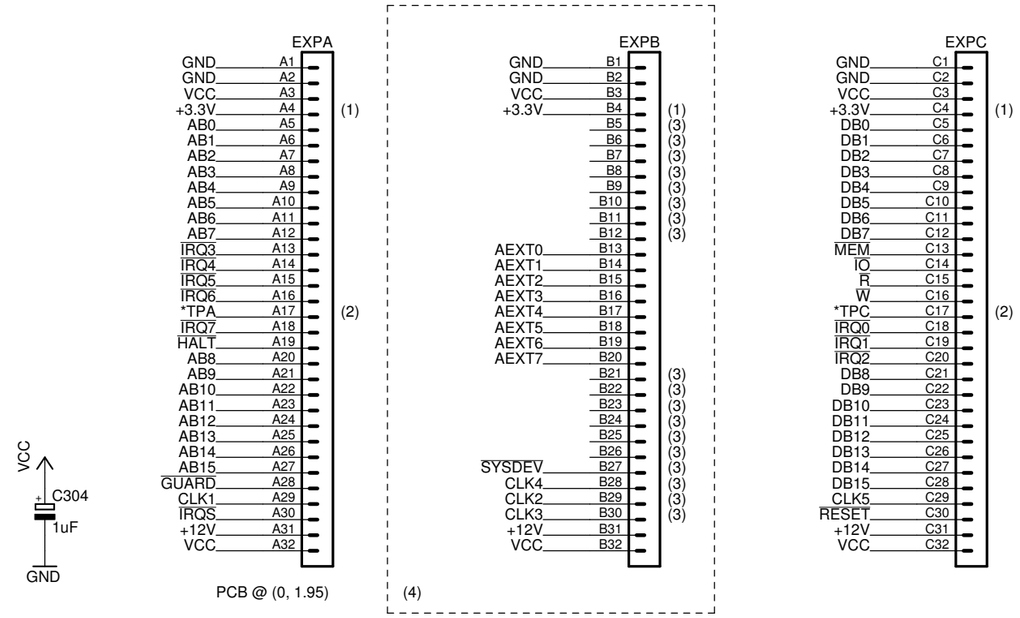
CFT Mini-Computer

Bus Connectors

Expansion Bus (computer bus)



Notes

(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it. It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) Bit18 of the microinstruction field. Currently unused, reserved for future expansion.

IC Sockets & Miscellaneous Extras

DIP8: RS 402-579 (£0.06@50), Farnell 1101345 (£0.125), Farnell-US 1183572 (£0.072)
DIP14: RS 402-765 (£0.10@50), Farnell-US 1183573 (£0.093/£0.086@100), Farnell 1101346 (£0.122@5)
DIP16: RS 402-771 (£0.11@50), Farnell-US 1183574 (£0.086@100), Farnell 1101347 (£0.147@5)
DIP18: RS 402-768 (£0.13@50), Farnell 1101348 (£0.126@5)
DIP20: RS 402-793 (£0.14@50), Farnell-US 1183577 (£0.119/£0.11@100), Farnell 4285608 (£0.146)
DIP24 (0.3"): RS 801-752 (£0.17@50), Farnell US 1557740 (£0.208), Farnell 1103849 (£0.75@5)
DIP32: RS 801-774 (£0.28@50), Farnell 1654375 (£0.27)
DIP40: RS 402-838 (£0.28@50), Farnel-US 1183580 (£0.236), Farnell 4285669 (£0.28)

Also:
Prototyping board, large:
Prototyping board, Eurocard 3U:
Solder:
Enamel wire:
Power rail wire:

H1 HOLE @ (.175, 3.675)
H2 HOLE @ (5.8, 3.675)
H3 HOLE @ (5.8, .225)
H4 HOLE @ (.175, .225)

U

Title: cft	
Revision: Rev B	
Last Change: 4 Mar 2012 16:42:11	
Drawn by: Alexios	38/38
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	