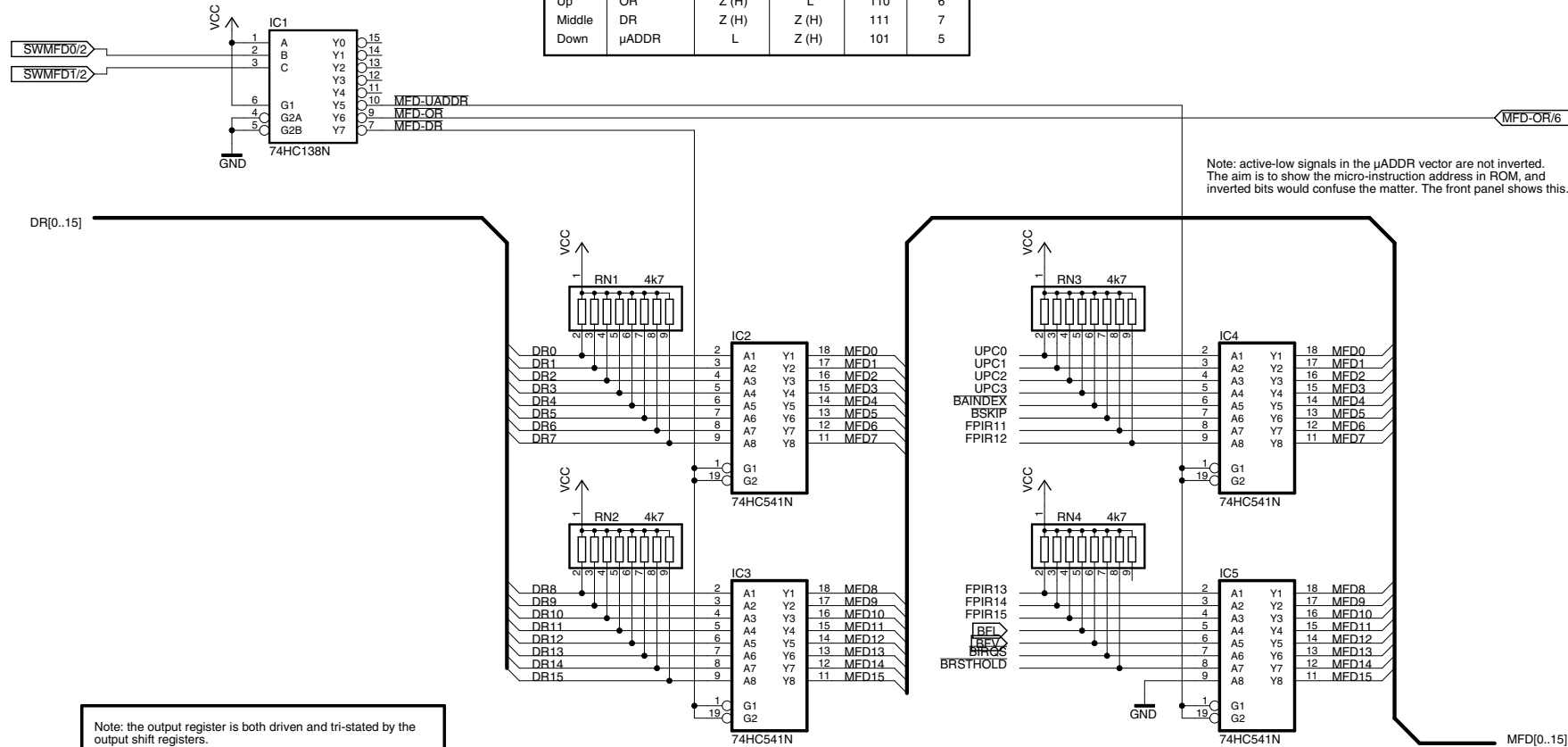


# CFT Mini-Computer

Front Panel: Multi-Function Display

Switch	MFD Shows	SWMFD0	SWMFD1	Vector	Output
Up	OR	Z (H)	L	110	6
Middle	DR	Z (H)	Z (H)	111	7
Down	$\mu$ ADDR	L	Z (H)	101	5

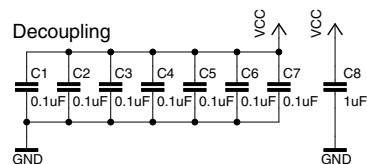


Note: the output register is both driven and tri-stated by the output shift registers.

Output Register

Data Register (DR)

$\mu$ ADDR Vector



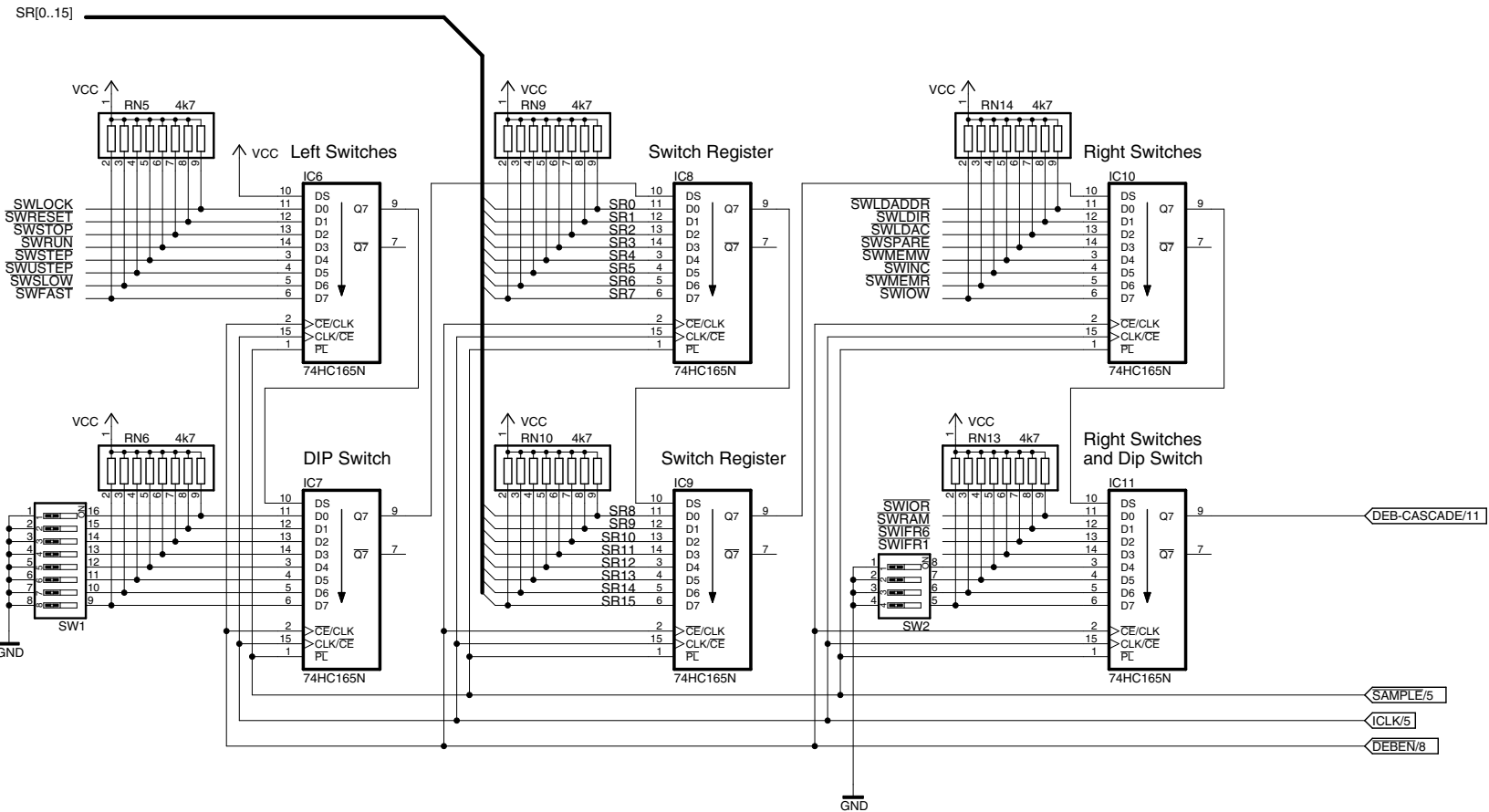
TODO: XXXXXXXXXX  
\* DRC

U

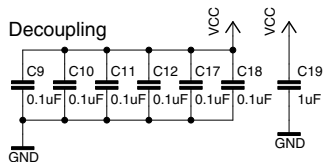
Title: front-panel-revD-DEB-board1  
Revision: Rev C  
Last Change: 29 Nov 2013 13:41:25  
Drawn by: Alexios 3/11  
Simulation filename: N/A  
More Info: <http://www.bedroomlan.org/cft>

# CFT Mini-Computer

Input Shift Registers, switches and computer buses



Decoupling



U

Title: front-panel-revD-DEB-board1

Revision: Rev A

Last Change: 29 Nov 2013 13:41:25

Drawn by: Alexios

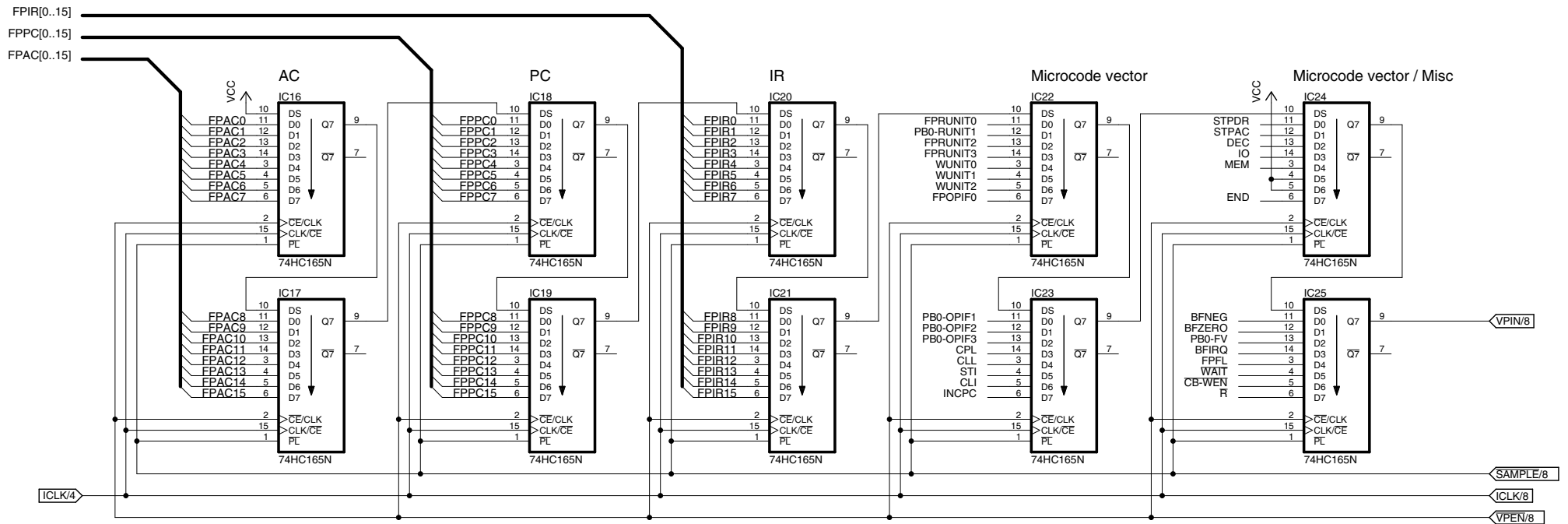
4/11

Simulation filename: To be coded

More Info: <http://www.bedroomlan.org/cft>

# CFT Mini-Computer

Input shift registers, processor state

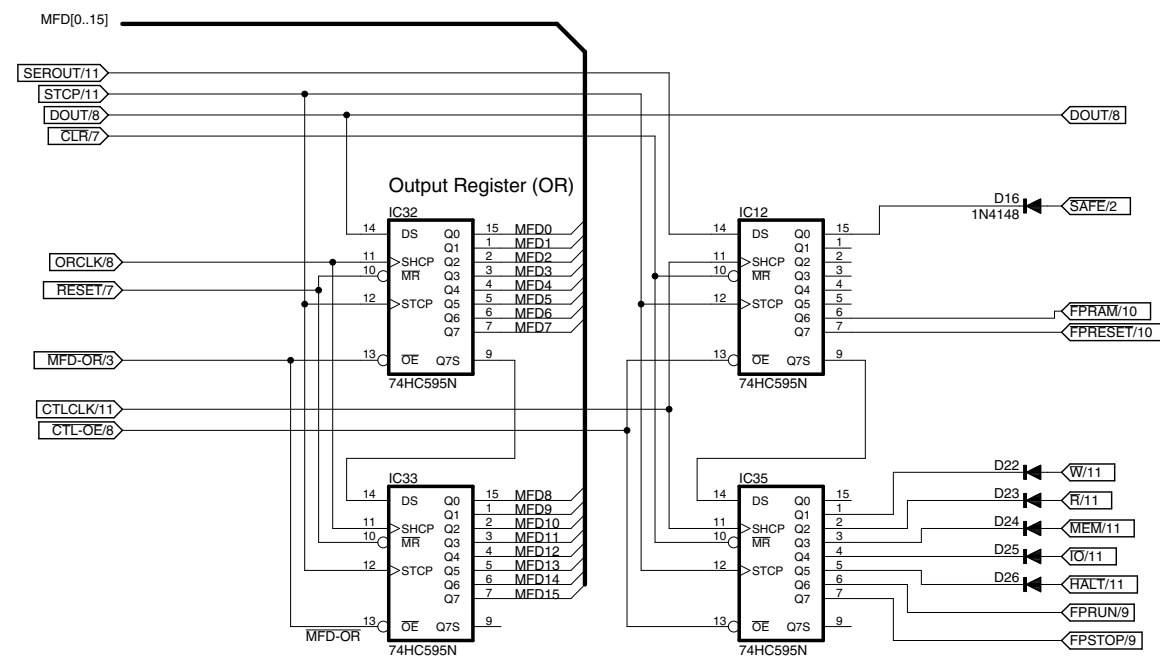


U

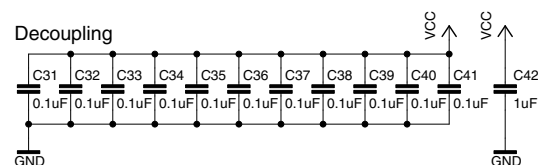
Title:	front-panel-revD-DEB-board1
Revision:	Rev A
Last Change:	29 Nov 2013 13:41:25
Drawn by:	Alexios
Simulation filename:	To be coded
More Info:	<a href="http://www.bedroomlan.org/cft">http://www.bedroomlan.org/cft</a>

# CFT Mini-Computer

Output shift registers



The OR supplies signals to the MFD bus directly.  
It displays on the front panel Multi Function Display (MFD)  
When the MFD switch is in the OR position (i.e. MFD-OR is low)  
It's also unaffected by CLR strobes, resetting to zero when  
the computer itself resets (RESET asserted).

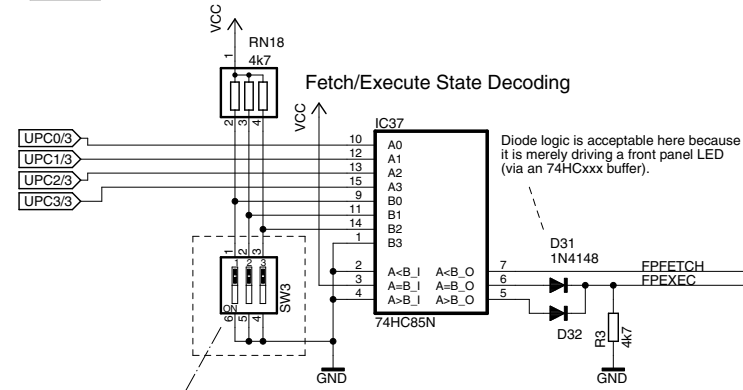
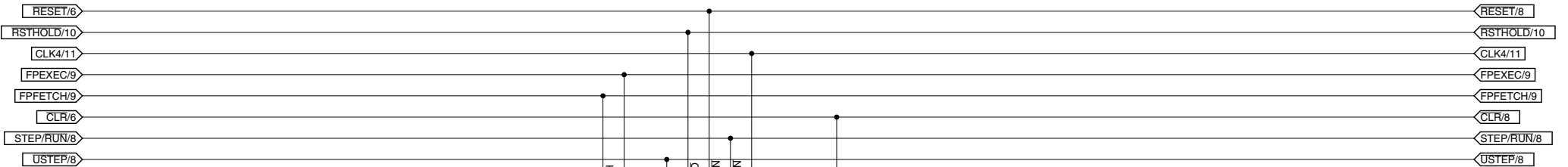


U

Title: front-panel-revD-DEB-board1
Revision: Rev A
Last Change: 29 Nov 2013 13:41:25
Drawn by: Alexios 6/11
Simulation filename: To be coded
More Info: <a href="http://www.bedroomlan.org/cft">http://www.bedroomlan.org/cft</a>

# CFT Mini-Computer

Front Panel: Fetch/Execute Decoding, Synchronous Stopping



Set jumpers/switches for first uPC address of Execute cycle.  
For Microcode v1-v3, this is 3. For Microcode v4+, it's 2.

State/Function Table

RESET	STEP/RUN	USTEP	FPCLKEN-IN	FPUSTEP-IN	State	Function	Clock
0	X	X	X	X	Resetting	Reset started	Full speed
\	X	X	X	X	Resetting	Reset hold	Full speed
1	0	X	1	X	Running	Normal operation	Full speed
1	0	X	0	X	Strobing	Running	Slow (FPUSTEP-IN)
1	/	X	1	X	Stepping	Step Initiated	Full speed
1	/	X	0	X	Stepping	Step Initiated	Slow (FPUSTEP-IN)
1	1	/	1	X	µStepping	µStep Initiated	Full speed
1	1	/	0	X	Strobing	µStep Initiated	Slow (FPUSTEP-IN)
1	1	1	1	X	Stopping	Stopping/Stopped	N/A
1	1	1	0	X	Strobing	Stopping/Stopped	N/A
1	1	1	0	0	Stopped	Stopped	N/A

Stopping  
Starting/Stepping

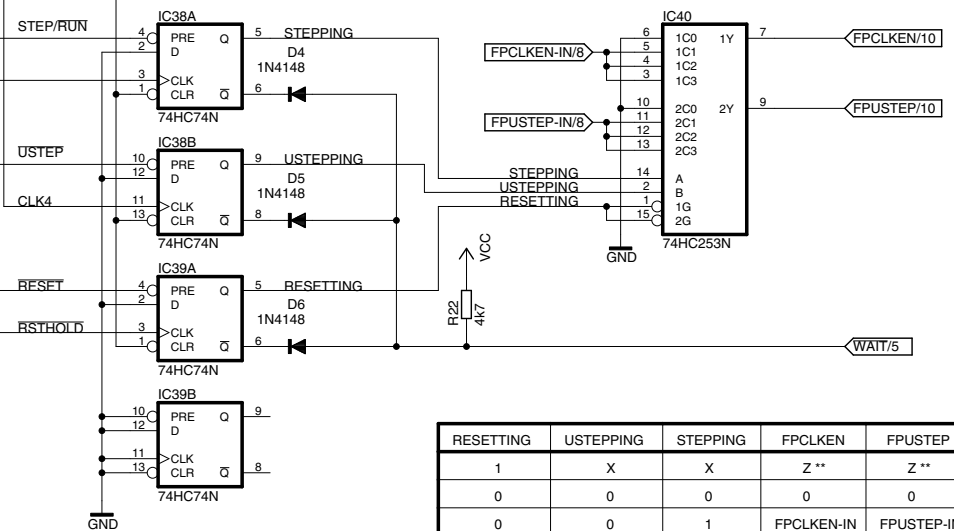
This is faster and more accurate than using the MCU to control stepping.

The STEP flip flop stops the computer at the beginning of the next fetch cycle.  
The µSTEP flip flop stops the computer on the rising edge of the next CLK4 (start of clock cycle).

The RESET-RUN flip flop tri-states the FPCLKEN signal from the start of RESET to the end of RSTHOLD.  
The tri-stated FPCLKEN is pulled up (on the PB1), enabling the full-speed clock which is needed for the RSTHOLD counter.

## Clock-synchronous Stopping

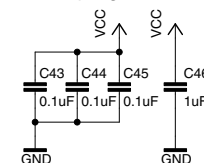
## Clock Enable Multiplexer



RESETTING	USTEPPING	STEPPING	FPCLKEN	FPUSTEP
1	X	X	Z **	Z **
0	0	0	0	0
0	0	1	FPCLKEN-IN	FPUSTEP-IN
0	1	0	FPCLKEN-IN	FPUSTEP-IN
0	1	1	FPCLKEN-IN	FPUSTEP-IN

\*\* PB0 board pulls up FPCLKEN, enabling the clock when the output is in the high impedance state.

## Decoupling



U

Title: front-panel-revD-DEB-board1

Revision: Rev A

Last Change: 29 Nov 2013 13:41:25

Drawn by: Alexios

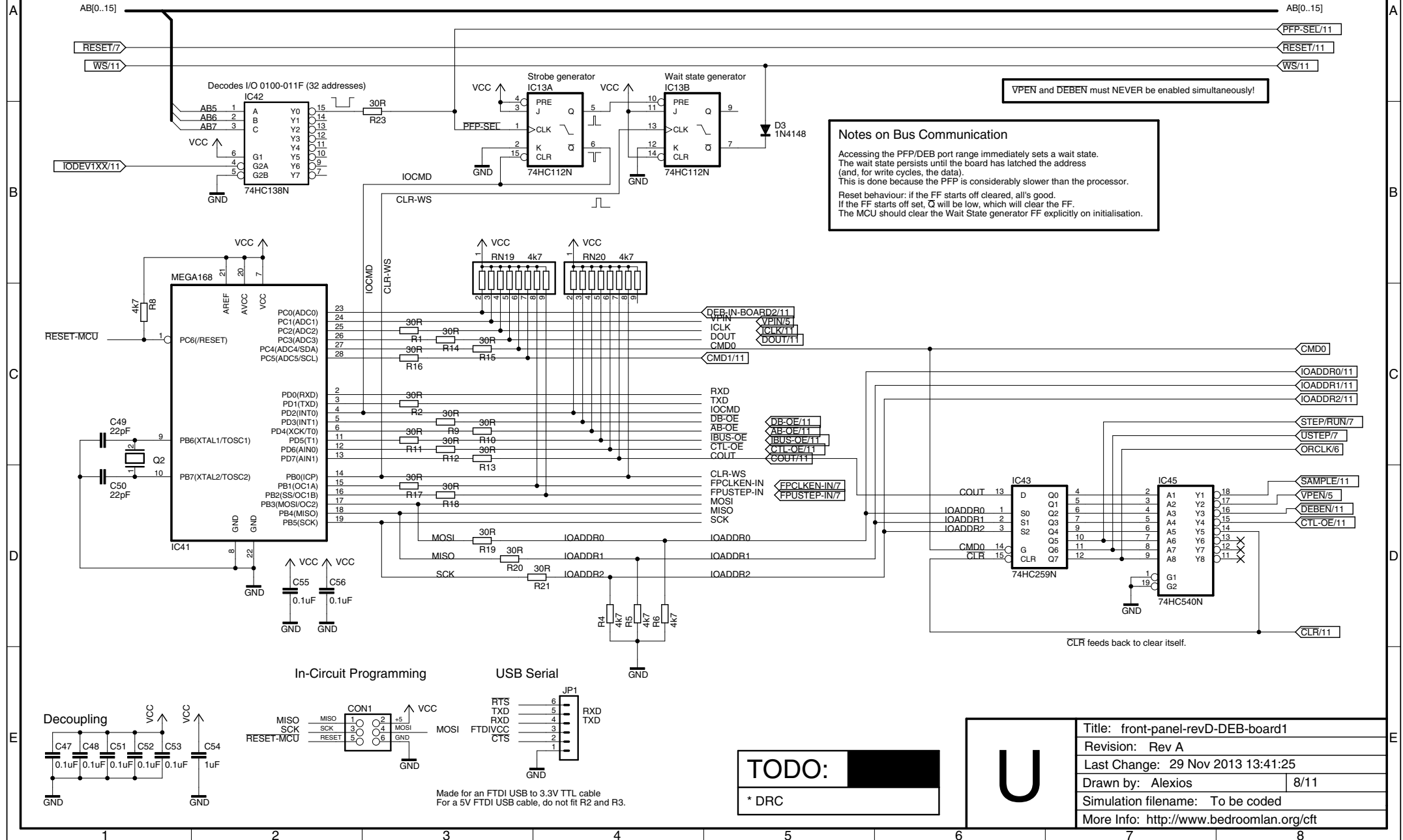
7/11

Simulation filename: To be coded

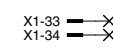
More Info: <http://www.bedroomlan.org/cft>

# CFT Mini-Computer

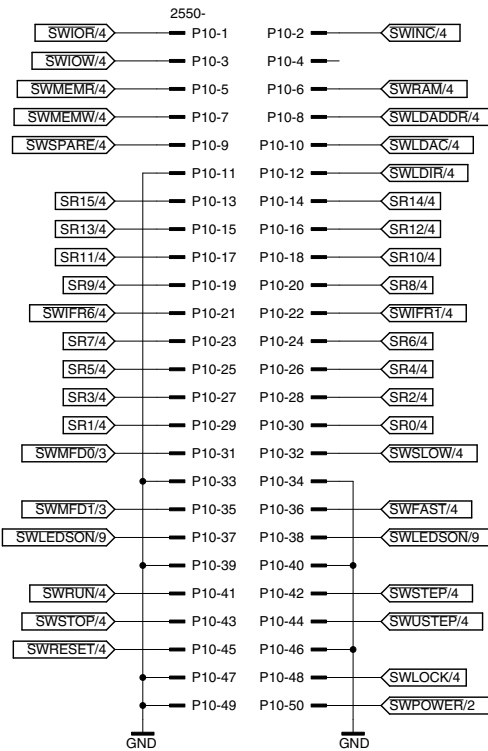
Front Panel: System Device



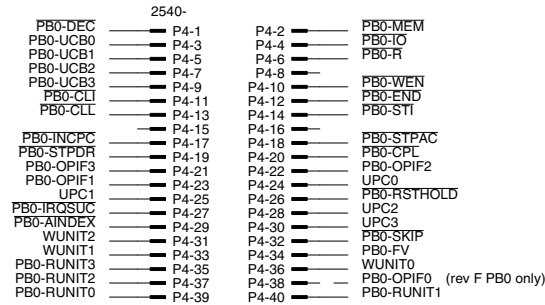
## Front Panel Light Connections



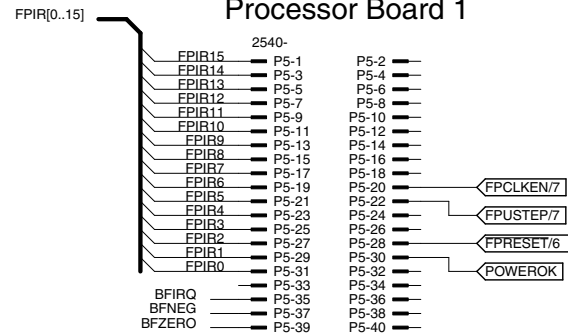
## Switch Assembly



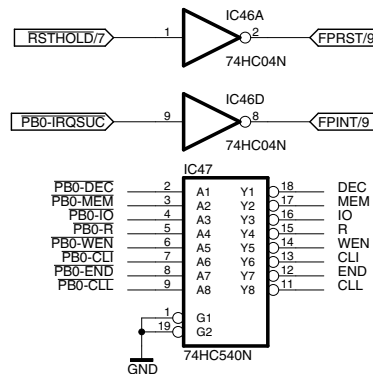
## Processor Board 0



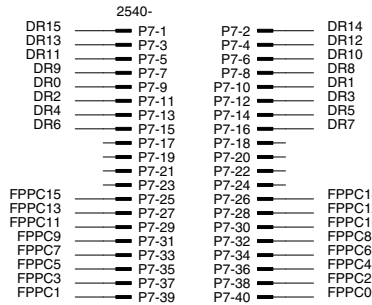
## Processor Board 1



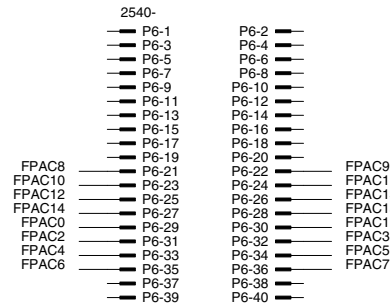
## Signal Inversion



## Processor Board 2



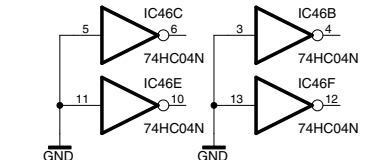
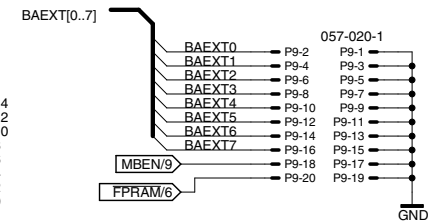
## Processor Board 2



## CFT Mini-Computer

Connectors

## Processor Board 3 (MBU)

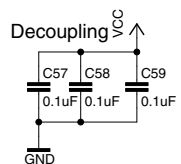
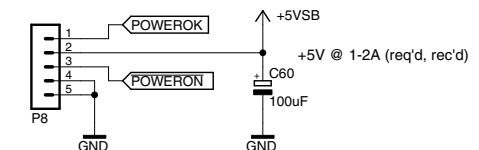


Microcode Address signals are NOT inverted.

PB0-IRQSUC	=	BIQRS
PB0-SKIP	=	BSKIP
PB0-RSTHOLD	=	BRSTHOLD
PB0-AINDEX	=	BAINDEX

## Power Supply

From power supply loom



T

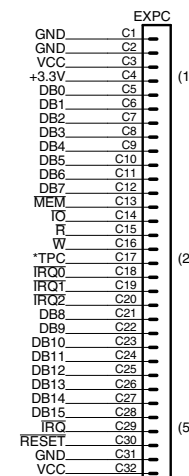
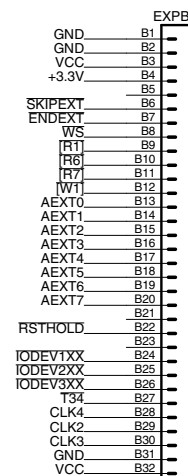
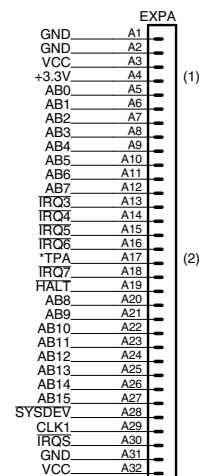
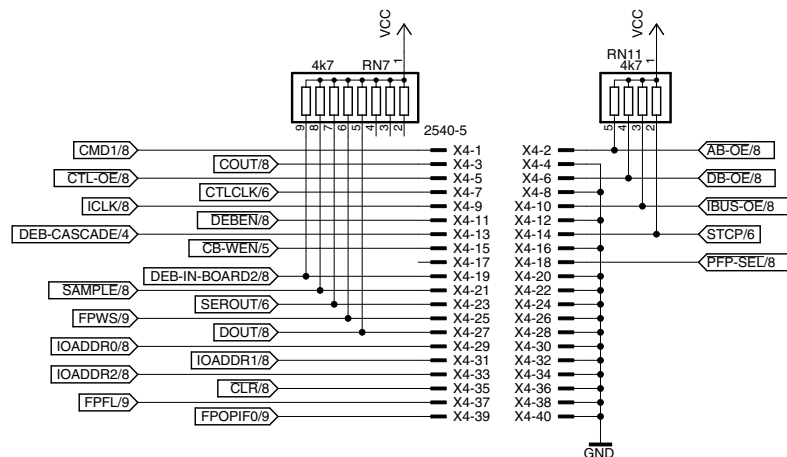
Title: front-panel-revD-DEB-board1
Revision: Rev C
Last Change: 29 Nov 2013 13:41:25
Drawn by: Alexios 10/11
Simulation filename: N/A
More Info: <a href="http://www.bedroomlan.org/cft">http://www.bedroomlan.org/cft</a>



# CFT Mini-Computer

Bus Connectors

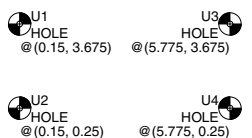
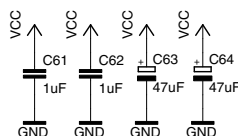
## Expansion Bus (computer bus)



PCB @ (0, 1.95)

### Notes

- (1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it. It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.
- (2) Pins \*TPA and \*TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.
- (3) Reserved for future expansion
- (4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.
- (5) IRQ is provided for systems which lack an interrupt controller (IRQ0-7)



[PCB Logo]

[QR Code <http://www.bedroomlan.org/cft> (shortened)]



J

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Drawn by: Alexios
Simulation filename: N/A
More Info: <a href="http://www.bedroomlan.org/cft">http://www.bedroomlan.org/cft</a>