CFT CPU

Front Panel System Device

FPWADDR
FPWAC
FPWIR
FPWMEM
FPWIO

IC2A 74HC21D

IC2B 74HC21D

Read from switch register

R
W
AB0
AB1
AB2

VCC

IC3 74HC138D

I/O Read 0008

I/O Read 0009 (dip switches)

IC1 74HC688DW

IO
AB3
AB4
AB5
AB6
AB7
SYSDEV
GND

P=Q

Decodes I/O 0008-000F

IC4 74HC138D

I/O Write 0008

Write to Output register (lights)

TP4

I/O Write 000F (HALT instruction)

HALTINSTR

To Run/Stop state machine

Note: since this is an I/O device, the DBUS should have been used instead, but since IBUS and DBUS are connected for memory and I/O R/W cycles, this has the same effect and arguably simplifies board routing.
This is, of course, only possible for boards connected directly to the processor, which the front panel board is.

RN1 2k2
RN2 2k2
RN3 2k2
RN4 2k2

Bit 0
Bit 7
Bit 8
Bit 15

SW1
SW2

IBUS[0..15]

IC5 IC6 74HC541DW

IC7 IC8 74HCT574D

IC9 IC10 74HC541DW

CON1-1 … CON1-8
CON2-1 … CON2-8
CON3-1 … CON3-8
CON4-1 … CON4-8

TP1
TP2
TP3

Dip Switch Register (optional)

Switch Register

Output Register

100nF C1
100nF C2
100nF C3
100nF C4
100nF C5
100nF C6
100nF C7
100nF C8
100nF C9
100nF C10
1uF C11

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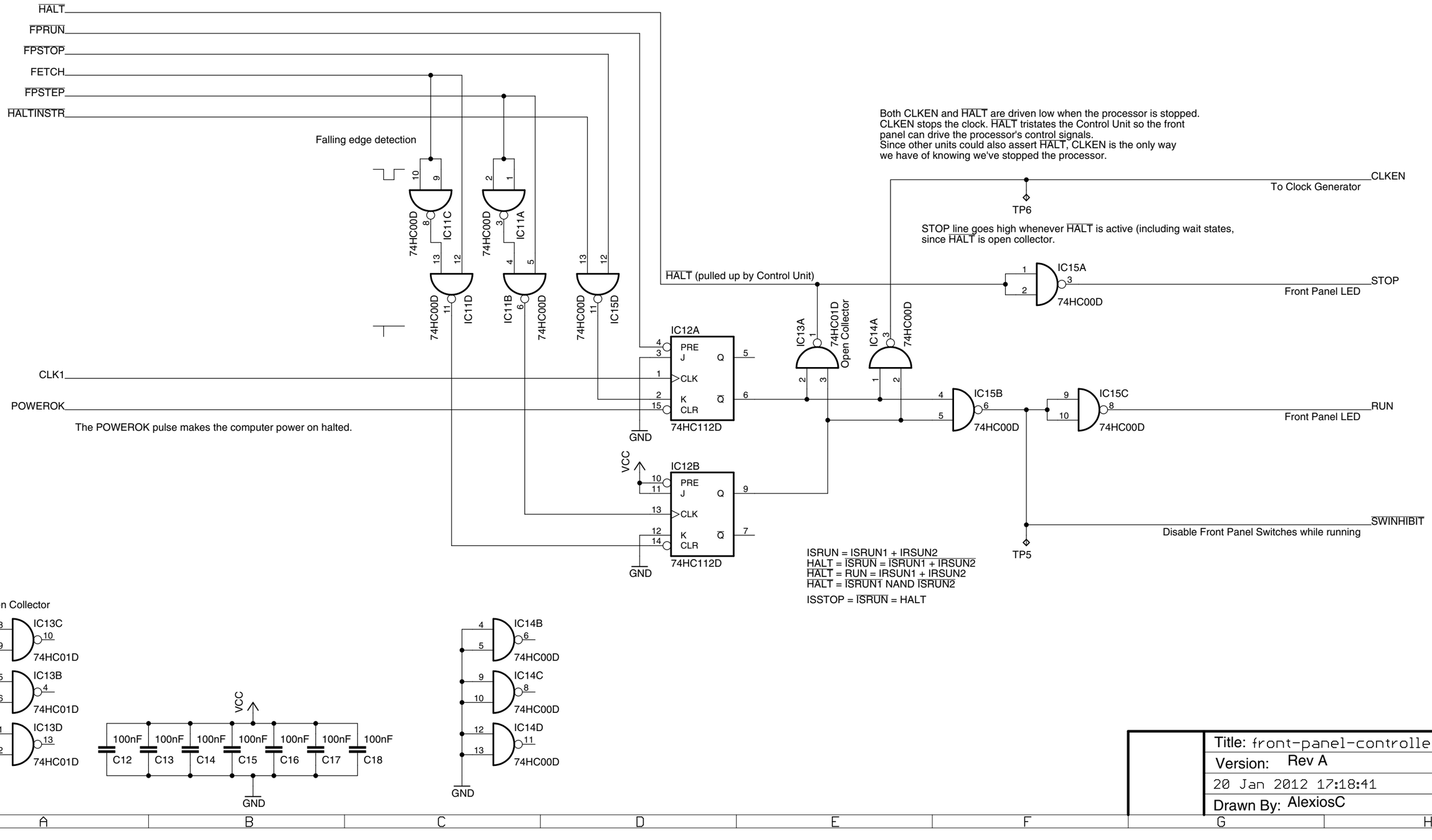
CFT CPU

Run/Stop State Machine



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CFT CPU

Front Panel Sequencer

The '125 buffers act as purposefully slow open collector buffers. When the FP input is high, the buffer is tri-stated. When it is low, the buffer drives, but only low (inputs connected to GND). In addition, the tPZL delay (typical 15ns) acts as a delay circuit that gives time for the switch register enables to be decoded and the switch register value put on the IBUS.

FPINCADDR
FPRMEM
FPRIO
FPWADDR
FPWAC
FPWIR
FPWMEM
FPWIO
RUN

Sequencer: MCSTART, MC0, MC1, MC2, MC3

Write Cycle: MCSTART, WAR, RPC, MEM / IO, INCPC, RAC, W

Read Cycle: MCSTART, WAR, RPC, MEM / IO, INCPC, R, WAC

74HC21D, IC16A, 74HC08D, IC19B, IC19A, IC19D, IC19C

VCC, R5 2k2, IC22B, 74HC125D, MCSTART

FPIO, FPMEM, FPR, FPW

IC22A, IC22C, IC22D, IC23A — 74HC125D

WPC, WDR, WAC, WIR

GND

These ICs receive input from the 74LS123 chips and must be TTL compatible.

IC20A, IC21A, IC20D, IC21D, IC20B, IC21B, IC21C, IC20C — 74HCT32D

IC24 — 74HCT541DW

MEM, IO, R, W, INCPC, RPC, WAR, RAC

IC23B — 74HC125D

WAC

As long as the processor is halted and the control unit tri-stated, the front panel controller will not introduce contention. Also, contention between the FPWAC signal and cycle sequencer cannot happen because even if multiple switches are operated simultaneously, WAC is either tri-stated or driven low.

IC23C, IC23D — 74HC125D; 74HC21D, IC16B; GND

100nF C19, C20, C21, C22, C23, C24, C25; VCC; GND

VCC

IC17A, IC17B, IC18A, IC18B — 74LS123D

R1 1k, C26 100nF, TW = ~20-45us
R2 4k7, C27 100nF, TW = ~94-211us
R3 4k7, C28 100nF, TW = ~94-211us
R4 1k, C29 100nF, TW = ~20-45us

TP7 MC0, TP8 MC1, TP9 MC2, TP10 MC3

GND

TW = 0.25 x R KOhms x C pF (1 + 0.7/R kOhms)

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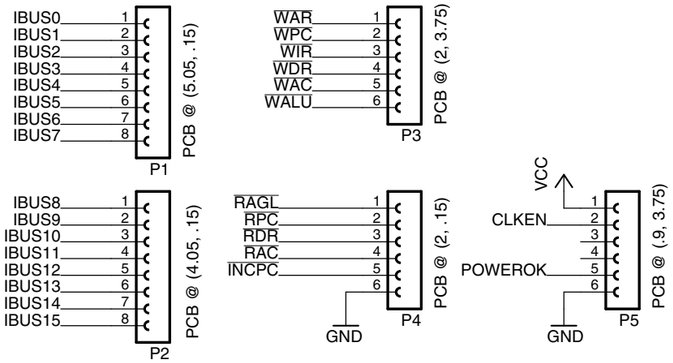
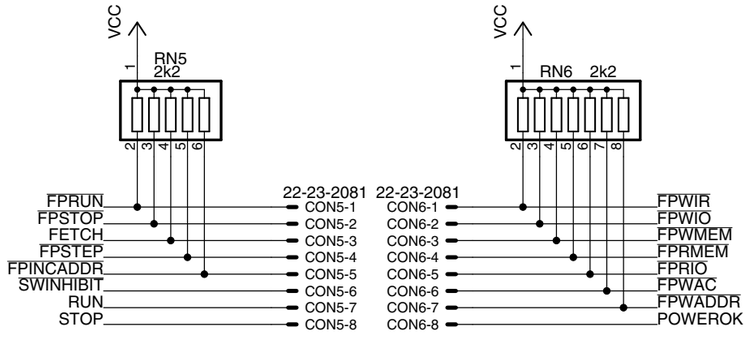
CFT CPU

Signal allocation to the Control and Expansion buses.

Control Bus Connectors

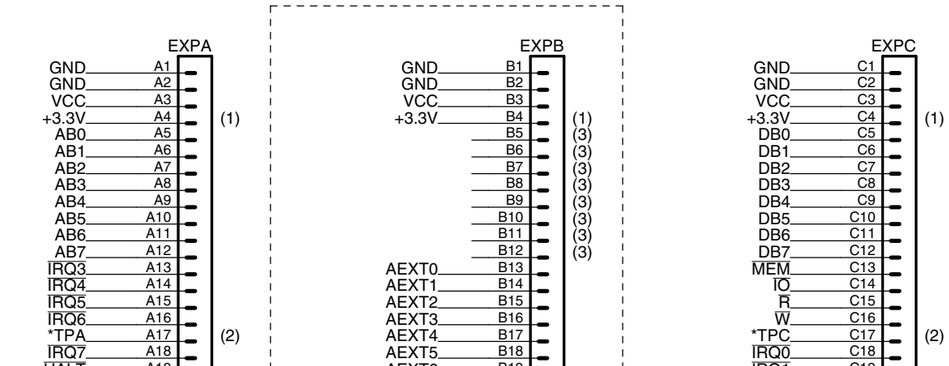


Front Panel Connector



Connector to Front Panel Controller Card.

Expansion Bus (computer bus)



Notes

(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it.
It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) Bit18 of the microinstruction field. Currently unused, reserved for future expansion.

H1 HOLE @ (.175, 3.675)
H2 HOLE @ (5.8, 3.675)
H3 HOLE @ (5.8, .225)
H4 HOLE @ (.175, .225)

This sheet shows the wiring and default parts of most CPU boards. Since these 10x16cm boards only have a single Eurocard connector, A board is either a CPU component or a computer component and must be fitted with ONE of the two connectors. Delete the other one.

[PCB Logo]

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