CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

- OD This input signal is open drain.
- TTL This input signal may be at TTL logic levels.
- Z This input may be at High Impedance.
- Z* This input (local to this board) may be at High Impedance.

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Note: the shading patterns below are in colour, and not distinguishable on black & white hard copies.

Circuits in need of improvement are marked like this.

Circuits known to be incorrect are marked like this.

Obsolete sections or circuits are marked like this.

Changes from previous revision are marked like this.

D	Title: front-panel-revD-DEB-board2
	Revision: Rev C
	Last Change: 12 Jun 2016 11:43:07
	Drawn by: Alexios 1/5
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Input Shift Registers, switches and computer buses

AB[0..15]

DB[0..15]

DEB-CASCADE/4

DBUS

ABUS

IC12

IC13

IC14

IC15

74HC165N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7

AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15

DS D0 D1 D2 D3 D4 D5 D6 D7 Q7 $\overline{Q7}$ $\overline{CE}$/CLK CLK/$\overline{CE}$ $\overline{PL}$

DEB-OUT/4

SAMPLE/4

ICLK/4

DEBEN/4

Decoupling

VCC

C9 0.1uF C10 0.1uF C11 0.1uF C18 0.1uF C19 1uF

GND

Switchable Pull-Up Resistors

BUSPU goes HIGH on initial start up, pulling the bus high.

If bus hold is detected, the PFP tristates BUSPU.

BUSPU/3

RN7 RN8 RN11 RN12 RN2 RN5 RN4 4k7

DB[0..15]

AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5 AEXT6 AEXT7

$\overline{MEM}$ IO $\overline{R}$ $\overline{W}$ $\overline{WS}$ $\overline{HALT}$ CLK4

$\overline{RSTHOLD}$ IODEV1XX IODEV2XX IODEV3XX SYSDEV $\overline{RESET}$

Since CMOS receivers are used on the bus, and there's a resistor in series, the current will be low enough to be drained by a buffer output.

D

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Drawn by: Alexios	2/5
Simulation filename: To be coded	
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CFT Mini-Computer

Output shift registers

IBUS[0..15]
AB[0..15]
DB[0..15]

COUT/4
IOADDR0/4
IOADDR1/4
IOADDR2/4
CMD1/4
CLR/4
DOUT/4

IC44 74HC259N: CLR, G, S2, S1, S0, D; Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0

IC3A 74HC125N

BUSPU is either HIGH or Z.
High on initial reset.

BUSPU/2
AB-OE/4
IBUS-OE/4
CTL-OE/4
DB-OE/4
R/2
PFP-SEL/4

DBCLK
STCP
R1 30R
R10 30R
IBUSCLK
ABCLK
ABCLK
AB-OE
IBUSCLK
IBUS-OE
CTLCLK

DBUS
IC26 74HC595N: DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
IC27 74HC595N: DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

ABUS
IC28 74HC595N: AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7
IC29 74HC595N: AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15

IBUS
IC30 74HC595N: IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
IC31 74HC595N: IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15

DB-OE-COMBINED
AB-OE
IBUS-OE

IC1 74HC251N: I0 I1 I2 I3 I4 I5 I6 I7, S0 S1 S2 OE, Y, $\overline{Y}$

Optional
IC2 74HC595N: AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5 AEXT6 AEXT7

STCP/4
VCC
RN15 4k7

Control
IC34 74HC595N

D1 D4 D17 D18 D2 D3 D19 D20
30R: R3 R2 R4 R5 R6 R7 R8 R9
IRQ1/5
CB-INCPC/5
CB-WAC/5
CB-RPC/5
CB-WAR/5
CB-WIR/5
CB-WPC/5

JP1: IRQ6/5, IRQ/5
R11 30R
SEROUT/4
CTLCLK/4

74HC04N IC46D

Decoupling
C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 0.1uF
C42 1uF
VCC
GND

D	S0 PFP-SEL	S1 R	S2 DB-OE	DB-OE-COMBINED (notes)
0	0	0	0	0 ($\overline{DBOE}$ asserted by MCU)
1	0	0	1	0 (CFT bus read cycle from DFP)
2	0	1	0	0 ($\overline{DBOE}$ asserted by MCU)
3	0	1	1	1 (DFP selected, but not a read cycle [yet])
4	1	0	0	0 ($\overline{DBOE}$ asserted by MCU)
5	1	0	1	1 (some other bus read cycle, DFP not selected)
6	1	1	0	0 ($\overline{DBOE}$ asserted by MCU)
7	1	1	1	1 (MCU and CFT bus idle, or write cycle)

DB-OE-COMBINED = DB-OE + (PFP-OE × R) (Negative logic, more intuitive)
$\overline{DB\text{-}OE\text{-}COMBINED} = \overline{DB\text{-}OE} \times (\overline{PFP\text{-}OE} + \overline{R})$ (Positive logic, deMorgan)

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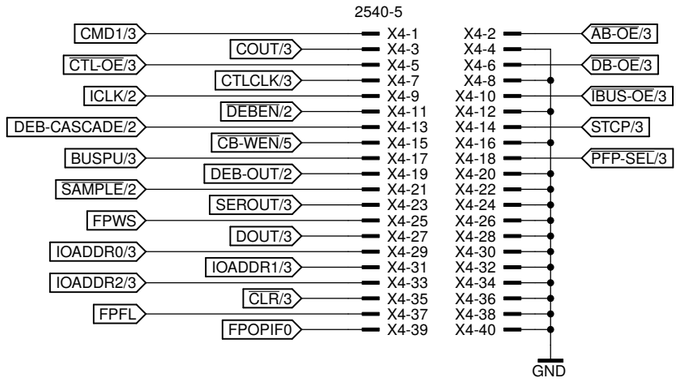
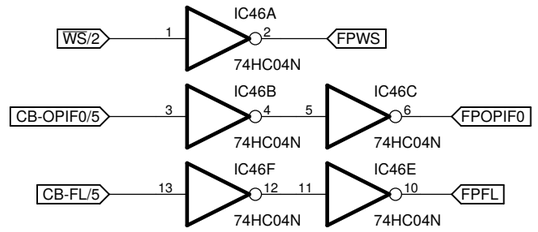
CFT Mini-Computer

Connectors

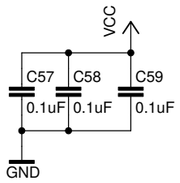
Connector to DFP Board 1



Signal Inversion



Decoupling



D	Title: front-panel-revD-DEB-board2
	Revision: Rev D
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	Simulation filename: N/A
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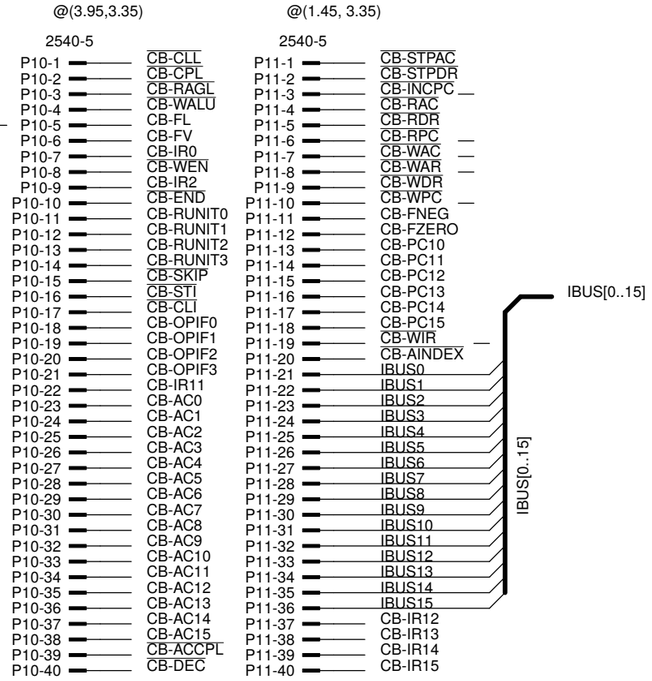
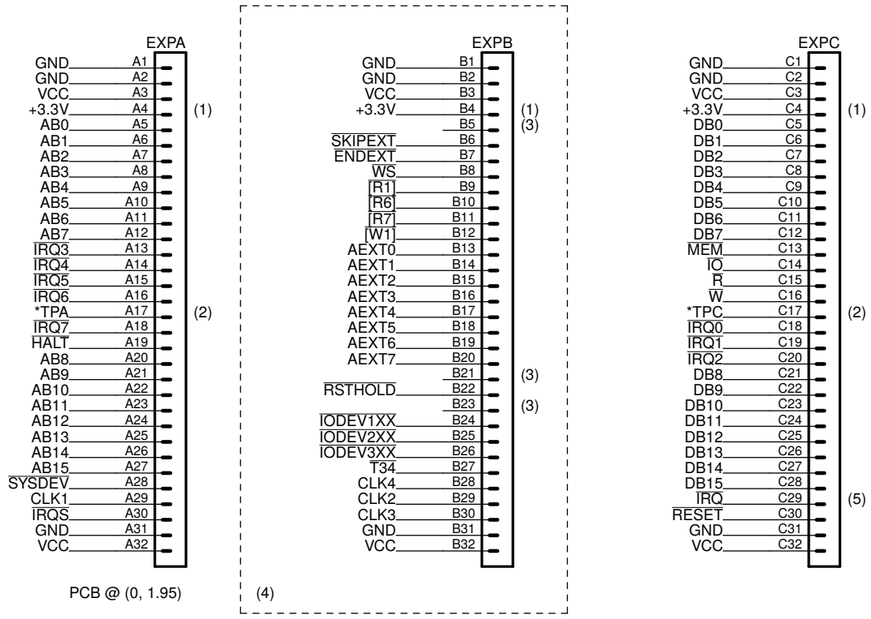
CFT Mini-Computer

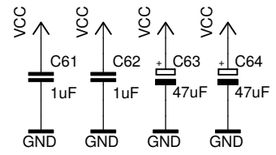
Bus Connectors

Control Bus (processor bus)



Expansion Bus (computer bus)





Notes

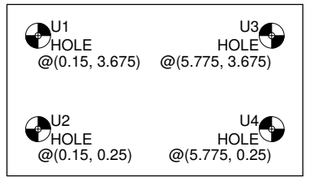
(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it.
It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) IRQ is provided for systems which lack an interrupt controller (IRQ0-7)



[PCB Logo]

[QR Code http://www.bedroomlan.org/cft (shortened)]

open hardware

J

Title: front-panel-revD-DEB-board2	
Revision: Rev J	
Last Change: 12 Jun 2016 11:43:07	
Drawn by: Alexios	5/5
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	