Micro-Instruction Control Vector

END W R MEM I/O DEC STP AC STP DR INC PC CLI STI CLL CPL IF3 IF2 IF1 IF0 WU2 WU1 WU0 RU3 RU2 RU1 RU0

Interrupt Requests

7 6 5 4 3 2 1 0

Memory Bank Unit

AEXT7 ROM AEXT6 AEXT5 AEXT4 AEXT3 AEXT2 AEXT1 AEXT0

Program Counter

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Enabled Interrupts

7 6 5 4 3 2 1 0

Flags

MBEN N Z V I L

Accumulator

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

7 6 5 4 3 2 1 0

State

RESET RUN STOP WS FETCH EXEC INT

Output Register/Data Register/Micro-address vector

$\overline{\text{RST}}$ $\overline{\text{INT}}$ V L OP3 OP2 OP1 OP0 I $\overline{\text{SKIP}}$ $\overline{\text{AIDX}}$ µPC3 µPC2 µPC1 µPC0

7 6 5 4 3 2 1 0

Microcode Bank

µCB3 µCB2 µCB1 µCB0

Instruction Register

OP3 OP2 OP1 OP0 I R 9 8 7 6 5 4 3 2 1 0

RESET RUN µSTEP FAST LTS ON OR

SLOW DR

Switch Register

SR→IR MEM W MEM R I/O W I/O R RAM BNK IFR1

START STOP STEP CREEP OFF µADDR VEC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8000	4000	2000	1000	800	400	200	100	80	40	20	10	8	4	2	1
100000	40000	20000	10000	4000	2000	1000	400	200	100	40	20	10	4	2	1
LIA/JMPII	ISZ	OP2/POP	OP1	XOR	OR	AND	ADD	JSR	JMP	OUT	IN	STORE	LOAD	IOT	TRAP

SR→PC SR→AC W NEXT R NEXT W NEXT R NEXT ROM BNK IFR6

POWER

PANEL LOCK

16 BIT SOLID STATE MINI COMPUTER