CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

OD This input signal is open drain.
TTL This input signal may be at TTL logic levels.
Z This input may be at High Impedance.
Z This input (local to this board) may be at High Impedance.

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Circuits in need of improvement are marked like this.

Obsolete sections or circuits are marked like this.

Circuits known to be incorrect are marked like this.

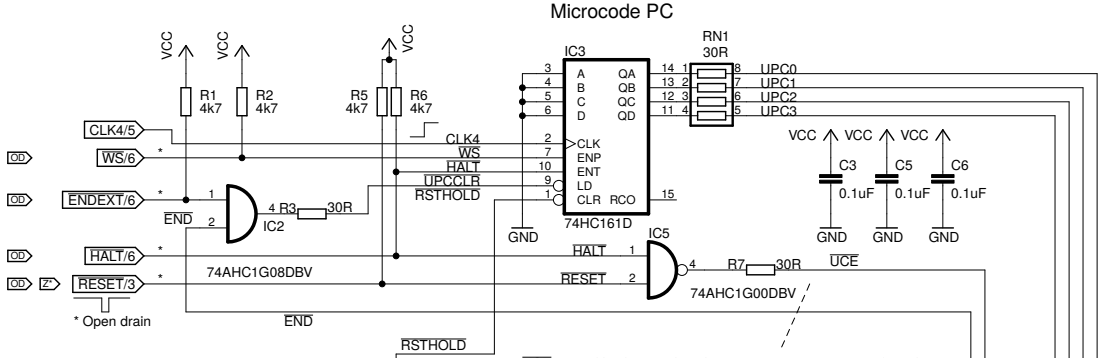
D

Title: CFT-PB0-revE-TSSOP	
Revision: Rev B	
Last Change: 5 Sep 2014 13:47:07	
Drawn by: Alexios	1/6
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Microcode Store and Sequencer

Microcode PC



UCE is used by the unit decoders to ensure no units are selected when either HALT or RESET are inactive.

Notes

32k x 8 (2x256) ICs required for Microcode v4.
512k x 8 ICs are cheaper and easier to come by, though, so this schematic uses these. Smaller ICs can be substituted.

ROMS to be socketed for easy reprogramming.

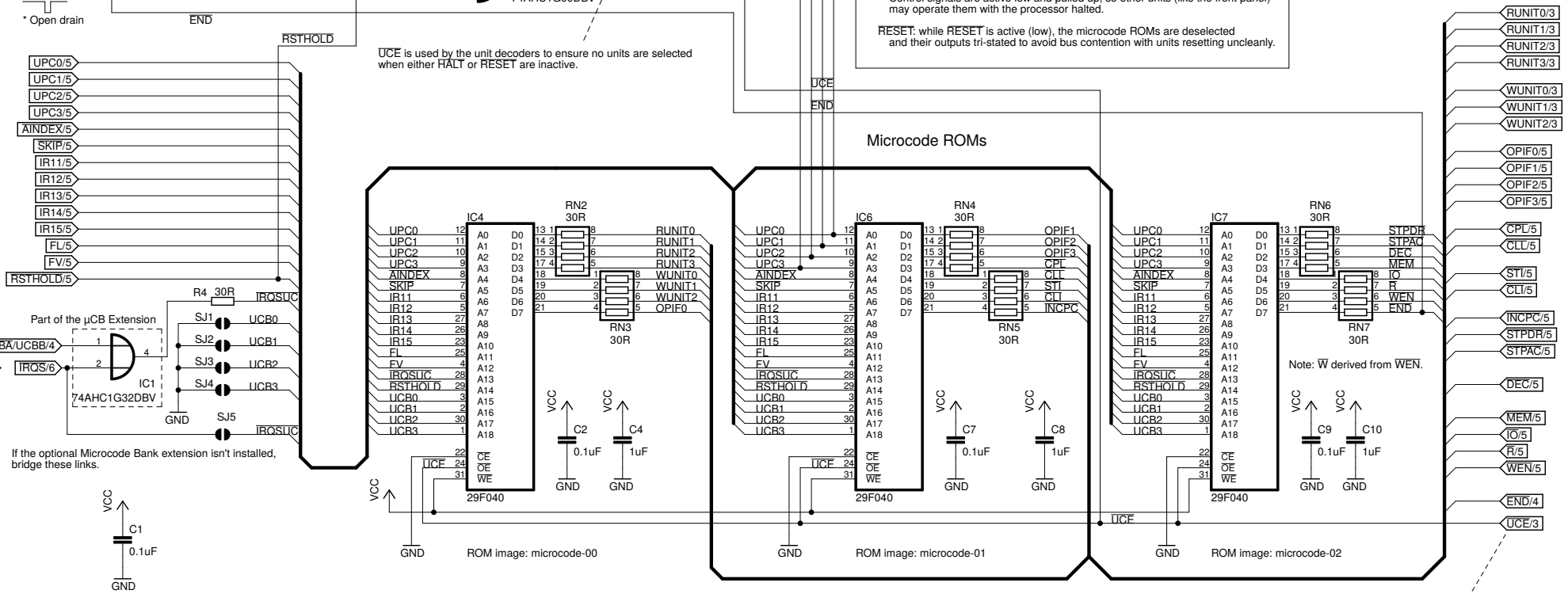
Use 70ns or 50ns chips.

Vertical microcode (unit selectors RUNIT, WUNIT and OPIF) are pulled low because a value of zero selects no unit.

WS: indicates a wait state. Inhibits the uPC counter.
HALT: halts the processor. The control unit's outputs are at High-Z. Consequently, the processor is disconnected from all busses. Control signals are active low and pulled up, so other units (like the front panel) may operate them with the processor halted.

RESET: while RESET is active (low), the microcode ROMs are deselected and their outputs tri-stated to avoid bus contention with units resetting uncleanly.

Microcode ROMs



UCE is used by the unit decoders to ensure no units are selected when either HALT or RESET are inactive.

0.1 uF capacitors are used for decoupling/bypass.

30R resistors are impedance matching resistors and may be replaced with 0R-100R units depending on requirements.

Nota Bene: this sequencer can only run Microcode v.5 and above!

Title:	CFT-PB0-revE-TSSOP
Revision:	Rev F
Last Change:	5 Sep 2014 13:47:07
Drawn by: Alexios	2/6
Simulation filename:	PB0-{UPC,ROM}.v
More Info:	http://www.bedroomlan.org/cft

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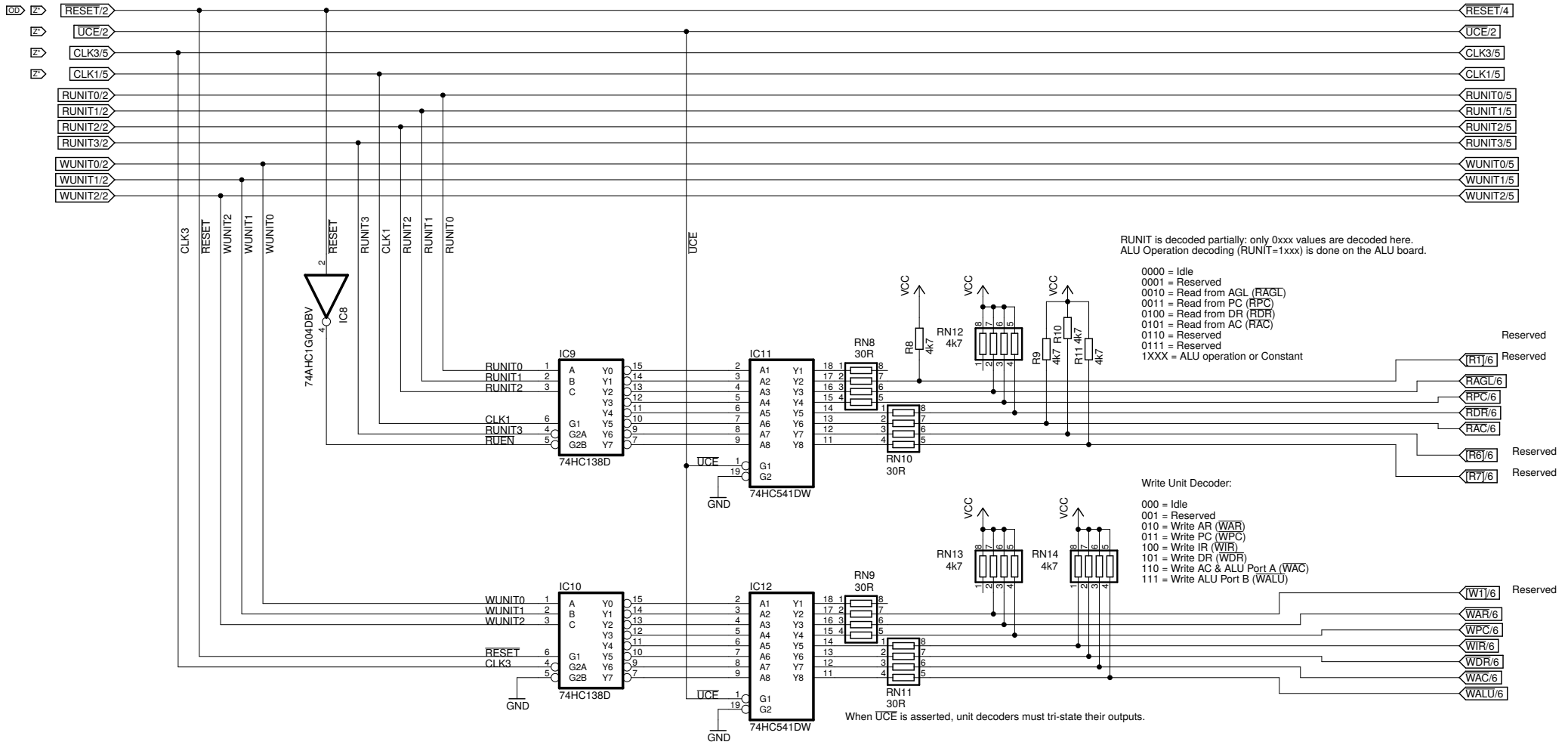
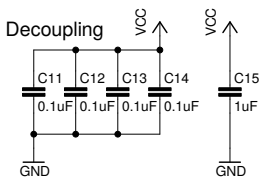
Read & Write Unit Decoding





Title: CFT-PB0-revE-TSSOP	
Revision: Rev F	
Last Change: 5 Sep 2014 13:47:07	
Drawn by: Alexios	3/6
Simulation filename: PB0_decoders.v	
More Info: http://www.bedroomlan.org/cft	

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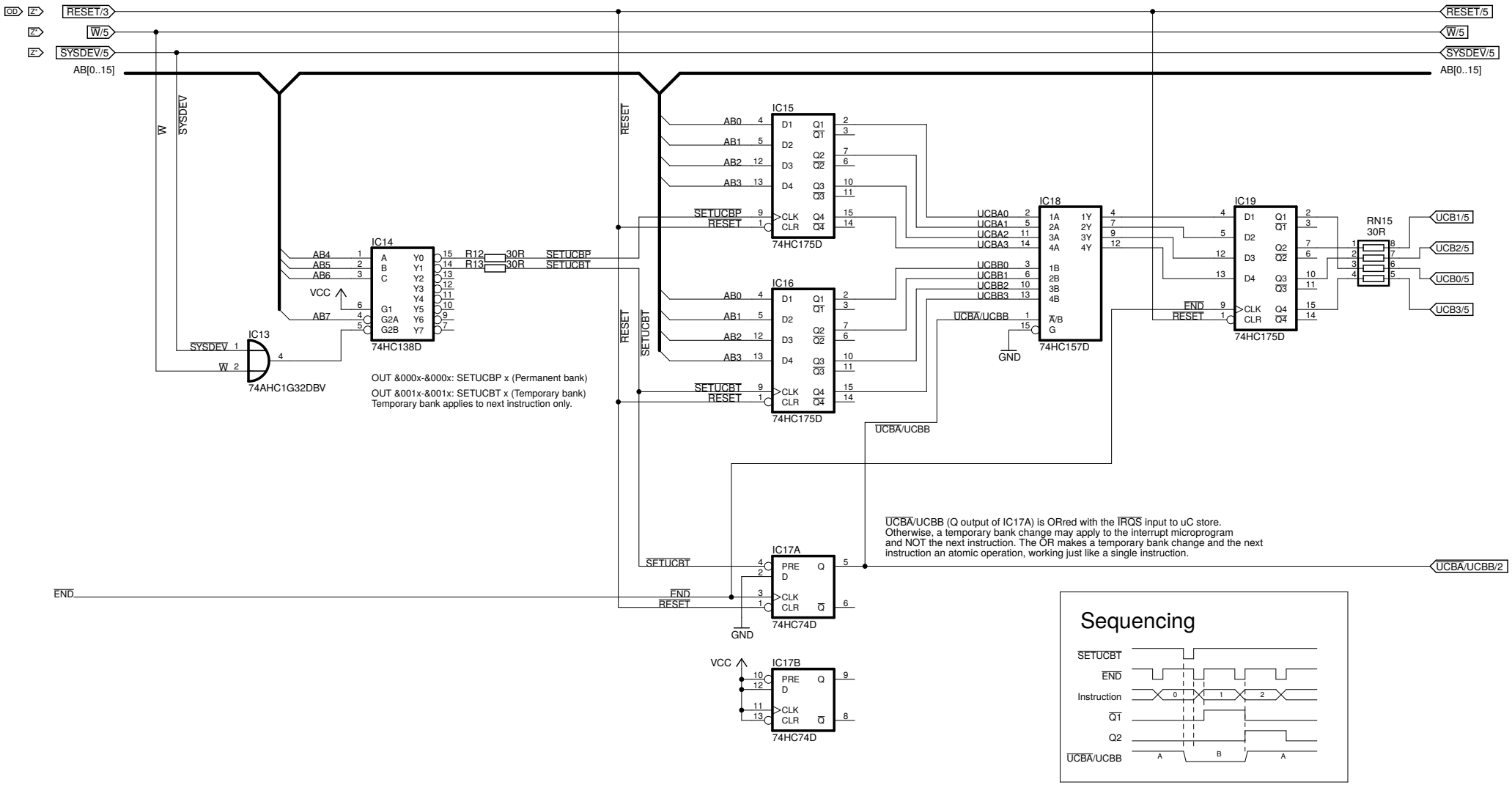
Microcode Banking



Title:	CFT-PB0-revE-TSSOP
Revision:	Rev F
Last Change:	5 Sep 2014 13:47:07
Drawn by: Alexios	4/6
Simulation filename:	PB0-UCB.v
More Info:	http://www.bedroomlan.org/cft

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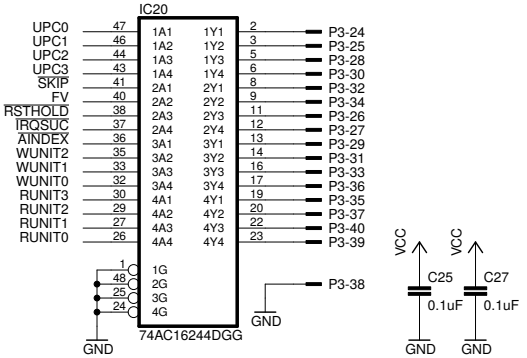
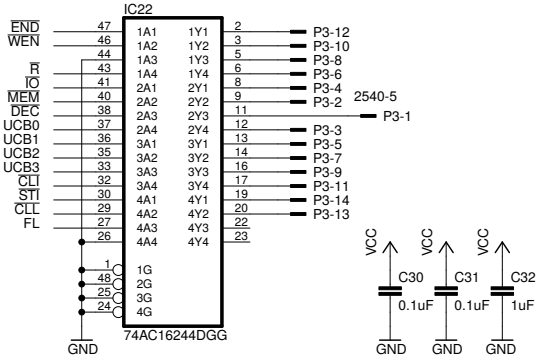
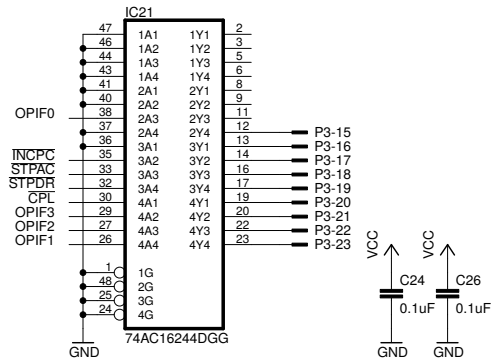
But Termination and Buffering

Front Panel Buffers

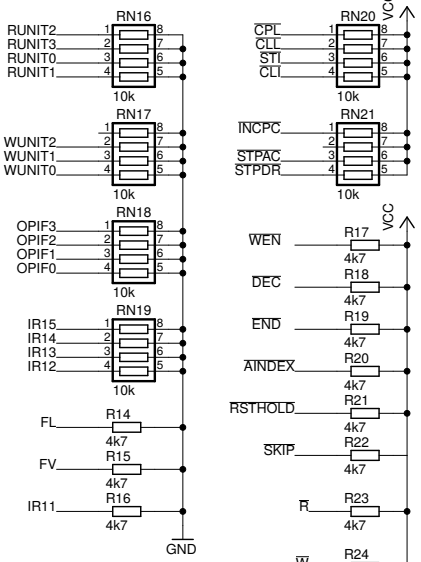




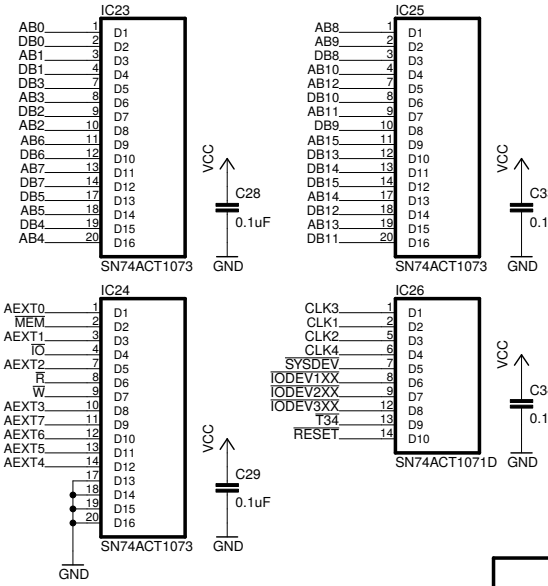


Note: IR10-15 not relayed to front panel. PB1 (where the whole IR lives) does this.

Pull-Ups and Pull-Downs



Bus Termination

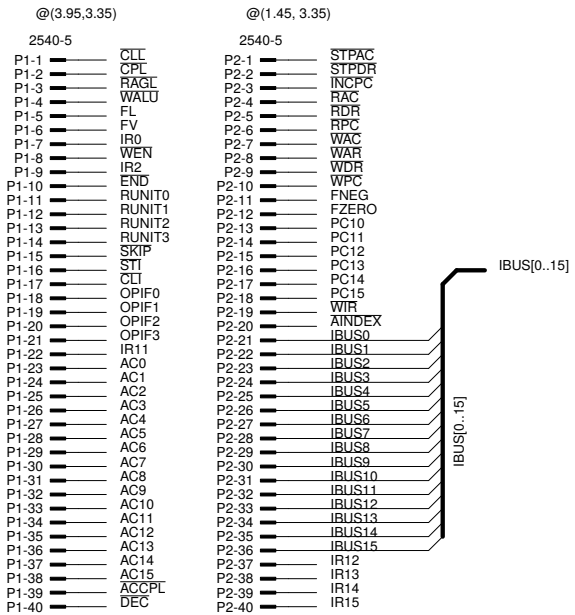


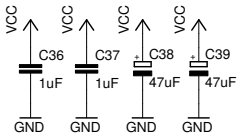
Title: CFT-PB0-revE-TSSOP	
Revision: Rev J	
Last Change: 5 Sep 2014 13:47:07	
Drawn by: Alexios	5/6
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

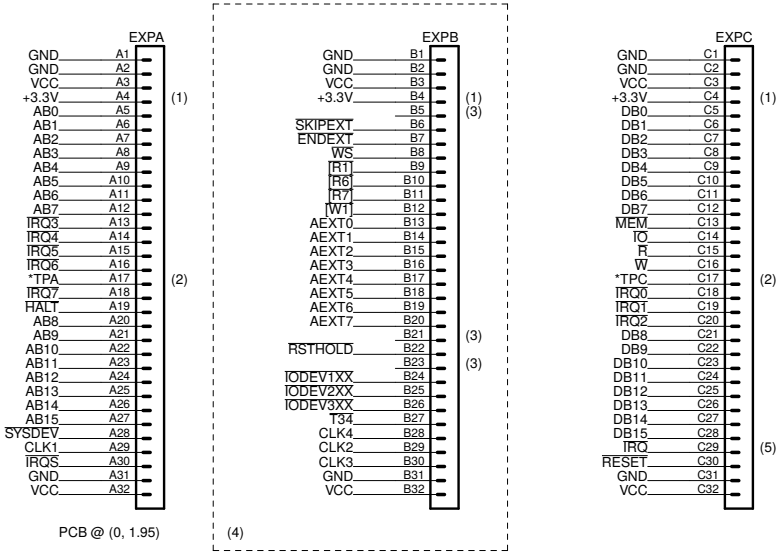
Bus Connectors

Control Bus (processor bus)





Expansion Bus (computer bus)



Notes

(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it. It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) $\overline{IRQ}$ is provided for systems which lack an interrupt controller ($\overline{IRQ0\text{-}7}$)

U1 HOLE @(0.15, 3.675)
U3 HOLE @(5.775, 3.675)
U2 HOLE @(0.15, 0.25)
U4 HOLE @(5.775, 0.25)

[PCB Logo]

[QR Code http://www.bedroomlan.org/cft (shortened)]

open hardware

J

Title: CFT-PB0-revE-TSSOP	
Revision: Rev J	
Last Change: 5 Sep 2014 13:47:07	
Drawn by: Alexios	6/6
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	