CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

NC = New Clock geometry applied

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Circuits in need of improvement are marked like this.

Obsolete sections or circuits are marked like this

Circuits known to be incorrect are marked like this.

NC D	Title: cft
	Revision: Rev B
	Last Change: 28 Aug 2012 13:33:26
	Drawn by: Alexios 1/45
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft