CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

NC = New Clock geometry applied

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Circuits in need of improvement are marked like this.

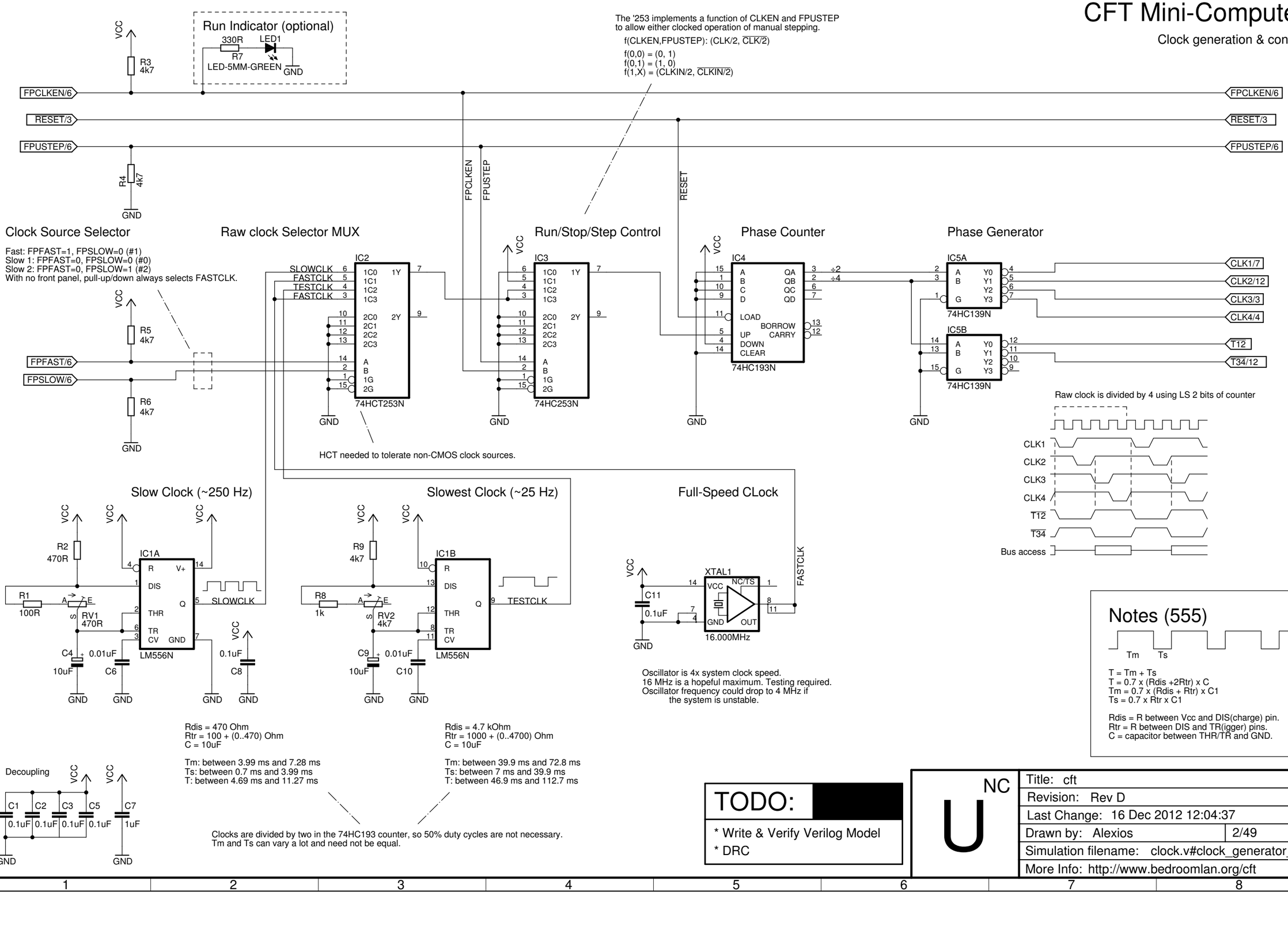
Obsolete sections or circuits are marked like this

Circuits known to be incorrect are marked like this.

NC D	Title: cft
	Revision: Rev B
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios 1/49
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Clock generation & control



TODO:

* Write & Verify Verilog Model
* DRC

Title: cft	
Revision: Rev D	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	2/49
Simulation filename: clock.v#clock_generator_v3	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Reset Handling and Sequencing

On $\overline{\text{RESET}}$, the reset timer drives $\overline{\text{RSTHOLD}}$ down for 255 CLK pulses.
Using a 16 MHz oscillator, this will assert $\overline{\text{RSTHOLD}}$ for 31.875 us.
Using the slow clock (~400 Hz raw), this will pulse for 1.275 seconds.
Finally, with the testing clock (~40 Hz raw), $\overline{\text{RSTHOLD}}$ will last 12.75 seconds.
NB: CLKIN/2 is RAWCLK divided by 2 (obviously).

RESET/2
CLK3/2
RESET/4
RSTHOLD/4
IBUS[0..15]

VCC
R16 4k7

Reset Sources

VCC R12 4k7
VCC R13 4k7
VCC R15 4k7

FPRESET/6 → 74HC14N IC6C (9 → 8)
POWEROK/6 → 74HC14N IC6B (11 → 10)

IC7A (1 → 2) 74HC05N
IC7C (5 → 6) 74HC05N
IC7D (9 → 8) 74HC05N → RESET

LED-5MM-GREEN LED2
330R R11
Power LED
GND

NB: Open Collector gate

NB: Open Drain gates

POWEROK comes from the ATX PSU via the front panel.
The PSU holds POWEROK low at power-up (or during brown-outs), until power stabilises. The computer is expected to reset when POWEROK is low.

Reset Button (optional)

JP1
S1
VCC R10 50k
IC6A (13 → 12) 74HC14N
VCC R14 4k7
C18 0.1uF
GND

If the reset button and debouncing circuit is installed, this resistor may be left out.

Reset timer

CLK3
RESET
VCC R17 4k7
RSTHOLD

IC8 74HC590N
CLK (11), CCKEN (12), CCLR (10), RCK (13), G (14), GND
QA (15), QB (1), QC (2), QD (3), QE (4), QF (5), QG (6), QH (7), RCO (9)

JP2
2ms
4ms
8ms
16ms
32ms

Install exactly ONE jumper.

Reset delay selector. Times shown for 4 MHz processor clock.

System Reset Vector (FFF0)

VCC
GND
RSTHOLD

IC9 74HC541N
A1 (2) A2 (3) A3 (4) A4 (5) A5 (6) A6 (7) A7 (8) A8 (9)
Y1 (18) IBUS0
Y2 (17) IBUS1
Y3 (16) IBUS2
Y4 (15) IBUS3
Y5 (14) IBUS4
Y6 (13) IBUS5
Y7 (12) IBUS6
Y8 (11) IBUS7
G1 (1), G2 (19)

IC10 74HC541N
A1 (2) A2 (3) A3 (4) A4 (5) A5 (6) A6 (7) A7 (8) A8 (9)
Y1 (18) IBUS8
Y2 (17) IBUS9
Y3 (16) IBUS10
Y4 (15) IBUS11
Y5 (14) IBUS12
Y6 (13) IBUS13
Y7 (12) IBUS14
Y8 (11) IBUS15
G1 (1), G2 (19)

IBUS[0..15]

Outputs binary 1111'1111'1111'0000 to the IBUS while $\overline{\text{RSTHOLD}}$ is asserted.
This value is picked up by other units of the processor, including the Program Counter, and becomes the computer's boot address.

Decoupling

VCC
C12 0.1uF, C13 0.1uF, C14 0.1uF, C15 0.1uF, C16 0.1uF, C17 1uF
GND GND

IC7E (11 → 10) 74HC05N
IC7F (13 → 12) 74HC05N
NB: Open Drain gate
GND GND

74HC05N IC7B (4 → 3)
IC6D (2 → 1) 74HC14N
IC6E (3 → 4) 74HC14N
IC6F (5 → 6) 74HC14N
GND

TODO:

* Write & Verify Verilog Model
* DRC

U NC

Title: cft	
Revision: Rev D	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	3/49
Simulation filename: reset.v	
More Info: http://www.bedroomlan.org/cft	

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Microcode Sequencer

Notes

32k x 8 (2x256) ICs required for Microcode v4.
512k x 8 ICs are cheaper and easier to come by, though,
so this schematic uses these. Smaller ICs can be substituted.

ROMS to be socketed for easy reprogramming.

Use 70ns or 50ns chips.

Vertical microcode (unit selectors RUNIT, WUNIT and OPIF) are pulled low because a value of zero selects no unit.

$\overline{WS}$: indicates a wait state. Inhibits the uPC counter.
$\overline{HALT}$: halts the processor. The control unit's outputs are at High-Z. Consequently, the processor is disconnected from all busses. Control signals are active low and pulled up, so other units (like the front panel) may operate them with the processor halted.

$\overline{RESET}$: while $\overline{RESET}$ is active (low), the microcode ROMs are deselected and their outputs tri-stated to avoid bus contention with units resetting uncleanly.

AINDEX/6 → AINDEX
SKIP/6 → SKIP
FL/6 → FL
FV/6 → FV
IRQS/6 → IRQS
RSTHOLD/3 → RSTHOLD

Microcode bank selection for future expansion or debugging. Bridge or jumper to 0000.

UCB0, UCB1, UCB2, UCB3 — SV1 — 4k7 RN2 — GND

Microcode PC

IC12 74HC161
P1 P2 P3 P4 Q1 Q2 Q3 Q4 → UPC0 UPC1 UPC2 UPC3
CLK CO LD PE TE CL
CLK4/2 → CLK4
WS/12 → WS
HALT
RSTHOLD
4k7 R19, 4k7 R20, VCC, GND

Open drain
4k7 R18
ENDEXT/44 → IC11C 74HC00N, IC11B 74HC00N → END

Microcode ROMs

IC13 29F040 — ROM image: microcode-00
IC14 29F040 — ROM image: microcode-01
IC15 29F040 — ROM image: microcode-02

UPC0 UPC1 UPC2 UPC3 AINDEX SKIP IR11 IR12 IR13 IR14 IR15 FL FV IRQS RSTHOLD UCB0 UCB1 UCB2 UCB3
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18
D0 D1 D2 D3 D4 D5 D6 D7
$\overline{CE}$ $\overline{OE}$ $\overline{WE}$

IR11/6 IR12/6 IR13/6 IR14/6 IR15/6

IC13 → RUNIT0 RUNIT1 RUNIT2 RUNIT3 WUNIT0 WUNIT1 WUNIT2 OPIF0
IC14 → OPIF1 OPIF2 OPIF3 $\overline{CPL}$ $\overline{CLL}$ $\overline{STI}$ $\overline{CLI}$ INCPC
IC15 → $\overline{STPDR}$ $\overline{STPAC}$ $\overline{DEC}$ $\overline{MEM}$ $\overline{IO}$ $\overline{R}$ $\overline{WEN}$ $\overline{END}$

RN1 4k7, RN4 4k7, RN3 4k7, RN5 4k7
C25 1uF, C26 1uF, C27 1uF

Note: $\overline{W}$ is $\overline{WEN}$ · CLK5.

RUNIT0/5 RUNIT1/5 RUNIT2/5 RUNIT3/5
WUNIT0/5 WUNIT1/5 WUNIT2/5
OPIF0/5 OPIF1/5 OPIF2/5 OPIF3/5
CPL/5 CLL/5 STI/5 CLI/5 INCPC/5 STPDR/5 STPAC/5 DEC/5 MEM/5 IO/5 R/5 WEN/5 END/5 UCE/7

HALT/43 → IC11A 74HC00N
RESET/3 → IC11A 74HC00N
IC11D 74HC00N → UCE

The ROMs may be placed on a daughterboard to facilitate easy expansion of the microcode store. In this case, a 46-pin header (2 power, 18 address, 2 control, 24 data) must be installed. Pull-ups/-downs to stay on the motherboard.

$\overline{UCE}$ is used by the unit decoders to ensure no units are selected when either $\overline{HALT}$ or $\overline{RESET}$ are inactive.

Decoupling

C19 C20 C21 C22 C23 0.1uF, C24 1uF, VCC, GND

Nota Bene: this sequencer can only run Microcode v.4!

TODO:

* Write & Verify Verilog Model
* DRC

U

Title: cft	
Revision: Rev F	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	4/49
Simulation filename: sequencer.v	
More Info: http://www.bedroomlan.org/cft	

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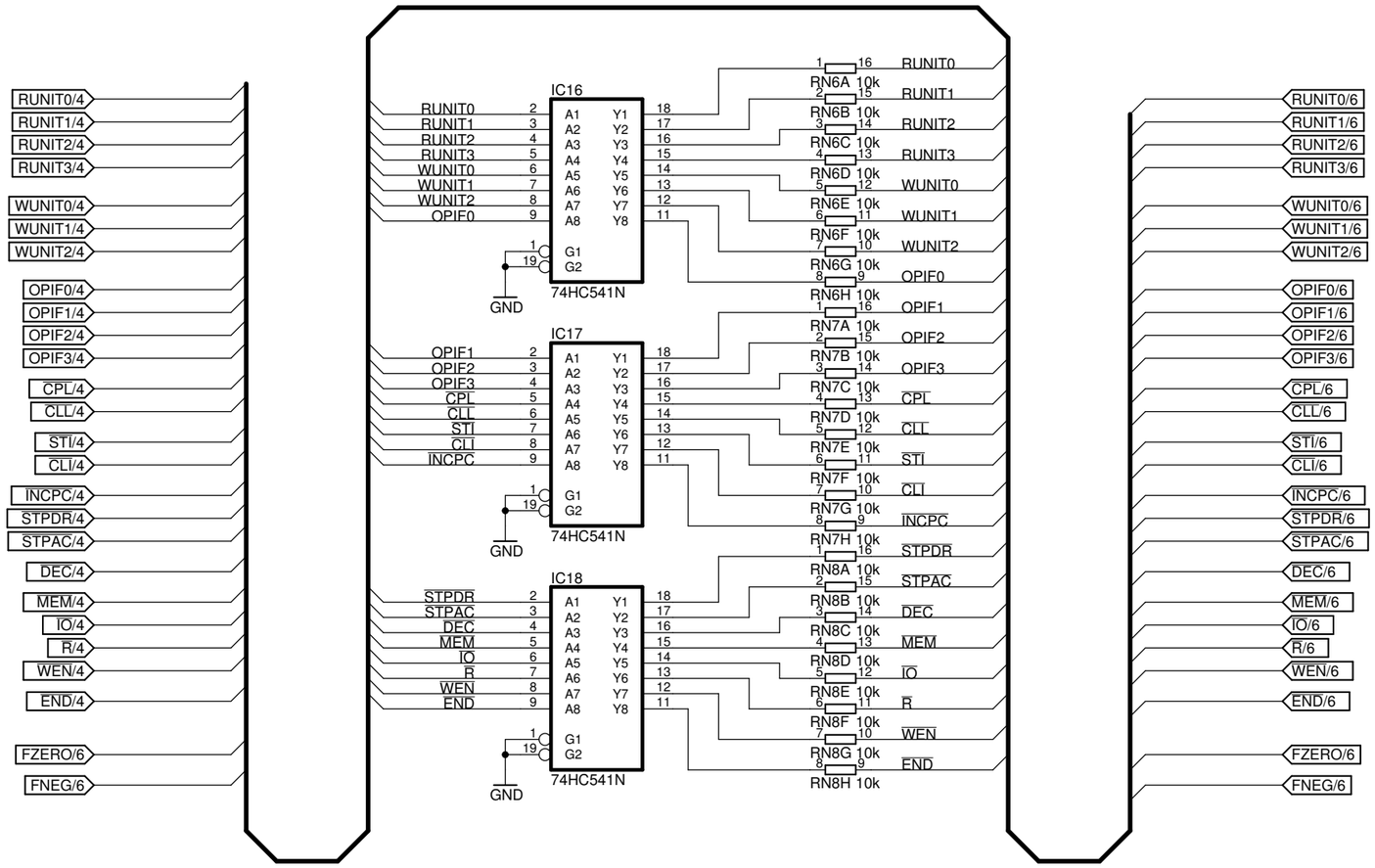
Microcode Sequencer Signal Hold

Probably Unnecessary -- to be verified in Verilog



TODO:

* DRC

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	5/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Processor Board A Connectors and Front Panel Buffers

IBUS[0..15]

FPIR[0..15]

UPC0/4
UPC1/4
UPC2/4
UPC3/4
AINDEX/4
SKIP/4
IR11/4
IR12/4
IR13/4
IR14/4
IR15/4
FL/4
FV/4
IRQS/4
RSTHOLD/4

IR[0..15] is sent to the Front Panel as FPIR[0..15].

RUNIT0/5
RUNIT1/5
RUNIT2/5
RUNIT3/5
WUNIT0/5
WUNIT1/5
WUNIT2/5
OPIF0/5
OPIF1/5
OPIF2/5
OPIF3/5
CPL/5
CLL/5
STI/5
CLI/5
INCPC/5
STPDR/5
STPAC/5
DEC/5
MEM/5
IO/5
R/5
WEN/5
END/5
FZERO/5
FNEG/5

IC19 — 74HC541N

UPC0	2	18	BUPC0
UPC1	3	17	BUPC1
UPC2	4	16	BUPC2
UPC3	5	15	BUPC3
AINDEX	6	14	BAINDEX
SKIP	7	13	BSKIP
FL	8	12	BFL
FV	9	11	BFV

IC20 — 74HC541N

IRQS	2	18	BIRQS
RSTHOLD	3	17	BRSTHOLD
RUNIT0	4	16	BRUNIT0
RUNIT1	5	15	BRUNIT1
RUNIT2	6	14	BRUNIT2
RUNIT3	7	13	BRUNIT3
WUNIT0	8	12	BWUNIT0
WUNIT1	9	11	BWUNIT1

IC21 — 74HC541N

FZERO	2	18	BFZERO
FNEG	3	17	BFNEG
FIRQ	4	16	BFIRQ
WUNIT2	5	15	BWUNIT2
OPIF0	6	14	BOPIF0
OPIF1	7	13	BOPIF1
OPIF2	8	12	BOPIF2
OPIF3	9	11	BOPIF3

IC22 — 74HC540N

CPL	2	18	BCPL
CLL	3	17	BCLL
STI	4	16	BSTI
CLI	5	15	BCLI
INCPC	6	14	BINCPC
STPDR	7	13	BINCDR
STPAC	8	12	BINCAC
DEC	9	11	BDEC

IC23 — 74HC540N

MEM	2	18	BMEM
IO	3	17	BIO
R	4	16	BR
WEN	5	15	BW
END	6	14	BEND

Front Panel lights #2 and FP Controller

JP3

FPIR0	1	2	INCPC
FPIR1	3	4	RAC
FPIR2	5	6	RPC
FPIR3	7	8	WAC
FPIR4	9	10	WAR
FPIR5	11	12	WDR
FPIR6	13	14	WIR
FPIR7	15	16	WPC
FPIR8	17	18	WEN
FPIR9	19	20	FPCLKEN
FPIR10	21	22	FPUSTEP
FPIR11	23	24	FPFAST
FPIR12	25	26	FPSLOW
FPIR13	27	28	FPRESET
FPIR14	29	30	POWEROK
FPIR15	31	32	
	33	34	
	35	36	
	37	38	
	39	40	

JP4

BUPC0	1	2	BMEM
BUPC1	3	4	BIO
BUPC2	5	6	BR
BUPC3	7	8	BW
BAINDEX	9	10	BEND
BSKIP	11	12	BCPL
BFL	13	14	BCLL
BFV	15	16	BSTI
BFIRQ	17	18	BCLI
BIRQS	19	20	BINCPC
BRSTHOLD	21	22	BSTPDR
BRUNIT0	23	24	BSTPAC
BRUNIT1	25	26	BDEC
BRUNIT2	27	28	BOPIF0
BRUNIT3	29	30	BOPIF1
BWUNIT0	31	32	BOPIF2
BWUNIT1	33	34	BOPIF3
BWUNIT2	35	36	
	37	38	
	39	40	

Front Panel lights #1

JP5

END	1	2	IBUS0
STPAC	3	4	IBUS1
STPDR	5	6	IBUS2
INCPC	7	8	IBUS3
RAC	9	10	IBUS4
RDR	11	12	IBUS5
RPC	13	14	IBUS6
WAC	15	16	IBUS7
WAR	17	18	IBUS8
WDR	19	20	IBUS9
WPC	21	22	IBUS10
FNEG	23	24	IBUS11
FZERO	25	26	IBUS12
PC10	27	28	IBUS13
PC11	29	30	IBUS14
PC12	31	32	IBUS15
PC13	33	34	
PC14	35	36	
PC15	37	38	
	39	40	

IBUS[0..15]

Control Bus, board A to B

JP6

CLL	1	2	IBUS0
CPL	3	4	IBUS1
RSTHOLD	5	6	IBUS2
WALU	7	8	IBUS3
FL	9	10	IBUS4
FV	11	12	IBUS5
IR0	13	14	IBUS6
IR2	15	16	IBUS7
RUNIT0	17	18	IBUS8
RUNIT1	19	20	IBUS9
RUNIT2	21	22	IBUS10
RUNIT3	23	24	IBUS11
	25	26	IBUS12
	27	28	IBUS13
	29	30	IBUS14
	31	32	IBUS15
	33	34	
	35	36	
	37	38	
	39	40	

IBUS[0..15]

Control Bus, board A to C

A B C

VCC

JP7

POWEROK/3

PSU header

JP8

FPCLKEN
FPUSTEP

To DEB board

Note: BW is really the buffered version of WEN, but the WEN strobe is counter-intuitive.

TODO:

* DRC

UNCU

Title: cft	
Revision: Rev F	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	6/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Read & Write Unit Decoding

RESET/4
UCE/4
CLK3/3
CLK1/2
RUNIT0/6
RUNIT1/6
RUNIT2/6
RUNIT3/6
WUNIT0/6
WUNIT1/6
WUNIT2/6

RESET/8
UCE/4
CLK3/17
CLK1/27
RUNIT0/18
RUNIT1/18
RUNIT2/18
RUNIT3/18
WUNIT0/6
WUNIT1/6
WUNIT2/6

CLK3 RESET WUNIT2 WUNIT1 WUNIT0 RESET RUNIT3 CLK1 RUNIT2 RUNIT1 RUNIT0 UCE

74HC04N IC24A

IC25 74HC138N
RUNIT0 RUNIT1 RUNIT2 CLK1 RUNIT3 RUEN

IC27 74HC541N
UCE GND

VCC RN9 4k7

RUNIT is decoded partially: only 0xxx values are decoded here.
ALU Operation decoding (RUNIT=1xxx) is done on the ALU board.

0000 = Idle
0001 = Reserved
0010 = Read from AGL (RAGL)
0011 = Read from PC (RPC)
0100 = Read from DR (RDR)
0101 = Read from AC (RAC)
0110 = Reserved
0111 = Reserved
1XXX = ALU operation or Constant

R1 Reserved
RAGL/9
RPC/14
RDR/15
RAC/16
R6 Reserved
R7 Reserved

IC26 74HC138N
WUNIT0 WUNIT1 WUNIT2 RESET CLK3

IC28 74HC541N
UCE GND

VCC RN10 4k7

Write Unit Decoder:

000 = Idle
001 = Reserved
010 = Write AR (WAR)
011 = Write PC (WPC)
100 = Write IR (WIR)
101 = Write DR (WDR)
110 = Write AC & ALU Port A (WAC)
111 = Write ALU Port B (WALU)

W1 Reserved
WAR/13
WPC/14
WIR/10
WDR/15
WAC/16
WALU/18

When UCE is asserted, unit decoders must tri-state their outputs.

TODO:

* DRC

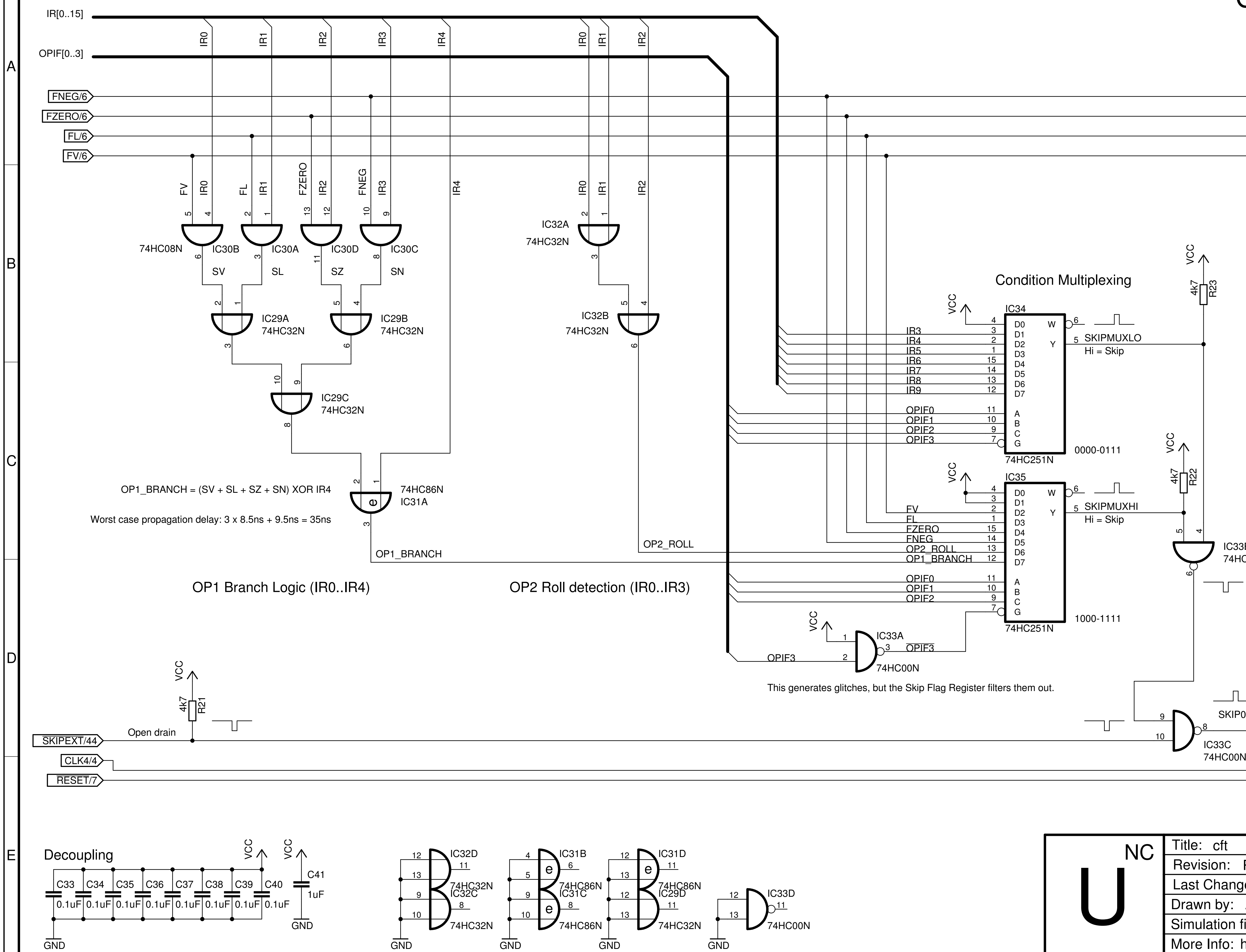
Decoupling
C28 C29 C30 C31 0.1uF
C32 1uF
GND

IC24B IC24C IC24D IC24E IC24F 74HC04N

Title:	cft
Revision:	Rev F
Last Change:	16 Dec 2012 12:04:37
Drawn by:	Alexios
	7/49
Simulation filename:	unit_decoder.v
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

Skip/Branch Logic



TODO:	[redacted]
* DRC	

Microcode v.4 OPIF field

OPIF = 0000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 0001: IF3 ($\overline{SKIP}$ = IR3)
OPIF = 0010: IF4 ($\overline{SKIP}$ = IR4)
OPIF = 0011: IF5 ($\overline{SKIP}$ = IR5)
OPIF = 0100: IF6 ($\overline{SKIP}$ = IR6)
OPIF = 0101: IF7 ($\overline{SKIP}$ = IR7)
OPIF = 0110: IF8 ($\overline{SKIP}$ = IR8)
OPIF = 0111: IF9 ($\overline{SKIP}$ = IR9)

OPIF = 1000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1001: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1010: IF$\overline{V}$ ($\overline{SKIP}$ = IFV, skip if V=0)
OPIF = 1011: IF$\overline{L}$ ($\overline{SKIP}$ = IFL, skip if L=0)
OPIF = 1100: IF$\overline{ZERO}$ ($\overline{SKIP}$ = IFZERO, skip if Z=0)
OPIF = 1101: IF$\overline{NEG}$ ($\overline{SKIP}$ = FNEG, skip if N=0)
OPIF = 1110: IFROLL ($\overline{SKIP}$ = IR0 + IR1 + IR2)
OPIF = 1111: IFBRANCH Logic

U NC	
Title: cft	
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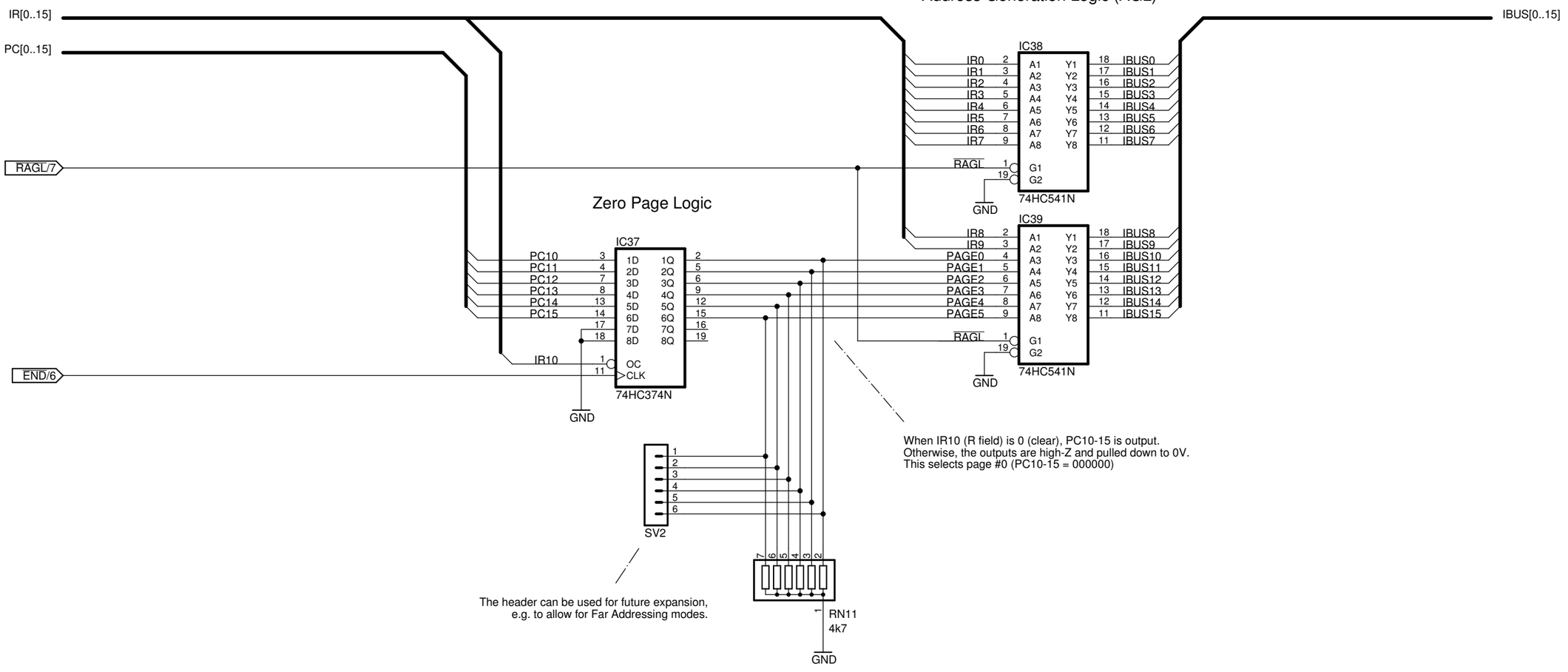
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	8/49
Simulation filename: skip_unit.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Address Generation Logic

Address Generation Logic (AGL)



Notes

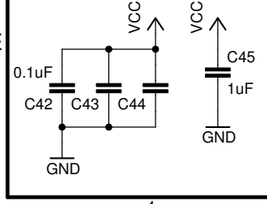
The value of the PC is clocked into the D-Flip Flop on the rising edge of $\overline{END}$.
At that point, the PC holds the value of the instruction about to be fetched.

If this registering doesn't take place, by the time the AGL is read, the PC will have been incremented (at the end of the fetch cycle), and pointing to the next instruction.

Thus, the AGL would generate addresses for PC+1. This works as the user expects for the first 1023 page offsets, and fails on the 1024th, where the AGL produces an address for the next page.

This would make programming with page-relative modes much less intuitive.

Decoupling



TODO:

* DRC

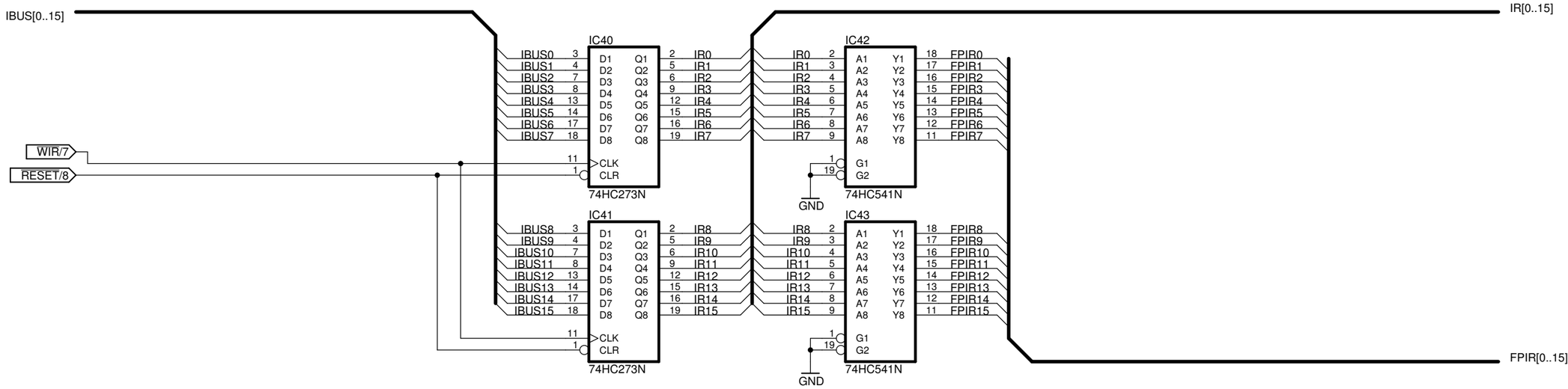
NC U	Title: cft
	Revision: Rev B
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios 9/49
	Simulation filename: agl.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

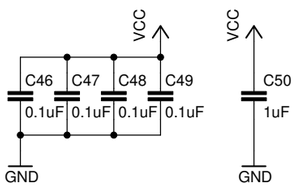
Instruction Register

Instruction Register (IR)

Front Panel Buffers & Connectors



Decoupling



TODO:

* DRC

Title: cft	
Revision: Rev B	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	10/49
Simulation filename: ir.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Interrupt State Machine

END/9
RESET/10
STI/6
CLI/6

END/13
RESET/12

VCC
R24
4k7
IRQ/22

IRQ should be driven by open-drain gates.
It is pulled up here.

Interrupt Flag (Asynchronous)

IC44A
74HC08N

IC46A
74HC112N
GND

FINT

Note: for testing purposes.

Masking and State (Synchronous)

IC45A
74HC32N

IC46B
74HC112N
GND

MASKEDIRQ
RESET_OR_CLI

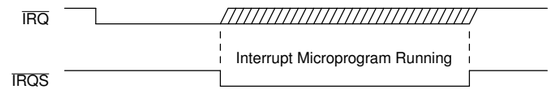
FIRQ/6

Note: for front panel use

Interrupts Enabled light (optional)

LED-5MM-GREEN
LED3
330R
R25
GND

Safe Interrupt Signalling



Assert IRQ, wait for IRQS, deassert IRQ.

Interrupt Seen light (optional)

LED-5MM-GREEN
LED4
330R
R26
GND

Interrupt Request Register FF
(Instruction-synchronous)

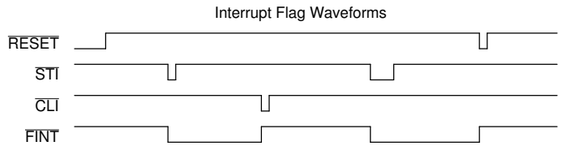
IC36B
74HC74N
VCC
FIRQ
END
RESET

IRQS/20

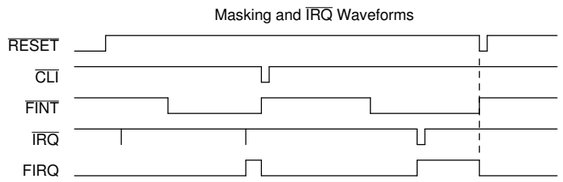
This is also the interrupt acknowledge signal.

Shared with IC36.

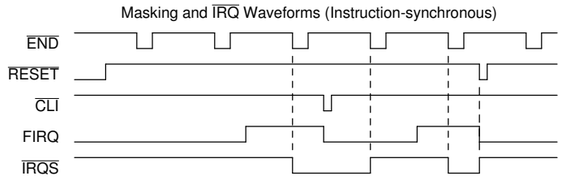
Interrupt Flag Waveforms



Masking and IRQ Waveforms



Masking and IRQ Waveforms (Instruction-synchronous)



Notes

The Interrupt flag denotes our disposition to handle incoming interrupts (allow or ignore).
At RESET time, interrupts are cleared and further interrupts are masked (ignored).
The falling edge of CLI or RESET clears the interrupt flag, ignoring interrupts.
The falling edge of STI sets the flag, allowing interrupts.

When the interrupt flag is set, the falling edge of IRQ triggers an interrupt (FIRQ high).

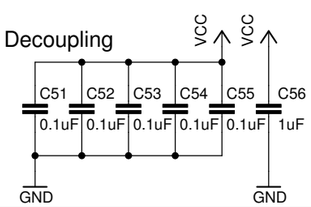
This is ignored until the end of the current instruction (falling edge of END).
At that point, the register FF clocks FIRQ in, asserting IRQS to the microcode sequencer.
The K input of the flip flop is held constantly high. With FIRQ high, this is a toggle action.

At the next instruction (falling edge of END), IRQS would toggle again.
Before this happens, the interrupt microprogram asserts CLI, clearing FIRQ, so no further toggling takes place. Instead, with K low and J high, IRQS is deasserted, resuming normal excecution.

TODO:

* DRC

Decoupling



IC44B
IC44C
74HC08N

IC44D
IC45B
74HC08N

IC45C
IC45D
74HC32N

74HC32N

Title:	cft
Revision:	Rev B
Last Change:	16 Dec 2012 12:04:37
Drawn by: Alexios	11/49
Simulation filename:	int.v
More Info:	http://www.bedroomlan.org/cft

U NC

CFT Mini-Computer

Data Bus Driver & Bus Termination

RESET/11
WS/4
MEM/6
IO/6
R/6
WEN/6
T34/2
CLK2/2
CLK4/8
IBUS[0..15]

RESET/13
WS/44
MEM/13
IO/13
R/22
WEN/42
T34/18
CLK2/44
CLK4/44

Wait State

RESET CLK2 T34 WS

IC51B 74HC32N

IC47A
PRE D Q
CLK CLR Q
74HC74N
CLK2 RESET WAITING

GND

IC51C 74HC32N

IC48A 74HC08N

T34 IO MEM

IC48B 74HC08N

Write Strobe Generation

CLK4 WEN

IC51A 74HC32N

IC51D 74HC32N

WAITING

Asserting WAITING inhibits W strobes.

IC52A 74HC04N

IC48D 74HC08N

IC52C 74HC04N

IC52B 74HC04N

RESET

IC48C 74HC08N

VCC

IC47B
PRE D Q
CLK CLR Q
74HC74N

W/21

Input from Q instead.

Data Bus Transceiver

IBUS[0..15]

DB[0..15]

IC49 74HC245N

IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7 → DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

R BUSEN

IC50 74HC245N

IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15 → DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

DB[0..15]

DB[0..15]

Bus Hold

IC53 74HC541N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8

G1 G2

GND

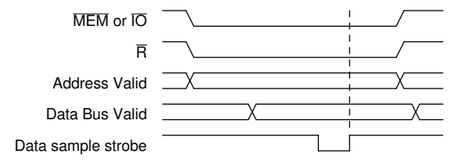
IC54 74HC541N

DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15 → Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8

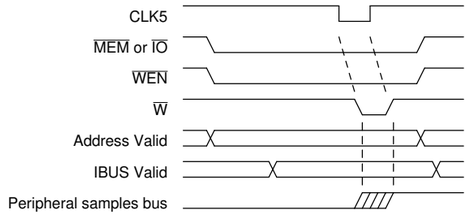
RN12A10k DB0
RN12B10k DB1
RN12C10k DB2
RN12D10k DB3
RN12E10k DB4
RN12F10k DB5
RN12G10k DB6
RN12H10k DB7
RN13A10k DB8
RN13B10k DB9
RN13C10k DB10
RN13D10k DB11
RN13E10k DB12
RN13F10k DB13
RN13G10k DB14
RN13H10k DB15

Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.

Memory or I/O Space Read Waveforms



Memory or I/O Space Write Waveforms



Decoupling

VCC

C57 0.1uF C58 0.1uF C59 0.1uF C60 0.1uF C61 0.1uF C62 1uF

GND GND

74HC04N

IC52F IC52E IC52D

GND

TODO:

* DRC

U

Title: cft	
Revision: Rev C	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	12/49
Simulation filename: databus.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Address Register, Address Bus Drivers & Termination, Autoindex Logic, Device Decoder

MEM/12
IO/12
IC55A
74HC08N
ABEN

IBUS[0..15]

Address Register (AR)

IC56 74HC273N
IC57 74HC273N
WAR/7
RESET/12
WAR
RESET

Address Bus Drive Logic

IC58 IC59 74HC541N
ABEN
GND

Address Bus Hold

IC61 IC62 74HC541N
AB[0..15]
RN14A 10k
RN14B 10k
RN14C 10k
RN14D 10k
RN14E 10k
RN14F 10k
RN14G 10k
RN14H 10k
RN15A 10k
RN15B 10k
RN15C 10k
RN15D 10k
RN15E 10k
RN15F 10k
RN15G 10k
RN15H 10k

Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.

TODO:
* DRC

END/11
END
IO

IC60 74HC688N
VCC
AR7 AR8 AR9 AR10 AR11 AR12 AR13 AR14 AR15

IC63A 74HC74N
AINDEX/6

Notes (Autoindex Logic)

This evaluates the function:

$\overline{AINDEX} = \overline{AR == 0000'0000'1XXX'XXXX}$

It is necessary to register $\overline{AINDEX}$ because AR is changed during execution of an indirect mode instruction.

The flag is cleared at the end of the instruction, when $\overline{END}$ is asserted.

Autoindex Logic

I/O Device Address Decoder

IC65 74HC138N
IC64 74HC688N
ABEN
IO
SYSDEV/21
IODEV1XX/44
IODEV2XX/44
IODEV3XX/44

Decodes I/O addresses 0n00-0nFF to simplify interfacing.

For n = 0, $\overline{SYSDEV}$ is asserted.
For n = 1, $\overline{IODEV1XX}$ is asserted.
For n = 2, $\overline{IODEV2XX}$ is asserted.
For n = 3, $\overline{IODEV3XX}$ is asserted.

Other devices must be decoded ad hoc.

Decoupling

C63 C64 C65 C66 C67 C68 C69 C70 C71 0.1uF
C72 1uF
VCC
GND

IC55D IC55B IC55C 74HC08N

IC63B 74HC74N

NC	Title: cft
	Revision: Rev A
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios — 13/49
	Simulation filename: addressing.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Major Registers: Program Counter (PC)

RPC/7
WPC/7
INCPC/6
RESET/13
IBUS[0..15]

NB: this is RESET inverted, fed to all 3 major registers' CLEAR signals ('193).

RESET/15
IBUS[0..15]

74HC04N IC66A

Register & Increment

VCC

IC67 74HC193N
IBUS0 IBUS1 IBUS2 IBUS3 → A B C D → PC0 PC1 PC2 PC3
WPC → LOAD
INCPC → UP
RESET → CLEAR
BORROW CARRY → DOWN

IC68 74HC193N
IBUS4 IBUS5 IBUS6 IBUS7 → A B C D → PC4 PC5 PC6 PC7
WPC → LOAD
RESET → CLEAR
BORROW CARRY → UP DOWN

IC69 74HC193N
IBUS8 IBUS9 IBUS10 IBUS11 → A B C D → PC8 PC9 PC10 PC11
WPC → LOAD
RESET → CLEAR
BORROW CARRY → UP DOWN

IC70 74HC193N
IBUS12 IBUS13 IBUS14 IBUS15 → A B C D → PC12 PC13 PC14 PC15
WPC → LOAD
RESET → CLEAR
BORROW CARRY → UP DOWN

Tri-State Buffering

IC71 74HC541N
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 → A1 A2 A3 A4 A5 A6 A7 A8
G1 G2 (1, 19)
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7

IC72 74HC541N
PC8 PC9 PC10 PC11 PC12 PC13 PC14 PC15 → A1 A2 A3 A4 A5 A6 A7 A8
G1 G2 (1, 19)
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15

PC[0..15]

Front Panel Buffers & Connectors

IC73 74HC541N
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 → A1 A2 A3 A4 A5 A6 A7 A8
G1 G2 (1, 19) → GND
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → 22-23-2081 CON1-1 CON1-2 CON1-3 CON1-4 CON1-5 CON1-6 CON1-7 CON1-8

IC74 74HC541N
PC8 PC9 PC10 PC11 PC12 PC13 PC14 PC15 → A1 A2 A3 A4 A5 A6 A7 A8
G1 G2 (1, 19) → GND
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → 22-23-2081 CON2-1 CON2-2 CON2-3 CON2-4 CON2-5 CON2-6 CON2-7 CON2-8

Decoupling

VCC
C73 C74 C75 C76 C77 C78 C79 C80 0.1uF
C81 1uF
GND

74HC04N IC66C IC66B IC66E IC66D IC66F
GND

TODO:
* DRC

NC

Title: cft	
Revision: Rev B	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	14/49
Simulation filename: register.v#reg_pc	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Major Registers: Data Register (DR)

RDR/7
WDR/7
STPDR/6
DEC/6
RESET/14
IBUS[0..15]

NB: this is $\overline{\text{RESET}}$ inverted.

DEC/16
RESET/16
IBUS[0..15]

Register & Increment

IC75A
74HC139N
GND

IC76
IC77
IC78
IC79
74HC193N

Tri-State Buffering

IC80
IC81
74HC541N

Front Panel Buffers & Connectors

IC82
IC83
74HC541N
22-23-2081
CON3-1 … CON3-8
CON4-1 … CON4-8

DR[0..15]

Decoupling

C82 C83 C84 C85 C86 C87 C88 C89 0.1uF
C90 1uF
VCC
GND

TODO:

* DRC

UNC

Title:	cft
Revision:	Rev C
Last Change:	16 Dec 2012 12:04:37
Drawn by:	Alexios
	15/49
Simulation filename:	register.v#reg_dr
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

Accumulator (AC), Zero Flag & Negative Flag

RAC/7
WAC/7
DEC/15
RESET/15
IBUS[0..15]
DEC/15
IBUS[0..15]

STPAC/6
IC75B
STPAC 14
DEC 13
A
B
G 15
Y0 12 ACDOWN
Y1 11 ACUP
Y2 10
Y3 9
74HC139N
GND

Register & Increment

IC84
IBUS0 15
IBUS1 1
IBUS2 10
IBUS3 9
WAC 11
ACUP 5
ACDOWN 4
RESET 14
A QA 3 AC0
B QB 2 AC1
C QC 6 AC2
D QD 7 AC3
LOAD
BORROW
UP CARRY 13 ACB1 12 ACC1
DOWN
CLEAR
74HC193N

ACB1
ACC1

IC85
IBUS4 15
IBUS5 1
IBUS6 10
IBUS7 9
WAC 11
ACC1 5
ACB1 4
RESET 14
A QA 3 AC4
B QB 2 AC5
C QC 6 AC6
D QD 7 AC7
LOAD
BORROW
UP CARRY 13 ACB2 12 ACC2
DOWN
CLEAR
74HC193N

ACB2
ACC2

IC86
IBUS8 15
IBUS9 1
IBUS10 10
IBUS11 9
WAC 11
ACC2 5
ACB1 4
RESET 14
A QA 3 AC8
B QB 2 AC9
C QC 6 AC10
D QD 7 AC11
LOAD
BORROW
UP CARRY 13 ACB3 12 ACC3
DOWN
CLEAR
74HC193N

ACB3
ACC3

IC87
IBUS12 15
IBUS13 1
IBUS14 10
IBUS15 9
WAC 11
ACC3 5
ACB1 4
RESET 14
A QA 3 AC12
B QB 2 AC13
C QC 6 AC14
D QD 7 AC15
LOAD
BORROW
UP CARRY 13 DECCPL 12 INCCPL
DOWN
CLEAR
74HC193N

DECAC reserved for future expansion

Tri-State Buffering

IC88
AC0 2
AC1 3
AC2 4
AC3 5
AC4 6
AC5 7
AC6 8
AC7 9
G1 1
G2 19
A1 Y1 18 IBUS0
A2 Y2 17 IBUS1
A3 Y3 16 IBUS2
A4 Y4 15 IBUS3
A5 Y5 14 IBUS4
A6 Y6 13 IBUS5
A7 Y7 12 IBUS6
A8 Y8 11 IBUS7
74HC541N

IC89
AC8 2
AC9 3
AC10 4
AC11 5
AC12 6
AC13 7
AC14 8
AC15 9
G1 1
G2 19
A1 Y1 18 IBUS8
A2 Y2 17 IBUS9
A3 Y3 16 IBUS10
A4 Y4 15 IBUS11
A5 Y5 14 IBUS12
A6 Y6 13 IBUS13
A7 Y7 12 IBUS14
A8 Y8 11 IBUS15
74HC541N

Zero Flag

IC91
AC0 2
AC1 4
AC2 6
AC3 8
AC4 11
AC5 13
AC6 15
AC7 17
P0 P=Q 19
P1
P2
P3
P4
P5
P6
P7
Q0 3
Q1 5
Q2 7
Q3 9
Q4 12
Q5 14
Q6 16
Q7 18
G 1
74HC688N
GND

IC90
AC8 2
AC9 4
AC10 6
AC11 8
AC12 11
AC13 13
AC14 15
AC15 17
P0 P=Q 19
P1
P2
P3
P4
P5
P6
P7
Q0 3
Q1 5
Q2 7
Q3 9
Q4 12
Q5 14
Q6 16
Q7 18
G 1
74HC688N
GND

FZERO

Front Panel Buffers & Connectors

IC93
AC0 2
AC1 3
AC2 4
AC3 5
AC4 6
AC5 7
AC6 8
AC7 9
G1 1
G2 19
A1 Y1 18 CON5-1
A2 Y2 17 CON5-2
A3 Y3 16 CON5-3
A4 Y4 15 CON5-4
A5 Y5 14 CON5-5
A6 Y6 13 CON5-6
A7 Y7 12 CON5-7
A8 Y8 11 CON5-8
22-23-2081
74HC541N
GND

IC94
AC8 2
AC9 3
AC10 4
AC11 5
AC12 6
AC13 7
AC14 8
AC15 9
G1 1
G2 19
A1 Y1 18 CON6-1
A2 Y2 17 CON6-2
A3 Y3 16 CON6-3
A4 Y4 15 CON6-4
A5 Y5 14 CON6-5
A6 Y6 13 CON6-6
A7 Y7 11 CON6-7
A8 Y8 11 CON6-8
22-23-2081
74HC541N
GND

AC15 = FNEG
FNEG/40

IC92A
FZERO 1
2
74HC04N
FZERO/40

DECCPL/17
INCCPL/17
Asynchronous toggles of L
AC[0..15]

Decoupling

VCC
C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 0.1uF
C101 1uF
GND

IC92B 3 4 74HC04N
IC92C 5 6 74HC04N
IC92D 9 8 74HC04N
IC92E 11 10 74HC04N
IC92F 13 12 74HC04N
GND

TODO:

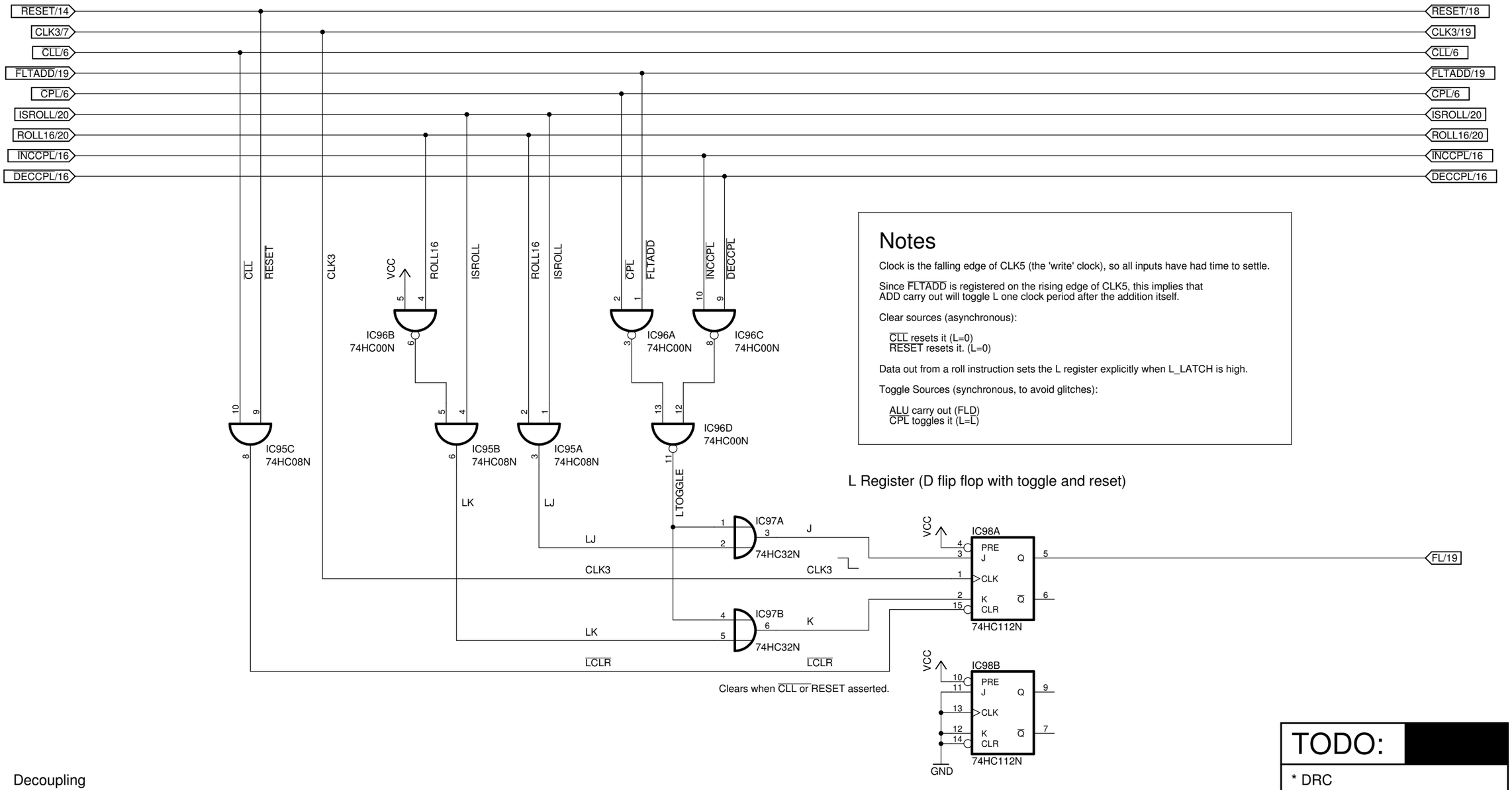
* DRC

NC

Title:	cft
Revision:	Rev C
Last Change:	16 Dec 2012 12:04:37
Drawn by:	Alexios
	16/49
Simulation filename:	register.v#reg_ac
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

The L Register



Notes

Clock is the falling edge of CLK5 (the 'write' clock), so all inputs have had time to settle.

Since FLTADD is registered on the rising edge of CLK5, this implies that ADD carry out will toggle L one clock period after the addition itself.

Clear sources (asynchronous):

CLL resets it (L=0)
RESET resets it. (L=0)

Data out from a roll instruction sets the L register explicitly when L_LATCH is high.

Toggle Sources (synchronous, to avoid glitches):

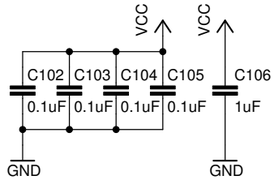
ALU carry out (FLD)
CPL toggles it (L=L)

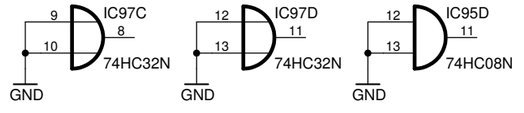
L Register (D flip flop with toggle and reset)

TODO:

* DRC

Decoupling





Size: U	Title: cft
	Revision: Rev B
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios — 17/49
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Arithmetic/Logic Unit: Decoding Logic

RUNIT[0..3]
IR[0..15]
IBUS[0..15]
WALU/7
RSTHOLD/6
RESET/17
T34/12

IBUS[0..15]
WALU/7
RSTHOLD/6
RESET/19
T34/44

WALU
IBUS[0..15]
RUNIT0
RUNIT1
IR0
IR2
T34
RESET
RSTHOLD
RUNIT3
RUNIT2

ALU Port B Buffer

B[0..15]

IC99

IBUS0	2	1D	1Q	19	B0
IBUS1	3	2D	2Q	18	B1
IBUS2	4	3D	3Q	17	B2
IBUS3	5	4D	4Q	16	B3
IBUS4	6	5D	5Q	15	B4
IBUS5	7	6D	6Q	14	B5
IBUS6	8	7D	7Q	13	B6
IBUS7	9	8D	8Q	12	B7
	11	CLK			
	1	OC			

74HC574N

GND

IC100

IBUS8	2	1D	1Q	19	B8
IBUS9	3	2D	2Q	18	B9
IBUS10	4	3D	3Q	17	B10
IBUS11	5	4D	4Q	16	B11
IBUS12	6	5D	5Q	15	B12
IBUS13	7	6D	6Q	14	B13
IBUS14	8	7D	7Q	13	B14
IBUS15	9	8D	8Q	12	B15
	11	CLK			
	1	OC			

74HC574N

GND

Unary Operation Decoder

UOP2

ROLLOP0
IR0
RUNIT0

ROLLOP2
IR2
RUNIT1

IC102

	6	1C0	1Y	7	UOP0
	5	1C1			
	4	1C2			
	3	1C3			
	10	2C0	2Y	9	UOP1
	11	2C1			
	12	2C2			
	13	2C3			
	14	A			
	2	B			
	1	1G			
	15	2G			

74HC253N

GND

IC101A

1		
2		
	3	

74HC32N

GND

These buffers are used to tristate the binary ALU ROMs.
The $\overline{OE}$ line on these ROMs is permanently low, to allow parallel execution.
This allows the most expensive op, ADD, to start fetching as soon
as AC is loaded, allowing a full clock cycle for carry propagation.
Since ADD can take up to 210ns to propagate carry, this allows
the processor to reach a theoretical clock speed of around 4 MHz.

IC103

RUNIT2	1	A	Y0	15	
RUNIT3	2	B	Y1	14	
RSTHOLD	3	C	Y2	13	
			Y3	12	
			Y4	11	
RESET	6	G1	Y5	10	
T34	4	G2A	Y6	9	
	5	G2B	Y7	7	

74HC138N

GND

IC104

Y0	2	A1	Y1	18	IBUS0
Y1	3	A2	Y2	17	IBUS1
Y2	4	A3	Y3	16	IBUS2
Y3	5	A4	Y4	15	IBUS3
Y4	6	A5	Y5	14	IBUS4
Y5	7	A6	Y6	13	IBUS5
Y6	8	A7	Y7	12	IBUS6
Y7	9	A8	Y8	11	IBUS7
	1	G1			
	19	G2			

74HC541N

BOE

IC105

Y8	2	A1	Y1	18	IBUS8
Y9	3	A2	Y2	17	IBUS9
Y10	4	A3	Y3	16	IBUS10
Y11	5	A4	Y4	15	IBUS11
Y12	6	A5	Y5	14	IBUS12
Y13	7	A6	Y6	13	IBUS13
Y14	8	A7	Y7	12	IBUS14
Y15	9	A8	Y8	11	IBUS15
	1	G1			
	19	G2			

74HC541N

ALU Operation ROM selector (unary/binary)

Y[0..15]
UOE/20
BOE/19
UOP[0..2]
B[0..15]

Decoupling

VCC
C107 0.1uF
C108 0.1uF
C109 0.1uF
C110 0.1uF
C111 1uF
GND

74HC32N
IC101D
IC101B
IC101C
74HC32N
74HC32N
GND

NC U	Title: cft
	Revision: Rev B
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios 18/49
	Simulation filename: alu.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

ALU Binary Operators

B[0..15]
AC[0..15]
RUNIT[0..3]
RESET/18
CLK3/17
BOE/18
FL/17

RESET/20
CLK3/44
BOE/18
FL/20

ALU Binary Operator ROMs

IC106 — 29F040 — ROM image: alu-binary-6bit-00
IC107 — 29F040 — ROM image: alu-binary-6bit-00
IC108 — 29F040 — ROM image: alu-binary-4bit-00

C118 1uF
C119 1uF
C120 1uF
4k7 R27
4k7 R28

Flag Strobe Generation

IC109 — 74HC253N

AB (BOE FLATCH) -> FLAGCLK
A = BOE = 0 and B = FLATCH = 1 -> Input 01 = xC2 = CLK3

IC110B — 74HC74N
IC110A — 74HC74N

Y[0..15]

Decoupling

C112 0.1uF, C113 0.1uF, C114 0.1uF, C115 0.1uF, C116 0.1uF, C117 1uF

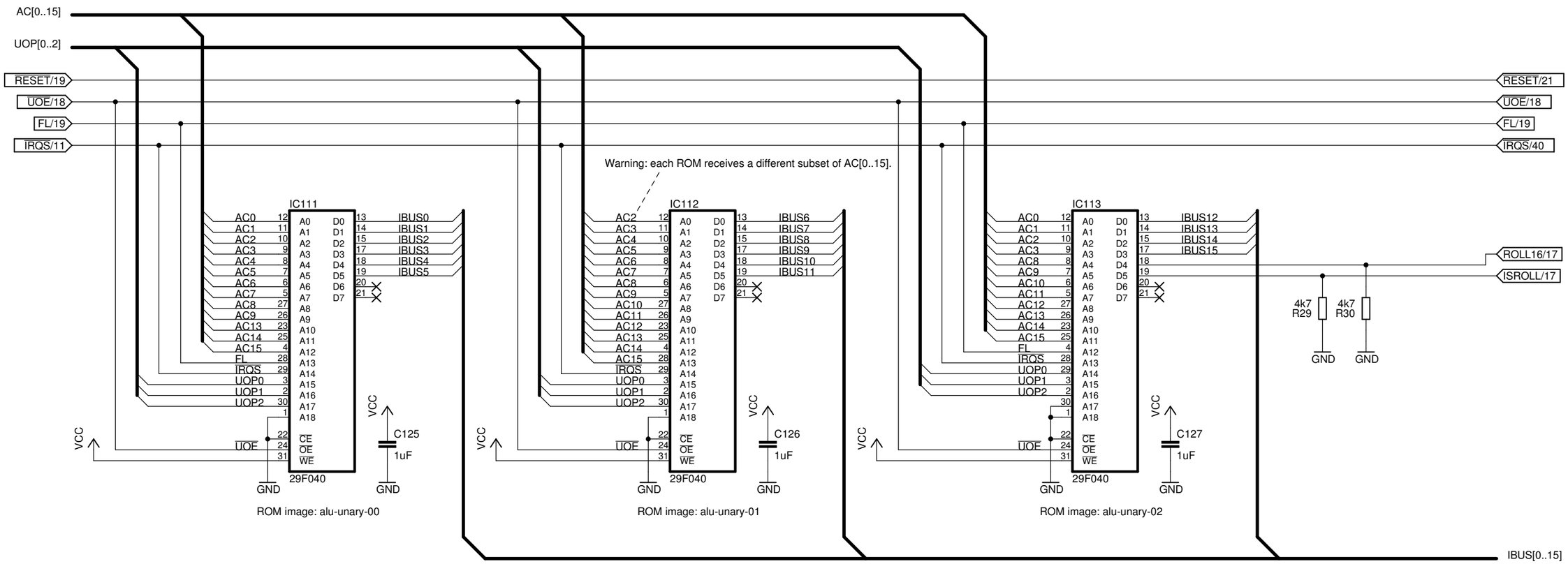
TODO:
* DRC

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	19/49
Simulation filename: alu.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

ALU Unary Operators and Constant Store

Unary Operations and Constant Store

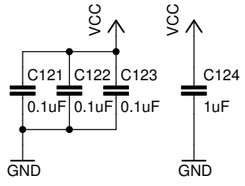


ROM image: alu-unary-00

ROM image: alu-unary-01

ROM image: alu-unary-02

Decoupling



Notes

ROMs to be socketed for easy re-programming.

TODO:

* DRC

Size	U
Title	cft
Revision	Rev B
Last Change	16 Dec 2012 12:04:37
Drawn by	Alexios
Sheet	20/49
Simulation filename	alu.v
More Info	http://www.bedroomlan.org/cft

CFT Mini-Computer

8 kW Bank Switching Memory Controller (without 74670)

AB[0..15]

DB[0..15]

AB14

AB13

RESET/20 → RESET/22

MEM/13 → MEM/24

W/12 → W/22

SYSDEV/13 → SYSDEV/22

AB15RAM → AB15RAM

IC115 74HC138N
- AB0, AB1, AB2 → A, B, C
- AB6 → G1
- AB5 → IC114A (74HC32N) → G2A
- AB7 → IC114A (74HC32N) → G2B
- W → IC114D (74HC32N)
- SYSDEV → IC114D (74HC32N)
- VCC → G1
- MEM → G2A
- GND → G2B
- Y0 BANKW0, Y1 BANKW1, Y2 BANKW2, Y3 BANKW3, Y4 BANKW4, Y5 BANKW5, Y6 BANKW6, Y7 BANKW7

IC116 74HC138N
- AB13, AB14, AB15 → A, B, C
- VCC → G1
- MEM → G2A
- GND → G2B
- Y0 BANKR0, Y1 BANKR1, Y2 BANKR2, Y3 BANKR3, Y4 BANKR4, Y5 BANKR5, Y6 BANKR6, Y7 BANKR7

IC118 74HC574N
- DB0..DB7 → 1D..8D
- BANKW0, BANKR0 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC119 74HC574N
- DB0..DB7 → 1D..8D
- BANKW1, BANKR1 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC120 74HC574N
- DB0..DB7 → 1D..8D
- BANKW2, BANKR2 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC121 74HC574N
- DB0..DB7 → 1D..8D
- BANKW3, BANKR3 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC122 74HC574N
- DB0..DB7 → 1D..8D
- BANKW4, BANKR4 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC123 74HC574N
- DB0..DB7 → 1D..8D
- BANKW5, BANKR5 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC124 74HC574N
- DB0..DB7 → 1D..8D
- BANKW6, BANKR6 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC125 74HC574N
- DB0..DB7 → 1D..8D
- BANKW7, BANKR7 → CLK, OC
- 1Q..8Q → AE'0..AE'7

IC126 74HC541N
- AE'0..AE'7 → A1..A8
- G1, G2 → GND
- Y1..Y8 → AEXT0..AEXT7

IC127 74HC541N
- AE'0..AE'7 → A1..A8
- G1, G2 → GND
- Y1..Y8 → AEXT0..AEXT7

IC128 74HC541N
- AEXT0..AEXT7 → A1..A8
- G1, G2 → GND
- Y1..Y8 → BANK0..BANK7

BANK[0..7]

AEXT[0..7]

IC117A 74HC74N
- PRE → VCC
- D → DB8
- CLK → BANKW7
- CLR → RESET/20
- Q → BANKING

IC117B 74HC74N
- PRE → VCC
- D → BANKING
- CLK → GND
- CLR → VCC
- Q → BANKING

BANKING → BANKING/32

IC114B 74HC32N

IC114C 74HC32N

LED-5MM-GREEN LED5 — R31 330R — GND

TODO:

* DRC

The 64 kW address space is split into 8 banks of 8 kW each.

The banking scheme allows page 0 to be swapped for other pages, although since page 0 has special significance, this should probably not be done normally. This leaves 7 banks and 56 kW available for switching.

Decoupling

C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142 0.1uF; C143 1uF; VCC; GND

Title:	cft
Revision:	Rev B
Last Change:	16 Dec 2012 12:04:37
Drawn by:	Alexios
Sheet	21/49
Simulation filename:	memory.v#bank_switch
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

Interrupt Controller

AB[0..15]

DB[0..15]

W/21

SYSDEV/21

RESET/21

R/12

R/24

W/24

SYSDEV/25

RESET/25

Interrupt Status Register

IC130 74HC138N

IC139D 74HC08N

IC132 74HC540N

IRF[0..7]

ISRR

IERW

Decodes addr: 0000 0000 0011 XXnn

LI 1, OUT &003n: enable IERn
LI 0, OUT &003n: disable IERn, acknowledge interrupt
IN &0030-&003F: read from ISR

Interrupt Enable Register

IC136 74HC259N

IEN[0..7]

Front Panel Buffers & Connectors

IC138 74HC541N

IC140 74HC541N

22-23-2081

CON7-1 … CON7-8

CON8-1 … CON8-8

GND

Interrupt registers

IEN[0..7]

IRQ[0..7]

IC129A IC131A IC134A IC135A 74HC112N

IC129B IC131B IC134B IC135B 74HC112N

IRF[0..7]

LED Displays (Optional)

LED-5MM-GREEN

LED6 … LED13

RN17 330R

LED-5MM-RED

LED14 … LED21

RN18 330R

IRQ Generator

IC137A IC137B IC137C IC137D 74HC08N

IC139A IC139B IC139C 74HC08N

IRQ/25

Note: if the Interrupt Controller is installed, IRQ is always driven.
Nothing else may drive IRQ, not even open drain outputs.

Decoupling

C144 … C155 0.1uF

C156 1uF

VCC

GND

TODO:

* DRC

U

NC

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	22/49
Simulation filename: to be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Control Bus Connectors

This sheet intentionally left blank.

U	Title: cft
	Revision: Rev H
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios | 23/49
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Memory (up to 512kW RAM, 512kW ROM)

AB[0..15]
AEXT[0..7]
DB[0..15]
MEM/21
R/22
W/22

AB[0..15]
AEXT[0..7]
DB[0..15]
MEM/42
R/25
W/25

RAM/ROM chip select

AEXT7=0: RAM. AEXT7=0: ROM.

IC141 74HC138N
AEXT6, AEXT7, MEM, VCC, GND
RAMEN0, RAMEN1, ROMEN0, ROMEN1

Low ROM

IC142 29F040
AB0..AB12, AEXT0..AEXT5, DB0..DB7
ROMEN, R, ROMUPG
C164 1uF

High ROM

IC144 29F040
AB0..AB12, AEXT0..AEXT5, DB8..DB15
ROMEN, R, ROMUPG
C166 1uF

Optional LED Display

IC146 74HC540N
LED-5MM-RED LED22 R32 330R
LED-5MM-GREEN LED23 R33 330R
LED-5MM-GREEN LED24 R34 330R
LED-5MM-GREEN LED25 R35 330R

JP9
ROMUPG

Jumper 1-2: normal operation.
Jumper 2-3: allow in-system ROM upgrade.

JP10
ROMEN1
ROMEN
ROMEN0

Jumper 1-2: ROM at &18000-&1FFFF
Jumper 2-3: ROM at &10000-&1FFFF

JP11
RAMEN1
RAMEN
RAMEN0

Jumper 1-2: RAM at &08000-&0FFFF
Jumper 2-3: RAM at &00000-&0FFFF

Low RAM

IC143 AS6C4008
AB0..AB12, AEXT0..AEXT5, DB0..DB7
RAMEN, R, W
C165 1uF

High RAM

IC145 AS6C4008
AB0..AB12, AEXT0..AEXT5, DB8..DB15
RAMEN, R, W
C167 1uF

Decoupling

C157 C158 C159 C160 C161 C162 0.1uF
C163 1uF
VCC, GND

To use RAM instead of ROM (making this a 1MW RAM card), install RAM chips in place of the ROM chips and install a shunt on pins 2-3 of the ROMUPG jumper (or bridge the pins) to allow writing.

TODO:

* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	24/49
Simulation filename: memory.v#memory	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

RS-232 Ports (16C550 UARTs)

DB[0..15]
AB[0..15]
RESET/22
R/24
W/24
SYSDEV/22
RESET/26
R/26
W/26
SYSDEV/26

Open drain inverting buffer configured as NOT gate.

IC148E 74HC05N

R40 4k7

IC147 74HC138N

AB3 AB4 AB5 AB6 AB7 SYSDEV

&0040 &0048 &0050 &0058 &0060 CS0 &0068 CS1 &0070 CS2 &0078 CS3

Addresses Decoding:

0000'0000'0110'XXXX (&006X) -> Chip #0 (UARTs 0, 1)
0000'0000'0111'XXXX (&007X) -> Chip #1 (UARTs 2, 3)

0000'0000'01AA'AXXX = &004X - &007F

IRQ[0..7]
IRQ/22

SV3 SV4

IRQ0 IRQ1 IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ

74HC05N IC148A IC148B IC148C IC148D

R36 4k7 R38 4k7 R37 4k7 R39 4k7

GND

Decoupling

C168 0.1uF C169 0.1uF C170 1uF C171 0.1uF

IC148F 74HC05N

XTAL2 1.8432 MHZ

IC149 IC150 SC16C2550

D7 D6 D5 D4 D3 D2 D1 D0

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

IOR IOW CSA CSB A0 A1 A2 RESET INTA INTB XTAL1 XTAL2

UARTRST INT0 INT1 INT2 INT3

RXRDYA RXA TXRDYA TXA CDA CTSA DSRA RIA RTSA DTRA OP2A RXRDYB RXB TXRDYB TXB CDB CTSB DSRB RIB RTSB DTRB OP2B

RXRDY0 RX0 TXRDY0 TX0 CD0 CTS0 DSR0 RI0 RTS0 DTR0 OPTWO0

RXRDY1 RX1 TXRDY1 TX1 CD1 CTS1 DSR1 RI1 RTS1 DTR1 OPTWO1

RXRDY2 RX2 TXRDY2 TX2 CD2 CTS2 DSR2 RI2 RTS2 DTR2 OPTWO2

RXRDY3 RX3 TXRDY3 TX3 CD3 CTS3 DSR3 RI3 RTS3 DTR3 OPTWO3

C172 1uF C173 1uF

IC151 IC152 IC153 MAX232

C1+ C1- C2+ C2- V+ V- T1IN T2IN R1OUT R2OUT T1OUT T2OUT R1IN R2IN

C174 C175 C176 C177 C178 C179 1uF

C180 C183 C181 C184 C182 C185 1uF

C186 C187 C188 10uF

UART0 UART1 UART2

CON9 CON10 CON11 G1 G2

CD RXD0 TXD0 DTR GND DSR RTS0 CTS0 RI

CD RXD1 TXD1 DTR GND DSR RTS1 CTS1 RI

CD TXD2 RXD2 DTR GND DSR CTS2 RTS2 RI

1M R41 R42 R43

GND DTE DCE EARTH

DB9 male or 2x5 pin header.

DB9 female or 2x5 pin header.

Attention: DCE wiring!

FT232 Serial cable pinout

SV5

CD3 TX3 RX3 RTS3

DTR
RXI (INPUT TTL to USB)
TXO (OUTPUT USB to TTL)
3V3/5V Power input
CTS

TTL (e.g FT232 5V cable)

TODO:

* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	25/49
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

IDE Bus Interface

AB[0..15]
DB[0..15]

R/25
W/25
RESET/25
SYSDEV/25
IRQ/25

R/27
W/27
RESET/28
SYSDEV/27
IRQ/27

Address Decoder (8-port blocks)

IC154 74HC138N

AB4
AB5
AB6
AB7
AB3
SYSDEV

A B C G1 G2A G2B Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

&00AX CS1A
&00BX CS3A
&00CX CS1B
&00DX CS3B

Address Decoding:

0000'0000'1aaa'0XXX

0000'0000'1010'0XXX -> &00A0-A7 Port 1 CS1
0000'0000'1011'0XXX -> &00B0-B7 Port 1 CS3

0000'0000'1100'0XXX -> &00C0-C7 Port 2 CS1
0000'0000'1101'0XXX -> &00D0-D7 Port 2 CS3

IRQ[0..7]

SV6
IRQ5 IRQ6 IRQ7 IRQ

BC548 TR1
4k7 R44
INTA
GND

SV7
IRQ5 IRQ6 IRQ7 IRQ

BC548 TR2
4k7 R45
INTB
GND

DD[0..15]

VCC
RN19 4k7
RN20 4k7

IC155 74HC245N
IC156 74HC245N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8

R
DIR
G
GND

DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7
DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15

CFT-to-IDE bus buffers. Could possibly be replaced with HC parts.
Could possibly be left out altogether, though they protect the CFT
bus from potential problems on the IDE side.

AB[0..15]

CON12 IDE-CONNECTOR
CON13 IDE-CONNECTOR

DAA CS1A CS3A AB0 AB1 AB2 R W INTA RESET
DAB CS1B CS3B AB0 AB1 AB2 R W INTB RESET

DASP CS1FX CS3FX DA0 DA1 DA2 DIOR DIOW DMACK DMARQ INTRQ RESET PDIAG
IOCS16 IORDY CSEL

GND

LED-5MM-RED LED26 R46 330R VCC
LED-5MM-RED LED27 R47 330R VCC
JP12 JP13

For external LEDs (e.g. MISCn on the front panel),
remove jumper shunt and connect pin 1 to external LED.

Decoupling

C189 C190 C191 C192 C193 0.1uF
C194 1uF
VCC
GND

TODO:

* Write & Verify Verilog Model

U

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	26/49
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Six Programmable Counters

Clock, Timers & NVRAM

Real Time Clock & NVRAM

Address Decoder (8-port blocks)

Address Decoder (4-port blocks)

Interrupt Selection Jumpers

Counter Interrupt Enables

Counter Clock Select MUXes

Gate/Output Expansion

32,768 Hz clock

Interrupt Mask Reg

AB[0..15]

DB[0..15]

R/26

W/26

IC158 74HC138N

IC160 74HC374N

IC161 74HC138N

IC162 74HC374N

IC163 74HC374N

IC164A 74HC32N

IC164B 74HC32N

IC164C 74HC32N

IC164D 74HC32N

IC166C 74HC02N

IC166D 74HC02N

IC165A 74HC02N

IC165B 74HC02N

IC165C 74HC02N

IC165D 74HC02N

IC166A 74HC02N

IC166B 74HC02N

74HC02N

IC167 M48T02

C213 1uF

D1 1N5817-B

IC170 82C54

IC171 82C54

IC168 74HC153N

IC169 74HC153N

RN21 4k7

SV10

SV11

IRQ[0..7]

IRQ/26

SV8

SV9

IC159A 74HC05N

IC159B 74HC05N

IC159C 74HC05N

IC159D 74HC05N

IC159E 74HC05N

IC159F 74HC05N

INTA0

INTA1

INTA2

INTB0

INTB1

INTB2

C195 1uF

C196 0.1uF

C197 0.1uF

C198 0.1uF

C199 0.1uF

C200 0.1uF

C201 0.1uF

C202 0.1uF

C203 0.1uF

C204 0.1uF

C205 0.1uF

C206 0.1uF

C207 0.1uF

C208 0.1uF

C209 0.1uF

C210 0.1uF

IC157A 74HC14N

R48 10M

R49 300k

XTAL3 32.768kHz

C211 22pF

C212 22pF

32KHZ

IC157B 74HC14N

IC157C 74HC14N

IC157D 74HC14N

IC157E 74HC14N

IC157F 74HC14N

SYSDEV/26

Addresses Decoding:

0000'0000'1000'XXXX (&008X) -> 16 bytes of NVRAM/clock data

0000'0000'1001'00xx (&0090-93) -> NVRAM addr offset (bits 4-10). Clock = &7F

0000'0000'1001'01xx (&0094-97) -> Timer #1

0000'0000'1001'10xx (&0098-9B) -> Timer #2

0000'0000'1001'11xx (&009C-9F) -> Timer Control Register (16 bits)

TODO:

* DRC

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	27/49
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

U

CLK1/7

CFT Mini-Computer

Ethernet Interface (WIZ5100 module)

DB[0..15]

AB[0..15]

R/27

W/27

RESET/26

SYSDEV/27

IRQ/27

R/29

W/29

RESET/29

SYSDEV/29

IRQ/29

Address Decoder (8-port blocks)

IC172 74HC138N

AB4 AB5 AB6 AB7 AB3 SYSDEV

&00AX &00BX &00CX &00DX &00EX &00FX

Address Decoding:

0000'0000'1aaa'0XXX

0000'0000'1110'0XXX -> &00E0-EF Read/Write data (4 regs, 4 copies)

IC173 74HC245N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

R

GND

The '245 may be unnecessary.
The databus buffers are also HCT
so they are 3.3V input tolerant.

Q1 WIZ812MJ

RESET CS W R SCLK SCS MOSI MISO INT RXLED TXLED LINKLED

3V3A 3V3B GND2 GND1

+3V3

AB0 AB1 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14

D0 D1 D2 D3 D4 D5 D6 D7

Optional LED indicators

LED-5MM-GREEN LED29 R53 330R

LED-5MM-RED LED30 R54 330R

LED-5MM-GREEN LED28 R55 330R

JP14 JP15 JP16

VCC

GND

IRQ[0..7]

SV12

IRQ5 IRQ6 IRQ7 IRQ

4k7 R50

BC548 TR3

GND

Optional power supply (if 3V3 supply unavailable)

+12V

D2 1N4002

+3V3

LM317T IC174

IN OUT ADJ

C223 0.1uF

R52 240R

C224 0.1uF

R51 390R

GND

Decoupling

VCC

C214 C215 C216 C217 C218 C219 C220 C221 0.1uF

C222 1uF

GND

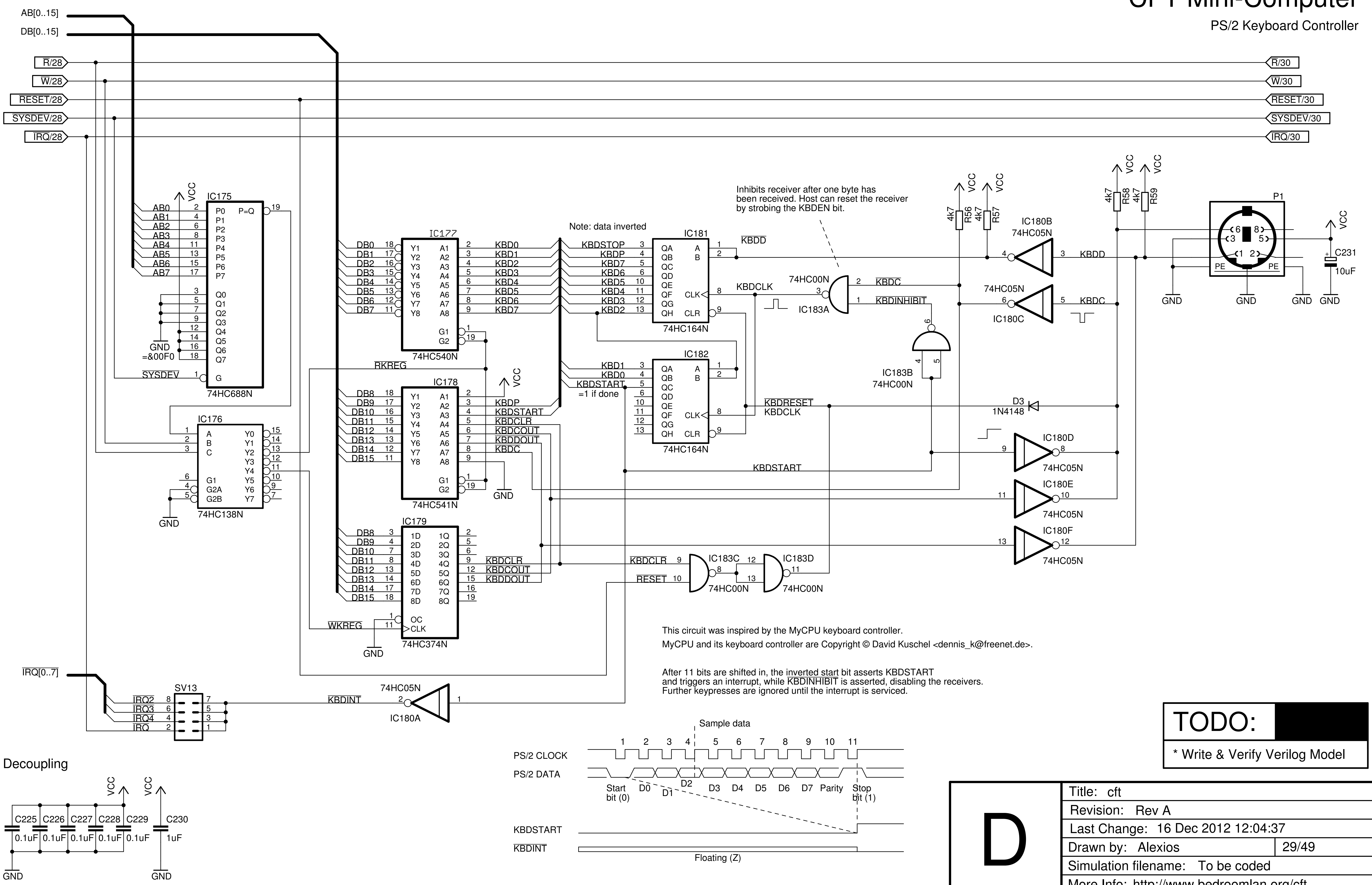
TODO:

* Write & Verify Verilog Model
* DRC

D	Title: cft
	Revision: Rev A
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios — 28/49
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

PS/2 Keyboard Controller



This circuit was inspired by the MyCPU keyboard controller.

MyCPU and its keyboard controller are Copyright © David Kuschel <dennis_k@freenet.de>.

After 11 bits are shifted in, the inverted start bit asserts KBDSTART and triggers an interrupt, while KBDINHIBIT is asserted, disabling the receivers. Further keypresses are ignored until the interrupt is serviced.

TODO:

* Write & Verify Verilog Model

D

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	29/49
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Audio Device 1 of 2 (Bus Interface & SpeakJet)

RESET/29
W/29
R/29
SYSDEV/29
IRQ/29
DB[0..15]
AB[0..15]

RESET/31
W/41
R/41
SYSDEV/41
IRQ/44
PSGW/31
IRQ[0..7]

R/W Bus Interface

IC185 74HC138N SJ/PSG
AB4 AB5 AB6 AB3 AB7 SYSDEV
&008a &009a &00Aa &00Ba &00Ca &00Da &00Ea &00F0-&00F3

IC186 74HC138N SJ/PSG
AB0 AB1 AB2 VCC SNDCS W
PSGW OUT &F0
SJW OUT &F1
SJCRW OUT &F2

IC187 74HC138N SJ
AB0 AB1 AB2 VCC SNDCS R
SJCRR IN&F2

SpeakJet Registers

IC188 74HC174N SJ
DB0 DB1 DB2 DB3 DB4 DB5
SJRST SJM0 SJM1 SJIRQEN
SJCRW RESET
OUT &F2

IC189 74HC574N SJ
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15
SJE0 SJE1 SJE2 SJE3 SJE4 SJE5 SJE6 SJE7
SJCRW
OUT &F2

IC190 74HC541N SJ
SJRDY SJSPK SJBHF SJCE
SJCRR
IN &F2

Interrupt Generator

IC192D 74HC00N SJ
SJIRQEN SJCE

IC195D 74HC04N
Spare NOT gate from next sheet.

R62 10k
TR4 BC548
R63 680R
GND

SV14 SJ
IRQ IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 IRQ2 IRQ1 IRQ0

IC193 74HC166N SJ
Stop bit DB7
SJCE SJCLK SJW SJRST

IC194 74HC166N SJ
DB6 DB5 DB4 DB3 DB2 DB1 DB0 Start bit
SJCE SJCLK SJW SJRST

SJ = Necessary for SpeakJet.
SJ/PSG = Necessary for both SpeakJet and PSG.

SpeakJet Chip

IC196 SPEAKJET SJ
SJRST SJDATA SJE0 SJE1 SJE2 SJE3 SJE4 SJE5 SJE6 SJE7 SJM0 SJM1
RST VOUT RCX E0 E1 E2 E3 E4 E5 RC0/E6 RC1/E7 M0 M1
D0/RDY D1/SPK D2/BHF
SJRDY SJSPK SJBHF
0.1uF C246 GND

Two-Pole High-Pass Filter

R64 27k
R65 27k
0.1uF C247
0.1uF C248
C249 10uF
R66 50k log
SJAUDIO/31
GND

Serial Transmitter

9.6 kHz Serial Clock

IC184 LM555N SJ
R60 560R
R61 470R
9620 Hz, 68.7% duty cycle
C237 0.1uF
C241 0.01uF
C245 0.1uF
SJW SJCLK

Serial Transmission State Machine

IC191 74HC193N SJ
0110 = 6
SJW SJCLK
IC192C 74HC00N
IC192B IC192A 74HC00N SJ

Decoupling

C232 C233 C234 C235 C236 C238 C239 C240 C242 C243 0.1uF
C244 1uF
VCC GND

SJCLK
RCX b0 b1 b2 b3 b4 b5 b6 b7
1 8 data bits (non-inverted) 0
SJRTS
SJIRQ

Title:	cft
Revision:	Rev A
Last Change:	16 Dec 2012 12:04:37
Drawn by: Alexios	30/49
Simulation filename:	N/A
More Info:	http://www.bedroomlan.org/cft

D

CFT Mini-Computer

Audio Device 2 of 2 (GI AY-3-8910 PSG)

RESET/30
CLK1/27
SJAUDIO/30
RESET/44
CLK1/43

BDIR	BC2	BC1	Action
0	1	0	Inactive (Z)
0	1	1	Read (not used)
1	1	0	Write to register
1	1	1	Select register *

* For reg select, DB4-DB7 MUST be 0000 (chip select)
BC1 = DB8 (software control via OUT)
A8, $\overline{A9}$ are chip select signals (A8$\overline{A9}$=01 to select).

Notes

The PSG has a minimum transaction period of 500ns (2 CFT cycles @ 16 MHz)
We don't use wait states, but we buffer & delay data for three clock ticks. Depending on CFT latency, this makes for a period of 570-750ns.

For simplicity, the PSG is attached write-only. This simplifies interfacing to its unusual control signals.

The two 8910 I/O ports must be configured as outputs (because tey can't be read by the CPU), and are brought out for use as 16 user output ports.

To write to a PSG register, first write to port &00F0-&00FF with the reg number (0..15) OR &0100. Then write 8-bit data with the ninth bit clear.

16-bit User Output

SV16: PSGO0 PSGO1 PSGO2 PSGO3 PSGO4 PSGO5 PSGO6 PSGO7 PSGO8 PSGO9 PSGO10 PSGO11 PSGO12 PSGO13 PSGO14 PSGO15

PSG Delay Line

IC197 74HC174N: CLK1, PSGW/30, PSGW, PSGCS
IC195F 74HC04N

Data Register

IC198 74HC574N: DB[0..15], DB0–DB7, PSGW, PSGCS, DB8

AY-3-8910

IC199: RESET, PSGCLK, PSGW, BDIR, BC2, DB8, A8, $\overline{A9}$, PSGCS
CHANNEL-A, CHANNEL-B, CHANNEL-C
IOA0–IOA7 → PSGO0–PSGO7
IOB0–IOB7 → PSGO8–PSGO15
DA0–DA7

C256 0.1uF

ABC Stereo mixer

R69 1k, R70 2k2, R71 2k2, R72 1k
C257 1uF, C258 1uF
R74 2k2, R75 2k2
LEFT-IN, RIGHT-IN
SV15: LEFT, LEFT-IN, RIGHT-IN, RIGHT
X2: 1503_09
GND GND
3.5mm audio jack on rear or front panel.
Two shielded stereo cables.

R77 1k, R78 1k
SJAUDIO

Note: SJAUDIO is 5V PTP (probably totem-pole PWM). this circuit may need adjustment.

Left Amplifier

IC201 LM386N-1
C261 10uF, C263 220uF, C262 47nF
C259 0.1uF, C260 0.1uF, R76 10R
10k log R73/1

Right Amplifier

IC202 LM386N-1
C266 10uF, C268 220uF, C267 47nF
C264 0.1uF, C265 0.1uF, R79 10R
10k log R73/2
SV17: L-SPK, R-SPK
Shielded stereo cable.

SP1 AL11P — Left speaker, 8 Ohm.
SP2 AL11P — Right speaker, 8 Ohm
Amplified speakers in computer case.

TODO:

* Write & Verify Verilog Model
* DRC

Decoupling

C250 0.1uF, C251 0.1uF, C252 0.1uF, C253 0.1uF, C254 1uF

1/2 MHz Clock

XTAL4 4MHz
10M R67, R68 330R, C255 0.1uF
IC195A, IC195B, IC195C, IC195E 74HC04N
IC200A, IC200B 74HC74N
1MHZ, 2MHZ
JP17
1-2: 2 MHz clock
2-3: 1 MHz clock (default)

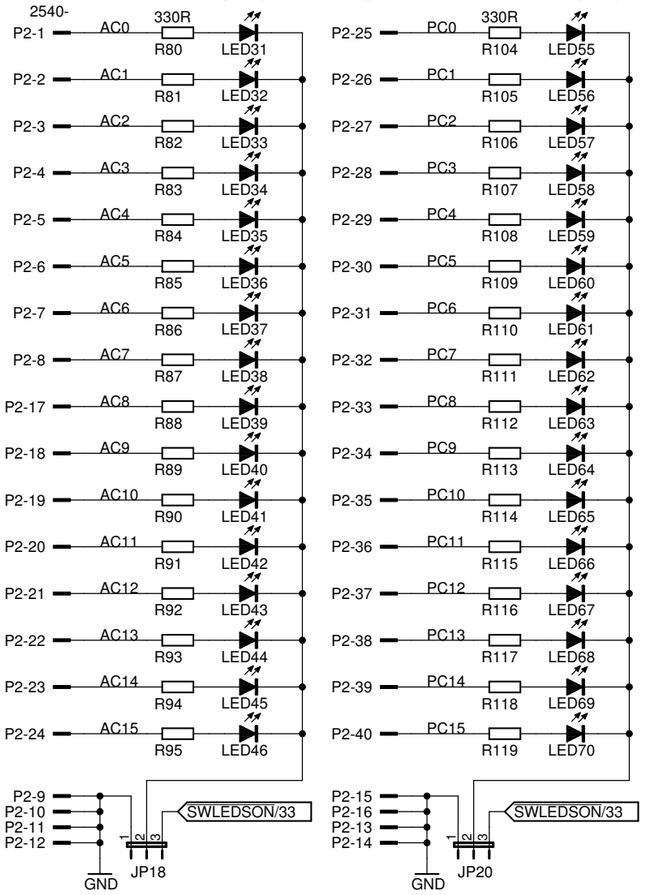
Title:	cft
Revision:	Rev B
Last Change:	16 Dec 2012 12:04:37
Drawn by:	Alexios
Simulation filename:	N/A
More Info:	http://www.bedroomlan.org/cft

D — 31/49

CFT Mini-Computer

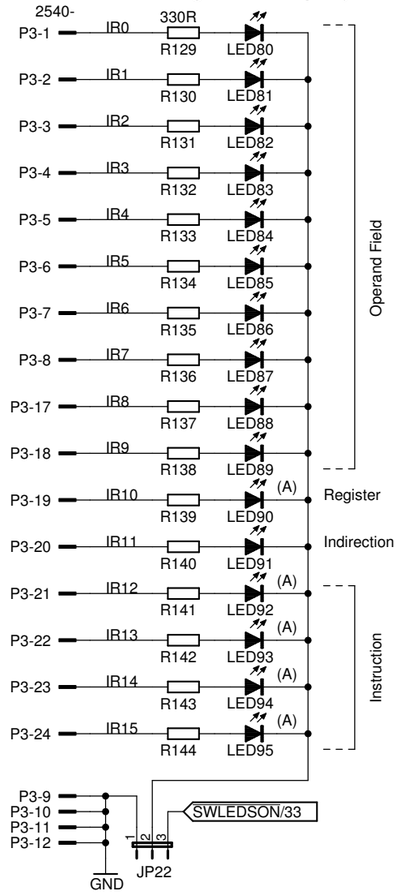
Front Panel: LED board

Accumulator Display

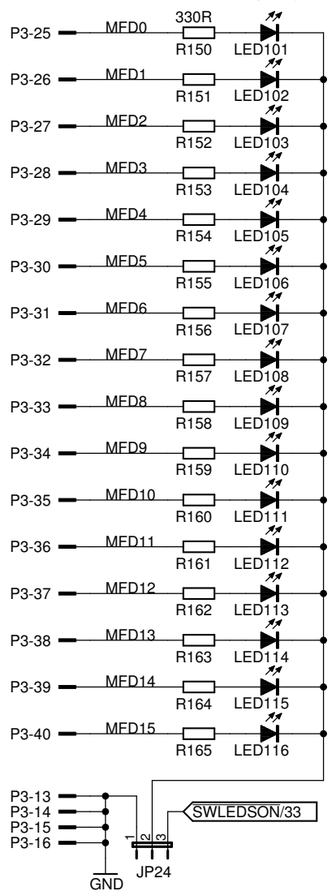


Program Counter Display

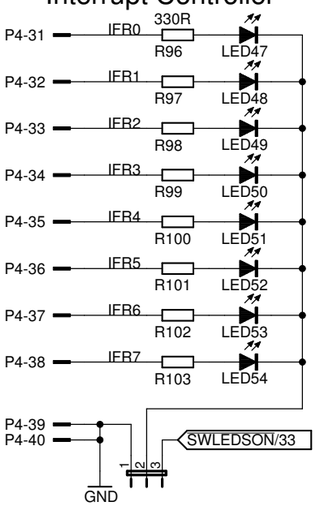
Instruction Register Display



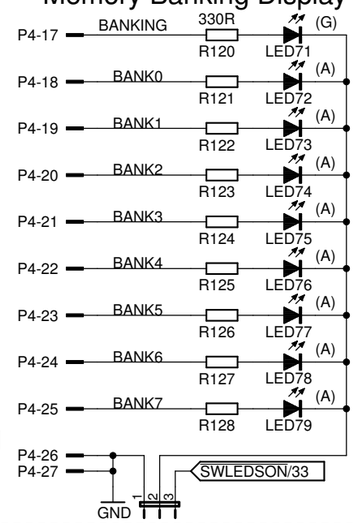
Multi-Function Display



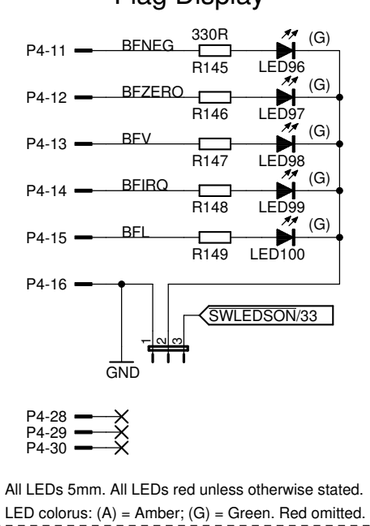
Interrupt Controller



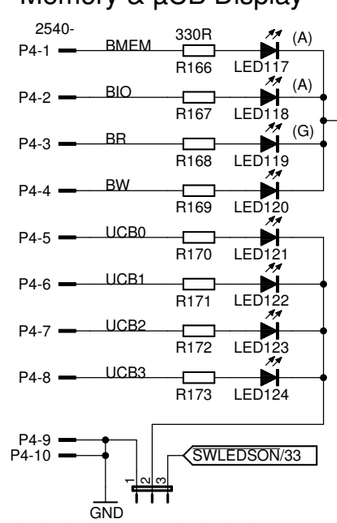
Memory Banking Display



Flag Display



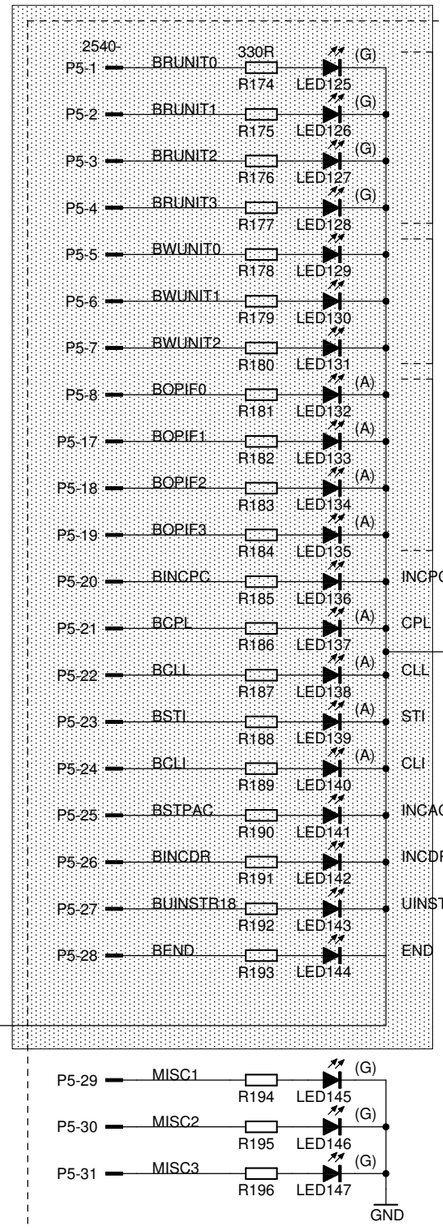
Memory & µCB Display



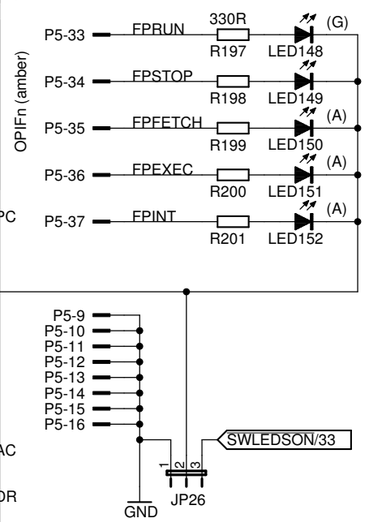
All LEDs 5mm. All LEDs red unless otherwise stated.

LED colorus: (A) = Amber; (G) = Green. Red omitted.

Front Panel LEDs



State Display



TODO:

* DRC

Title: cft	
Revision: Rev C	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	32/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

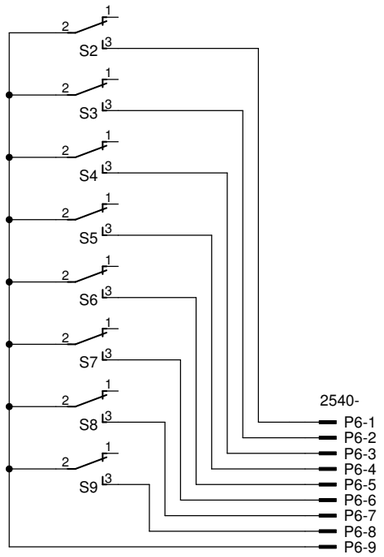
U

CFT Mini-Computer

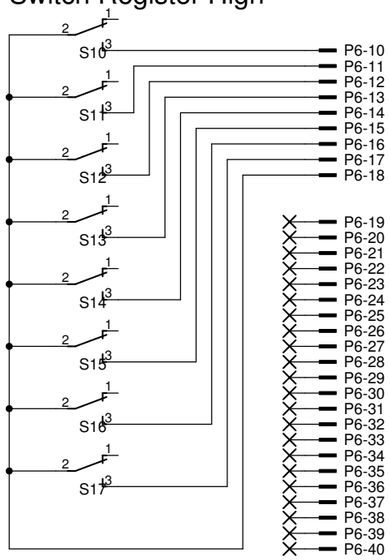
Front Panel: Switch board

Informational & Override Switches (FPLOCK lock-out)

Switch Register Low



Switch Register High

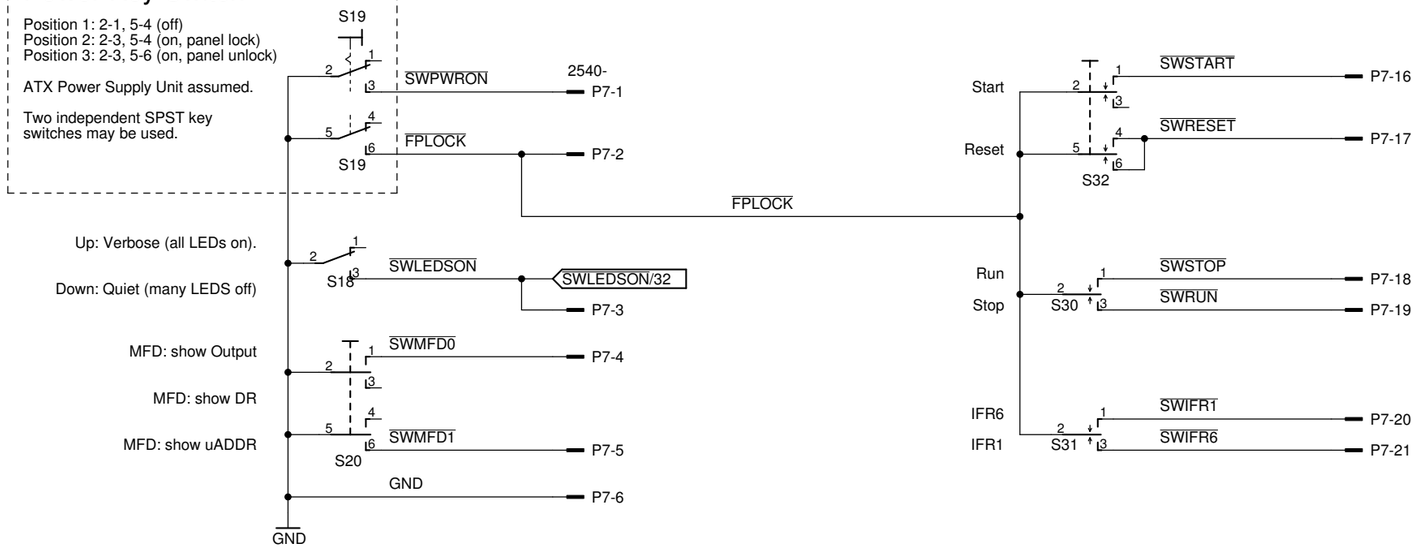


Power Key Switch

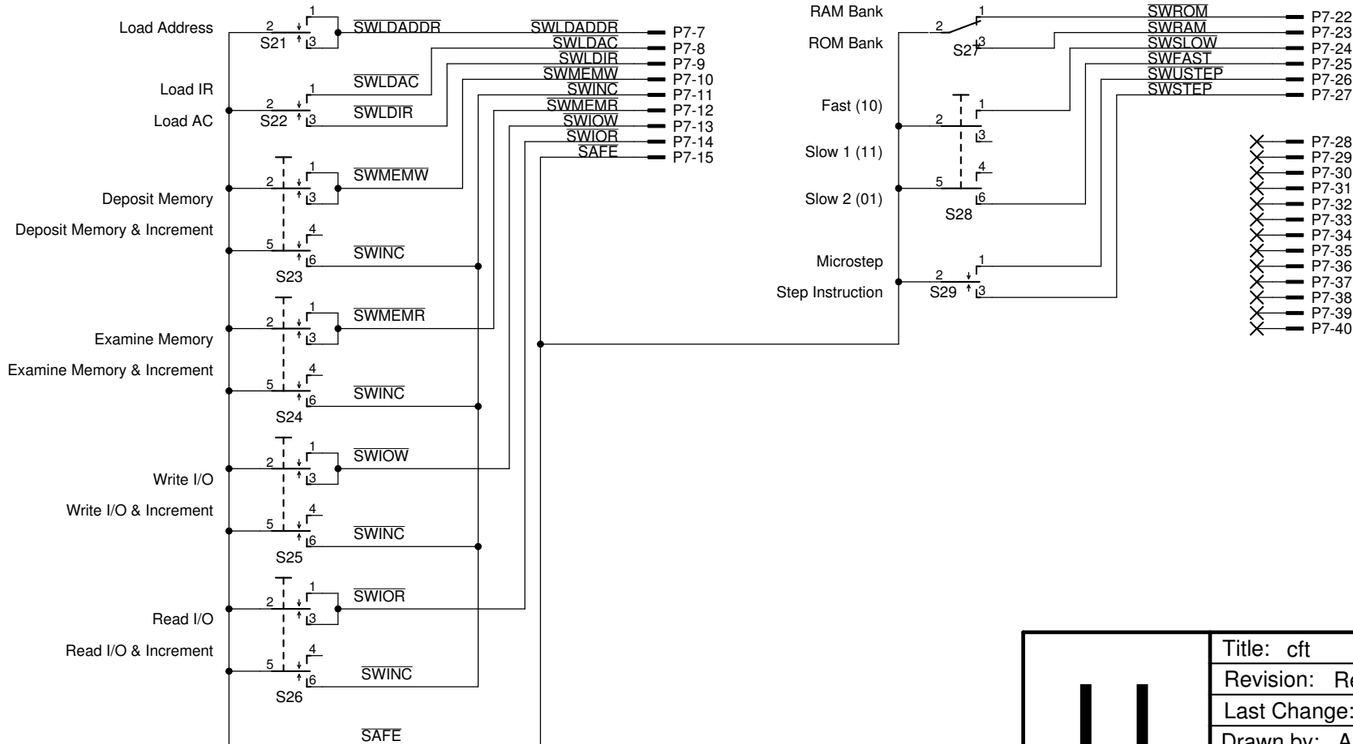
Position 1: 2-1, 5-4 (off)
Position 2: 2-3, 5-4 (on, panel lock)
Position 3: 2-3, 5-6 (on, panel unlock)

ATX Power Supply Unit assumed.

Two independent SPST key switches may be used.



Debugging Switches (SAFE lock-out)



TODO:

* DRC

U	Title: cft
	Revision: Rev D
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios — 33/49
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Front Panel: Switch Register and Switches 1/2

FPCLKEN/6

FPCLKEN/43

IC205A
74HC04N

VCC

RN22 10k

Power Key Switch

Position 1: 2-1, 5-4 (off)
Position 2: 2-3, 5-4 (on, panel lock)
Position 3: 2-3, 5-6 (on, panel unlock)

ATX Power Supply Unit assumed.

S33

GND

Keeps power on when a break-before-make key switch moves between ON & PANEL positions.

C278 1uF

C279 1uF

GND

FPPWRON/40 — Activates the Power Supply Unit, turning the computer on.

FPLOCK/36 — Disables the panel switches.

FPLEDSON/37 — Disables many debugging lights to avoid visual overload.

Verbose / Quiet — S34

ROM High / RAM High — S35

FPROM/40

FPRAM/40

FPROM & FPRAM are not debounced because they are handled off-board by a clocked J-K flip-flop.

Fast (10) / Slow 1 (11) / Slow 2 (01) — S36

C274 +1uF

RN23A 50k

IC203A 74HC14N

IC205B 74HC04N

IC206
74HC373N
1D 2D 3D 4D 5D 6D 7D 8D → 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
OC, ENC

FPFAST/40

Fast: FPFAST=1, FPSLOW=0
Slow 1: FPFAST=0, FPSLOW=0
Slow 2: FPFAST=0, FPSLOW=1

RN23B 50k

C275 1uF

IC203B 74HC14N

IC205C 74HC04N

FPSLOW/40

Clock speed latch: clock speed may be changed only when the clock is stopped (CLKEN is high)

SAFE

C276 +1uF

RN23C 50k

RN23D 50k

C277 1uF

IC203C 74HC14N

IC205D 74HC04N

FPSTEP-IN FPSTEP

FPSTEP/35

Install shunt if auto-repeat circuit is absent/disabled.
Auto-repeat circuit plugs into jumper header.
Another two pins needed for daughterboard (Vcc, GND).

JP27

Microstep / Step Instruction — S37

FPSTEP-IN/35

IC203D 74HC14N

IC204B 74HC03N Open drain

FPUSTEP/40

GND

Some Schmitt trigger gates shared with sheet after next.

Switches:

16x On-Off / On-On / On-None-Off / On-None-On
2x On-None-On / On-On
1x On-Off-On DP
1x (On)-Off-(On)

SAFE

SAFE/33

Decoupling

VCC

C269 0.1uF
C270 0.1uF
C271 0.1uF
C272 0.1uF
C273 1uF

GND

IC205E 74HC04N

IC205F 74HC04N

GND

TODO:

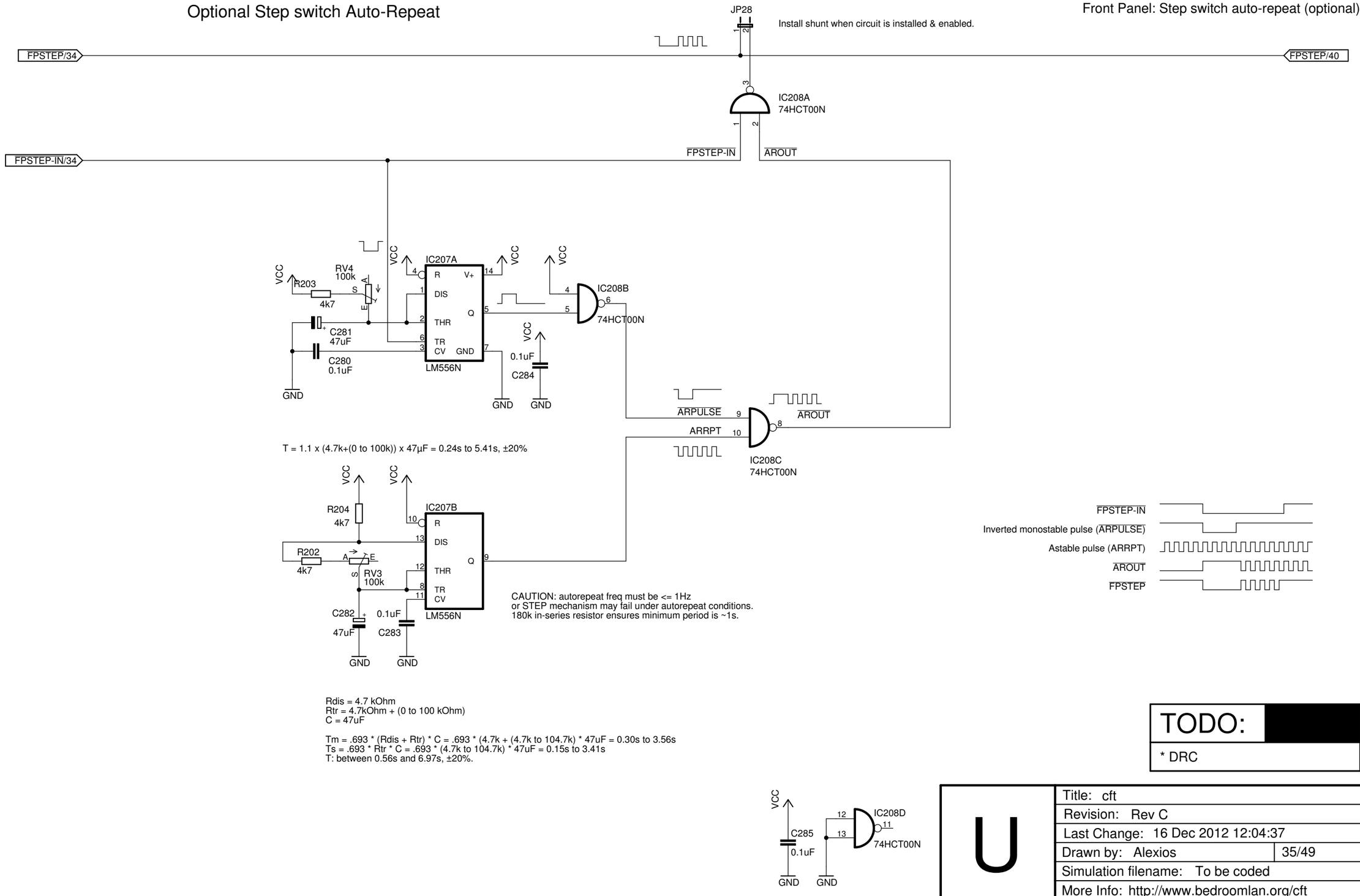
* DRC

Title: cft	
Revision: Rev B	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	34/49
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Optional Step switch Auto-Repeat

Front Panel: Step switch auto-repeat (optional)



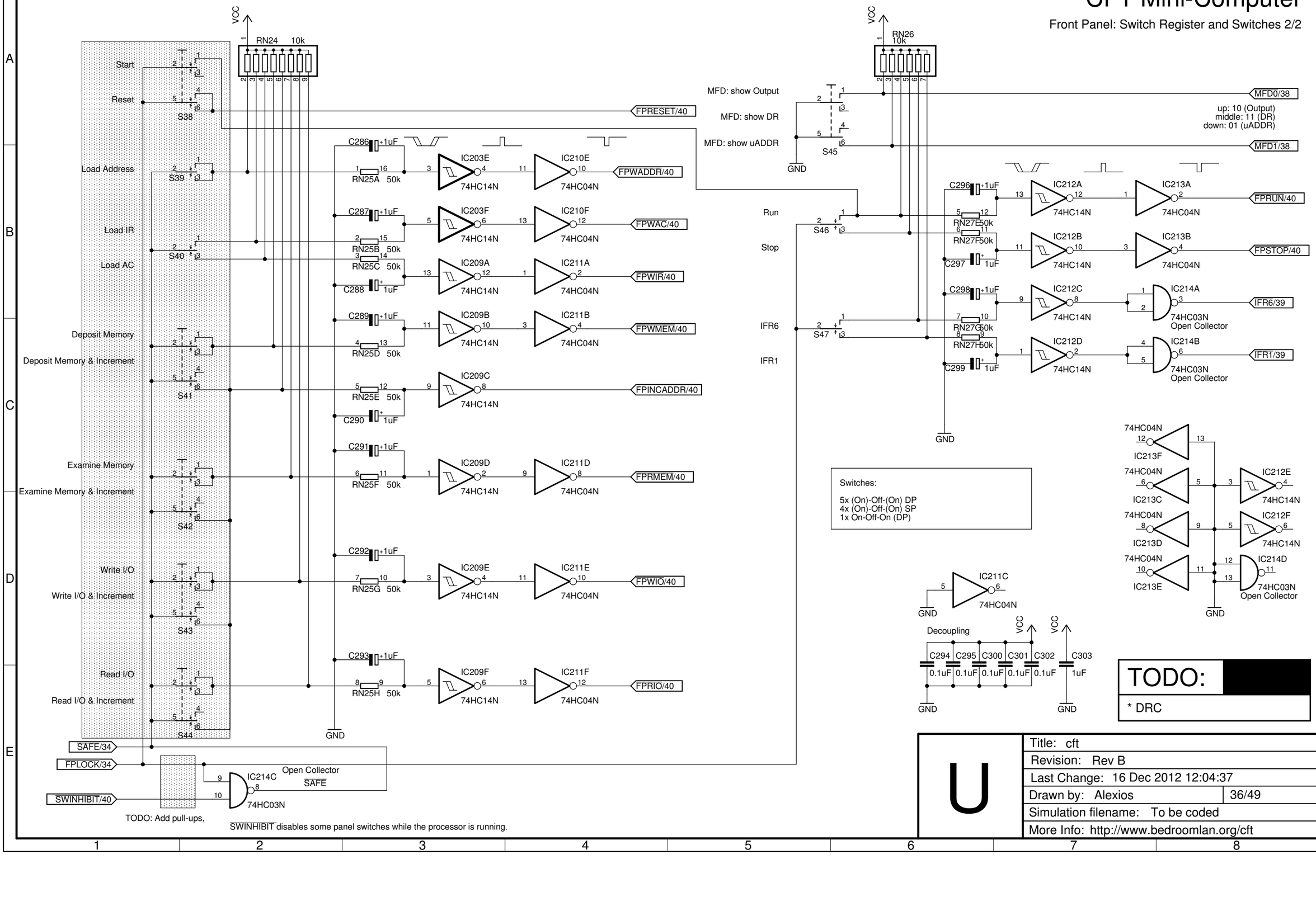
TODO:

* DRC

U	Title: cft
	Revision: Rev C
	Last Change: 16 Dec 2012 12:04:37
	Drawn by: Alexios — 35/49
	Simulation filename: To be coded
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Front Panel: Switch Register and Switches 2/2



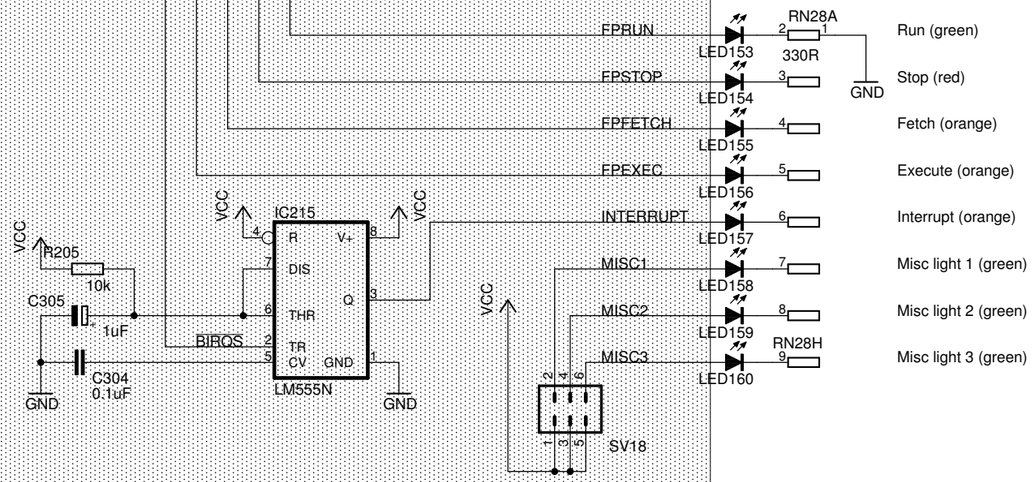
CFT Mini-Computer

Front Panel: LEDs 2

FPLEDSON/34
FPRUN/32
FPSTOP/32
FPFETCH/32
FPEXEC/32
BIRQS/6

FPLEDSON/39
FPRUN/40
FPSTOP/40
FPFETCH/38
FPEXEC/38
BIRQS/38

State & Miscellaneous lights

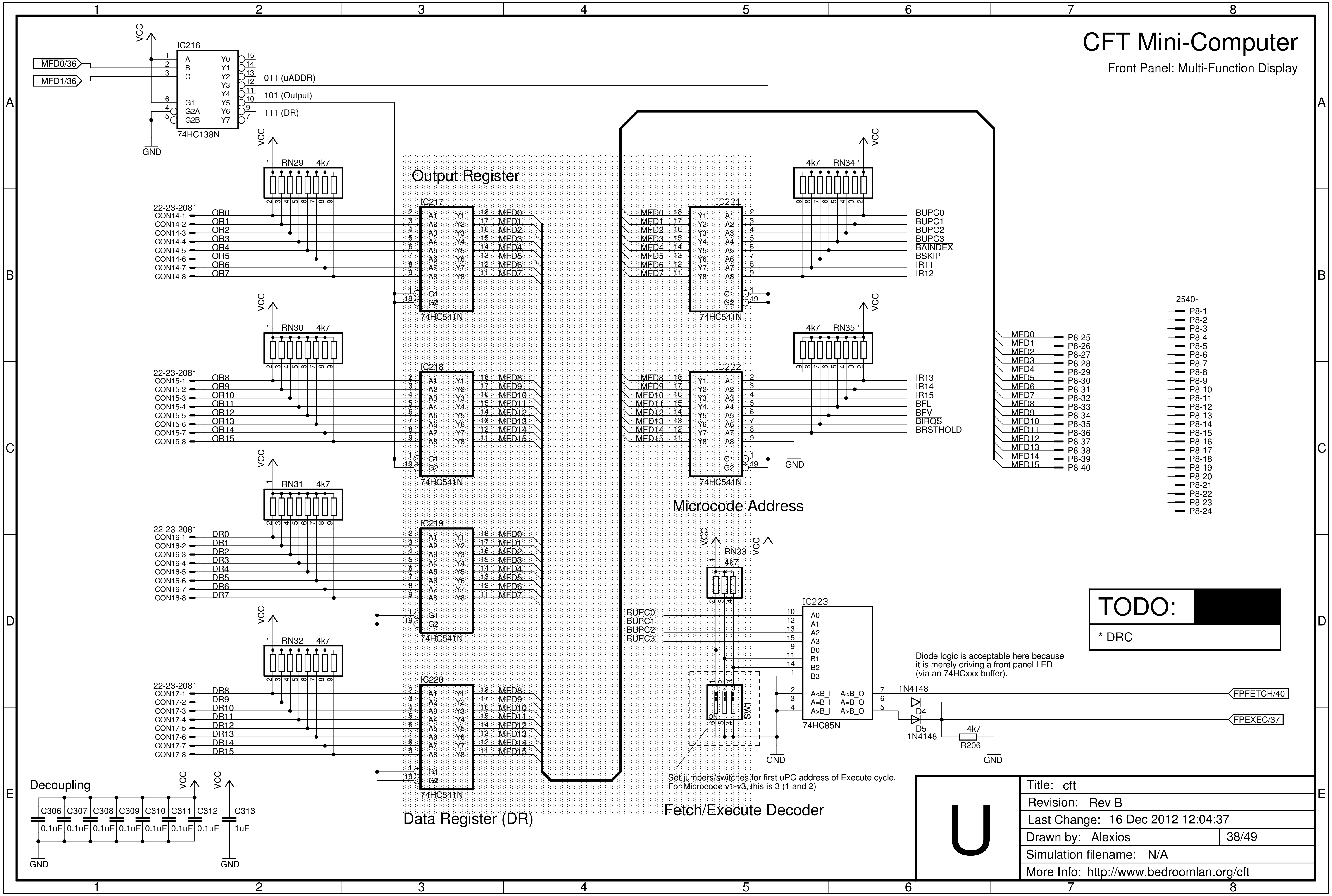


TODO:

* DRC

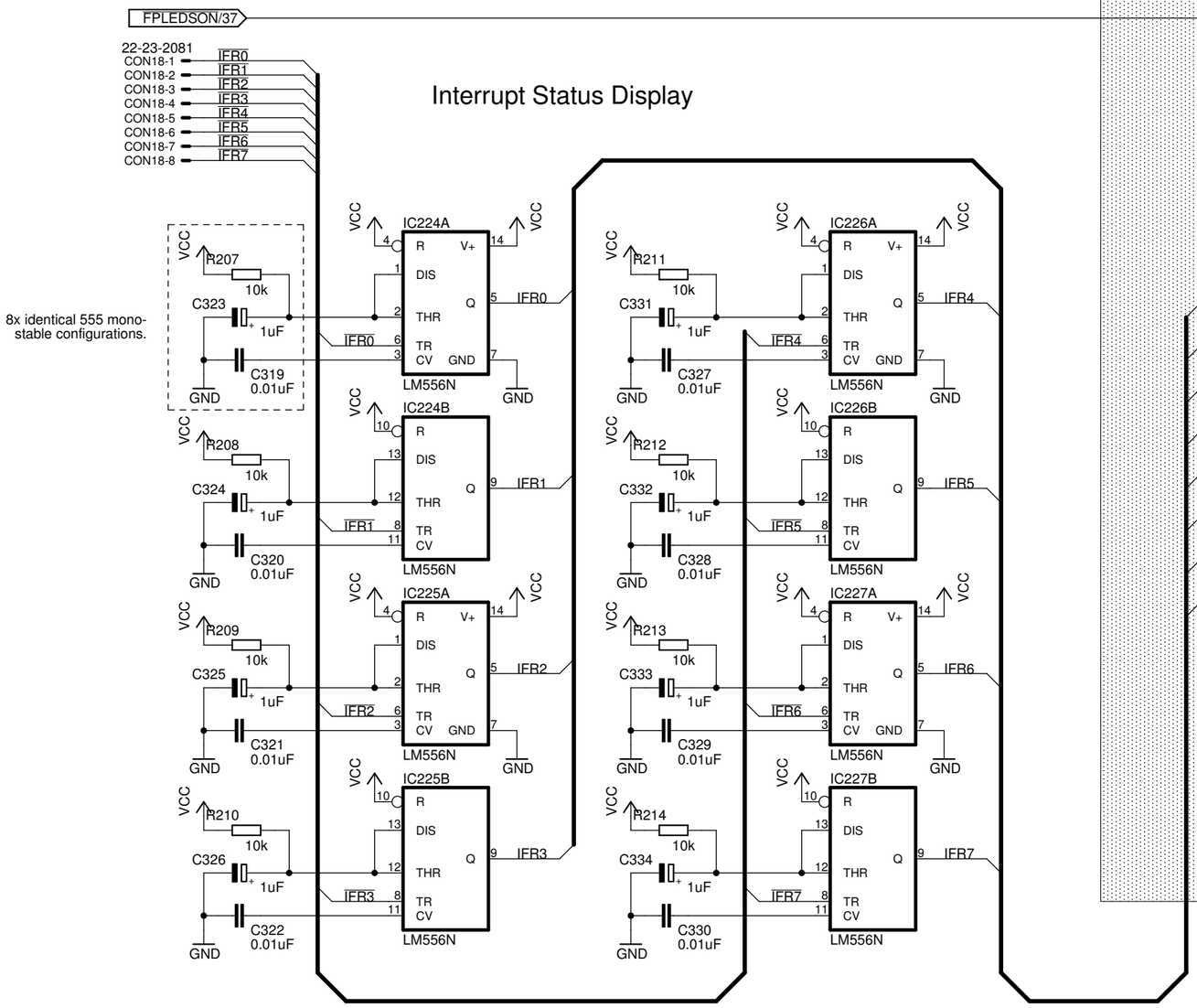
U

Title: cft	
Revision: Rev B	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	37/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

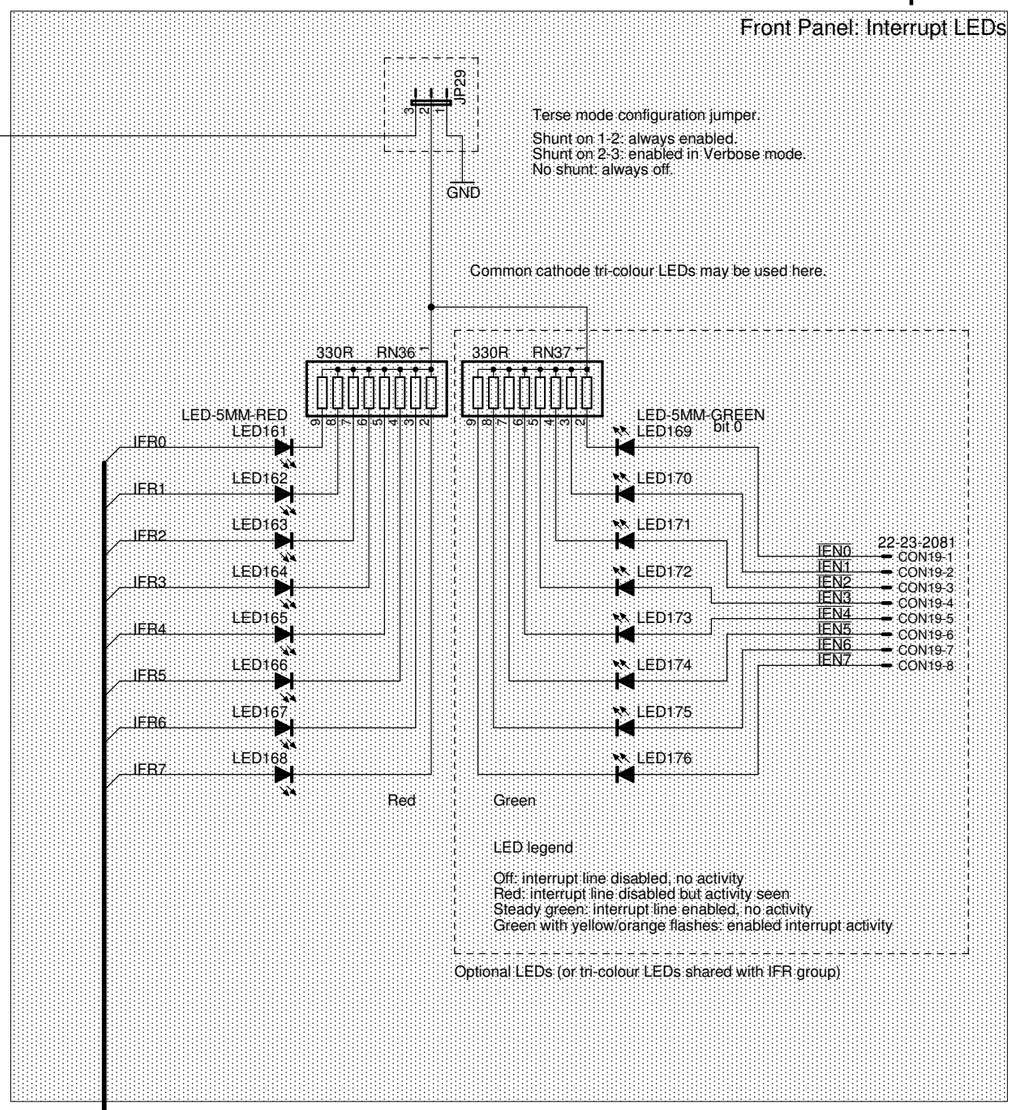

CFT Mini-Computer
Front Panel: Multi-Function Display
IC216
74HC138N
MFD0/36
MFD1/36
011 (uADDR)
101 (Output)
111 (DR)
Output Register
IC217 74HC541N
IC218 74HC541N
IC219 74HC541N
IC220 74HC541N
RN29 4k7
RN30 4k7
RN31 4k7
RN32 4k7
22-23-2081
OR0 OR1 OR2 OR3 OR4 OR5 OR6 OR7
OR8 OR9 OR10 OR11 OR12 OR13 OR14 OR15
DR0 DR1 DR2 DR3 DR4 DR5 DR6 DR7
DR8 DR9 DR10 DR11 DR12 DR13 DR14 DR15
Data Register (DR)
Microcode Address
IC221 74HC541N
IC222 74HC541N
RN34 4k7
RN35 4k7
BUPC0 BUPC1 BUPC2 BUPC3 BAINDEX BSKIP IR11 IR12
IR13 IR14 IR15 BFL BFV BIRQS BRSTHOLD
2540-
P8-1 … P8-40
Fetch/Execute Decoder
IC223 74HC85N
RN33 4k7
SW1
FPFETCH/40
FPEXEC/37
1N4148 D4
D5 1N4148
4k7 R206
Diode logic is acceptable here because it is merely driving a front panel LED (via an 74HCxxx buffer).
Set jumpers/switches for first uPC address of Execute cycle. For Microcode v1-v3, this is 3 (1 and 2)
TODO:
* DRC
Decoupling
C306 C307 C308 C309 C310 C311 C312 0.1uF
C313 1uF
VCC
GND
Title: cft
Revision: Rev B
Last Change: 16 Dec 2012 12:04:37
Drawn by: Alexios
38/49
Simulation filename: N/A
More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

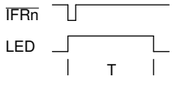
Interrupt Status Display



Front Panel: Interrupt LEDs

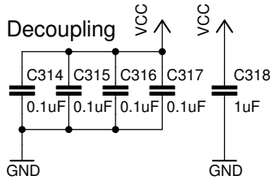


IFRn pulses are not normally visible to the naked eye.
Eight identical '555 (or four '556) monostable vibrators produce visible light pulses.



T = 1.1 x R x C

R=10k, C=1uF: ~0.011s



TODO:

* DRC

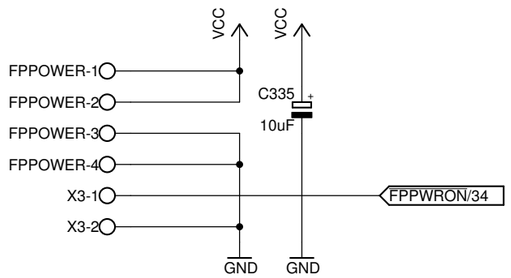
U

Title: cft	
Revision: Rev C	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	39/49
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

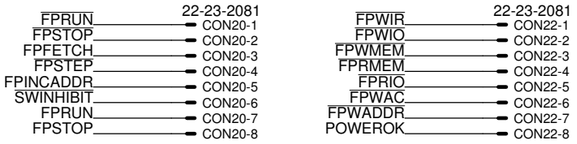
Front Panel: Connectors

Front Panel Power Input



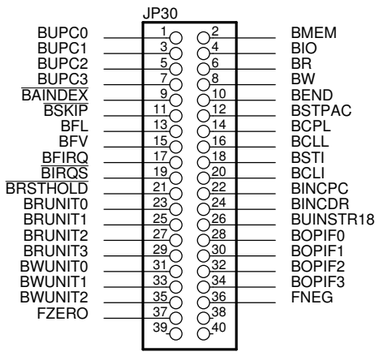
Assumes ATX power supply.

Front Panel Controller Connections

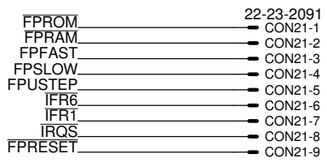


Connector to Front Panel Controller Card.

Sequencer



Connections to Other Cards



TODO:

* DRC

U

Title: cft	
Revision: Rev B	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	40/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: System Device

AB[0..15]
DB[0..15]
AB[0..15]
DB[0..15]

FPWADDR/40
FPWAC/40
FPWIR/40
FPWMEM/40
FPWIO/40
R/30
W/30

FPWADDR/42
FPWAC/42
FPWIR/42
FPWMEM/42
FPWIO/42
R/42
W/44

IC228
74HC138N
Decodes I/O 0008-000F
AB4
AB5
AB6
AB3
AB7
SYSDEV/30

IC231
74HC138N
AB0
AB1
AB2
R
IN &0008
IN &0009 (dip switches)

IC232
74HC138N
AB0
AB1
AB2
W
OUT &000A (OR)
OUT &000F (HALT)
FPHALT/43

IC235A
74HC21N
IC235B
74HC21N
VCC

RN38 4k7
RN39 4k7
RN40 4k7
RN41 4k7

Dip Switch Register (optional)

Output Register

Switch Register

DB[0..15]

Bit 0
Bit 7
SW2
Bit 8
Bit 15
SW3
GND

IC229
74HC541N
IC230
74HC541N
TP20

IC233
74HC574N
IC234
74HC574N

CON25-1
CON25-2
CON25-3
CON25-4
CON25-5
CON25-6
CON25-7
CON25-8
CON26-1
CON26-2
CON26-3
CON26-4
CON26-5
CON26-6
CON26-7
CON26-8

IC236
74HC541N
IC237
74HC541N
TP22

Decoupling

C336 C337 C338 C339 C340 C341 C342 C343 C344 C345 0.1uF
C346 1uF
VCC
GND

TODO:

* DRC

U

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	41/49
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Sequencer

FPINCADDR/40
FPRMEM/40
FPRIO/40
FPWADDR/41
FPWAC/41
FPWIR/41
FPWMEM/41
FPWIO/41
FPRUN/40

The '125 buffers act as purposefully slow open collector buffers. When the FP input is high, the buffer is tri-stated. When it is low, the buffer drives, but only low (inputs connected to GND). In addition, the tPZL delay (typical 15ns) acts as a delay circuit that gives time for the switch register enables to be decoded and the switch register value put on the IBUS.

FPWADDR
FPWAC
FPWIR

IC244A 74HC125N → WPC/14
IC244C 74HC125N → WDR/15
IC244D 74HC125N → WAC/16
IC245A 74HC125N → WIR/10

VCC
IC245C 74HC125N
FPRUN
R215 4k7
GND
Configured as a NOT gate.

IC238A 74HC21N
IC239B 74HC00N
IC239A 74HC00N
IC239D 74HC00N
IC239C 74HC00N

IC244B 74HC125N
R217 4k7
FPIO
FPMEM
FPR
FPW

These ICs receive input from the 556 chips and must be TTL compatible.

MCSTART
FPRUN

Sequencer

MCSTART
MC0
MC1
MC2
MC3

Write Cycle

MCSTART
WAR
RPC
MEM / IO, INCPC
RAC
WEN

Note: Due to the WEN to W conversion, numerous W strobes will be generated. This is OK for RAM, bad for some I/O (e.g. shift regs)

Read Cycle

MCSTART
WAR
RPC
MEM / IO, INCPC
R
WAC

IC240A LM556N
R218 4k7
C362 1uF
C358 0.01uF
T = 1.1 x 4.7k x 1u = 0.00517s
MC0

IC240B LM556N
R219 10k
C363 1uF
C359 0.01uF
T = 1.1 x 10k x 1u = 0.011s
MC1

Configured as a NOT gate.
IC245D 74HC125N
R216 4k7

IC241A LM556N
R220 4k7
C364 1uF
C360 0.01uF
MC2

IC241B LM556N
R221 10k
C365 1uF
C361 0.01uF
MC3

IC242A 74HCT00N
IC242B 74HCT00N
IC242C 74HCT00N
IC242D 74HCT00N
IC243A 74HCT00N
IC243B 74HCT00N
IC243C 74HCT00N
IC243D 74HCT00N

IC246 74HC541N
MEM/44
IO/44
R/44
WEN/12
INCPC/14
RPC/14
WAR/13
RAC/16

IC245B 74HC125N
WAC

As long as the processor is halted and the control unit tri-stated, the front panel controller will not introduce contention. Also, contention between the FPWAC signal and cycle sequencer cannot happen because even if multiple switches are operated simultaneously, WAC is either tri-stated or driven low.

Decoupling

C347 C348 C349 C350 C351 C352 C353 C354 C355 C356 0.1uF
C357 1uF

IC238B 74HC21N

TODO:

* Write & Verify Verilog Model
* DRC

Title: cft	
Revision: Rev B	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	42/49
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

U

CFT Mini-Computer

Front Panel: Run/Stop State Machine

HALT/4
FPRUN/42
FPSTOP/40
FPFETCH/40
FPSTEP/40
FPHALT/41
POWEROK/40
CLK1/31

HALT/44
FPRUN/42
FPSTOP/40
FPFETCH/40
FPSTEP/40
FPHALT/41
POWEROK/40
CLK1/44

FPFETCH
FPSTEP
FPHALT
FPSTOP
POWEROK
CLK1

Falling edge detection

IC247C 74HC00N
IC247A 74HC00N
IC247D 74HC00N
IC247B 74HC00N
IC250D 74HC00N

Both CLKEN and HALT are driven low when the processor is stopped.
CLKEN stops the clock. HALT tristates the Control Unit so the front panel can drive the processor's control signals.
Since other units could also assert HALT, CLKEN is the only way we have of knowing we've stopped the processor.

To Clock Generator — FPCLKEN/45

TP23

STOP line goes high whenever HALT is active (including wait states, since HALT is open collector.

HALT (pulled up by Control Unit)

IC250A 74HC00N — Front Panel LED — FPSTOP/40

IC249A 74HC112N
CLK1
STOP
POWEROK
GND

IC204A 74HC03N — Open Collector
IC204C 74HC03N — Open Collector

IC250B 74HC00N
IC250C 74HC00N — Front Panel LED — FPRUN/42

The POWEROK pulse makes the computer power on halted.

VCC
IC249B 74HC112N
STEP/
FETCH/
GND

TP21

Disable Front Panel Switches while running — SWINHIBIT/40

ISRUN = ISRUN1 + IRSUN2
HALT = ISRUN = ISRUN1 + IRSUN2
HALT = RUN = IRSUN1 + IRSUN2
HALT = ISRUN1 NAND ISRUN2

ISSTOP = ISRUN = HALT

Decoupling
C366 0.1uF, C367 0.1uF, C368 0.1uF, C369 0.1uF, C370 0.1uF, C371 1uF
VCC
GND

IC248C 74HC00N
IC248D 74HC00N
IC248B 74HC00N
IC204D 74HC03N — Open Collector

TODO:

* Write & Verify Verilog Model
* DRC

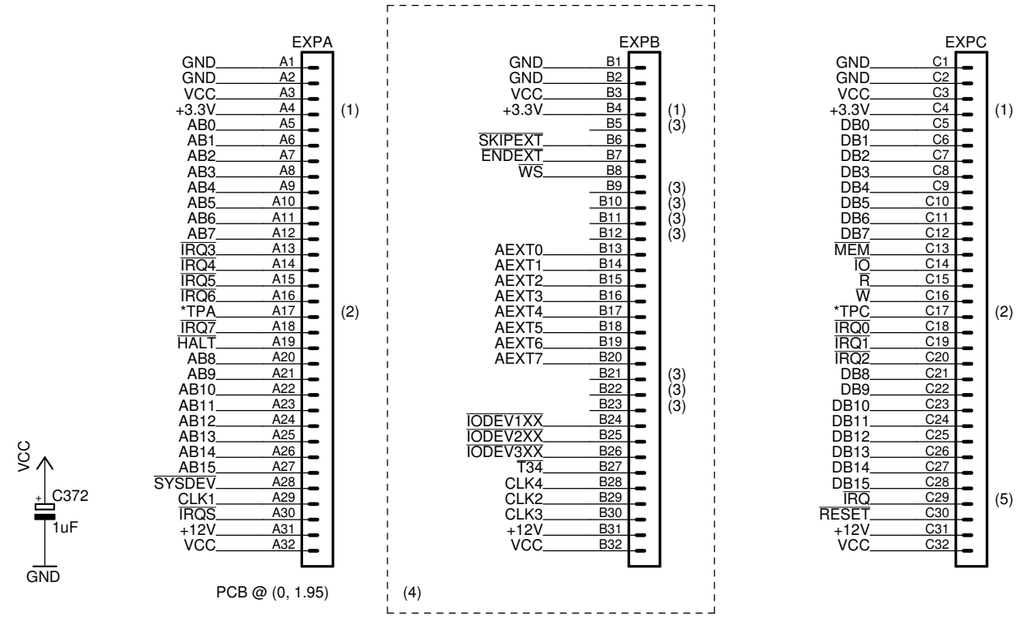
U

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	43/49
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Bus Connectors

Expansion Bus (computer bus)



Notes

(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it. It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) $\overline{\text{IRQ}}$ is provided for systems which lack an interrupt controller ($\overline{\text{IRQ0-7}}$)

IC Sockets & Miscellaneous Extras

DIP8: RS 402-579 (£0.06@50), Farnell 1101345 (£0.125), Farnell-US 1183572 (£0.072)
DIP14: RS 402-765 (£0.10@50), Farnell-US 1183573 (£0.093/£0.086@100), Farnell 1101346 (£0.122@5)
DIP16: RS 402-771 (£0.11@50), Farnell-US 1183574 (£0.086@100), Farnell 1101347 (£0.147@5)
DIP18: RS 402-768 (£0.13@50), Farnell 1101348 (£0.126@5)
DIP20: RS 402-793 (£0.14@50), Farnell-US 1183577 (£0.119/£0.11@100), Farnell 4285608 (£0.146)
DIP24 (0.3"): RS 801-752 (£0.17@50), Farnell US 1557740 (£0.208), Farnell 1103849 (£0.75@5)
DIP32: RS 801-774 (£0.28@50), Farnell 1654375 (£0.27)
DIP40: RS 402-838 (£0.28@50), Farnel-US 1183580 (£0.236), Farnell 4285669 (£0.28)

Also:
Prototyping board, large:
Prototyping board, Eurocard 3U:
Solder:
Enamel wire:
Power rail wire:

H1 HOLE	@ (.175, 3.675)
H2 HOLE	@ (5.8, 3.675)
H3 HOLE	@ (5.8, .225)
H4 HOLE	@ (.175, .225)

U

Title: cft	
Revision: Rev J	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	44/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Debugging Card

IO/44
MEM/44
R/44
RESET/44
W/44
IODEV3XX/44
HALT/44
WS/44
AB[0..15]
DB[0..15]

IO/46
MEM/46
R/46
RESET/46
W/46
IODEV3XX/46
HALT/46
WS/46

Bus Interface

IC253 74HC138N
IODEV3XX
AB4 AB5 AB6 AB7 W IODEV3XX
&038x &039x &03Ax &00Bx &00Cx &00Dx &00Ex &03FX DEBW

IC254A 74HC74N
RESET DEBCONT DEBW
Q=1: no WS
Q=0: no WS

IC256A 74HC05N

IC251 MCP23016 I²C addr 0x20
IC255 MCP23016 I²C addr 0x21
IC252 MCP23016 I²C addr 0x23
DEBSCL DEBSDA
C374 C375 C378 C379 C381 C382 0.1uF 33pF
R222 R223 R224 3k9
JP32 JP31

Status display

DEBLED0 DEBLED1 DEBLED2 MOSI DEBLED3
R225 R226 R227 R228 330R
LED177 LED178 LED179 LED180
T1 T2 T3 T4/Prog

ATMEGA168

C383 C386 0.1uF
DEBRST S48 C384 22pF C385 22pF 14.7456 XTAL5
PC6(/RESET) PB6(XTAL1/TOSC1) PB7(XTAL2/TOSC2)
PC0(ADC0) PC1(ADC1) PC2(ADC2) PC3(ADC3) PC4(ADC4/SDA) PC5(ADC5/SCL)
PD0(RXD) PD1(TXD) PD2(INT0) PD3(INT1) PD4(XCK/T0) PD5(T1) PD6(AIN0) PD7(AIN1)
PB0(ICP) PB1(OC1A) PB2(SS/OC1B) PB3(MOSI/OC2) PB4(MISO) PB5(SCK)
R231 4k7
R232 4k7
IC257

JP33 DEBRST
External reset (or alternate pushbutton)

USB Serial

JP34 RXD TXD -RTS DEBOUT DEBIN FTDIVCC -CTS
R229 R230 1k
Made for an FTDI USB to 3.3V TTL cable
For a 5V FTDI USB cable, do not fit R2 and R3.

ISP Programmer

JP35 ISP MOSI MISO SCK RESET +5 GND

IC256C IC256B 74HC05N
CFTRST DEBHALT RESET HALT

To front panel controller
JP36
FPCLKEN/43
FPUSTEP/40

Test Point Headers

JP37 SKIPEXT ENDEXT WS
JP39 IODEV1XX IODEV2XX IODEV3XX T34 SYSDEV
JP38 IRQ4 IRQ3 IRQ5 IRQ6 IRQ7 IRQ0 HALT IRQ1 IRQ2
JP40 CLK4 CLK1 CLK2 CLK3 IRQS

Expansion Bus (computer bus)

EXP1A EXP1B EXP1C

EXP1A	EXP1B	EXP1C
GND A1	GND B1	GND C1
GND A2	GND B2	GND C2
VCC A3	VCC B3	VCC C3
+3.3V A4	+3.3V B4	+3.3V C4
AB0 A5	B5	DB0 C5
AB1 A6	SKIPEXT B6	DB1 C6
AB2 A7	ENDEXT B7	DB2 C7
AB3 A8	WS B8	DB3 C8
AB4 A9	B9	DB4 C9
AB5 A10	B10	DB5 C10
AB6 A11	B11	DB6 C11
AB7 A12	B12	DB7 C12
IRQ3 A13	AEXT0 B13	MEM C13
IRQ4 A14	AEXT1 B14	IO C14
IRQ5 A15	AEXT2 B15	R C15
IRQ6 A16	AEXT3 B16	W C16
*TPA A17	AEXT4 B17	*TPC C17
IRQ7 A18	AEXT5 B18	IRQ0 C18
HALT A19	AEXT6 B19	IRQ1 C19
AB8 A20	AEXT7 B20	IRQ2 C20
AB9 A21	B21	DB8 C21
AB10 A22	B22	DB9 C22
AB11 A23	B23	DB10 C23
AB12 A24	IODEV1XX B24	DB11 C24
AB13 A25	IODEV2XX B25	DB12 C25
AB14 A26	IODEV3XX B26	DB13 C26
AB15 A27	T34 B27	DB14 C27
SYSDEV A28	CLK4 B28	DB15 C28
CLK1 A29	CLK2 B29	CLK5 C29
IRQS A30	CLK3 B30	RESET C30
+12V A31	+12V B31	+12V C31
VCC A32	VCC B32	VCC C32

PCB @ (0, 1.95)

Decoupling

C373 C376 C377 0.1uF
C380 1uF

IC254B 74HC74N
IC256D IC256E IC256F 74HC05N
C387 1uF

[PCB Logo]
[PCB Logo]
[PCB Logo]

H5 HOLE	@ (.175, 3.675)
H6 HOLE	@ (5.8, 3.675)
H7 HOLE	@ (5.8, .225)
H8 HOLE	@ (.175, .225)

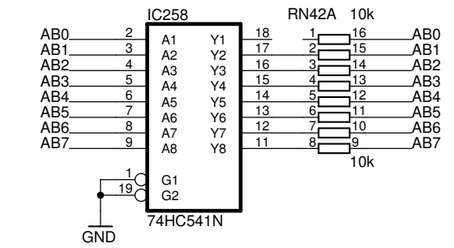
T

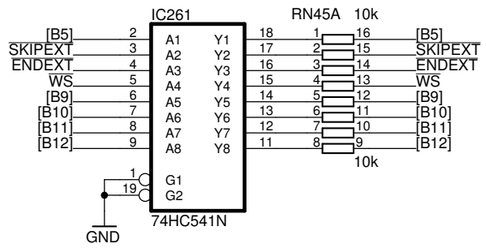
Title:	cft
Revision:	Rev A
Last Change:	16 Dec 2012 12:04:37
Drawn by: Alexios	45/49
Simulation filename:	N/A
More Info:	http://www.bedroomlan.org/cft

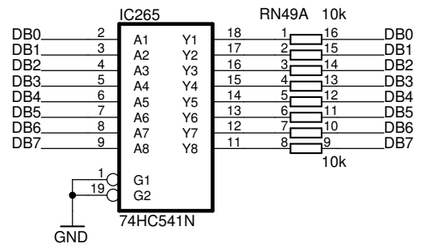
CFT Mini-Computer

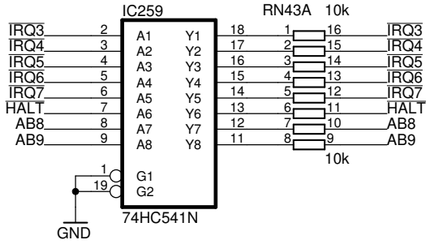
Bus Hold

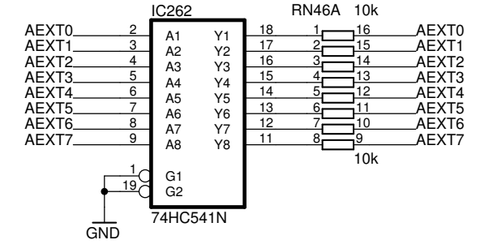
Bus Hold

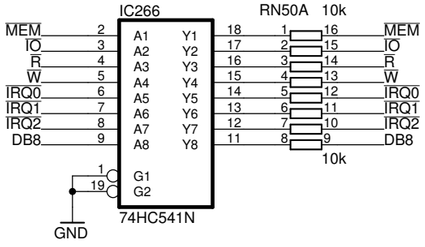


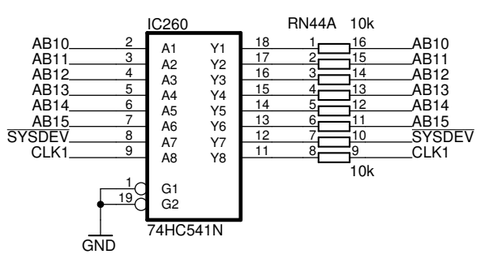


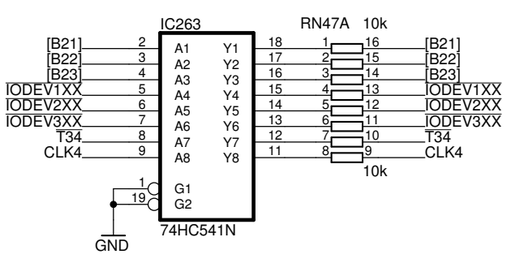


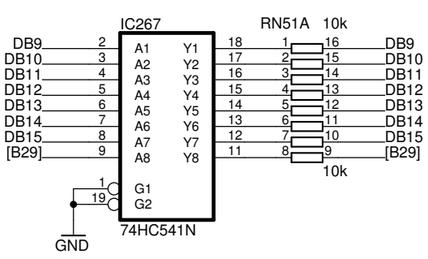


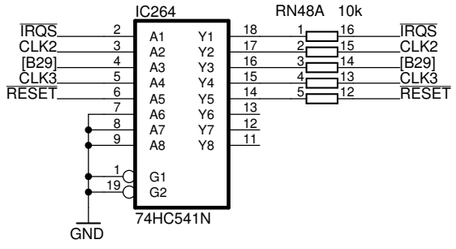


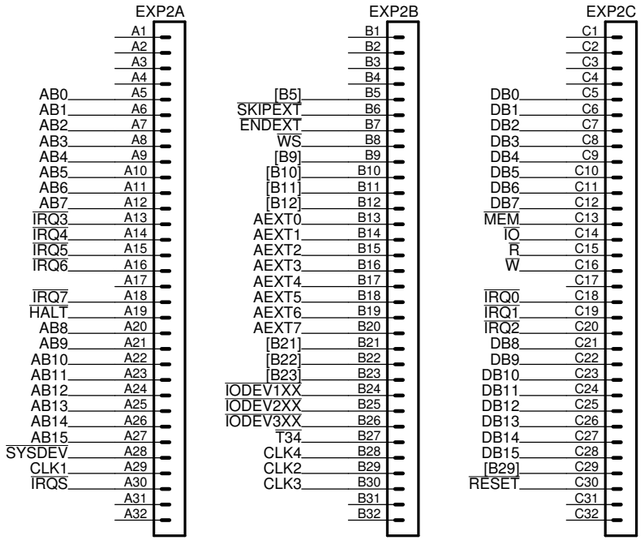




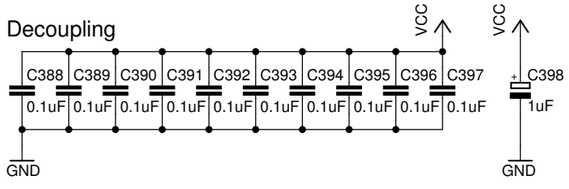








PCB @ (0, 1.95)



H9 HOLE	@ (.175, 3.675)
H10 HOLE	@ (5.8, 3.675)
H11 HOLE	@ (5.8, .225)
H12 HOLE	@ (.175, .225)

U

Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	46/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Floppy Drive Controller

DB[0..15]
AB[0..15]
R/46
W/46
RESET/46
IODEV1XX/46
IRQ/44
AB0

R/48
W/48
RESET/46
IODEV1XX/48
IRQ/44

Address Decoder

IC268A
74HC139N
AB1
AB2
FDCCS
FDCOR
FDCCR
FDCREG

IC269
74HC688N
=&0100-&0107
AB3
AB4
AB5
AB6
AB7
IODEV1XX
GND
VCC

IC268B
74HC139N

74HC32N
IC270A

FDC Control Register

IC287
74HC259N
DB0
DB1
DB2
DB3
FDCRST
DHCGEN
FDCPC
FDCDRV
MON1
MON2

Floppy Controller

IC272
WD37C65B
R
W
AB0
FDCIRQ
FDCRST
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DMA
DACK
TC
CS
LDOR
LDCR
PCVAL
DRV
XT1
XT2
WE
WD
STEP
DIRC
HDL
HS
DS1
DS2
MO1/DS3
MO2/DS4
RWC/RPM
RDD
WP
TR00
IDX
DHCG
DHCGEN

IBM connectors allow two drives with motor control.
They use a 34-conductor flat cable with a 7-conductor twist because drives typically have no DIP switches for configuration.
The two drives are mapped to DS3 and DS4, so the IBM drives are always units #3 and #4. The Shugart drives can have any ID.

Drive Connectors

50-pin Shugart Interface (for 8-inch drives)

2550-5

RWC
DHCG
HS
HDL
IDX
DS1
DS2
DS3
DS4
DIRC
STEP
WD
WE
TR00
WP
RDD

CON27-1 CON27-2 CON27-3 CON27-4 CON27-5 CON27-6 CON27-7 CON27-8 CON27-9 CON27-10 CON27-11 CON27-12 CON27-13 CON27-14 CON27-15 CON27-16 CON27-17 CON27-18 CON27-19 CON27-20 CON27-21 CON27-22 CON27-23 CON27-24 CON27-25 CON27-26 CON27-27 CON27-28 CON27-29 CON27-30 CON27-31 CON27-32 CON27-33 CON27-34 CON27-35 CON27-36 CON27-37 CON27-38 CON27-39 CON27-40 CON27-41 CON27-42 CON27-43 CON27-44 CON27-45 CON27-46 CON27-47 CON27-48 CON27-49 CON27-50

150R
RN52
JP41
Install shunt to enable FDC-side signal termination.

2534-5

DENSITY
IDX
MOTOR1
DS4
DS3
MOTOR2
DIRC
STEP
WD
WE
TR00
WP
RDD
HS
DHCG

CON28-1 CON28-2 CON28-3 CON28-4 CON28-5 CON28-6 CON28-7 CON28-8 CON28-9 CON28-10 CON28-11 CON28-12 CON28-13 CON28-14 CON28-15 CON28-16 CON28-17 CON28-18 CON28-19 CON28-20 CON28-21 CON28-22 CON28-23 CON28-24 CON28-25 CON28-26 CON28-27 CON28-28 CON28-29 CON28-30 CON28-31 CON28-32 CON28-33 CON28-34

1-2: High density
2-3: Low density
JP42
R236
1k

34-pin Shugart Interface (IBM-style)

IBM Floppy Motor Control

MON1
MON2
4k7
R234
R235
BC548
TR6
TR7
MOTOR1
MOTOR2

Interrupt Line Driver

IRQ[0..7]
SV19
IRQ2
IRQ3
IRQ4
IRQ
4k7
R233
FDCIRQ
BC548
TR5

Decoupling

C399 C400 C401 C402 C403 0.1uF
C404 1uF

IC270B IC270C IC270D 74HC32N

XTAL6 9.600 MHz
XTAL7 16.000 MHz
C405 C406 0.1uF

D	
Title: cft	
Revision: Rev A	
Last Change: 16 Dec 2012 12:04:37	
Drawn by: Alexios	47/49
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

General Purpose I/O (1/2)

Address Decoder

IC273A, IC273B — 74HC139N

IC274 — 74HC688N =&0108-&0109

Output Latches

IC275, IC276, IC277, IC278 — 74HC373N

Input Buffers

IC279, IC280 — 74HC540N

IC281, IC282 — 74HCT541N

Decoupling

C407–C416 0.1uF, C417 1uF

TODO:

* Write & Verify Verilog Model
* DRC

Title:	cft
Revision:	Rev A
Last Change:	16 Dec 2012 12:04:37
Drawn by:	Alexios
	48/49
Simulation filename:	N/A
More Info:	http://www.bedroomlan.org/cft

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CFT Mini-Computer

General Purpose I/O, 2/2

GPOB[0..15]
GPIB[0..15]
GPOA[0..15]
GPIA[0..15]

User port 0

VCC
RN53 4k7
RN54 4k7
74HCT14N
IC283A
IC283B
IC283C
IC283D
IC283E
IC283F
GPIA0
GPIA1
GPIA2
GPIA3
GPIA4
GPIA5
GPIA6
GPIA7
RN55A 100R
RN55B 100R
RN55C 100R
RN55D 100R
RN55E 100R
RN55F 100R
RN55G 100R
RN55H 100R
CON29
GPOA0
GPOA1
GPOA2
GPOA3
GPOA4
GPOA5
GPOA6
GPOA7
GND

User port 1

IC284A
IC284B
IC284C
IC284D
IC284E
IC284F
GPIA8
GPIA9
GPIA10
GPIA11
GPIA12
GPIA13
GPIA14
GPIA15
RN56A 100R
RN56B 100R
RN56C 100R
RN56D 100R
RN56E 100R
RN56F 100R
RN56G 100R
RN56H 100R
CON30
GPOA8
GPOA9
GPOA10
GPOA11
GPOA12
GPOA13
GPOA14
GPOA15
GND

RN57 4k7
GPIB0
GPIB1
GPIB2
GPIB3
GPIB4
GPIB5
GPIB6
GPIB7
RN58 4k7
GPIB8
GPIB9
GPIB10
GPIB11
GPIB12
GPIB13
GPIB14
GPIB15

Printer

CON31
STROBE
D0
D1
D2
D3
D4
D5
D6
D7
ACK
BUSY
PE
SEL
AUTOFD
ERROR
INIT
SELIN
GPOB0
GPOB1
GPOB2
GPOB3
GPOB4
GPOB5
GPOB6
GPOB7
GPIB0
GPIB1
GPIB2
GPOB11
GPIB3
GPIB4
GPOB9
GPOB10
GPIB4
GPIB3

Joystick 0 (L)

CON32
Up
Left
Pot B
Pot A
Down
Right
Button
GPIB6
GPIB8
GPIB7
GPIB9
GPIB10

Joystick 1 (R)

CON33
GPIB11
GPIB13
GPIB12
GPIB14
GPIB15

Front Panel GP LEDs

CON35
GPOB12
GPOB13
GPOB14
GPOB15
GPIB5
R240
R241
R242
R251
R243
Tape read data

Tape output attenuator

~1.5V peak to peak
GPOB15
R244 22k
MIC
R247 10k
C420 100nF
Tape
MIC
Write to tape
EAR
Read from tape
CON34

Tape input amplifier

R248 10k
C422 47nF
R250 10k
IC285A
LM358N
R245 22k
R238 1k
R246 100k
R249 10k
C421 100nF
IC285B
LM358N
C423 0.1uF
GPIB5
BC548 TR8
R237 10k

Decoupling

C418 0.1uF
C419 0.1uF

TODO:

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