CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

- OD This input signal is open drain.
- TTL This input signal may be at TTL logic levels.
- Z This input may be at High Impedance.
- Z* This input (local to this board) may be at High Impedance.

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Note: the shading patterns below are in colour, and not distinguishable on black & white hard copies.

Circuits in need of improvement are marked like this.

Circuits known to be incorrect are marked like this.

Obsolete sections or circuits are marked like this

Changes from previous revision are marked like this.

D	Title: front-panel-revD-DEB
	Revision: Rev B
	Last Change: 18 Oct 2013 17:04:38
	Drawn by: Alexios 1/11
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Switch Wiring

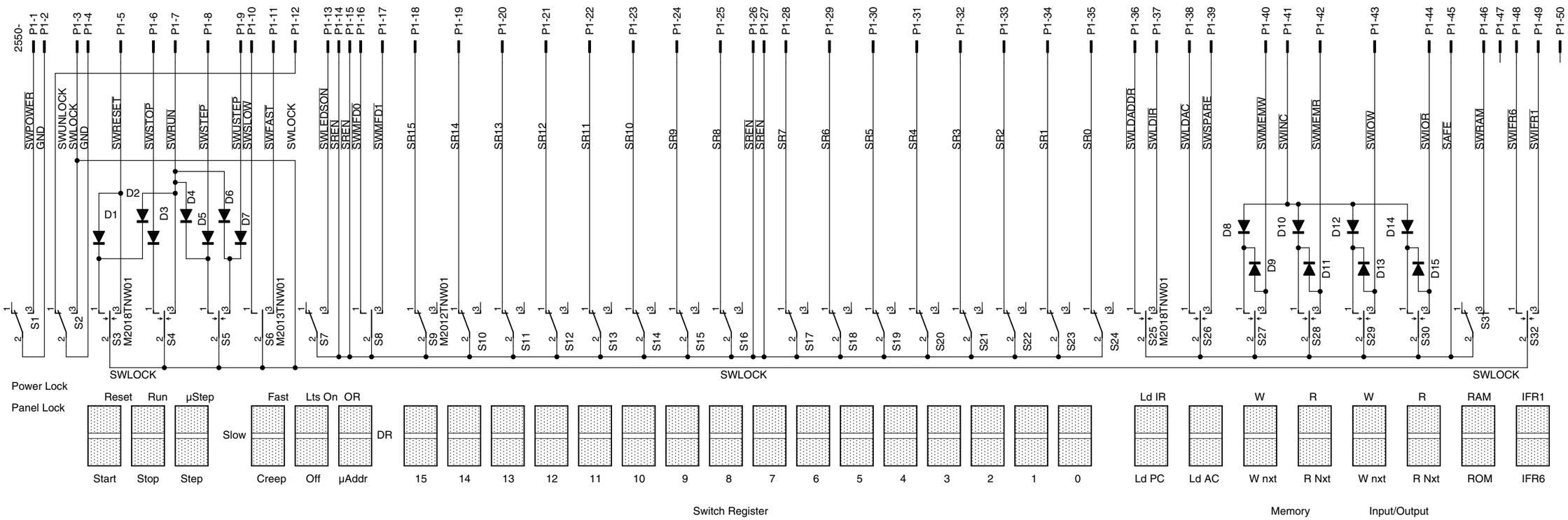
Left switch actuation truth table

	SWRESET	SWRUN	SWSTOP	SWSTEP	SWUSTEP
Reset	L				
Start	L	L			
Run		L			
Stop			L		
Step		L **		L	
uStep		L **			L

* The machine is temporarily set to the RUN state during stepping.

Right switch actuation truth table

	SWMEMR	SWMEMW	SWIOR	SWIOW	SWINC
Memory Read	L				
Memory Read Next	L	L			L
Memory Write		L			
Memory Write Next			L		L
I/O Read			L		
I/O Read Next				L	L
I/O Write				L	
I/O Write Next					L

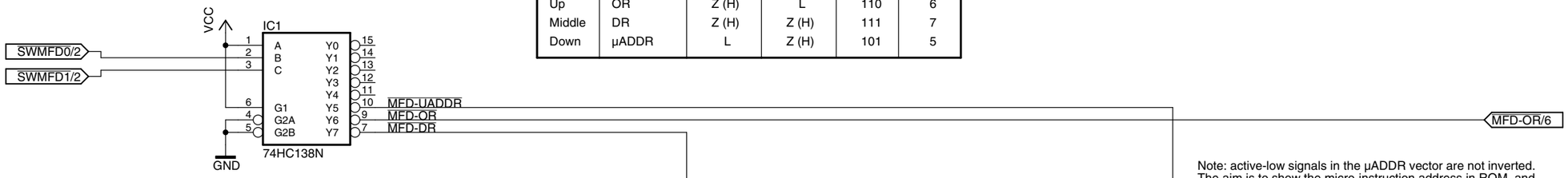


U	Title: front-panel-revD-DEB
	Revision: Rev D
	Last Change: 18 Oct 2013 17:04:38
	Drawn by: Alexios 2/11
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

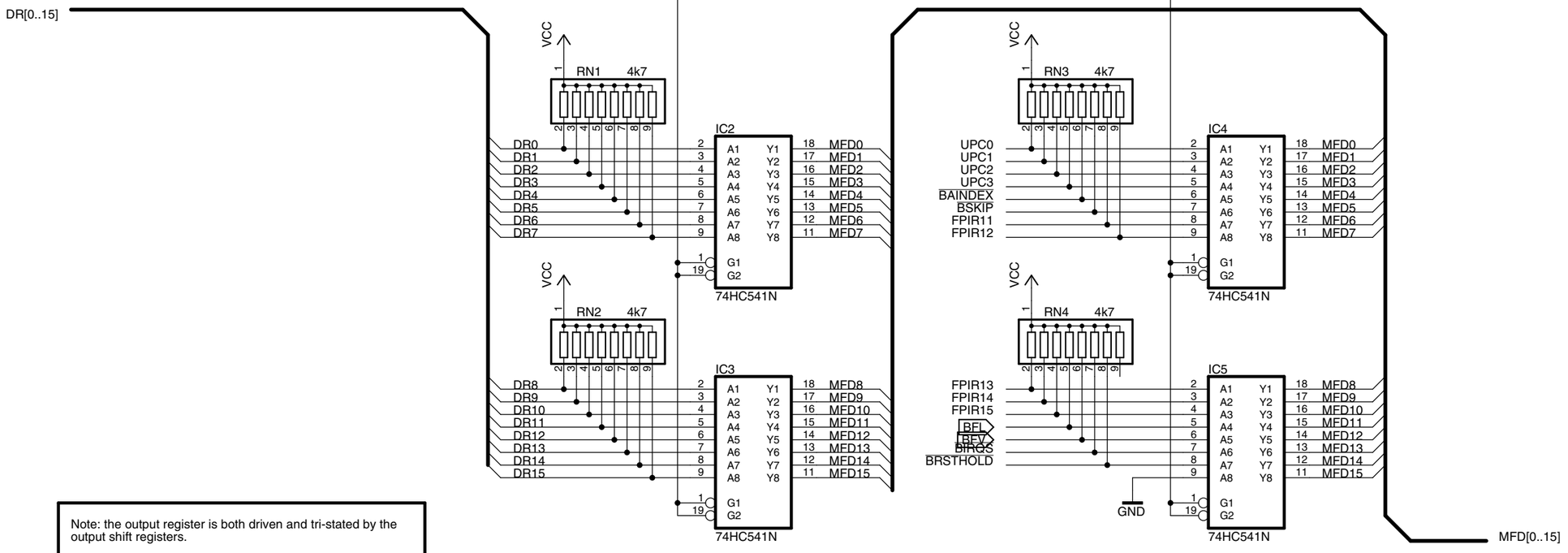
CFT Mini-Computer

Front Panel: Multi-Function Display

Switch	MFD Shows	$\overline{\text{SWMFD0}}$	$\overline{\text{SWMFD1}}$	Vector	Output
Up	OR	Z (H)	L	110	6
Middle	DR	Z (H)	Z (H)	111	7
Down	µADDR	L	Z (H)	101	5



Note: active-low signals in the µADDR vector are not inverted. The aim is to show the micro-instruction address in ROM, and inverted bits would confuse the matter. The front panel shows this.

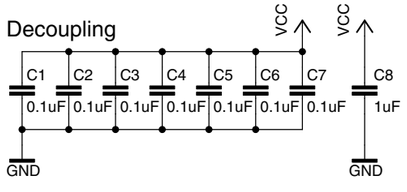


Note: the output register is both driven and tri-stated by the output shift registers.

Output Register

Data Register (DR)

µADDR Vector



TODO:

* DRC

U

Title: front-panel-revD-DEB	
Revision: Rev C	
Last Change: 18 Oct 2013 17:04:38	
Drawn by: Alexios	3/11
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Input Shift Registers, switches and computer buses

AB[0..15]
DB[0..15]
SR[0..15]

Left Switches

VCC
RN5 4k7
R2 4k7
IC6
74HC165N

SWPOWER
SWLOCK
SWRESET
SWSTOP
SWRUN
SWSTEP
SWUSTEP
SWSLOW
SWFAST

Switch Register

RN9 4k7
IC8
74HC165N

SR0 SR1 SR2 SR3 SR4 SR5 SR6 SR7

Right Switches

RN14 4k7
IC10
74HC165N

SWLDADDR
SWLDIR
SWLDAC
SWSPARE
SWMEMW
SWINC
SWMEMR
SWIOW

DBUS

IC12
74HC165N

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

ABUS

IC14
74HC165N

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7

DIP Switch

RN6 4k7
IC7
SW1
74HC165N

GND

Switch Register

RN10 4k7
IC9
74HC165N

SR8 SR9 SR10 SR11 SR12 SR13 SR14 SR15

Right Switches and Dip Switch

RN13 4k7
IC11
SW2
74HC165N

SWIOR
SWRAM
SWIFR6
SWIFR1

DBUS

IC13
74HC165N

DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

ABUS

IC15
74HC165N

AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15

SAMPLE/5
ICLK/5
DEBEN/8
DIN/5
DIN/5

Switchable Pull-Up Resistors

VCC
Q1 IRL520N
BUSPU/8
10K R1

RN7 4k7 — DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
RN8 4k7 — DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15
RN11 4k7 — AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7
RN12 4k7 — AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15

DB[0..15]

GND

Decoupling

C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 — 0.1uF
C19 — 1uF

GND

These are enabled when the processor board is not present
(and thus there is no bus conditioning)
The Power MOSFET isn't required (the current will be low),
but I have lots of them from another project.

U

Title: front-panel-revD-DEB	
Revision: Rev A	
Last Change: 18 Oct 2013 17:04:38	
Drawn by: Alexios	4/11
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Input shift registers, processor state

FPIR[0..15]
FPPC[0..15]
FPAC[0..15]

AC

IC16: FPAC0 FPAC1 FPAC2 FPAC3 FPAC4 FPAC5 FPAC6 FPAC7 → 74HC165N
IC17: FPAC8 FPAC9 FPAC10 FPAC11 FPAC12 FPAC13 FPAC14 FPAC15 → 74HC165N

PC

IC18: FPPC0 FPPC1 FPPC2 FPPC3 FPPC4 FPPC5 FPPC6 FPPC7 → 74HC165N
IC19: FPPC8 FPPC9 FPPC10 FPPC11 FPPC12 FPPC13 FPPC14 FPPC15 → 74HC165N

IR

IC20: FPIR0 FPIR1 FPIR2 FPIR3 FPIR4 FPIR5 FPIR6 FPIR7 → 74HC165N
IC21: FPIR8 FPIR9 FPIR10 FPIR11 FPIR12 FPIR13 FPIR14 FPIR15 → 74HC165N

Microcode vector

IC22: FPRUNIT0 FPRUNIT1 FPRUNIT2 FPRUNIT3 WUNIT0 WUNIT1 WUNIT2 FPOPIF0 → 74HC165N
IC23: PB0-OPIF1 PB0-OPIF2 PB0-OPIF3 CPL CLL STI CLI INCPC → 74HC165N

Microcode vector / Misc

IC24: STPDR STPAC DEC IO MEM END → 74HC165N
IC25: BFNEG BFZERO PB0-FV BFIRQ FPFL WEN R → 74HC165N

DIN/8
SAMPLE/8
ICLK/8
VPEN/8
ICLK/4

Decoupling

C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 — 0.1uF
C30 — 1uF
VCC, GND

Title:	front-panel-revD-DEB
Revision:	Rev A
Last Change:	18 Oct 2013 17:04:38
Drawn by:	Alexios 5/11
Simulation filename:	To be coded
More Info:	http://www.bedroomlan.org/cft

U

CFT Mini-Computer

Output shift registers

MFD[0..15]
IBUS[0..15]
AB[0..15]
DB[0..15]

STCP/8
DOUT/8
CLR/8

DBCLK/8
DB-OE/8
ABCLK/8
AB-OE/8
IBUSCLK/8
IBUS-OE/8
CTLCLK/8
CTL-OE/8
ORCLK/8
MFD-OR/3
RESET/7

DBUS

IC26 74HC595N: DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

IC27 74HC595N: DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

DB-OE

ABUS

IC28 74HC595N: AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7

IC29 74HC595N: AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15

AB-OE

IBUS

IC30 74HC595N: IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7

IC31 74HC595N: IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15

IBUS-OE

Output Register (OR)

IC32 74HC595N: MFD0 MFD1 MFD2 MFD3 MFD4 MFD5 MFD6 MFD7

IC33 74HC595N: MFD8 MFD9 MFD10 MFD11 MFD12 MFD13 MFD14 MFD15

MFD-OR

The OR supplies signals to the MFD bus directly.
It displays on the front panel Multi Function Display (MFD)
When the MFD switch is in the OR position (i.e. MFD-OR is low)
It's also unaffected by CLR strobes, resetting to zero when
the computer itself resets (RESET asserted).

Control

IC34 74HC595N

VCC RN15 4k7

D16 1N4148 POWERON/10
D17 SAFE/10
D18 IRQ1/11
IRQ6/11
FPRAM/10
FPRESET/10
D19 WPC/11
D20 WAC/11

VCC RN16 4k7

IC35 74HC595N

D21 WIR/11
D22 W/11
D23 R/11
D24 MEM/11
D25 IO/11
D26 WAR/11
D27 RPC/11
D28 WAC/11

VCC RN17 4k7

IC36 74HC595N

D29 INCPC/11
D30 HALT/11
FPRUN/9
FPSTOP/9

Decoupling

C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 0.1uF
C42 1uF
VCC VCC
GND GND

U

Title: front-panel-revD-DEB	
Revision: Rev A	
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Drawn by: Alexios	6/11
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: Fetch/Execute Decoding, Synchronous Stopping

RESET/6
RSTHOLD/11
CLK4/11
FPEXEC/9
FPFETCH/9
STEP/8
USTEP/8

RESET/8
RSTHOLD/11
CLK4/11
FPEXEC/9
FPFETCH/9
STEP/8
USTEP/8

Fetch/Execute State Decoding

VCC
RN18
4k7

UPC0/3
UPC1/3
UPC2/3
UPC3/3

SW3

IC37
74HC85N
A0 A1 A2 A3 B0 B1 B2 B3
A<B_I A=B_I A>B_I
A<B_O A=B_O A>B_O

Diode logic is acceptable here because it is merely driving a front panel LED (via an 74HCxxx buffer).

D31
1N4148
D32
R3
4k7

FPFETCH
FPEXEC

GND

Set jumpers/switches for first uPC address of Execute cycle.
For Microcode v1-v3, this is 3. For Microcode v4+, it's 2.

Clock-synchronous Stopping

VCC

IC38A
74HC74N
PRE D CLK CLR Q Q̄

STEP
STEP-STOP

IC38B
74HC74N

USTEP
USTEP-STOP

CLK4

IC39B
74HC74N

RESET
RESET-RUN

RSTHOLD

GND

Clock Enable Multiplexer

IC40
74HC253N
1C0 1C1 1C2 1C3 2C0 2C1 2C2 2C3 A B 1G 2G
1Y 2Y

FPCLKEN-IN
FPUSTEP-IN
STEP-STOP
USTEP-STOP
RESET-RUN

FPCLKEN/10
FPUSTEP/10

GND

This is faster and more accurate than using the MCU to control stepping.

The STEP flip flop stops the computer at the beginning of the next fetch cycle.
The µSTEP flip flop stops the computer on the rising edge of the next CLK4 (start of clock cycle).

The $\overline{\text{RESET-RUN}}$ flip flop tri-states the FPCLKEN signal
from the start of $\overline{\text{RESET}}$ to the end of $\overline{\text{RSTHOLD}}$.
The tri-stated FPCLKEN is pulled up (on the PB1), enabling the full-speed clock
which is needed for the $\overline{\text{RSTHOLD}}$ counter.

Decoupling

VCC
C43 0.1uF
C44 0.1uF
C45 0.1uF
C46 1uF
GND

TODO:

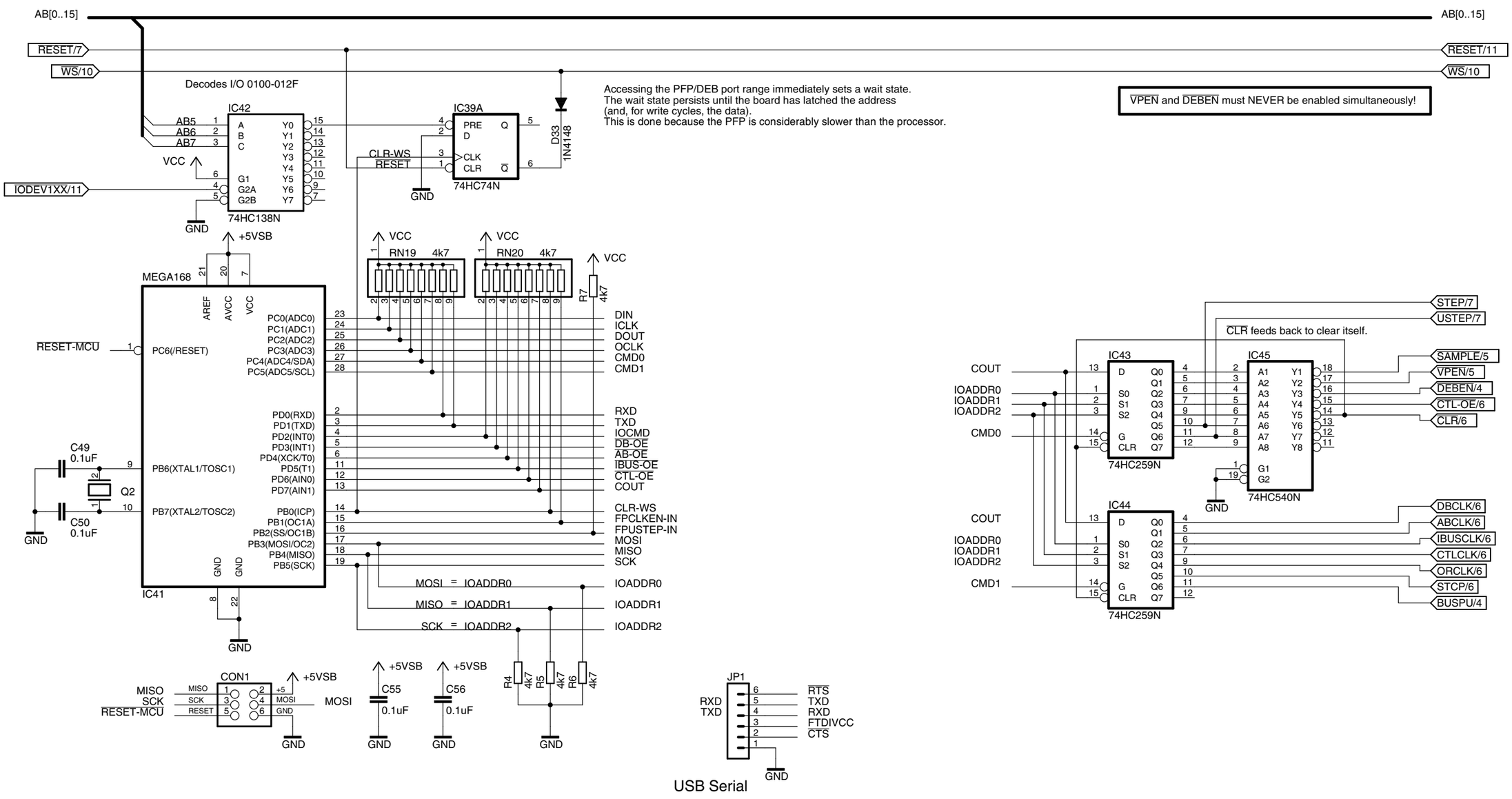
* DRC

U

Title: front-panel-revD-DEB	
Revision: Rev A	
Last Change: 18 Oct 2013 17:04:38	
Drawn by: Alexios	7/11
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel: System Device



Made for an FTDI USB to 3.3V TTL cable
For a 5V FTDI USB cable, do not fit R2 and R3.

Decoupling

C47 0.1uF, C48 0.1uF, C51 0.1uF, C52 0.1uF, C53 0.1uF, C54 1uF

TODO:

* DRC

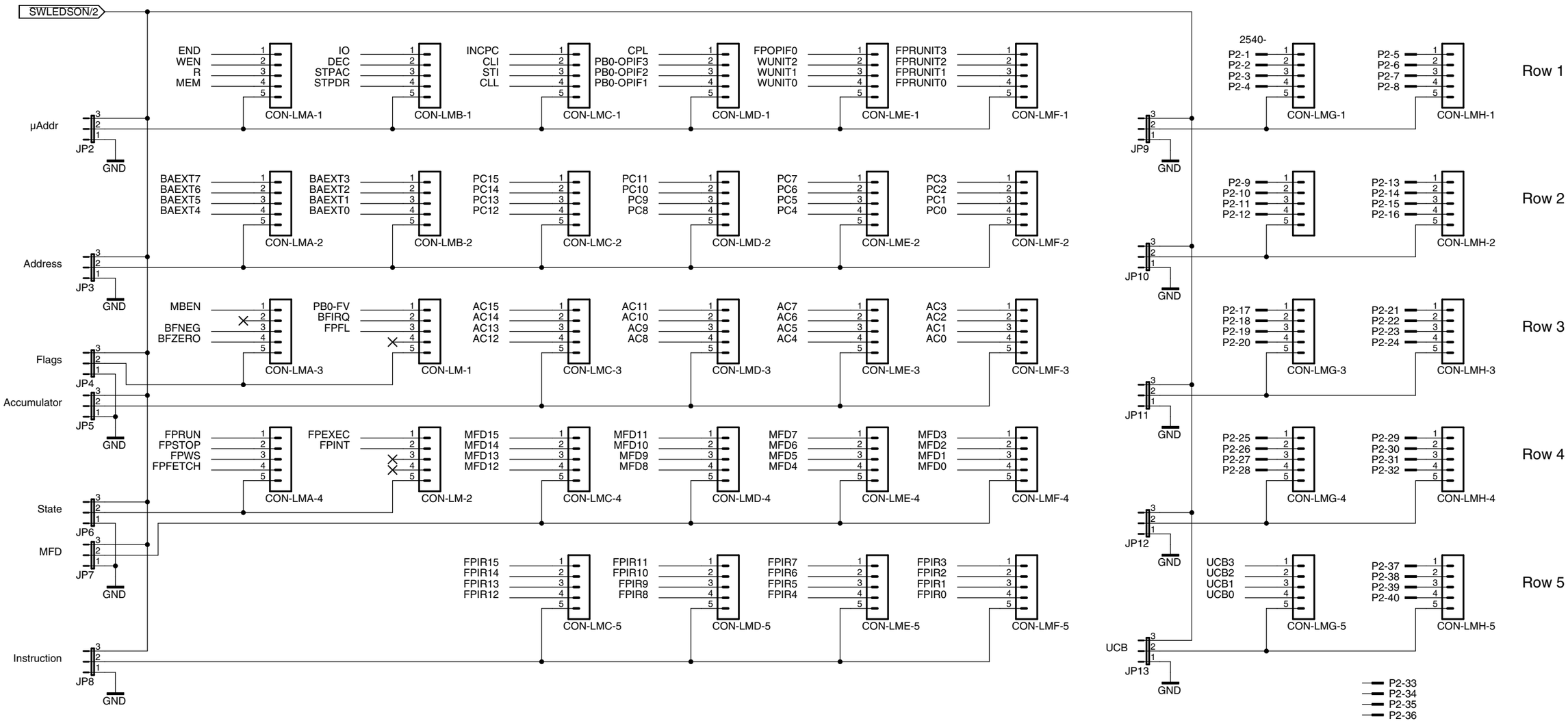
U

Title: front-panel-revD-DEB	
Revision: Rev A	
Last Change: 18 Oct 2013 17:04:38	
Drawn by: Alexios	8/11
Simulation filename: To be coded	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Front Panel Light Connections

Module 1 Columns 1-4	Module 2 Columns 5-9	Module 3 Columns 10-13	Module 4 Columns 14-17	Module 5 Columns 18-21	Module 6 Columns 22-25	Module 7 Columns 26-29	Module 8 Columns 30-33

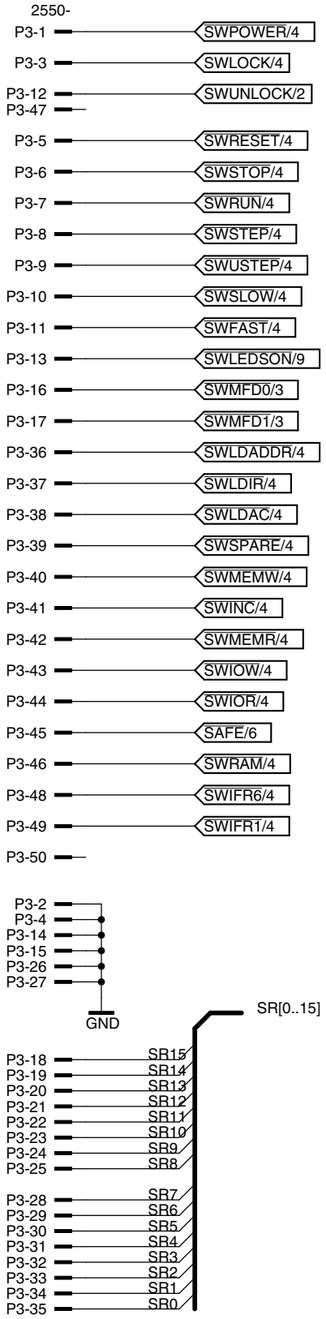


U	Title: front-panel-revD-DEB
	Revision: Rev A
	Last Change: 18 Oct 2013 17:04:38
	Drawn by: Alexios 9/11
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

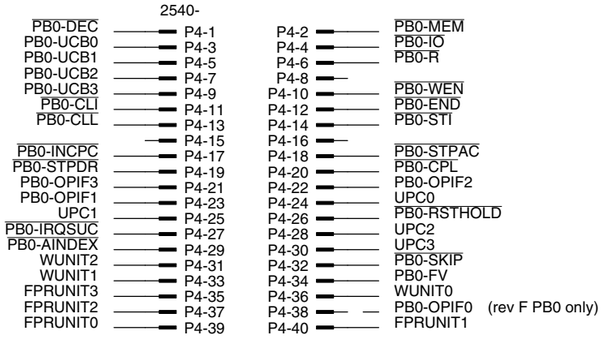
CFT Mini-Computer

Connectors

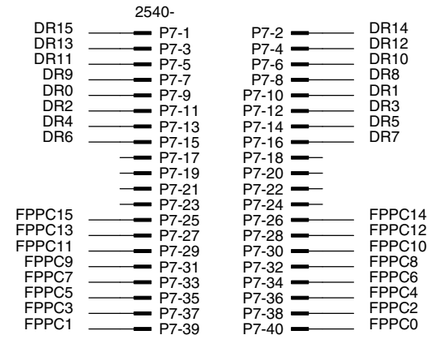
Switch Assembly



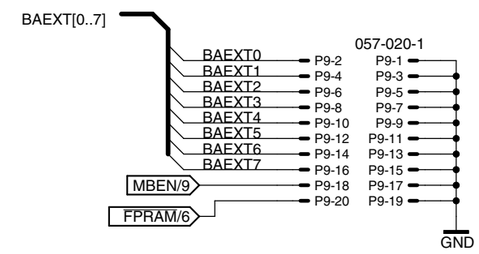
Processor Board 0



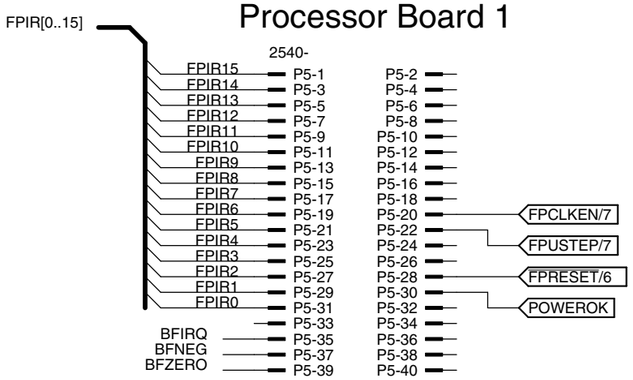
Processor Board 2



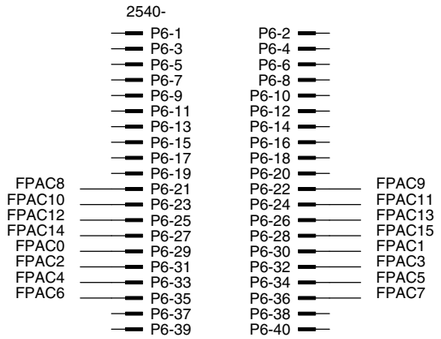
Processor Board 3 (MBU)



Processor Board 1



Processor Board 2



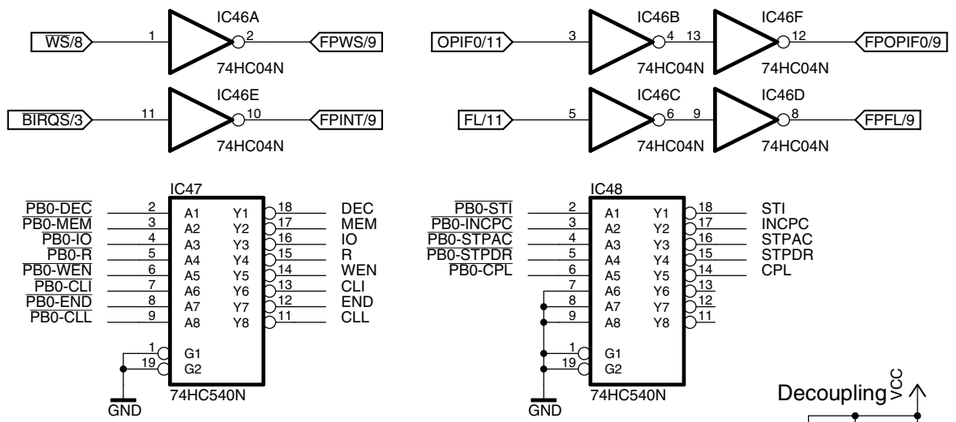
Signal Renaming

PB0-UCB0	=	UCB0
PB0-UCB1	=	UBC1
PB0-UCB2	=	UCB2
PB0-UCB3	=	UCB3
PB0-OPIF3	=	OPIF3
PB0-OPIF2	=	OPIF2
PB0-OPIF1	=	OPIF1
PB0-WUNIT2	=	WUNIT2
PB0-WUNIT1	=	WUNIT1
PB0-WUNIT0	=	WUNIT0
PB0-RUNIT3	=	RUNIT3
PB0-RUNIT2	=	RUNIT2
PB0-RUNIT1	=	RUNIT1
PB0-RUNIT0	=	RUNIT0

Microcode Address signals are NOT inverted.

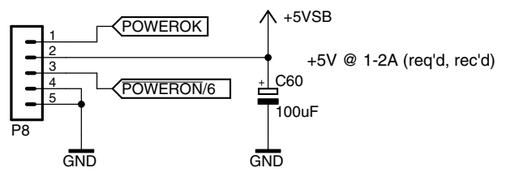
PB0-IRQSUC	=	BIRQS
PB0-SKIP	=	BSKIP
PB0-RSTHOLD	=	BRSTHOLD
PB0-AINDEX	=	BAINDEX

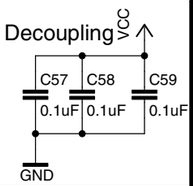
Signal Inversion



Power Supply

From power supply loom





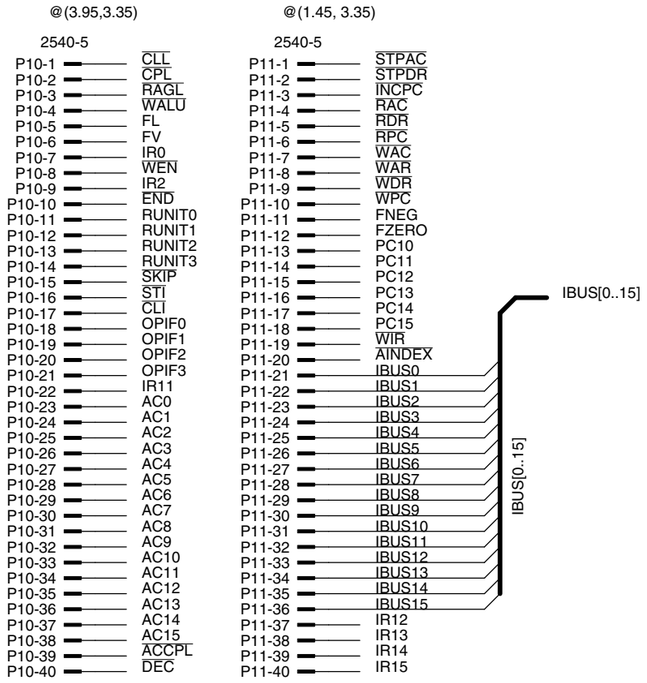
T

Title: front-panel-revD-DEB	
Revision: Rev C	
Last Change: 18 Oct 2013 17:04:38	
Drawn by: Alexios	10/11
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

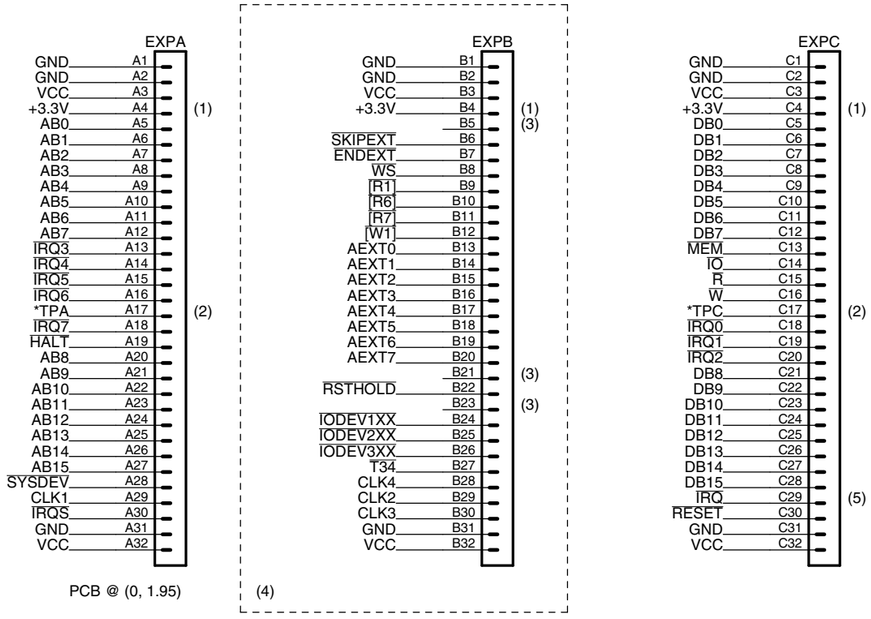
CFT Mini-Computer

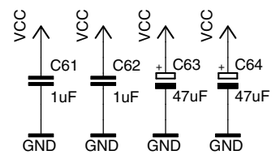
Bus Connectors

Control Bus (processor bus)



Expansion Bus (computer bus)





Notes

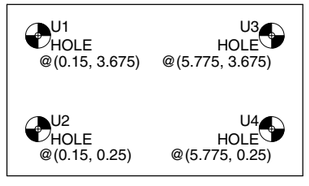
(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it.
It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) $\overline{\text{IRQ}}$ is provided for systems which lack an interrupt controller ($\overline{\text{IRQ0-7}}$)



[PCB Logo]

[QR Code http://www.bedroomlan.org/cft (shortened)]

open hardware

J	Title: front-panel-revD-DEB
	Revision: Rev J
	Last Change: 18 Oct 2013 17:04:38
	Drawn by: Alexios — 11/11
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft