# CFT

# 16-bit Mini-Computer

Processor Board 3, Surface Mount Components.

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

OD This input signal is open drain.
TTL This input signal may be at TTL logic levels.
Z This input may be at High Impedance.
Z' This input (local to this board) may be at High Impedance.

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing
C: Constructed and Tested

## Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

## TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Circuits in need of improvement are marked like this.

Obsolete sections or circuits are marked like this.

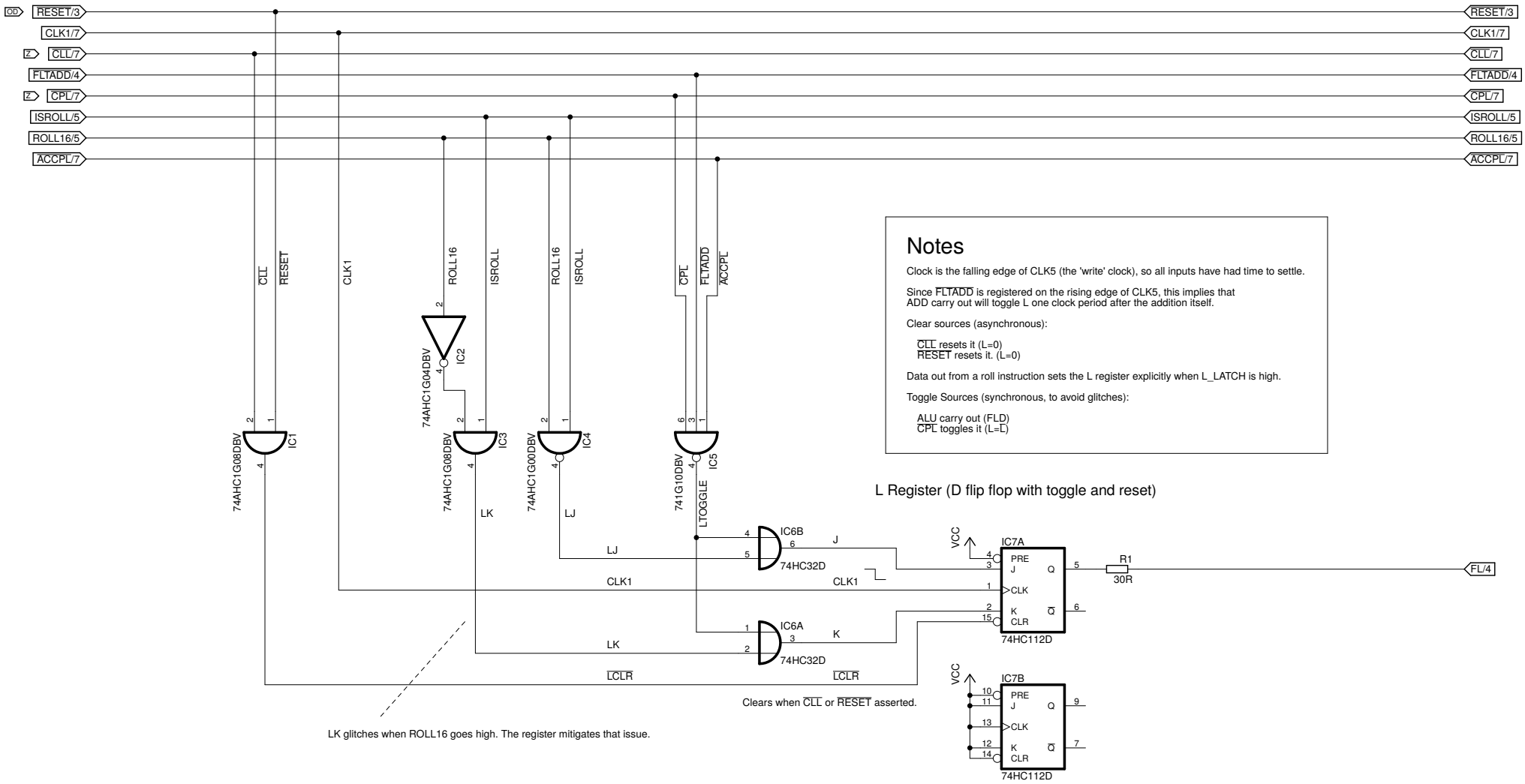
Circuits known to be incorrect are marked like this.

D

| | |
|---|---|
| Title: CFT-PB3-revC | |
| Revision: Rev B | |
| Last Change: 30 Dec 2018 17:07:21 | |
| Drawn by: Alexios | 1/7 |
| Simulation filename: register.v#reg_L | |
| More Info: http://www.bedroomlan.org/cft | |

# CFT Mini-Computer

The L Register




## Notes

Clock is the falling edge of CLK5 (the 'write' clock), so all inputs have had time to settle.

Since FLTADD is registered on the rising edge of CLK5, this implies that ADD carry out will toggle L one clock period after the addition itself.

Clear sources (asynchronous):

CLL resets it (L=0)
RESET resets it. (L=0)

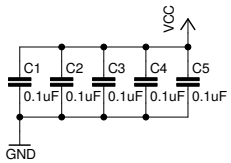
Data out from a roll instruction sets the L register explicitly when L_LATCH is high.

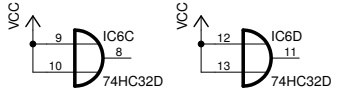
Toggle Sources (synchronous, to avoid glitches):

ALU carry out (FLD)
CPL toggles it (L=L)

L Register (D flip flop with toggle and reset)

Decoupling



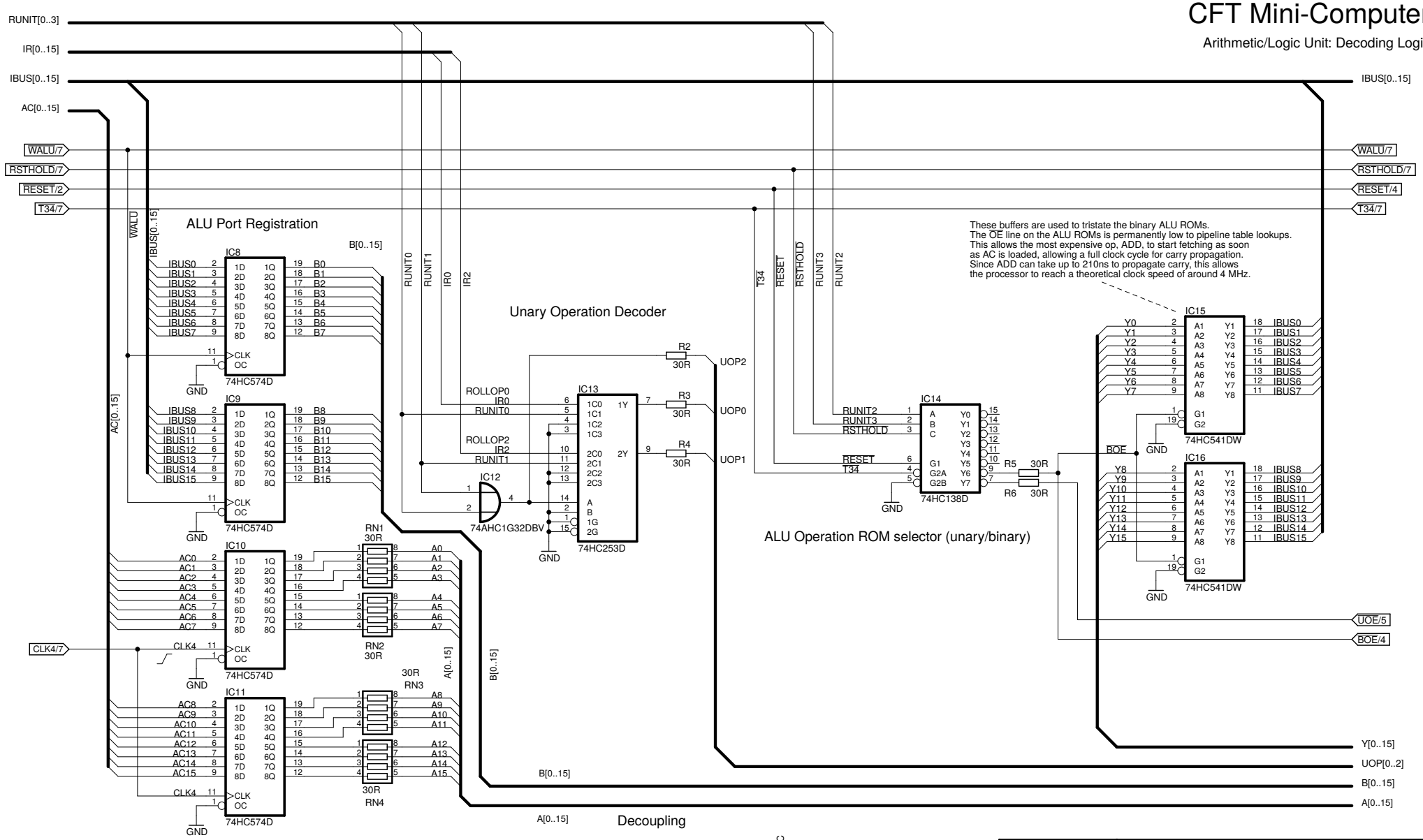




U

| | |
|---|---|
| Title: CFT-PB3-revC | |
| Revision: Rev C | |
| Last Change: 30 Dec 2018 17:07:21 | |
| Drawn by: Alexios | 2/7 |
| Simulation filename: register.v#reg_L | |
| More Info: http://www.bedroomlan.org/cft | |

# CFT Mini-Computer

Arithmetic/Logic Unit: Decoding Logic

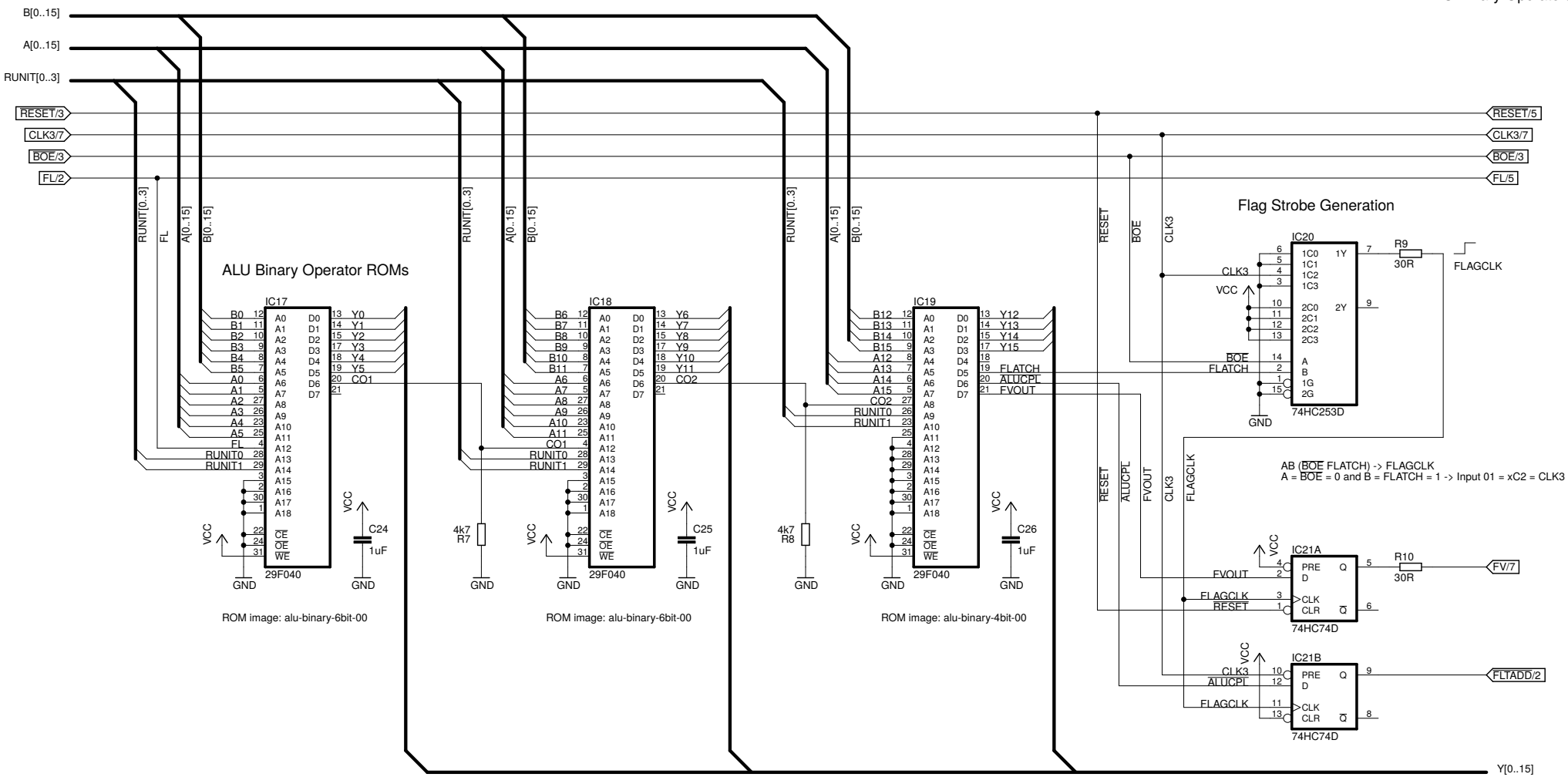



| | |
|---|---|
| Title: | CFT-PB3-revC |
| Revision: | Rev C |
| Last Change: | 30 Dec 2018 17:07:21 |
| Drawn by: | Alexios |
| | 3/7 |
| Simulation filename: | alu.v |
| More Info: | http://www.bedroomlan.org/cft |

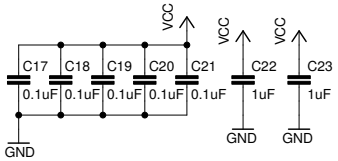
U

# CFT Mini-Computer

ALU Binary Operators




## Decoupling

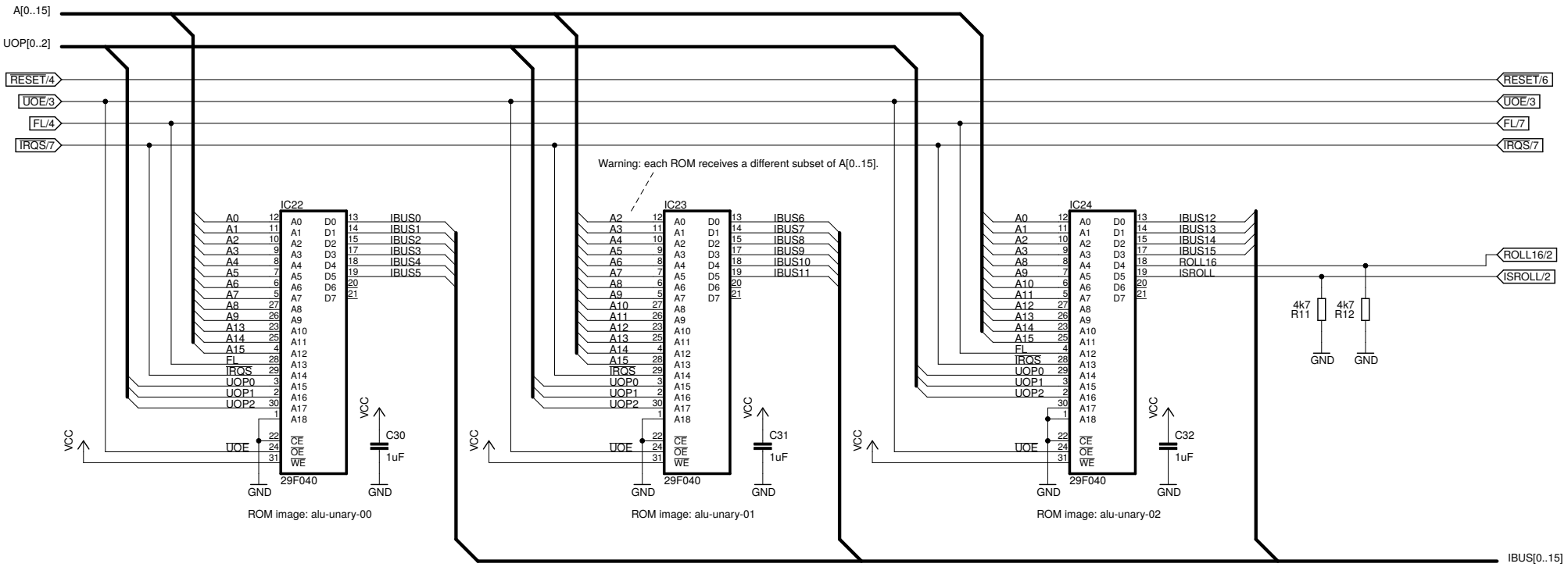



| | |
|---|---|
| U | Title: CFT-PB3-revC |
| | Revision: Rev C |
| | Last Change: 30 Dec 2018 17:07:21 |
| | Drawn by: Alexios 4/7 |
| | Simulation filename: alu.v |
| | More Info: http://www.bedroomlan.org/cft |

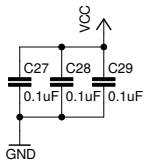
# CFT Mini-Computer

ALU Unary Operators and Constant Store

## Unary Operations and Constant Store




### Decoupling




### Notes

ROMs to be socketed for easy re-programming.

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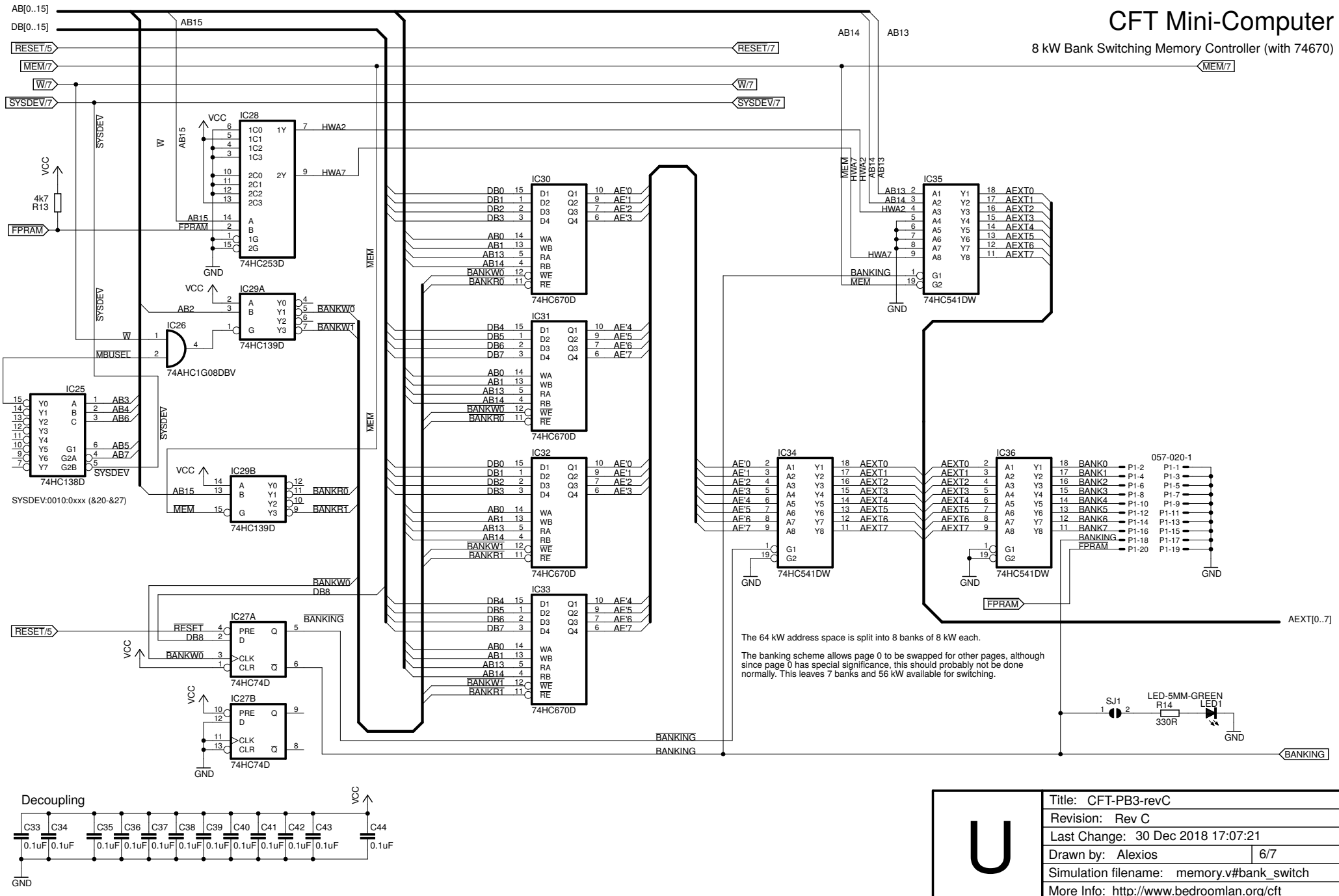
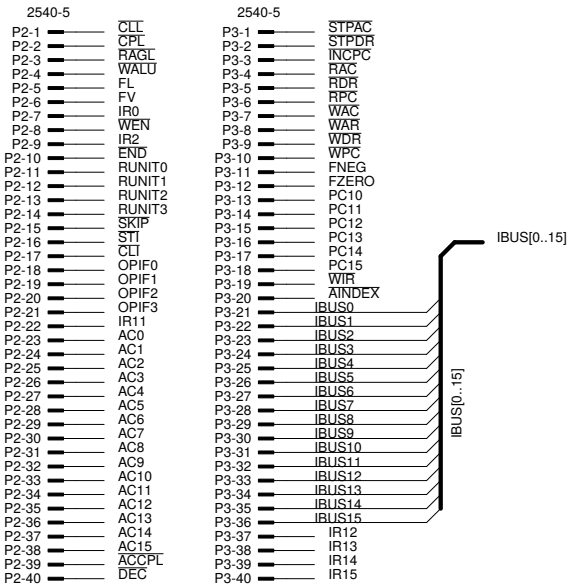
|---|---|
| Title: CFT-PB3-revC | |
| Revision: Rev C | |
| Last Change: 30 Dec 2018 17:07:21 | |
| Drawn by: Alexios | 5/7 |
| Simulation filename: alu.v | |
| More Info: http://www.bedroomlan.org/cft | |


CFT Mini-Computer
8 kW Bank Switching Memory Controller (with 74670)
AB[0..15]
DB[0..15]
RESET/5
MEM/7
W/7
SYSDEV/7
RESET/7
AB14
AB13
IC28
74HC253D
IC30
IC31
IC32
IC33
74HC670D
IC35
74HC541DW
IC34
IC36
IC29A
IC29B
74HC139D
IC26
74AHC1G08DBV
IC25
74HC138D
SYSDEV:0010:0xxx (&20-&27)
IC27A
IC27B
74HC74D
4k7
R13
FPRAM
BANKW0
BANKW1
BANKR0
BANKR1
BANKING
MBUSEL
057-020-1
SJ1
LED-5MM-GREEN
LED1
R14
330R
AEXT[0..7]
The 64 kW address space is split into 8 banks of 8 kW each.
The banking scheme allows page 0 to be swapped for other pages, although since page 0 has special significance, this should probably not be done normally. This leaves 7 banks and 56 kW available for switching.
Decoupling
C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44
0.1uF
GND
VCC
U
Title: CFT-PB3-revC
Revision: Rev C
Last Change: 30 Dec 2018 17:07:21
Drawn by: Alexios
6/7
Simulation filename: memory.v#bank_switch
More Info: http://www.bedroomlan.org/cft

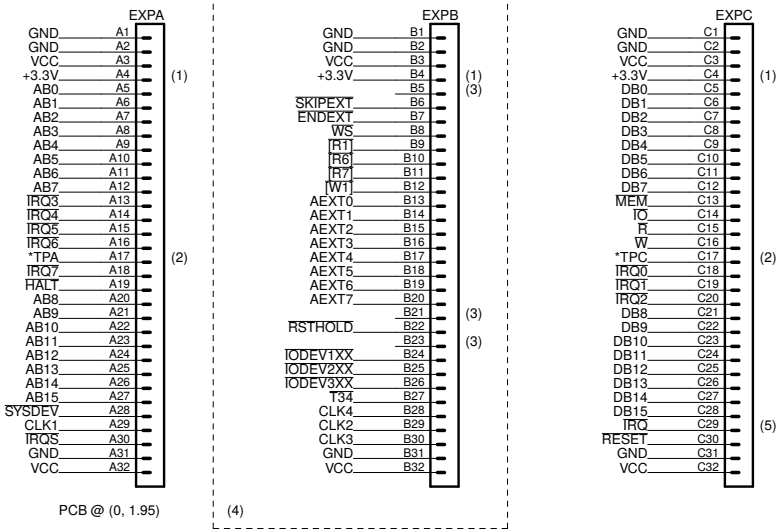
# CFT Mini-Computer

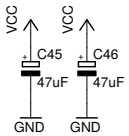
Bus Connectors

## Control Bus (processor bus)




## Expansion Bus (computer bus)




Notes

(1) This pin is connected to a bus bar for power distribution, but the CFT does not (yet) require it. It's likely to be connected to another voltage level like +3.3V for easier interfacing. Reserved for now.

(2) Pins *TPA and *TPC are not bussed. They are locally connected to each card's corresponding test pins (A17 & C17) to serve as test points.

(3) Reserved for future expansion

(4) Cheaper, 64-pin A+C row DIN41662 Type C plugs may be used for most expansion cards.

(5) $\overline{IRQ}$ is provided for systems which lack an interrupt controller ($\overline{IRQ0\text{-}7}$)

U1 HOLE @(0.15, 3.675)
U3 HOLE @(5.775, 3.675)
U2 HOLE @(0.15, 0.25)
U4 HOLE @(5.775, 0.25)

[PCB Logo]

[QR Code http://www.bedroomlan.org/cft (shortened)]

open hardware

open hardware

U

| | |
|---|---|
| Title: CFT-PB3-revC | |
| Revision: Rev J | |
| Last Change: 30 Dec 2018 17:07:21 | |
| Drawn by: Alexios | 7/7 |
| Simulation filename: N/A | |
| More Info: http://www.bedroomlan.org/cft | |