CFT

16-bit Mini-Computer

Collected schematics of the entire computer and its peripherals

This is a work in progress.
Sheets being worked on are indicated by the 'TODO' frame

Sheet status is indicated here IN RED.

D: Draft
U: Untested
T: Initial Testing

NC = New Clock geometry applied

Notes

VCC is +5V unless otherwise indicated.
All decoupling capacitors are ceramic, 100nF.
All ICs are through-hole DIP packages.
All pull-ups and pull-downs are 4.7 kOhm.

TODO:

* Check Signals
* Check Decoupling Capacitors
* Clean Up Layout
* Write & Verify Verilog Model
* Check Packages & IC Families
* Bill of Materials
* DRC

Circuits in need of improvement are marked like this.

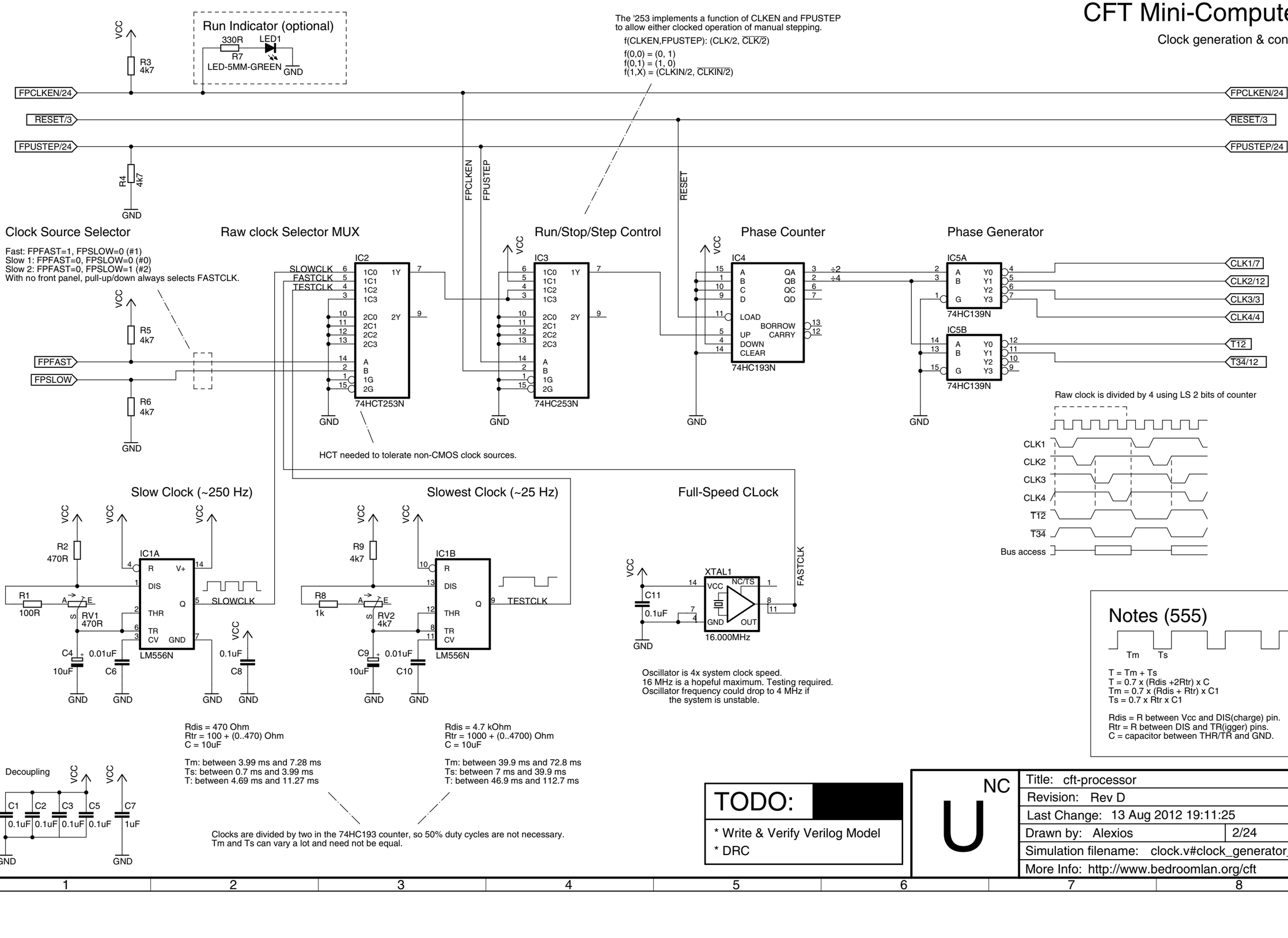
Obsolete sections or circuits are marked like this

Circuits known to be incorrect are marked like this.

NC D	Title: cft-processor
	Revision: Rev B
	Last Change: 13 Aug 2012 19:11:25
	Drawn by: Alexios 1/24
	Simulation filename: register.v#reg_L
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Clock generation & control



TODO:

* Write & Verify Verilog Model
* DRC

Title: cft-processor	
Revision: Rev D	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	2/24
Simulation filename: clock.v#clock_generator_v3	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Reset Handling and Sequencing

On RESET, the reset timer drives RSTHOLD down for 255 CLK pulses.
Using a 16 MHz oscillator, this will assert RSTHOLD for 31.875 us.
Using the slow clock (~400 Hz raw), this will pulse for 1.275 seconds.
Finally, with the testing clock (~40 Hz raw), RSTHOLD will last 12.75 seconds.
NB: CLKIN/2 is RAWCLK divided by 2 (obviously).

RESET/2
CLK3/2
RESET/4
RSTHOLD/4
IBUS[0..15]
CLK3
RESET
RSTHOLD

VCC
R16 4k7

Reset Sources

VCC
R12 4k7
R13 4k7
R15 4k7

FPRESET
POWEROK

74HC14N
IC6C
IC6B
74HC14N

IC7A
74HC05N
IC7C
74HC05N
IC7D
74HC05N

NB: Open Collector gate

LED-5MM-GREEN
330R R11
LED2
Power LED
GND

NB: Open Drain gates

POWEROK comes from the ATX PSU via the front panel.
The PSU holds POWEROK low at power-up (or during brown-outs), until power stabilises. The computer is expected to reset when POWEROK is low.

Reset Button (optional)

JP1
S1
R10 50k
C18 0.1uF
IC6A
74HC14N
R14 4k7

If the reset button and debouncing circuit is installed, this resistor may be left out.

Reset timer

VCC
R17 4k7
RSTHOLD

IC8
CLK
CCKEN
CCLR
RCK
QA
QB
QC
QD
QE
QF
QG
QH
G
RCO
74HC590N
GND

JP2
2ms
4ms
8ms
16ms
32ms

Install exactly ONE jumper.

Reset delay selector. Times shown for 4 MHz processor clock.

System Reset Vector (FFF0)

VCC
GND
RSTHOLD

IC9
IC10
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1
G2
74HC541N

IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15
IBUS[0..15]

Outputs binary 1111'1111'1111'0000 to the IBUS while RSTHOLD is asserted.
This value is picked up by other units of the processor, including the Program Counter, and becomes the computer's boot address.

Decoupling

VCC
C12 0.1uF
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 1uF
GND

IC7E
IC7F
74HC05N
IC7B
IC6D
74HC14N
IC6E
IC6F
74HC14N

NB: Open Drain gate

TODO:

* Write & Verify Verilog Model
* DRC

U

NC

Title: cft-processor	
Revision: Rev D	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	3/24
Simulation filename: reset.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Microcode Sequencer

Notes

32k x 8 (2x256) ICs required for Microcode v4.
512k x 8 ICs are cheaper and easier to come by, though,
so this schematic uses these. Smaller ICs can be substituted.

ROMS to be socketed for easy reprogramming.

Use 70ns or 50ns chips.

Vertical microcode (unit selectors RUNIT, WUNIT and OPIF) are pulled low because a value of zero selects no unit.

$\overline{WS}$: indicates a wait state. Inhibits the uPC counter.
$\overline{HALT}$: halts the processor. The control unit's outputs are at High-Z.
Consequently, the processor is disconnected from all busses.
Control signals are active low and pulled up, so other units (like the front panel) may operate them with the processor halted.

$\overline{RESET}$: while $\overline{RESET}$ is active (low), the microcode ROMs are deselected and their outputs tri-stated to avoid bus contention with units resetting uncleanly.

AINDEX/6
SKIP/6
FL/6
FV/6
IRQS/6
RSTHOLD/3

AINDEX
SKIP
FL
FV
IRQS
RSTHOLD

Microcode bank selection for future expansion or debugging. Bridge or jumper to 0000.

UCB0
UCB1
UCB2
UCB3

SV1

4k7 RN2

GND

Microcode PC

IC12 74HC161

VCC 4k7 R19
4k7 R20

CLK4/2
WS/12

CLK4
WS
HALT
RSTHOLD

UPC0
UPC1
UPC2
UPC3

Open drain
4k7 R18
ENDEXT/24

IC11C 74HC00N
IC11B 74HC00N

END

Microcode ROMs

RN3 4k7

IC13 29F040
IC14 29F040
IC15 29F040

UPC0
UPC1
UPC2
UPC3
AINDEX
SKIP
IR11
IR12
IR13
IR14
IR15
FL
FV
IRQS
RSTHOLD
UCB0
UCB1
UCB2
UCB3

IR11/6
IR12/6
IR13/6
IR14/6
IR15/6

RUNIT0
RUNIT1
RUNIT2
RUNIT3
WUNIT0
WUNIT1
WUNIT2
OPIF0

OPIF1
OPIF2
OPIF3
INCAC
CPL
CLL
STI
CLI

INCPC
INCDR
UINSTR18
MEM
IO
R
WEN
END

4k7 RN1
4k7 RN4
RN5 4k7

C25 1uF
C26 1uF
C27 1uF

ROM image: microcode-00
ROM image: microcode-01
ROM image: microcode-02

Note: $\overline{W}$ is $\overline{WEN} \cdot CLK5$.

RUNIT0/5
RUNIT1/5
RUNIT2/5
RUNIT3/5
WUNIT0/5
WUNIT1/5
WUNIT2/5
OPIF0/5
OPIF1/5
OPIF2/5
OPIF3/5
CPL/5
CLL/5
STI/5
CLI/5
INCAC/5
INCPC/5
INCDR/5
UINSTR18/5
MEM/5
IO/5
R/5
WEN/5
END/5
UCE/7

HALT/24
RESET/3

IC11A 74HC00N
IC11D 74HC00N

UCE

The ROMs may be placed on a daughterboard to facilitate easy expansion of the microcode store. In this case, a 46-pin header (2 power, 18 address, 2 control, 24 data) must be installed. Pull-ups/-downs to stay on the motherboard.

$\overline{UCE}$ is used by the unit decoders to ensure no units are selected when either $\overline{HALT}$ or $\overline{RESET}$ are inactive.

Decoupling

C19 C20 C21 C22 C23 0.1uF
IC12P
C24 1uF

Nota Bene: this sequencer can only run Microcode v.4!

TODO:

* Write & Verify Verilog Model
* DRC

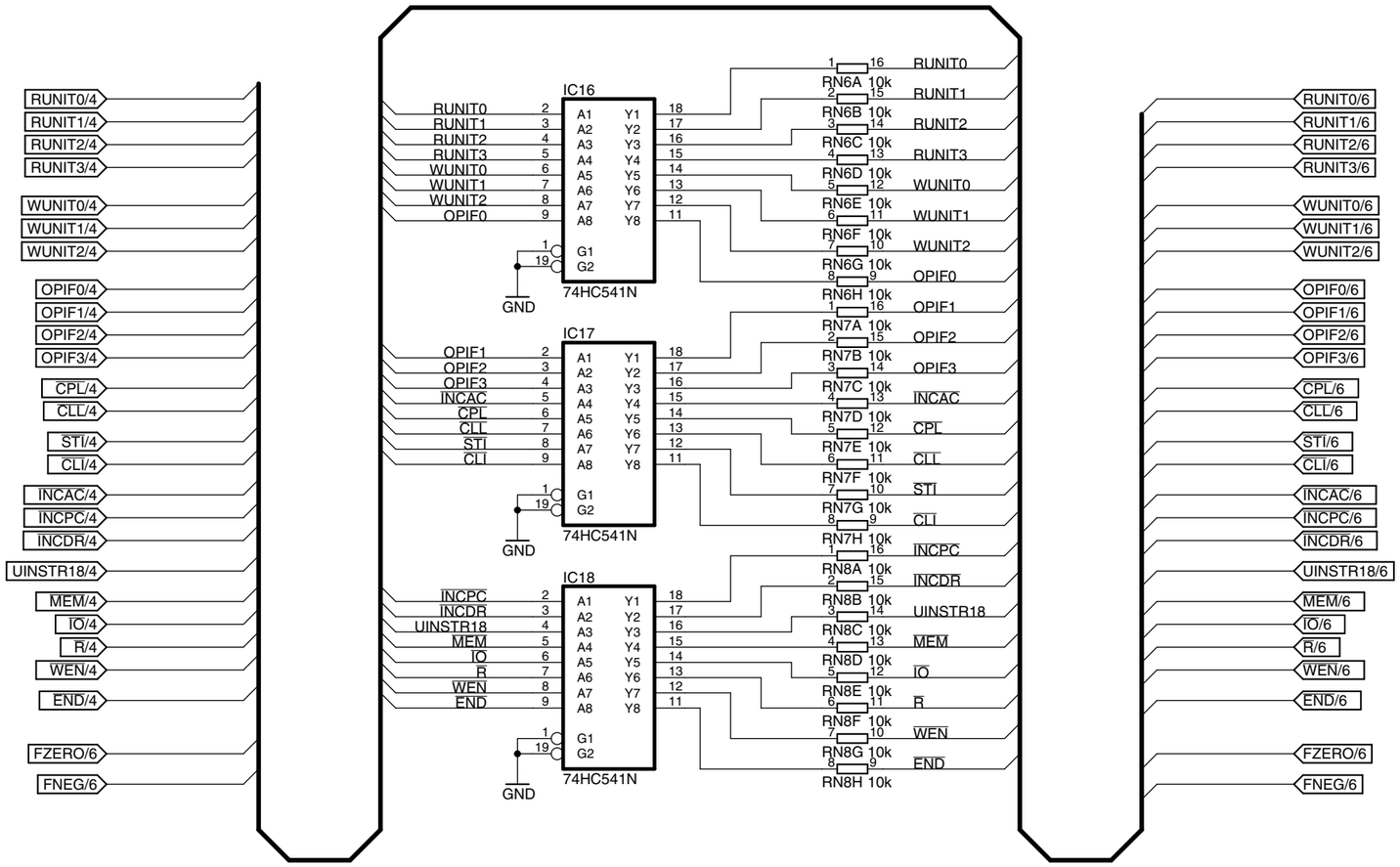
U

Title: cft-processor	
Revision: Rev F	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	4/24
Simulation filename: sequencer.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Microcode Sequencer Signal Hold

Probably Unnecessary -- to be verified in Verilog



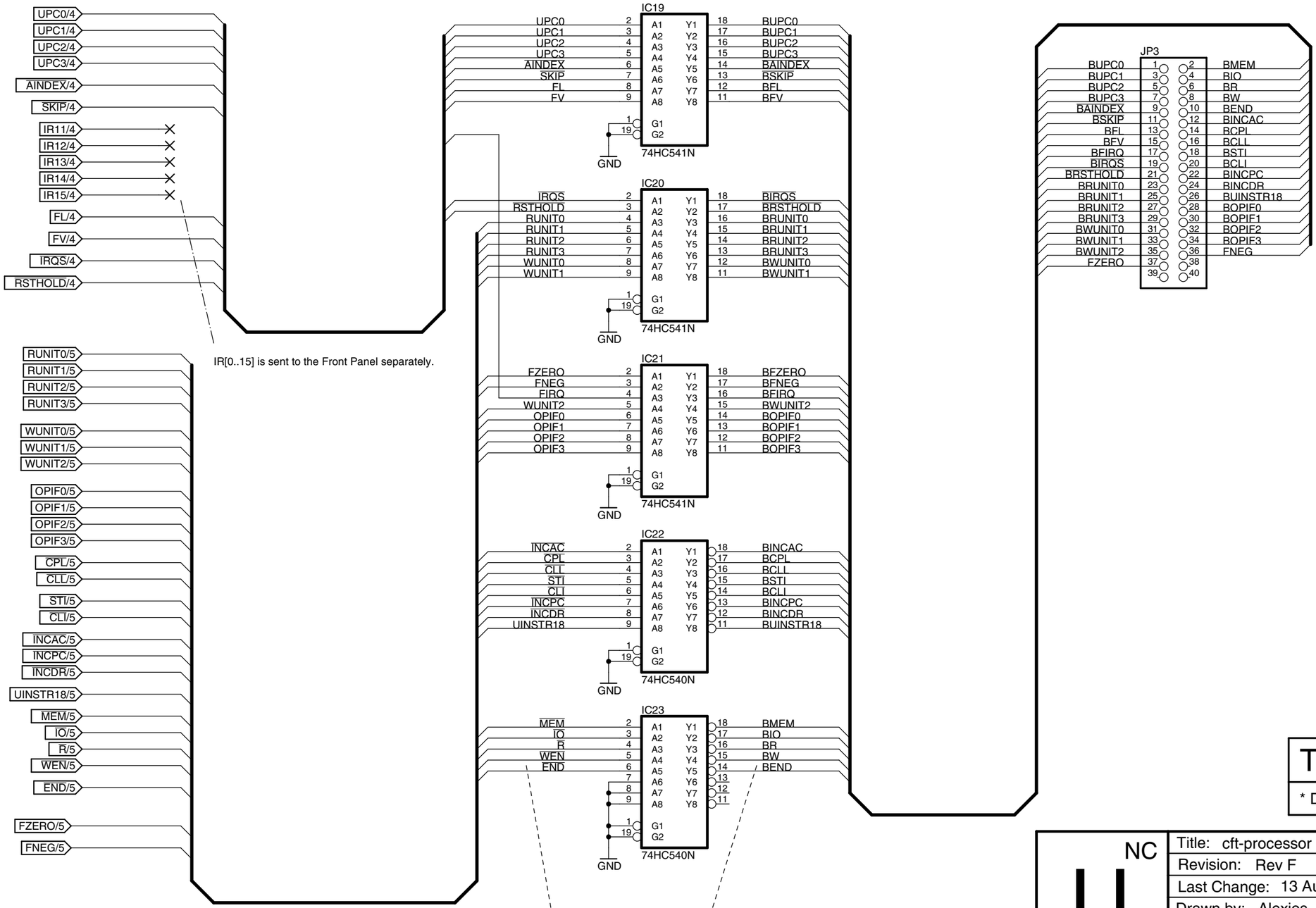
TODO:

* DRC

NC U	Title: cft-processor
	Revision: Rev A
	Last Change: 13 Aug 2012 19:11:25
	Drawn by: Alexios | 5/24
	Simulation filename: N/A
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Microcode Sequencer Front Panel Connections



TODO:

* DRC

U NC

Title: cft-processor	
Revision: Rev F	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	6/24
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Read & Write Unit Decoding

RESET/4
UCE/4
CLK3/3
CLK1/2
RUNIT0/6
RUNIT1/6
RUNIT2/6
RUNIT3/6
WUNIT0/6
WUNIT1/6
WUNIT2/6

RESET/8
UCE/4
CLK3/17
CLK1/24
RUNIT0/18
RUNIT1/18
RUNIT2/18
RUNIT3/18
WUNIT0/6
WUNIT1/6
WUNIT2/6

CLK3 RESET WUNIT2 WUNIT1 WUNIT0 RESET RUNIT3 CLK1 RUNIT2 RUNIT1 RUNIT0 UCE

74HC04N IC24A

IC25 74HC138N
RUNIT0 RUNIT1 RUNIT2 CLK1 RUNIT3 RESET
A B C G1 G2A G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

IC27 74HC541N
UCE UCE GND
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2

VCC RN9 4k7

RUNIT is decoded partially: only 0xxx values are decoded here.
ALU Operation decoding (RUNIT=1xxx) is done on the ALU board.

0000 = Idle
0001 = Reserved
0010 = Read from AGL (RAGL)
0011 = Read from PC (RPC)
0100 = Read from DR (RDR)
0101 = Read from AC (RAC)
0110 = Reserved
0111 = Reserved
1XXX = ALU operation or Constant

Reserved
RAGL/9
RPC/14
RDR/15
RAC/16
Reserved
Reserved
Reserved

IC26 74HC138N
WUNIT0 WUNIT1 WUNIT2 RESET CLK3
A B C G1 G2A G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

IC28 74HC541N
UCE UCE GND
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2

VCC RN10 4k7

Write Unit Decoder:

000 = Idle
001 = Reserved
010 = Write AR (WAR)
011 = Write PC (WPC)
100 = Write IR (WIR)
101 = Write DR (WDR)
110 = Write AC & ALU Port A (WAC)
111 = Write ALU Port B (WALU)

Reserved
WAR/13
WPC/14
WIR/10
WDR/15
WAC/16
WALU/18

When UCE is asserted, unit decoders must tri-state their outputs.

TODO:

* DRC

Decoupling
VCC
C28 0.1uF C29 0.1uF C30 0.1uF C31 0.1uF
C32 1uF
GND

IC24B IC24C IC24D IC24E IC24F 74HC04N

Title:	cft-processor
Revision:	Rev F
Last Change:	13 Aug 2012 19:11:25
Drawn by:	Alexios 7/24
Simulation filename:	unit_decoder.v
More Info:	http://www.bedroomlan.org/cft

U NC

CFT Mini-Computer

Skip/Branch Logic

IR[0..15]

OPIF[0..3]

FNEG/6

FZERO/6

FL/6

FV/6

FNEG/16

FZERO/16

FL/17

FV/19

TODO:

* DRC

OP1 Branch Logic (IR0..IR4)

74HC08N IC30B SV, IC30A SL, IC30D SZ, IC30C SN

IC29A 74HC32N, IC29B 74HC32N

IC29C 74HC32N

OP1_BRANCH = (SV + SL + SZ + SN) XOR IR4

74HC86N IC31A

Worst case propagation delay: 3 x 8.5ns + 9.5ns = 35ns

OP1_BRANCH

OP2 Roll detection (IR0..IR3)

IC32A 74HC32N

IC32B 74HC32N

OP2_ROLL

Condition Multiplexing

IC34 74HC251N

IR3 IR4 IR5 IR6 IR7 IR8 IR9

OPIF0 OPIF1 OPIF2 OPIF3

SKIPMUXLO

Hi = Skip

0000-0111

IC35 74HC251N

FV FL FZERO FNEG OP2_ROLL OP1_BRANCH

OPIF0 OPIF1 OPIF2

SKIPMUXHI

Hi = Skip

1000-1111

IC33A 74HC00N

OPIF3

This generates glitches, but the Skip Flag Register filters them out.

VCC 4k7 R23

VCC 4k7 R22

IC33B 74HC00N

Microcode v.4 OPIF field

OPIF = 0000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 0001: IF3 ($\overline{SKIP}$ = IR3)
OPIF = 0010: IF4 ($\overline{SKIP}$ = IR4)
OPIF = 0011: IF5 ($\overline{SKIP}$ = IR5)
OPIF = 0100: IF6 ($\overline{SKIP}$ = IR6)
OPIF = 0101: IF7 ($\overline{SKIP}$ = IR7)
OPIF = 0110: IF8 ($\overline{SKIP}$ = IR8)
OPIF = 0111: IF9 ($\overline{SKIP}$ = IR9)

OPIF = 1000: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1001: IDLE ($\overline{SKIP}$ = 1)
OPIF = 1010: IFV ($\overline{SKIP}$ = IFV, skip if V=0)
OPIF = 1011: IFL ($\overline{SKIP}$ = IFL, skip if L=0)
OPIF = 1100: IFZERO ($\overline{SKIP}$ = IFZERO, skip if Z=0)
OPIF = 1101: IFNEG ($\overline{SKIP}$ = FNEG, skip if N=0)
OPIF = 1110: IFROLL ($\overline{SKIP}$ = IR0 + IR1 + IR2)
OPIF = 1111: IFBRANCH Logic

Skip flag register

SKIP0

IC33C 74HC00N

IC36A 74HC74N

SKIP/6

VCC 4k7 R21

Open drain

SKIPEXT/24

CLK4/4

RESET/7

GND

Decoupling

C33 C34 C35 C36 C37 C38 C39 C40 0.1uF

C41 1uF

IC32D IC32C 74HC32N

IC31B IC31C 74HC86N

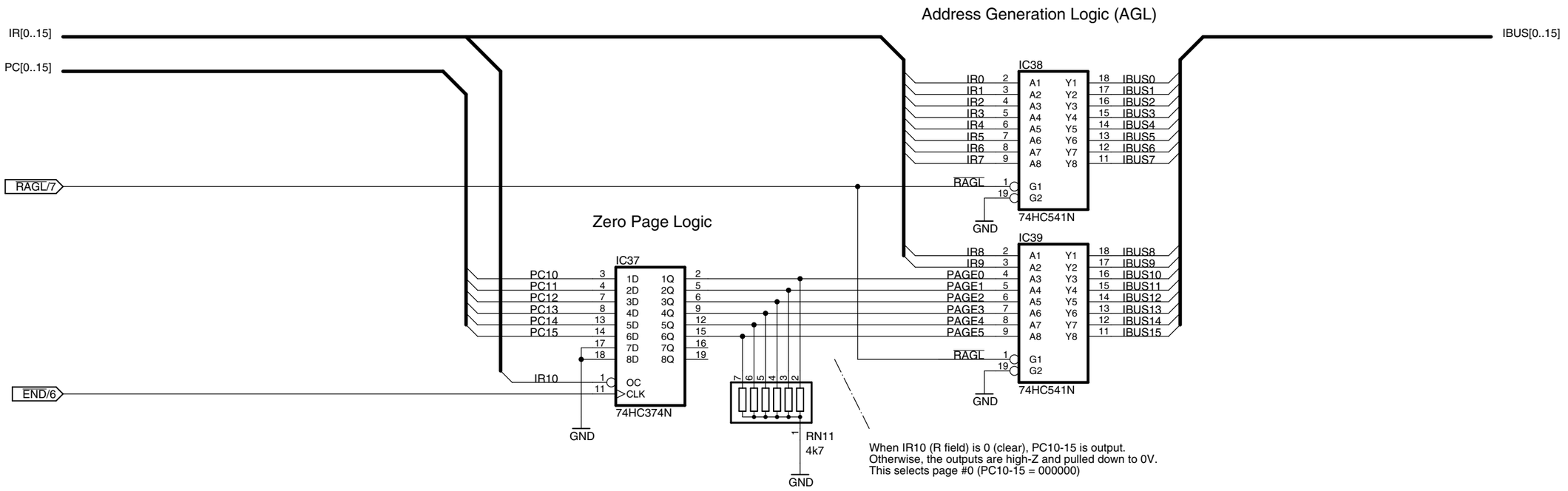
IC31D IC29D 74HC86N, 74HC32N

IC33D 74HC00N

NC U	Title: cft-processor
	Revision: Rev F
	Last Change: 13 Aug 2012 19:11:25
	Drawn by: Alexios 8/24
	Simulation filename: skip_unit.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Address Generation Logic



Notes

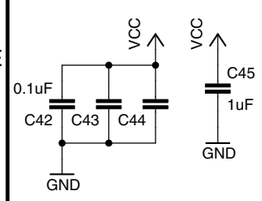
The value of the PC is clocked into the D-Flip Flop on the rising edge of $\overline{\text{END}}$.
At that point, the PC holds the value of the instruction about to be fetched.

If this registering doesn't take place, by the time the AGL is read, the PC will have been incremented (at the end of the fetch cycle), and pointing to the next instruction.

Thus, the AGL would generate addresses for PC+1. This works as the user expects for the first 1023 page offsets, and fails on the 1024th, where the AGL produces an address for the next page.

This would make programming with page-relative modes much less intuitive.

Decoupling



TODO:

* DRC

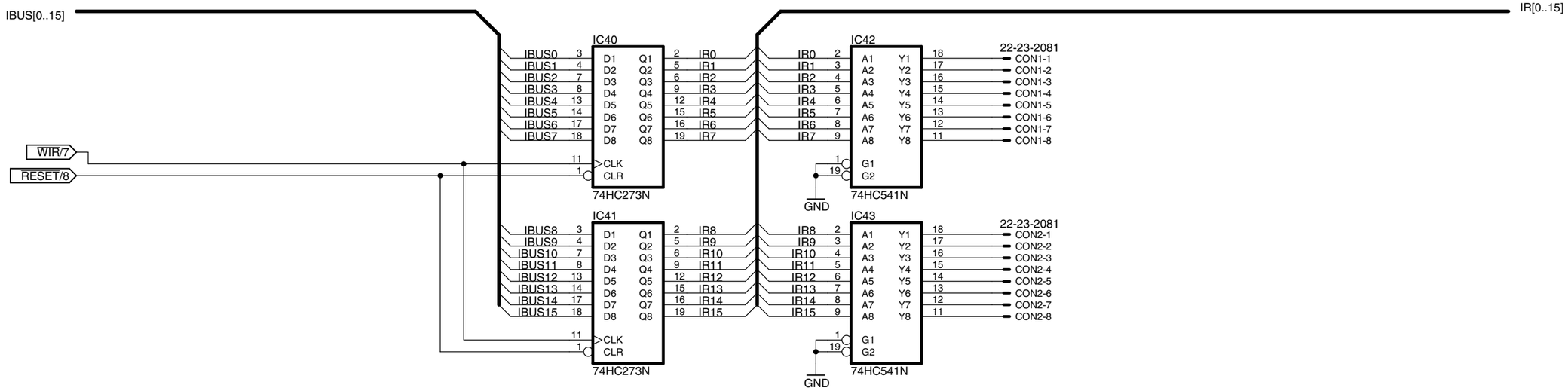
NC U	Title: cft-processor
	Revision: Rev B
	Last Change: 13 Aug 2012 19:11:25
	Drawn by: Alexios 9/24
	Simulation filename: agl.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

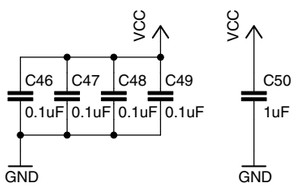
Instruction Register

Instruction Register (IR)

Front Panel Buffers & Connectors



Decoupling



TODO:

* DRC

Title: cft-processor	
Revision: Rev B	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	10/24
Simulation filename: ir.v	
More Info: http://www.bedroomlan.org/cft	

U NC

CFT Mini-Computer

Interrupt State Machine

END/9
RESET/10
STI/6
CLI/6

END/13
RESET/12

VCC
R24
4k7
IRQ/22

$\overline{IRQ}$ should be driven by open-drain gates.
It is pulled up here.

Interrupt Flag (Asynchronous)

STI
RESET
CLI
IC44A
74HC08N
RESET_OR_CLI
IC46A
PRE
J
CLK
K
CLR
Q
74HC112N
GND
FINT

Masking and State (Synchronous)

FINT
IRQ
IC45A
74HC32N
MASKEDIRQ
RESET_OR_CLI
IC46B
74HC112N
GND
FIRQ/6

Note: for testing purposes.

Interrupts Enabled light (optional)

LED-5MM-GREEN
LED3
330R
R25
GND

Safe Interrupt Signalling

IRQ
IRQS
Interrupt Microprogram Running

Assert $\overline{IRQ}$, wait for $\overline{IRQS}$, deassert $\overline{IRQ}$.

Interrupt Request Register FF (Instruction-synchronous)

VCC
IC36B
PRE
D
CLK
CLR
Q
74HC74N
FIRQ
END
RESET
IRQS/20

This is also the interrupt acknowledge signal.

Shared with IC36.

Interrupt Seen light (optional)

LED-5MM-GREEN
LED4
330R
R26
GND

Interrupt Flag Waveforms

RESET
STI
CLI
FINT

Masking and $\overline{IRQ}$ Waveforms

RESET
CLI
FINT
IRQ
FIRQ

Masking and $\overline{IRQ}$ Waveforms (Instruction-synchronous)

END
RESET
CLI
FIRQ
IRQS

Notes

The Interrupt flag denotes our disposition to handle incoming interrupts (allow or ignore).
At $\overline{RESET}$ time, interrupts are cleared and further interrupts are masked (ignored).
The falling edge of $\overline{CLI}$ or $\overline{RESET}$ clears the interrupt flag, ignoring interrupts.
The falling edge of $\overline{STI}$ sets the flag, allowing interrupts.

When the interrupt flag is set, the falling edge of $\overline{IRQ}$ triggers an interrupt (FIRQ high).

This is ignored until the end of the current instruction (falling edge of $\overline{END}$).
At that point, the register FF clocks FIRQ in, asserting $\overline{IRQS}$ to the microcode sequencer.
The K input of the flip flop is held constantly high. With FIRQ high, this is a toggle action.

At the next instruction (falling edge of $\overline{END}$), $\overline{IRQS}$ would toggle again.
Before this happens, the interrupt microprogram asserts $\overline{CLI}$, clearing FIRQ, so no further toggling takes place. Instead, with K low and J high, $\overline{IRQS}$ is deasserted, resuming normal excecution.

TODO:

* DRC

Decoupling

VCC
C51 0.1uF
C52 0.1uF
C53 0.1uF
C54 0.1uF
C55 0.1uF
C56 1uF
GND

IC44B
IC44C
74HC08N
IC44D
IC45B
74HC08N
IC45C
IC45D
74HC32N

NC	Title: cft-processor
	Revision: Rev B
	Last Change: 13 Aug 2012 19:11:25
	Drawn by: Alexios 11/24
	Simulation filename: int.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Data Bus Driver & Bus Termination

RESET/11
WS/4
MEM/6
IO/6
R/6
WEN/6
T34/2
CLK2/2
CLK4/8
IBUS[0..15]

RESET/13
WS/24
MEM/13
IO/13
R/22
WEN/6
T34/18
CLK2/24
CLK4/24

Wait State

RESET, CLK2, T34, WS

IC51B 74HC32N

IC47A
PRE D Q
CLK CLR Q
74HC74N
WAITING

CLK2
RESET
GND

IC51C 74HC32N

T34, IO, MEM

IC48A 74HC08N

IC48B 74HC08N

Write Strobe Generation

CLK4, WEN

IC51A 74HC32N

IC51D 74HC32N

WAITING

Asserting WAITING inhibits W strobes.

IC52A 74HC04N

IC52B 74HC04N

IC52C 74HC04N

IC48D 74HC08N

IC48C 74HC08N

RESET

VCC

IC47B
PRE D Q
CLK CLR Q
74HC74N

W/21

Data Bus Transceiver

IBUS[0..15]

DB[0..15]

IC49 74HC245N
IBUS0 DB0
IBUS1 DB1
IBUS2 DB2
IBUS3 DB3
IBUS4 DB4
IBUS5 DB5
IBUS6 DB6
IBUS7 DB7
R
BUSEN
DIR G

IC50 74HC245N
IBUS8 DB8
IBUS9 DB9
IBUS10 DB10
IBUS11 DB11
IBUS12 DB12
IBUS13 DB13
IBUS14 DB14
IBUS15 DB15
R
BUSEN
DIR G

DB[0..15]

DB[0..15]

Bus Hold

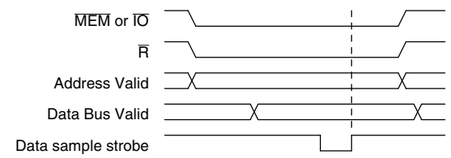
IC53 74HC541N
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
A1..A8 Y1..Y8
G1 G2
GND

IC54 74HC541N
DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15
A1..A8 Y1..Y8
G1 G2
GND

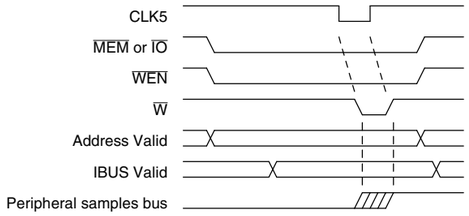
RN12A10k DB0
RN12B10k DB1
RN12C10k DB2
RN12D10k DB3
RN12E10k DB4
RN12F10k DB5
RN12G10k DB6
RN12H10k DB7
RN13A10k DB8
RN13B10k DB9
RN13C10k DB10
RN13D10k DB11
RN13E10k DB12
RN13F10k DB13
RN13G10k DB14
RN13H10k DB15

Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.

Memory or I/O Space Read Waveforms



Memory or I/O Space Write Waveforms



Decoupling

VCC

C57 0.1uF, C58 0.1uF, C59 0.1uF, C60 0.1uF, C61 0.1uF, C62 1uF

GND

74HC04N

IC52F, IC52E, IC52D

GND

TODO:

* DRC

U

Title:	cft-processor
Revision:	Rev C
Last Change:	13 Aug 2012 19:11:25
Drawn by:	Alexios
	12/24
Simulation filename:	databus.v
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

Address Register, Address Bus Drivers & Termination, Autoindex Logic, Device Decoder

MEM/12
IO/12
IC55A
74HC08N
ABEN

IBUS[0..15]

Address Register (AR)

IC56 — 74HC273N
IC57 — 74HC273N
WAR/7
RESET/12

Address Bus Drive Logic

IC58 — 74HC541N
IC59 — 74HC541N
ABEN

Address Bus Hold

IC61 — 74HC541N
IC62 — 74HC541N

AB[0..15]

RN14A 10k
RN14B 10k
RN14C 10k
RN14D 10k
RN14E 10k
RN14F 10k
RN14G 10k
RN14H 10k
RN15A 10k
RN15B 10k
RN15C 10k
RN15D 10k
RN15E 10k
RN15F 10k
RN15G 10k
RN15H 10k

Or Check SN74AC1071D (Farnell 1741471), 10-bit bus hold, 14SOIC.
Alternatively, SN74ACT1073DW (Farnell 1741471), 16-bit, 20SOIC.

TODO:

* DRC

END/11
END
IO

IC60 — 74HC688N
AR15

Autoindex Logic

IC63A — 74HC74N
AINDEX/23

I/O Device Address Decoder

IC65 — 74HC138N
IC64 — 74HC688N
ABEN
IO

SYSDEV/21
IODEV1XX/24
IODEV2XX/24
IODEV3XX/24

Decodes I/O addresses 0n00-0nFF to simplify interfacing.

For n = 0, SYSDEV is asserted.
For n = 1, IODEV1XX is asserted.
For n = 2, IODEV2XX is asserted.
For n = 3, IODEV3XX is asserted.

Other devices must be decoded ad hoc.

Notes (Autoindex Logic)

This evaluates the function:

AINDEX = AR == 0000'0000'1XXX'XXXX

It is necessary to register AINDEX because AR is changed during execution of an indirect mode instruction.

The flag is cleared at the end of the instruction, when END is asserted.

Decoupling

C63 C64 C65 C66 C67 C68 C69 C70 C71 — 0.1uF
C72 — 1uF

IC55D, IC55B, IC55C — 74HC08N
IC63B — 74HC74N

NC	Title: cft-processor
	Revision: Rev A
	Last Change: 13 Aug 2012 19:11:25
	Drawn by: Alexios — 13/24
	Simulation filename: addressing.v
	More Info: http://www.bedroomlan.org/cft

CFT Mini-Computer

Major Registers: Program Counter (PC)

RPC/7
WPC/7
INCPC/6
RESET/13
IBUS[0..15]

NB: this is RESET inverted, fed to all 3 major registers' CLEAR signals ('193).

RESET/15
IBUS[0..15]

74HC04N IC66A

Register & Increment

VCC

IC67 74HC193N
IBUS0 IBUS1 IBUS2 IBUS3 → A B C D → PC0 PC1 PC2 PC3
WPC → LOAD
INCPC → UP
RESET → CLEAR
BORROW CARRY DOWN

IC68 74HC193N
IBUS4 IBUS5 IBUS6 IBUS7 → A B C D → PC4 PC5 PC6 PC7
WPC → LOAD
RESET → CLEAR

IC69 74HC193N
IBUS8 IBUS9 IBUS10 IBUS11 → A B C D → PC8 PC9 PC10 PC11
WPC → LOAD
RESET → CLEAR

IC70 74HC193N
IBUS12 IBUS13 IBUS14 IBUS15 → A B C D → PC12 PC13 PC14 PC15
WPC → LOAD
RESET → CLEAR

Tri-State Buffering

IC71 74HC541N
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 → A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
G1 G2

IC72 74HC541N
PC8 PC9 PC10 PC11 PC12 PC13 PC14 PC15 → A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15
G1 G2

PC[0..15]

Front Panel Buffers & Connectors

IC73 74HC541N
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 → A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → 22-23-2081 CON3-1 CON3-2 CON3-3 CON3-4 CON3-5 CON3-6 CON3-7 CON3-8
G1 G2
GND

IC74 74HC541N
PC8 PC9 PC10 PC11 PC12 PC13 PC14 PC15 → A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 → 22-23-2081 CON4-1 CON4-2 CON4-3 CON4-4 CON4-5 CON4-6 CON4-7 CON4-8
G1 G2
GND

Decoupling

VCC VCC
C73 0.1uF C74 0.1uF C75 0.1uF C76 0.1uF C77 0.1uF C78 0.1uF C79 0.1uF C80 0.1uF C81 1uF
GND GND

74HC04N IC66C IC66B 74HC04N IC66E IC66D 74HC04N IC66F 74HC04N
GND GND GND

TODO:
* DRC

NC

Title: cft-processor	
Revision: Rev B	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	14/24
Simulation filename: register.v#reg_pc	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Major Registers: Data Register (DR)

RDR/7
WDR/7
INCDR/6
RESET/14
IBUS[0..15]

NB: this is $\overline{\text{RESET}}$ inverted.

RESET/16
IBUS[0..15]

Register & Increment

VCC

IC75 74HC193N
IBUS0 15 — A — QA 3 — DR0
IBUS1 1 — B — QB 2 — DR1
IBUS2 10 — C — QC 6 — DR2
IBUS3 9 — D — QD 7 — DR3
$\overline{\text{WDR}}$ 11 — LOAD
$\overline{\text{INCDR}}$ 5 — UP
4 — DOWN
RESET 14 — CLEAR
BORROW 13
CARRY 12

IC76 74HC193N
IBUS4 15 — A — QA 3 — DR4
IBUS5 1 — B — QB 2 — DR5
IBUS6 10 — C — QC 6 — DR6
IBUS7 9 — D — QD 7 — DR7
$\overline{\text{WDR}}$ 11 — LOAD
5 — UP
4 — DOWN
RESET 14 — CLEAR
BORROW 13
CARRY 12

IC77 74HC193N
IBUS8 15 — A — QA 3 — DR8
IBUS9 1 — B — QB 2 — DR9
IBUS10 10 — C — QC 6 — DR10
IBUS11 9 — D — QD 7 — DR11
WDR 11 — LOAD
5 — UP
4 — DOWN
RESET 14 — CLEAR
BORROW 13
CARRY 12

IC78 74HC193N
IBUS12 15 — A — QA 3 — DR12
IBUS13 1 — B — QB 2 — DR13
IBUS14 10 — C — QC 6 — DR14
IBUS15 9 — D — QD 7 — DR15
WDR 11 — LOAD
5 — UP
4 — DOWN
RESET 14 — CLEAR
BORROW 13
CARRY 12

Tri-State Buffering

IC79 74HC541N
DR0 2 — A1 — Y1 18 — IBUS0
DR1 3 — A2 — Y2 17 — IBUS1
DR2 4 — A3 — Y3 16 — IBUS2
DR3 5 — A4 — Y4 15 — IBUS3
DR4 6 — A5 — Y5 14 — IBUS4
DR5 7 — A6 — Y6 13 — IBUS5
DR6 8 — A7 — Y7 12 — IBUS6
DR7 9 — A8 — Y8 11 — IBUS7
1 — G1
19 — G2

IC80 74HC541N
DR8 2 — A1 — Y1 18 — IBUS8
DR9 3 — A2 — Y2 17 — IBUS9
DR10 4 — A3 — Y3 16 — IBUS10
DR11 5 — A4 — Y4 15 — IBUS11
DR12 6 — A5 — Y5 14 — IBUS12
DR13 7 — A6 — Y6 13 — IBUS13
DR14 8 — A7 — Y7 12 — IBUS14
DR15 9 — A8 — Y8 11 — IBUS15
1 — G1
19 — G2

Front Panel Buffers & Connectors

IC81 74HC541N
DR0 2 — A1 — Y1 18 — 22-23-2081 CON5-1
DR1 3 — A2 — Y2 17 — CON5-2
DR2 4 — A3 — Y3 16 — CON5-3
DR3 5 — A4 — Y4 15 — CON5-4
DR4 6 — A5 — Y5 14 — CON5-5
DR5 7 — A6 — Y6 13 — CON5-6
DR6 8 — A7 — Y7 12 — CON5-7
DR7 9 — A8 — Y8 11 — CON5-8
1 — G1
19 — G2
GND

IC82 74HC541N
DR8 2 — A1 — Y1 18 — 22-23-2081 CON6-1
DR9 3 — A2 — Y2 17 — CON6-2
DR10 4 — A3 — Y3 16 — CON6-3
DR11 5 — A4 — Y4 15 — CON6-4
DR12 6 — A5 — Y5 14 — CON6-5
DR13 7 — A6 — Y6 13 — CON6-6
DR14 8 — A7 — Y7 12 — CON6-7
DR15 9 — A8 — Y8 11 — CON6-8
1 — G1
19 — G2
GND

DR[0..15]

Decoupling

VCC
C82 0.1uF
C83 0.1uF
C84 0.1uF
C85 0.1uF
C86 0.1uF
C87 0.1uF
C88 0.1uF
C89 0.1uF
GND

VCC
C90 1uF
GND

TODO:

* DRC

UNC

Title:	cft-processor
Revision:	Rev C
Last Change:	13 Aug 2012 19:11:25
Drawn by: Alexios	15/24
Simulation filename:	register.v#reg_dr
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

Accumulator (AC), Zero Flag & Negative Flag

RAC/7
WAC/7
INCAC/6
RESET/15
IBUS[0..15]

Register & Increment

IC83 — 74HC193N
IC84 — 74HC193N
IC85 — 74HC193N
IC86 — 74HC193N

IBUS0 IBUS1 IBUS2 IBUS3 → AC0 AC1 AC2 AC3
IBUS4 IBUS5 IBUS6 IBUS7 → AC4 AC5 AC6 AC7
IBUS8 IBUS9 IBUS10 IBUS11 → AC8 AC9 AC10 AC11
IBUS12 IBUS13 IBUS14 IBUS15 → AC12 AC13 AC14 AC15

WAC
INCAC
DECAC
RESET

VCC
4k7
R27
DECAC

DECAC reserved for future expansion

Tri-State Buffering

IC87 — 74HC541N
IC88 — 74HC541N

AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7 → IBUS0 IBUS1 IBUS2 IBUS3 IBUS4 IBUS5 IBUS6 IBUS7
AC8 AC9 AC10 AC11 AC12 AC13 AC14 AC15 → IBUS8 IBUS9 IBUS10 IBUS11 IBUS12 IBUS13 IBUS14 IBUS15

Zero Flag

IC90 — 74HC688N
IC89 — 74HC688N

AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7
AC8 AC9 AC10 AC11 AC12 AC13 AC14 AC15

Front Panel Buffers & Connectors

IC92 — 74HC541N
IC93 — 74HC541N

AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7 → CON7-1 CON7-2 CON7-3 CON7-4 CON7-5 CON7-6 CON7-7 CON7-8
AC8 AC9 AC10 AC11 AC12 AC13 AC14 AC15 → CON8-1 CON8-2 CON8-3 CON8-4 CON8-5 CON8-6 CON8-7 CON8-8

22-23-2081

GND

AC15 = FNEG → FNEG/23

IC91A — 74HC04N
FZERO/23

INCCPL
Asynchronous toggle of L

AC[0..15]

Decoupling

C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 — 0.1uF
C101 — 1uF
VCC
GND

IC91B IC91C IC91D IC91E IC91F — 74HC04N

TODO:

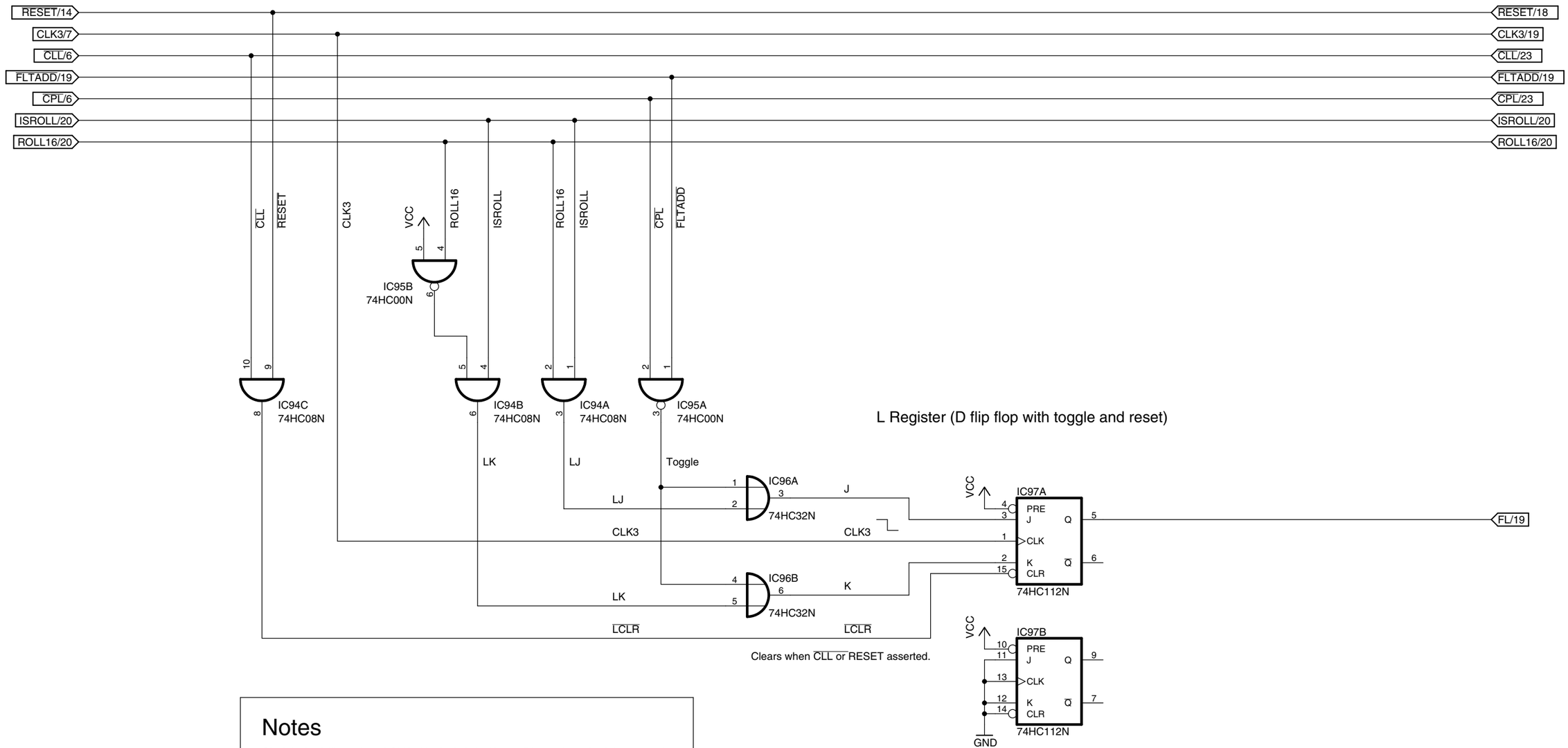
* DRC

NC

Title:	cft-processor
Revision:	Rev C
Last Change:	13 Aug 2012 19:11:25
Drawn by:	Alexios
	16/24
Simulation filename:	register.v#reg_ac
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

The L Register



Notes

Clock is the falling edge of CLK5 (the 'write' clock), so all inputs have had time to settle.

Since FLTADD is registered on the rising edge of CLK5, this implies that ADD carry out will toggle L one clock period after the addition itself.

Clear sources (asynchronous):

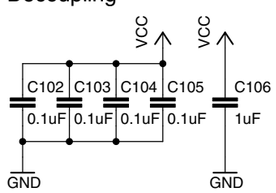
CLL resets it (L=0)
RESET resets it. (L=0)

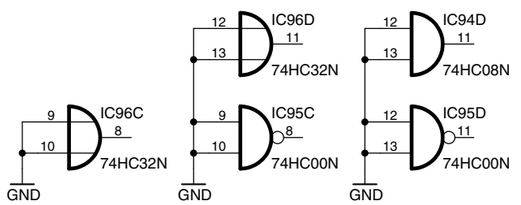
Data out from a roll instruction sets the L register explicitly when L_LATCH is high.

Toggle Sources (synchronous, to avoid glitches):

ALU carry out (FLD)
CPL toggles it (L=L)

Decoupling





TODO:

* DRC

U

NC

Title: cft-processor	
Revision: Rev B	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	17/24
Simulation filename: register.v#reg_L	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Arithmetic/Logic Unit: Decoding Logic

RUNIT[0..3]
IR[0..15]
IBUS[0..15]
WALU/7
RSTHOLD/6
RESET/17
T34/12

IBUS[0..15]
WALU/23
RSTHOLD/6
RESET/19
T34/24

WALU
IBUS[0..15]
RUNIT0
RUNIT1
IR0
IR2
T34
RESET
RSTHOLD
RUNIT3
RUNIT2

ALU Port B Buffer

B[0..15]

IC98
IBUS0 2 1D 1Q 19 B0
IBUS1 3 2D 2Q 18 B1
IBUS2 4 3D 3Q 17 B2
IBUS3 5 4D 4Q 16 B3
IBUS4 6 5D 5Q 15 B4
IBUS5 7 6D 6Q 14 B5
IBUS6 8 7D 7Q 13 B6
IBUS7 9 8D 8Q 12 B7
11 CLK
1 OC
74HC574N
GND

IC99
IBUS8 2 1D 1Q 19 B8
IBUS9 3 2D 2Q 18 B9
IBUS10 4 3D 3Q 17 B10
IBUS11 5 4D 4Q 16 B11
IBUS12 6 5D 5Q 15 B12
IBUS13 7 6D 6Q 14 B13
IBUS14 8 7D 7Q 13 B14
IBUS15 9 8D 8Q 12 B15
11 CLK
1 OC
74HC574N
GND

Unary Operation Decoder

UOP2
ROLLOP0
IR0
RUNIT0
ROLLOP2
IR2
RUNIT1

IC101
1C0 1C1 1C2 1C3 1Y 7 UOP0
2C0 2C1 2C2 2C3 2Y 9 UOP1
A B 1G 2G
74HC253N
GND

IC100A
1 2 3
74HC32N
GND

These buffers are used to tristate the binary ALU ROMs.
The $\overline{OE}$ line on these ROMs is permanently low, to allow parallel execution.
This allows the most expensive op, ADD, to start fetching as soon
as AC is loaded, allowing a full clock cycle for carry propagation.
Since ADD can take up to 210ns to propagate carry, this allows
the processor to reach a theoretical clock speed of around 4 MHz.

IC102
RUNIT2 1 A
RUNIT3 2 B
RSTHOLD 3 C
RESET 6 G1
T34 4 G2A
5 G2B
Y0 15 Y1 14 Y2 13 Y3 12 Y4 11 Y5 10 Y6 9 Y7 7
74HC138N
GND

IC103
Y0 2 Y1 3 Y2 4 Y3 5 Y4 6 Y5 7 Y6 8 Y7 9
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
18 IBUS0 17 IBUS1 16 IBUS2 15 IBUS3 14 IBUS4 13 IBUS5 12 IBUS6 11 IBUS7
1 19 G1 G2
74HC541N

BOE

IC104
Y8 2 Y9 3 Y10 4 Y11 5 Y12 6 Y13 7 Y14 8 Y15 9
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
18 IBUS8 17 IBUS9 16 IBUS10 15 IBUS11 14 IBUS12 13 IBUS13 12 IBUS14 11 IBUS15
1 19 G1 G2
74HC541N

ALU Operation ROM selector (unary/binary)

Y[0..15]
UOE/20
BOE/19
UOP[0..2]
B[0..15]

Decoupling

VCC
C107 C108 C109 C110 0.1uF 0.1uF 0.1uF 0.1uF
C111 1uF
GND

74HC32N IC100D 11 12 13
IC100B 4 6
74HC32N IC100C 5 9
74HC32N 10 8
GND

NC U	Title: cft-processor	
	Revision: Rev B	
	Last Change: 13 Aug 2012 19:11:25	
	Drawn by: Alexios	18/24
	Simulation filename: alu.v	
	More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

ALU Binary Operators

B[0..15]
AC[0..15]
RUNIT[0..3]
RESET/18
CLK3/17
BOE/18
FL/17

RESET/20
CLK3/24
BOE/18
FL/20

ALU Binary Operator ROMs

IC105 — 29F040 — ROM image: alu-binary-6bit-00
IC106 — 29F040 — ROM image: alu-binary-6bit-00
IC107 — 29F040 — ROM image: alu-binary-4bit-00

C118 1uF
C119 1uF
C120 1uF
4k7 R28
4k7 R29

Flag Strobe Generation

IC108 — 74HC253N

AB (BOE FLATCH) -> FLAGCLK
A = BOE = 0 and B = FLATCH = 1 -> Input 01 = xC2 = CLK3

IC109B — 74HC74N
IC109A — 74HC74N

Y[0..15]

Decoupling

C112 0.1uF, C113 0.1uF, C114 0.1uF, C115 0.1uF, C116 0.1uF, C117 1uF

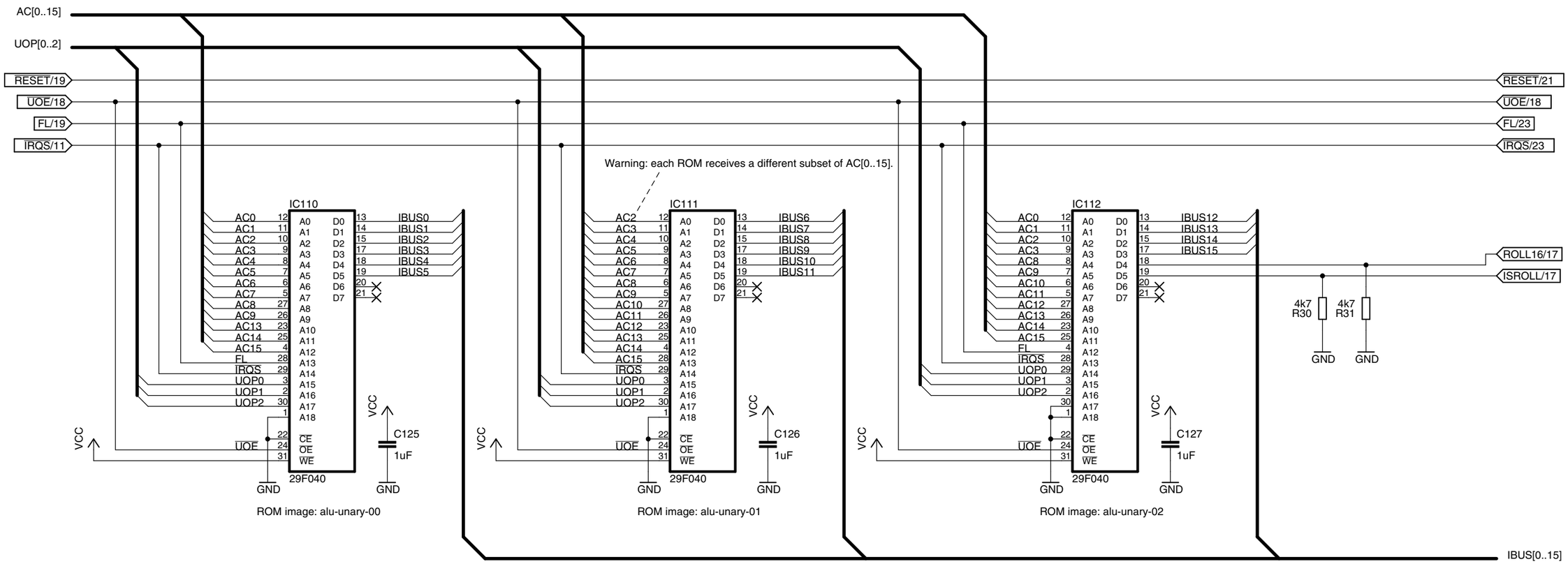
TODO:
* DRC

Title:	cft-processor
Revision:	Rev A
Last Change:	13 Aug 2012 19:11:25
Drawn by:	Alexios 19/24
Simulation filename:	alu.v
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

ALU Unary Operators and Constant Store

Unary Operations and Constant Store

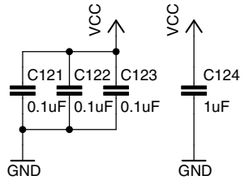


ROM image: alu-unary-00

ROM image: alu-unary-01

ROM image: alu-unary-02

Decoupling



Notes

ROMs to be socketed for easy re-programming.

TODO:

* DRC

NC

U

Title: cft-processor	
Revision: Rev B	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	20/24
Simulation filename: alu.v	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

8 kW Bank Switching Memory Controller (without 74670)

AB[0..15]

DB[0..15]

AB14

AB13

RESET/20 → RESET/22

MEM/13 → MEM/24

W/12 → W/22

SYSDEV/13 → SYSDEV/22

AB15RAM → AB15RAM

IC114 74HC138N: AB0 AB1 AB2 → A B C; AB6 → G1; AB5 → G2A; AB7 → G2B; Y0..Y7 → BANKW0..BANKW7

IC113A 74HC32N: 1, 2 → 3

IC113D 74HC32N: W, SYSDEV → 11

IC115 74HC138N: AB13 AB14 AB15 → A B C; VCC → G1; MEM → G2A; GND → G2B; Y0..Y7 → BANKR0..BANKR7

IC117 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW0, BANKR0 → CLK, OC

IC118 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW1, BANKR1 → CLK, OC

IC119 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW2, BANKR2 → CLK, OC

IC120 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW3, BANKR3 → CLK, OC

IC121 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW4, BANKR4 → CLK, OC

IC122 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW5, BANKR5 → CLK, OC

IC123 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW6, BANKR6 → CLK, OC

IC124 74HC574N: DB0..DB7 → 1D..8D; 1Q..8Q → AE'0..AE'7; BANKW7, BANKR7 → CLK, OC

IC125 74HC541N: A1..A8 → AE'0..AE'7; G1, G2 → GND; Y1..Y8 → AEXT0..AEXT7

IC126 74HC541N: AE'0..AE'7 → A1..A8; G1, G2 → GND; Y1..Y8 → AEXT0..AEXT7

IC127 74HC541N: AEXT0..AEXT7 → A1..A8; G1, G2 → GND; Y1..Y8 → BANK0..BANK7

BANK[0..7]

AEXT[0..7]

IC116A 74HC74N: DB8 → D; BANKW7 → CLK; RESET/20 → CLR; VCC → PRE; Q → DB8 BANKW7; Q̄ → 6

IC116B 74HC74N: 12 → D; 11 → CLK; 13 → CLR; VCC → PRE; GND; Q → 9; Q̄ → 8

BANKING

BANKING

TODO:

* DRC

The 64 kW address space is split into 8 banks of 8 kW each.

The banking scheme allows page 0 to be swapped for other pages, although since page 0 has special significance, this should probably not be done normally. This leaves 7 banks and 56 kW available for switching.

LED-5MM-GREEN R32 330R LED5 → GND

BANKING

Decoupling

C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142 0.1uF; C143 1uF; VCC; GND

IC113B 74HC32N: 4, 5 → 6

IC113C 74HC32N: 9, 10 → 8

GND

Title:	cft-processor
Revision:	Rev B
Last Change:	13 Aug 2012 19:11:25
Drawn by:	Alexios
Sheet	21/24
Simulation filename:	memory.v#bank_switch
More Info:	http://www.bedroomlan.org/cft

CFT Mini-Computer

Interrupt Controller

DB[0..15]
AB[0..15]
W/21
SYSDEV/21
RESET/21
R/12
R/24
W/24
SYSDEV/24
RESET/24

IC129 74HC138N
IC138D 74HC08N

Decodes addr: 0000 0000 0011 XXnn

OUT &0030-&003F: write to IER
IN &0030-&003F: read from ISR

Interrupt Status Register

IRF[0..7]
IC131 74HC540N
ISRR
IERW

Interrupt Enable Register

IC135 74HC574N
IC132A 74HC112N
RESET
GND

Front Panel Buffers & Connectors

IC137 74HC541N
IC139 74HC541N
22-23-2081
CON9-1 … CON9-8
CON10-1 … CON10-8

Interrupt registers

IEN[0..7]
IRQ[0..7]
IC128A, IC130A, IC133A, IC134A, IC128B, IC130B, IC133B, IC134B — 74HC112N
IRF[0..7]

LED Displays (Optional)

LED-5MM-GREEN
LED-5MM-RED
LED6 … LED13
LED14 … LED21
RN17 330R
RN18 330R
RN16 4k7

IRQ Generator

IC136A, IC136B, IC136C, IC136D — 74HC08N
IC138B, IC138C, IC138A — 74HC08N
IRQ/11

Note: if the Interrupt Controller is installed, IRQ is always driven. Nothing else may drive IRQ, not even open drain outputs.

Decoupling

C144 … C155: 0.1uF
C156: 1uF
VCC
GND

IC132B 74HC112N

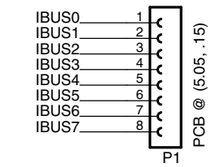
TODO:
* DRC

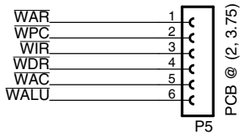
Title:	cft-processor
Revision:	Rev A
Last Change:	13 Aug 2012 19:11:25
Drawn by:	Alexios — 22/24
Simulation filename:	to be coded
More Info:	http://www.bedroomlan.org/cft

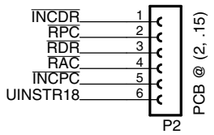
CFT Mini-Computer

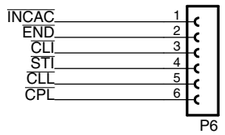
Control Bus Connectors

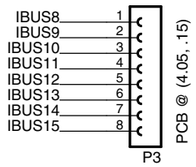
Control Bus Connectors

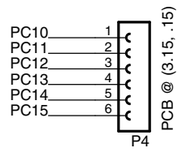


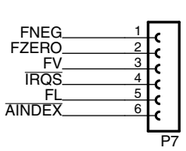












Notes

This is only useful for building the processor on separate cards.

U

Title: cft-processor	
Revision: Rev H	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	23/24
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	

CFT Mini-Computer

Debugging Card

IO/13
MEM/21
R/22
RESET/22
W/22
IODEV3XX/13
HALT/4
WS/12
AB[0..15]
DB[0..15]

Bus Interface

IC252 74HC138N
IODEV3XX
AB4 AB5 AB6 AB7 W IODEV3XX
&038x &039x &03Ax &00Bx &00Cx &00Dx &00Ex &03FX DEBW

IC253A 74HC74N
RESET DEBCONT DEBW
Q=1: no WS
Q̄=0: no WS

IC255A 74HC05N

Test Point Headers

JP32: SKIPEXT ENDEXT WS
JP34: IODEV1XX IODEV2XX IODEV3XX T34 SYSDEV
JP33: IRQ4 IRQ3 IRQ5 IRQ6 IRQ7 IRQ0 HALT IRQ1 IRQ2
JP35: CLK4 CLK1 CLK2 CLK3 IRQS

ATMEGA168

IC256
VCC C383 0.1uF GND, VCC C386 0.1uF GND, VCC AREF AVCC
DEBRST S48 GND
C384 22pF, C385 22pF, 14.7456 XTAL5
PC6(/RESET) PC0(ADC0) PC1(ADC1) PC2(ADC2) PC3(ADC3) PC4(ADC4/SDA) PC5(ADC5/SCL)
PB6(XTAL1/TOSC1) PB7(XTAL2/TOSC2)
PD0(RXD) PD1(TXD) PD2(INT0) PD3(INT1) PD4(XCK/T0) PD5(T1) PD6(AIN0) PD7(AIN1)
PB0(ICP) PB1(OC1A) PB2(SS/OC1B) PB3(MOSI/OC2) PB4(MISO) PB5(SCK)
R R/22, W W/22, MEM MEM/21, IO IO/13, DEBSCL, DEBSDA
DEBIN DEBOUT DEBW DEBCONT CFTRST DEBHALT
DEBLED0 DEBLED1 DEBLED2 MOSI MISO SCK
R232 4k7, R233 4k7

CFTRST → IC255C 74HC05N → RESET
DEBHALT → IC255B 74HC05N → HALT

To front panel controller
JP31
FPCLKEN/2
FPUSTEP/2

Expansion Bus (computer bus)

EXP1A: GND GND VCC +3.3V AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 IRQ3 IRQ4 IRQ5 IRQ6 *TPA IRQ7 HALT AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15 SYSDEV CLK1 IRQS +12V VCC
EXP1B: GND GND VCC +3.3V SKIPEXT ENDEXT WS AEXT0 AEXT1 AEXT2 AEXT3 AEXT4 AEXT5 AEXT6 AEXT7 IODEV1XX IODEV2XX IODEV3XX T34 CLK4 CLK2 CLK3 +12V VCC
EXP1C: GND GND VCC +3.3V DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 MEM IO R W *TPC IRQ0 IRQ1 IRQ2 DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15 CLK5 RESET +12V VCC

PCB @ (0, 1.95)

ISP Programmer

MOSI VCC
JP30: MISO SCK RESET +5 MOSI GND
ISP

USB Serial

JP29: RXD TXD -RTS DEBOUT DEBIN FTDIVCC -CTS
R230 1k, R231 1k
Made for an FTDI USB to 3.3V TTL cable
For a 5V FTDI USB cable, do not fit R2 and R3.

Status display

DEBLED0 R226 330R LED177 T1
DEBLED1 R227 330R LED178 T2
DEBLED2 R228 330R LED179 T3
MOSI DEBLED3 R229 330R LED180 T4/Prog

External reset (or alternate pushbutton)

DEBRST JP28

IC250

SCL SDA A0 A1 A2 INT CLK
GP0.0 GP0.1 GP0.2 GP0.3 GP0.4 GP0.5 GP0.6 GP0.7 GP1.0 GP1.1 GP1.2 GP1.3 GP1.4 GP1.5 GP1.6 GP1.7
DEBSCL DEBSDA DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7
C374 0.1uF, R223 3k9, C378 33pF
MCP23016

IC254

SCL SDA A0 A1 A2 INT CLK
GP0.0 GP0.1 GP0.2 GP0.3 GP0.4 GP0.5 GP0.6 GP0.7 GP1.0 GP1.1 GP1.2 GP1.3 GP1.4 GP1.5 GP1.6 GP1.7
DEBSCL DEBSDA DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15 AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15
C381 0.1uF, R225 3k9, C382 33pF
MCP23016

IC251

SCL SDA A0 A1 A2 INT CLK
GP0.0 GP0.1 GP0.2 GP0.3 GP0.4 GP0.5 GP0.6 GP0.7 GP1.0 GP1.1 GP1.2 GP1.3 GP1.4 GP1.5 GP1.6 GP1.7
DEBSCL DEBSDA JP26
C375 0.1uF, R224 3k9, C379 33pF
MCP23016
JP27

Decoupling

C373 0.1uF, C376 0.1uF, C377 0.1uF, C380 1uF

IC253B 74HC74N
IC255D 74HC05N
IC255E 74HC05N
IC255F 74HC05N
C387 1uF

[PCB Logo] [PCB Logo] [PCB Logo]
H5 HOLE @ (.175, 3.675)
H6 HOLE @ (5.8, 3.675)
H7 HOLE @ (5.8, .225)
H8 HOLE @ (.175, .225)

U

Title: cft-processor	
Revision: Rev A	
Last Change: 13 Aug 2012 19:11:25	
Drawn by: Alexios	24/24
Simulation filename: N/A	
More Info: http://www.bedroomlan.org/cft	