

# Simultaneous Multithreading: Multiplying Alpha Performance

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## Outline

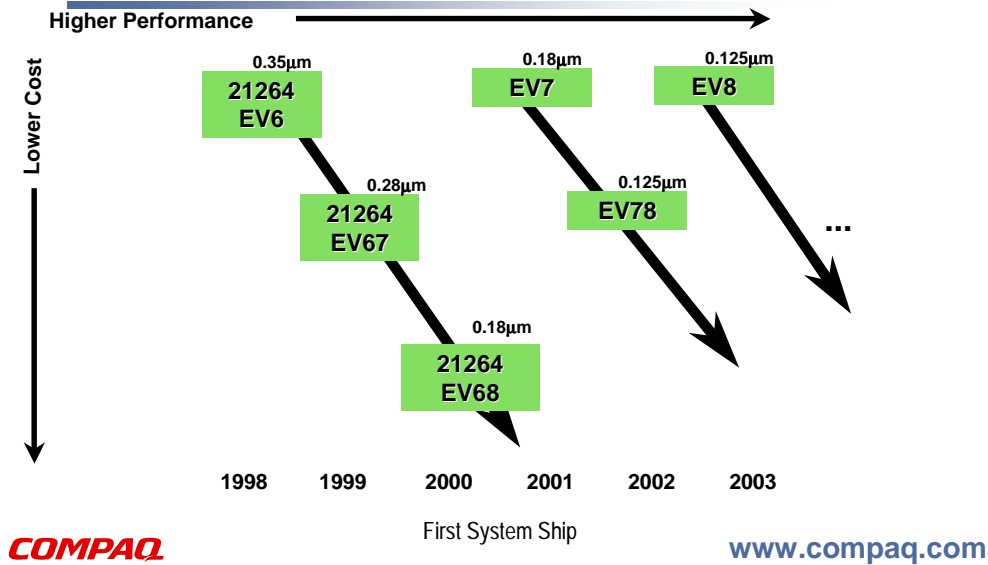
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- ◆ Alpha Processor Roadmap
- ◆ Motivation for Introducing SMT
- ◆ Implementation of an SMT CPU
- ◆ Performance Estimates
- ◆ Architectural Abstraction

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## Alpha Microprocessor Overview



## EV8 Technology Overview

- ◆ Leading edge process technology – 1.2-2.0GHz
  - 0.125μm CMOS
  - SOI-compatible
  - Cu interconnect
  - low-k dielectrics
- ◆ Chip characteristics
  - ~1.2V Vdd
  - ~250 Million transistors
  - ~1100 signal pins in flip chip packaging

## EV8 Architecture Overview

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- ◆ Enhanced out-of-order execution
- ◆ 8-wide superscalar
- ◆ Large on-chip L2 cache
- ◆ Direct RAMBUS interface
- ◆ On-chip router for system interconnect
- ◆ Glueless, directory-based, ccNUMA for up to 512-way SMP
- ◆ 4-way simultaneous multithreading (SMT)

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## Goals

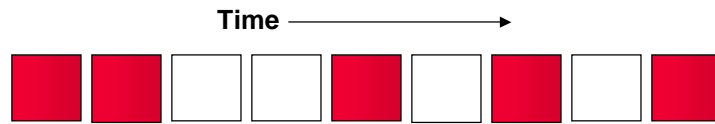
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- ◆ Leadership single stream performance
- ◆ Extra multistream performance with multithreading
  - Without major architectural changes
  - Without significant additional cost

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## Instruction Issue

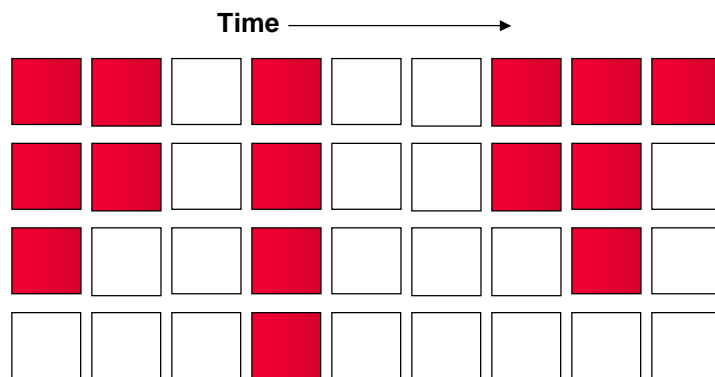


Reduced function unit utilization due to dependencies

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## Superscalar Issue

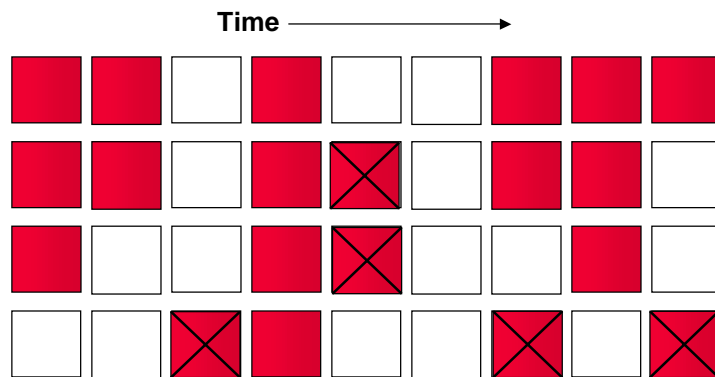


Superscalar leads to more performance, but lower utilization

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## Predicated Issue

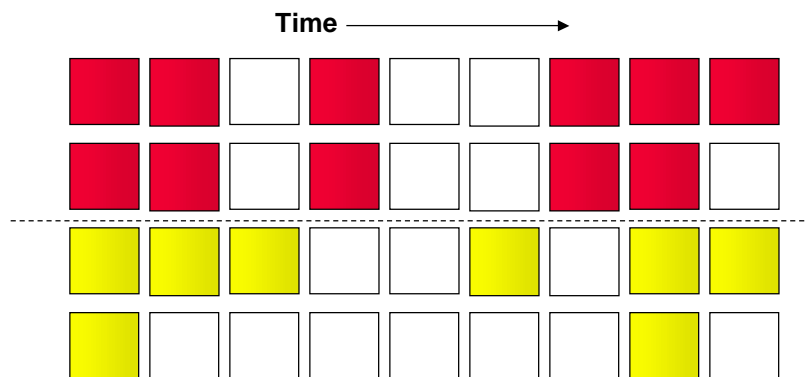


Adds to function unit utilization, but results are thrown away

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## Chip Multiprocessor

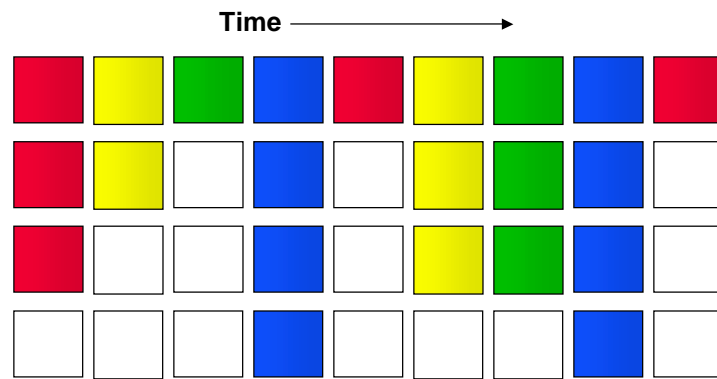


Limited utilization when only running one thread

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## Fine Grained Multithreading

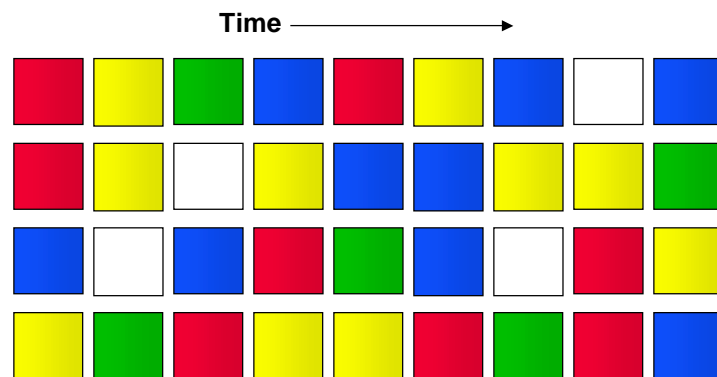


Intra-thread dependencies still limit performance

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## Simultaneous Multithreading

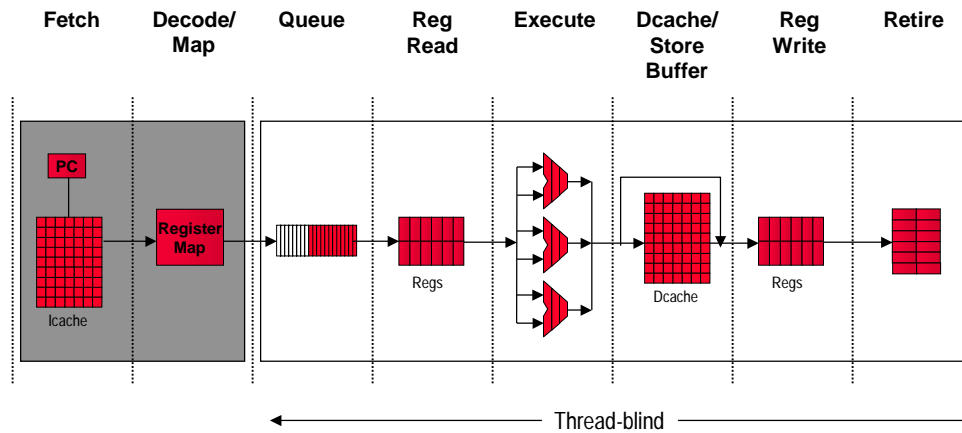


Maximum utilization of function units by independent operations

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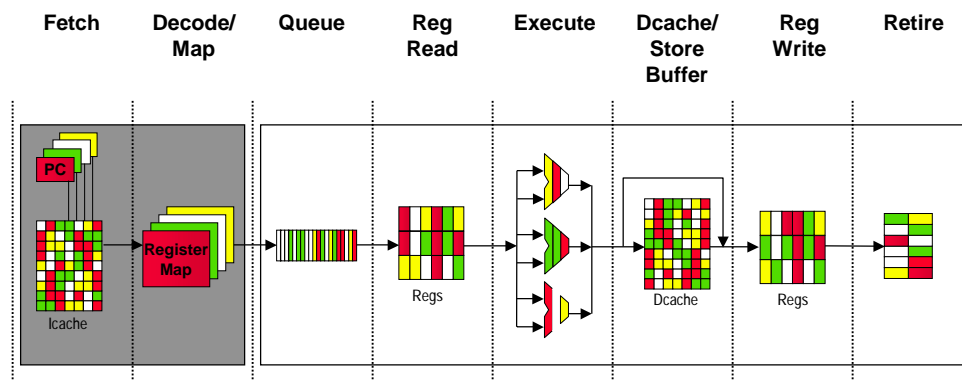
## Basic Out-of-order Pipeline



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## SMT Pipeline



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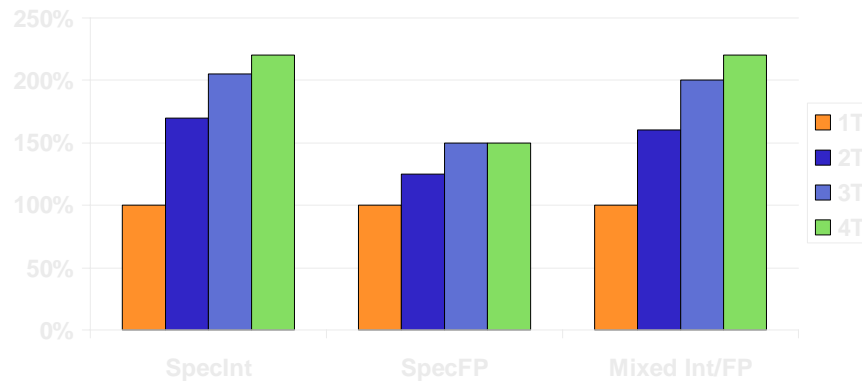
## Changes for SMT

- ◆ Basic pipeline – unchanged
- ◆ Replicated resources
  - Program counters
  - Register maps
- ◆ Shared resources
  - Register file (size increased)
  - Instruction queue
  - First and second level caches
  - Translation buffers
  - Branch predictor

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## Multiprogrammed workload

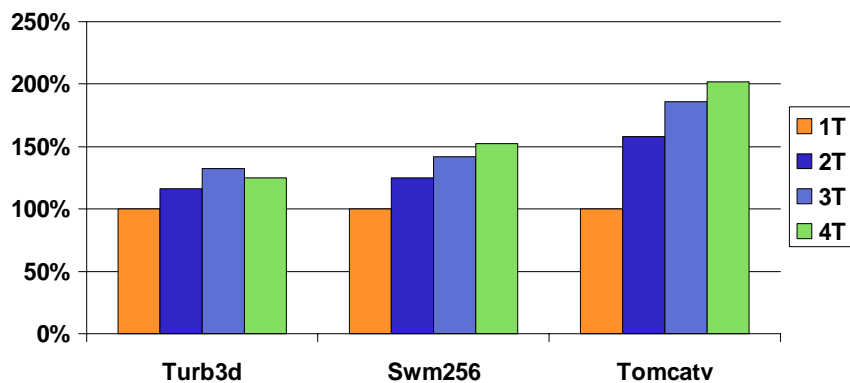


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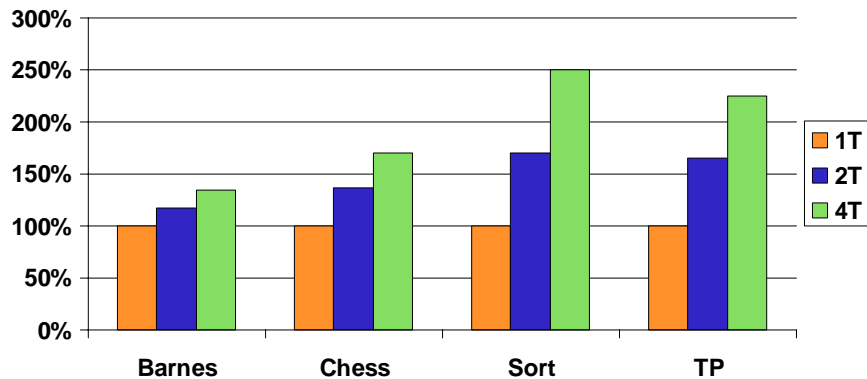
## Decomposed SPEC95 Applications



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## Multithreaded Applications

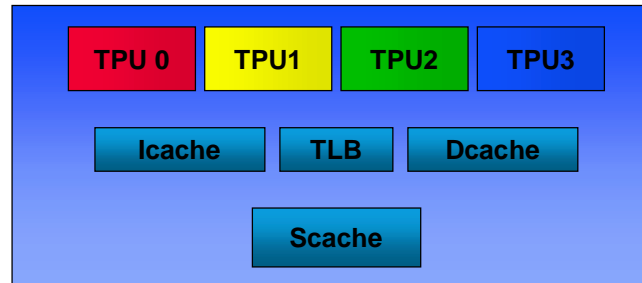


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## Architectural Abstraction

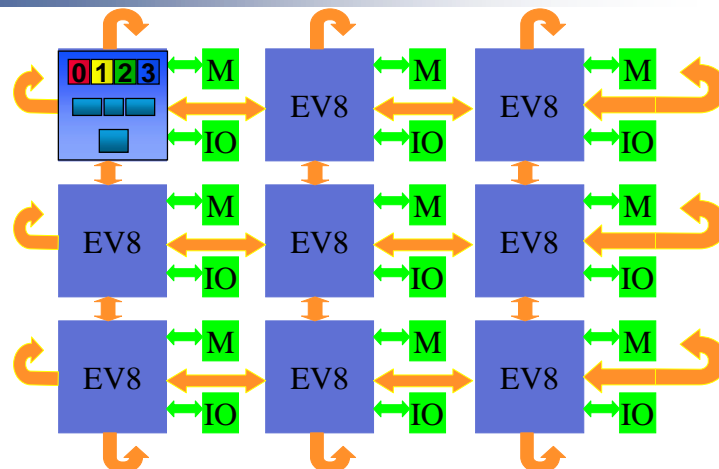
- ◆ 1 CPU with 4 Thread Processing Units (TPUs)
- ◆ Shared hardware resources



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## System Block Diagram



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## Quiescing Idle Threads

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- ◆ Problem:  
Spin looping thread consumes resources
- ◆ Solution:  
Provide quiescing operation that allows a TPU to sleep until a memory location changes

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## Summary

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- ◆ Alpha will maintain single stream performance leadership
- ◆ SMT will significantly enhance multistream performance
  - Across a wide range of applications,
  - Without significant hardware cost, and
  - Without major architectural changes

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## References

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- ♦ "*Simultaneous Multithreading: Maximizing On-Chip Parallelism*" by Tullsen, Eggers and Levy in ISCA95.
- ♦ "*Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreaded Processor*" by Tullsen, Eggers, Emer, Levy, Lo and Stamm in ISCA96.
- ♦ "*Converting Thread-Level Parallelism to Instruction-Level Parallelism via Simultaneous Multithreading*" by Lo, Eggers, Emer, Levy, Stamm and Tullsen in ACM Transactions on Computer Systems, August 1997.
- ♦ "Simultaneous Multithreading: A Platform for Next-Generation Processors" by Eggers, Emer, Levy, Lo, Stamm and Tullsen in IEEE Micro, October, 1997.