A Millimeter-Wave Software-Defined Radio for Wireless Experimentation

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Overview

- Motivation
- Proposed millimeter-wave SDR architecture
- Proposed transmission and reception methods
- Beam-sweeping experiment and results
- Final remarks

Motivation

- Millimeter-wave (mmWave) communications is one of the key enablers for high-throughput systems by allowing directive links over a large bandwidth
- For mmWave systems, experimentation in real-world environments is a major challenge because of lack of low-cost and portable mmWave SDRs
- Motivation: Developing a portable, low-cost, and easy-to-construct mmWave SDR and building UAVs equipped with mmWave SDRs for NSF AERPAW platform

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Proposed SDR Architecture

Architecture: Goal and Strategy

- Goal: Flexibility
  - To transmit and receive an arbitrary waveform by considering the unique aspects of mmWave communications such as beamforming and large bandwidths
- Strategy: Implement a minimal feature set independent from the application
- The proposed SDR uses
  - Sivers EVK06002 evaluation kit
  - Xilinx RFSoC2x2 FPGA board
- It provides an API for a companion computer (CC)-based baseband signal processing

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Architecture: Sivers EVK06002 Evaluation Kit

- Converts the continuous-time baseband I and Q signals to the passband or vice versa
  - Frequency range: 57-71 GHz, Bandwidth: 2 GHz
- Integrates 2 phased-antenna arrays (PAAs) for TX and RX
- Each PAA provides 16 channels, where each channel is wired to 4 patch antennas
- Stores 64 custom antenna weighting vectors (AWVs)
- Controllable over a USB interface
- Costs less than $2.5K

Figure 1: Sivers EVK06002

Architecture: Xilinx RFSoC2x2 FPGA board

- Features Zynq UltraScale+ XCZU28DR
- Provides SMA connections to two built-in 12-bit ADCs
  - The maximum sample rate: 4.096 Gsps
- Provides SMA connections to two built-in 14-bit DACs
  - The maximum sample rate: 6.554 Gsps
- Integrates Arm Cortex-A53 64-bit quad-core processor
- Supports PYNQ: An open-source Linux-based system
  - Facilitates the interaction between the FPGA design, i.e., programmable logic (PL), with a custom software, i.e., programmable system (PS)
- Costs $2.15K

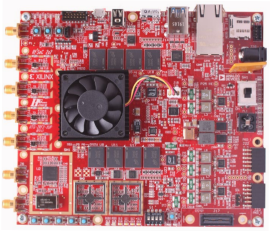

Figure 2: Xilinx RFSoC

Architecture: Implementation

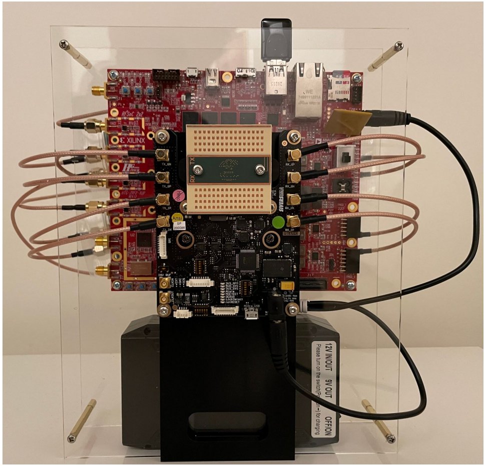

Figure 3: The proposed mmWave SDR along with a 12 V battery. The total cost is less than $5K.

Architecture: Functionality

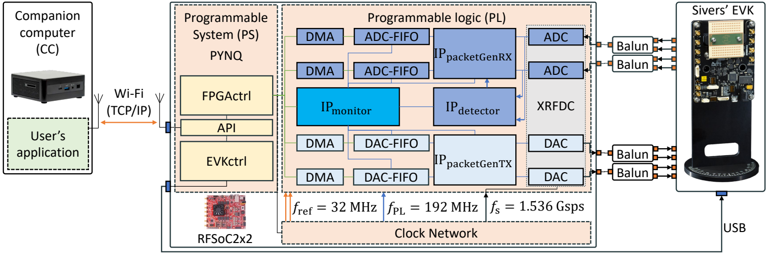

Figure 4: The architecture of the proposed SDR.

RFSoC2x2 is responsible for the following tasks:

- Task 1/4: Generating I and Q continuous signals based on the IQ samples at the CC
- Task 2/4: Acquiring IQ data by sampling I and Q signals and passing them to the CC
- Task 3/4: Configuring and controlling EVK06002 over a USB port
- Task 4/4: Providing a TCP/IP-based API for CC

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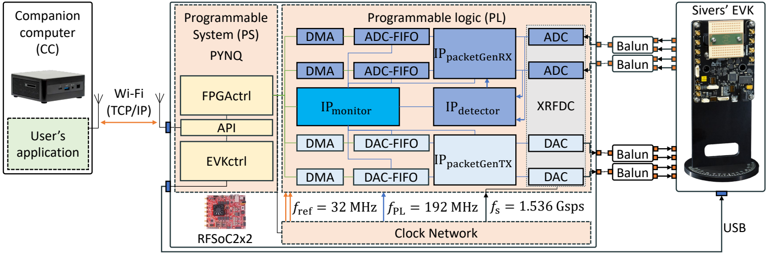

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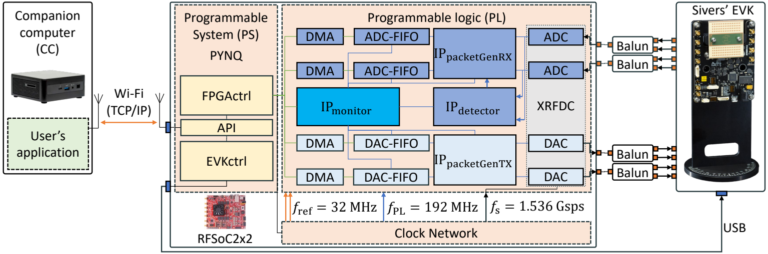

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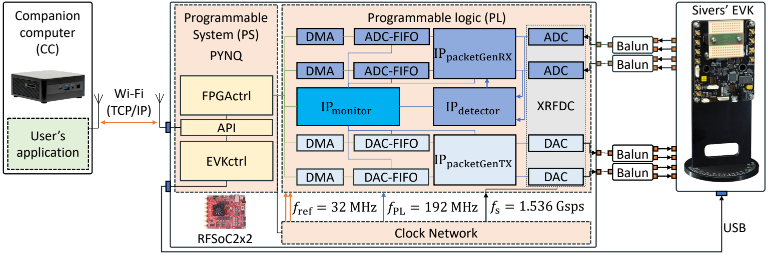

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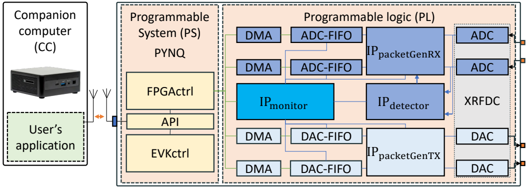
Proposed transmission and reception methods

Transmission

A transmission is initiated by the CC, e.g., transmit(IQ data)

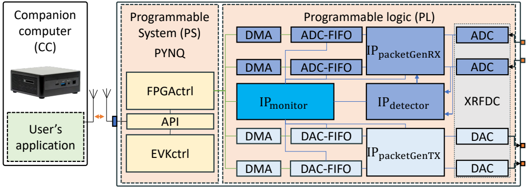
- **Step 1**: `FPGActrl` writes the IQ samples to the DAC-FIFOs
- **Step 2**: `FPGActrl` sets the transfer size based on # of IQ samples
- **Step 3**: `FPGActrl` triggers the transmission
- **Step 4**: $\mathrm{IP}_{\mathrm{packetGenTX}}$ enables XRFDC to read IQ samples from DAC-FIFOs.



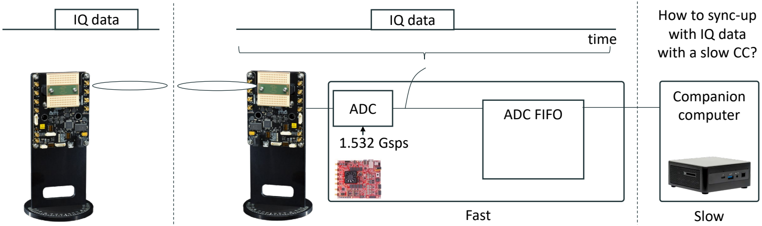
Reception: Software-triggered reception (STR)

A reception is initiated by CC after a setup phase

- Setup phase (RX mode: STR)
  - **Step 1**: CC sets S_{rx} IQ samples to be acquired per packet
- Trigger&reception phase
  - **Step 1**: CC invokes receive(N_{packet})
  - **Step 2**: `FPGActrl` triggers the acquisition by N_{packet} times
  - **Step 3**: $\mathrm{IP}_{\mathrm{packetGenRX}}$ passes the IQ samples from XRFDC to ADC-FIFOs
  - **Step 4**: `FPGActrl` reads $S_{\mathrm{rx}} N_{\mathrm{packet}}$ IQ samples from the ADC-FIFOs



A new reception mode: Waveform-triggered reception (WTR)



- For a mmWave SDR, there is a large difference between the processing speed of the CC and the sample rate of analog-to-digital converters
- It is very challenging to find transmitted IQ data based on a correlator at the CC

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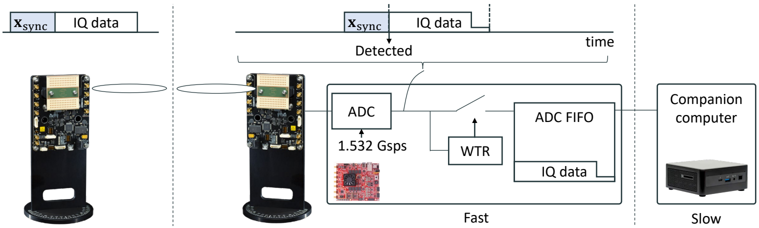
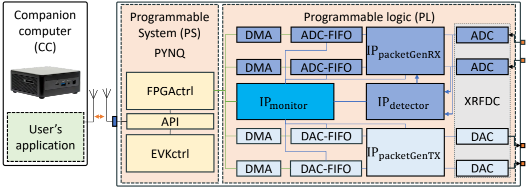


- We address this issue with WTR, where an IP search for a trigger waveform $\mathbf{x}_{\mathrm{SYNC}}$ to acquire a pre-determined number of IQ samples upon the detection
  - Agnostic to the user's IQ data
  - Reduces the load on the interface between CC and SDR
  - Off-loads coarse time synchronization needed for baseband processing to FPGA
  - $\mathbf{x}_{\mathrm{SYNC}}$ is a single-carrier waveform based on a Golay sequence of length 32

Reception: Waveform-triggered reception (WTR)

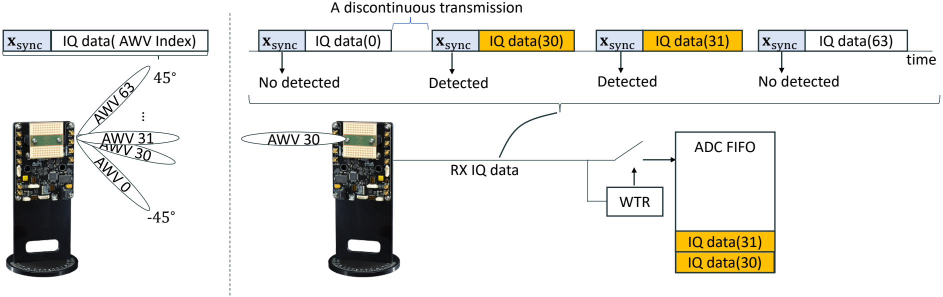
As compared to STR, IQ samples are acquired upon the detection of $\mathbf{x}_{\mathrm{SYNC}}$ with WTR

- Trigger phase
  - **Step 1**: $\mathrm{IP}_{\mathrm{detector}}$ searches for trigger waveform. If it detects, triggers the acquisition and increases N_{packet} by 1
  - **Step 2**: $\mathrm{IP}_{\mathrm{packetGenRX}}$ passes the IQ samples from XRFDC to ADC-FIFOs
- Reception phase
  - **Step 1**: CC reads N_{packet} and invokes receive(N_{packet})
  - **Step 2**: `FPGActrl` reads $S_{\mathrm{rx}} N_{\mathrm{packet}}$ IQ samples from the ADC-FIFOs



Discontinuous transmissions with WTR

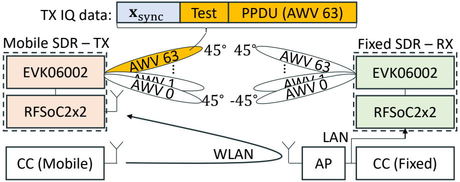
- WTR enables a large number of transfers to be stored in the ADC-FIFOs, where the receptions depend on the transmission instants
- Useful for CC-based beam sweeping by allowing only necessary information to be passed to the ADC FIFOs:



Beam-sweeping Experiment

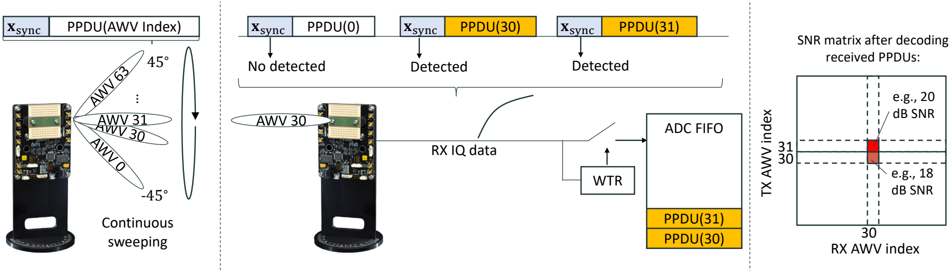
Experiment Setup

- One fixed SDR and a mobile SDR, where the SDRs face each other
- We reduce the link distance between the SDRs from 9.75 m to 2.44 m with a spacing of 12”
- 64 AWVs sweeping the azimuth between -45° and 45° uniformly for $f_c = 60.48$ GHz
  - Leads to 4096 TX-RX AWV index pairs
- Our goal is to evaluate the SNR for each pair at different locations for $f_c \in \{60.48, 65.34\}$ GHz



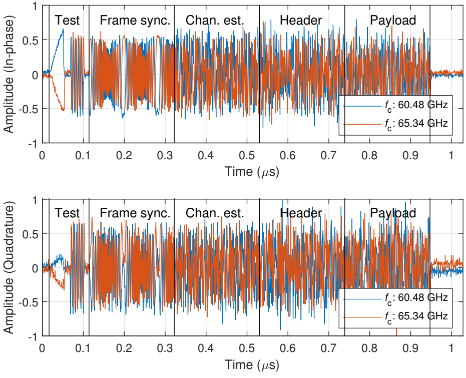
Procedure and Dataset Generation

- TX transmits an OFDM-based PPDU along with a test waveform, where the data bits indicate the AWV index and sweep all 64 AWVs continuously
  - The PPDU consists of 4 OFDM symbols and its length is 1280 complex samples
- RX sets its AWV index and waits for 2 second in WTR mode for TX to complete sweeping
  - The detected ones are recorded for dataset generation
  - The decodable ones are used for generating SNR matrix

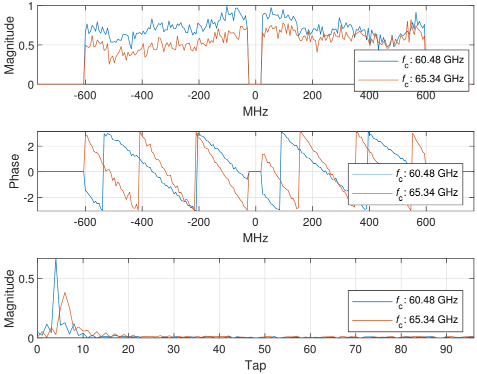


Measurements: An Example of Received PPDU

- The received IQ data samples and the measured channel frequency response (CFR) and channel impulse response (CIR) for two measurements at 9.75 m



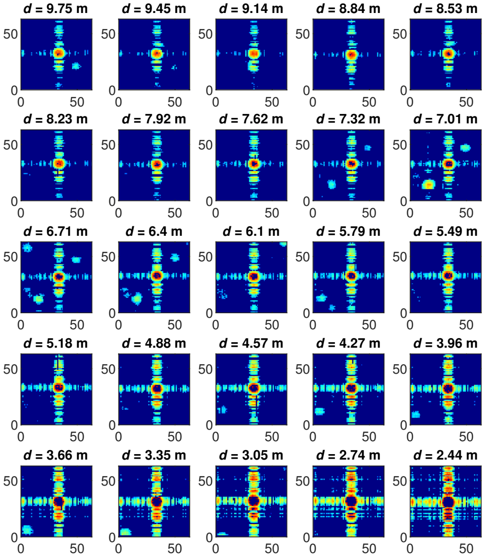
(a) The IQ samples



(b) The measured CFR and CIR.

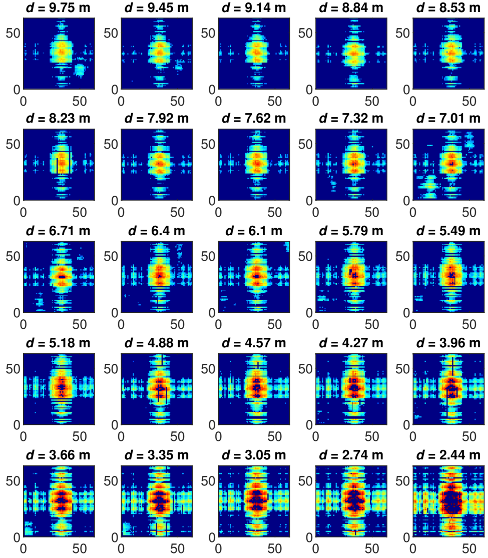
Measurements: SNR Matrix at 60.48 GHz

- SNR can reach up to 30 dB when the beams are well-aligned, e.g., when the RX AWV and TX AWV indices are around 32, i.e., 0 degrees
- If the received signal is powerful, the receiver may not be able to decode the PPDU due to saturation
- The link can still be maintained over a reflection. For $d = 7.01$ m, the link can be maintained if both TX AWV and RX AWV indices are set to 13, likely over a reflection due to the metal cabinets



Measurements: SNR Matrix at 65.34 GHz

- We observe a large difference in the SNR matrices when f_{c} is switched to 65.34 GHz
- Since we still use the AWVs for $f_{\mathrm{c}} = 60.48$ GHz, the beams are not focused for $f_{\mathrm{c}} = 65.34$ GHz, i.e., causes a beam squint effect
- While the mismatch allows the link via the antenna side lobes, it becomes more blind to the reflections as the power is dispersed to the different angles



Concluding Remarks

- We propose a mmWave SDR solution for experimentation in the 60 GHz band and introduce WTR and a buffering approach for discontinuous transmission to achieve a flexible CC-based baseband signal processing
    - Advantages: Low-cost, portable, and easy to construct
    - Source code: https://github.com/alphansahin/mmWaveSDR
    - Dataset: https://ieee-dataport.org/documents/iq-data-given-tx-rx-beam-index-pair-link-level-analysis-60-ghz-band
- Future work:
    - Integrating and testing it with UAVs in the NSF AERPAW platform at 28 GHz
    - Developing a digital twin to emulate the UAVs in conjunction with the proposed SDRs

Questions?