Amin Mamandipoor

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EDUCATION

University of Kansas, Lawrence **2022 - 2027 (*expected*)**

Ph.D. in Computer Science *GPA: 3.97/4.00*

- Current Advisor: Prof. Heechul Yun (focusing on **Computer Architecture** and **Real-Time Systems**)
- Former Advisor: Prof. Mohammad Alian (now at Cornell University)
- Focus Areas: **Computer Architecture**, **Datacenter Networking**, **Real-Time Systems**, **Memory Subsystem**

University of Tabriz, Iran **2018 - 2021**

M.Sc. in Computer Engineering *GPA: 4.00/4.00*

- Thesis: "**FPGA-based Acceleration of Deep Neural Networks**" - Designed and implemented custom hardware accelerators for CNN inference
- Coursework: Advanced Computer Architecture, Digital System Design, VLSI Design, Test and Testability

University of Tabriz, Iran **2013 - 2018**

B.Sc. in Computer Engineering *GPA: 3.95/4.00*

- Coursework: Computer Architecture, Digital Logic Design, Embedded Systems, Operating Systems, Computer Networks

TECHNICAL SKILLS

Research Interests: Computer Architecture, Hardware Acceleration, CPU Microarchitecture, Real-Time Systems, Memory Systems, Datacenter Networking
Hardware Description Languages: Verilog, SystemC, VHDL
Programming Languages: C/C++, Python, Java, MIPS assembly, ARM assembly
Computer Architecture Tools: gem5, ModelSim, Cadence Virtuoso, Vivado HLS, Vitis AI
Performance Analysis: Intel PIN, Intel VTune, Intel CAT, perf, valgrind
Development Tools: MATLAB, Git, Docker, QEMU, Jupyter

EXPERIENCES

University of Kansas **January 2022 – December 2023**

Graduate Research Assistant *Lawrence, KS*

- Designed and evaluated heterogeneous multi-accelerator architectures for datacenter applications that achieved up to 8.2× improvement in latency, 13.6× in throughput, and 5.2× in energy efficiency (**Hardware Acceleration**, **Computer Architecture**)
- Conducted detailed performance profiling of the **gem5** simulator, identifying that its performance is extremely sensitive to L1 cache size, and designed a **RISC-V** core with optimized cache configuration that improved simulation speed by 31% to 61% (**Performance Analysis**, **Computer Architecture**)
- Developed an in-memory acceleration system for upper-layer network protocols using Samsung's AxDIMM platform, working with **DDR4 command sequences (ACT, rdCAS, wrCAS)** and buffer device timing parameters, achieving 1.21× to 10.28× higher requests per second and 36.3% to 88.9% lower memory bandwidth utilization (**Memory Systems**, **DDR Protocol**, **Datacenter Networking**)
- Designed an accelerated software-defined far memory architecture that exploits DRAM refresh cycles to eliminate memory bandwidth utilization when performing compression operations, resulting in 5% to 27% performance improvement for co-running applications (**Memory Systems**, **Hardware Acceleration**)
- Designed and evaluated a novel Simultaneous MultitThreading architecture to reduce datacenter networking tax, creating a chip multiprocessor with specialized network threads that achieved 49% die area reduction and 32% lower power consumption while maintaining network throughput within 10% of baseline Chip MultiProcessor designs (**CPU Microarchitecture**, **Datacenter Networking**)

University of Kansas **Spring '24, Fall '24, '25**

Graduate Teaching Assistant *Lawrence, KS*

- Teaching **Introduction to Computer Architecture** (EECS 645), covering topics such as pipelining, memory hierarchy, and multicore architectures, helping students understand fundamental hardware concepts
- Instructing **Embedded Systems** (EECS 388), guiding students in developing applications on microcontrollers, programming in C/C++, implementing real-time systems, and interfacing with peripheral devices
- Developed and delivered lecture materials on architectural simulators (**gem5** and **MARS**), enabling students to analyze processor performance and explore design trade-offs

University of Tabriz **Sep 2017 – May 2020**

Graduate Teaching Assistant *Tabriz, Iran*

- Led lab sessions for **Introduction to Computer Architecture**, focusing on processor design concepts, pipelining, and memory hierarchy
- Instructed students in **Digital Circuit Design** courses, covering Verilog HDL, and fundamental digital design principles including combinational and sequential logic
- Developed and evaluated assignments on processor design, cache architecture, and digital circuit implementation, helping students bridge theoretical concepts with practical applications

PUBLICATIONS

ISCA 2025 - Conference — **Amin Mamandipoor**, Huy Dinh Tran, Mohammad Alian, "**SDT: Simultaneous Data Delivery Thread**" — Under Review

IEEE Computer Architecture Letters - Journal — **Amin Mamandipoor**, Huy Dinh Tran, Mohammad Alian, "**Cutting Datacenter Tax Through Simultaneous Network Threads**" — Paper

HPCA 2024 - Conference — Neel Patel, **Amin Mamandipoor**, Mohammad Nouri, Mohammad Alian, "**SmartDIMM: In-Memory Acceleration of Upper Layer I/O Protocols**" — Paper

MICRO 2023 - Conference — Neel Patel, **Amin Mamandipoor**, Derrick Quinn, Mohammad Alian, "**XFM: Accelerated Software-Defined Far Memory**" — Paper

HPCA 2024 - Conference — Shu-Ting Wang, Hanyang Xu, **Amin Mamandipoor**, Rohan Mahapatra, Byung Hoon Ahn, Soroush Ghodrati, Krishnan Kailas, Mohammad Alian, Hadi Esmaeilzadeh, "**Data Motion Acceleration for Heterogeneous Cross Domain Accelerator Chaining**" — Paper

ISPASS 2023 - Conference — Johnson Umeike, Neel Patel, Alex Manley, **Amin Mamandipoor**, Heechul Yun, Mohammad Alian, "**Profiling gem5 Simulator**" — Paper

AWARDS

Conference Travel Grants: gem5 Bootcamp (2024), ISPASS (2023), MICRO (2022)
Research Excellence: First Place, I2S Student Research Symposium (2024)
Service Recognition: Nominee, Graduate Student Distinguished Service Award (2024-2025), Primary Advisor for KU's IndySCC Team (2024)
Industry Recognition: Second Runner-up, Samsung Open Innovation Contest for AxDIMM Technology (2022)
Academic Honors: Outstanding Student Award, University of Tabriz (2014, 2021)

PROJECTS

Simultaneous Multi-Threading (SMT) for gem5 Full-System Simulation **2024**
Developed and integrated SMT support for gem5's full-system mode, implementing resource partitioning policies for shared microarchitectural resources to enable advanced processor architecture research. Resulted in an upcoming arXiv publication.

Simultaneous Data Delivery Thread (SDT) **2023-2024**
Designed an adaptive partitioning policy using fetch throttling instead of pipeline flushes for efficient resource re-partitioning, reducing latency while maintaining throughput. Implemented specialized network threads with reduced overhead, resulting in submissions to IEEE Computer Architecture Letters and ISCA.

Real-time Sound Classification on Embedded Systems **2024**
Implemented a CNN-based sound classifier on ESP32-S3 microcontroller achieving 94% accuracy with only 599ms latency and 17.8KB RAM usage, optimized through int8 quantization for edge deployment

In-Memory Compression During DRAM Refresh Operations **2023**
Designed and implemented a novel far memory architecture that leverages DRAM refresh operations for compression, resulting in a publication at MICRO 2023. Optimized memory access patterns to reduce bandwidth contention, improving performance of co-running applications by up to 27% compared to state-of-the-art solutions.

Near-Memory Acceleration of Network Protocols **2022**
Implemented a proof-of-concept for accelerating network protocols using processing-in-memory techniques on Samsung's AxDIMM platform, achieving 2.3× speedup over conventional CPU implementation, resulting in a publication at HPCA 2024.

Quash: UNIX Shell Implementation **2022**
Developed a command-line interface with functionality comparable to bash, featuring robust user input parsing, dynamic pipeline detection, custom tokenization mechanisms, and concurrent command execution. Implemented process management, job control, and signal handling in C with POSIX compliance.

VLSI Design **2021**
Designed and implemented an 8-bit counter using Cadence Virtuoso on TSMC's 180nm process, including layout, verification, and timing analysis