

# SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

SDLS090 – OCTOBER 1976 – REVISED MARCH 1988

- Contains Eight Flip-Flops With Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:  
Buffer/Storage Registers  
Shift Registers  
Pattern Generators

## description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

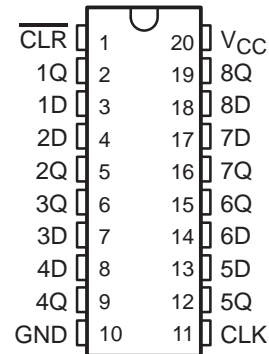
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

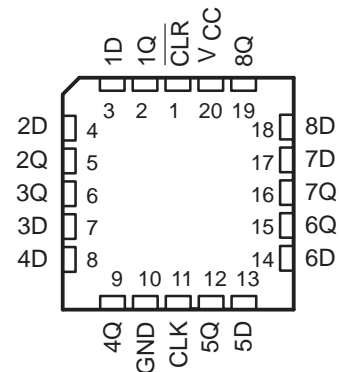
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
CLEAR	CLOCK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

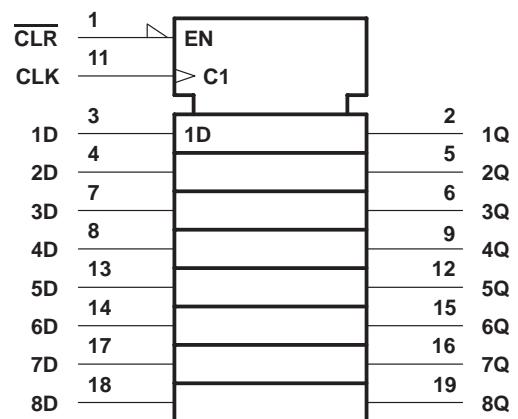
SN54273, SN74LS273 . . . J OR W PACKAGE  
SN74273 . . . N PACKAGE  
SN74LS273 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54LS273 . . . FK PACKAGE  
(TOP VIEW)



## logic symbol†



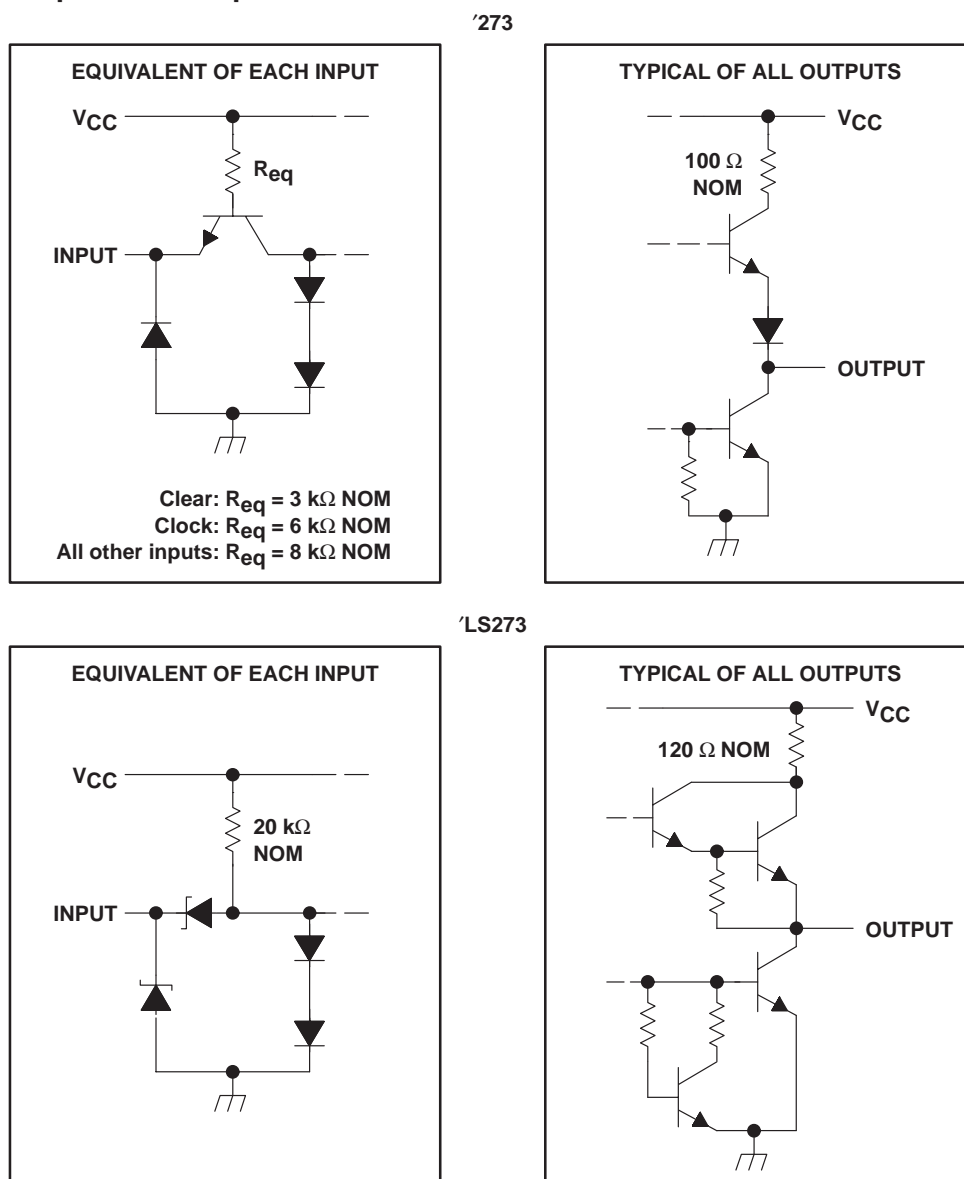
† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, J, N, and W packages.

# SN54273, SN54LS273, SN74273, SN74LS273

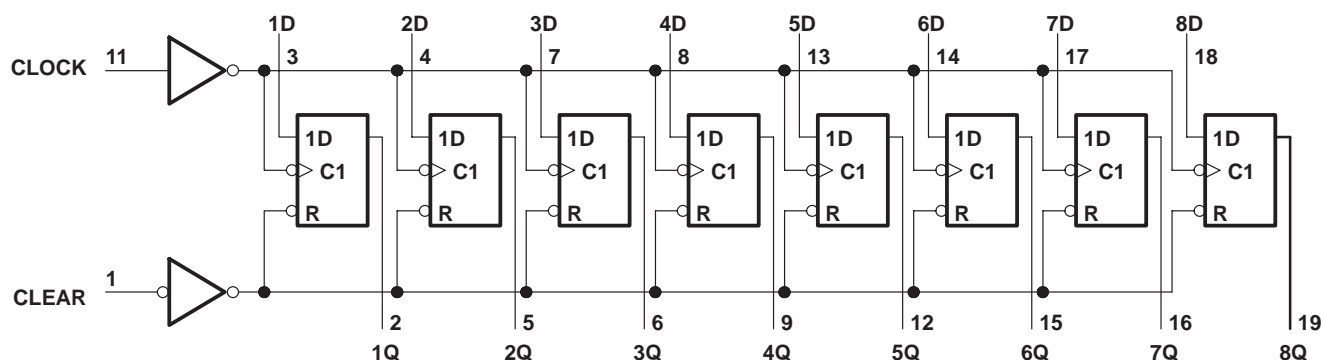
## OCTAL D-TYPE FLIP-FLOP WITH CLEAR

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### schematics of inputs and outputs



### logic diagram (positive logic)



Pin numbers shown are for the DW, J, N, and W packages.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range, $T_A$ : SN54273	–55°C to 125°C
SN74273	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54273			SN74273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$				–800			–800	$\mu$ A
Low-level output current, $I_{OL}$				16			16	mA
Clock frequency, $f_{clock}$		0		30	0		30	MHz
Width of clock or clear pulse, $t_w$		16.5			16.5			ns
Setup time, $t_{su}$	Data input	20 $\uparrow$			20 $\uparrow$			ns
	Clear inactive state	25 $\uparrow$			25 $\uparrow$			
Data hold time, $t_h$		5 $\uparrow$			5 $\uparrow$			ns
Operating free-air temperature, $T_A$		–55		125	0		70	°C

$\uparrow$  The arrow indicates that the rising edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS $\dagger$		MIN	TYP $\ddagger$	MAX	UNIT
$V_{IH}$	High-level input voltage			2			V
$V_{IL}$	Low-level input voltage					0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$				–1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -800 \mu\text{A}$		2.4	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = 16 \text{ mA}$				0.4	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$				1	mA
$I_{IH}$	High-level input current	Clear	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			80	$\mu$ A
		Clock or D				40	
$I_{IL}$	Low-level input current	Clear	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			–3.2	mA
		Clock or D				–1.6	
$I_{OS}$	Short-circuit output current $\S$	$V_{CC} = \text{MAX}$		–18		–57	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , See Note 2			62	94	mA

$\dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

$\ddagger$  All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

$\S$  Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to clock.



# SN54273, SN54LS273, SN74273, SN74LS273

## OCTAL D-TYPE FLIP-FLOP WITH CLEAR

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### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$ Maximum clock frequency	$C_L = 15\text{ pF}$ , $R_L = 400\ \Omega$ , See Note 3	30	40		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			18	27	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock			17	27	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range, $T_A$ : SN54LS273	$-55^\circ\text{C}$ to $125^\circ\text{C}$
SN74LS273	$0^\circ\text{C}$ to $70^\circ\text{C}$
Storage temperature range	$-65^\circ\text{C}$ to $150^\circ\text{C}$

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

		SN54LS273			SN74LS273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$				-400			-400	$\mu\text{A}$
Low-level output current, $I_{OL}$				4			8	mA
Clock frequency, $f_{\text{clock}}$		0		30	0		30	MHz
Width of clock or clear pulse, $t_w$		20			20			ns
Setup time, $t_{su}$	Data input	20 $\uparrow$			20 $\uparrow$			ns
	Clear inactive state	25 $\uparrow$			25 $\uparrow$			
Data hold time, $t_h$		5 $\uparrow$			5 $\uparrow$			ns
Operating free-air temperature, $T_A$		-55		125	0		70	$^\circ\text{C}$

$\uparrow$  The arrow indicates that the rising edge of the clock pulse is used for reference.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONST		SN54LS273		SN74LS273		UNIT
				MIN	TYP‡	MAX	MIN	
V <sub>IH</sub>	High-level input voltage			2			2	V
V <sub>IL</sub>	Low-level input voltage					0.7		0.8
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN,	I <sub>I</sub> = − 18 mA			−1.5		−1.5
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,					
		V <sub>IL</sub> = V <sub>ILmax</sub> ,	I <sub>OH</sub> = −400 μA	2.5	3.4		2.7	3.4
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4
				I <sub>OL</sub> = 8 mA			0.35	0.5
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V			0.1		0.1
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V			20		20
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V			−0.4		−0.4
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX		−20		−100	−20	−100
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX,	See Note 2		17	27		17
							27	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to clock.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{max}}$ Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 3	30	40		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			18	27	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock			17	27	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



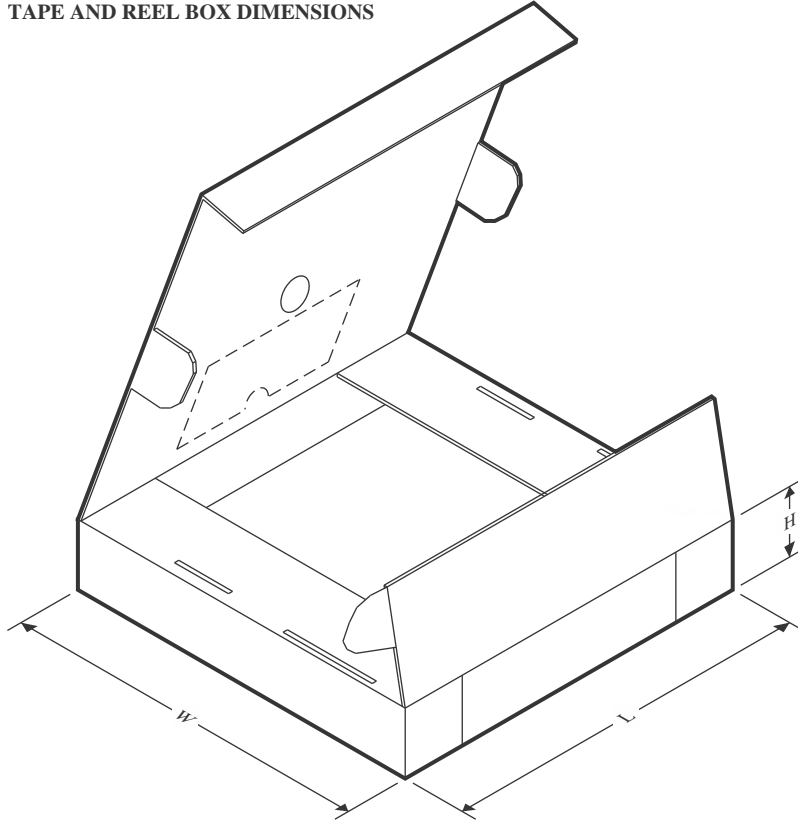
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS273DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LS273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS273NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

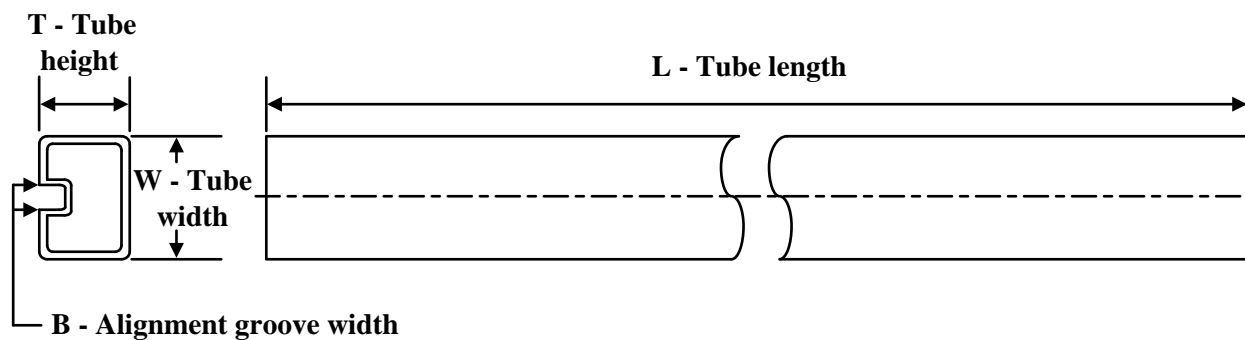
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS273DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LS273NSR	SOP	NS	20	2000	356.0	356.0	45.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
78010012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7801001SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/32501B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/32501B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/32501BSA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/32501BSA.A	W	CFP	20	25	506.98	26.16	6220	NA
M38510/32501B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/32501BSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LS273N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS273N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS273NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS273FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS273FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS273W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54LS273W.A	W	CFP	20	25	506.98	26.16	6220	NA



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