Am25S07•Am25S08

Hex/Quad Parallel D Registers With Register Enable

Distinctive Characteristics

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

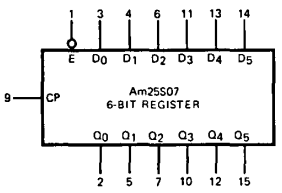
FUNCTIONAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similiar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

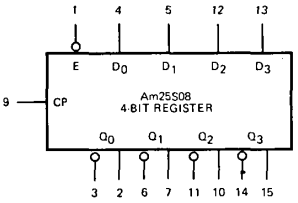
Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC SYMBOLS

Am25S07



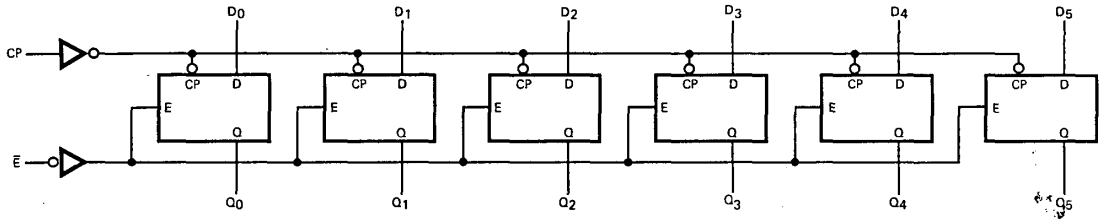
Am25S08



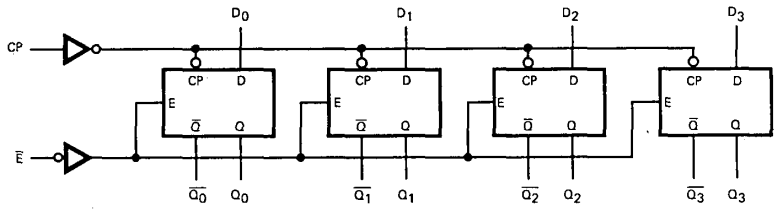
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am25S07



Am25S08

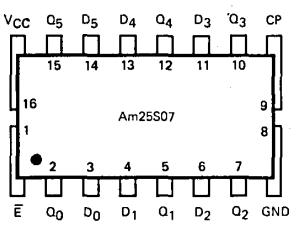


ORDERING INFORMATION

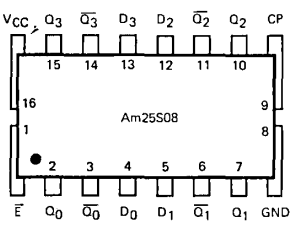
Package Type	Temperature Range	Am25S07 Order Number	Am25S08 Order Number
Molded DIP	0°C to +70°C	AM25S07PC	AM25S08PC
Hermetic DIP	0°C to +70°C	AM25S07DC	AM25S08DC
Dice	0°C to +70°C	AM25S07XC	AM25S08XC
Hermetic DIP	–55°C to +125°C	AM25S07DM	AM25S08DM
Hermetic Flat Pak	–55°C to +125°C	AM25S07FM	AM25S08FM
Dice	–55°C to +125°C	AM25S07XM	AM25S08XM

CONNECTION DIAGRAMS
Top Views

Am25S07



Am25S08



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S07XC, Am25S08XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am25S07XM, Am25S08XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XC	2.7	3.4		Volts
			XM	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	S07		90	144	mA
			S08		60	96	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280 Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data		5.5			ns
t_s	Enable			7		ns
t_h	Data		3	0		ns
t_h	Enable		3	0		ns

Am25S07 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

Am25S08 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Q_i The TRUE register outputs.

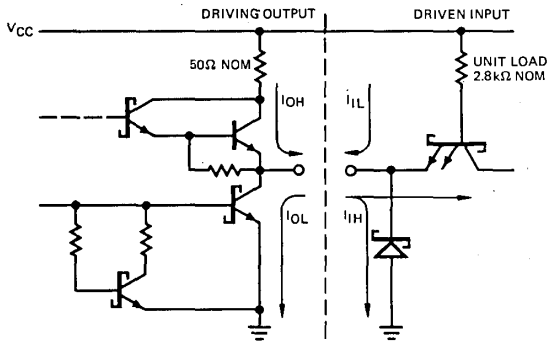
$\overline{Q}_i$ The complement register outputs

FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_i	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

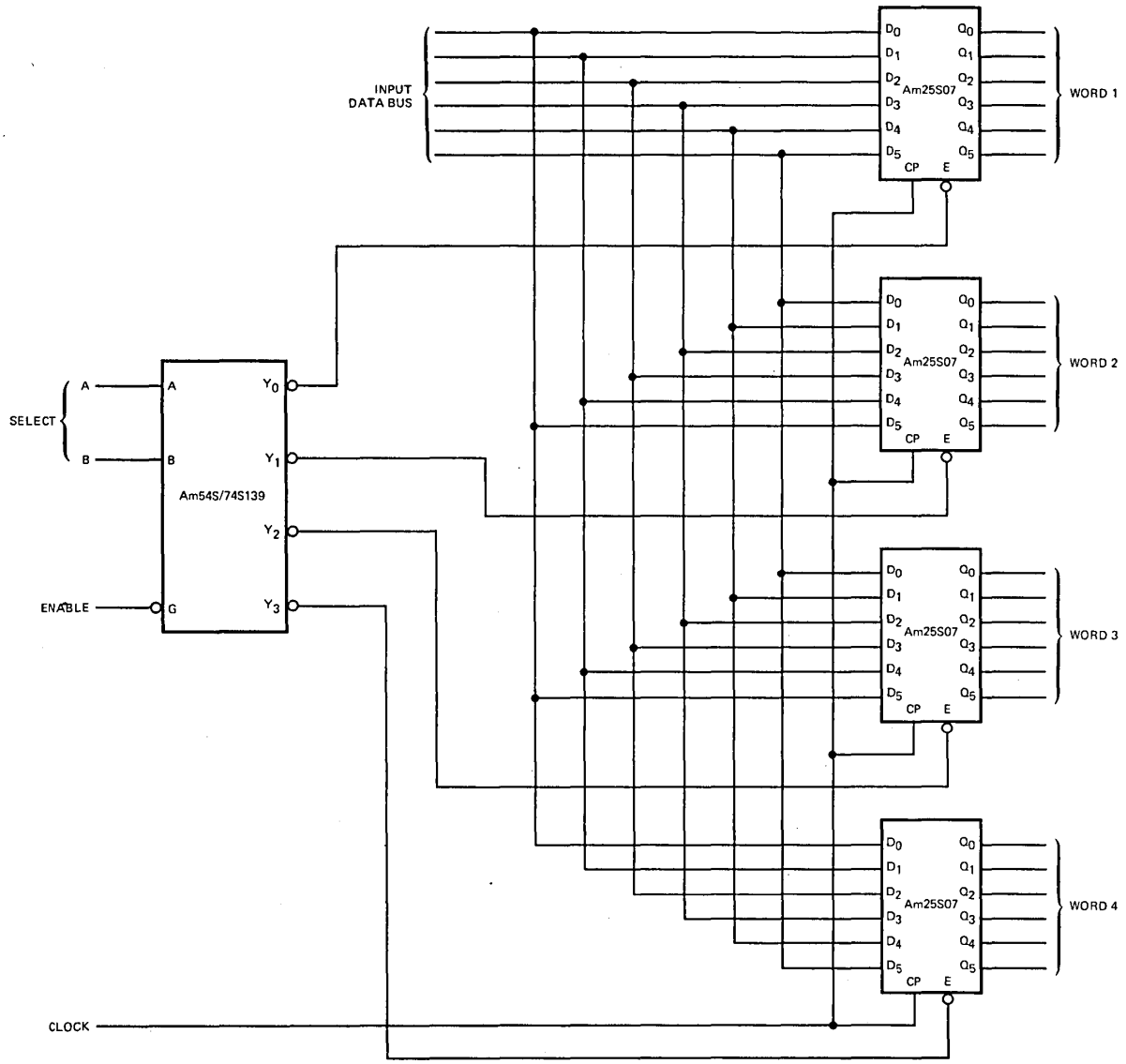
H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25S08 Only

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



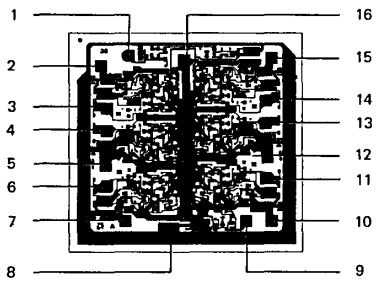
Note: Actual current flow direction shown.

APPLICATIONS



Selective Register Loading of Data on Synchronous Clock.

Pad Layout



DIE SIZE 0.085" X 0.081"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

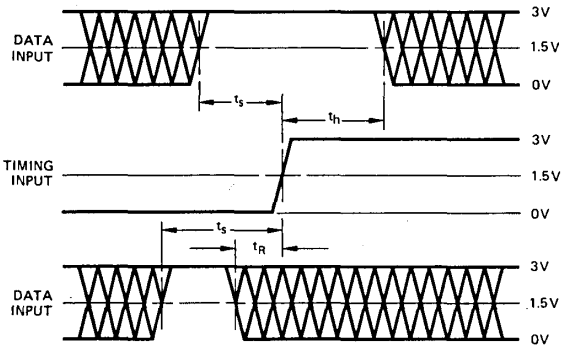
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

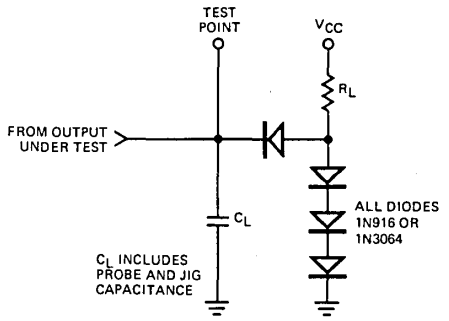
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

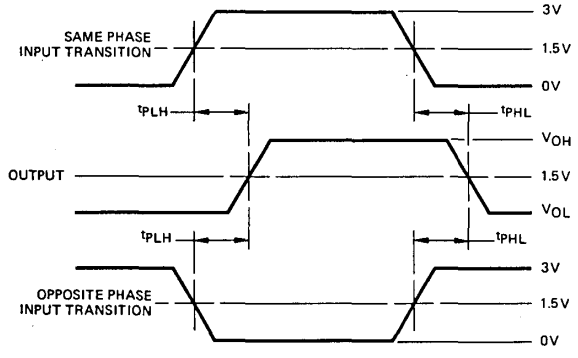


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

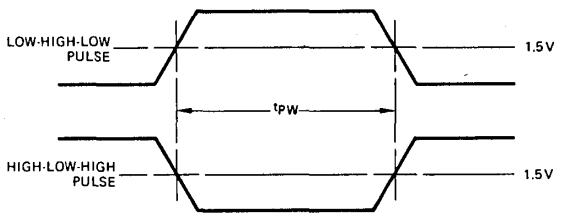
LOAD TEST CIRCUIT



PROPAGATION DELAY

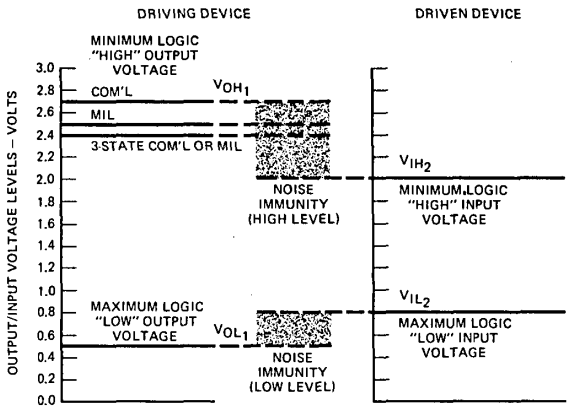


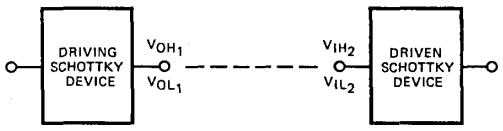
PULSE WIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$, $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

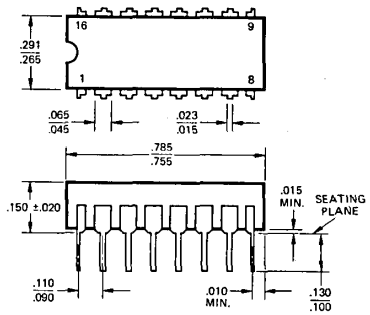
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

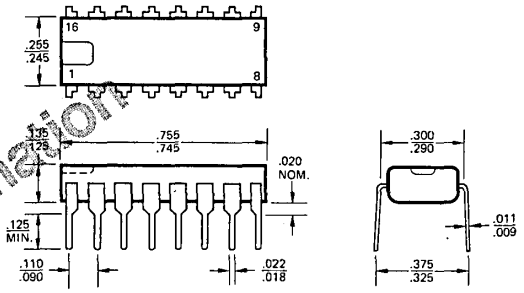
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

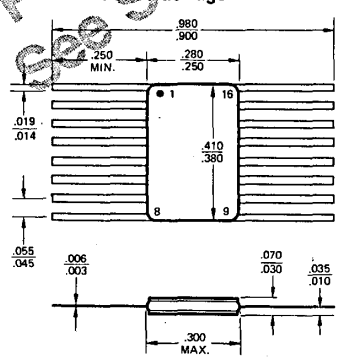
Molded



Ceramic



Flat Package



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