Am29700 • Am29701

Noninverting Schottky 64-Bit RAM

Refer to

Am27S06 • Am27S07

Bipolar Memory RAM Product Specification

The Am29700 is replaced by the Am27S06 (open collector).

The Am29701 is replaced by the Am27S07 (three-state).

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Am27LS06 • Am27LS07

Low Power, Noninverting 64-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit low power Schottky RAMs
- Ultra-low power: I_{CC} typically 30mA
- High-speed: Address access time typically 40ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27LS07) or with open collector outputs (Am27LS06)
- 100% MIL-STD-883 assurance testing
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

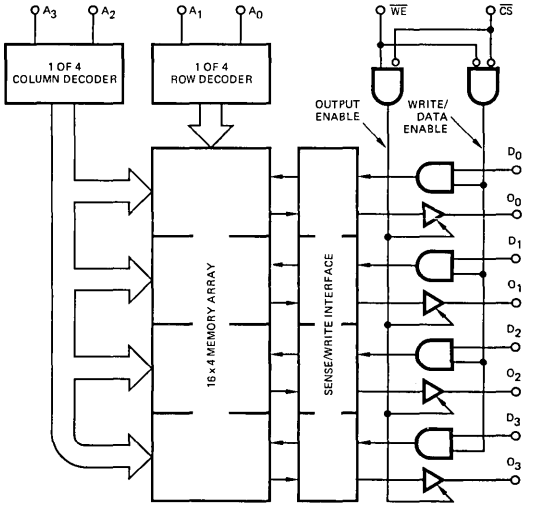
The Am27LS06 and Am27LS07 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27LS06) or three-state outputs (Am27LS07). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74LS189.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four noninverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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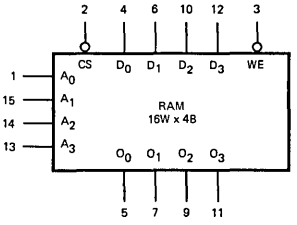
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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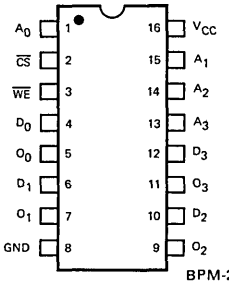
CONNECTION DIAGRAMS
Top Views

DIP



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Chip-Pak™

Note: Pin 1 is marked for orientation.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Input		Function	Data Output Status O_{0-3}
$\overline{CS}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word (Not Inverted)
High	Don't Care	Deselect	Output Disabled

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	DC Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Am27LS07 only)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.6		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.280	0.45	Volts
			I_{OL} = 10mA			0.310	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3			−0.015	−0.250	mA
			$\overline{CS}$			−0.030	−0.250	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V				0	10	μA
I_{SC} (Am27LS07 only)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX		COM'L		30	35	mA
				MIL		30	38	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V	Am27LS06/07			0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX	Am27LS07		−40	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots and undershoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

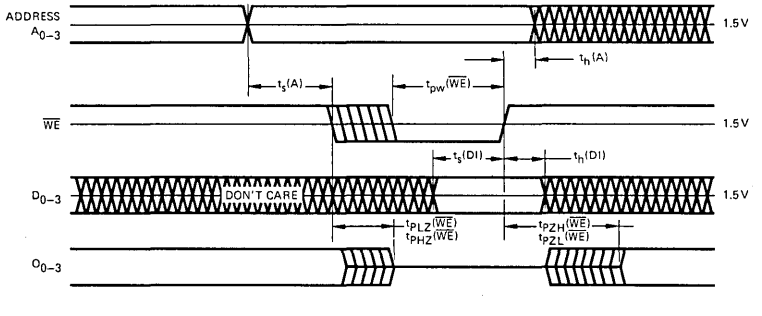
Parameters	Description		AC Test Conditions	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	Figure 3 Test Load and Figure 4 for Input Waveform Characteristics See Notes 3 and 4	40		55		65	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select to Active Output and Correct Data	See Fig. 2		18		30		35	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1		18		30		35	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1		−17	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1		−6	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1		16	45		55		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1		−8	0		0		ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	See Fig. 1		25	45		55		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (HI-Z)	See Fig. 2		18		30		35	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1		18		30		35	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in (noninverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. For open collector Am27LS06, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (O_0-O_3), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and C_L = 30pF and with both the input and output timing referenced to 1.5V.
4. For 3-state output Am27LS07, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

SWITCHING WAVEFORMS

WRITE MODE

($\overline{CS}$ = LOW unless otherwise noted)



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KEY TO TIMING DIAGRAM

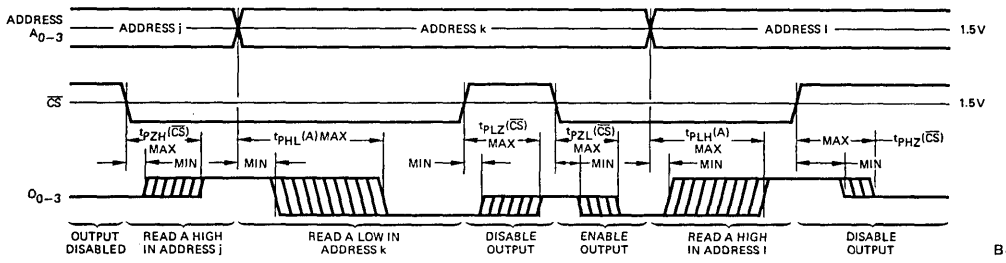
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
⟋⟋⟋	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⟋⟋⟋	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS07) while the write enable is LOW or the chip select is HIGH.

Figure 1.

SWITCHING WAVEFORMS (Cont.)

READ MODE



Switching delays from address and chip select inputs to the data output. For the Am27LS07, disabled output is "OFF", represented by a single center line. For the Am27LS06, a disabled output is HIGH.

Figure 2.

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

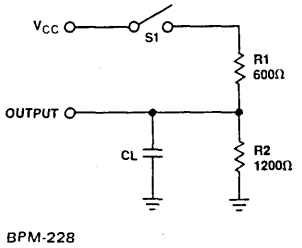


Figure 3.

INPUT PULSES

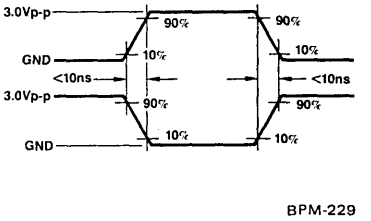


Figure 4.

See notes 2, 3 and 4 of Switching Characteristics.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
55ns	AM27LS06PC	AM27LS07PC	P-16-1	C-1	COM'L
	AM27LS06PCB	AM27LS07PCB	P-16-1	B-1	
	AM27LS06DC	AM27LS07DC	D-16-1	C-1	
	AM27LS06DCB	AM27LS07DCB	D-16-1	B-1	
	AM27LS06LC	AM27LS07LC	Consult Factory	C-1	
	AM27LS06LCB	AM27LS07LCB	Consult Factory	B-1	
65ns	AM27LS06DM	AM27LS07DM	D-16-1	C-3	MIL
	AM27LS06DMB	AM27LS07DMB	D-16-1	B-3	
	AM27LS06FM	AM27LS07FM	F-16-1	C-3	
	AM27LS06FMB	AM27LS07FMB	F-16-1	B-3	
	AM27LS06LM	AM27LS07LM	Consult Factory	C-3	
	AM27LS06LMB	AM27LS07LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.