Prototype Design

S2019 – Edit this document into a deliverable.

Lab Section:	1	Group:	17

Necessary Changes and Notes

Answer these questions by editing and adding to Table 1 and Table 2 below.

Table 1: What changes had to be made to get your Feasibility Model working as expected?

Table 1: Necessary Design Changes

#	Change	Reason/Notes
1	Update resistor values for multiplexer	There were some discontinuities in values we can measure with the old resistors
2	Connect Z input within multiplexer to 3.3V	Some misunderstandings on how the multiplexer functions resulted in incorrect connection of the Z output
3	Averaged the ADC values to reduce noise	The values of the ADC were changing too frequently due to noise

Table 2: Lessons Learned – Is there anything you want to remember so that you don't make the same mistake again? Or, not waste time on something you already figured out?

Table 2: Important Notes

#	Note
1	The enable pin on the multiplexer is active low
2	The resistance sensing circuit is more accurate if the reference resistor is higher than the unknown resistance
3	The ADC internal reference voltage can be adjusted to be 3.3V or 1.5V

Signal Specifications

Answer these questions by editing and adding to Table 3 below.

Table 3: For all the important signals in your Prototype:

- Name the signal
- State which signal property is important (voltage, frequency, rise time, etc.)
- State whether you need to include a Test Point (TP) on the PCB so you can probe the signal
- State which software mode will let you test the signal as indicated
  - You may need to create a special test mode in your code to exercise the signal to its limits
- State the Minimum (Min), Nominal, and Maximum (Max) acceptable values for that signal property
- Include signals for attached components, modules, sensors, etc. Do not include power rails.

Table 3: Hardware Signal Test Plan

Signal (TP*)	Property	Required Software Mode	Min	Nominal	Max
Mux Enable	Voltage	Setup	0 V		3.3 V

Mux Select 0	Voltage	Switching resistances	0 V	3.3 V
Mux Select 1	Voltage	Switching resistances	0 V	3.3 V
Mux Select 2	Voltage	Switching resistances	0 V	3.3 V
ADC In (*)	Voltage	Connecting new resistance	0 V	3.3 V

**Indicates Test Point Required*

Signal Mapping

Answer these questions by editing and adding to Table 4 below.

Table 4: How will your Prototype design electrically connect to the LaunchPad?

MSP430FR4133 IC pin <--> BoosterPack pin on J1/J2 of the LaunchPad <--> Your Prototype

Table 4: Hardware Signal Connectivity

Signal	MSP430FR4133 Pin	LaunchPad J1/J2 Pin	Prototype Connection
Analog In	P8.0 (A8)	J2 pin 6	Unknown resistor
Analog Out	P5.0	J3 pin 4	Mux Enable
Analog Out	P1.3	J3 pin 8	Mux Select 0
Analog Out	P1.4	J3 pin 9	Mux Select 1
Analog Out	P1.5	J3 pin 10	Mux Select 2

Tips for making your schematic

This is covered in the **DipTrace Schematic Design Guidelines** document but is noted here for convenience in the order it appears in Checklist #2.

- All schematic sheets have a border with Project Name, Lab Session, and Group. This makes it really clear whose schematic is whose.
- There is a common GND used for 5.0 V and 3.3 V powered devices. This ensures that 0 V is the same for all pins and devices.
- Add a GND header pin to your board so that lab equipment probes can have a signal reference. You can clip onto it with scope probe ground or alligator clips.
- There are bulk decoupling capacitors (10 µF) added for power pins. They work like charge gas tanks to keep the voltage high during a current spike.
- There are device decoupling capacitors (100 nF) added between device power and GND pins. This gives a low impedance path for noise voltage to GND instead of through the device.
- All signal nets are named and assigned to their ap propriate net class. Just like variables in your code, you want to explicitly name everything in your schematic.
- Analog signals are kept separate from digital signals to avoid switching noise via capacitive coupling.
- Test points are included as per Table 3.
- The last schematic sheet is a Bill of Materials (BOM).
- An ERC (Electrical Rules Check, under Verification → Electrical Rule Check in DipTrace) for schematic net connections has been run successfully.
- The schematic is "reader friendly"
  - Busses to group signals. For example, if an IC needs eight data bits, group them in a bus
  - Don't make the reader hunt for net connection endpoints
  - Nets are neat and tidy, aligned with each other, and not unnecessarily crisscrossing
- Expected rail currents are listed. Add up all the max current you expect to draw from 3.3 V and 5.0 V and note them in the schematic.

Tips for making your PCB

This is covered in the **DipTrace PCB Design Guidelines** document but is noted here for convenience in the order it appears in Checklist #2.

- The PCB form factor has (X, Y) corner coordinates at (0.0, 0.0); (57.2, 0.0); (57.2, 34.3); and (0.0, 34.3) measured in mm. This is the required board size we need so we can get it properly fabricated.
- The Launchpad connectors are at (X, Y) = (5.7, 17.8) mm for J1; and at (X, Y) = (51.4, 17.8) mm for J2. Otherwise, your PCB won't fit onto the LaunchPad BoosterPack headers.
- The remaining components are properly placed and grouped This means that components working together are nearby.
- The devices are properly oriented for best routing. E.g., resistors in parallel should be placed side by side oriented so that the commonly shared nets are physically close.
- The decoupling capacitors are properly placed and routed, meaning they are physically close to the device power pins
- The PCB has test points in appropriate locations (physically accessible by a scope probe, near the signal of interest).

- Silkscreen includes reference designators, identifiers, and polarity markings (include Pin 1 marking for multi-pin components – could be a dot, a number '1', etc.)
- Silkscreen text and markings are of adequate size and are not on pads
- (LAB SESSION#_GROUP#) been added on the Top Silkscreen layer by the J1 connector (e.g. 2_13)
- DRC (Design Rules Check, under Verification → Check Design Rules in DipTrace) passes with the ECE-298_mm.rul file. This means that there are no anticipated fabrication problems (traces aren't too narrow, too wide, no unrouted nets, etc.)
- LVS (Layout vs Schematic, under Verification → Compare To Schematic in DipTrace) passes design net connectivity comparison with schematic

Other Best Practices

- Keep decoupling capacitors close to digital device power pins
- Keep adequate space around components to add part identifier silkscreen info ("R1", "C6", etc.)
- Separate analog devices power/GND signal paths from digital devices power/GND routes
- If there is room, add info in the Top Silkscreen layer for indicator functions (e.g., "Temp Good", "Test Mode", etc.)
- You may place components on the bottom if the need arises (i.e., insufficient room on the top side), but it is usually cheaper in production to get all components on **one** side of a PCB, if possible.
- Your circuit devices may have connections that include GND as a reference (see below). Especially for ANALOG signals it is important to route the GND connection for signals separately from GND returns for devices, otherwise power noise may be coupled from the signal to the MCU.