Authoring Since 2018

Foreword

In 2018, my research was concentrated in **quantum computer**, especially superconducting quantum computer, but since 2019 I have taken a final decision to fix my research on **satellite broadband** Internet related **modulation and demodulation IC** technologies and design. This research orientation will be final.

Therefore in my future years my writing will be as follows:

- the writing of my mother's biography,
- the writing of my autobiography,
- and possibly one or two book(s) or papers in IC design for satellite Internet communications, particularly modulation and demodulation technologies.

Apart from these, I might also prepare for some business reports in the IC industry, particularly in the satellite internet industry, and possibly in other areas of businesses.

From time to time I might also write something important in our time.

And if I could be admitted into theological studies at a university or college or seminary, I would also plan to write one or two works in this direction.

And finally I need to maintain my two websites, one for satellite Internet, and the other is my private site. In addition to these I may maintain my presence on the web with my blogs, social media sites etc.

The above basically depicts all what I need to write in my late years. The crazy writing years of 2007-2017 is forever over.

ACADEMIC WRITING

IC Design and Verification

Hardware Verification

Review of Verification IP & IP Core Verification – An Abstract

Verification Methodologies-A Concise Introduction

000Hardware Verification for Analog and Mixed Signal.docx (new)

000Hardware Verification Planning - A Concise Introduction.docx (new)

Hardware Verification Tools

000Hardware Verification Planning Tools.docx (new)

000Hardware Verification Planning Tools.pdf

https://drive.google.com/
minghua.chen888@gmail.com
https://drive.google.com/file/d/1rOyMMHrYnQ-LdcI5KHTYgjFRHFR6wCkU/view?usp=sharing
https://drive.google.com/file/d/1rOyMMHrYnQ-LdcI5KHTYgjFRHFR6wCkU/view?usp=sharing
<iframe src="https://drive.google.com/file/d/1rOyMMHrYnQ-LdcI5KHTYgjFRHFR6wCkU/
preview" width="640" height="480" allow="autoplay"></iframe>

000AI ML Machine Learning for Hardware Design, Verification & Manufacturing.docx

000000ML Machine Learning for Analog and Mixed Signal Verification.docx

000AI ML Machine Learning for Hardware Verification.docx

Hardware Verification Language

Comprehensive Review of Hardware Verification Languages (Except Python)

Hardware Verification in Python

<iframe src=" /preview" width="840" height="680" allow="autoplay"></iframe>

Chapt. 01 Why Python
https://drive.google.com/file/d/1k73H7Xg4IyUuTkylqKRtaZkvCsvV3-md/view?usp=share_link
https://drive.google.com/file/d/1k73H7Xg4IyUuTkylqKRtaZkvCsvV3-md/view?usp=share_link

<iframe src=" https://drive.google.com/file/d/1k73H7Xg4IyUuTkylqKRtaZkvCsvV3-md/preview" width="840" height="680" allow="autoplay"></iframe>

Chapt. 02 Pure Python

https://drive.google.com/file/d/1azQBe88n8mrGH1_PuoIG_h_sU3_O8ShA/view?usp=share_link

<iframe src="https://drive.google.com/file/d/1azQBe88n8mrGH1_PuoIG_h_sU3_O8ShA/preview" width="840" height="680" allow="autoplay"></iframe>

Chapt. 03 cocotb

https://drive.google.com/file/d/1qJSaZlBfSm2szrV0RtFLNSidSncjsEjy/view?usp=sharing

<iframe src="https://drive.google.com/file/d/1qJSaZlBfSm2szrV0RtFLNSidSncjsEjy/preview" width="840" height="680" allow="autoplay"></iframe>

Chapt. 11 MyHDL - Python Based Hardware Description And Verification Language

https://drive.google.com/file/d/1BvqOp9d2g6Mc5EBRNpuI9G6bo_xlDUe5/view?usp=share_link

<iframe src="https://drive.google.com/file/d/1BvqOp9d2g6Mc5EBRNpuI9G6bo_xlDUe5/preview" width="840" height="680" allow="autoplay"></iframe>

Hardware Verification with Artificial Intelligence – current focus !!!!!!!!!!

My current research topic:

Artificial Neural Network for Test Generation Optimization in Hardware Verification

Book titled “Silicon IP – More than just Design” (stopped)

This book or rather a platform, a knowledge center, an information hub or an interactive venue on the Internet is being prepared along with my design work. It contains all aspects of the IP core business, industry,

technology as well as design process. It will become a book in huge volume - perhaps thousands of pages in A4 size, possibly web based and forever-updated (in the area of IP Core) with an interim title of "Silicon IP – More than just Design". The topic will go far beyond just the design aspect of the IP industry, and it will eventually all major sectors of this business. I will publish a small part of it in document formats such as Word or PDF, and also a small part of it will be made available at my website. But if you want more, you need pay for them.

Here below is a recently updated chaptering plan (it's changing on daily basis):

as of March 20, 2022

VOLUME 01 IP Core Introduction Chapter 0.docx
VOLUME 02 IP Core Types Chapter 1.docx
VOLUME 05 IP Core Development Flow Chapter 1.docx
VOLUME 05 IP Core Development Flow Chapter 2
VOLUME 05 IP Core Development Flow Chapter 3 - IP Core Generation for ASIC Design.docx
VOLUME 05 IP Core Development Flow Chapter 4
VOLUME 05 IP Core Development Flow Chapter 5
VOLUME 05 IP Core Development Flow Chapter 6
VOLUME 05 IP Core Development Flow Chapter 7
VOLUME 06 IP Core Design Technology Chapter 1 - ASIC.docx
VOLUME 06 IP Core Design Technology Chapter 2 - FPGA.docx
VOLUME 06 IP Core Design Technology Chapter 3 - SDR.docx
VOLUME 06 IP Core Design Technology Chapter 4 - DSP.docx
VOLUME 06 IP Core Design Technology Chapter 5 - GPU.docx
VOLUME 07 IP Core Design Languages Chapter 1 - VHDL.docx
VOLUME 07 IP Core Design Languages Chapter 2 - Verilog.docx
VOLUME 07 IP Core Design Languages Chapter 3 - Matlab.docx
VOLUME 07 IP Core Design Languages Chapter 4
VOLUME 07 IP Core Design Languages Chapter 4 - SpecC.docx
VOLUME 07 IP Core Design Languages Chapter 9 Transformation.docx
VOLUME 08 IP Core Development Tools Chapter.docx
VOLUME 09 IP Core from Soft to Hard Chapter.docx
VOLUME 10 Verification IP - VM History.docx
VOLUME 10 Verification IP.docx
VOLUME 11 Test IP.docx
VOLUME 12 Programmable Logic IP Cores in SoC Design.docx
VOLUME 13 Evolvable IP Cores.docx
VOLUME 14 IP Core Interface Chapter.docx
VOLUME 15 IP Core Synthesizing.docx
VOLUME 16 IP Core Testing Chapter.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-00 Foreword.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-01 Encryption of HDL Codes.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-02 Watermarking.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-03 Obfuscation of Designs.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-04 Fingerprinting.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-06 Physical Unclonable Functions(PUFs)-Based Authentication.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-07 Protection of IP Leakage.docx
VOLUME 17 IP CORE PROTECTION – Part I Soft IP - Chapter I-10 Computational Forensic Engineering.docx

VOLUME 17 IP CORE PROTECTION – Part IV General IP - Chapter IV -03 Remote Activation.docx
VOLUME 17 IP CORE PROTECTION – Part IV General IP - Chapter IV -04 Active Control.docx
VOLUME 17 IP CORE PROTECTION – Part IV General IP - Chapter IV -10 Tools.docx
VOLUME 18 IP Core License Chapter.docx
VOLUME 29 IP Core Deliverables Chapter.docx
VOLUME 30 IP Core Sources 01 Management Chapter.docx
VOLUME 30 IP Core Sources 02 Chapter 1 IP Core Sources.docx
VOLUME 30 IP Core Sources 03 Chapter 2 IP Core Developers.docx
VOLUME 30 IP Core Sources 04 Chapter 3 Organization.docx
VOLUME 30 IP Core Sources 05 Trustworthiness & Reliability Chapter 16.docx
VOLUME 30 IP Core Sources 06 Qualification Chapter.docx
VOLUME 30 IP Core Sources 07 Integration Chapter.docx
VOLUME 30 IP Core Sources 08 Integration Chapter 2 - IP Cores In SoC.docx
VOLUME 80 IP Core Research & The Academia.docx
VOLUME 90 IP Core Industry & Business World.docx
VOLUME 99 IP Core Additional Subjects.docx
VOLUME 100 IP Core Mathematics.docx
VOLUME 101 IP Core Physics.docx
References_Codes.docx
References_Literature.docx
References_Websites.docx

IP Core Protection

Protecting Your IP Cores – Part I Soft IP

IP Core Mathematics

Math for IP core and IC design and verification is a huge topic, and here below is a preliminary listing of possible areas of researches to be carried out over the next years: (updated Nov 25, 2022)

000000 VOLUME 16 IP Core Mathematics.docx

ARTIFICIAL INTELLIGENCE AI

0000Artificial Intelligence AI.docx

000artificial neural network.docx

000computer vision.docx

000ML_deep reinforcement learning.docx

000ML_DL deep learning.docx

000ML_Joint Learning.docx

000ML_Quantum Geometric Machine Learning.docx

000ML_RL Reinforcement Learning.docx

000ML_semi-supervised learning.docx

000ML_supervised learning.docx

000neural network.docx

000support-vector machines.docx

000weighted-majority voting.docx

Artificial Neural Network
Computer Vision
Expert Systems
Fuzzy Logic
Neural Network
Swarm Intelligence

Machine Learning

Active Learning
Bayesian Optimization
Deep Learning
Deep Reinforcement Learning
Joint Learning
Kernel Methods
Linear Regression
Logistic Regression
Quantum Geometric Machine Learning
Reinforcement Learning

Dyna-Style Reinforcement Learning
Prioritized Reinforcement Learning

Semi-Supervised Learning
Supervised Learning

BIG DATA

GRAPH COMBINATORICS OPTIMIZATION

HEURISTICS

Binary Decision Diagrams (BDD's).
Constraint Programming And Integer Programming
Coordinate Search
Genetic Search
Hooke-Jeeves
MADS - Mesh Adaptive Direct Search
Nelder-Mead Simplex
PSADE (global)
SAT solver
SMT solver
Successive Approximation Simplex

OTHERS

Benchmark Sets
Formal Methods

Formal Verification

Bounded Model-Checking (BMC)
Semantic Representations

Model Checking

Kripke Structures
Partitioned Transition Relations
Symbolic Model Checking
Temporal Logic Model Checking Algorithm

Probability

Monte Carlo Analysis

QUANTUM COMPUTER

Math (AI & Heuristics) for Quantum Algorithms

Math (AI & Heuristics) for Qubits

Coherent Transport
Correlated Qubit Errors
Decoupling
Design Of Logical Qubits
Quantum Error Correction
Quantum Interference
Quantum Spin Chains

Quantum Spin-1/2 Network
Quantum State Preparation
Qubit Allocation
qubit assignment
Qubit Coherence
Qubit Coherent Superposition
Qubit Coherent Transport
Qubit Control
Qubit Decoupling
Qubit Detection
Qubit Entanglement
Qubit Fidelity
Qubit Fine-Tuning
Qubit Layout
Qubit Mapping
Qubit Measurement
Qubit Movement
Qubit Placement
Qubit Readout
Qubit Routing
Qubit Scalability
Qubit Scheduling
Qubit Superposition
Teleported Operations

000Math (AI & Heuristics) for Qubit Allocation.docx
000Math (AI & Heuristics) for Qubit Mapping.docx
000Math (AI & Heuristics) for Qubit Measurement.docx
000Math (AI & Heuristics) for Qubit Placement.docx

000Math (AI & Heuristics) for Qubit Routing with AI ML RL
000Math (AI & Heuristics) for Qubit Routing.docx
000Math (AI & Heuristics) for Qubits.docx

Math (AI & Heuristics) for Quantum Gates

Math (AI & Heuristics) for Quantum Circuits

Quantum circuit layout

Math (AI & Heuristics) for quantum registers

Math (AI & Heuristics) for quantum processors

Math (AI & Heuristics) for Quantum Computer

Math (AI & Heuristics) for quantum compiler

Quantum Computer (old days, Stopped)

Quantum Computer in General (Stopped)

Following documents were being prepared:
quantum_intro

quantum_research_plan

quantum_studies_schedule

quantum_computer_writing_plan

quantum algebra

quantum_Turing_machine

quantum_algorithms

quantum_arithmetic

quantum_basics

quantum_chip

quantum_circuits

quantum_communication

quantum_complexity

quantum_computation

quantum_computer

quantum_computing

quantum_device

quantum_electronics

quantum_gates

quantum_general

quantum_informatics

quantum_information

quantum_logic

quantum_mechanics

quantum_network

quantum_optics

quantum_physics

quantum_probability

quantum_processor

quantum_programming

quantum_qubits

quantum_register

quantum_researchers

quantum_switching

quantum_technologies

quantum_theory

quantum_wires

graph4quantum

Superconducting Qumputer (Stopped)

Stopped

ResearchWritingProject4SuperconductingQumputer_Letter_DE.docx
ResearchWritingProject4SuperconductingQumputer_Letter_EN.docx
ResearchWritingProject4SuperconductingQumputer_Letter_FR.docx
ResearchWritingProject4SuperconductingQumputer_Plan_DE.docx
ResearchWritingProject4SuperconductingQumputer_Plan_DE.pdf
ResearchWritingProject4SuperconductingQumputer_Plan_EN.docx
ResearchWritingProject4SuperconductingQumputer_Plan_EN.pdf
ResearchWritingProject4SuperconductingQumputer_Plan_FR.docx
ResearchWritingProject4SuperconductingQumputer_Plan_FR.pdf

SuperconductingQumputer19People.docx

SuperconductingQumputer01Definitions.docx

SuperconductingQumputer02Theories.docx

SuperconductingQumputer03AlgorithmsApplications.docx

SuperconductingQumputer04Types.docx

SuperconductingQumputer05ArchitectureStructures.docx

SuperconductingQumputer06Materials.docx

SuperconductingQumputer07Designs.docx

SuperconductingQumputer08Features.docx

SuperconductingQumputer09Manufacturing.docx

SuperconductingQumputer10MeasurementControl.docx

SuperconductingQumputer11CalibrationCharacterization.docx

SuperconductingQumputer12Tests.docx

SuperconductingQumputer13Operations.docx

SuperconductingQumputer13OperationsCoherence.docx

SuperconductingQumputer13OperationsDecoherence.docx

SuperconductingQumputer13OperationsEntanglement.docx

SuperconductingQumputer13OperationsErrorCorrection.docx

SuperconductingQumputer13OperationsFaultTolerance.docx

SuperconductingQumputer13OperationsInterference.docx

SuperconductingQumputer13OperationsSuperposition.docx

SuperconductingQumputer13OperationsTeleportation.docx

SuperconductingQumputer14QuantumGates.docx

SuperconductingQumputer15QuantumCircuits.docx

SuperconductingQumputer16QuantumComputer.docx

SuperconductingQumputer17Software.docx

SuperconductingQumputer18Breakthroughs.docx

SuperconductingQumputer20Organizations.docx

SuperconductingQumputer22Literature.docx

Satellite Internet Modem Design

Modulator, Demodulator, Modem ICs for Satellite Internet Terminals - Ongoing

Ongoing

Modulator, Demodulator, Modem ICs for Satellite Internet Terminals.docx

This design involves a lot of relevant technologies, for example:

algorithms.docx

coding_error_correction.docx

CORDIC.docx

dac_adc.docx

decimators_interpolators.docx

design_methodologies.docx

filtering.docx

framing.docx

frequency_bands.docx

frequency_conversion.docx

interleaving.docx

local_oscillator.docx

mapping.docx

mode_adaptation.docx

modulations_demodulation.docx

phase_lock_loop.docx

scrambling.docx

standards_protocols.docx

stream_adaptation.docx

systems.docx

Graph Theory (Stopped)

Hypergraph partition pp210

Hypergraph modeling of circuits - general, pp40

APPLICATION WRITING

Software reverse engineering (Stopped)
pp350

Network security technologies (Stopped)
pp80

BUSINESS WRITING

China Satellite Broadband MONTHLY REPORT, presentation, pp50
China IC MONTHLY REPORT, A Brief Introduction, pp50

OTHERS

Mother's biography – suspended
Autobiography – suspended

WEBSITES

http://www.plutuse.com/ obsolete
http://www.angelia.space/ obsolete