Angelia RFID TAG - EPC C1G2 - No 001 v1.0

EPC Gen-2 RFID Tag Baseband Processor IP Core in Verilog

Introduction

A low-cost low-power baseband processor IP core for EPC Gen-2 UHF RFID Tag written in Verilog language.

Part No

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FEATURES

It is operated in the lowest frequency (see FM0 and Miller Encoder/Decoder) with clock gating, and operand isolation.

It is improved by TSMC 180 nm CMOS standard process.

To use it, you need a memory (ROM or RAM)

STANDARD SPECIFICATIONS

EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID
Specification for RFID Air Interface Protocol for Communications at 860 MHz – 960 MHz
Version 2.0.0 Ratified

Verilog Modules / Files

NAME	DESCRIPTION
bb_proc	baseband processor, top module
cmd_buf	command buffer, serial to parallel
cmd_proc	command processor, processes received commands
crc16	CRC-16 encoder/decoder
crc5	CRC-5 encoder/decoder
crg	clock/reset generator, timing control
fm0_enc	FM0 encoder, operates in the lowest freq.
frmgen	frame generator, generates preamble, backscattered data, end-of-signaling
fs_detector	frame-sync detector
mem_if	memory interface
miller_enc	Miller encoder, operates in the lowest freq.
prng	16-bit Pseudorandom number generator
rx	receiver
two_dff_sync	synchronizer, synchronizes signals from clock domain A to B
tx	transmitter

Test Bench

bb_proc_tb : an example of the communication between a Reader and a single Tag

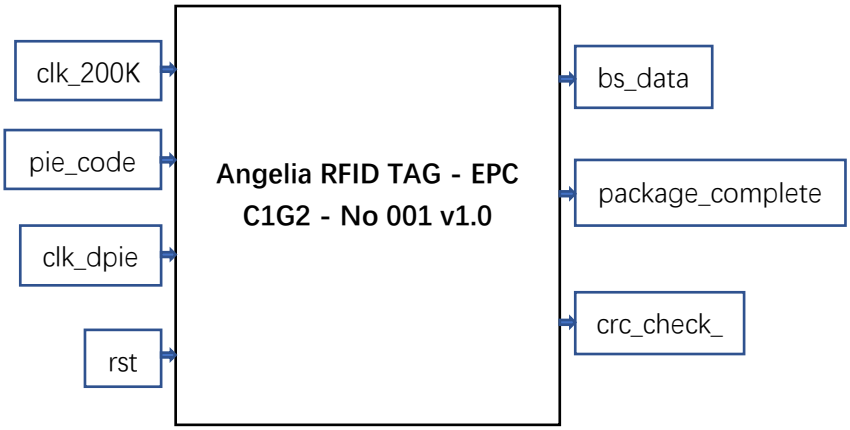
Scripts

bb_proc_syn : for synthesis
bb_proc_apr : for APR

ROM Code File

rom_code : 64x16, 64 words and 16 bits per word

Pins



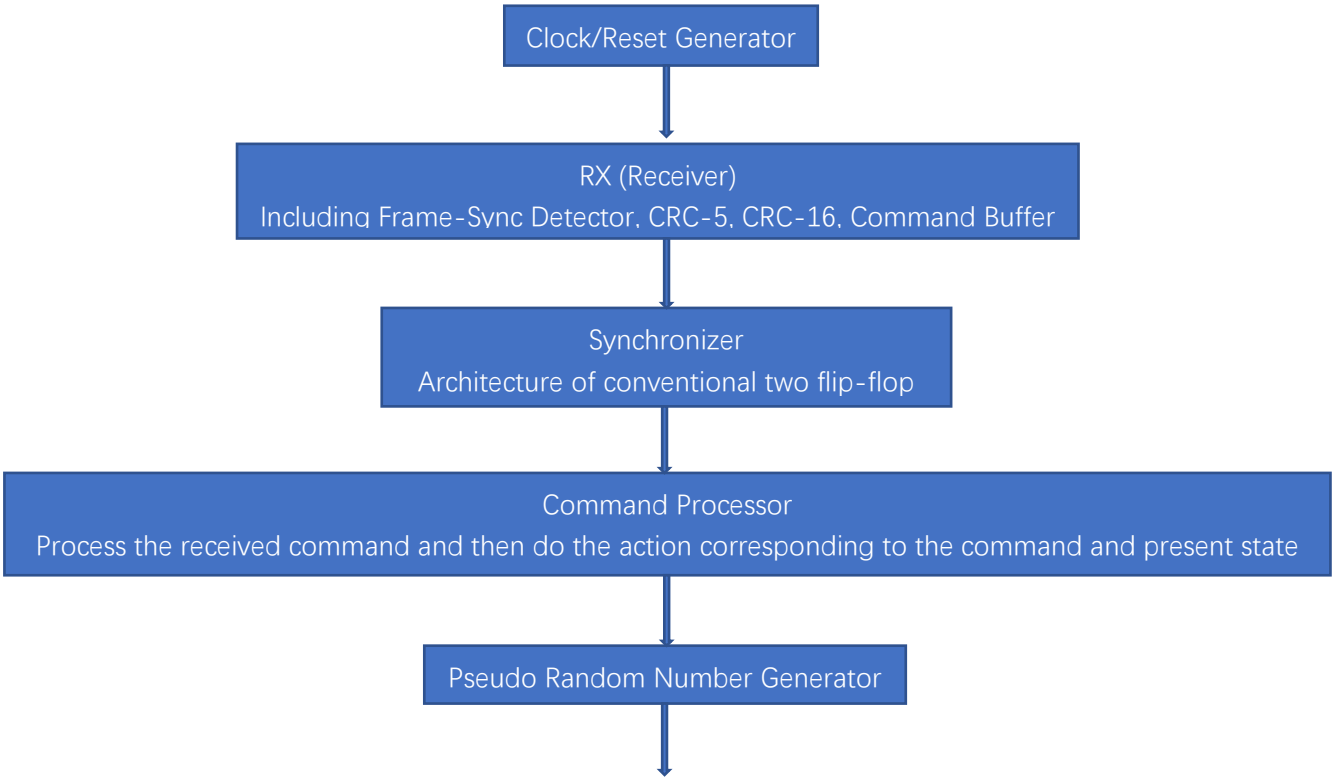
Input PIE code (pie_code)
Input delayed PIE code (clk_dpie)

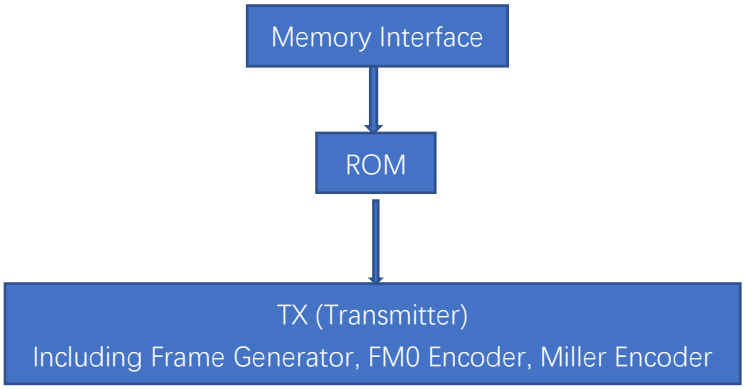
Clock signal in 200 KHz generated by Multivinrator to generate the clock signal in BLF. (clk_200K)
rst is generated by POR circuit in our analog front-end circuit to reset the baseband processor. (rst)

Output the backscattered data after processing and computing to control the backscatter circuit in our analog front-end circuit. (bs_data)

Output signals package_complete and crc_check_pass are not necessary for our RFID Tag design.

Block Diagram





Notes

This design is improved by TSMC 180 nm CMOS standard process. For tapeout, I suggest you to generate an EEPROM.

Deliverables

Verilog source code

Verilog testbenches

Test bench Scripts

Synopsys synthesis scripts
Synthesized by Synopsys Design Compiler

Synopsys IC Compiler
APR by Synopsys IC Compiler

Design specification

Integration Guide

See INTEGRATION GUIDE.pdf

Developer

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