DVB S2 Demodulator IP Core in Verilog

IP Core Serial Number

IP Type

Soft IP

Standard

DVB S2 System from ETSI EN 302 307-1 V1.4.1 (2014-11)
Digital Video Broadcasting (DVB);
Second generation framing structure, channel coding and modulation systems for Broadcasting, Interactive Services, News Gathering and other broadband satellite applications;
Part 1: DVB-S2

Language

Verilog

Maturity / Status

Pre-Silicon

Overview

The design, architecture and implementation of a digital baseband demodulator for DVB-S2 satellite receivers are presented. The demodulator's architecture is based on a powerful DSP processor with on-chip memory and external highspeed data ports, thus providing a stand-alone solution. The demodulator implements the full signal-processing chain at the physical layer including: symbol timing recovery, frame synchronization, carrier frequency and phase recovery, automatic gain control and constellation decoding. The integration of the different multi-domain signal processing stages in a single processor is realized by the development of efficient fixedpoint implementations of the various demodulation algorithms that exploit the parallel-instruction execution capabilities of the target CPU. Efficient time-scheduling of the various software tasks enables the dynamic intercommunication of the different signal processing stages that are executed sequentially or in parallel, thus enabling real-time execution.

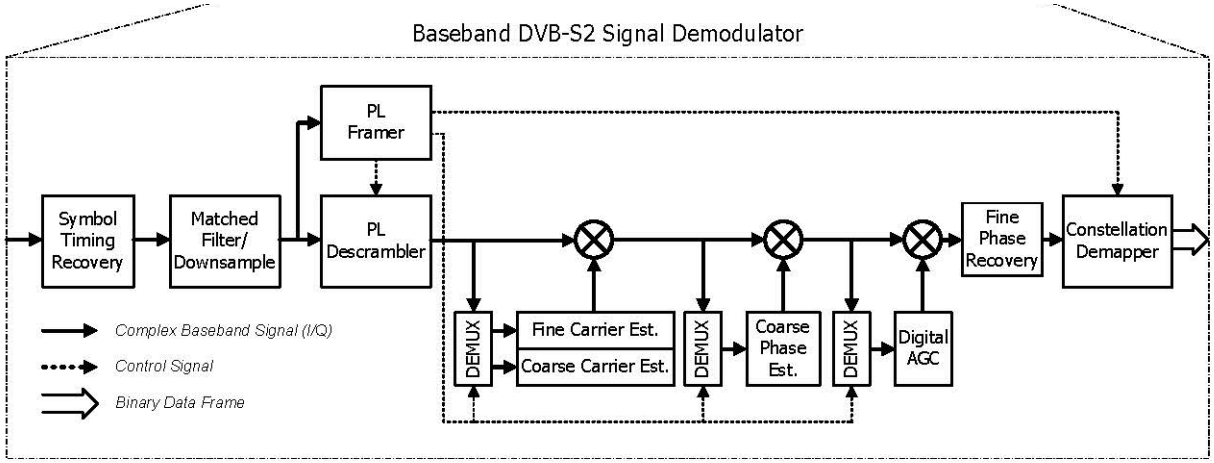
The prototyping of the demodulator and its verification in the design of a complete digital DVB-S2 satellite receiver using a versatile testbed is also presented.

The implementations of the DVB S2 demodulator IP core are realized in GNU Radio, GPU, FPGA, ASICs, and other appropriate architectures.

Deliverables

Verilog source code
HDL simulation models
Comprehensive documentation

Block Diagram



Functional block diagram of the DVB-S2 Demodulator

System Components

The demodulator implements the full baseband signal-processing chain including: symbol timing recovery, frame synchronization, carrier frequency and phase error recovery, automatic gain control and M-ary constellation decoding. In particular, QPSK, 8PSK, 16APSK and 32APSK modulation formats are supported. FEC decoding is carried out by the concatenation of an LDPC inner decoder and a BCH outer decoder. A block de-interleaver is also preceded when high-order modulation formats, such as 8PSK, 16APSK and 32APSK, are used. DVBS2 supports two major transport modes: the MPEG transport stream and the DVB-S2 generic stream.

Symbol Timing Recovery

The first stage of the demodulator is the symbol timing recovery (STR). The functionality of this module is to track the symbol rate fluctuations introduced during signal transmission. STR is implemented as a second order feedback loop utilizing a Farrow structured cubic interpolator along with the non-data-aided (NDA) timing error detector (TED) proposed by Gardner, which provides the loop with the required error signal. Gardner TED is capable of operating under random symbols and unknown carrier frequency offset error without precise carrier synchronization.

At the output of the STR interpolator, the synchronized samples stream is matched filtered and finally down-sampled leading to a rate of one sample per symbol that feeds the rest of the signal processing chain. Fig. 1 shows the closed-loop STR using the NDA Gardner TED.

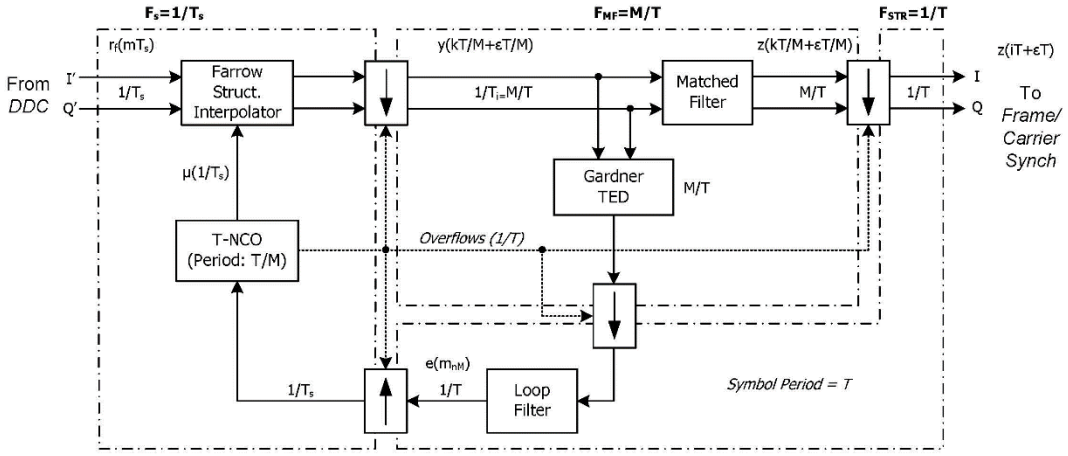


Fig. 1 Closed-Loop STR using the NDA Gardner TED

Frame Synchronization

After the STR has reached steady state, the next function to be performed is frame synchronization. This is done by searching the physical layer (PL) header using an appropriate correlator that operates on a symbol-by-symbol basis. Using differential detection, accurate frame synchronization is possible even in the presence of strong carrier frequency error. Fig. 2 shows the shift-register structure used for the detection of the DVB-S2 frame boundaries. Each frame starts with the PL header that consists of two parts, the Start of Frame (SOF) and the Physical Layer Signalling code (PLSC). SOF is a known 26-symbol pattern, while PLSC is a 64-bit linear binary code. The shift register in Fig 2 is partitioned into two sections. The first is associated with the SOF, the second with the PLSC. The output of the correlator drives a peak detector and has its maximum value when the whole PL header appears in the shift register.

A finite-state machine (FSM) controls the frame synchronization unit during acquisition and normal operation. After frame synchronization has locked, the data symbols (I/Q) of each frame are descrambled using a special Gold sequence in the complex domain. The scrambling process at the transmitter provides symbol randomization and is used for energy dispersal. In our implementation, the descrambling sequence is precalculated and stored locally in the DSP memory. Based on the correct framing alignment, it is possible to demultiplex (DEMUX) the pilot symbols from the incoming frame in order to drive the various pilot-aided carrier and phase synchronization circuits.

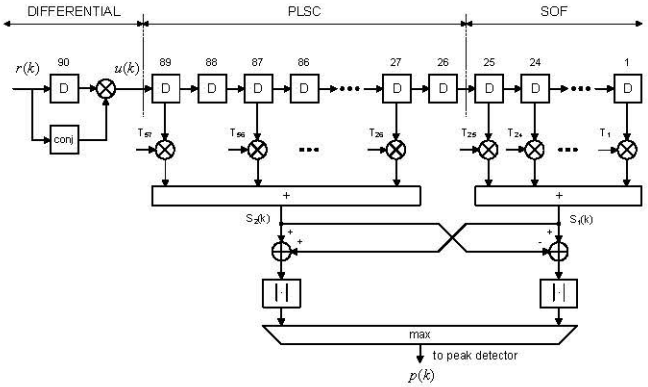


Fig. 2 Differential PL header detection

Carrier Frequency Recovery

Carrier frequency recovery (CFR) is invoked directly after the frame synchronization unit has detected the start of the transmitted frames and thus the locations of the respective pilot fields. CFR is performed in two sequential steps, which both use the known pilot symbols that are regularly repeated in the form of fields during the payload transmission of the DVB-S2 frames.

The first step of carrier synchronization consists of a coarse carrier recovery mechanism, which compensates large frequency offset errors up to several MHz and is implemented as a second order feedback loop based on a delay-and-multiply (DM) frequency error detector. The compensation of this loop is applied through the numerical control oscillator (NCO) embedded inside the DDC logic. Fig. 3 shows the coarse CFR mechanism, where Fs is the sampling frequency, Rs is the nominal symbol frequency and Rs is the recovered symbol frequency.

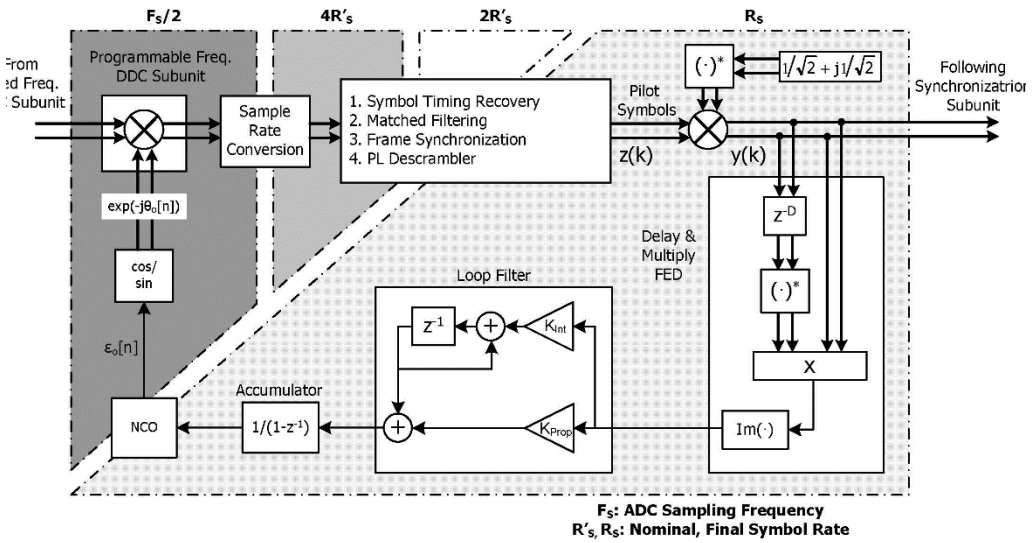


Fig. 3 Coarse carrier frequency recovery

After the convergence of the coarse carrier recovery loop, fine carrier recovery is initiated where the frequency offset error is in the order of a few hundreds of kHz.

Fine frequency recovery deploys a feed-forward estimation algorithm, derived from an alteration of the L&R

technique, and an integrator look-up table for the respective frequency offset removal. Fig. 4 depicts the fine frequency recovery scheme, which is also based on a closed loop structure.

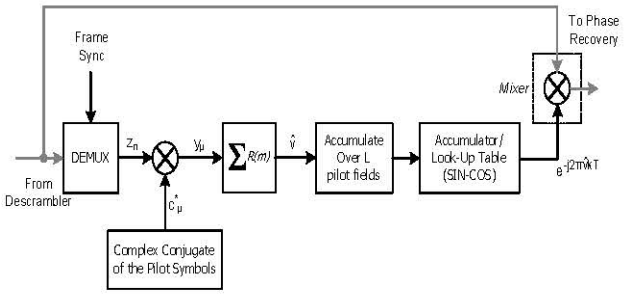


Fig. 4 Fine carrier frequency recovery

Phase Recovery

Phase recovery needs to cope with residual frequency offset resulting from both carrier recovery procedures. In case of low order modulation transmissions (QPSK or 8PSK), a pilot assisted maximum-likelihood (ML) feed-forward estimator is used for computing the average phase of each pilot field.

Phase compensation is based on the interpolation between the estimations of two consecutive pilot fields. When high-order modulations of 16APSK or 32APSK are used, an additional phase synchronizer is needed, which consists of a closed-loop based on the NDA phase error detector of Q-th power (Q=3 for 16APSK and Q=4 for 32APSK) . This NDA feedback loop is located after the digital amplitude control unit, which is described in the next subsection, and is initiated as soon as the ML feed-forward coarse estimator has reached its steady state. Figures 5 and 6 show the coarse and fine phase recovery units respectively.

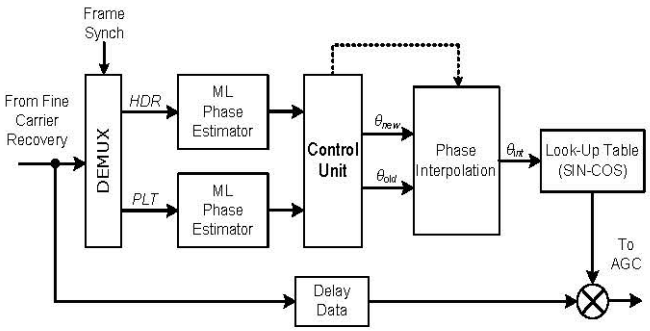


Fig. 5 Coarse phase recovery

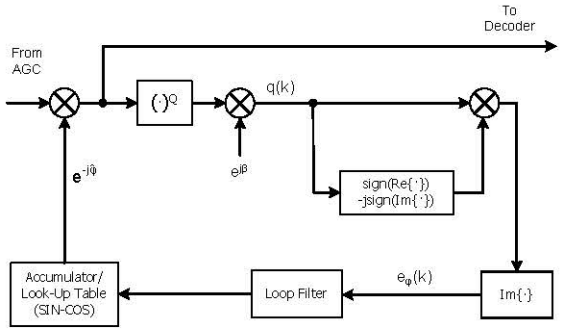


Fig. 6 Fine phase recovery

Digital Automatic Gain Control

Digital automatic gain control (DAGC) takes place after the first level of phase recovery and is based on a dataaided (pilot-assisted) vector tracker mechanism (DA-VT), which utilizes the known pilot symbols in order to determine the amplitude multiplication factor. Therefore, the DAGC is activated during the transmission of the pilot fields and it is frozen during data symbol transmissions, where proper amplitude adjustments are applied. Fig. 7 shows the DAGC unit.

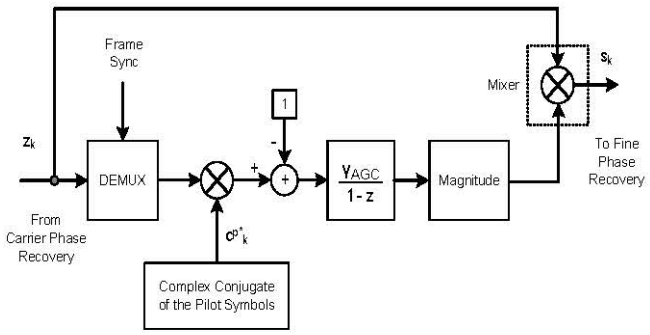


Fig. 7 Digital automatic gain control (DAGC)

Constellation Decoder

After the various synchronization parameters have been compensated, the complex I/Q symbols of the incoming frame are demapped into the data bit sequence based on the used modulation efficiency. The DVB-S2 standard supports the following modulation formats: QPSK, 8PSK, 16APSK and 32APSK. The output bit sequence is grouped into coded data frames (blocks) that feed the FEC decoding unit.

Fig. 8 describes the format of the physical layer frame (PLFRAME).

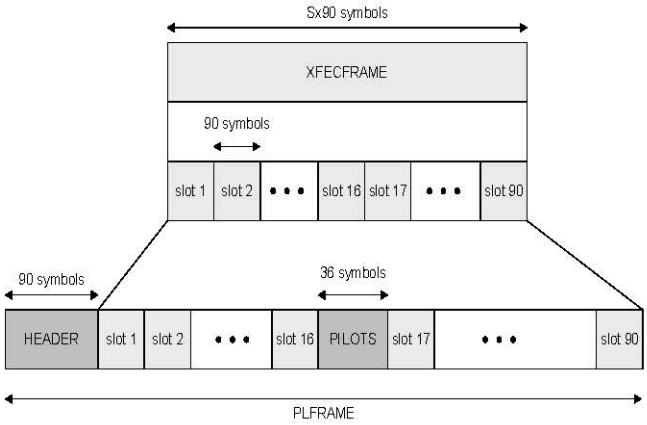


Fig. 8 Format of the DVB-S2 PLFRAME

The FEC encoded data, i.e. the LDPC codeword, form the FECFRAME, the length of which is 64800 or 16200 bit depending on the type of the DVB-S2 frame, namely normal or short frame respectively. Based on the modulation efficiency, the FECFRAME is divided into S slots of complex symbols, which form the XFECFRAME. The size of each slot is 90 symbols. The number of slots is given by
S = ηLDPC/(90 · ηMOD), where ηLDPC is the size of the LDPC codeword in bits and ηMOD is the modulation efficiency in bits-per-symbol.

In order to form the PLFRAME, a header is inserted in the beginning of each frame. If pilots are used, then a 36 symbols pilot field is inserted every 16 slots of data symbols. Given that a PLFRAME cannot terminate to a pilot field, the total number of pilot fields is αPIL = (S − 1)/16 . The total length of the PLFRAME in symbols is

K =
90 × (S + 1) without pilots
90 × (S + 1) + 36 × αPIL with pilots
(1)
while the efficiency of the frame format is η = (90 × S)/K. Table I displays the different parameters of the normal and short DVB-S2 frame for all constellation formats.

TABLE I
PARAMETERS OF THE *normal* AND *short* PLFRAME

	normal frame: η_{LDPC} = 64800 bits				short frame: η_{LDPC} = 16200 bits			
η_{MOD}	S	a_{PIL}	K	η (%)	S	a_{PIL}	K	η (%)
QPSK: 2	360	22	33282	97.35	90	5	8370	96.77
8PSK: 3	240	14	22194	97.32	60	3	5598	96.46
16APSK: 4	180	11	16686	97.09	45	2	4212	96.15
32APSK: 5	144	8	13338	97.17	36	2	3402	95.24

SOFTWARE ARCHITECTURE OF DEMODULATOR ALGORITHMS

The demodulator presented in this work comprises the basic component of a software-defined radio (SDR) implementation of a DVB-S2 satellite receiver developed on a powerful and reprogrammable hardware platform that utilizes four Texas Instrument Modules (TIMs). The demodulator is implemented in a single TIM that combines a C6416T DSP running at 1GHz along with a Virtex-II Pro (XC2VP30) FPGA.

As shown in Fig. 9, the demodulator's TIM is interconnected via dedicated high-speed data and control links with the digital down-converter (DDC) unit, which feeds the input to the demodulator, and with the forward error correction (FEC) unit, which receives the output bit stream. The interconnection links are implemented in the FPGA. The development of the demodulator's subunits is based on a multi-thread DSP implementation, where the various signal processing algorithms are organized and executed into different threads.

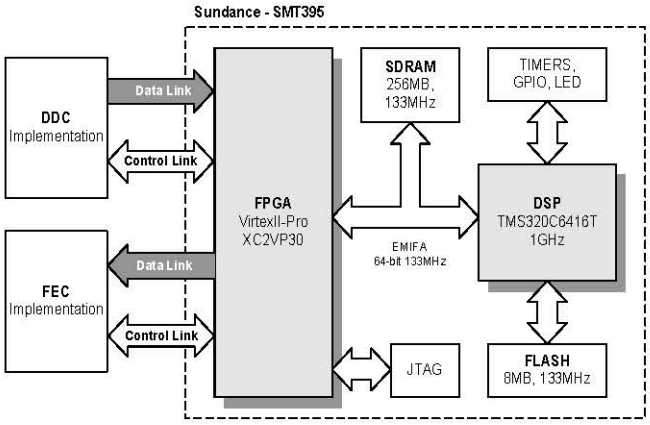


Fig. 9 Architecture of the demodulator's TIM development module

Mapping of Demodulator Subunits into Threads

Fig. 10 shows the structure of the demodulator's threadbased implementation. The various signal processing units are divided into two threads. The first thread is fed with the complex I/Q samples derived from the DDC unit, which is located at a different TIM, and implements part of the demodulator's signal processing chain. The second thread completes the demodulation process and drives the output bitstream to another TIM that implements the FEC operations of the DVB-S2 receiver. The two threads are controlled by an appropriate interrupt handler associated with a DSP timer whose frequency is proportional to the sampling rate of the input signal.

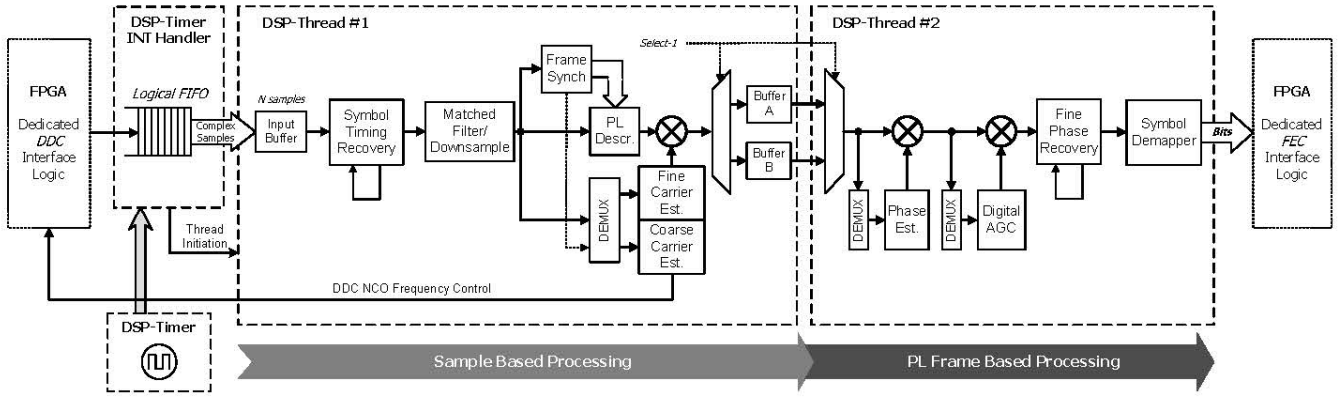


Fig. 10 Software thread architecture of the DVB-S2 demodulator

As shown in Fig. 10, the DDC input samples are transferred to the demodulator's TIM via a dedicated interface logic. The interrupt handler holds a logical FIFO that stores the Incoming samples. Using a frequency of twice the nominal symbol rate, in order to account for the STR mechanism (the Gardner detector needs 2 samples/symbol), the interrupt handler reads a block of N samples and then invokes the first thread by signalling a specific semaphore.

The first thread consists of the synchronization mechanisms that recover the actual symbol rate (STR), identify the start of a each new frame (PL framer) and compensate the carrier frequency offset errors (coarse and a fine CFR).

These procedures are executed on a block of N samples that has been transferred from the logical FIFO to a dedicated input buffer, which is directly accessible by the various threads. The output of the first thread is enabled as long as the underlying synchronization stages have converged. A two output buffer strategy is used in order to preserve real-time operation. These buffers are named A and B in Fig. 10. The size of each buffer equals to the size of a PLFRAME. When a complete PLFRAME has been written into buffer A, the second thread is initiated via a dedicated semaphore for processing the stored samples. At the same time, the first thread stores the compensated samples of the next PLFRAME into buffer B. The interrupt handler provides efficient synchronization between the two threads in order to preserve real-time functionality.

The second thread, whose activation is frame-based, implements carrier phase recovery, automatic gain control and demapping. Carrier phase is recovered using two separate steps: a coarse step that is adequate for single ring constellations (QPSK and 8PSK) and a fine step, which is necessary for two and three ring constellations (16APSK and 32APSK). The automatic gain control mechanism is embedded between the two steps of the phase recovery, while the demapper comprises the last processing stage of the demodulator. The output of the second thread is the decoded bitstream that feeds the FEC unit of the DVB-S2 receiver.

In order to support the different modes of the DVB-S2 signal (see Table I), it is important that the first thread is able to complete the processing of each block of N samples between two successive interrupt signals, even when most of its processing stages are active. This requirement imposes that the first thread is called immediately after the interrupt, while the second thread is paused periodically by the interrupt handler and resumed after the completion of the first thread.

Demodulator Operational Modes and Threads Execution 1(

The presented SDR demodulator has three modes of operation.

The first mode is called initial acquisition and is the initial mode after power-up. In this mode, the demodulator attempts to recover the symbol rate, as well as to determine the start of the PLFRAME. Therefore, during this mode only the STR and PL framer stages are executed in the first thread, while the second thread remains inactive. The operations during this mode are triggered by the timer-based interrupt handler, which signals the availability of a new block of N samples.

After the STR and PL framer subunits converge, the operational mode of the demodulator is switched to the second mode, which is called frequency acquisition. During this mode, the descrambling and carrier frequency recovery stages are also executed in the first thread, while the second thread remains inactive. In addition, the PL framer functions during this mode are reduced. The differential PL header detector is enabled only in a window of M symbols before and after the expected reception of the next frame header. This results in significant savings on CPU resources, which can be devoted to other functions. During this mode, the descrambler is enabled in order to generate the unscrambled symbol sequence. The descrambler operates on a complete PLFRAME excluding the frame header. The coarse frequency recovery mechanism is also enabled and drives the frequency control input of the DDC's NCO. The NCO is only updated whenever a pilot field is present. When the coarse recovery subunit converges, its processing is paused and the fine compensation algorithm is enabled. The latter is also pilot-based and is executed during the pilot fields. The operations during this mode are triggered by the timer-based interrupt handler, as soon as a new block of N input samples is available. The flowchart for the initial acquisition and frequency acquisition modes is shown in Fig. 11-(a).

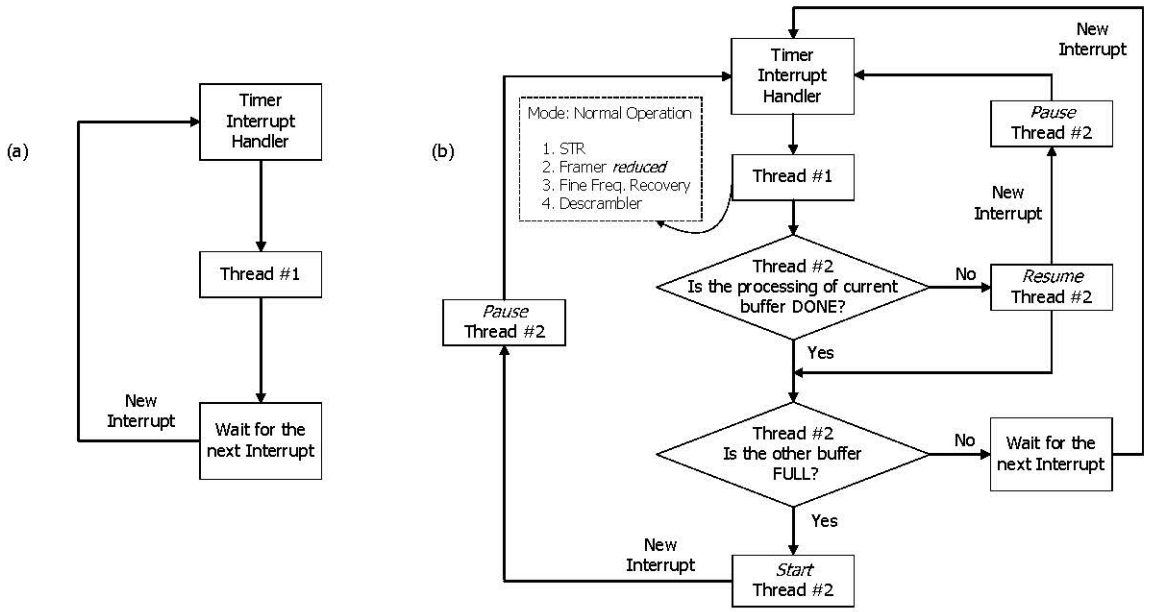


Fig. 11 Execution of threads according to the demodulator's mode of operation: (a) initial acquisition and frequency acquisition, (b) normal operation.

When the fine frequency recovery subunit converges, the demodulator's mode changes to normal operation. During this mode, we consider that all synchronization circuits of the first thread have converged and most of the errors have been compensated. Therefore, the first thread stores the recovered frames at the output buffers A or B and enables the second thread in order to process the data. During this mode the STR, the PL framer, the carrier frequency recovery and the output buffer writing subunits of the first thread are enabled along with all circuits of the second thread. The flowchart of the normal operation mode is depicted in Fig. 11-(b).

A critical restriction that affects the performance of the presented multi-thread DSP implementation is related with the total processing time of all threads that should not exceed the total duration of the transmission of a complete PLFRAME.

The mapping of the demodulator's subunits as well as the dynamic scheduling of the various DSP circuits according to the operational modes described in this Section ensure that the processing of all subsequent frames is performed in real-time.

Table II gives the duration of the normal DVB-S2 frame, as well as the duration of one data slot (90 symbols) and one pilot field (36 symbols) for 1MBaud symbol rate and for all constellation formats.

TABLE II DURATION OF normal PLFRAME WITH PILOT FIELDS FOR 1MBAUD SYMBOL RATE

η_{MOD}	Total PLFRAME (msec)	Data Slot (μsec)	Pilot Field (μsec)
QPSK: 2	33.282	90	36
8PSK: 3	22.194	90	36
16APSK: 4	16.686	90	36
32APSK: 5	13.338	90	36

Source File Description

hdl

Library & Module List

DVB-S2X MODEM HDL Top Level descriptions used for FPGA (or ASIC) implementation. Includes unit test definitions.

This folder contains the HDL description of the modem with associated tests.

APSK Modulator

APSK (Amplitude Phase Shift Keying) Modulator RTL Module

A generic APSK modulator engine, supporting one to eight bits per sample. Designed to form part of a DVB-S2X transmitter.

The design currently instantiates Xilinx primitive macros although these could be easily changed to another architecture (FPGA or ASIC).

FIR Filter
FIR Filter RTL Module

A FIR filter engine. Designed to form part of a DVB-S2X transmitter.

Lookup Table
Lookup Table RTL Module

A lookup implementation which is essentially a wrapper around a Xilinx RAMB18E1 macro. Designed to form part of a DVB-S2X transmitter.

lookup_table_behavioural
Lookup Table RTL Module

A lookup implementation which is essentially a wrapper around a Xilinx RAMB18E1 macro. Designed to form part of a DVB-S2X transmitter.

Multiply Accumulate
Multiply Accumulate RTL Module

A multiply accumulate (MAC) implementation which is essentially a wrapper around a Xilinx DSP48E1 macro. Designed to form part of a DVB-S2X transmitter.

multiply_accumulate_behavioural
Multiply Accumulate RTL Module

A multiply accumulate (MAC) implementation which mirrors the behavior of the DSP48E1 Multiply Accumulat module but implemented purely in behavioral Verilog. Designed to form part of a DVB-S2X transmitter.

- [Polyphase Filter](library/polyphase_filter)
Polyphase Filter RTL Module

A polyphase filter engine to perform filtered rate change in an efficient manner. Designed to form part of a DVB-S2X transmitter.

Testing

All modules use the [CocoTB](https://github.com/cocotb/cocotb) library for high level test bench creation. Each module has unit tests to perform regression testing following changes.

Setup

System Installs

Install the required simulation tools on a Ubuntu/Debian distribution:

CocoTB Installation

python

A collection of Python code which is used to model, simulate and verify the modem implementation.

Algorithm

Scripts used for algorithm development

Library

A number of library files which are used across the modem design for modelling and verification. Notable files include:

- [DVB-S2X Constellation Generator](library/generate_dvb-s2x_constellations.py)
- [DVB-S2X Constellation Definition](library/DVB-S2X_constellations.json)
- [Generic Modulator](library/generic_modem.py)

cocotb

Additional or modified CocoTB drivers used during HDL verification.

rfnoc-modem

Integrating UHD and fpga files into one directory

Based on copy block - Bypassing input into output

Testing

PROTOTYPING TESTBED 14

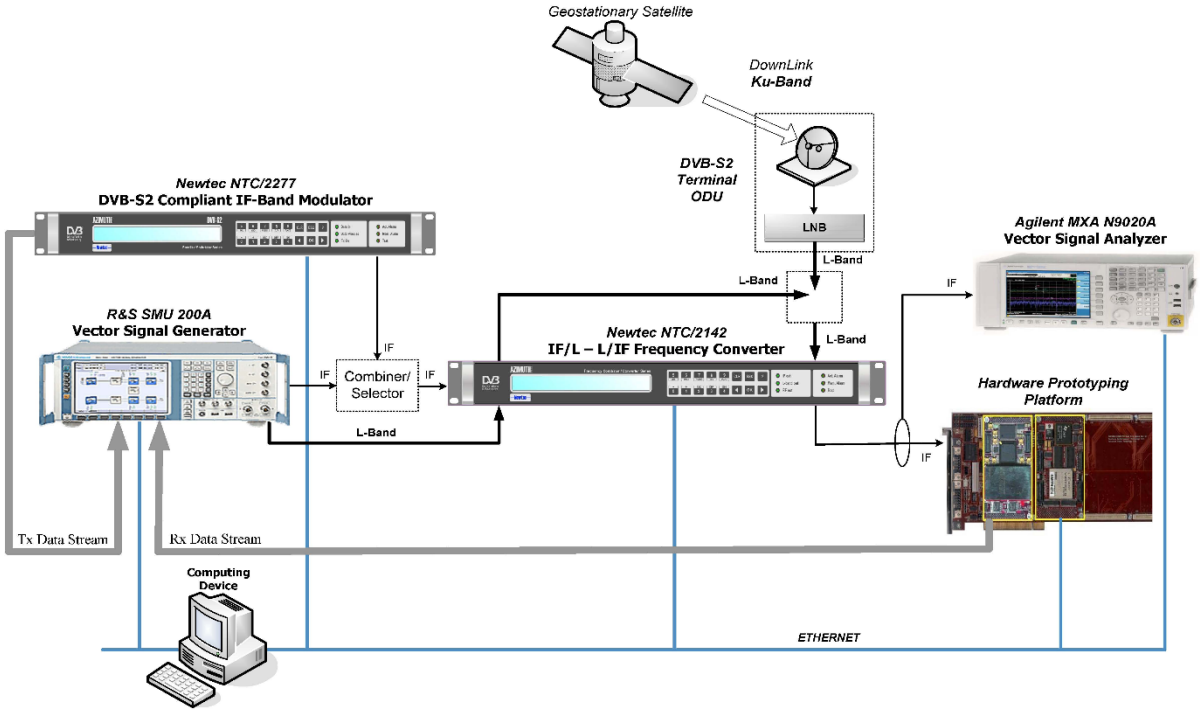
The figure below shows the prototyping testbed, used for the development, testing and demonstration of the DVB-S2

demodulator.

It consists of a versatile laboratory setup based on commercially available equipment and custom devices that enable the measurement and analysis of the DVB-S2 receiver functionality and performance under different signal conditions and operating modes. In particular, the setup consists of a set of DVB-S2 compliant signal generators, programmable up and down frequency conversion units, a noise injection prototyping platform and a host computing environment for visualization of measurements, diagnostics and signal statistics using a custom MATLAB-based application.

The DVB-S2 signal generator consists of a NEWTEC NTC2277 IF modulator at 70 MHz and an IP host traffic generator. System parameters such as baud rate, modulation and coding modes, roll-off factor and transmit power are user selectable. DVB-S2 signal generation can also be performed by Vector Signal Generators (VSG). The programmable frequency conversion unit (FCU) supports multiple signal paths, with independent L-band to IF and IF to L-band conversion modules, thus allowing the addition of various signal impairments at different signal processing stages. The FCU along with the VSG provides various signal distortion options, including white and colored Gaussian noise and RF interference.

Additionally, the FCU can also be interfaced with an outdoor unit with a LNB that provides L-band signal under realistic conditions. and multi-channel fading conditions emulator, the hardware



The DVB-S2 receiver testbed

Integration Guide

See INTEGRATION GUIDE.pdf

Developer

Mark Chen
Angelia Technology / ICTech
http://www.angelia.eu.org

License

See “License Agreement”.