Hardware Verification and Artificial Intelligence

I started designing ICs since 2013. My current design focuses on hardware verification, particularly verification with UVM, OSVVM, UVVM, cocotb, ABV (SVA, PSL).

My another activity in this area is the application of Artificial Intelligence and Machine Learning to hardware verification with my current focus on Neural Networks. At the moment I am going to write and publish some works in the following direction: *** Artificial Neural Network for Test Generation Optimization in Hardware Verification ***

This is one of the key areas of concerns for the verification engineers.

I have been involving in AI well since 2013, when I was studying the graph-theoretical aspects of IC (integrated circuits) design, where AI is also key to developing EDA algorithms for VLSI design. A couple of years ago my IC verification activities have also been involving lots of AI/ML techniques and algorithms, as well as my quantum circuits design for example qubit routing which employs deep reinforcement learning to improve the routing efficiency.

However, my IC career has been undergoing a long path, telling the whole story is not the purpose of this introductory message. However, I can simply summarize them in the following:

As fa as design is considered, I have been concentrated on design and verification of ICs and IP cores for wireless communications (modulation and demodulation) during 2018-2022, particularly for satellite broadband Internet.

As far as authoring is concerned, I have been authoring a huge volume of books containing all aspects of the verification processes - from methodologies to languages, from platforms to testing systems. My first book in this direction was related to verification languages with Python, and afterwards SystemC, VHDL, (System)Verilog and a bunch of other verification languages.; then come the verification methodologies - UVM, UVVM, OSVVM, OVM etc.

I used also to write the gigantic book series titled "Silicon IP – Not just Design".

Other books I have drafted include the following:

Protecting Your IP Cores
Review of Verification IP & IP Core Verification – An Abstract
Verification Methodologies - A Concise Introduction
Comprehensive Review of Hardware Verification Languages (Except Python)
Hardware Verification Planning - A Concise Introduction
Hardware Verification Planning Tools
Hardware Verification in Python

So far as web development is considered, I used to put huge efforts in developing a web portal about IP core development, but now this site is reoriented to be my personal site with my information about hardware verification, see www.ipcoredesign.net for reference.

Considering my earlier researches, apart from my researches many years ago, which you may find in my CV or my personal site, I can cite the one that is the mathematics for development and design of quantum computer (particularly Artificial Intelligence (Machine Learning and others) & heuristics). I started from qubit routing with a comprehensive review of that area together with an indepth study of a specific topic, one no one has tried sofar. I have initiated the writing of the following articles but stopped 2 or 3 years ago:

- 1) Math (Al & Heuristics) for Qubit Routing A Survey
- 2) Qubit Routing with Machine Learning (Reinforcement Learning etc)

This research and writing was just the start of my huge research and writing plan in the quantum area. In fact, I have done a number of researches on quantum computer before, notably on graph theoretical applications for quantum circuits design, in line with the D-Wave quantum computer developed by a Canadian company a couple of years ago. I don't know what is its status now, because since 2016 my quantum research is stopped.

Websites:

Angelia Technologies / IPCore Design, hardware verification with Artificial Intelligence https://www.ipcoredesign.net
Plutus Business Consultants (PBC) - Artificial Intelligence for Health, my current business focus https://www.plutus.eu.org
Github
https://github.com/worldsoft998
Personal
http://markchen.int.eu.org/