PC104 pin layout for Kletskous

1	I01/RX SREAD	2	IO2	3	IO3	4	IO4/ RX TxRxDATA
5	IO5/RX SDATA	6	IO6/RX CE	7	IO7/RX SWD	8	IO8/RX SLC
9	IO9/RX SCLK	10	IO10	11	EPS_EOC	12	IO12/RX TxRxCLK
13	IO13/EPS SPI CLK	14	IO14/EPS SPI MISO	15	IO15/EPS SPI MOSI	16	IO16/EPS SPI CS
17	SDA3	18	SCL3	19	IO17	20	IO18
21	IO_11	22	IO20	23	IO21	24	IO22
25	IO23/TX CE	26	IO24	27	IO25	28	IO26
29	IO27TX SWD	30	IO28	31	IO29	32	IO30
33	IO31TX SLE	34	IO32	35	IO33	36	IO34
37	IO35/TX SREAD	38	IO36	39	IO37	40	IO38
41	IO39/TX SDATA	42	IO40/TX TxRxDATA	43	IO41	44	ANT RELEASE
45	IO43/TX SCLK	46	IO44/TX TxRxCLK	47	+3V3	48	+3V3
49	RESERVED	50	IO45/BATT_OFF	51	+5V	52	+5V
53	RESERVED	54	IO46/CHG_INH	55	VCHARGE	56	VCHARGE
57	RESERVED	58	SDA2	59	ANL_GND	60	ANL_GND
61	RESERVED	62	+5V USB	63	DIG_GND	64	DIG_GND
65	SCL2	66	IO47	67	S1_COMM	68	S1_COMM
69	IO48	70	IO49	71	S1_NO	72	S1_NO
73	IO50	74	IO51	75	S1_NC	76	S1_NC
77	VBAT_SWITCH_EN	78	IO53	79	S2_COMM	80	S2_COMM
81	SDA1	82	VBACKUP	83	S2_NO	84	S2_NO
85	SCL1	86	RESERVED	87	S2_NC	88	S2_NC
89	VBAT_SWITCH	90	VBAT_SWITCH	91	VBATTERY	92	VBATTERY
93	USER0	94	USER1	95	USER6	96	USER7
97	USER2	98	USER3	99	USER8	100	USER9
101	USER4	102	USER5	103	USER10	104	USER11

PIN	Description	Assigned	Direction
SDA3, SCL3	I_2C bus 3	NO	IO
SDA2, SCL2	I_2C bus 2	N0	IO
SDA1, SCL1	I_2C bus 1	YES BY RTCC	IO
VCHARGE	External DC connector to charge batteries	YES BY EPS	INPUT
+5V USB	+5V available when connected to USB	NO	INPUT
VBACKUP	From 3V lithium cell used by RTCC	RTCC	OUTPUT
VBATTERY	Battery voltage output	EPS	OUTPUT
VBAT_SWITCH	Switched battery voltage output	EPS	OUTPUT
VBAT_SWITCH_EN	Switched battery voltage control	EPS	INPUT
+5V	+5V Supply from ESP	EPS	OUTPUT
+3V3	+3V3 Supply from EPS	EPS	OUTPUT
ANL_GND	All analogue ground returns	ALL	INPUT
DIG_GND	All digital ground returns	ALL	INPUT
S1_NC	Release before flight Normally Closed contact	EPS	IO
S1_NO	Release before flight Normally Open contact	EPS	IO
S1_COMM	Release before flight Normally Common contact	EPS	IO
S2_NC	Deployment switch Normally Closed contact EPS	EPS	IO
S2_NO	Deployment switch Normally Open contact	EPS	IO
S2_COMM	Deployment switch Normally Common contact	EPS	IO
I01/RX SREAD	Receiver Serial Data Out	RADIO	OUTPUT
IO4/ RX TxRxDATA	Receiver Data Input Output	RADIO	IO
IO5/RX SDATA	Receiver Serial Data Input	RADIO	INPUT
IO6/RX CE	Receiver Chip Enable	RADIO	INPUT
IO7/RX SWD	Receiver Sync Word Detect	RADIO	OUTPUT

PIN	Description	Assigned	Direction
IO8/RX SLE	Receiver Serial Load Enable	RADIO	INPUT
IO9/RX SCLK	Receiver Serial Clock Input	RADIO	INPUT
IO12/RX TxRxCLK	Receiver Data Clock	RADIO	OUTPUT
IO13/EPS_SPI_CLK	EPS SPI Clock	EPS	INPUT
IO14/EPS_MISO	EPS SPI Master in Slave out	EPS	OUTPUT
IO15/EPS_MOSI	EPS SPI Master out Slave in	EPS	INPUT
IO16/EPS_CS	EPS SPI Chip Select	EPS	INPUT
ANT RELEASE	Antenna Release	EPS	INPUT
EPS_EOC	EPS End of Conversion	EPS	OUTPUT
IO23/TX CE	Transmitter Chip Enable	RADIO	INPUT
IO27TX SWD	Transmitter Sync Word Detect	RADIO	OUTPUT
IO31TX SLE	Transmitter Serial Load Enable	RADIO	INPUT
IO35/TX SREAD	Transmitter Serial Data Out	RADIO	OUTPUT
IO39/TX SDATA	Transmitter Serial Data Input	RADIO	INPUT
IO40/TX TxRxDATA	Transmitter Data Input Output	RADIO	IO
IO43/TX SCLK	Transmitter Serial Clock Input	RADIO	INPUT
IO44/TX TxRxCLK	Transmitter Data Clock	RADIO	OUTPUT
IO45/BATT_OFF	Disconnect Battery Output	EPS	INPUT
IO46/CHG_INH	Disconnect Battery Charger	EPS	INPUT
CPU_HEART	CPU Heartbeat	CPU	OUTPUT
IOxx	Digital Input or Output	NO	IO
RESERVED	Reserved for use by CPU	CPU	IO
USER0-11	User defined IO not connected to CPU	NO	IO

NOTES:

1. CPU_HEART
   2Hz output from the CPU to indicate that the CPU is running. If this line goes permanently high or low thereis a problem with the CPU and the other systems must take over as fail safe.

2. VBACKUP
   +3V Output from the RTCC backup battery.

3. IOxx
   Inputs, Outputs and Analogue inputs available to other system components. Pins will be assigned as requiredby other system builders.