

# Project 1 Report

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## 1 Results

### 1.1 Number of fetched instructions

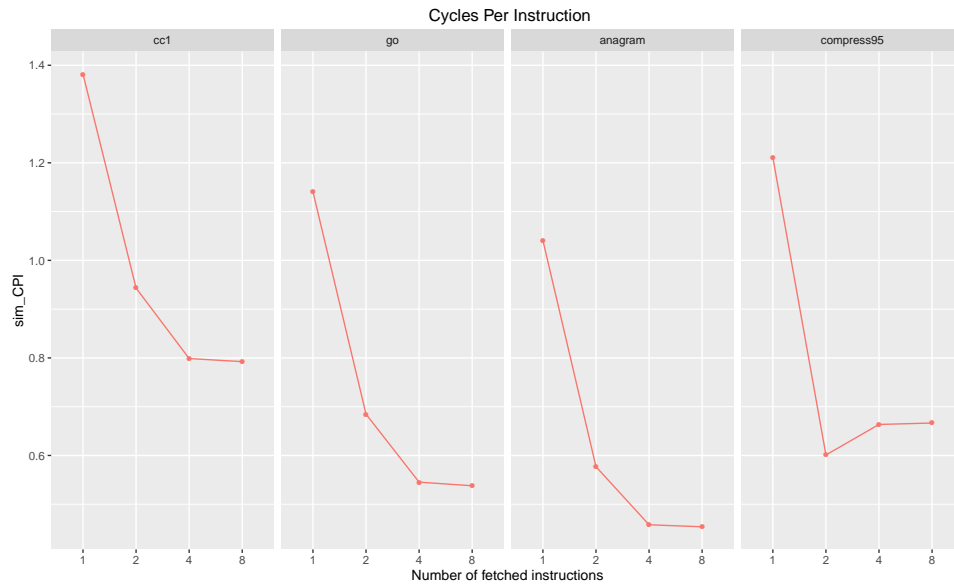


Figure 1: Cycles per instructions vs number of fetched instructions.

### 1.2 Number of decoded instructions

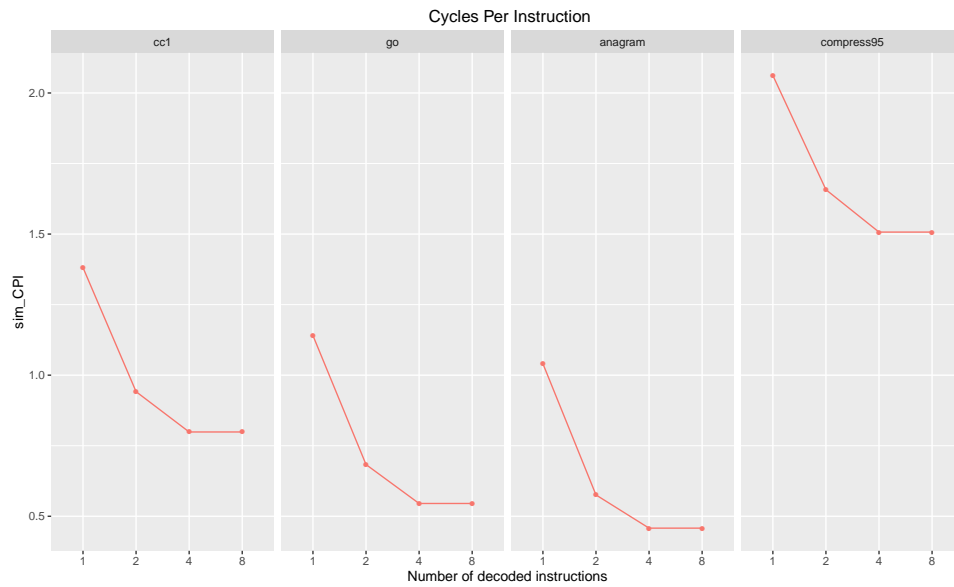


Figure 2: Cycles per instructions vs number of decoded instructions.

### 1.3 Number of issued instructions



Figure 3: Cycles per instructions vs number of issued instructions.

### 1.4 Number of committed instructions

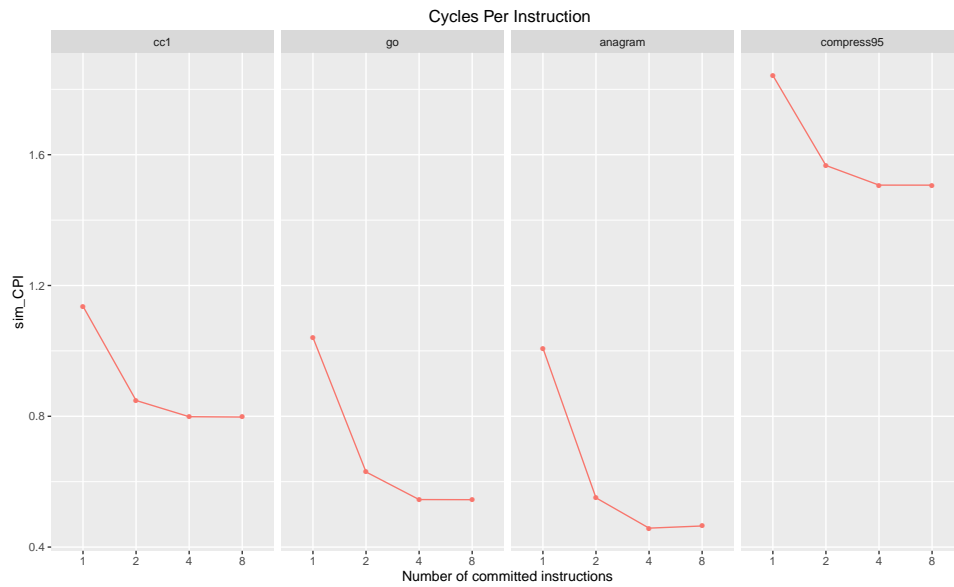


Figure 4: Cycles per instructions vs number of committed instructions.

## 1.5 Branch prediction

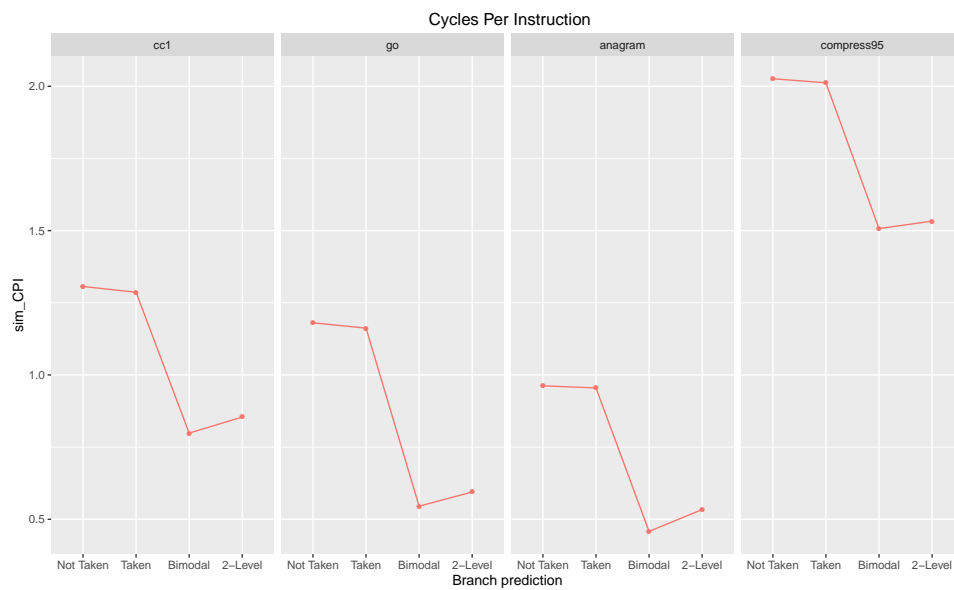


Figure 5: Cycles per instructions vs branch prediction methods.

## 1.6 Cache block size



Figure 6: Cycles per instructions vs branch prediction methods.

## 1.7 Cache replacement policy

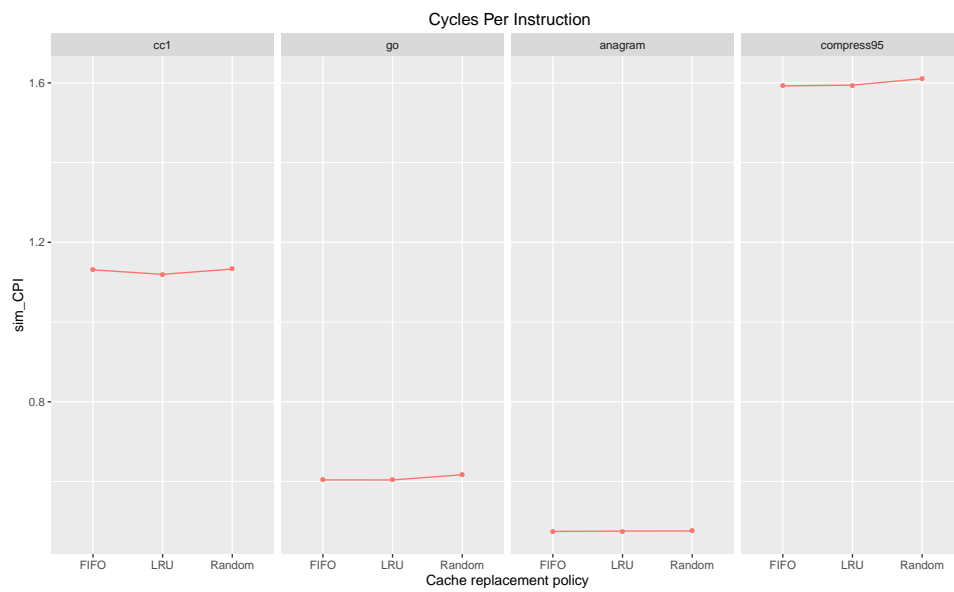


Figure 7: Cycles per instructions vs branch prediction methods.

## 1.8 Cache associativity

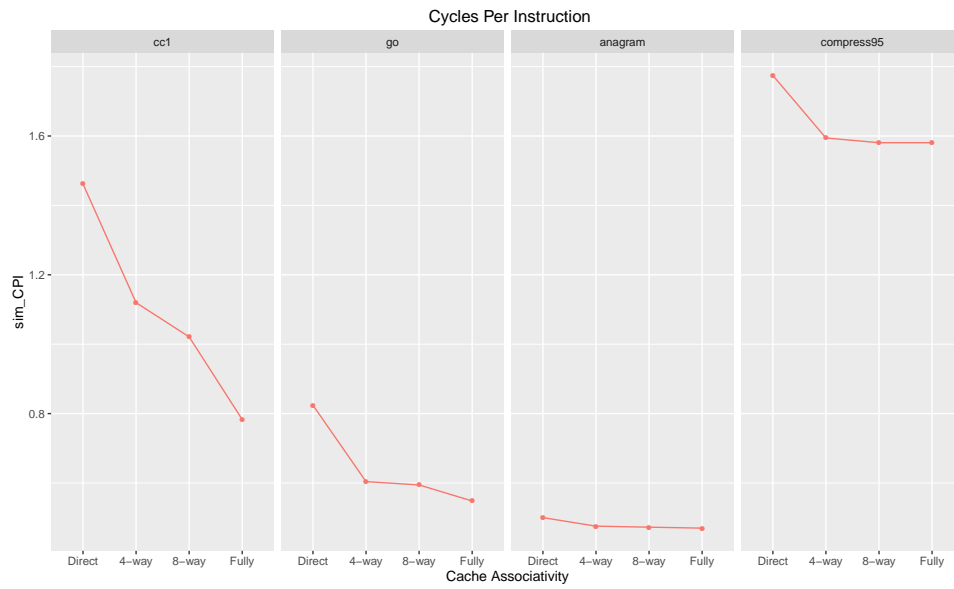


Figure 8: Cycles per instructions vs branch prediction methods.

## 2 Discussion

### 3 Commands

```

1  #!/bin/bash
2  # Number of instructions fetched...
3  ./sim-outorder -fetch:ifqsize 1 ../benchmarks/cc1.alpha 2> Results/results_F1.txt
4  ./sim-outorder -fetch:ifqsize 2 ../benchmarks/cc1.alpha 2> Results/results_F2.txt
5  ./sim-outorder -fetch:ifqsize 4 ../benchmarks/cc1.alpha 2> Results/results_F4.txt
6  ./sim-outorder -fetch:ifqsize 8 ../benchmarks/cc1.alpha 2> Results/results_F8.txt
7
8  # Number of instructions decoded...
9  ./sim-outorder -decode:width 1 ../benchmarks/cc1.alpha 2> Results/results_D1.txt
10 ./sim-outorder -decode:width 2 ../benchmarks/cc1.alpha 2> Results/results_D2.txt
11 ./sim-outorder -decode:width 4 ../benchmarks/cc1.alpha 2> Results/results_D4.txt
12 ./sim-outorder -decode:width 8 ../benchmarks/cc1.alpha 2> Results/results_D8.txt
13
14 # Number of instructions issued...
15 ./sim-outorder -issue:width 1 ../benchmarks/cc1.alpha 2> Results/results_I1.txt
16 ./sim-outorder -issue:width 2 ../benchmarks/cc1.alpha 2> Results/results_I2.txt
17 ./sim-outorder -issue:width 4 ../benchmarks/cc1.alpha 2> Results/results_I4.txt
18 ./sim-outorder -issue:width 8 ../benchmarks/cc1.alpha 2> Results/results_I8.txt
19
20 # Number of instructions committed...
21 ./sim-outorder -commit:width 1 ../benchmarks/cc1.alpha 2> Results/results_C1.txt
22 ./sim-outorder -commit:width 2 ../benchmarks/cc1.alpha 2> Results/results_C2.txt
23 ./sim-outorder -commit:width 4 ../benchmarks/cc1.alpha 2> Results/results_C4.txt
24 ./sim-outorder -commit:width 8 ../benchmarks/cc1.alpha 2> Results/results_C8.txt
25
26 # Branch prediction...
27 ./sim-outorder -bpred nottaken ../benchmarks/cc1.alpha 2> Results/results_BPNT.txt
28 ./sim-outorder -bpred taken ../benchmarks/cc1.alpha 2> Results/results_BPT.txt
29 ./sim-outorder -bpred bimod ../benchmarks/cc1.alpha 2> Results/results_BPM.txt
30 ./sim-outorder -bpred 2lev ../benchmarks/cc1.alpha 2> Results/results_BP2L.txt
31
32 # Cache block size...
33 ./sim-outorder -cache:d12 u12:128:32:4:1 ../benchmarks/cc1.alpha 2> Results/results_CacheBS32.txt
34 ./sim-outorder -cache:d12 u12:128:64:4:1 ../benchmarks/cc1.alpha 2> Results/results_CacheBS64.txt
35 ./sim-outorder -cache:d12 u12:128:128:4:1 ../benchmarks/cc1.alpha 2> Results/results_CacheBS128.txt
36 ./sim-outorder -cache:d12 u12:128:256:4:1 ../benchmarks/cc1.alpha 2> Results/results_CacheBS256.txt
37
38 # Cache replacement policy...
39 ./sim-outorder -cache:d12 u12:128:32:4:f ../benchmarks/cc1.alpha 2> Results/results_CacheRPF.txt
40 ./sim-outorder -cache:d12 u12:128:32:4:l ../benchmarks/cc1.alpha 2> Results/results_CacheRPL.txt
41 ./sim-outorder -cache:d12 u12:128:32:4:r ../benchmarks/cc1.alpha 2> Results/results_CacheRPR.txt
42
43 # Cache associativity...
44 ./sim-outorder -cache:d12 u12:128:32:1:1 ../benchmarks/cc1.alpha 2> Results/results_CacheA1.txt
45 ./sim-outorder -cache:d12 u12:128:32:4:1 ../benchmarks/cc1.alpha 2> Results/results_CacheA4.txt
46 ./sim-outorder -cache:d12 u12:128:32:8:1 ../benchmarks/cc1.alpha 2> Results/results_CacheA8.txt
47 ./sim-outorder -cache:d12 u12:128:32:64:1 ../benchmarks/cc1.alpha 2> Results/results_CacheA64.txt

```

Listing 1: Simulation execution commands for *cc1* application.

```

1  #!/bin/bash
2  # Number of instructions fetched...
3  ./sim-outorder -fetch:ifqsize 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F1.txt
4  ./sim-outorder -fetch:ifqsize 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F2.txt
5  ./sim-outorder -fetch:ifqsize 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F4.txt
6  ./sim-outorder -fetch:ifqsize 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F8.txt
7
8  # Number of instructions decoded...
9  ./sim-outorder -decode:width 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D1.txt
10 ./sim-outorder -decode:width 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D2.txt
11 ./sim-outorder -decode:width 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D4.txt
12 ./sim-outorder -decode:width 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D8.txt
13
14 # Number of instructions issued...
15 ./sim-outorder -issue:width 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I1.txt
16 ./sim-outorder -issue:width 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I2.txt
17 ./sim-outorder -issue:width 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I4.txt
18 ./sim-outorder -issue:width 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I8.txt
19
20 # Number of instructions committed...
21 ./sim-outorder -commit:width 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C1.txt
22 ./sim-outorder -commit:width 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C2.txt
23 ./sim-outorder -commit:width 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C4.txt
24 ./sim-outorder -commit:width 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C8.txt
25
26 # Branch prediction...
27 ./sim-outorder -bpred nottaken ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BPNT.txt
28 ./sim-outorder -bpred taken ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BPT.txt
29 ./sim-outorder -bpred bimod ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BPBM.txt
30 ./sim-outorder -bpred 2lev ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BP2L.txt
31
32 # Cache block size...
33 ./sim-outorder -cache:d12 ul2:128:32:4:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS32.txt
34 ./sim-outorder -cache:d12 ul2:128:64:4:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS64.txt
35 ./sim-outorder -cache:d12 ul2:128:128:4:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS128.txt
36 ./sim-outorder -cache:d12 ul2:128:256:4:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS256.txt
37
38 # Cache replacement policy...
39 ./sim-outorder -cache:d12 ul2:128:32:4:f ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheRPF.txt
40 ./sim-outorder -cache:d12 ul2:128:32:4:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheRPL.txt
41 ./sim-outorder -cache:d12 ul2:128:32:4:r ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheRPR.txt
42
43 # Cache associativity...
44 ./sim-outorder -cache:d12 ul2:128:32:1:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA1.txt
45 ./sim-outorder -cache:d12 ul2:128:32:4:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA4.txt
46 ./sim-outorder -cache:d12 ul2:128:32:8:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA8.txt
47 ./sim-outorder -cache:d12 ul2:128:32:64:1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA64.txt

```

Listing 2: Simulation execution commands for *anagram* application.



```

1  #!/bin/bash
2  # Number of instructions fetched...
3  ./sim-outorder -fetch:ifqsize 1 ../benchmarks/compress95.alpha 2> Results/results_C_F1.txt
4  ./sim-outorder -fetch:ifqsize 2 ../benchmarks/compress95.alpha 2> Results/results_C_F2.txt
5  ./sim-outorder -fetch:ifqsize 4 ../benchmarks/compress95.alpha 2> Results/results_C_F4.txt
6  ./sim-outorder -fetch:ifqsize 8 ../benchmarks/compress95.alpha 2> Results/results_C_F8.txt
7
8  # Number of instructions decoded...
9  ./sim-outorder -decode:width 1 ../benchmarks/compress95.alpha 2> Results/results_C_D1.txt
10 ./sim-outorder -decode:width 2 ../benchmarks/compress95.alpha 2> Results/results_C_D2.txt
11 ./sim-outorder -decode:width 4 ../benchmarks/compress95.alpha 2> Results/results_C_D4.txt
12 ./sim-outorder -decode:width 8 ../benchmarks/compress95.alpha 2> Results/results_C_D8.txt
13
14 # Number of instructions issued...
15 ./sim-outorder -issue:width 1 ../benchmarks/compress95.alpha 2> Results/results_C_I1.txt
16 ./sim-outorder -issue:width 2 ../benchmarks/compress95.alpha 2> Results/results_C_I2.txt
17 ./sim-outorder -issue:width 4 ../benchmarks/compress95.alpha 2> Results/results_C_I4.txt
18 ./sim-outorder -issue:width 8 ../benchmarks/compress95.alpha 2> Results/results_C_I8.txt
19
20 # Number of instructions committed...
21 ./sim-outorder -commit:width 1 ../benchmarks/compress95.alpha 2> Results/results_C_C1.txt
22 ./sim-outorder -commit:width 2 ../benchmarks/compress95.alpha 2> Results/results_C_C2.txt
23 ./sim-outorder -commit:width 4 ../benchmarks/compress95.alpha 2> Results/results_C_C4.txt
24 ./sim-outorder -commit:width 8 ../benchmarks/compress95.alpha 2> Results/results_C_C8.txt
25
26 # Branch prediction...
27 ./sim-outorder -bpred nottaken ../benchmarks/compress95.alpha 2> Results/results_C_BPNT.txt
28 ./sim-outorder -bpred taken ../benchmarks/compress95.alpha 2> Results/results_C_BPT.txt
29 ./sim-outorder -bpred bimod ../benchmarks/compress95.alpha 2> Results/results_C_BPBM.txt
30 ./sim-outorder -bpred 2lev ../benchmarks/compress95.alpha 2> Results/results_C_BP2L.txt
31
32 # Cache block size...
33 ./sim-outorder -cache:d12 u12:128:32:4:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheBS32.txt
34 ./sim-outorder -cache:d12 u12:128:64:4:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheBS64.txt
35 ./sim-outorder -cache:d12 u12:128:128:4:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheBS128.txt
36 ./sim-outorder -cache:d12 u12:128:256:4:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheBS256.txt
37
38 # Cache replacement policy...
39 ./sim-outorder -cache:d12 u12:128:32:4:f ../benchmarks/compress95.alpha 2> Results/results_C_CacheRPF.txt
40 ./sim-outorder -cache:d12 u12:128:32:4:l ../benchmarks/compress95.alpha 2> Results/results_C_CacheRPL.txt
41 ./sim-outorder -cache:d12 u12:128:32:4:r ../benchmarks/compress95.alpha 2> Results/results_C_CacheRPR.txt
42
43 # Cache associativity...
44 ./sim-outorder -cache:d12 u12:128:32:1:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheA1.txt
45 ./sim-outorder -cache:d12 u12:128:32:4:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheA4.txt
46 ./sim-outorder -cache:d12 u12:128:32:8:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheA8.txt
47 ./sim-outorder -cache:d12 u12:128:32:64:1 ../benchmarks/compress95.alpha 2> Results/results_C_CacheA64.txt

```

Listing 3: Simulation execution commands for *compress95* application.

```

1  #!/bin/bash
2  # Number of instructions fetched...
3  ./sim-outorder -fetch:ifqsize 1 ../benchmarks/go.alpha 2> Results/results_G_F1.txt
4  ./sim-outorder -fetch:ifqsize 2 ../benchmarks/go.alpha 2> Results/results_G_F2.txt
5  ./sim-outorder -fetch:ifqsize 4 ../benchmarks/go.alpha 2> Results/results_G_F4.txt
6  ./sim-outorder -fetch:ifqsize 8 ../benchmarks/go.alpha 2> Results/results_G_F8.txt
7
8  # Number of instructions decoded...
9  ./sim-outorder -decode:width 1 ../benchmarks/go.alpha 2> Results/results_G_D1.txt
10 ./sim-outorder -decode:width 2 ../benchmarks/go.alpha 2> Results/results_G_D2.txt
11 ./sim-outorder -decode:width 4 ../benchmarks/go.alpha 2> Results/results_G_D4.txt
12 ./sim-outorder -decode:width 8 ../benchmarks/go.alpha 2> Results/results_G_D8.txt
13
14 # Number of instructions issued...
15 ./sim-outorder -issue:width 1 ../benchmarks/go.alpha 2> Results/results_G_I1.txt
16 ./sim-outorder -issue:width 2 ../benchmarks/go.alpha 2> Results/results_G_I2.txt
17 ./sim-outorder -issue:width 4 ../benchmarks/go.alpha 2> Results/results_G_I4.txt
18 ./sim-outorder -issue:width 8 ../benchmarks/go.alpha 2> Results/results_G_I8.txt
19
20 # Number of instructions committed...
21 ./sim-outorder -commit:width 1 ../benchmarks/go.alpha 2> Results/results_G_C1.txt
22 ./sim-outorder -commit:width 2 ../benchmarks/go.alpha 2> Results/results_G_C2.txt
23 ./sim-outorder -commit:width 4 ../benchmarks/go.alpha 2> Results/results_G_C4.txt
24 ./sim-outorder -commit:width 8 ../benchmarks/go.alpha 2> Results/results_G_C8.txt
25
26 # Branch prediction...
27 ./sim-outorder -bpred nottaken ../benchmarks/go.alpha 2> Results/results_G_BPNT.txt
28 ./sim-outorder -bpred taken ../benchmarks/go.alpha 2> Results/results_G_BPT.txt
29 ./sim-outorder -bpred bimod ../benchmarks/go.alpha 2> Results/results_G_BPBM.txt
30 ./sim-outorder -bpred 2lev ../benchmarks/go.alpha 2> Results/results_G_BP2L.txt
31
32 # Cache block size...
33 ./sim-outorder -cache:d12 ul2:128:32:4:1 ../benchmarks/go.alpha 2> Results/results_G_CacheBS32.txt
34 ./sim-outorder -cache:d12 ul2:128:64:4:1 ../benchmarks/go.alpha 2> Results/results_G_CacheBS64.txt
35 ./sim-outorder -cache:d12 ul2:128:128:4:1 ../benchmarks/go.alpha 2> Results/results_G_CacheBS128.txt
36 ./sim-outorder -cache:d12 ul2:128:256:4:1 ../benchmarks/go.alpha 2> Results/results_G_CacheBS256.txt
37
38 # Cache replacement policy...
39 ./sim-outorder -cache:d12 ul2:128:32:4:f ../benchmarks/go.alpha 2> Results/results_G_CacheRPF.txt
40 ./sim-outorder -cache:d12 ul2:128:32:4:l ../benchmarks/go.alpha 2> Results/results_G_CacheRPL.txt
41 ./sim-outorder -cache:d12 ul2:128:32:4:r ../benchmarks/go.alpha 2> Results/results_G_CacheRPR.txt
42
43 # Cache associativity...
44 ./sim-outorder -cache:d12 ul2:128:32:1:1 ../benchmarks/go.alpha 2> Results/results_G_CacheA1.txt
45 ./sim-outorder -cache:d12 ul2:128:32:4:1 ../benchmarks/go.alpha 2> Results/results_G_CacheA4.txt
46 ./sim-outorder -cache:d12 ul2:128:32:8:1 ../benchmarks/go.alpha 2> Results/results_G_CacheA8.txt
47 ./sim-outorder -cache:d12 ul2:128:32:64:1 ../benchmarks/go.alpha 2> Results/results_G_CacheA64.txt

```

Listing 4: Simulation execution commands for *go* application.