Critique Week 4

Andres Calderon - SID:861243796

February 1, 2016

Transactional Memory - Architecture Support for Lock-Free Data Structures (Herlihy and Moss, 1993)

The paper introduces transactional memory (TM), a novel multiprocessor architecture designed to address common problems of traditional locking techniques. It extends the cache coherence protocol by defining custom read-modify-write operations. One important goal of the authors was that TM should be at least as efficient and easy to use as previous methods.

There are three main problems in locking: priority inversion, convoying and deadlocks. TM attempts to address them by using transactions and a set of primitive instructions. A transaction is a finite sequence of machine instructions with two important properties: serializability and atomicity. In addition, TM provides primitive instructions for accessing memory (LX, LTX and ST) and manipulating transaction state (COMMIT, ABORT and VALIDATE). TM avoids the use of locks by using (1) LT or LTX to read, (2) VALIDATE to check consistency, (3) ST to modify, and (4) COMMIT to make the changes permanent.

The authors note that the concept of transaction is similar to the Database concept. However, the main difference is that a TM transaction is a short-lived activity. It should last less than a quantum and make few location accesses.

The paper provides an implementation by modifying standard multiprocessor cache coherence protocols. The basic idea is that the capabilities present in previous protocols to detect accessibility conflicts can also detect conflicts in transactions. They extend snoopy caches and network-based architectures. The authors stresses that in the case of snoopy caches, they use two exclusive caches to reduce the impact of non-transactional loads.

The paper presents three simulation scenarios. They provide the code and performance analysis for counting, producer/consumer and doubly-linked list benchmarks. TM is compared against two software mechanisms and two hardware mechanisms. Overall, TM outperforms the other methods in almost all the benchmarks.

In my opinion, the ideas presented in the paper are well supported and organized. Even though, the details in the implementation are highly technical, the notions given in the general approach suffice to get the big picture. It is quite interesting that the authors stress the limitations and possible solutions both during the implementation and the simulations. Providing the source code of the benchmarks is always a plus.