Project 1 Report

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1 Results

In the this section we present some results we found interesting using the commands show in section 3. Section 2 presents our discussion about these figures.

1.1 Number of fetched instructions

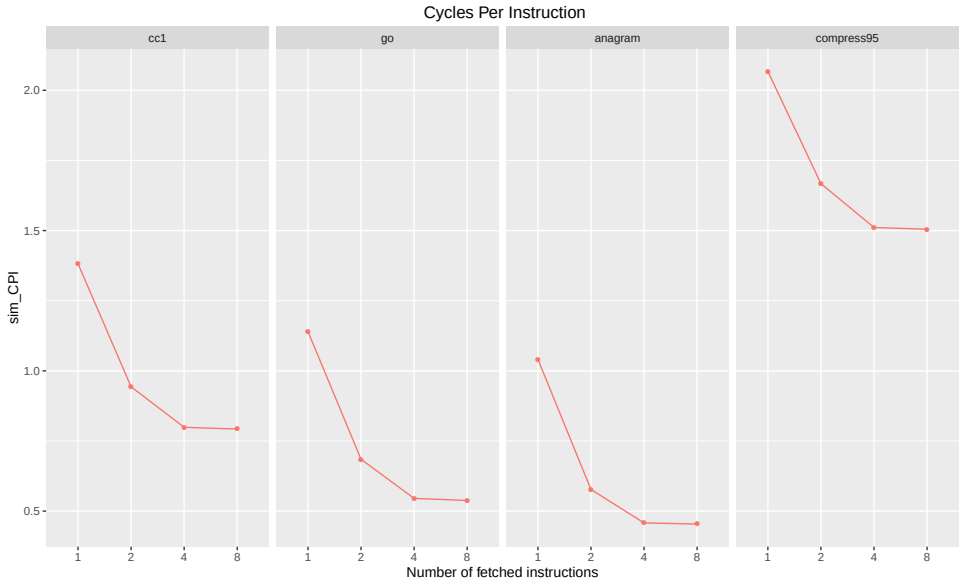

Figure 1: Cycles per instructions vs number of fetched instructions.

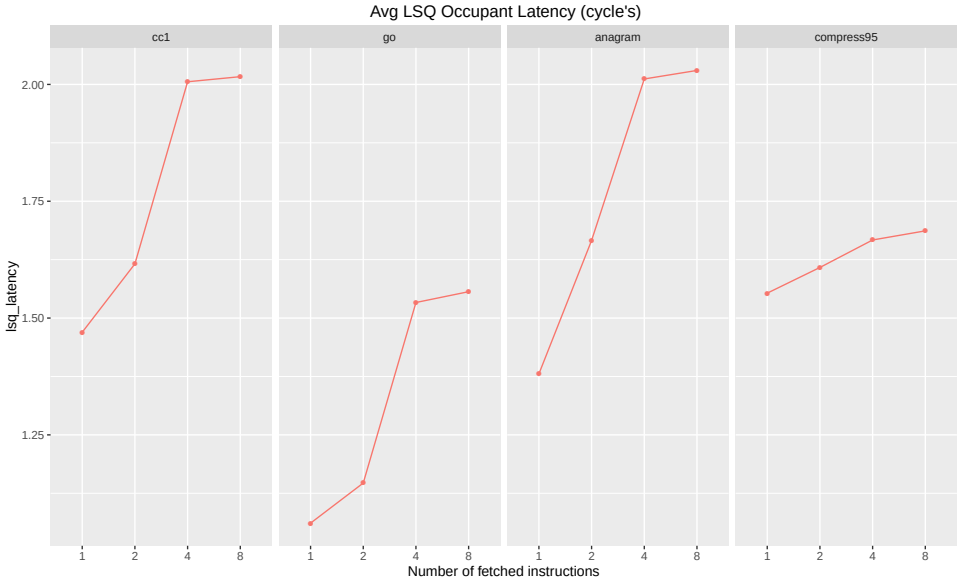

Figure 2: LSQ latency vs number of fetched instructions.

1.2 Number of decoded instructions

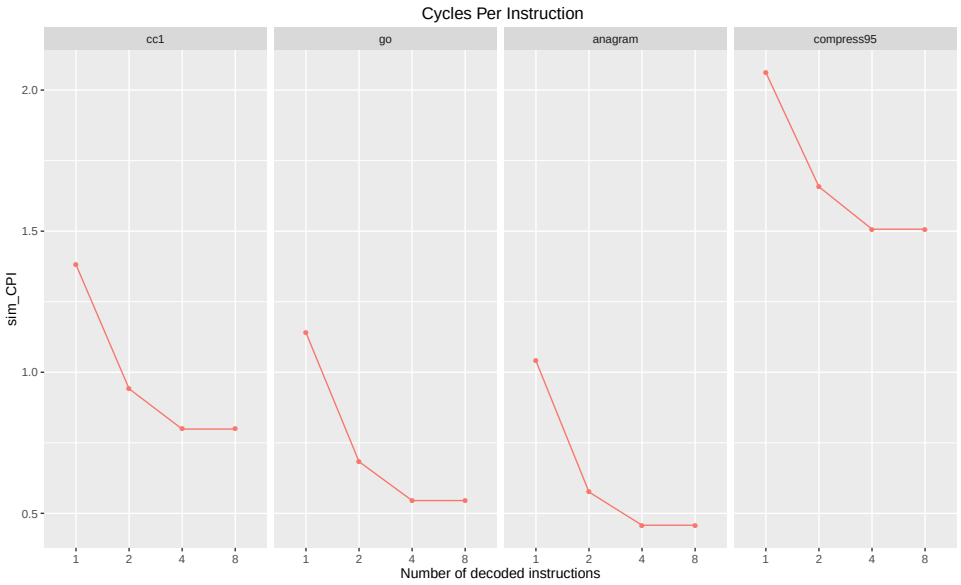

Figure 3: Cycles per instructions vs number of decoded instructions.

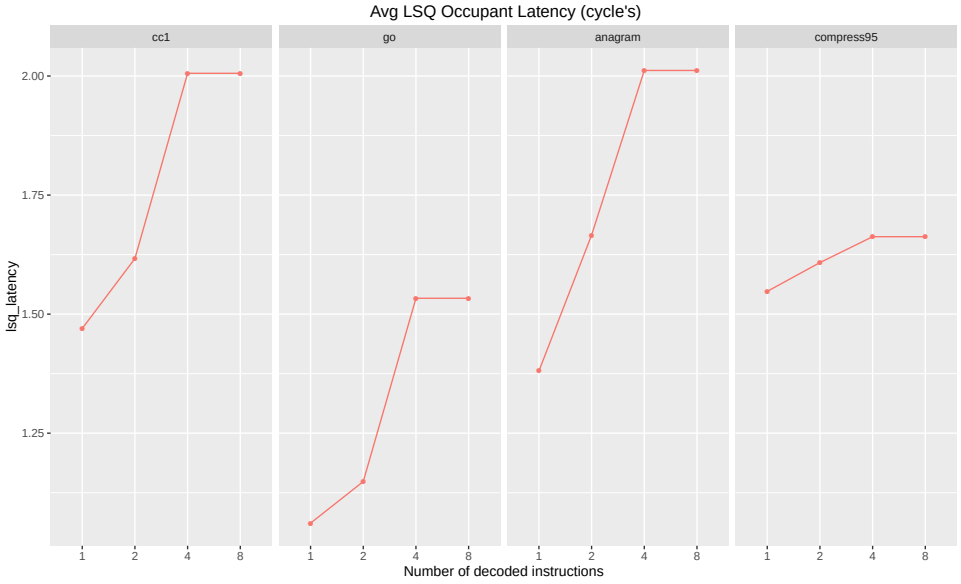

Figure 4: LSQ latency vs number of decoded instructions.

1.3 Number of issued instructions

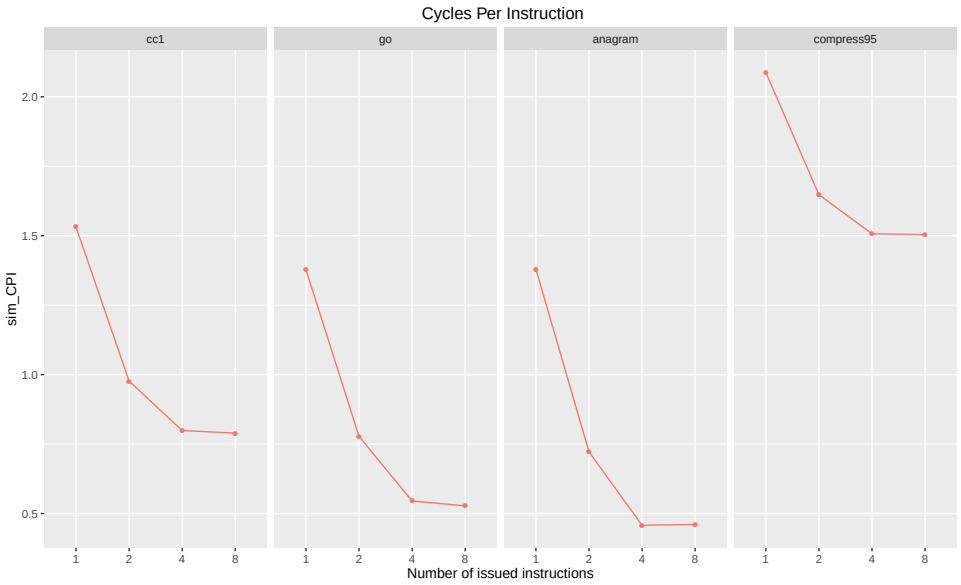

Figure 5: Cycles per instructions vs number of issued instructions.

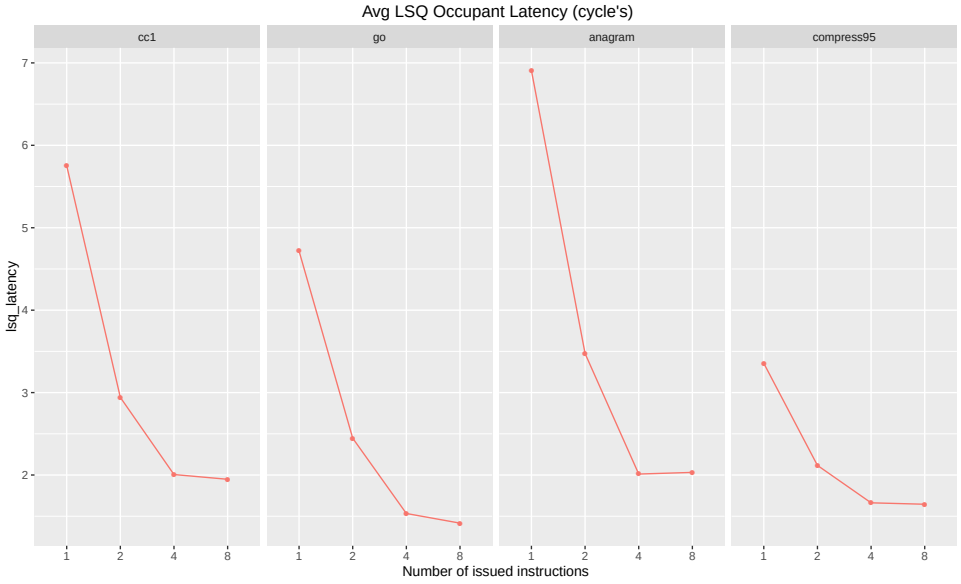

Figure 6: LSQ latency vs number of issued instructions.

1.4 Number of committed instructions

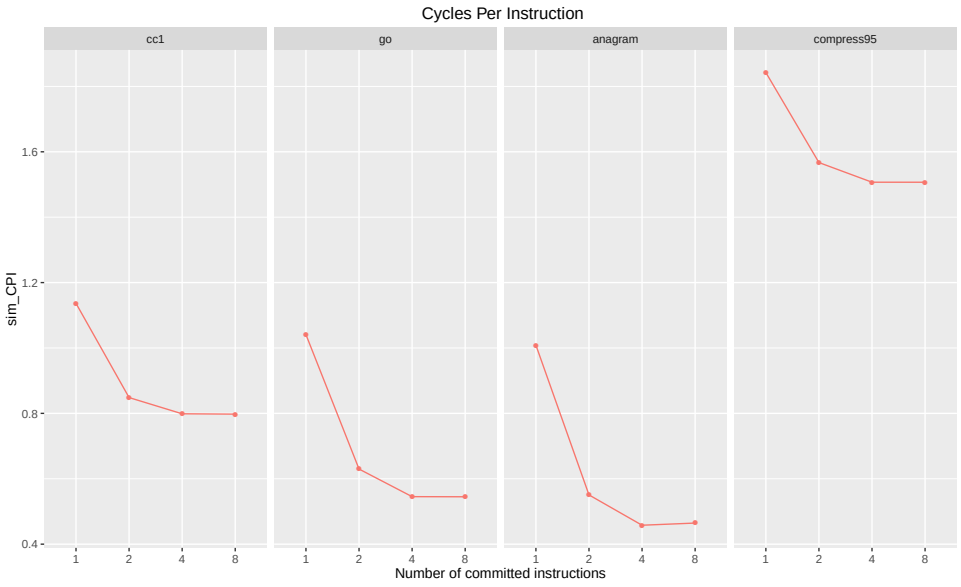

Figure 7: Cycles per instructions vs number of committed instructions.

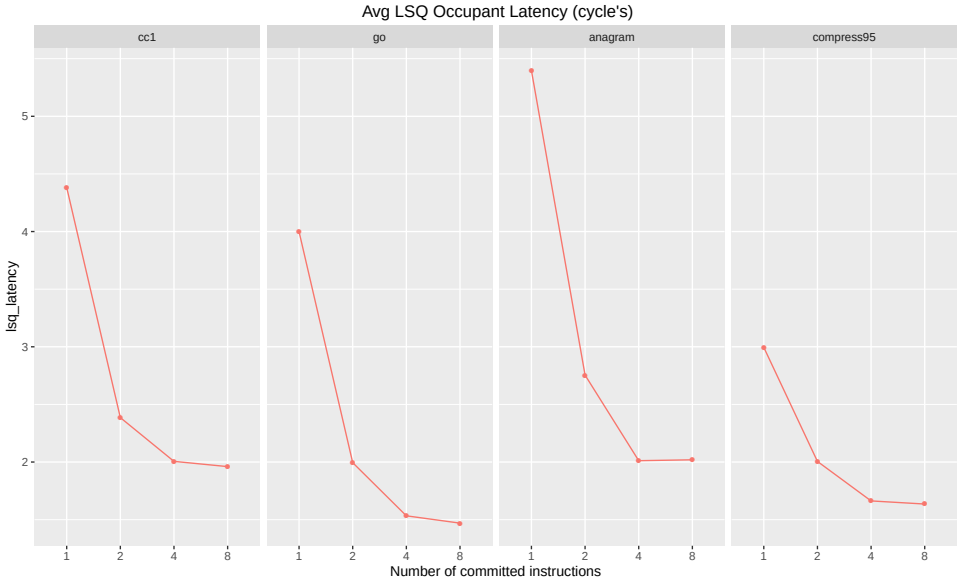

Figure 8: LSQ latency vs number of committed instructions.

1.5 Branch prediction

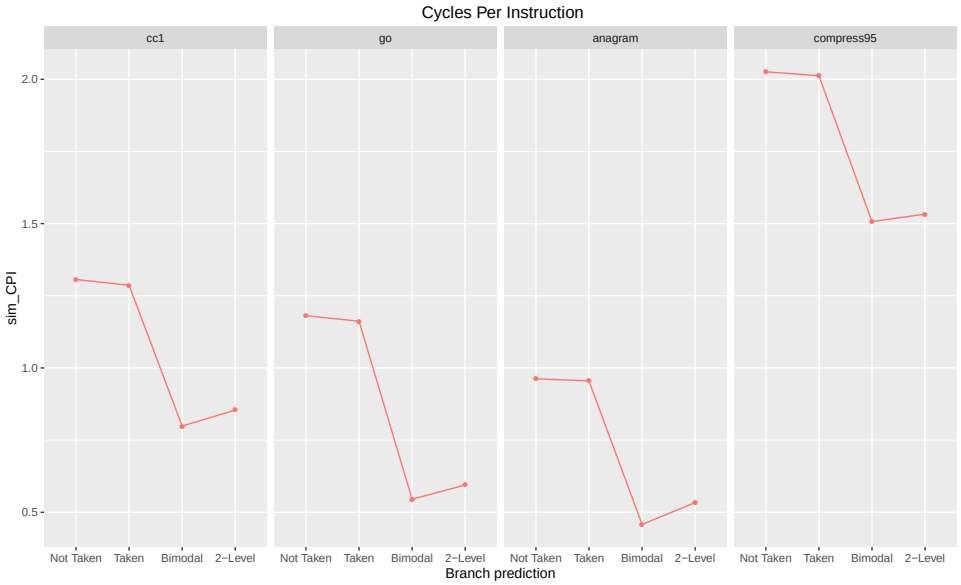

Figure 9: Cycles per instructions vs branch prediction methods.

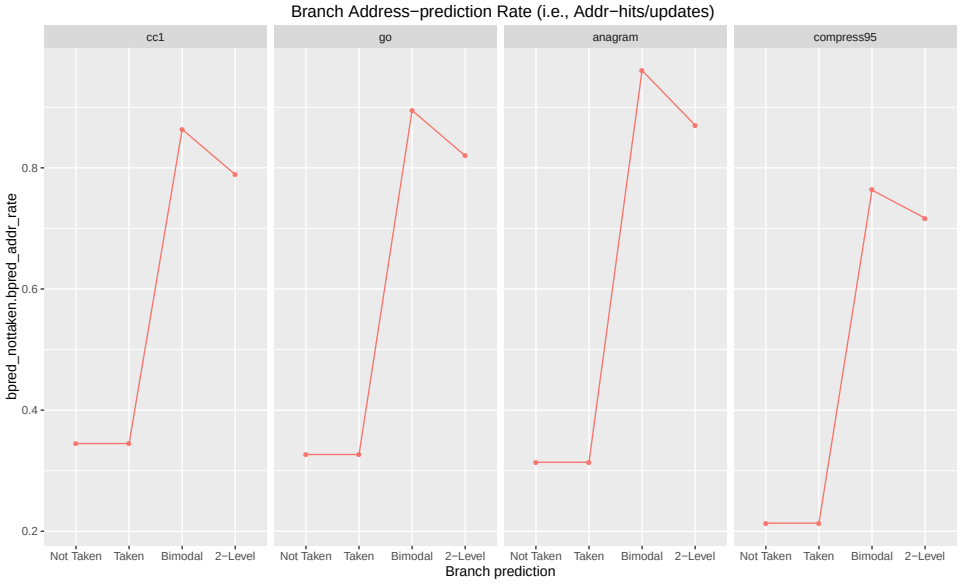

Figure 10: Branch address prediction rate vs branch prediction methods.

1.6 Cache block size

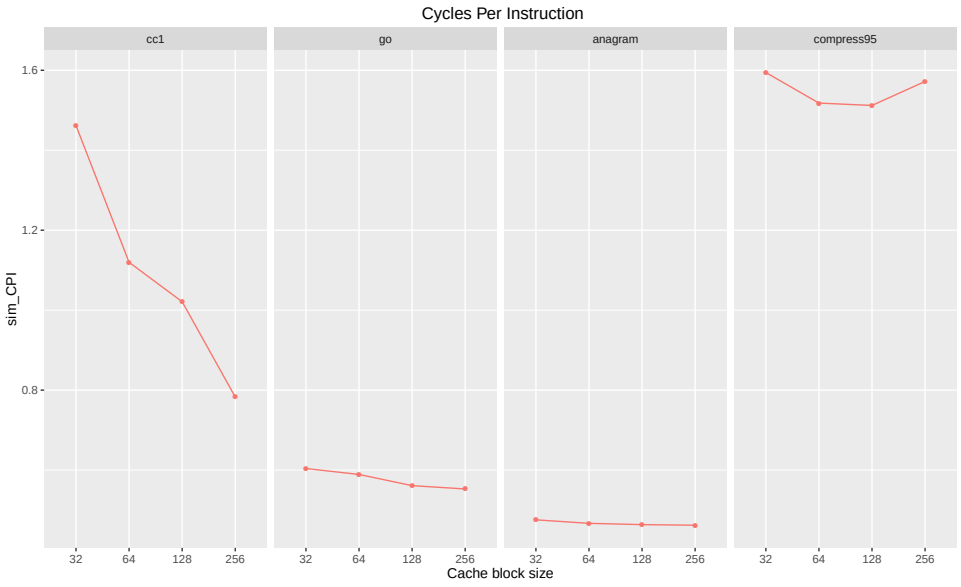

Figure 11: Cycles per instructions vs cache block size.

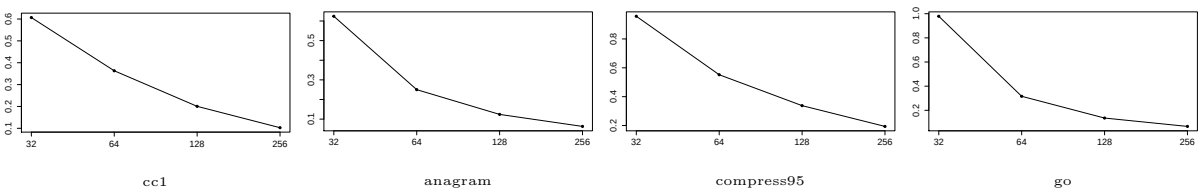

Figure 12: Miss rate vs cache block size.

1.7 Cache replacement policy

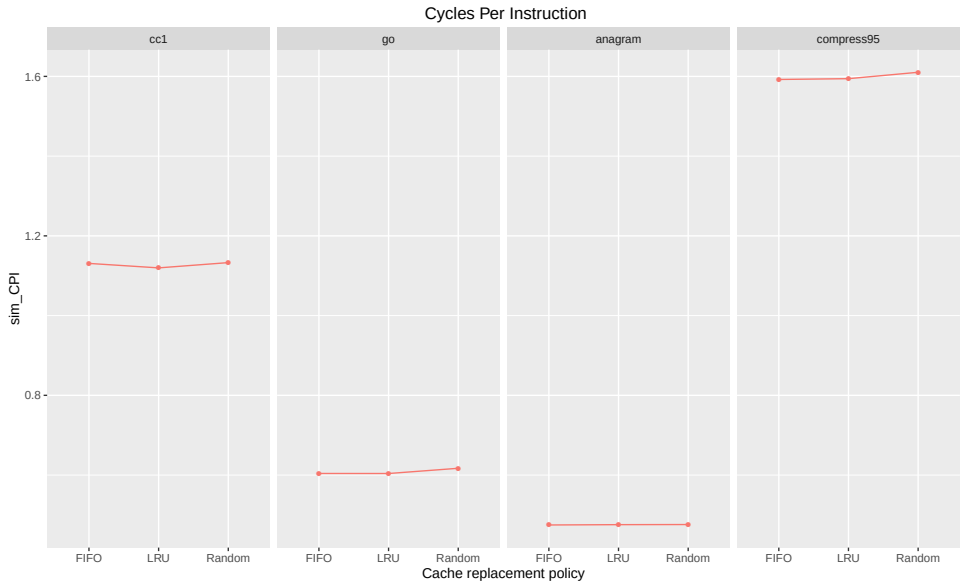

Figure 13: Cycles per instructions vs cache replacement policies.

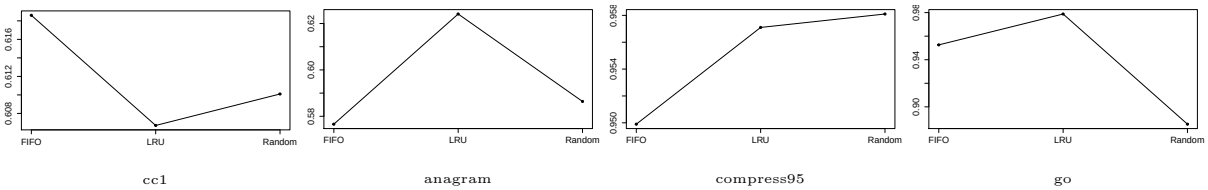

Figure 14: Miss rate vs cache replacement policies.

1.8 Cache associativity

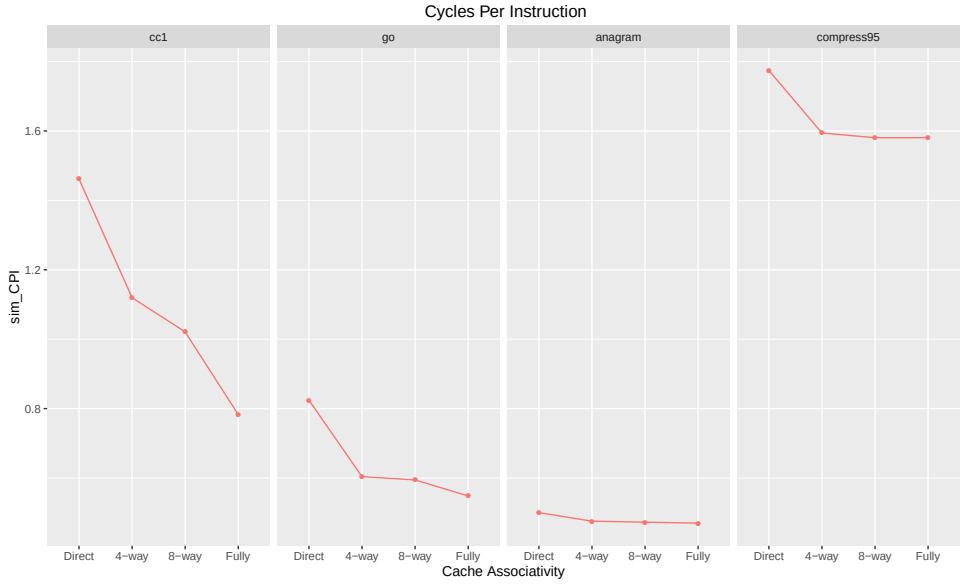

Figure 15: Cycles per instructions vs cache associativity methods.

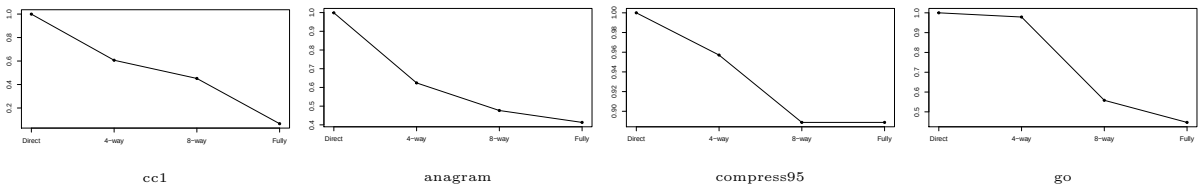

Figure 16: Miss rate vs cache associativity methods.

2 Discussion

In the first part of the assignment, we chose to present the results from the following metrics: CPI (figures 1,3,5,7) and LSQ_latency (figures 2,4,6,8). We observe from the graphs that the CPI metric has the same behavior for all the four benchmarks. This happens because CPI measures the number of cycles per instruction,which is the inverse of IPC (number of instructions per cycle). As a result, if we increase the number of instructions, CPI is decreased. That is the behavior that we observe in all the graphs of CPI vs IPC (fetched, decoded, issued and committed).

For the LSQ_latency metric we have similar behavior for fetched and decoded instructions and for committed and issued but different among those two groups. When we increase the number of fetched and decoded instructions, it is reasonable that the latency in load/store queue will be increased as we increase the data stored in it. In contrast, when we increase the number of issued and committed instructions it is not certain that all of them will use the aforementioned queue.

In part 2 of the assignment (branch prediction), we chose to report the results of CPI (figure 9) and rate of addresses predicted (figure 10). We change the status of the branch predictions between taken (go to the branch), not taken (do not go to the branch), bimodal (go to the branch according to what happened in the past in this branch) and 2-level (go to the branch according to what happened in the past in the other branches). When the program is completed, if the prediction that we made was not correct, we have to go back and execute or not the branch according to what we did during the prediction phase.

As a result, when the status is not taken, it means that we do not execute the branch but if we were wrong we have to go back so we have to execute more instructions. As a result, the cycles are increased. The same happens with the taken status. In contrast, when the status is 2-level, and specifically bimodal, the number of instructions are less because we depend on what happened on the history. So, the system

is learning from a pattern and it goes back less times.

The second metric as we mentioned above was the number of addresses predicted. As we explained in the previous paragraph, we have more chances to predict a correct outcome in the bimodal and 2-level status than in taken and not taken ones. So, the number of addresses predicted correctly is larger for bimodal and 2-level status.

Finally, in the third part of the assignment (caches) we chose to present the results for CPI (figures 11,13,15) and miss_rate (figures 12,14,16). First, we notice that as the block size increases both of those metrics are decreased. This happens because as the block size is increased, the number of missed may be also increased but the rate with which it is increased is decreased. Since, the miss rate is decreased, the average cycles that an instruction uses is also, decreased.

Then, we can see that the same behavior described above is also observed for cache associativity. The justification is the same.

Finally, for the replacement policy, we observe that the behavior for each metric is different for each benchmark. As a result, we believe that the optimal replacement policy depends on the application that we use.

3 Commands

This section presents the scripts in `bash` we used to collect the data from the simulations and benchmarks (see listings 1,2,3,4). We used shell redirect to send the output to files using a specific format naming. Then we coded scripts in `R`[1] to process those files.

We scanned the files and retrieved the "`** simulation statistics **`" section. We collected the metrics for each benchmark changing the corresponding parameters for each feature (i.e. fetched or decoded instructions). Then we used the standard deviation and range to sort the metrics according to their variability and selected the more relevant. Finally, we used the `ggplot2`[2] package to generate the plots.

The scripts in `bash` and `R`, together with additional materials, can be accessed at `https://github.com/aocalderon/PhD/tree/master/Y1Q3/Architecture/Project01`.

[1] The R Project for Statistical Computing (`https://www.r-project.org/`)
[2] `https://cran.r-project.org/web/packages/ggplot2/index.html`

```
#!/bin/bash
# Number of instructions fetched...
./sim-outorder -fetch:ifqsize 1 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_F1.txt
./sim-outorder -fetch:ifqsize 2 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_F2.txt
./sim-outorder -fetch:ifqsize 4 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_F4.txt
./sim-outorder -fetch:ifqsize 8 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_F8.txt

# Number of instructions decoded...
./sim-outorder -decode:width 1 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_D1.txt
./sim-outorder -decode:width 2 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_D2.txt
./sim-outorder -decode:width 4 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_D4.txt
./sim-outorder -decode:width 8 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_D8.txt

# Number of instructions issued...
./sim-outorder -issue:width 1 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_I1.txt
./sim-outorder -issue:width 2 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_I2.txt
./sim-outorder -issue:width 4 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_I4.txt
./sim-outorder -issue:width 8 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_I8.txt

# Number of instructions commited...
./sim-outorder -commit:width 1 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_C1.txt
./sim-outorder -commit:width 2 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_C2.txt
./sim-outorder -commit:width 4 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_C4.txt
./sim-outorder -commit:width 8 ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_C8.txt

# Branch prediction...
./sim-outorder -bpred nottaken ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_BPNT.txt
./sim-outorder -bpred taken ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_BPT.txt
./sim-outorder -bpred bimod ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_BPBM.txt
./sim-outorder -bpred 2lev ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_BP2L.txt

# Cache block size...
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheBS32.txt
./sim-outorder -cache:dl2 ul2:128:64:4:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheBS64.txt
./sim-outorder -cache:dl2 ul2:128:128:4:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheBS128.txt
./sim-outorder -cache:dl2 ul2:128:256:4:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheBS256.txt

# Cache replacement policy...
./sim-outorder -cache:dl2 ul2:128:32:4:f ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheRPF.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheRPL.txt
./sim-outorder -cache:dl2 ul2:128:32:4:r ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheRPR.txt

# Cache associativity...
./sim-outorder -cache:dl2 ul2:128:32:1:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheA1.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheA4.txt
./sim-outorder -cache:dl2 ul2:128:32:8:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheA8.txt
./sim-outorder -cache:dl2 ul2:128:32:64:l ../benchmarks/cc1.alpha ../benchmarks/1stmt.i 2> Results/results_CacheA64.txt
```

Listing 1: Simulation execution commands for *cc1* application.

```
#!/bin/bash
# Number of instructions fetched...
./sim-outorder -fetch:ifqsize 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F1.txt
./sim-outorder -fetch:ifqsize 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F2.txt
./sim-outorder -fetch:ifqsize 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F4.txt
./sim-outorder -fetch:ifqsize 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_F8.txt

# Number of instructions decoded...
./sim-outorder -decode:width 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D1.txt
./sim-outorder -decode:width 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D2.txt
./sim-outorder -decode:width 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D4.txt
./sim-outorder -decode:width 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_D8.txt

# Number of instructions issued...
./sim-outorder -issue:width 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I1.txt
./sim-outorder -issue:width 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I2.txt
./sim-outorder -issue:width 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I4.txt
./sim-outorder -issue:width 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_I8.txt

# Number of instructions commited...
./sim-outorder -commit:width 1 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C1.txt
./sim-outorder -commit:width 2 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C2.txt
./sim-outorder -commit:width 4 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C4.txt
./sim-outorder -commit:width 8 ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_C8.txt

# Branch prediction...
./sim-outorder -bpred nottaken ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BPNT.txt
./sim-outorder -bpred taken ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BPT.txt
./sim-outorder -bpred bimod ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BPBM.txt
./sim-outorder -bpred 2lev ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_BP2L.txt

# Cache block size...
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS32.txt
./sim-outorder -cache:dl2 ul2:128:64:4:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS64.txt
./sim-outorder -cache:dl2 ul2:128:128:4:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS128.txt
./sim-outorder -cache:dl2 ul2:128:256:4:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheBS256.txt

# Cache replacement policy...
./sim-outorder -cache:dl2 ul2:128:32:4:f ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheRPF.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheRPL.txt
./sim-outorder -cache:dl2 ul2:128:32:4:r ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheRPR.txt

# Cache associativity...
./sim-outorder -cache:dl2 ul2:128:32:1:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA1.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA4.txt
./sim-outorder -cache:dl2 ul2:128:32:8:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA8.txt
./sim-outorder -cache:dl2 ul2:128:32:64:l ../benchmarks/anagram.alpha ../benchmarks/words < ../benchmarks/anagram.in 2> Results/results_A_CacheA64.txt
```

Listing 2: Simulation execution commands for *anagram* application.

```
#!/bin/bash
# Number of instructions fetched...
./sim-outorder -fetch:ifqsize 1 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_F1.txt
./sim-outorder -fetch:ifqsize 2 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_F2.txt
./sim-outorder -fetch:ifqsize 4 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_F4.txt
./sim-outorder -fetch:ifqsize 8 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_F8.txt

# Number of instructions decoded...
./sim-outorder -decode:width 1 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_D1.txt
./sim-outorder -decode:width 2 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_D2.txt
./sim-outorder -decode:width 4 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_D4.txt
./sim-outorder -decode:width 8 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_D8.txt

# Number of instructions issued...
./sim-outorder -issue:width 1 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_I1.txt
./sim-outorder -issue:width 2 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_I2.txt
./sim-outorder -issue:width 4 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_I4.txt
./sim-outorder -issue:width 8 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_I8.txt

# Number of instructions commited...
./sim-outorder -commit:width 1 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_C1.txt
./sim-outorder -commit:width 2 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_C2.txt
./sim-outorder -commit:width 4 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_C4.txt
./sim-outorder -commit:width 8 ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_C8.txt

# Branch prediction...
./sim-outorder -bpred nottaken ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_BPNT.txt
./sim-outorder -bpred taken ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_BPT.txt
./sim-outorder -bpred bimod ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_BPBM.txt
./sim-outorder -bpred 2lev ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_BP2L.txt

# Cache block size...
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheBS32.txt
./sim-outorder -cache:dl2 ul2:128:64:4:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheBS64.txt
./sim-outorder -cache:dl2 ul2:128:128:4:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheBS128.txt
./sim-outorder -cache:dl2 ul2:128:256:4:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheBS256.txt

# Cache replacement policy...
./sim-outorder -cache:dl2 ul2:128:32:4:f ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheRPF.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheRPL.txt
./sim-outorder -cache:dl2 ul2:128:32:4:r ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheRPR.txt

# Cache associativity...
./sim-outorder -cache:dl2 ul2:128:32:1:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheA1.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheA4.txt
./sim-outorder -cache:dl2 ul2:128:32:8:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheA8.txt
./sim-outorder -cache:dl2 ul2:128:32:64:l ../benchmarks/compress95.alpha ../benchmarks/1stmt.i 2> Results/results_C_CacheA64.txt
```

Listing 3: Simulation execution commands for *compress95* application.

```
#!/bin/bash
# Number of instructions fetched...
./sim-outorder -fetch:ifqsize 1 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_F1.txt
./sim-outorder -fetch:ifqsize 2 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_F2.txt
./sim-outorder -fetch:ifqsize 4 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_F4.txt
./sim-outorder -fetch:ifqsize 8 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_F8.txt

# Number of instructions decoded...
./sim-outorder -decode:width 1 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_D1.txt
./sim-outorder -decode:width 2 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_D2.txt
./sim-outorder -decode:width 4 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_D4.txt
./sim-outorder -decode:width 8 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_D8.txt

# Number of instructions issued...
./sim-outorder -issue:width 1 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_I1.txt
./sim-outorder -issue:width 2 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_I2.txt
./sim-outorder -issue:width 4 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_I4.txt
./sim-outorder -issue:width 8 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_I8.txt

# Number of instructions commited...
./sim-outorder -commit:width 1 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_C1.txt
./sim-outorder -commit:width 2 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_C2.txt
./sim-outorder -commit:width 4 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_C4.txt
./sim-outorder -commit:width 8 ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_C8.txt

# Branch prediction...
./sim-outorder -bpred nottaken ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_BPNT.txt
./sim-outorder -bpred taken ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_BPT.txt
./sim-outorder -bpred bimod ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_BPBM.txt
./sim-outorder -bpred 2lev ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_BP2L.txt

# Cache block size...
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheBS32.txt
./sim-outorder -cache:dl2 ul2:128:64:4:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheBS64.txt
./sim-outorder -cache:dl2 ul2:128:128:4:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheBS128.txt
./sim-outorder -cache:dl2 ul2:128:256:4:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheBS256.txt

# Cache replacement policy...
./sim-outorder -cache:dl2 ul2:128:32:4:f ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheRPF.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheRPL.txt
./sim-outorder -cache:dl2 ul2:128:32:4:r ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheRPR.txt

# Cache associativity...
./sim-outorder -cache:dl2 ul2:128:32:1:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheA1.txt
./sim-outorder -cache:dl2 ul2:128:32:4:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheA4.txt
./sim-outorder -cache:dl2 ul2:128:32:8:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheA8.txt
./sim-outorder -cache:dl2 ul2:128:32:64:l ../benchmarks/go.alpha ../benchmarks/1stmt.i 2> Results/results_G_CacheA64.txt
```

Listing 4: Simulation execution commands for *go* application.