Apollo CMv3 Synthesizer and Clock Distribution Production Testing

This document describes a procedure for testing the five synthesizers on the CMv3, along with the distribution wiring of the clocks to the FPGAs and to the other synthesizers. Overall, it is a two-step process.

Step 1: Every synthesizer is configured with unique frequencies on each output, requiring 5 configuration files. Each synthesizer uses its own local crystal oscillator to generate the outputs. Frequency counters in the FPGAs are used to measure the frequency of each incoming clock. The measured values are compared against expected values.

Step 2: Configuration files that use the various input clocks to each synthesizer are loaded. Each configuration only exercises a single clock input, so 12 configuration files are required for full coverage. Since the distribution wiring was tested and verified in step 1, only a single incoming clock in each FPGA needs to be measured and verified.

Rather than downloading configuration files from the computer as each is needed, it is suggested that all configurations be loaded in the EPROM. The desired configurations will be copied from the EPROM to the synthesizers as they are needed. This should allow all tests to run without human intervention.

Associated Files

Many files are found on github at https://github.com/apollo-lhc/Cornell_CM_Rev3_HW . Documents related to testing are found in the "BoardTesting" directory. Synthesizer configuration are found in the "ClockBuilderPRO" directory.

Standalone Test Board

The tests in this document use the 6089-129_CM_TESTBOARD. It has been designed to exercise the CM on the benchtop without using an SM. The schematic is in the "BoardTesting" directory.

1 Testing the distribution of REFCLK and Logic Clock signals

Each FPGA has 28 REFCLK inputs, 6 logic clock inputs, one clock input on "spare_in[2]" from the other FPGA, and one input from a 200 MHz oscillator. Each FPGA will need 35 frequency counters to test the clock distribution. The 200 MHz oscillator will be used as a reference to gate the frequency counters. It is also sent to the other FPGA on "spare_out[2]". The spare pair cross-connect is used to check the 200 MHz oscillators.

Testing of the TCDS RECOVERED CLOCK requires a 40 MHz clock on the TCDS_RECOV_CLOCK output pins of FPGA#1. This clock should be created from the 200 MHz oscillator input.

Load the frequency counter test code into the FPGAs. Table 2 lists the transceiver clocks that need to be checked. These require an IBUFDS_GTE4 followed by a BUFG_GT to connect the clock pins to the

frequency counter. Table 3 list the logic clocks that need to be checked. These require an IBUFDS to connect the clock pins to the frequency counter.

A set of clock synthesizer configuration files have been developed for these tests. They attempt to generate as many unique frequencies as possible. Tables or lists of expected frequencies are provided for each test step.

Eight of the clocks generated from the R0A and R0B synthesizers are fanned out to multiple destinations (see schematic sheet 2.08 REFCLK R0 FANOUT). These are noted in the tables with a number in the “A/B Switch” column. The information in the “A/B Switch” column tells which I2C register output in Table 1 (schematic sheet 4.03: I2C CLOCK CONTROL) controls switching the source between R0A and R0B.

A list of the required configuration file for each synth will be given at the start of each test. If a particular synth is not listed then it does not matter how that synth is configured.

Table 1 Switching clock source between R0A and R0B

A/B Switch	Signal	IC	Bit #
1	F1L_X12_R0_SEL	U88	P00
2	F1L_X4_R0_SEL	U88	P01
3	F1R_X12_R0_SEL	U88	P02
4	F1R_X4_R0_SEL	U88	P03
5	F2L_X12_R0_SEL	U83	P00
6	F2L_X4_R0_SEL	U83	P01
7	F2R_X12_R0_SEL	U83	P02
8	F2R_X4_R0_SEL	U83	P03

1.1 Check the outputs of all synths

Load the following configuration files into the synthesizers. All of these are free running, using the attached 48 MHz crystal.

R0A: R0Av3X01
R0B: R0Bv3X01
R1A: R1Av3X01
R1B: R1Bv3X01
R1C: R1Cv3X01

1.1.1 Use R0A to drive the clocks

Configure the clock source for the clock buffers on schematic 2.08 to use the outputs of synth R0A. Do this by setting the 4 lowest bits of both I2C registers on schematic 4.03 to zeroes.

1.1.2 Verify the frequency of each R0A clock

Read the frequency counters from each FPGA. Confirm that the values for each FPGA match the expected frequencies from Table 2 (GTY REFCLKs) and Table 3 (Logic Clocks). Where two frequencies are listed, like “300/290”, the first number is the frequency from synth R0A.

1.1.3 Use R0B to drive the clocks

Configure the clock source for the clock buffers on schematic 2.08 to use the outputs of synth R0B. Do this by setting the 4 lowest bits of both I2C registers on schematic 4.03 to ones.

1.1.4 Verify the frequency of each R0B clock

Read the frequency counters from each FPGA. Confirm that the values for each FPGA match the expected frequencies from Table 2 (GTY REFCLKs) and Table 3 (Logic Clocks). Where two frequencies are listed, like “300/290”, the second number is the frequency from synth R0B.

There is no need to re-verify the outputs of R1A, R1B, and R1C.

Table 2 Step #1 Frequencies for REFCLK inputs (IBUFDS_GTE4 followed by a BUFG_GT)

Quad #	Quad Letter	Ref #	Vivado Constraints Name		FPGA #1 A/B Switch	FPGA #1 Source	FPGA #1 Freq		FPGA #2 A/B Switch	FPGA #2 Source	FPGA #2 Freq
120	AB	R0	lf_r0_ab			R1A-0A	60			R1A-0	40
120	AB	R1	lf_r1_ab			R1B-0	220			R1B-1	110
122	AD	R0	lf_r0_ad		1	R0A/B-2	300/290		5	R0A/B-6	260/250
122	AD	R1	lf_r1_ad			R1B-2	132			R1B-6	148
124	AF	R0	lf_r0_af		2	R0A/B-3	150/145		6	R0A/B-7	130/125
124	AF	R1	lf_r1_af			R1A-4	168			R1A-6	156
126	R	R0	lf_r0_r		1	R0A/B-2	300/290		5	R0A/B-6	260/250
126	R	R1	lf_r1_r			R1B-3	296			F1B-7	268
129	U	R0	lf_r0_u		1	R0A/B-2	300/290		5	R0A/B-6	260/250
129	U	R1	lf_r1_u			R1B-0A	176			R1B-5	326
131	W	R0	lf_r0_w		2	R0A/B-3	150/145		6	R0A/B-7	130/125
131	W	R1	lf_r1_w			R1A-3	312			R1A-5	336
133	Y	R0	lf_r0_y		1	R0A/B-2	300/290		5	R0A/B-6	260/250
133	Y	R1	lf_r1_y			R1B-4	163			R1B-8	134
220	L	R0	rt_r0_l			OSC	200			OSC	200
220	L	R1	rt_r1_l			R1A-7	272			R1A-8	136
222	N	R0	rt_r0_n		3	R0A/B-1	160/155		7	R0A/B-0	320/310
222	N	R1	rt_r1_n			R1C-4	170			R1C-5	340
224	P	R0	rt_r0_p		4	R0A/B-4	280/270		8	R0A/B-5	140/135
224	P	R1	rt_r1_p			R1C-0A	116			R1C-9	226
226	B	R0	rt_r0_b		3	R0A/B-1	160/155		7	R0A/B-0	320/310
226	B	R1	rt_r1_b			R1C-6	155			R1C-3	310
229	E	R0	rt_r0_e		3	R0A/B-1	160/155		7	R0A/B-0	320/310
229	E	R1	rt_r1_e			R1C-7	286			R1C-2	348
231	G	R0	rt_r0_g		4	R0A/B-4	280/270		8	R0A/B-5	140/135
231	G	R1	rt_r1_g			R1C-8	143			R1C-0	232
233	I	R0	rt_r0_i		3	R0A/B-1	160/155		7	R0A/B-0	320/310
233	I	R1	rt_r1_i			R1C-9A	113			R1C-1	174

Table 3 Step #1 Frequencies for Logic Clock inputs (IBUFDS)

					FPGA #1				FPGA #2	
Logic Clock Name (schematic)	Logic Clock Name (constraint file)	Logic Clock Pins		A/B Switch	Source	Freq		A/B Switch	Source	Freq
FnL_X12_R0_CLK	lf_x12_r0_clk	P33/P34		1	R0A/B-2	300/290		5	R0A/B-6	260/250
FnL_X4_R0_CLK	lf_x4_r0_clk	N32/M32		2	R0A/B-3	150/145		6	R0A/B-7	130/125
FnR_X12_R0_CLK	rt_x12_r0_clk	R18/R17		3	R0A/B-1	160/155		7	R0A/B-0	320/310
FnR_X4_R0_CLK	rt_x4_r0_clk	N19/N18		4	R0A/B-4	280/270		8	R0A/B-5	140/135
Fn_TCDS40_CLK	tcds40_clk	BF27/BF28			R1B-9	55			R1B-9	55
LHC_CLK	lhc_clk	BE26/BE27			SM	40			SM	40
FnFmSPARE2	in_spare[2]	C29/C30			FPGA#2	200			FPGA#1	200

1.2 Test clock inputs to synth R0B

1.2.1 Use R0B to drive the clocks

Configure the clock source for the clock buffers on schematic 2.08 to use the outputs of synth R0B. Do this by setting the 4 lowest bits of both I2C registers on schematic 4.03 to ones.

1.2.2 Test Input IN_0 coming from synth R0A OUT_8

R0A: R0Av3X01 (no change if following test sequence)
R0B: R0Bv3X02

This configuration for synth R0B will use the 240 MHz signal that comes from OUT_8 on R0A as its input. This configuration sets all FPGA clocks at 240 MHz. It also enables the feedback input to use the 240 MHz signal from OUT_9A.

Since the output connections of synth R0B have already been checked, only one of them needs to be checked for the 240 MHz signal.

1.2.3 (optional) Test Input IN_1 from front panel connector F1_EXT_CLK

R0A: R0Av3X01 (no change if following test sequence)
R0B: R0Bv3X03

Install a cable from the “FP CLK 1” connector on the test board to the front panel “F1 EXT CLK” connector. Configure the test board so that the 320 MHz oscillator is driving the cable.

This configuration for synth R0B will use the signal from the front panel “F1 EXT CLK” connector as its input. This configuration sets all FPGA clocks at 320 MHz. It also enables the feedback input to use the 320 MHz signal from OUT_9A.

Since the output connections of synth R0B have already been checked, only one of them needs to be checked for the 320 MHz signal.

1.2.4 Test Input IN_2 from backplane 40 MHZ LHC CLK

R0A: R0Av3X01 (no change if following test sequence)
R0B: R0Bv3X04

This configuration for synth R0B will use the 40 MHz signal that comes from the SM connector “LHC CLK” as its input. This configuration file sets all FPGA clocks at 200 MHz. It also enables the feedback input to use the 200 MHz signal from OUT_9A.

Since the output connections of synth R0B have already been checked, only one of them needs to be checked for the 200 MHz signal.

1.3 Test clock inputs to synth R0A

1.3.1 Use R0A to drive the clocks

Configure the clock source for the clock buffers on schematic 2.08 to use the outputs of synth R0A. Do this by setting the 4 lowest bits of both I2C registers on schematic 4.03 to zeroes.

1.3.2 Test Input IN_1 coming from synth R0B OUT_8

R0A: R0Av3X02
R0B: R0Bv3X01

This configuration for synth R0A will use the 230 MHz signal that comes from OUT_8 on R0B as its input. This configuration file sets all FPGA clocks at 230 MHz. It also enables the feedback input to use the 230 MHz signal from OUT_9A.

Since the output connections of synth R0A have already been checked, only one of them needs to be checked for the 230 MHz signal.

1.4 Test clock inputs to synth R1A

1.4.1 Test Input IN_0 from backplane 320 MHz HQ CLK

R1A: R1Av3X02

This configuration for synth R1A will use the 320 MHz signal that comes from the SM connector “HQ CLK” as its input. This configuration file sets all FPGA clocks at 320 MHz. It also enables the feedback input to use the 320 MHz signal from OUT_9A.

Since the output connections of synth R1A have already been checked, only one of them needs to be checked for the 320 MHz signal.

1.4.2 (optional) Test Input IN_1 from front panel connector F2_EXT_CLK

R1A: R1Av3X03

Install a cable from the “FP CLK 2” connector on the test board to the front panel “F2 EXT CLK” connector. Configure the test board so that the 40 MHz oscillator is driving the cable.

This configuration for synth R1A will use the signal from the front panel “F2 EXT CLK” connector as its input. This configuration sets all FPGA clocks at 160 MHz. It also enables the feedback input to use the 40 MHz signal from OUT_9A.

Since the output connections of synth R1A have already been checked, only one of them needs to be checked for the 160 MHz signal.

1.4.3 Test Input IN_2 from backplane 40 MHz LHC CLK

R1A: R1Av3X04

This configuration for synth R1A will use the 40 MHz signal that comes from the SM connector “LHC CLK” as its input. This configuration file sets all FPGA clocks at 120 MHz. It also enables the feedback input to use the 40 MHz signal from OUT_9A.

Since the output connections of synth R1A have already been checked, only one of them needs to be checked for the 120 MHz signal.

1.5 Test clock inputs to synth R1B

1.5.1 Test Input IN_0 from synth R1A OUT_1 at 100 MHz

R1A: R1Av3X01
R1B: R1Bv3X02

This configuration for synth R1B will use the 100 MHz signal that comes from OUT_1 on R1A as its input. This configuration file sets all FPGA clocks at 200 MHz. It also enables the feedback input to use the 100 MHz signal from OUT_9A.

Since the output connections of synth R1B have already been checked, only one of them needs to be checked for the 200 MHz signal.

1.5.2 Test Input IN_1 from 40 MHz TCDS RECOVERED CLOCK

R1B: R1Bv3X03

Be sure that FPGA#1 has been programmed to put a 40 MHz clock on the TCDS_RECOV_CLOCK output pins. It should generate this clock from the fixed 200 MHz oscillator input.

This configuration for synth R1B will use the signal from the TCDS RECOVERED CLOCK as its input. This configuration sets all FPGA clocks at 280 MHz. It also enables the feedback input to use the 40 MHz signal from OUT_9A.

Since the output connections of synth R1B have already been checked, only one of them needs to be checked for the 280 MHz signal.

1.5.3 Test Input IN_2 from backplane LHC CLK

R1B: R1Bv3X04

This configuration for synth R1B will use the 40 MHz signal that comes from the SM connector “LHC CLK” as its input. This configuration file sets all FPGA clocks at 120 MHz. It also enables the feedback input to use the 40 MHz signal from OUT_9A.

Since the output connections of synth R1B have already been checked, only one of them needs to be checked for the 120 MHz signal.

1.6 Test clock inputs to synth R1C

1.6.1 Test Input IN_0 from synth R1A OUT_2 at 120 MHz

R1A: R1Av3X01
R1C: R1Cv3X02

This configuration for synth R1C will use the 120 MHz signal that comes from OUT_2 on R1A as its input. This configuration file sets all FPGA clocks at 240 MHz. R1C does not use feedback.

Since the output connections of synth R1C have already been checked, only one of them needs to be checked for the 240 MHz signal.

1.6.2 Test Input IN_2 from backplane 40 MHz LHC CLK

R1C: R1Cv3X03

This configuration for synth R1C will use the 40 MHz signal that comes from the SM connector “LHC CLK” as its input. This configuration file sets all FPGA clocks at 180 MHz. R1C does not use feedback.

Since the output connections of synth R1C have already been checked, only one of them needs to be checked for the 180 MHz signal.