# Associated Files

Many files are found on github at <https://github.com/apollo-lhc/Cornell_CM_Rev3_HW> . Documents related to testing are found in the “BoardTesting” directory.

# Standalone Test Board

The 6089-129\_CM\_TESTBOARD has been designed to exercise the CM without using an SM. The schematic is in the “BoardTesting” directory.

The test board mates with the three main connectors on the CM. Optional short cables mate with the front panel connectors of the CM. The test board provides connectors for 12 volt power, the Xilinx JTAG programmer, Linux UART cables, and Linux I2C and digital I/O cables. It also has jumper sites to allow one to connect most CM signal traces in a loop-back mode. Single-ended to differential input buffers allow external sources to drive many CM signals, while differential to single-ended output buffers support connections to scopes or other test equipment.

The photos below show the test board alone, and mated with an Apollo CMv3 board.

A green circuit board with many small ports

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A green circuit board with many small chips

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# Power Connector

Connector J1 is used to provide DC power to the CM (figure 1-1). For testing, the external power supply should provide a variable voltage from 0 to 12 volts at a current of at least 5 amps (60 watts). For applications without an SM, a 20 amp supply, plus cooling, is required.

The “12V LED” will gradually brighten as the voltage approaches 12 volts. The “3V3 LED” will turn on when the input voltage passes approximately 6.4 volts.

Figure ‑ 12 Volt Power Connector

A green circuit board with a green connector

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The power cable uses a 4-pin plug (DigiKey 277-2418) at the board end. The power supply end will use whatever is appropriate for the given supply. Banana plugs may be good for up to 5 amps.

Twist together two lengths of red and two lengths of black stranded wire, #20 gauge for testing and #16 gauge for non-SM applications. Twist the two colors together and connect as shown in figure 1-2.

Figure ‑ Power Cable Wiring

A green and black electrical connector

Description automatically generated A close-up of a black and red electrical plugs

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# UART Connections

Connector J27, labeled “ZYNQ UART”, is used to connect to the MCU’s UART #0. The is the SM’s ZYNC UART. Connector J28, labeled “IPMC UART”, is used to connect to the MCU’s UART #3. The is the SM’s IPMC UART. See figure 2-1.

Figure ‑ UART Connectors

A close-up of a circuit board

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The UART signals are connected to a computer using a 3.3 volt USB-to-TTL\_RS232 cable. This is an FTDI “TTL-232R-3V3” (DigiKey 768-1015). The 6-pin header that comes on the cable must be replaced with a 6-pin plug (DigiKey 277-2414). It is wired as shown in figure 2-2. Pins 2, 3, and 6 are not connected on the test board.

1-Black

2-Brown

3-Red

4-Yellow

5-Orange

6-Green

Figure ‑ UART Connector Wiring

A green electrical device with wires

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Figure ‑ UART Cable Colors and Signals

A diagram of a wire

Description automatically generated

# UART Jumpers

Headers J20 and J21 allow one to configure how the UART signals from the CM are connected. There are four options: A) MCU UART signals to cable, B) MCU UART signals looped back, C) MCU UART signals floating, and D) special wiring with wire-wrap wires.

In figure 2-1, J20 is configured to connect the ZYNQ UART signals from the MCU to the UART cable that is plugged into the “ZYNQ UART” header. J21 is configured to loop the IPMC UART transmit signal back to the receive signal. This allows the MCU to test itself by activating the transmit line and verifying that the receive line detects the same activity.

Figure ‑ UART Connector Schematic

A close-up of a computer wiring

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# I2C and GPIO Connections

Connector J18 and J19 are used to interface the test board with a USB-to-I2C/GPIO cable (figure 4-1). J19, labeled “ZYNQ I2C”, is used to connect to the MCU’s I2C channel #8. The is the MCU’s port on pins 35 and 36. It connects to the SM’s ZYNC. The current use is in flux. It might be used as a uni-directional UART, rather than an I2C port. There are also four GPIO signal on this connector.

Connector J18, labeled “IPMC I2C”, is used to connect to the MCU’s I2C channel #0. The is the MCU’s “slave” I2C port on MCU pins 91 and 92. It connects to the SM’s IPMC “master” I2C port. There are also four GPIO signal on this connector.

Figure ‑ I2C and GPIO Connectors

Close-up of a green circuit board

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The I2C and GPIO signals are connected to a computer using a 3.3 volt USB-to-I2C cable. This is an FTDI “C232HM-DDHSL” (DigiKey 768-1106). The 10 flying leads that comes on the cable must be replaced with a 10-pin plug (DigiKey 277-5730). It is wired as shown in figure 4-2. Pins 1 and 5 are not connected on the test board.

1-Red

2-Orange

3-Yellow

4-Green

5-Brown

6-Gray

7-Purple

8-White

9-Blue

10-Black

Figure ‑ I2C Connector Wiring

A green electrical connector with colored wires

Description automatically generated with medium confidence

Figure ‑ I2C and GPIO Connector Schematic

# I2C and GPIO Jumpers

Figure 5-1 shows the connections between the USB cable connectors and the CM’s low-speed connector.

Figure ‑ I2C and GPIO Connector Schematic

A diagram of a computer

Description automatically generated

Header J8 through J13 allow one to configure how the I2C and GPIO signals from the CM are connected. There are four options: A) signals to cable, B) signals looped back, C) signals floating, and D) special wiring with wire-wrap wires.

J8-1 (MCU pin-91): IPMC\_I2C\_SCL

J8-3 (MCU pin-92): IPMC\_I2C\_SDA

For basic testing, use a loopback jumper from pin-1 to pin-3, and program one pin as an output and the other pin as an input. Note that pins 2 and 4 are always wired to the I2C signals on the FireFly. There are 2.2k pullup resistors on these signals.

J9-1 (MCU RESET): CABLE\_SM\_TO\_CM\_PWR\_EN

J9-3 (FIREFLY\_RESET):

For basic testing, leave these floating. Install a jumper from J9-1 to J9-2 if GPIO#0 on the IPMC I2C connector will be used to control booting of the MCU. Otherwise, just use the MCU BOOT switch to take the MCU out of its RESET state (switch=OFF) and allow it to boot (switch=BOOT) .

J10-1 (MCU pin-76): CM\_TO\_SM\_PWR\_OK

J10-3: CABLE\_SM\_SOFT\_PWR\_EN

For basic testing, use loopback jumper, and program MCU pin-76 as an output. Program MCU pin-30 SM\_SOFT\_PWR\_EN as an input. Set the CM\_PWR\_EN toggle switch to OFF. NOTE: A loopback jumper in this position will prevent “normal” MCU code from turning on the power supplies, due to the requirement that the PWR\_EN be asserted before the MCU asserts PWR\_OK.

J11-1 (MCU pin 35): ZYNQ\_I2C\_SCL

J11-3 (MCU pin-36): ZYNQ\_I2C\_SDA

For basic testing, use loopback jumper, and program one pin as an output and the other pin as an input.

J12-1 (MCU pin-25): ZYNQ\_GPIO1

J12-3 (MCU pin-24): ZYNQ\_GPIO2

For basic testing, use loopback jumper, and program one pin as an output and the other pin as an input.

J13-1 (MCU pin-40): CPLD\_GPIO0

J13-3 (MCU pin-41): CPLD\_GPIO1

For basic testing, use loopback jumper, and program one pin as an output and the other pin as an input.

Figure 5-1 shows a typical jumper configuration using loopback jumpers on J8, J11, J12, and J13.

Figure ‑ I2C and GPIO Jumpers

Close-up of a circuit board

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# FPGA JTAG connector

Connector J22 is a keyed 14-pin header that will mate with the standard cable on a Xilinx JTAG programmer. It has latches to hold the connector in place. The ejectors may not engage with some cables. The voltage level for the JTAG signaling is 3.3 volts.

Figure ‑ JTAG Cable Plugged into Connector J22

A close-up of a circuit board

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# Switches

The toggle switch labeled “MCU BOOT” holds the MCU in its RESET state by pulling SM\_TO\_CM\_PWR\_EN low when the switch is in the OFF position. The BOOT position allows the MCU to boot up and run. It probably needs to be in the BOOT position to allow the CM’s front-panel MCU JTAG connector to be used.

The toggle switch labeled “CM PWR EN” controls the SM\_SOFT\_PWR\_EN signal. It is low when the switch is in the OFF position. Moving to the ENA position allows normal MCU code to turn on the DC-DC converters on the CM. This signal is used in normal CM operation. Basic test programs may not need to have this signal asserted.

Figure ‑ "MCU BOOT" and "CM PWR EN" switches

Close-up of a circuit board

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# HDMI External Digital I/O Connectors

Each FPGA on the CM has 12 traces that are wired to an HDMI connector on the front panel. Figure 8-1 shows the front panel connector for FPGA #1. Figure 8-2 shows the connector for FPGA #2. Figure 8-3 shows the FPGA connections. The use of these signals is not pre-defined, and can be different for each FPGA. They can be configured as inputs or outputs. The TEST\_CONN\_0 through TEST\_CONN\_4 signals can be used as differential pairs or as single-ended signals. TEST\_CONN\_5 and TEST\_CONN\_6 are not a twisted pair in most HDMI cables. The TEST\_CONN\_0 signals are connected to global clock capable FPGA pins.

Figure ‑ HDMI External Digital I/O Connector for FPGA #1 (right side)

A close up of a device

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Figure ‑ HDMI External Digital I/O Connector for FPGA #2 (left side)

A close up of a white object

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Figure ‑ HDMI Connections at the FPGA

A screen shot of a computer

Description automatically generated

By using HDMI-to-HDMI cables, the 12 FPGA signals can be accessed on the test board. Each connector is wired to a wire-wrap pin in a header. Figure 8-4 shows the connectors and headers, and figure 8-5 shows which signals are accessible on which header pins. Wires must be added to the board to use any of the signals. Wires can connect to the test board’s single-ended to differential input buffers, differential to single-ended output buffers, differential clock sources, or to the other FPGA’s HDMI connector.

Figure ‑ HDMI Connectors and Signal Headers

Close-up of a circuit board

Description automatically generated

Figure ‑ HDMI Header Wiring

A diagram of a computer

Description automatically generated

The LEDs were supposed to light when a cable from the CM is installed and the CM is powered. Due to a logic error, the LED turn off in this situation.

# HDMI Single-ended to Differential Input Buffers

There are four channels of single-ended to differential buffers that are designated as “HDMI input buffers” (SMA connectors J53, J54, J55, and J56). Figure 9-1 shows the location of the buffers. Figure 9-2 shows the schematic of each channel.

All four channels have a two-pin header that allows one to terminate the SMA input with a 50 ohm resistor to ground (Headers J45, J46, J47, and J48). Install a 2-pin jumper to make this connection.

All four channels have a two-pin header that allows one to use wire-wrap wires to make a connection from the differential signal to a point elsewhere on the board (J37, J38, J39, and J40).

Figure ‑ HDMI Input Buffers

A close-up of a circuit board

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Figure ‑ HDMI Input Buffer Schematic (Channel 1 shown)A diagram of a computer

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# HDMI Differential to Single-ended Output Buffers

There are four channels of differential to single-ended buffers that are designated as “HDMI output buffers” (SMA connectors J49, J50, J51, and J52). Figure 10-1 shows the location of the buffers. Figure 10-2 shows the schematic of each channel.

All four channels provide a 100 ohm resistor to terminate the incoming LVDS signal.

All four channels have a two-pin header that allows one to utilize 33 ohms of “source-series termination” resistance in the SMA output for driving unterminated loads. (Headers J41, J42, J43, and J48=4). Install a 2-pin jumper to bypass the resistor.

All four channels have a two-pin header that allows one to use wire-wrap wires to make a connection to the differential signal to a point elsewhere on the board (J33, J34, J35, and J36).

Figure ‑ HDMI Output Buffers

A close-up of a circuit board

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Figure ‑ HDMI Output Buffer Schematic (Channel 1 shown)

A diagram of a circuit

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# Standard SM-to-CM Clocks

There are two clocks that connect to the CM through one of the “high speed” SM-to-CM connectors (P1). In a normal system, they will come from the ATCA backplane. One is the nominal 40 MHz “LHC CLOCK” and the other is the nominal 320 MHz “HQ CLOCK”. Each of these two clocks can be driven from an on-board oscillator, from an off-board source, or from elsewhere on the board. Figure 11-2 shows the schematic for one of the clocks.

The on-board oscillators that are currently installed are 40.0000 MHz and 320.0000 MHz.

Single-ended to differential input buffers are provided for connecting single-ended off-board sources (SMA connectors J29 and J30). The buffers have a two-pin header that allows one to terminate the SMA input with a 50 ohm resistor to ground. Install a 2-pin jumper to make this connection.

A 6-pin header (J14 or J15) is used to connect the desired source. A pair of 2-pin jumpers will source the clock from either the oscillator or the buffer. Figure 11-1 shows the jumpers installed to source the clocks from the oscillators. Alternatively, wire-wrap wires can be used to route a differential signal from elsewhere on the board, or from off-board.

Figure ‑ Standard Clocks from Oscillators

A close-up of a circuit board

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Figure ‑ Standard ATCA Clock Source

A diagram of a computer

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# CM Front Panel Clocks

There are two clocks that connect to the CM’s clock network through connectors on the front panel. Each of these two clocks can be connected from the test board with a USB 2.0 MINI-B cable, driven from an on-board oscillator, from an off-board source, or from elsewhere on the board. The CM front panel “F1\_CLK” connector (left side of figure 12-1) feeds the “REFCLK\_R0” network, while the “F2\_CLK” connector (right side of figure 12-2) feeds the “REFCLK\_R1” network.

Figure ‑ F1\_CLK Connector (left side of picture)

A close up of a device

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Figure ‑ F2\_CLK Connector (right side of picture)

A close up of a white object

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The on-board oscillators that are currently installed are 40.0000 MHz in FP\_CLK\_2 and 320.0000 MHz in FP\_CLK\_1.

Single-ended to differential input buffers are provided for connecting single-ended off-board sources (SMA connectors J16 and J17). The buffers have a two-pin header that allows one to terminate the SMA input with a 50 ohm resistor to ground. Install a 2-pin jumper to make this connection.

A 6-pin header (J4 or J5) is used to connect the desired source. A pair of 2-pin jumpers will source the clock from either the oscillator or the buffer. Figure 12-3 shows the jumpers installed to source the clocks from the buffers. Alternatively, wire-wrap wires can be used to route a differential signal from elsewhere on the board, or from off-board.

A schematic of one channel is shown in figure 12-4.

Figure ‑ Front Panel Clocks from SMA Connectors

Close-up of a circuit board

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Figure ‑ Front Panel Clock Schematic

A close-up of a circuit diagram

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# CM C2C and TCDS Loopback Connections

Two C2C (Chip-to-Chip) links and one TCDS link from FPGA #1 are connected to high speed connector P1. Two C2C (Chip-to-Chip) links and one TCDS link from FPGA #2 are connected to high speed connector P2.

For circuit testing, all six links have the transmit pairs looped back to the receive pairs through 0.1 uf capacitors. At each connector, two capacitors are on the top side of the board and four capacitors are on the bottom side.

Figure ‑ P1 Top Loopback Capacitors

A close up of a circuit board

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Figure ‑ P1 Bottom Loopback Capacitors

A close up of a circuit board

Description automatically generated

Figure ‑ P2 Top Loopback Capacitors

A close up of a circuit board

Description automatically generated

Figure ‑ P2 Bottom Loopback Capacitors

A green circuit board with many small holes

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# CM C2C FireFly Connections

The C2C links can be connected to the FireFly socket on the test board. This is done by removing the capacitors C2, C4, C39, and C41 from the P1 connector. Remove capacitors C3, C5, C40, and C42 from the P2 connector. Install eight zero-ohm resistors at each connector; four on the top side and four on the bottom side.

The TCDS links cannot be used for anything other than a signal loopback on the test board. Do not remove capacitors C43, C44, C45, and C46.

Install a 4-lane 25 Gb/s FireFly transceiver in the FireFly socket (figure 14-1). The I2C port on the FireFly can be accessed from a Linux system through the “IPMC I2C” header (figure 14-2). This must be used if the firefly is to operate in any way other than the default mode. One will probably need to turn off CDR and run the FireFly at 10 Gb/s.

Figure ‑ FireFly Socket

A close up of a circuit board

Description automatically generated

Figure ‑ I2C Connection for FireFly

A diagram of a circuit

Description automatically generated