Apollo CMv3 FPGA for Production Testing

Each FPGA needs to be programmed to support specific board testing functions. The specific needs are documented here. It may require multiple “bit” files to provide complete test coverage.

Associated Files

Many files are found on github at https://github.com/apollo-lhc/Cornell_CM_Rev3_HW . Documents related to testing are found in the “BoardTesting” directory.

Standalone Test Board vs. Service Module (SM)

The 6089-129_CM_TESTBOARD has been designed to exercise the CM on the benchtop without using an SM. The schematic is in the “BoardTesting” directory.

The test board can be used for low-power FPGA tests. There is insufficient cooling for tests that involve significant power consumption, such as the heater tests.

1 Overview of the FPGA specs

One or more FPGA programs will support testing the following board functions.

1.1 FPGA JTAG programming

The first firmware loaded into the FPGAs will also confirm the functionality of the FPGA JTAG chain. Both FPGAs will be programmed.

1.2 FPGA FLASH programming and FPGA booting from FLASH

The firmware can be programmed into the FLASH memory to confirm the programming ability. MCU signals can be manipulated to confirm that the FPGAs can boot from FLASH. The MCU can drive “FPGA_CFG_FROM_FLASH”, “F1_CFG_START, and “F2_CFG_START”. The MCU will read “/Fn_CFG_DONE” and “/Fn_INSTALLED”.

1.3 Testing of specific MCU signals

Several signals between the MCU and the FPGAs can be tested by having the FPGA loop specific input signals to output signals. The MCU can toggle the input signals and verify that it sees changes on the output signals. The FPGA inputs are “MCU_to_Fn” (n = 1 or 2). The FPGA outputs are “Fn_TO_MCU” and “Fn_C2C_OK”

1.4 Testing of front panel I/O connections

The signals between the FPGAs and the front panel I/O connector can be tested by using a cable from the front panel to the standalone test board. Specific jumper wires can be installed on the test board to support the testing scheme.

1.5 MCU-to-FPGA I2C Communication

Each FPGA has two I2C links with the MCU. The FPGAs can be configured as slaves. The MCU can confirm that it can communicate over all 4 I2C links.

1.6 Distribution of REFCLK and Logic Clock signals

Test configurations can be loaded into the clock synthesizers. Frequency counters in the FPGAs can report the clock frequency seen on each clock input.

1.7 Eye diagrams for GTY links

Operating configurations can be loaded into the clock synthesizers. Eye diagrams can be collected for each GTY link by using loopback connections.

1.8 High current power supply operation and thermal performance

Heater code can be loaded into the FPGAs and the operation of the power supplies at high current can be tested. The effectiveness of the cooling for the FPGAs, and possibly the FireFlys, can be verified.

2 Distribution of REFCLK and Logic Clock signals

Each FPGA has 28 REFCLK inputs, 6 logic clock inputs, one clock input on “spare_in[2]” from the other FPGA, and one input from a 200 MHz oscillator. Each FPGA will need 35 frequency counters to test the clock distribution. The 200 MHz oscillator will be used as a reference to gate the frequency counters. It is also sent to the other FPGA on “spare_out[2]”. The spare pair cross-connect is used to check the 200 MHz oscillators.

A method to read out the frequency counters needs to be developed (I2C?).

A set of clock synthesizer configuration files have been developed for this test. They attempt to generate as many unique frequencies as possible. Tables of expected frequencies are provided for each test step.

Eight of the clocks generated from the R0A and R0B synthesizers are fanned out to multiple destinations (see schematic sheet 2.08 REFCLK R0 FANOUT). These are noted in the tables with a number in the “A/B Switch” column. The information in the “A/B Switch” column tells which I2C register output in Table 1 (schematic sheet 4.03: I2C CLOCK CONTROL) controls switching the source between R0A and R0B.

Table 1 Switching clock source between R0A and R0B

A/B Switch	Signal	IC	Bit #
1	F1L_X12_R0_SEL	U88	P00
2	F1L_X4_R0_SEL	U88	P01
3	F1R_X12_R0_SEL	U88	P02
4	F1R_X4_R0_SEL	U88	P03
5	F2L_X12_R0_SEL	U83	P00
6	F2L_X4_R0_SEL	U83	P01
7	F2R_X12_R0_SEL	U83	P02
8	F2R_X4_R0_SEL	U83	P03

2.1 Load the "Step 1" configuration files into each synthesizer

The "Step 1" set of configuration files are: R0Av3X01, R0Bv3X01, R1Av3X01, R1Bv3X01, and R1Cv3X01. All of these are free running, using the attached 48 MHz crystal.

2.2 Load the test code into the FPGA

2.3 Verify the frequency of each clock

Read the frequency counters from each FPGA. Confirm that the values for each FPGA match the expected frequencies from Table 2 (GTY REFCLKs) and Table 3 (Logic Clocks). Change the source for some clocks from R0A to R0B and reverify. If it is easy, switch signals in table 1 one at a time and do verification. Otherwise, switch all eight controls and do a single verification.

Table 2 Step #1 Frequencies for REFCLK inputs

Quad #	Quad Letter	Ref #	Vivado Constraints Name		FPGA #1 A/B Switch	FPGA #1 Source	FPGA #1 Freq		FPGA #2 A/B Switch	FPGA #2 Source	FPGA #2 Freq
120	AB	R0	lf_r0_ab			R1A-0A	60			R1A-0	40
120	AB	R1	lf_r1_ab			R1B-0	220			R1B-1	110
122	AD	R0	lf_r0_ad		1	R0A/B-2	300/290		5	R0A/B-6	260/250
122	AD	R1	lf_r1_ad			R1B-2	132			R1B-6	148
124	AF	R0	lf_r0_af		2	R0A/B-3	150/145		6	R0A/B-7	130/125
124	AF	R1	lf_r1_af			R1A-4	168			R1A-6	156
126	R	R0	lf_r0_r		1	R0A/B-2	300/290		5	R0A/B-6	260/250
126	R	R1	lf_r1_r			R1B-3	296			F1B-7	268
129	U	R0	lf_r0_u		1	R0A/B-2	300/290		5	R0A/B-6	260/250
129	U	R1	lf_r1_u			R1B-0A	176			R1B-5	326
131	W	R0	lf_r0_w		2	R0A/B-3	150/145		6	R0A/B-7	130/125
131	W	R1	lf_r1_w			R1A-3	312			R1A-5	336
133	Y	R0	lf_r0_y		1	R0A/B-2	300/290		5	R0A/B-6	260/250
133	Y	R1	lf_r1_y			R1B-4	163			R1B-8	134
220	L	R0	rt_r0_l			OSC	200			OSC	200
220	L	R1	rt_r1_l			R1A-7	272			R1A-8	136
222	N	R0	rt_r0_n		3	R0A/B-1	160/155		7	R0A/B-0	320/310
222	N	R1	rt_r1_n			R1C-4	170			R1C-5	340
224	P	R0	rt_r0_p		4	R0A/B-4	280/270		8	R0A/B-5	140/135
224	P	R1	rt_r1_p			R1C-0A	116			R1C-9	226
226	B	R0	rt_r0_b		3	R0A/B-1	160/155		7	R0A/B-0	320/310
226	B	R1	rt_r1_b			R1C-6	155			R1C-3	310
229	E	R0	rt_r0_e		3	R0A/B-1	160/155		7	R0A/B-0	320/310
229	E	R1	rt_r1_e			R1C-7	286			R1C-2	348
231	G	R0	rt_r0_g		4	R0A/B-4	280/270		8	R0A/B-5	140/135
231	G	R1	rt_r1_g			R1C-8	143			R1C-0	232
233	I	R0	rt_r0_i		3	R0A/B-1	160/155		7	R0A/B-0	320/310
233	I	R1	rt_r1_i			R1C-9A	113			R1C-1	174

Table 3 Step #1 Frequencies for Logic Clock inputs

					FPGA #1				FPGA #2	
Logic Clock Name (schematic)	Logic Clock Name (constraint file)	Logic Clock Pins		A/B Switch	Source	Freq		A/B Switch	Source	Freq
FnL_X12_R0_CLK	lf_x12_r0_clk	P33/P34		1	R0A/B-2	300/290		5	R0A/B-6	260/250
FnL_X4_R0_CLK	lf_x4_r0_clk	N32/M32		2	R0A/B-3	150/145		6	R0A/B-7	130/125
FnR_X12_R0_CLK	rt_x12_r0_clk	R18/R17		3	R0A/B-1	160/155		7	R0A/B-0	320/310
FnR_X4_R0_CLK	rt_x4_r0_clk	N19/N18		4	R0A/B-4	280/270		8	R0A/B-5	140/135
Fn_TCDS40_CLK	tcds40_clk	BF27/BF28			R1B-9	55			R1B-9	55
LHC_CLK	lhc_clk	BE26/BE27			SM	40			SM	40
FnFmSPARE2	in_spare[2]	C29/C30			FPGA#2	200			FPGA#1	200

2.4 Test clock inputs to synth R0B

2.4.1 Input IN_0 from synth R0A with R0Bv3X02

Leave the I2C switching on schematic 2.08 in the mode to use synth R0B for the FPGA clock sources. Leave (or reload) synth R0A with R0Av3X01. Load configuration file R0Bv3X02 into synth R0B. This will cause synth R0B to use the 240 MHz signal that comes from OUT_8 on R0A as its input. Since the output connections of synth R0B have already been checked, this configuration file sets all FPGA clocks at 240 MHz and only one of them needs to be checked. It also enables the feedback input to use the 240 MHz signal from OUT_9A.

2.4.2 (optional) Input IN_1 from front panel connector with R0Bv3X03

Install a cable from the “FP CLK 1” connector on the test board to the front panel “F1 EXT CLK” connector. Configure the test board so that the 320 MHz oscillator is driving the cable.

Leave the I2C switching on schematic 2.08 in the mode to use synth R0B for the FPGA clock sources. Load configuration file R0Bv3X03 into synth R0B. This will cause synth R0B to use the signal from the front panel “F1 EXT CLK” connector as its input. Since the output connections of synth R0B have already been checked, this configuration file sets all FPGA clocks at 320 MHz. It also enables the feedback input to use the 320 MHz signal from OUT_9A.

2.4.3 Input IN_2 from backplane LHC CLK with R0Bv3X04

Leave the I2C switching on schematic 2.08 in the mode to use synth R0B for the FPGA clock sources. Leave (or reload) synth R0A with R0Av3X01. Load configuration file R0Bv3X04 into synth R0B. This will cause synth R0B to use the 40 MHz signal that comes from the SM connector “LHC CLK” as its input. Since the output connections of synth R0B have already been checked, this configuration file sets all FPGA clocks at 200 MHz and only one of them needs to be checked. It also enables the feedback input to use the 40 MHz signal from OUT_9A.

2.5 Test clock inputs to synth R0A

2.5.1 Input IN_1 from synth R0B with R0Av3X02

Change the I2C switching on schematic 2.08 to the mode to use synth R0A for the FPGA clock sources. Load synth R0B with R0Bv3X01. Load configuration file R0Av3X02 into synth R0A. This will cause synth R0A to use the 230 MHz signal that comes from OUT_8 on R0B as its input. Since the output connections of synth R0A have already been checked, this configuration file sets all FPGA clocks at 230 MHz and only one of them needs to be checked. It also enables the feedback input to use the 230 MHz signal from OUT_9A.

Additional test steps will be added here. Many will require loading new configuration files in some synthesizers. Briefly:

1) test various inputs on R1A, R1B, and R1C. Consider using I2C controls to change inputs. It may save a few reconfigurations.