THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE. ON ANY PAGE, THE NUMBER OF THE CONNECTING PAGE(S) IS SHOWN IN A SMALL NUMBER BELOW THE SIGNAL NAME. PAGE NUMBERS CAN BE FOUND IN SMALL TYPE AT THE BOTTOM OF THE TITLE BLOCK.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY. THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: OFF-BOARD SIGNALS (SM AND FRONT PANEL), GLOBAL CLOCKING, C2C AND TCDS
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: FPGA#1 POWER AND SIGNAL (NON-MGT)
6: FPGA#2 POWER AND SIGNAL (NON-MGT)
7: FPGA#1 GTY TRANSCEIVERS FOR FIREFLY
8: FPGA#2 GTY TRANSCEIVERS FOR FIREFLY
9: BETWEEN-FPGA GTY TRANSCEIVERS
9.99: MECHANICAL PARTS
These are some general signal naming conventions:

1) Signals connected to the FPGAs contain either "F1" or "F2".

2) Signals connected to the Service Module contain "SM".

3) Signals connected to the Front Panel contain "FP".

4) Signal names starting with “PG” are “Power Good” signals from power modules.

5) Signal names starting with “EN” are “Enable” signals to turn on power modules.

6) GTY reference clock names indicate FPGA followed by side (F1L, F1R, F2L, F2R), then the reference clock (R0 or R1), finishing with the sequence order (1 thru 7).

7) Power source names start with "V_", then the voltage with the letter "V" as a decimal point. (V_3V3 is a 3.3 volt source)

8) The MCU I/Os are 3.3 volt and the FPGA I/Os are 1.8 volt. Level shifters are used for the conversion. Signal names on the FPGA side are prefaced with "lov" (low voltage) and signals on the MCU side are prefaced with "hiv" (high voltage).

Make JPG pictures for the block diagrams by displaying them in a PowerPoint slide show that fills the screen. Do a "print screen", then paste it in "paint". Crop, save file, and insert picture.

TO DO:

Consider making page numbers larger

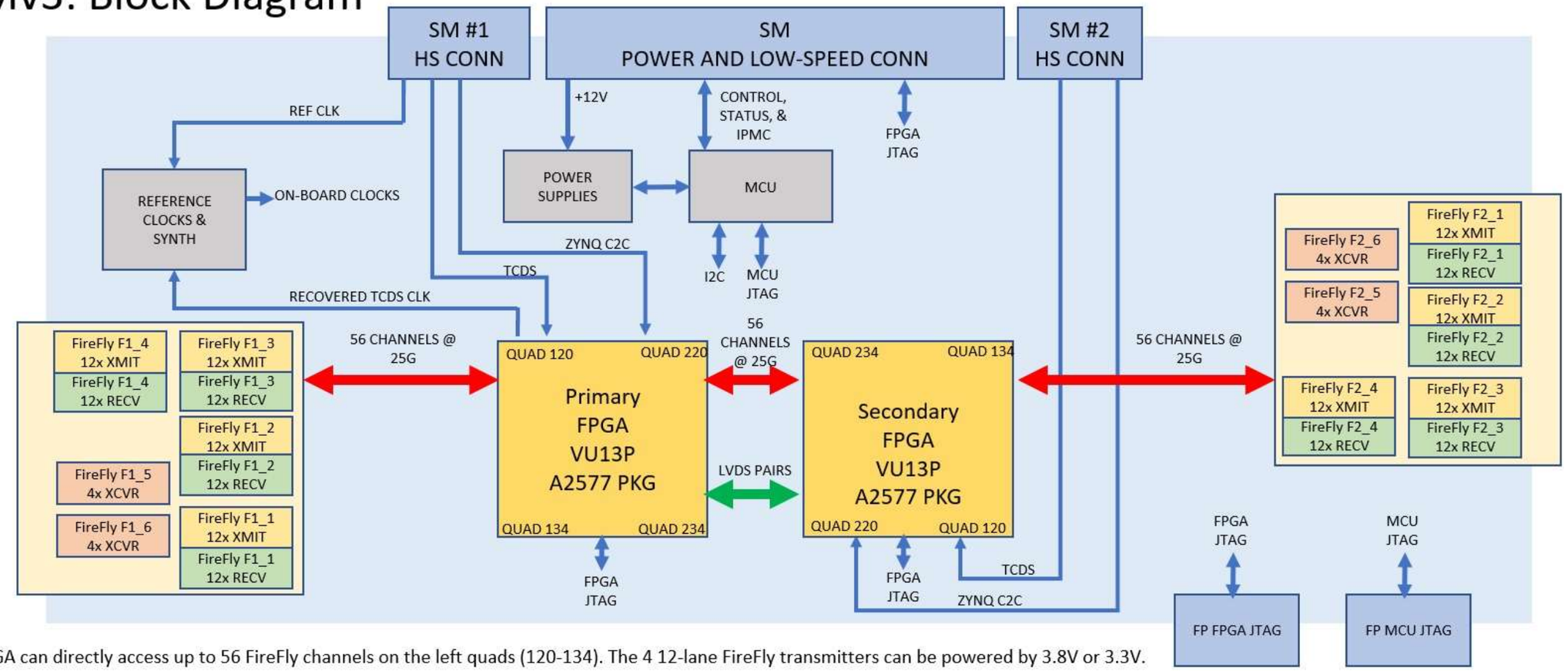
Update MCU code with new scale factor for 12V current reading

Update MCU code to accomodate reassigned pins on I2C register chips

Make design notes on the 5 synth pages match

APOLLO CM v3		
Title: 1.01: NOTES		
Size	Document Number: 6089-127	Rev: A
Date: Monday, November 04, 2024	Sheet 1 of 81	

Apollo CMv3: Block Diagram

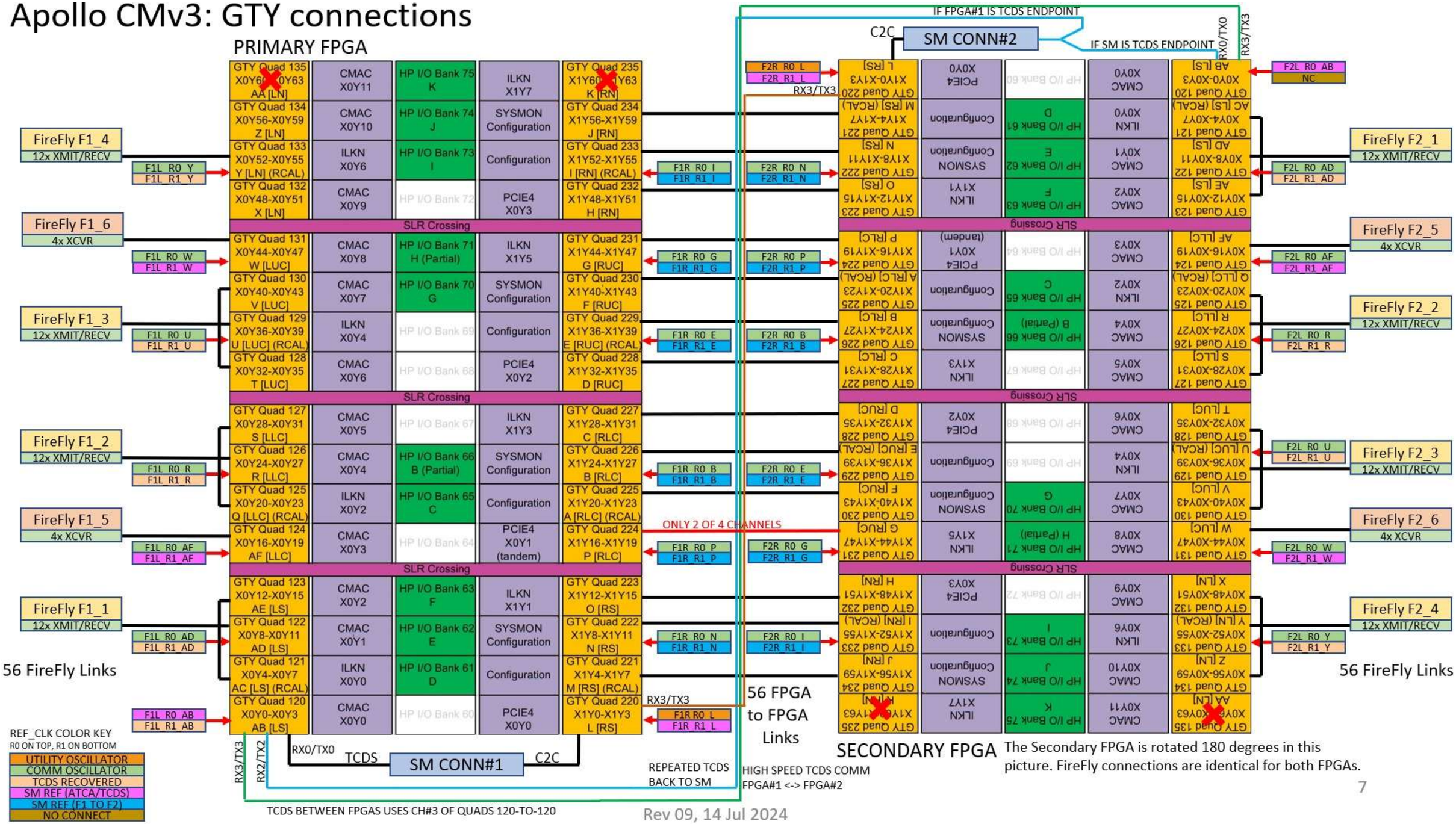


- Each FPGA can directly access up to 56 FireFly channels on the left quads (120-134). The 4 12-lane FireFly transmitters can be powered by 3.8V or 3.3V.
- 56 GTY links are provided between the FPGA sites on the right quads (220-234). These are AC-coupled.
- Other I/O:
  - 2 GTY links for chip-to-chip (or PCI) from each FPGA to the Zynq on the SM (Service Module).
  - 1 GTY link for TCDS from each FPGA to the SM
  - 1 GTY link for TCDS support between FPGAs
  - 6 LVDS pairs between the FPGA sites.
  - 5 LVDS pairs plus 2 single-ended wires from each FPGA site to front panel HDMI-style connectors. For diagnostics or unforeseen I/O needs.
  - 4 LVDS pairs plus 2 single-ended wires from each FPGA site to a 20-pin 1-mm pitch header on the bottom side of the board.
- The MCU and the FPGAs have independent JTAG chains. The FPGA JTAG chain can be accessed from the SM or from the front panel. The MCU JTAG only has front panel access. The MCU code can be changed from an SM serial port.
- The recovered TCDS clock is only available from the primary FPGA.

Rev 09, 14 Jul 2024

APOLLO CM v3		
Title: 1.02: BLOCK DIAGRAM		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 2 of 81	

Apollo CMv3: GTY connections



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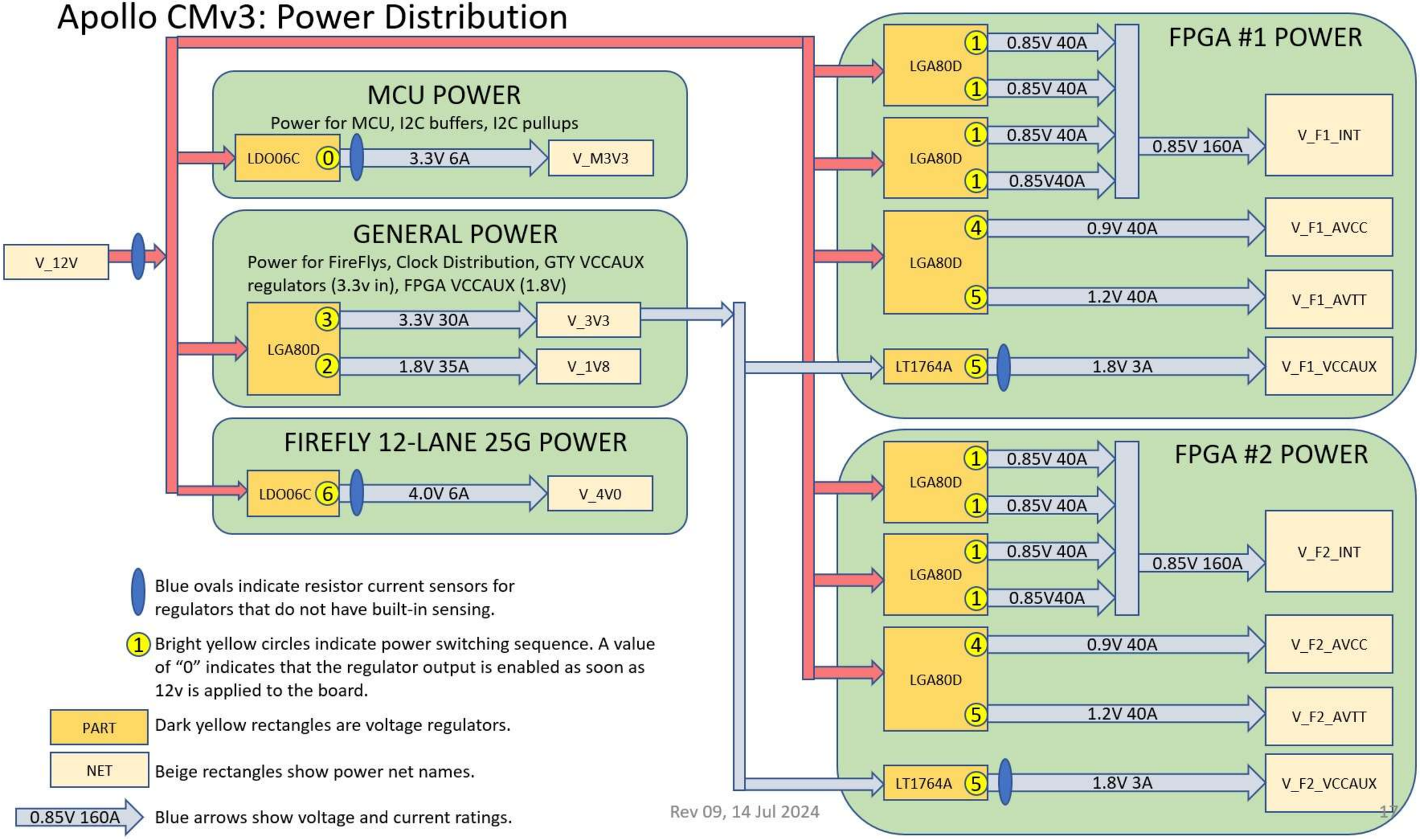
Rev 09, 14 Jul 2024

APOLLO CM v3			
Title: 1.03: GTY CONNECTIONS			
Size	Document Number: 6089-127		Rev: A
Date: Wednesday, October 16, 2024	Sheet 3 of 81		

Apollo CMv3: Power Distribution



Blue ovals indicate resistor current sensors for regulators that do not have built-in sensing.

(1) Bright yellow circles indicate power switching sequence. A value of "0" indicates that the regulator output is enabled as soon as 12v is applied to the board.

PART — Dark yellow rectangles are voltage regulators.

NET — Beige rectangles show power net names.

0.85V 160A — Blue arrows show voltage and current ratings.

APOLLO CM v3		
Title: 1.04: POWER		
Size	Document Number: 6089-127	Rev: A
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Apollo CMv3: Utility Clock / Reference Clock 0 (R0) Distribution

XTAL OSC
SI510
200.000000

200 MHZ CLOCKS ARE UTILITY CLOCKS FOR THE FPGA LOGIC AND REFERENCE CLOCKS FOR THE SM C2C LINKS

CLK_0, CLK_1 → SI53340 → O_0: F1_UTIL_CLK; O_1: F2_UTIL_CLK; O_2: F1R_R0_L; O_3: F2R_R0_L

XTAL 48MHz → OSC

SYN_R0_SA_IN1 → IN_1

SYNTH "R0A" SI5395A

IN_0, IN_2, FB

O_0A, O_0: F2R_X12_R0_SA; O_1: F1R_X12_R0_SA; O_2: F1L_X12_R0_SA; O_3: F1L_X4_R0_SA; O_4: F1R_X4_R0_SA; O_5: F2R_X4_R0_SA; O_6: F2L_X12_R0_SA; O_7: F2L_X4_R0_SA; O_8: SYN_R0_SB_IN0; O_9, O_9A

THE GREEN ARROWS SHOW THAT THE SYNTHESIZERS ARE CROSS-CONNECTED. ALL R0 CLOCKS CAN COME FROM THE SAME SOURCE.

XTAL 48MHz → OSC

SYN_R0_SB_IN0 → IN_0

R0_FP_CLK → IN_1

LHC_CLK 40 MHz ATCA BKPL → SM CONN #1 → (f) 40 MHZ FROM 1:6 BUFFER → IN_2

SYNTH "R0B" SI5395A

IN_3/FB

O_0A, O_0: F2R_X4_R0_SB; O_1: F2R_X12_R0_SB; O_2: F1R_X4_R0_SB; O_3: F1R_X12_R0_SB; O_4: F1L_X4_R0_SB; O_5: F1L_X12_R0_SB; O_6: F2L_X12_R0_SB; O_7: F2L_X4_R0_SB; O_8: SYN_R0_SA_IN1; O_9, O_9A

THE REFERENCE CLOCK 0 SYNTHESIZER "B" CAN BE DRIVEN BY A LOCAL CRYSTAL, THE OUTPUT OF SYNTHESIZER "A", THE 40 MHZ LHC CLOCK FROM THE BACKPLANE, OR THE OPTIONAL FRONT PANEL CONNECTOR. THE LHC CLOCK WOULD BE USED FOR SYSTEM-WIDE SYNCHRONOUS COMMUNICATION.

FPGA #1

LEFT QUADS

12x FIREFLYS

F1L_X12_R0_SA, F1L_X12_R0_SB, F1L_X12_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F1L_R0_AD; Q1: F1L_R0_R; Q2: F1L_R0_Y; Q3: F1L_X12_R0_CLK; Q4: F1L_R0_U; Q5

4x FIREFLYS

F1L_X4_R0_SA, F1L_X4_R0_SB, F1L_X4_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F1L_X4_R0_CLK; Q1; Q2: F1L_R0_W; Q3: F1L_R0_AF; Q4; Q5

RIGHT QUADS

12x LINKS

F1R_X12_R0_SA, F1R_X12_R0_SB, F1R_X12_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F1R_R0_N; Q1: F1R_R0_B; Q2: F1R_R0_E; Q3: F1R_R0_I; Q4: F1R_X12_R0_CLK; Q5

4x LINKS

F1R_X4_R0_SA, F1R_X4_R0_SB, F1R_X4_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F1R_R0_P; Q1: F1R_R0_G; Q2: F1R_X4_R0_CLK; Q3; Q4; Q5

F1_UTIL_CLK, F1L_X12_R0_CLK, F1L_X4_R0_CLK, F1R_X12_R0_CLK, F1R_X4_R0_CLK → LOGIC

FPGA #2

LEFT QUADS

12x FIREFLYS

F2L_X12_R0_SA, F2L_X12_R0_SB, F2L_X12_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F2L_R0_Y; Q1: F2L_R0_R; Q2: F2L_R0_AD; Q3: F2L_X12_R0_CLK; Q4: F2L_R0_U; Q5

4x FIREFLYS

F2L_X4_R0_SA, F2L_X4_R0_SB, F2L_X4_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F2L_R0_AF; Q1; Q2: F2L_R0_W; Q3: F2L_X4_R0_CLK; Q4; Q5

RIGHT QUADS

12x LINKS

F2R_X12_R0_SA, F2R_X12_R0_SB, F2R_X12_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F2R_X12_R0_CLK; Q1: F2R_R0_I; Q2: F2R_R0_B; Q3: F2R_R0_E; Q4: F2R_R0_N; Q5

4x LINKS

F2R_X4_R0_SA, F2R_X4_R0_SB, F2R_X4_R0_SEL → CLK_0, CLK_1, SEL → SI53342 → Q0: F1R_X4_R0_CLK; Q1: F2R_R0_P; Q2: F2R_R0_G; Q3; Q4; Q5

F2_UTIL_CLK, F2L_X12_R0_CLK, F2L_X4_R0_CLK, F2R_X12_R0_CLK, F2R_X4_R0_CLK → LOGIC

APOLLO CM v3		
Title: 1.05: R0 SYNTH CLOCKS		
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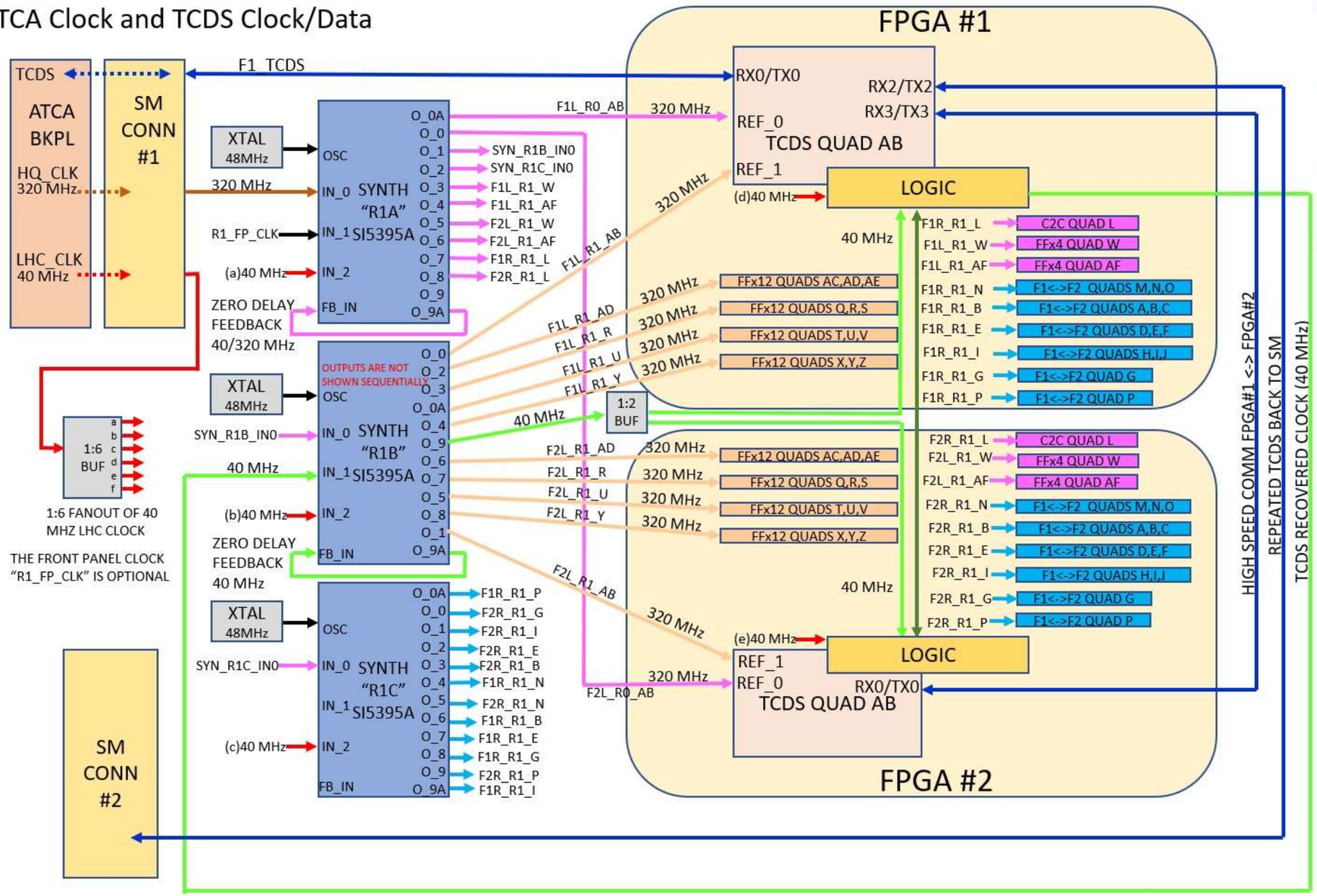
Apollo CMv3: External Clock Sources

ATCA Clock and TCDS Clock/Data



GBIT TCDS CLOCK/DATA COMBINED

LHC 40 MHz ATCA CLOCK

This is the 40 MHz clock passed from the ATCA backplane through the SM. It is fanned out through a 1:6 buffer. The frequency of this clock changes when the LHC is ramping.

LHC 320 MHz ATCA CLOCK

This is the 320 MHz clock passed from the ATCA backplane through the SM. The frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK

If the top synthesizer is using the clock on "IN_0", then these 320 MHz clocks all have zero phase offset relative to the incoming LHC REFERENCE CLOCK signal.

40 MHz TCDS RECOVERED CLOCK

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

FPGA TO FPGA R1 CLOCK

These clocks drive the R1 reference for the FPGA quads that connect to the other FPGA. The frequency follows the 320 MHz REF CLOCK.

TTC/TTS DATA/CONTROL

These signals possibly contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

OTHER CLOCKS

These include the front panel inputs and outputs of various crystal oscillators. These can be used for testing or for adding flexibility to the synthesizer outputs.

GTY QUADS

FFx12 QUADS	12-lane FireFlys. For the IT-DTC, these will be detector facing.
FFx4 QUADS	4-lane FireFlys.
F1<->F2 QUADS	Connections between the two FPGAs.
TCDS QUAD	Dedicated for TCDS function.

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APOLLO CM v3		
Title: 1.06: R1 SYNTH CLOCKS		
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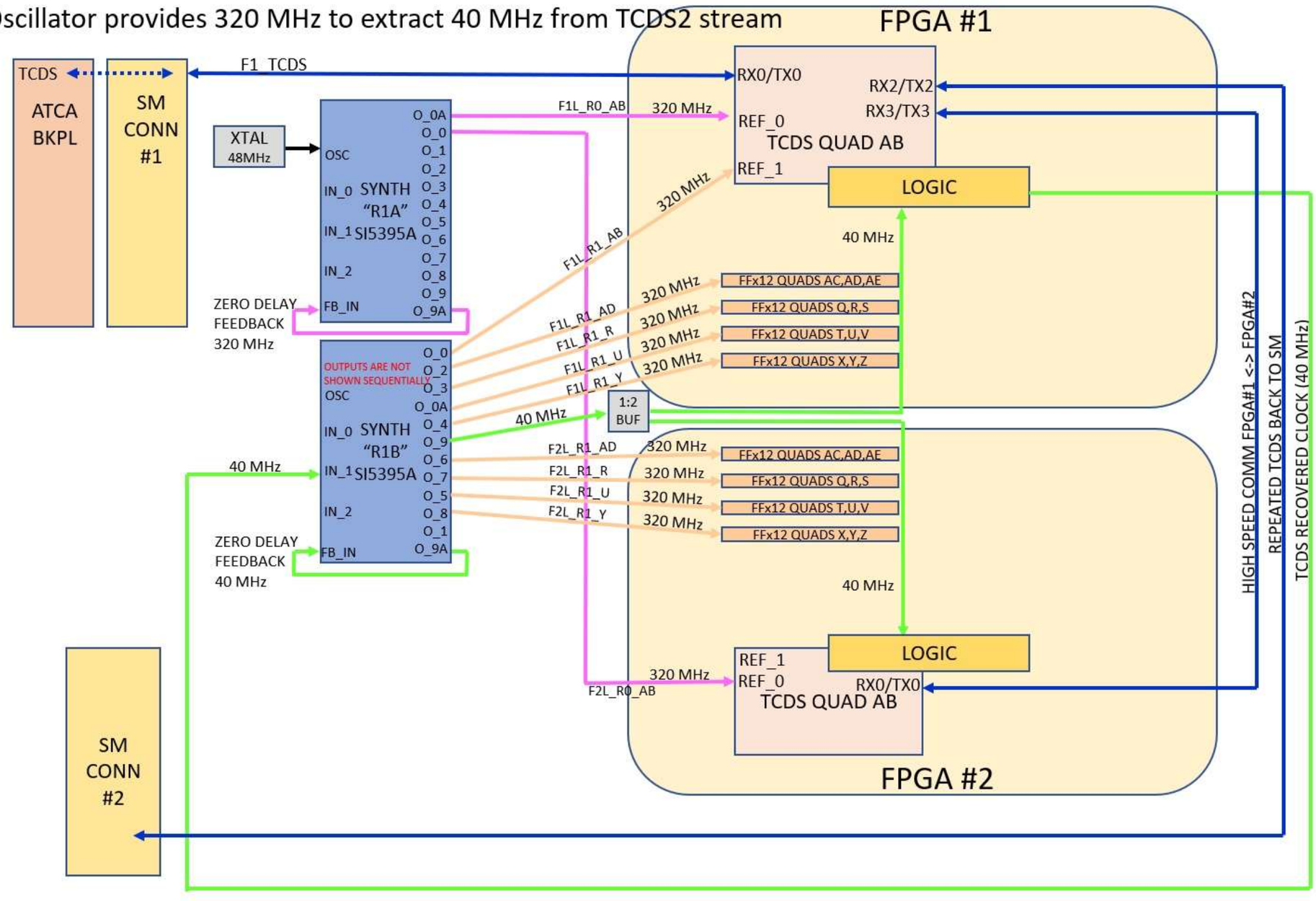
Apollo CMv3: Full TCDS2

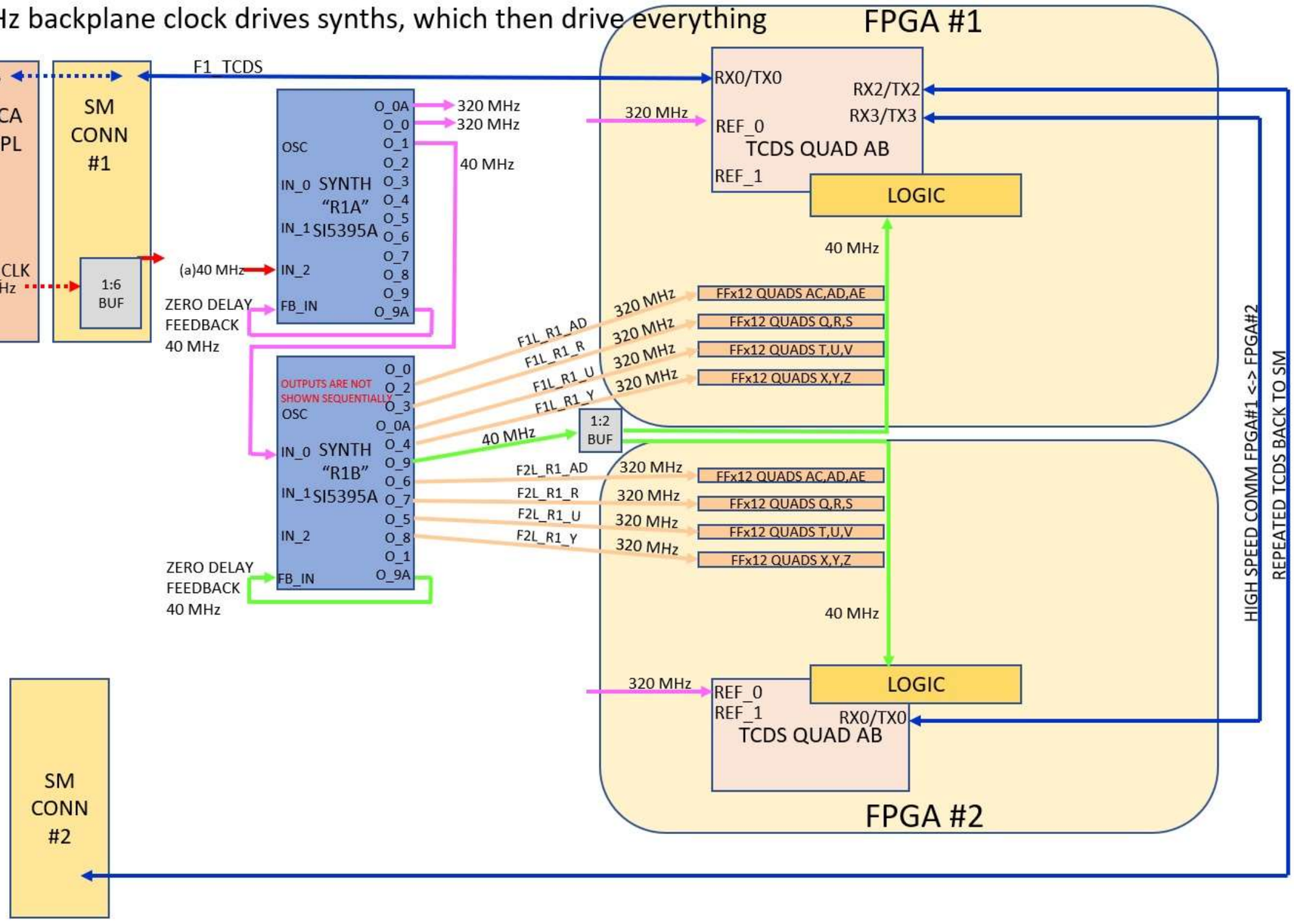
Oscillator provides 320 MHz to extract 40 MHz from TCDS2 stream



APOLLO CM v3			
Title: 1.07: TCDS FULL (SIMPLIFIED)			
Size	Document Number: 6089-127		Rev: A
Date: Wednesday, October 16, 2024	Sheet 7 of 81		

Apollo CMv3: Lightweight TCDS2 “A”

40 MHz backplane clock drives synths, which then drive everything



Rev 09, 14 Jul 2024

APOLLO CM v3		
Title: 1.08: TCDS LIGHTWEIGHT-A (SIMPLIFIED)		
Size	Document Number: 6089-127	Rev: A
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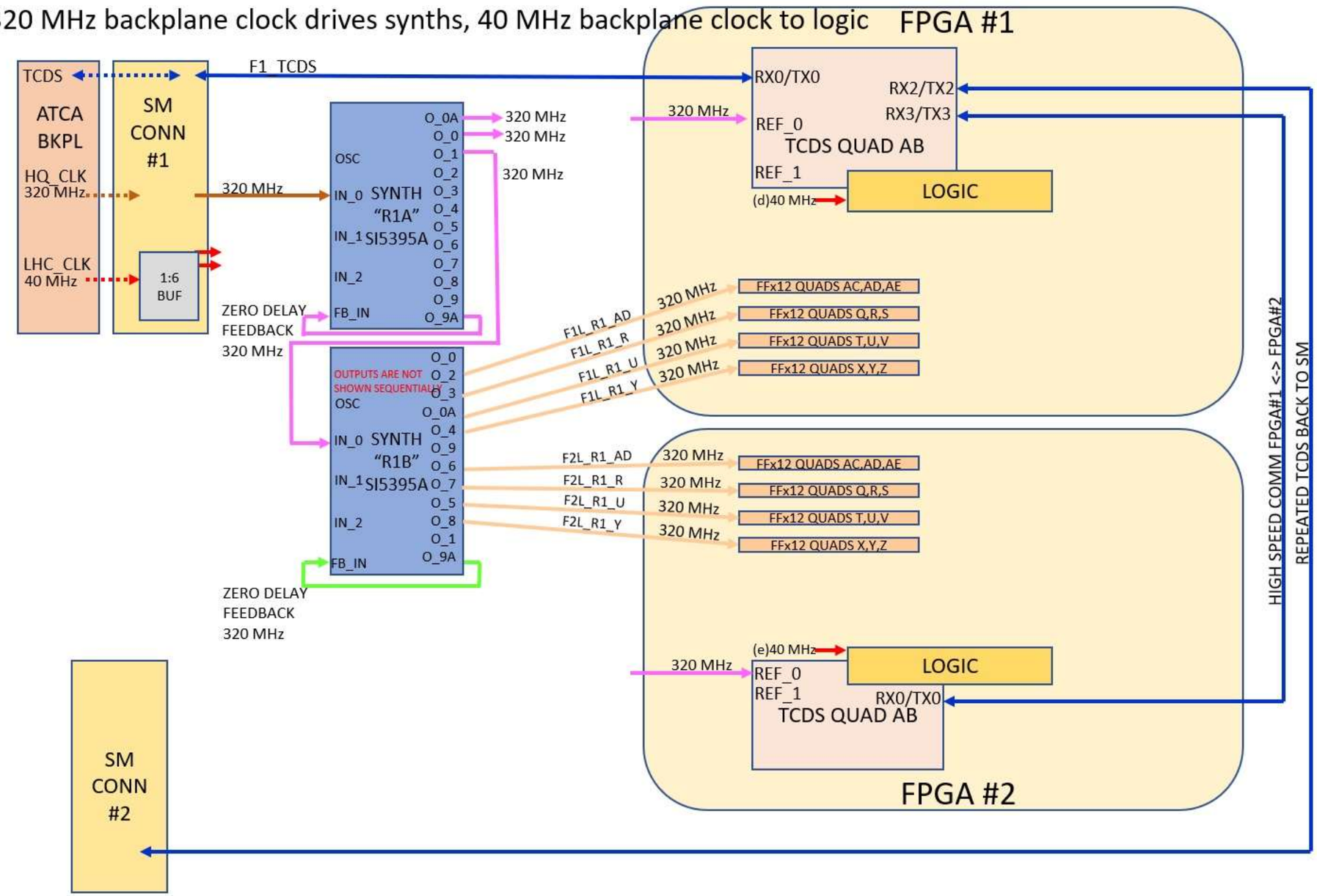
Apollo CMv3: Lightweight TCDS2 “B”

320 MHz backplane clock drives synths, 40 MHz backplane clock to logic



APOLLO CM v3		
Title: 1.09: TCDS LIGHTWEIGHT-B (SIMPLIFIED)		
Size	Document Number: 6089-127	Rev: A
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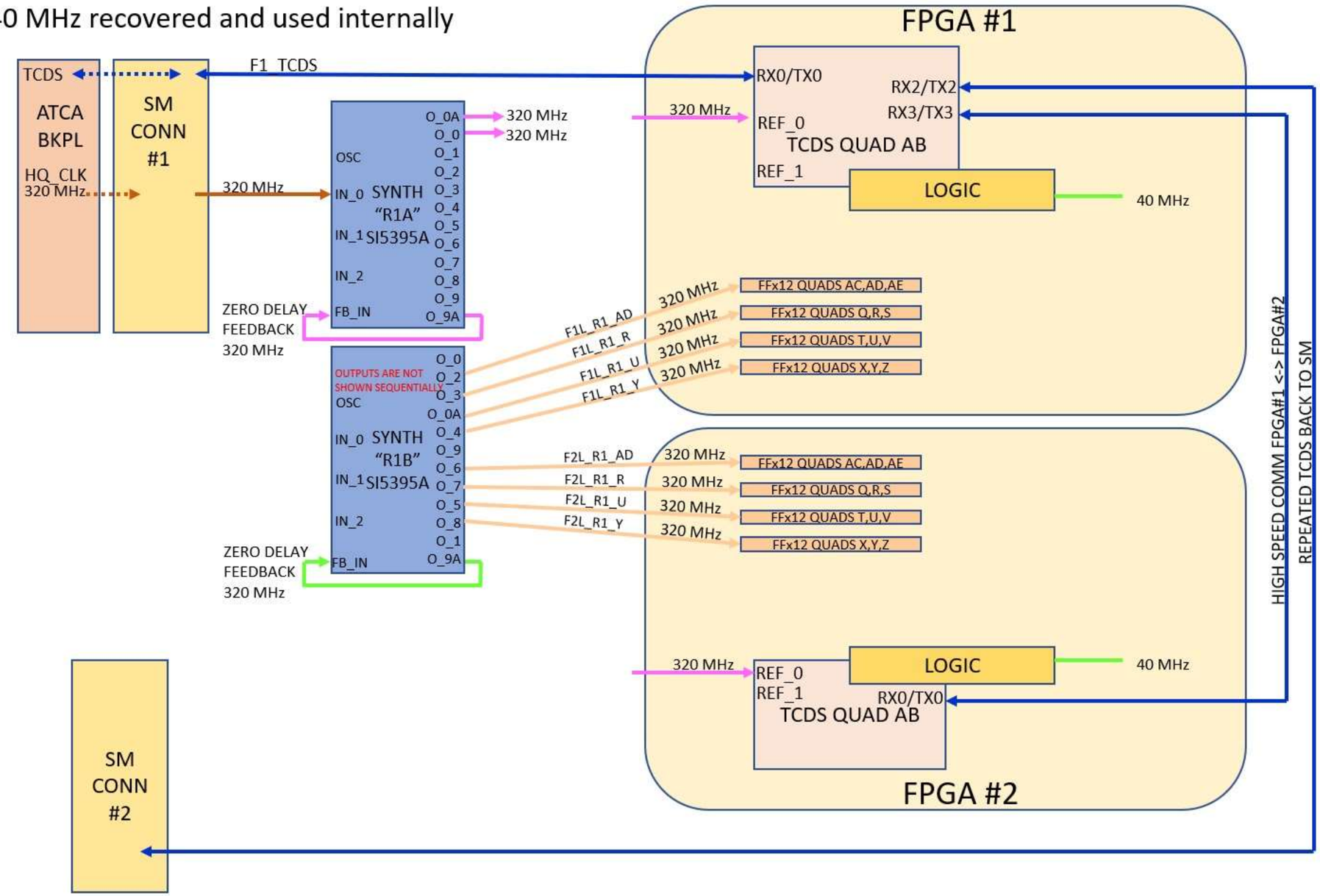
Apollo CMv3: Lightweight TCDS2 “C”

40 MHz recovered and used internally



APOLLO CM v3		
Title: 1.10: TCDS LIGHTWEIGHT-C (SIMPLIFIED)		
Size	Document Number: 6089-127	Rev: A
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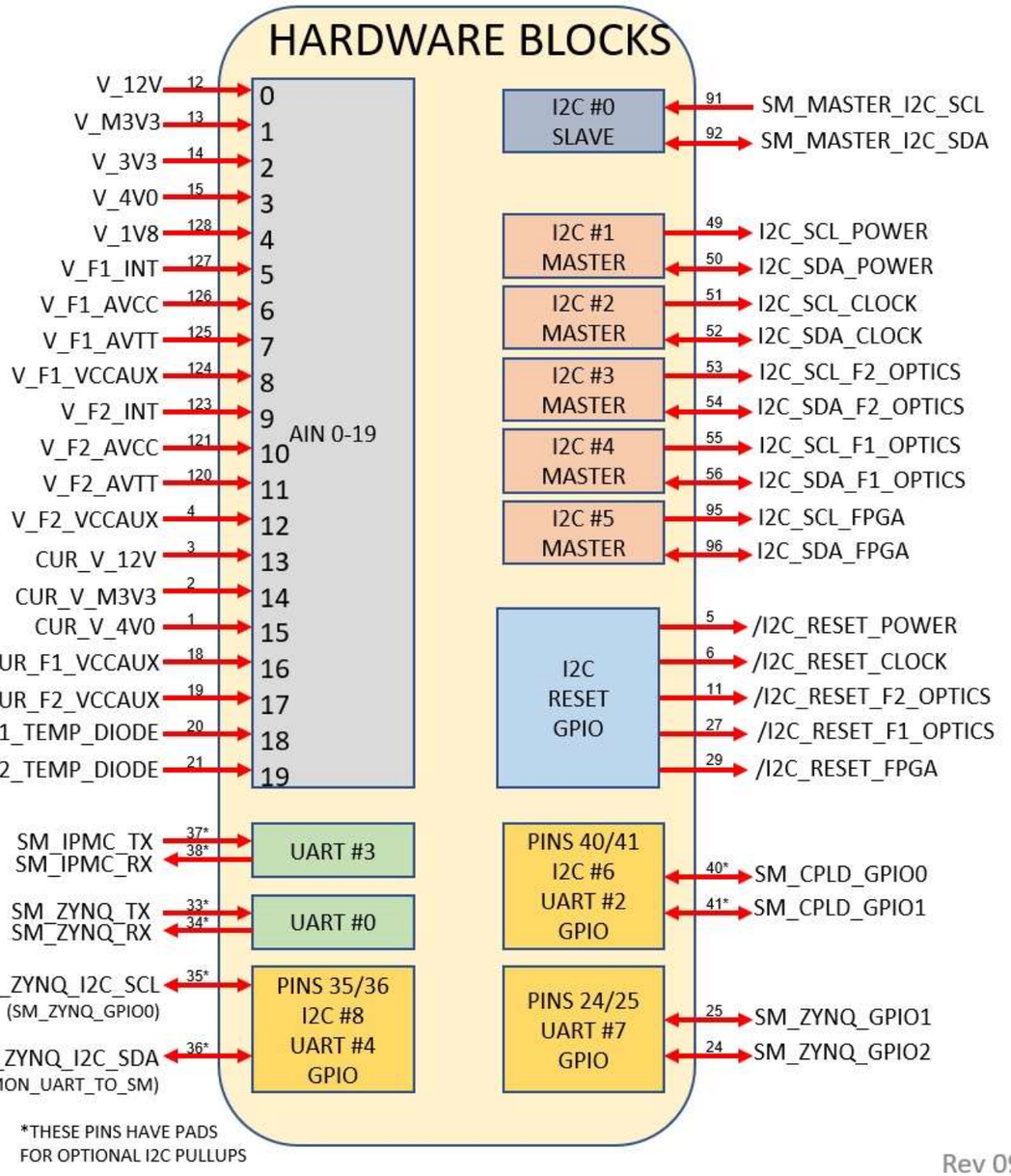
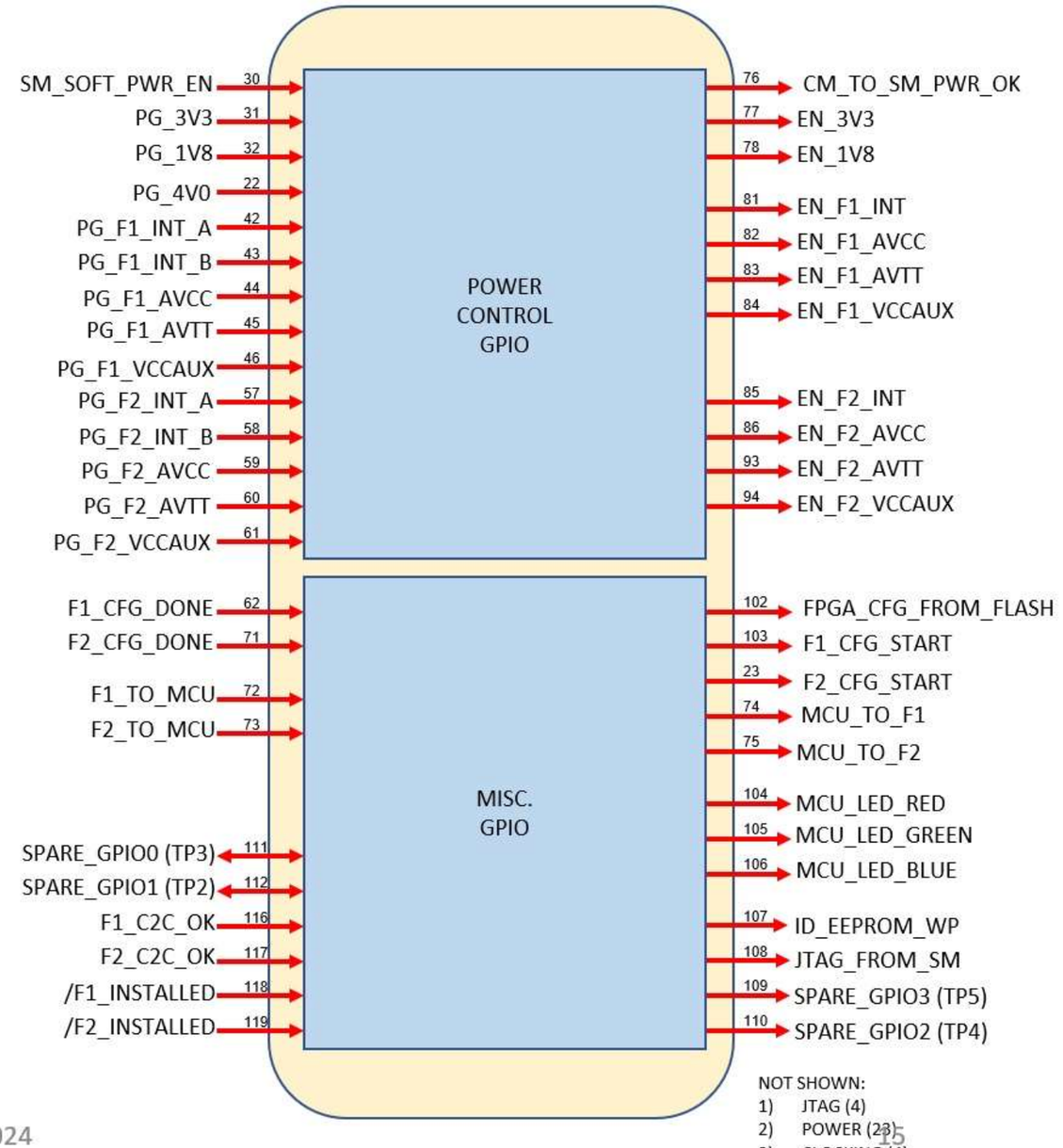
Apollo CMv3: MCU Connections and Internal Resources





NOT SHOWN:
1) JTAG (4)
2) POWER (23)
3) CLOCKING (4)
4) CONTROL (3)

Rev 09, 14 Jul 2024

APOLLO CM v3		
Title: 1.11: MCU I/O AND INTERNALS		
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2.01: SM POWER AND CONTROL CONNECTOR

THE "POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE MCU HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

POWER OK LED

THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 1 MILLIOHMS AND A CURRENT OF 30 AMPS WILL PRODUCE A VOLTAGE OF 30 MILLIVOLTS. THE SENSE AMPLIFIER HAS A GAIN OF 100, YIELDING 3.0 VOLTS AT 30 AMPS. THIS EQUALS 360 WATTS.

THIS DIVIDER FOLLOWING THE AMPLIFIER ALLOWS THE AMPLIFIER OUTPUT TO EXCEED THE 2.5 VOLT FULL-SCALE INPUT LIMIT OF THE MCU. WITH Rtop=2K AND Rbottom=10K, THE SCALE FACTOR NEEDED IN THE MCU IS 12.5 AMPS PER VOLT AND THE MAXIMUM CURRENT BEFORE SATURATION IS 30 AMPS (360 WATTS).

V_12V
R = 0.001 OHM
GAIN = 100 V/V
DIVIDER = 83%
SCALE = 12.5 AMPS PER VOLT

I2C0 IS A SLAVE INTERFACE. IT IS CONNECTED TO THE IPMC ON THE SM.

I2C8 CAN BE A MASTER OR A SLAVE. IT IS USED TO GET MONITORING DATA INTO THE ZYNQ. ON CMv1, THIS IS THE UART#4 PATH. IT IS CONNECTED TO THE ZYNQ ON THE SM.

I2C6 IS AVAILABLE FOR FUTURE USE. IT IS CONNECTED TO THE CPLD ON THE SM. PULLUPS ARE NOT INSTALLED.

THE I2C7 PINS ARE INITIALLY USED FOR UART#3 CONNECTIONS TO THE IPMC ON THE SM. PULLUPS ARE NOT INSTALLED.

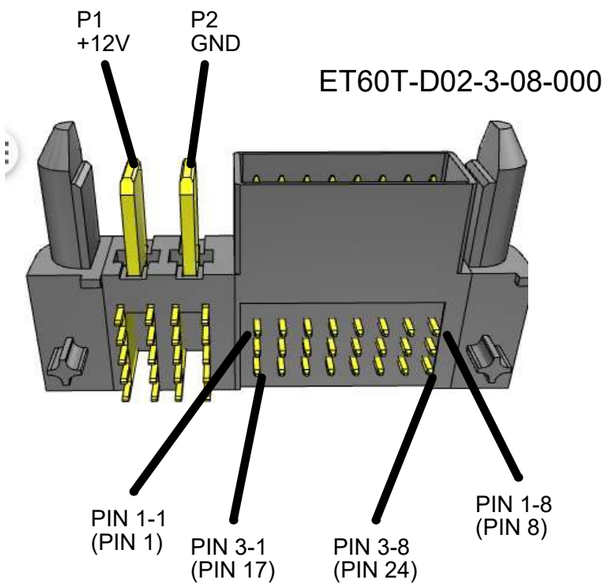
THE I2C9 PINS ARE INITIALLY USED FOR UART#0 CONNECTIONS TO THE ZYNQ ON THE SM.THIS PROVIDES A BOOTLOADER FUNCTION FOR THE MCU. PULLUPS ARE NOT INSTALLED.

IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH. IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

TM4C SLAVE I2C ADDR = 0X40

TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.

FOR STANDALONE USB-TO-UART CONNECTION, USE DIGIKEY 768-1015 (FTDI TTL-232R-3V3). CONNECT IT TO AN ADAPTER THAT PLUGS INTO CONNECTOR P1. USE PIN 5 (SM_ZYNQ_TX) AND PIN 21 (SM_ZYNG_RX).



THESE ARE THE SIGNAL NAMES ON THE SMv2

/PS_RST IS NOT USED IN THIS DESIGN

ZERO-OHM RESISTORS ON PIN 4 AND PIN 20 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES.

THE SAME IS TRUE FOR THE RESISTORS ON PIN 5 AND PIN 21.

IN ROW 2, PINS 1, 4, 6, AND 8 ARE "GND" ON SMv1. A CMv3 BOARD MUST BE ABLE TO TOLERATE A HARD GND CONNECTION ON THESE PINS IN CASE IT IS CONNECTED TO AN SMv1.

IF THE MCU IS DRIVING AN OUTPUT HIGH, AND THE SIGNAL IS SHORTED TO GND, A 270 OHM RESISTOR WILL LIMIT THE CURRENT TO 12 MA. THE RESISTOR POWER WILL BE 0.04 WATTS.

APOLLO CM v3			
Title: 2.01: SM POWER AND CONTROL CONNECTOR			
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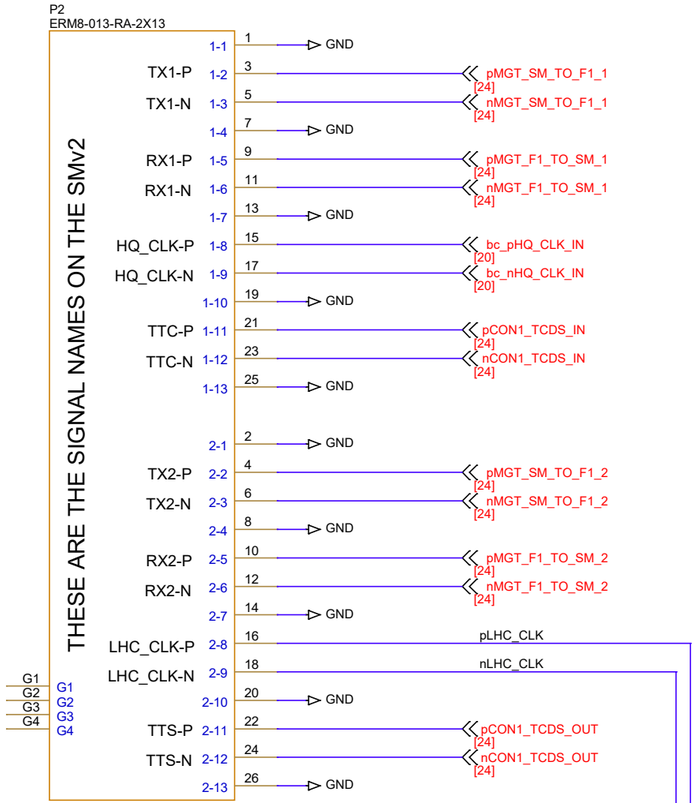
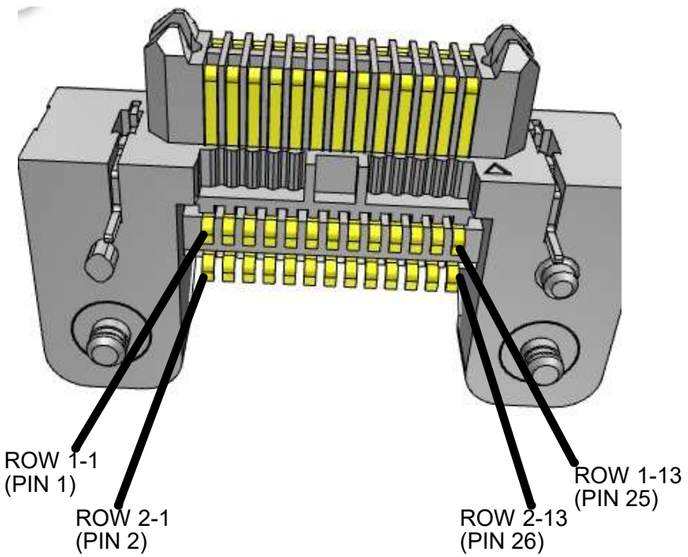
2.02: SM HIGH SPEED CONNECTORS

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. AC COUPLING CAPACITORS ARE ASSUMED TO BE ON THE SM.

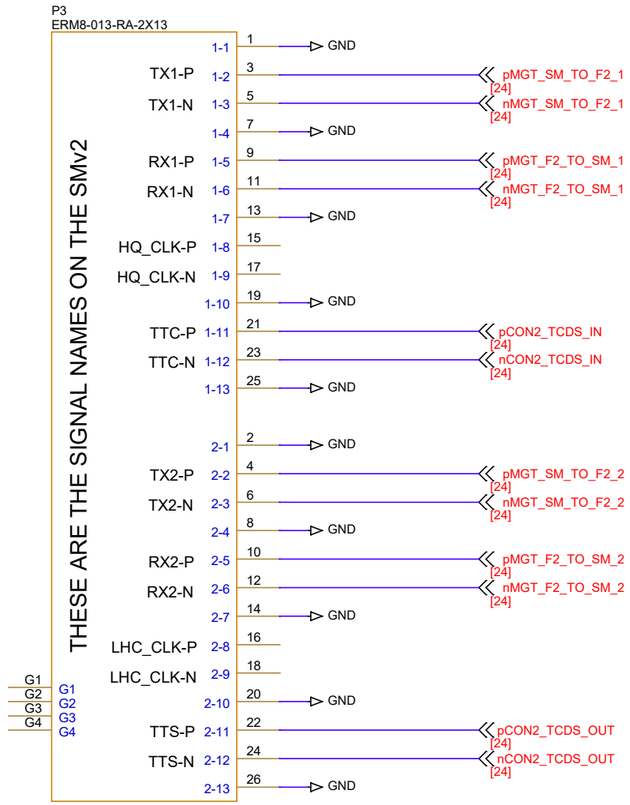
FPGA#1 AND BACKPLANE CLOCK SIGNALS



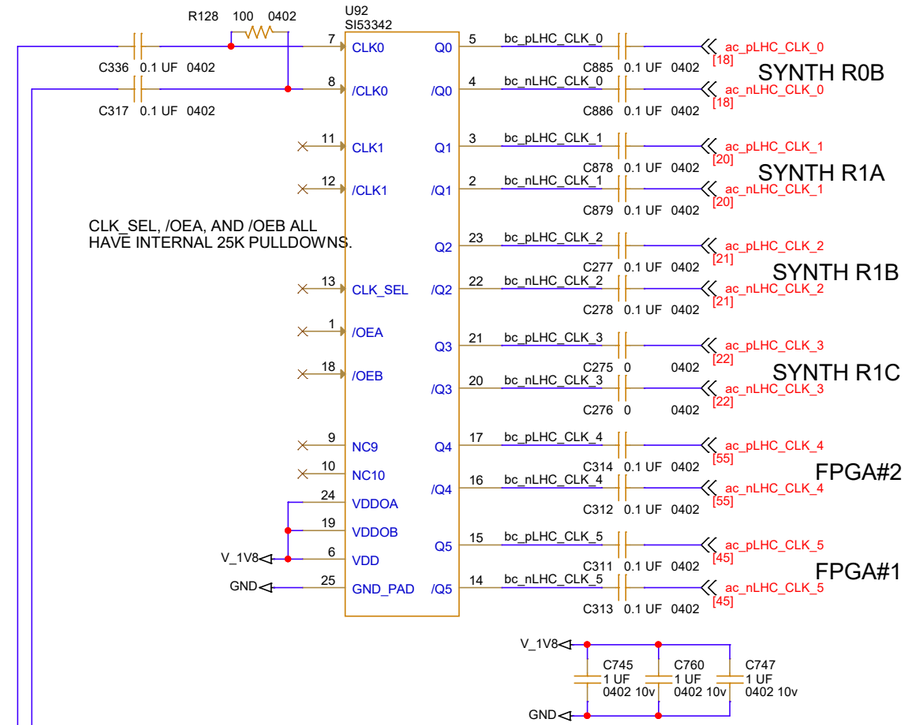


ERM8-013-01-L-D-RA-DS

FPGA#2 SIGNALS



40 MHZ LHC CLOCK FANOUT



APOLLO CM v3		
Title: 2.02: SM HIGH SPEED CONNECTORS		
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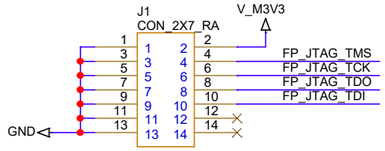
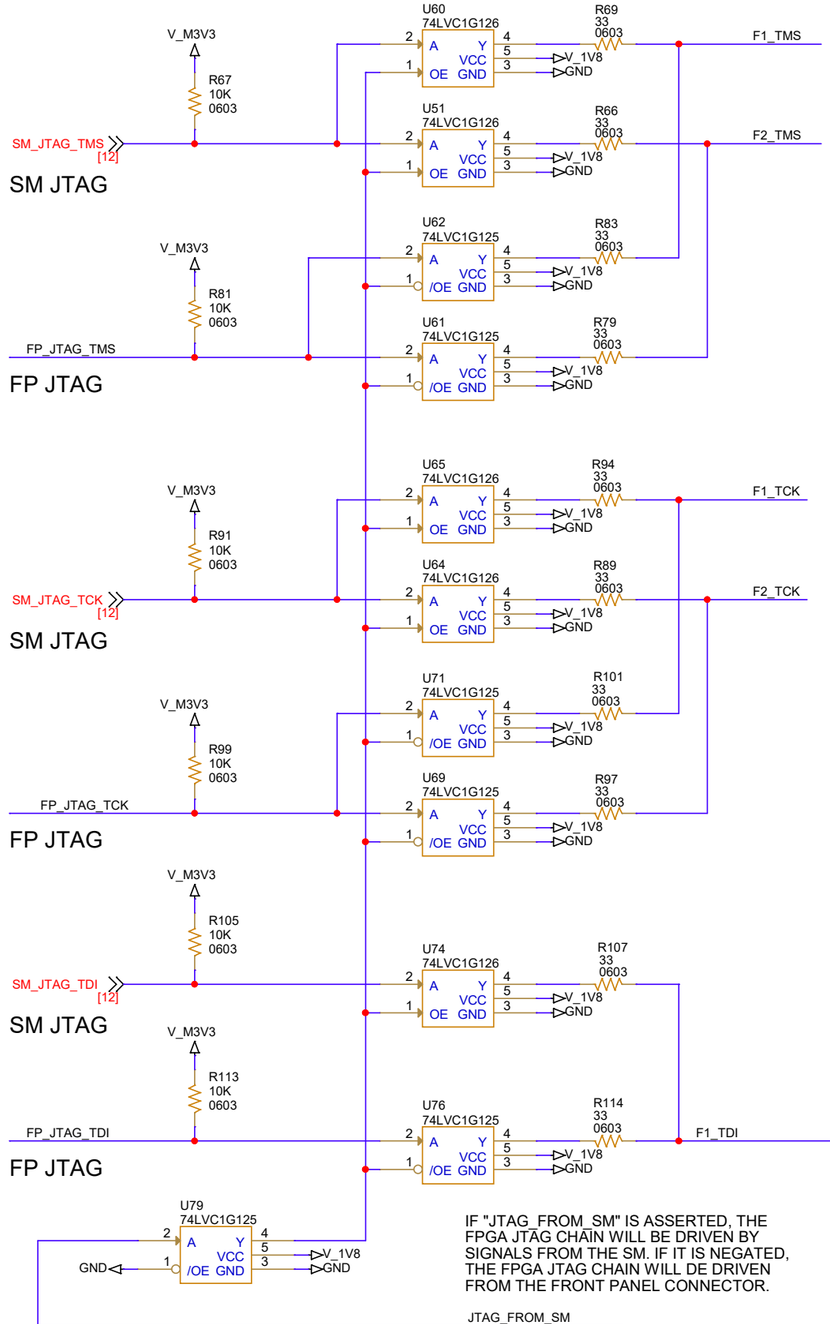
2.03: MCU AND FPGA JTAG

THE FPGA JTAG REFERENCE IS 3.3 VOLTS.



FRONT PANEL FPGA JTAG

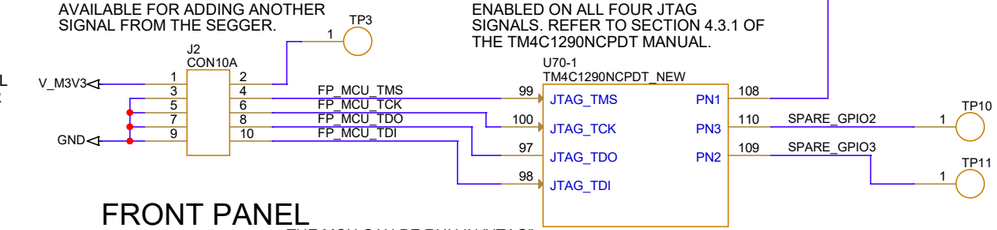


IF "JTAG_FROM_SM" IS ASSERTED, THE FPGA JTAG CHAIN WILL BE DRIVEN BY SIGNALS FROM THE SM. IF IT IS NEGATED, THE FPGA JTAG CHAIN WILL DE DRIVEN FROM THE FRONT PANEL CONNECTOR.

JTAG_FROM_SM

THE TEST POINT ON PIN 2 IS AVAILABLE FOR ADDING ANOTHER SIGNAL FROM THE SEGGER.

THE MCU HAS INTERNAL PULLUPS ENABLED ON ALL FOUR JTAG SIGNALS. REFER TO SECTION 4.3.1 OF THE TM4C1290NCPDT MANUAL.



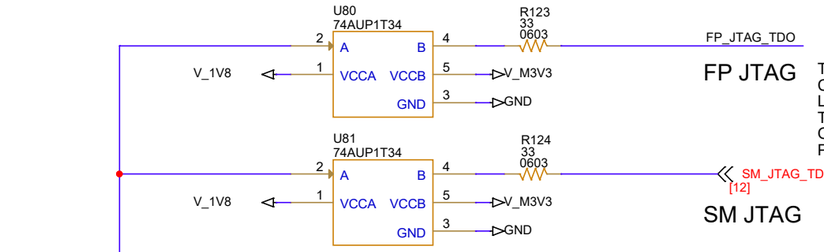
THE TEST POINTS ON PINS 109 AND 110 ARE AVAILABLE FOR DEBUGGING OR MEETING NEW REQUIREMENTS.

THE MCU CONNECTOR ON THE FRONT PANEL IS A 10-PIN 50-MIL PITCH CONNECTOR. A SEGGER MODEL 8.06.28 "50-MIL 10-PIN PATCH ADAPTER" IS USED AT THE PROGRAMMER.

THE MCU JTAG REFERENCE IS 3.3 VOLTS.

FRONT PANEL MCU JTAG

THE MCU CAN BE RUN IN "JTAG" MODE OR "ARM SWD" MODE.

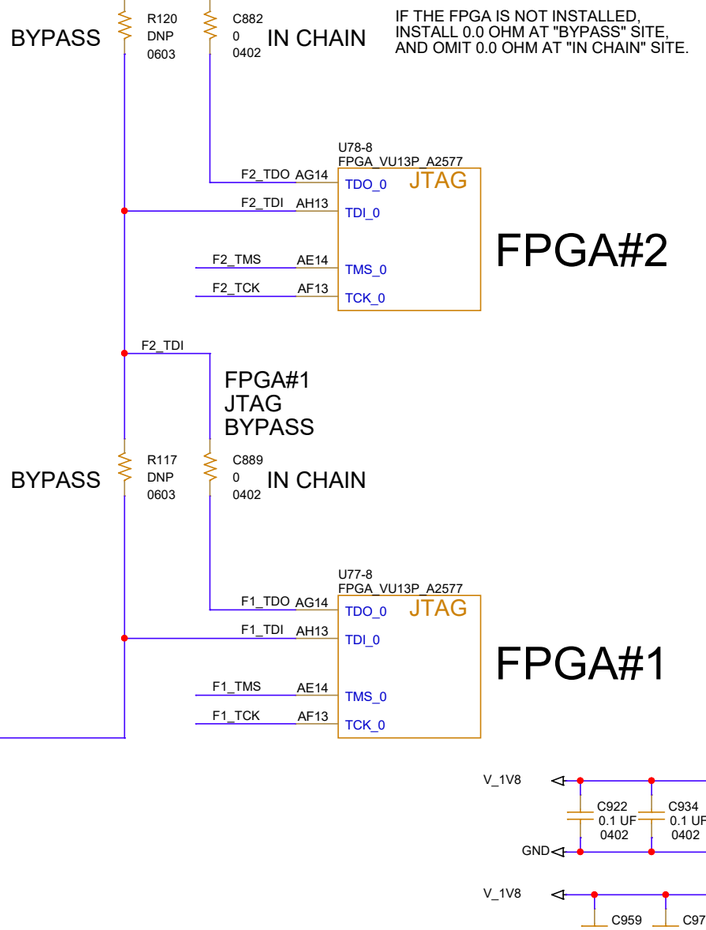


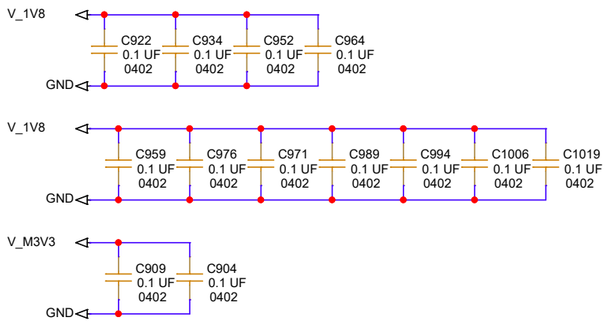
THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE SM OR THE EXTERNAL PROGRAMMER.

FPGA#2 JTAG BYPASS

IF THE FPGA IS INSTALLED AND PART OF THE JTAG CHAIN, INSTALL 0.0 OHM AT "IN CHAIN" SITE, AND OMIT 0.0 OHM AT "BYPASS" SITE.

IF THE FPGA IS NOT INSTALLED, INSTALL 0.0 OHM AT "BYPASS" SITE, AND OMIT 0.0 OHM AT "IN CHAIN" SITE.





APOLLO CM v3		
Title: 2.03: MCU AND FPGA JTAG		
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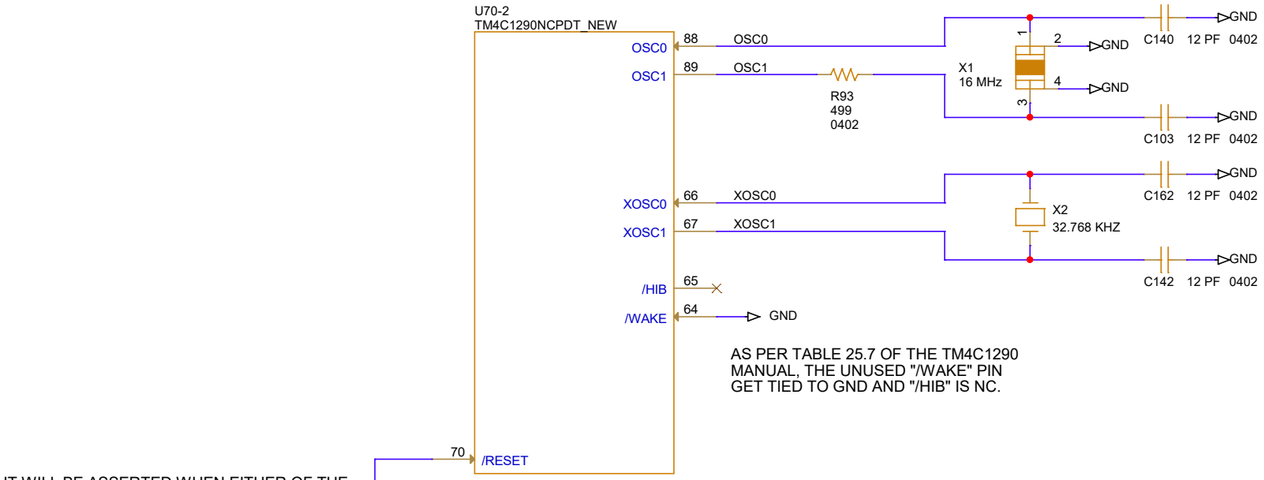
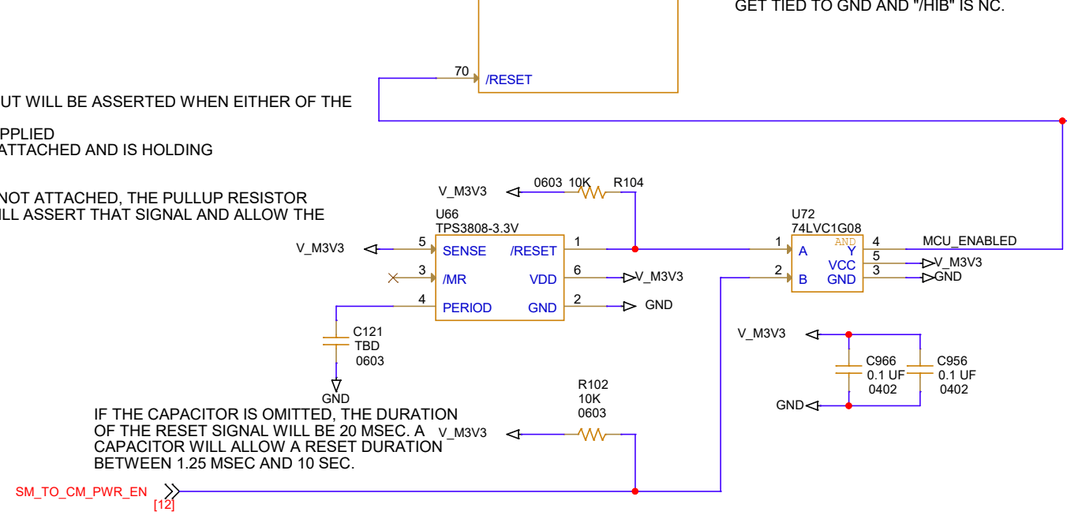
2.04: MCU I/O AND POWER

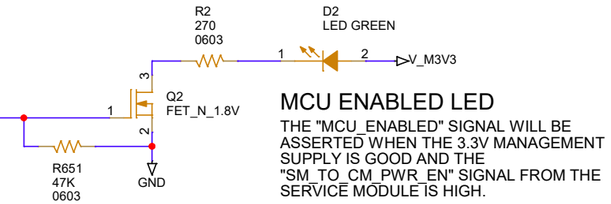


AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "/WAKE" PIN GET TIED TO GND AND "/HIB" IS NC.

THE ACTIVE-LO "/RESET" INPUT WILL BE ASSERTED WHEN EITHER OF THE FOLLOWING ARE TRUE:
1) POWER HAS JUST BEEN APPLIED
2) THE SERVICE MODULE IS ATTACHED AND IS HOLDING "SM_TO_CM_PWR_EN" LO.

IF THE SERVICE MODULE IS NOT ATTACHED, THE PULLUP RESISTOR ON"SM_TO_CM_PWR_EN" WILL ASSERT THAT SIGNAL AND ALLOW THE BOARD TO POWER UP.

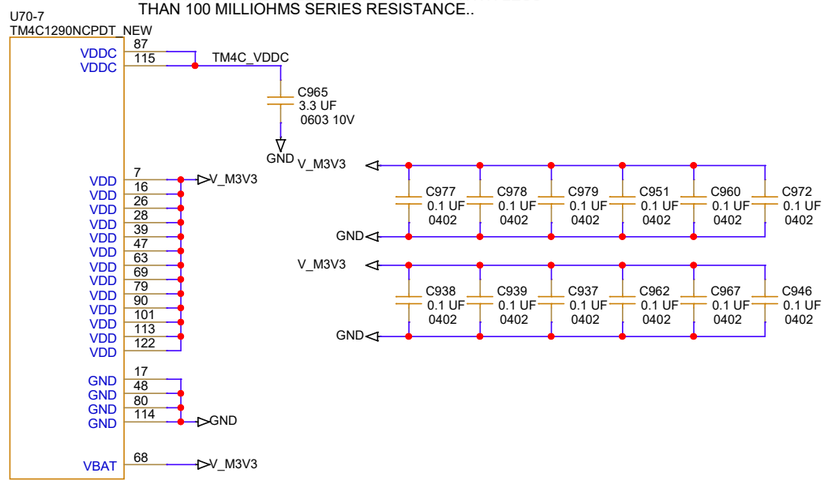




MCU ENABLED LED

THE "MCU_ENABLED" SIGNAL WILL BE ASSERTED WHEN THE 3.3V MANAGEMENT SUPPLY IS GOOD AND THE "SM_TO_CM_PWR_EN" SIGNAL FROM THE SERVICE MODULE IS HIGH.

AS PER TABLE 26.15 OF THE TM4C1290 MANUAL, THE "VDDC" PINS GET TIED TOGETHER AND CONNECTED TO A CAPACITOR BETWEEN 2.5 UF AND 4 UF WITH LESS THAN 100 MILLIOHMS SERIES RESISTANCE..



AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "VBAT" PIN GET TIED TO VDD.

APOLLO CM v3		
Title: 2.04: MCU I/O AND POWER		
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2.05: UTILITY CLOCK

THE POLARITY IS SWAPPED TO SIMPLIFY BOARD LAYOUT.

R106 DNP 0603
R109 DNP 0603
R112 DNP 0603
R115 DNP 0603
V_1V8
GND

U75
SI510_200P0000
OE1 CLK+
OE2 CLK-
VDD
GND

bc_nUTIL
bc_pUTIL
ac_nUTIL
ac_pUTIL
C197 0.1 UF 0402
C198 0.1 UF 0402

C932 0.1 UF 0402

THIS OSCILLATOR HAS A STANDARD VALUE OF 200.0000 MHZ AND AN LVDS OUTPUT.
INITIAL P/N 510BBA200M000AAG

THE LAST "A" IN "BBA" INDICATES THAT THE OUTPUT ENABLE IS ON PIN 1 AND IS ACTIVE-HI. THE DEVICE CLAIMS TO HAVE AN INTERNAL PULLUP ON PIN 1. RESISTOR PADS ARE PROVIDED IN CASE SOMETHING DIFFERENT IS NEEDED.

R121
100
0402

U82
SI53340
CLK0 Q0
/CLK0 /Q0
CLK1 Q1
/CLK1 /Q1
NC8 Q2
CLK_SEL /Q2
Q3
/QE
VDD
GND PAD

THE "CLK_SEL" PIN HAS AN INTERNAL PULL-DOWN RESISTOR.

bc_pUTIL_0
bc_nUTIL_0
bc_pUTIL_1
bc_nUTIL_1
bc_pUTIL_2
bc_nUTIL_2
bc_pUTIL_3
bc_nUTIL_3

C242 0 0402
C241 0 0402
C240 0.1 UF 0402
C239 0.1 UF 0402
C238 0.1 UF 0402
C237 0.1 UF 0402
C236 0 0402
C235 0 0402

ac_pF2_XTAL_200 [56]
ac_nF2_XTAL_200 [56]
ac_pF1R_R0_L [24]
ac_nF1R_R0_L [24]
ac_pF2R_R0_L [24]
ac_nF2R_R0_L [24]
ac_pF1_XTAL_200 [46]
ac_nF1_XTAL_200 [46]

F2 LOGIC
F1 QUAD L
F2 QUAD L
F1 LOGIC

C910 1 UF 0402 10v

THESE CLOCKS DRIVE THE FPGA QUADS USED FOR UTILITY FUNCTIONS, LIKE THE C2C LINK TO THE SM. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC. THE LOGIC CLOCKS ARE DC-COUPLED, WITH ZERO-OHM RESISTORS ON THE CAPACITOR PADS.

APOLLO CM v3		
Title: 2.05: UTILITY CLOCK		
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2.06: REFCLK SYNTHESIZER R0A

U86-1
SI5395

X3
48 MHz

pXTAL_R0A → XA (8)
X1_SHIELD (7)
X2_SHIELD (10)
nXTAL_R0A → XB (9)

OUT_0A (21) /OUT_0A (20)

IN_0 (63) /IN_0 (64)
IN_1 (1) /IN_1 (2)
IN_2 (14) /IN_2 (15)

R345
100
0402

bc_pSYN_R0A_IN1 [18] — C881 0.1 UF 0402 — ac_pSYN_R0A_IN1
bc_nSYN_R0A_IN1 [18] — C917 0.1 UF 0402 — ac_nSYN_R0A_IN1

FROM SYNTH
"R0_B"

OUT_0 (24)	bc_pR0A_0	C326 0.1 UF 0402	ac_pF2R_X12_R0A [19]	F2 R0 RIGHT QUADS 12X FIREFLYS
/OUT_0 (23)	bc_nR0A_0	C327 0.1 UF 0402	ac_nF2R_X12_R0A [19]	
OUT_1 (28)	bc_pR0A_1	C377 0.1 UF 0402	ac_pF1R_X12_R0A [19]	F1 R0 RIGHT QUADS 12X FIREFLYS
/OUT_1 (27)	bc_nR0A_1	C378 0.1 UF 0402	ac_nF1R_X12_R0A [19]	
OUT_2 (31)	bc_pR0A_2	C324 0.1 UF 0402	ac_pF1L_X12_R0A [19]	F1 R0 LEFT QUADS 12X FIREFLYS
/OUT_2 (30)	bc_nR0A_2	C325 0.1 UF 0402	ac_nF1L_X12_R0A [19]	
OUT_3 (35)	bc_pR0A_3	C375 0.1 UF 0402	ac_pF1L_X4_R0A [19]	F1 R0 LEFT QUADS 4X FIREFLYS
/OUT_3 (34)	bc_nR0A_3	C376 0.1 UF 0402	ac_nF1L_X4_R0A [19]	
OUT_4 (38)	bc_pR0A_4	C322 0.1 UF 0402	ac_pF1R_X4_R0A [19]	F1 R0 RIGHT QUADS 4X FIREFLYS
/OUT_4 (37)	bc_nR0A_4	C323 0.1 UF 0402	ac_nF1R_X4_R0A [19]	
OUT_5 (42)	bc_pR0A_5	C373 0.1 UF 0402	ac_pF2R_X4_R0A [19]	F2 R0 RIGHT QUADS 4X FIREFLYS
/OUT_5 (41)	bc_nR0A_5	C374 0.1 UF 0402	ac_nF2R_X4_R0A [19]	
OUT_6 (45)	bc_pR0A_6	C320 0.1 UF 0402	ac_pF2L_X12_R0A [19]	F2 R0 LEFT QUADS 12X FIREFLYS
/OUT_6 (44)	bc_nR0A_6	C321 0.1 UF 0402	ac_nF2L_X12_R0A [19]	
OUT_7 (51)	bc_pR0A_7	C371 0.1 UF 0402	ac_pF2L_X4_R0A [19]	F2 R0 LEFT QUADS 4X FIREFLYS
/OUT_7 (50)	bc_nR0A_7	C372 0.1 UF 0402	ac_nF2L_X4_R0A [19]	
OUT_8 (54)	bc_pR0A_8	C318 0.1 UF 0402	ac_pSYN_R0B_IN0 [18]	SYNTH "R0_B"
/OUT_8 (53)	bc_nR0A_8	C319 0.1 UF 0402	ac_nSYN_R0B_IN0 [18]	

OUT_9 (56) /OUT_9 (55)

ac_pR0A_FB — C844 0.1 UF 0402 — R320 100 0402 — FB_IN (61) — OUT_9A (59) — bc_pR0A_FB
ac_nR0A_FB — C857 0.1 UF 0402 — /FB_IN (62) — /OUT_9A (58) — bc_nR0A_FB

A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.

U86-2
SI5395

I2C_SEL (39)	/INTR (12)	/SYN_R0A_INT [36]	
I2C_SDA_SYN_R0A [36]	SDA/SDIO (18)	SCLK (16)	I2C_SCL_SYN_R0A [36]
/SYN_R0A_RESET [36]	/RST (6)	/OE (11)	
SYN_R0A_IN_SEL0 [36]	IN_SEL_0 (3)	IN_SEL_1 (4)	SYN_R0A_IN_SEL1 [36]
FINC (48)	FDEC (25)	RSVD (5)	

V_3V3 — R334 10K 0603 — A1/SDO (17)
GND — R333 DNP 0603 — A1/SDO (17)
V_3V3 — R313 10K 0603 — A0//CS (19)
GND — R312 DNP 0603 — A0//CS (19)

I2C ADDR = 0X77

PLACE 3V3 BYPASS
CAPS NEAR PIN 13

V_3V3 — C863 1 UF 0402 10v — GND

V_1V8 — C845 1 UF 0402 10v — C827 1 UF 0402 10v — C790 1 UF 0402 10v — C787 1 UF 0402 10v — C832 1 UF 0402 10v — C850 1 UF 0402 10v — C788 1 UF 0402 10v — C789 1 UF 0402 10v — GND

TWO 1V8 BYPASS CAPS ALONG EACH EDGE

U86-3
SI5395

VDD (32)	VDD (46)	VDD (60)
VDDA (13)		
VDDO_0 (22)	VDDO_1 (26)	VDDO_2 (29)
VDDO_3 (33)	VDDO_4 (36)	VDDO_5 (40)
VDDO_6 (43)	VDDO_7 (49)	VDDO_8 (52)
VDDO_9 (57)	GND_PAD (65)	

V_1V8 / V_3V3 / GND

APOLLO CM v3				
Title: 2.06: REFCLK SYNTHESIZER R0A				
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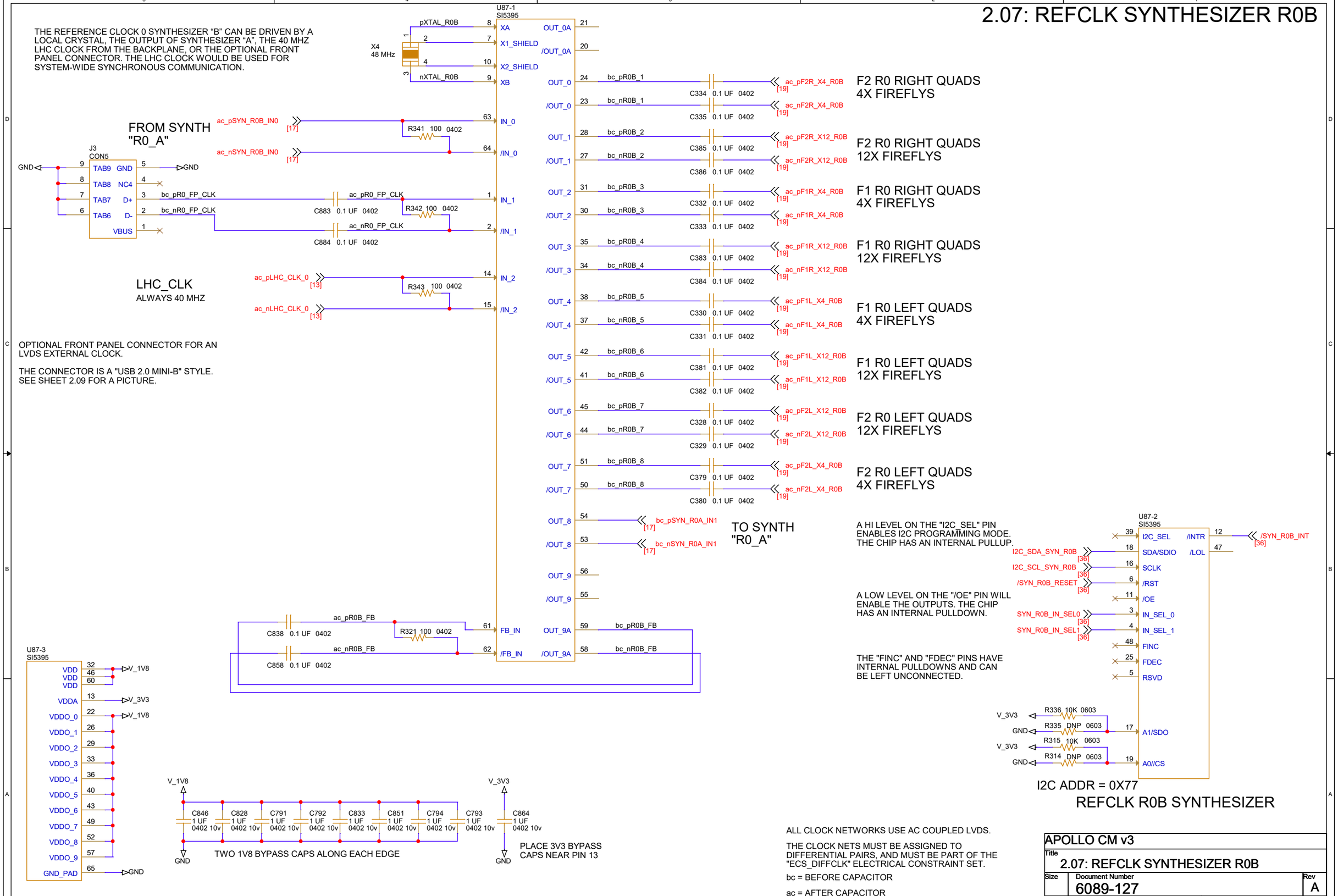
2.07: REFCLK SYNTHESIZER R0B

THE REFERENCE CLOCK 0 SYNTHESIZER "B" CAN BE DRIVEN BY A LOCAL CRYSTAL, THE OUTPUT OF SYNTHESIZER "A", THE 40 MHZ LHC CLOCK FROM THE BACKPLANE, OR THE OPTIONAL FRONT PANEL CONNECTOR. THE LHC CLOCK WOULD BE USED FOR SYSTEM-WIDE SYNCHRONOUS COMMUNICATION.



ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM v3		
Title: 2.07: REFCLK SYNTHESIZER R0B		
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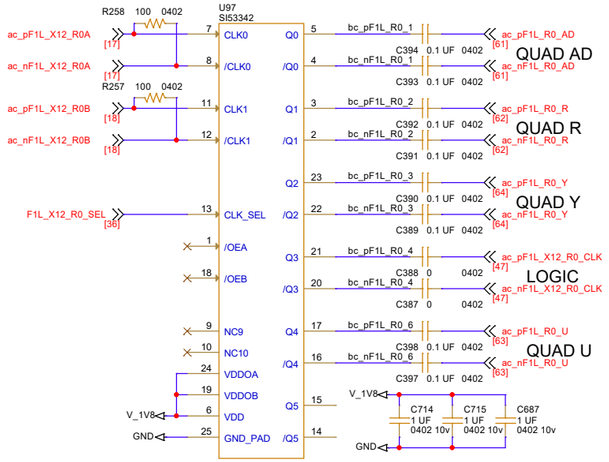
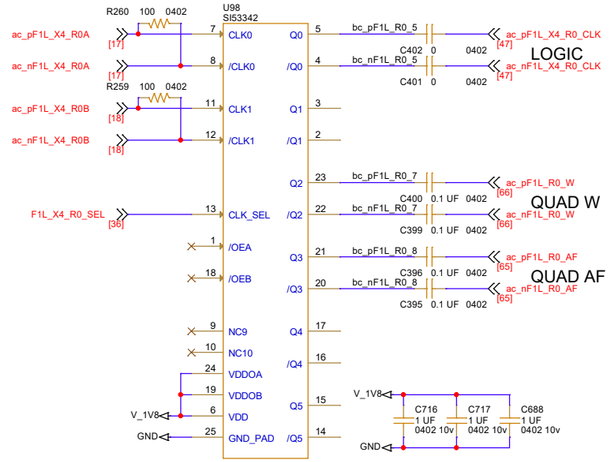
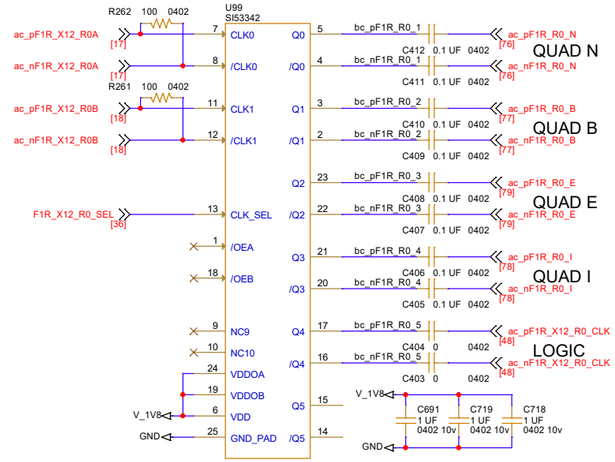
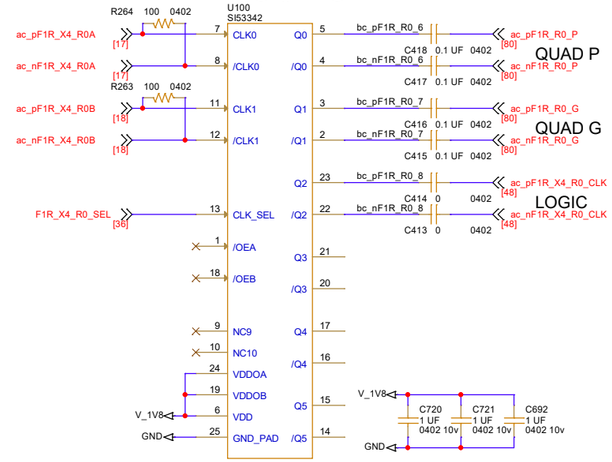
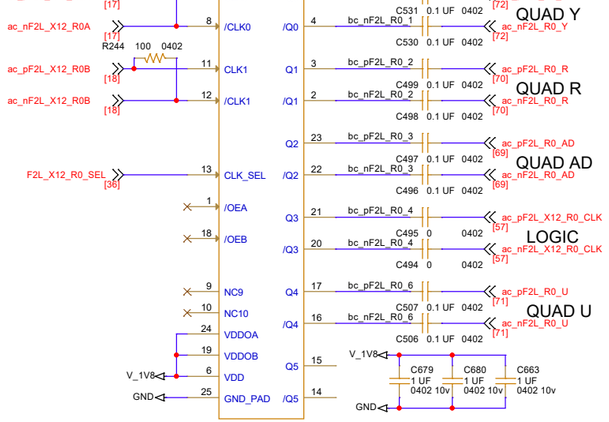
2.08: REFCLK R0 FANOUT

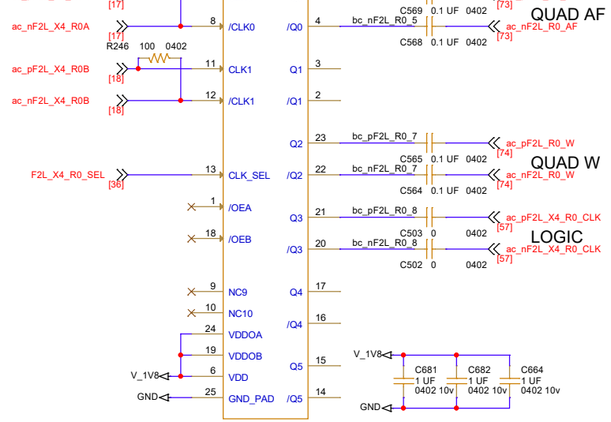


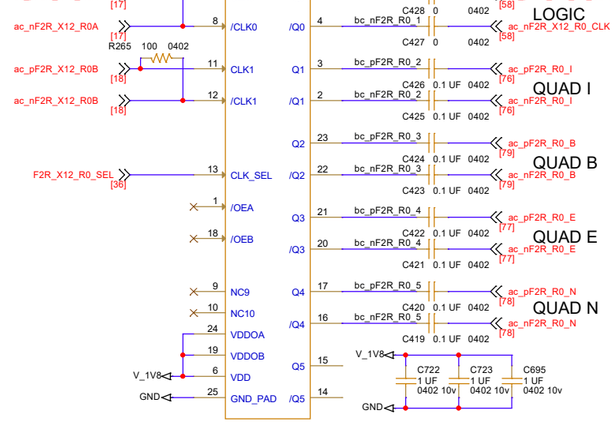


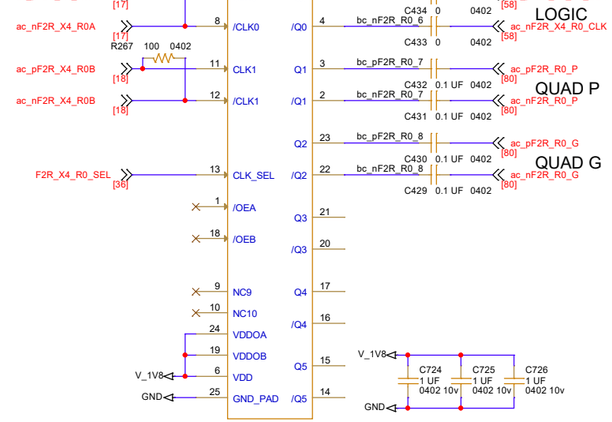












ALL GTY CLOCK NETWORKS USE AC COUPLED LVDS.
ALL LOGIC CLOCK NETWORKS USE DC COUPLED LVDS, WITH ZERO-OHM RESISTORS ON THE CAPACITOR PADS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM v3		
Title: 2.08: REFCLK R0 FANOUT		
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2.09: REFCLK SYNTHESIZER R1A

U91-1
SI5395

X7
48 MHz
pXTAL_R1A
nXTAL_R1A

IF THE HQ_CLK OR LHC_CLK IS AC-COUPLED ON THE SM, USE ZERO-OHM RESISTORS ON THESE CAPACITOR PADS.

HQ_CLK
320 MHZ WITH FPGA#1 AS TCDS ENDPOINT.

bc_pHQ_CLK_IN [13] — C870 0.1 UF 0402 — ac_pHQ_CLK_IN — R325 100 0402 — IN_0
bc_nHQ_CLK_IN [13] — C871 0.1 UF 0402 — ac_nHQ_CLK_IN — /IN_0

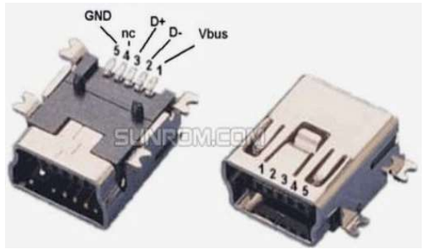
J4
CON5
GND — TAB9 GND — 9, 5 — GND
TAB8 NC4 — 8, 4
TAB7 D+ — 7, 3 — bc_pR1_FP_CLK — C874 0.1 UF 0402 — ac_pR1_FP_CLK — R340 100 0402 — IN_1
TAB6 D- — 6, 2 — bc_nR1_FP_CLK — C875 0.1 UF 0402 — ac_nR1_FP_CLK — /IN_1
VBUS — 1

LHC_CLK
ALWAYS 40 MHZ

ac_pLHC_CLK_1 [13] — R339 100 0402 — IN_2
ac_nLHC_CLK_1 [13] — /IN_2

OPTIONAL FRONT PANEL CONNECTOR FOR AN LVDS EXTERNAL CLOCK.

THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE.



OUT_0A	21	bc_pR1A_10	C369 0.1 UF 0402	ac_pF1L_R0_AB [24]
/OUT_0A	20	bc_nR1A_10	C370 0.1 UF 0402	ac_nF1L_R0_AB [24]
OUT_0	24	bc_pR1A_0	C465 0.1 UF 0402	ac_pF2L_R0_AB [24]
/OUT_0	23	bc_nR1A_0	C466 0.1 UF 0402	ac_nF2L_R0_AB [24]
OUT_1	28	bc_pR1A_1	C367 0.1 UF 0402	ac_pSYN_R1B_IN0 [21]
/OUT_1	27	bc_nR1A_1	C368 0.1 UF 0402	ac_nSYN_R1B_IN0 [21]
OUT_2	31	bc_pR1A_2	C463 0.1 UF 0402	ac_pSYN_R1C_IN0 [22]
/OUT_2	30	bc_nR1A_2	C464 0.1 UF 0402	ac_nSYN_R1C_IN0 [22]
OUT_3	35	bc_pR1A_3	C365 0.1 UF 0402	ac_pF1L_R1_W [66]
/OUT_3	34	bc_nR1A_3	C366 0.1 UF 0402	ac_nF1L_R1_W [66]
OUT_4	38	bc_pR1A_4	C461 0.1 UF 0402	ac_pF1L_R1_AF [65]
/OUT_4	37	bc_nR1A_4	C462 0.1 UF 0402	ac_nF1L_R1_AF [65]
OUT_5	42	bc_pR1A_5	C363 0.1 UF 0402	ac_pF2L_R1_W [74]
/OUT_5	41	bc_nR1A_5	C364 0.1 UF 0402	ac_nF2L_R1_W [74]
OUT_6	45	bc_pR1A_6	C459 0.1 UF 0402	ac_pF2L_R1_AF [73]
/OUT_6	44	bc_nR1A_6	C460 0.1 UF 0402	ac_nF2L_R1_AF [73]
OUT_7	51	bc_pR1A_7	C361 0.1 UF 0402	ac_pF1R_R1_L [24]
/OUT_7	50	bc_nR1A_7	C362 0.1 UF 0402	ac_nF1R_R1_L [24]
OUT_8	54	bc_pR1A_8	C457 0.1 UF 0402	ac_pF2R_R1_L [24]
/OUT_8	53	bc_nR1A_8	C458 0.1 UF 0402	ac_nF2R_R1_L [24]
OUT_9	56			
/OUT_9	55			

F1 QUAD AB (TCDS QUAD)
F2 QUAD AB (TCDS QUAD)
SYN R1B IN0
SYN R1C IN0
F1 QUAD W
F1 QUAD AF
F2 QUAD W
F2 QUAD AF
F1 QUAD L (C2C/TCDS QUAD)
F2 QUAD L (C2C/TCDS QUAD)

OUTPUTS 9 AND 9A MUST BE THE SAME FREQUENCY.

ZERO-DELAY FEEDBACK
320 MHZ WITH FPGA#1 AS TCDS ENDPOINT.

ac_pR1A_FB — C840 0.1 UF 0402 — R318 100 0402 — FB_IN — OUT_9A — 59 — bc_pR1A_FB
ac_nR1A_FB — C853 0.1 UF 0402 — /FB_IN — /OUT_9A — 58 — bc_nR1A_FB

A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

U91-2
SI5395

39	I2C_SEL	/INTR	12 — /SYN_R1A_INT [36]
I2C_SDA_SYN_R1A [36] — 18	SDA/SDIO	/LOL	47
I2C_SCL_SYN_R1A [36] — 16	SCLK		
/SYN_R1A_RESET [36] — 6	/RST		
11	/OE		
SYN_R1A_IN_SEL0 [36] — 3	IN_SEL_0		
SYN_R1A_IN_SEL1 [36] — 4	IN_SEL_1		
48	FINC		
25	FDEC		
5	RSVD		
V_3V3 — R331 10K 0603			
GND — R330 DNP 0603 — 17	A1/SDO		
V_3V3 — R311 10K 0603			
GND — R310 DNP 0603 — 19	A0//CS		

I2C ADDR = 0X77

V_3V3 — C862 1 UF 0402 10v — GND

V_1V8 — C785 1 UF 0402 10v — C843 1 UF 0402 10v — C826 1 UF 0402 10v — C784 1 UF 0402 10v — C783 1 UF 0402 10v — C849 1 UF 0402 10v — C831 1 UF 0402 10v — C782 1 UF 0402 10v — GND

U91-3
SI5395

VDD	32	V_1V8
VDD	46	
VDD	60	
VDDA	13	V_3V3
VDDO_0	22	V_1V8
VDDO_1	26	
VDDO_2	29	
VDDO_3	33	
VDDO_4	36	
VDDO_5	40	
VDDO_6	43	
VDDO_7	49	
VDDO_8	52	
VDDO_9	57	
GND_PAD	65	GND

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM v3

Title: 2.09: REFCLK SYNTHESIZER R1A

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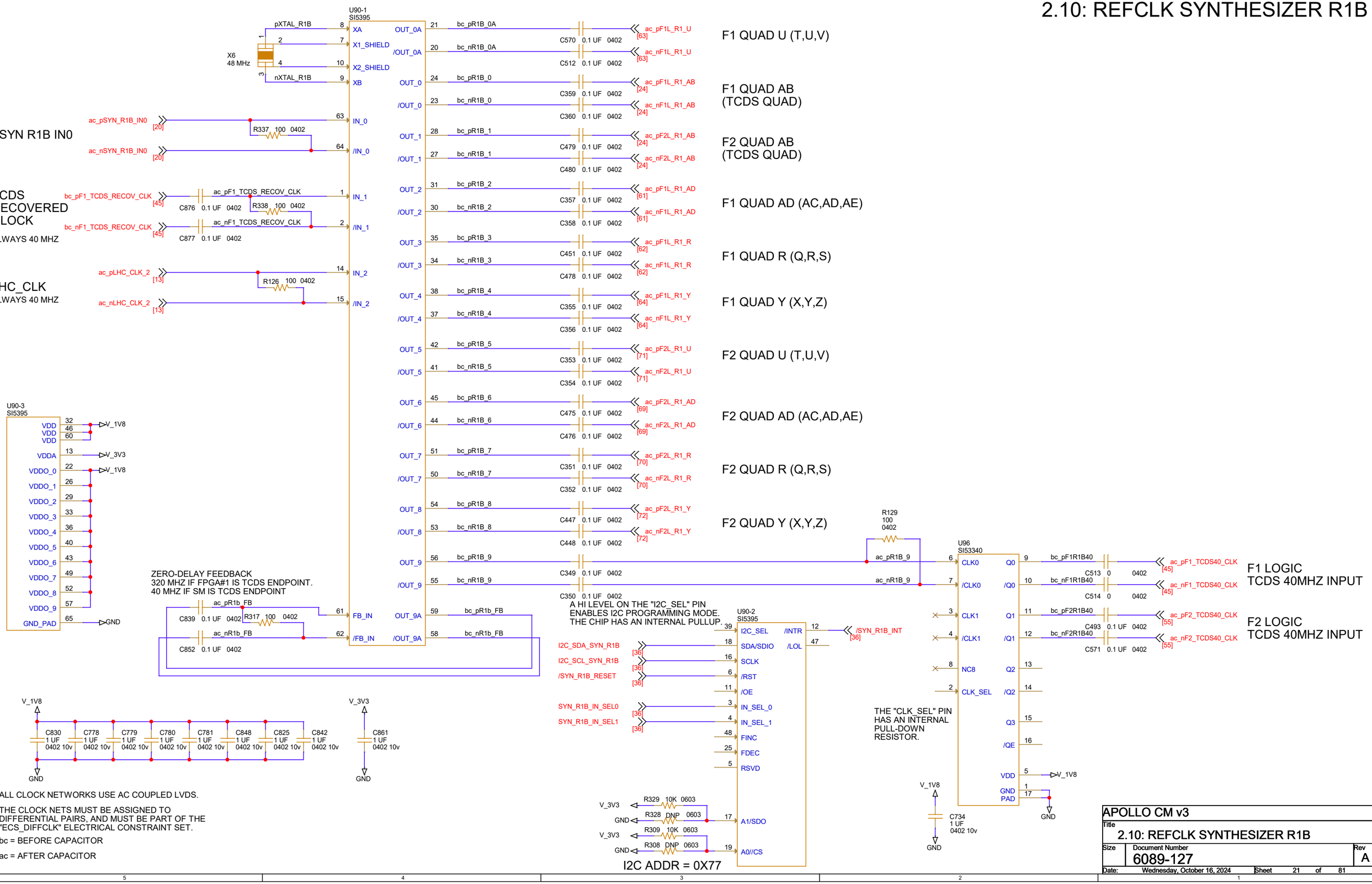
2.10: REFCLK SYNTHESIZER R1B



Title	2.10: REFCLK SYNTHESIZER R1B
Size	Document Number: 6089-127
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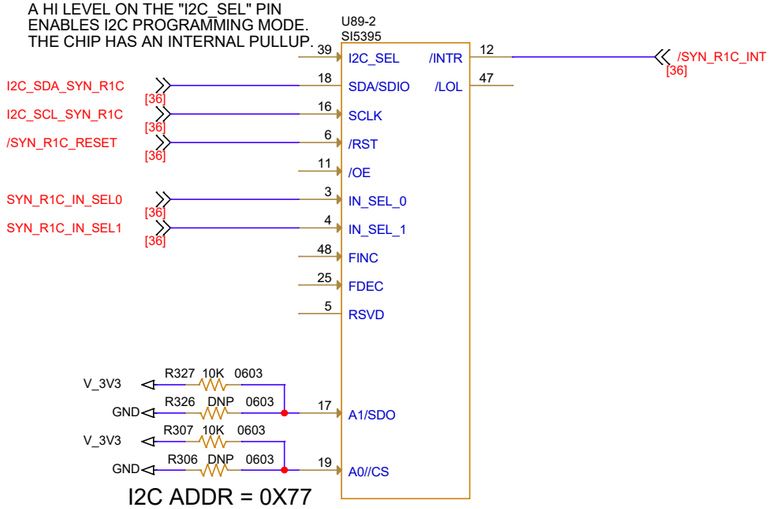
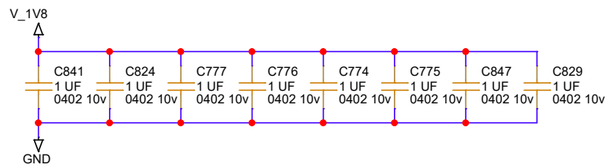
APOLLO CM v3

2.11: REFCLK SYNTHESIZER R1C





ALL CLOCK NETWORKS USE AC COUPLED LVDS.

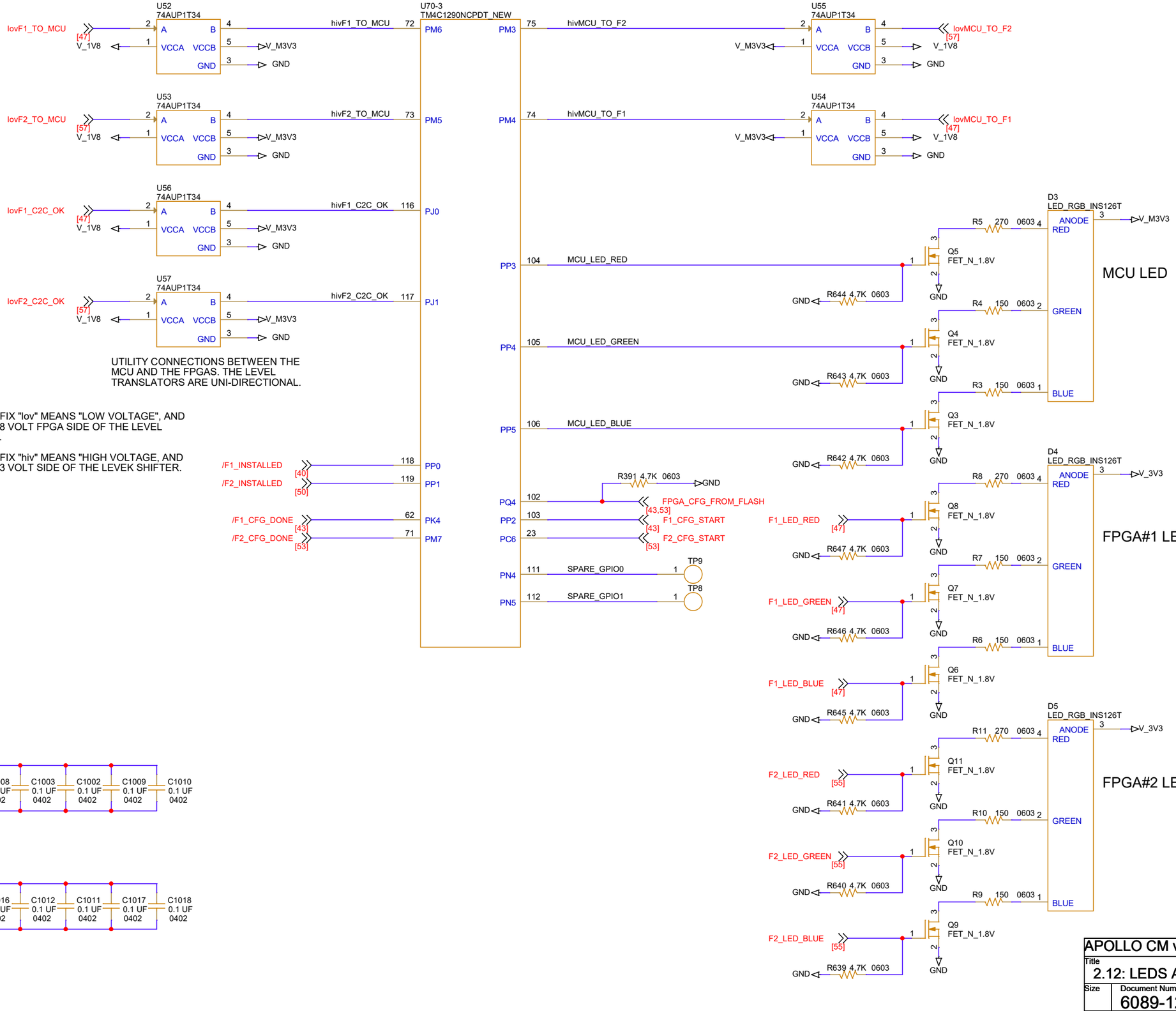
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM v3		
Title: 2.11: REFCLK SYNTHESIZER R1C		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 22 of 81	

2.12: LEDS AND LEVEL SHIFTERS



UTILITY CONNECTIONS BETWEEN THE MCU AND THE FPGAS. THE LEVEL TRANSLATORS ARE UNI-DIRECTIONAL.

THE PREFIX "lov" MEANS "LOW VOLTAGE", AND IS THE 1.8 VOLT FPGA SIDE OF THE LEVEL SHIFTER.

THE PREFIX "hiv" MEANS "HIGH VOLTAGE, AND IS THE 3.3 VOLT SIDE OF THE LEVEK SHIFTER.

APOLLO CM v3		
Title: 2.12: LEDS AND LEVEL SHIFTERS		
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2.13: C2C AND TCDS QUADS

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "AB" QUADS ARE DEDICATED TO TCDS SIGNALS. THE "L" QUADS ARE DEDICATED TO C2C SIGNALS. TCDS AND C2C NETS COME FROM THE SERVICE BOARD HIGH SPEED CONNECTORS

U77-23
FPGA_VU13P_A2577
AB GTY QUAD 120
FPGA#1

ac_pF1L_R0_AB [20] → BD39 MGTREFCLK0P_120, BD40 MGTREFCLK0N_120
ac_nF1L_R0_AB [20]
ac_pF1L_R1_AB [21] → BC41 MGTREFCLK1P_120, BC42 MGTREFCLK1N_120
ac_nF1L_R1_AB [21]
pCON1_TCDS_IN [13] → BG32 MGTYRXP0_120, BG33 MGTYRXN0_120
nCON1_TCDS_IN [13]
pCON1_TCDS_OUT [13] → BH39 MGTYTXP0_120, BH40 MGTYTXN0_120
nCON1_TCDS_OUT [13]
BF34 MGTYRXP1_120, BF35 MGTYRXN1_120
BF39 MGTYTXP1_120, BF40 MGTYTXN1_120
pCON2_TCDS_IN [13] → BJ32 MGTYRXP2_120, BJ33 MGTYRXN2_120
nCON2_TCDS_IN [13]
pCON2_TCDS_OUT [13] → BJ37 MGTYTXP2_120, BJ38 MGTYTXN2_120
nCON2_TCDS_OUT [13]
pF1_TCDS_CROSS_RECV_A, nF1_TCDS_CROSS_RECV_A → BH34 MGTYRXP3_120, BH35 MGTYRXN3_120
pF1_TCDS_CROSS_XMIT_A, nF1_TCDS_CROSS_XMIT_A → BG37 MGTYTXP3_120, BG38 MGTYTXN3_120

C246 0.1 UF 0402
C245 0.1 UF 0402
C243 0.1 UF 0402
C244 0.1 UF 0402

THE CROSS-CONNECT SIGNALS ON GTY CHANNEL 3 ARE USED TO TRANSFER TCDS DATA FROM THE FPGA#1 MASTER TO THE FPGA#2 SLAVE.

F2 QUAD AB
(TCDS QUAD)

U78-23
FPGA_VU13P_A2577
AB GTY QUAD 120
FPGA#2

ac_pF2L_R0_AB [20] → BD39 MGTREFCLK0P_120, BD40 MGTREFCLK0N_120
ac_nF2L_R0_AB [20]
ac_pF2L_R1_AB [21] → BC41 MGTREFCLK1P_120, BC42 MGTREFCLK1N_120
ac_nF2L_R1_AB [21]
pF2_TCDS_CROSS_RECV_A, nF2_TCDS_CROSS_RECV_A → BG32 MGTYRXP0_120, BG33 MGTYRXN0_120
pF2_TCDS_CROSS_XMIT_A, nF2_TCDS_CROSS_XMIT_A → BH39 MGTYTXP0_120, BH40 MGTYTXN0_120
BF34 MGTYRXP1_120, BF35 MGTYRXN1_120
BF39 MGTYTXP1_120, BF40 MGTYTXN1_120
BJ32 MGTYRXP2_120, BJ33 MGTYRXN2_120
BJ37 MGTYTXP2_120, BJ38 MGTYTXN2_120
BH34 MGTYRXP3_120, BH35 MGTYRXN3_120
BG37 MGTYTXP3_120, BG38 MGTYTXN3_120

THE FORWARDED TCDS2 SIGNALS CONNECT TO CHANNEL 0 OF THE TCDS QUAD. THIS ALLOWS THE SAME FPGA CODE TO BE USED ON BOTH FPGAS.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

U77-39
FPGA_VU13P_A2577
L GTY QUAD 220
FPGA#1

ac_pF1R_R0_L [18]
ac_nF1R_R0_L [18]
ac_pF1R_R1_L [20]
ac_nF1R_R1_L [20]
BD13 MGTREFCLK0P_220, BD12 MGTREFCLK0N_220
BC11 MGTREFCLK1P_220, BC10 MGTREFCLK1N_220
pMGT_SM_TO_F1_1 [13]
nMGT_SM_TO_F1_1 [13]
pMGT_F1_TO_SM_1 [13]
nMGT_F1_TO_SM_1 [13]
BG20 MGTYRXP0_220, BG19 MGTYRXN0_220
pMGT_SM_TO_F1_2 [13]
nMGT_SM_TO_F1_2 [13]
pMGT_F1_TO_SM_2 [13]
nMGT_F1_TO_SM_2 [13]
BH13 MGTYTXP0_220, BH12 MGTYTXN0_220
BF18 MGTYRXP1_220, BF17 MGTYRXN1_220
BF13 MGTYTXP1_220, BF12 MGTYTXN1_220
BJ20 MGTYRXP2_220, BJ19 MGTYRXN2_220
BJ15 MGTYTXP2_220, BJ14 MGTYTXN2_220
pF1_C2C_CROSS_RECV_B, nF1_C2C_CROSS_RECV_B → BH18 MGTYRXP3_220, BH17 MGTYRXN3_220
pF1_C2C_CROSS_XMIT_B, nF1_C2C_CROSS_XMIT_B → BG15 MGTYTXP3_220, BG14 MGTYTXN3_220

C247 0.1 UF 0402
C248 0.1 UF 0402
C249 0.1 UF 0402
C250 0.1 UF 0402

U78-39
FPGA_VU13P_A2577
L GTY QUAD 220
FPGA#2

ac_pF2R_R0_L [18]
ac_nF2R_R0_L [18]
ac_pF2R_R1_L [20]
ac_nF2R_R1_L [20]
BD13 MGTREFCLK0P_220, BD12 MGTREFCLK0N_220
BC11 MGTREFCLK1P_220, BC10 MGTREFCLK1N_220
pMGT_SM_TO_F2_1 [13]
nMGT_SM_TO_F2_1 [13]
pMGT_F2_TO_SM_1 [13]
nMGT_F2_TO_SM_1 [13]
BG20 MGTYRXP0_220, BG19 MGTYRXN0_220
pMGT_SM_TO_F2_2 [13]
nMGT_SM_TO_F2_2 [13]
pMGT_F2_TO_SM_2 [13]
nMGT_F2_TO_SM_2 [13]
BH13 MGTYTXP0_220, BH12 MGTYTXN0_220
BF18 MGTYRXP1_220, BF17 MGTYRXN1_220
BF13 MGTYTXP1_220, BF12 MGTYTXN1_220
BJ20 MGTYRXP2_220, BJ19 MGTYRXN2_220
BJ15 MGTYTXP2_220, BJ14 MGTYTXN2_220
pF2_C2C_CROSS_RECV_B, nF2_C2C_CROSS_RECV_B → BH18 MGTYRXP3_220, BH17 MGTYRXN3_220
pF2_C2C_CROSS_XMIT_B, nF2_C2C_CROSS_XMIT_B → BG15 MGTYTXP3_220, BG14 MGTYTXN3_220

APOLLO CM v3
Title: 2.13: C2C_AND_TCDS_QUADS
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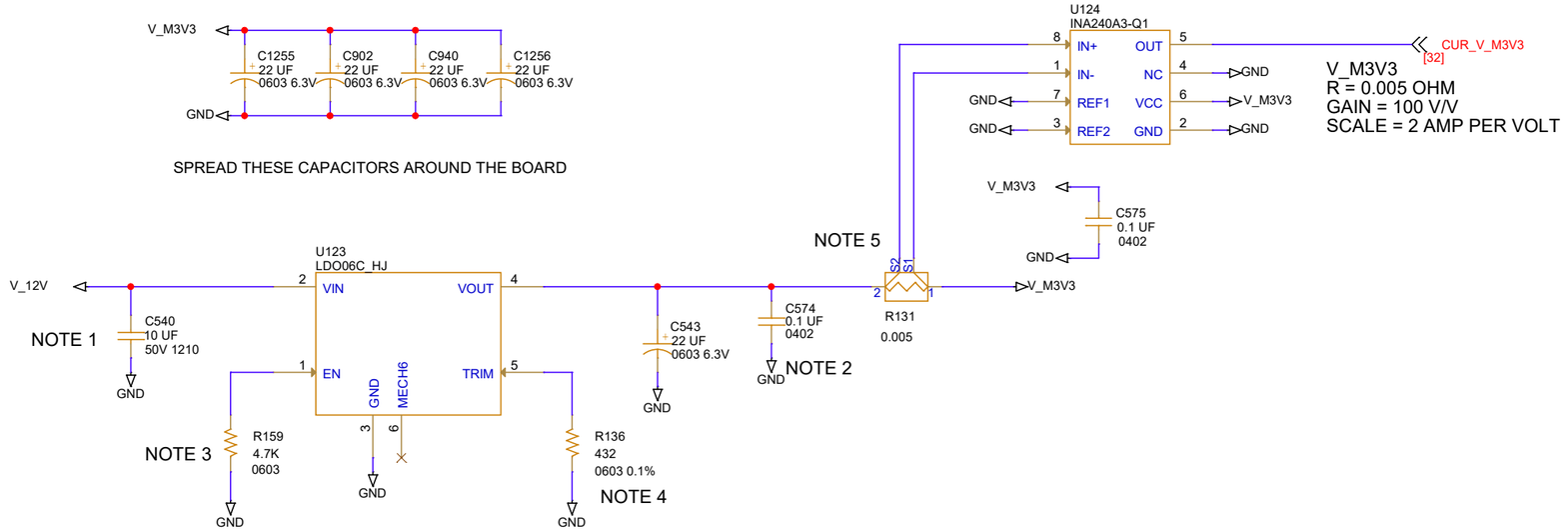
3.01: POWER MANAGEMENT M3V3



GENERAL NOTES:

V_M3V3 IS THE "MANAGEMENT" POWER. IT PROVIDES POWER TO THE POWER SEQUENCING CIRCUIT. IT IS ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

NOTE 1 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL INPUT CAPACITORS.

NOTE 2 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL OUTPUT CAPACITORS.

NOTE 3 UNDERVOLTAGE LOCKOUT RESISTOR
R = 14.81 * (6.81 / ((6.81*Ven) - 18.16))
A 4.7K RESISTOR GIVES 5.8 VOLTS MINIMUM TURNON VOLTAGE

NOTE 4 OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 3.3 VOLTS, R = 436 OHMS (IF R=432 THEN V=3.327)

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

APOLLO CM v3		
Title: 3.01: POWER MANAGEMENT M3V3		
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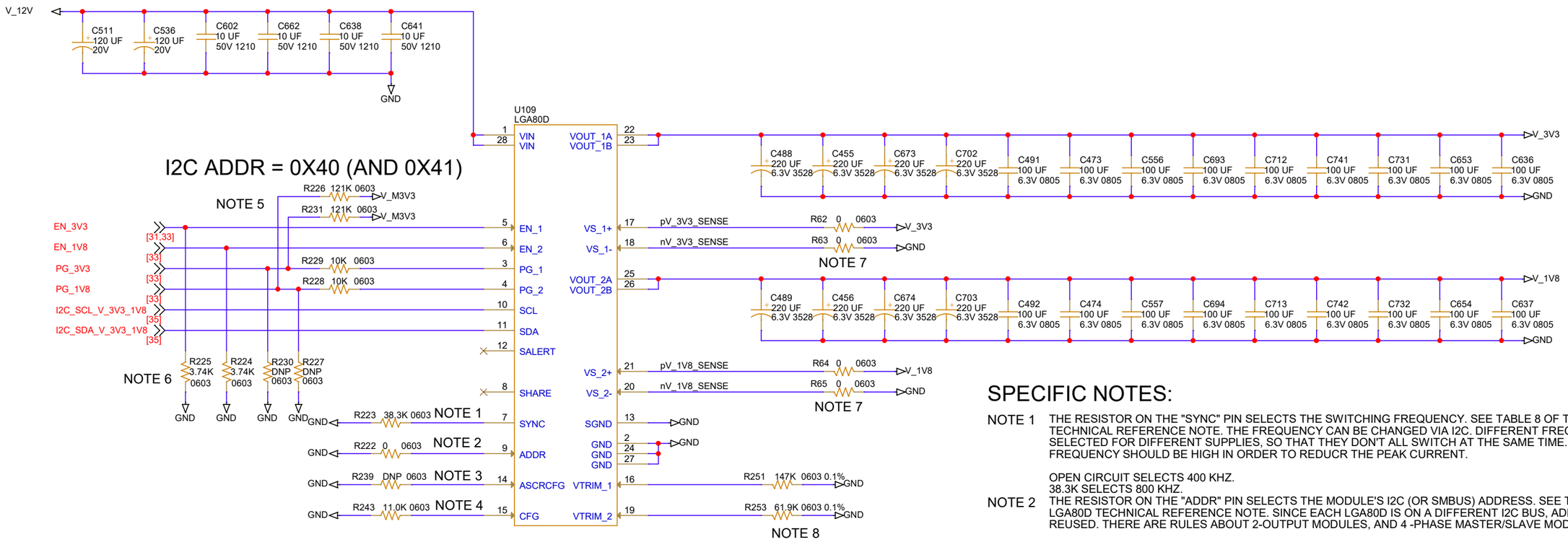
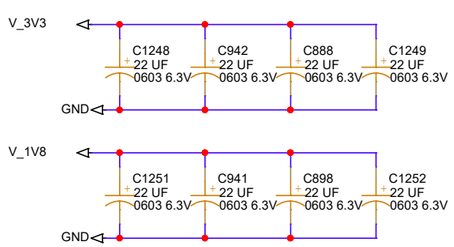
3.02: POWER GLOBAL 3.3V AND 1.8V





NOTE 9

SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME. FOR 3.3V, THE FREQUENCY SHOULD BE HIGH IN ORDER TO REDUCR THE PEAK CURRENT.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER: R=12.1K -> ADDR = 0X44
V_F1_INT SLAVE: R=11K -> ADDR = 0X43
V_F2_INT MASTER: R=12.1K -> ADDR = 0X44
V_F2_INT SLAVE: R=11K -> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=11K SELECTS 2-OUTPUT @ 35A(avg)/45A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 147K FOR 3.3V
RSET = 61.9K FOR 1.8V

NOTE 9 SPREAD THESE CAPACITORS AROUND THE BOARD

GENERAL NOTES:

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM v3		
Title: 3.02: POWER GLOBAL 3.3V AND 1.8V		
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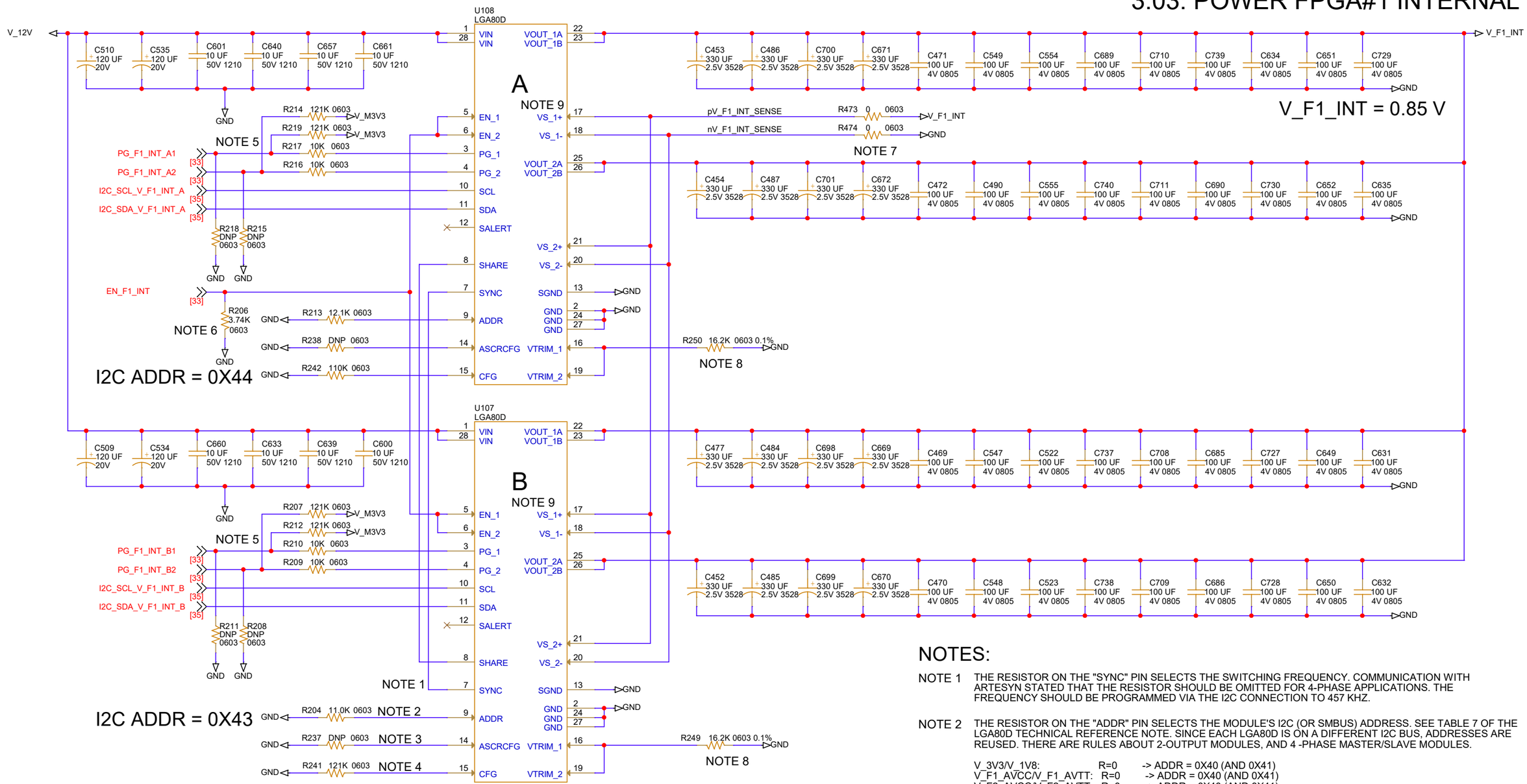
3.03: POWER FPGA#1 INTERNAL



NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

NOTE 10 PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER: R=12.1K -> ADDR = 0X44
V_F1_INT SLAVE: R=11K -> ADDR = 0X43
V_F2_INT MASTER: R=12.1K -> ADDR = 0X44
V_F2_INT SLAVE: R=11K -> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

APOLLO CM v3		
Title: 3.03: POWER FPGA#1 INTERNAL		
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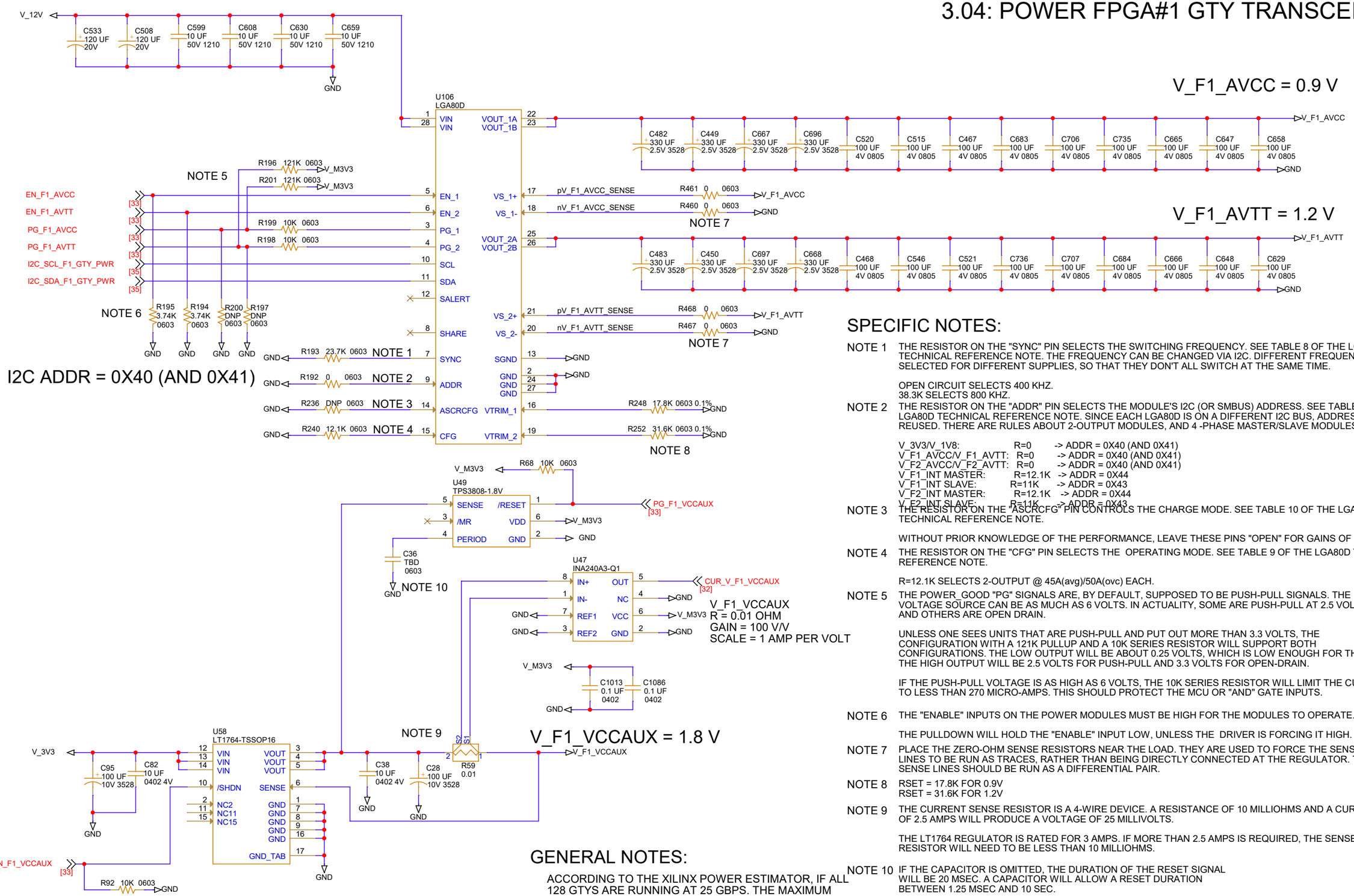
3.04: POWER FPGA#1 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER: R=12.1K -> ADDR = 0X44
V_F1_INT SLAVE: R=11K -> ADDR = 0X43
V_F2_INT MASTER: R=12.1K -> ADDR = 0X44
V_F2_INT SLAVE: R=11K -> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

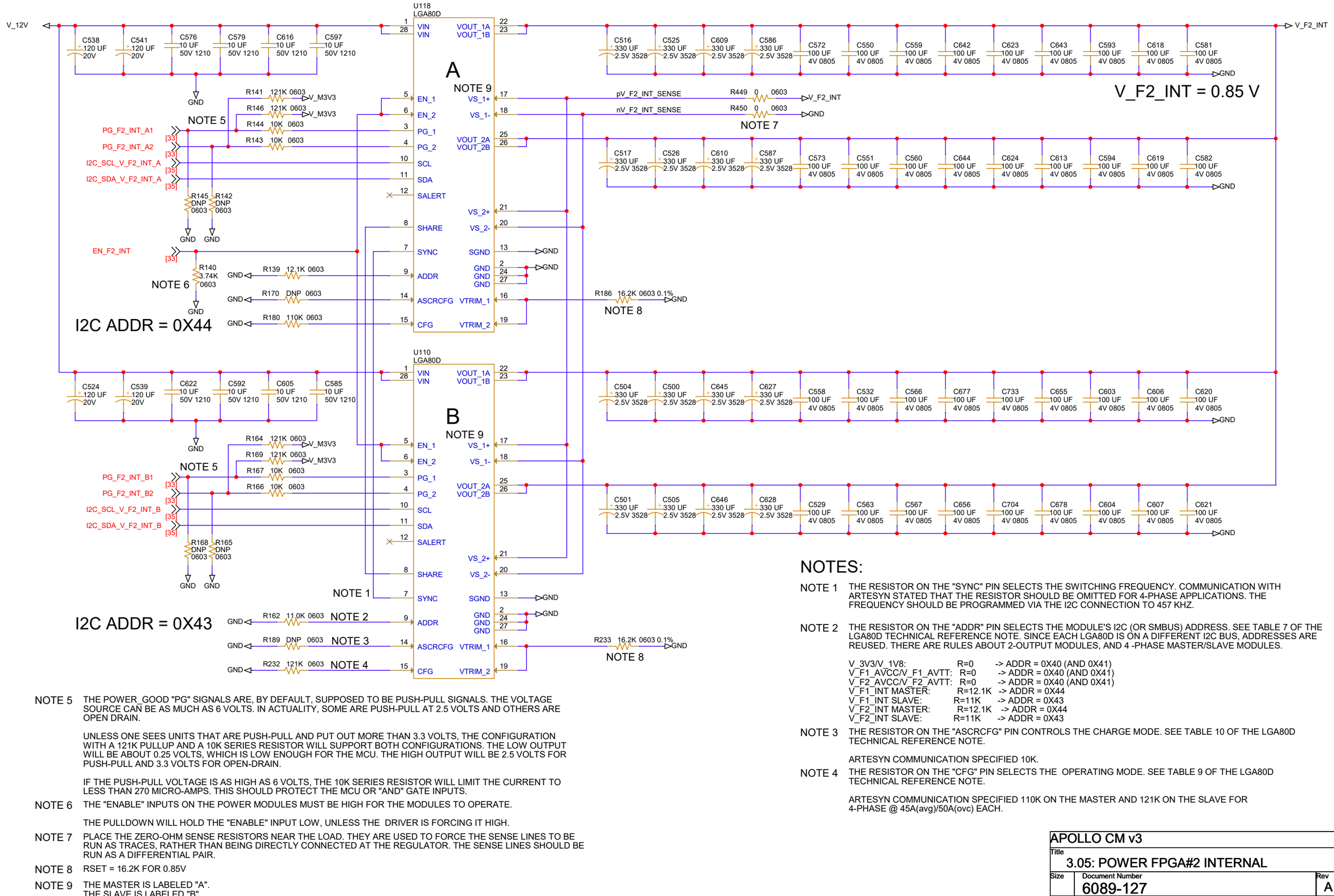
GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM v3		
Title: 3.04: POWER FPGA#1 GTY TRANSCEIVER		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 28 of 81	

3.05: POWER FPGA#2 INTERNAL



NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER: R=12.1K -> ADDR = 0X44
V_F1_INT SLAVE: R=11K -> ADDR = 0X43
V_F2_INT MASTER: R=12.1K -> ADDR = 0X44
V_F2_INT SLAVE: R=11K -> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

APOLLO CM v3		
Title: 3.05: POWER FPGA#2 INTERNAL		
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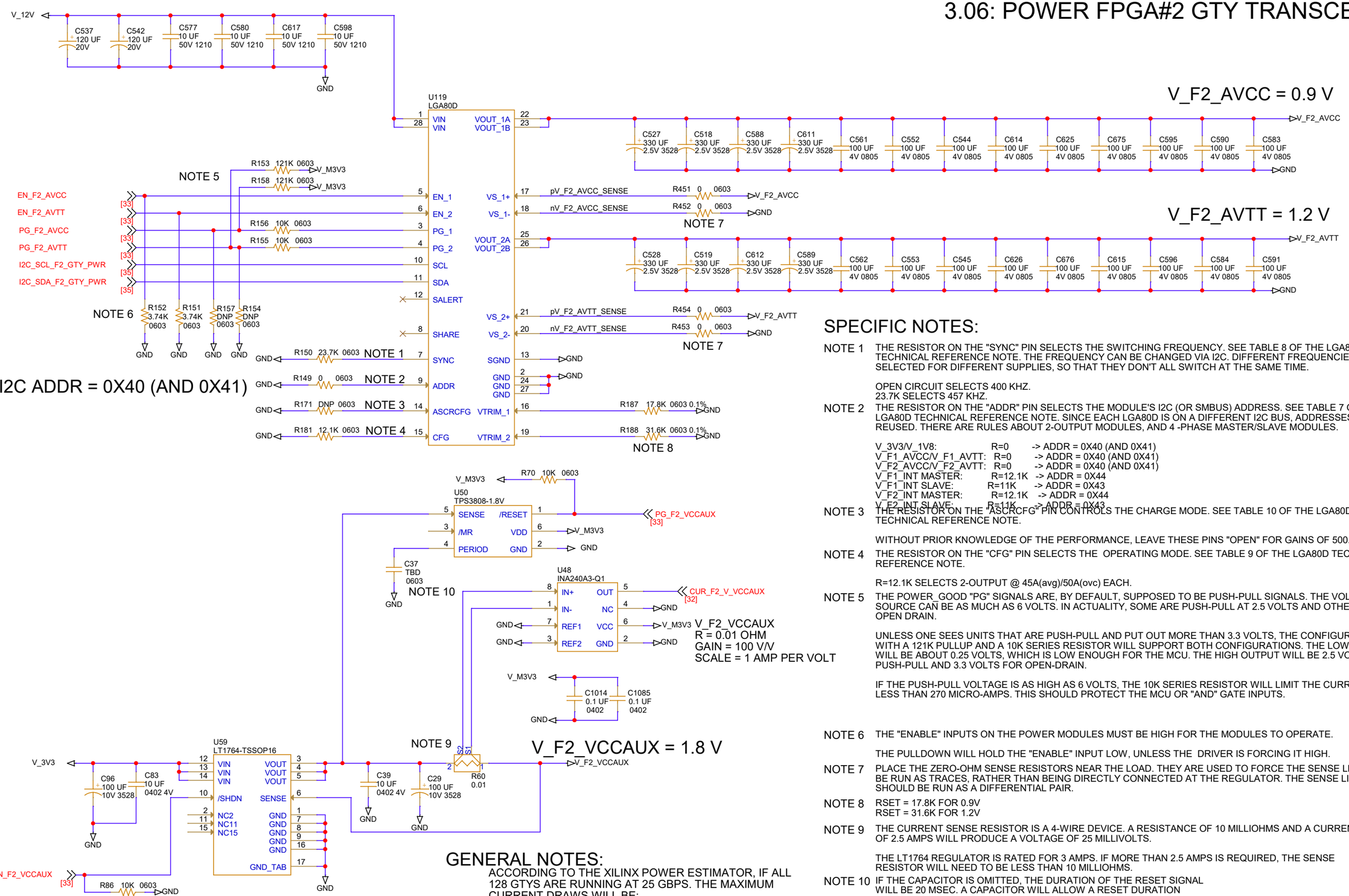
3.06: POWER FPGA#2 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
23.7K SELECTS 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER: R=12.1K -> ADDR = 0X44
V_F1_INT SLAVE: R=11K -> ADDR = 0X43
V_F2_INT MASTER: R=12.1K -> ADDR = 0X44
V_F2_INT SLAVE: R=11K -> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

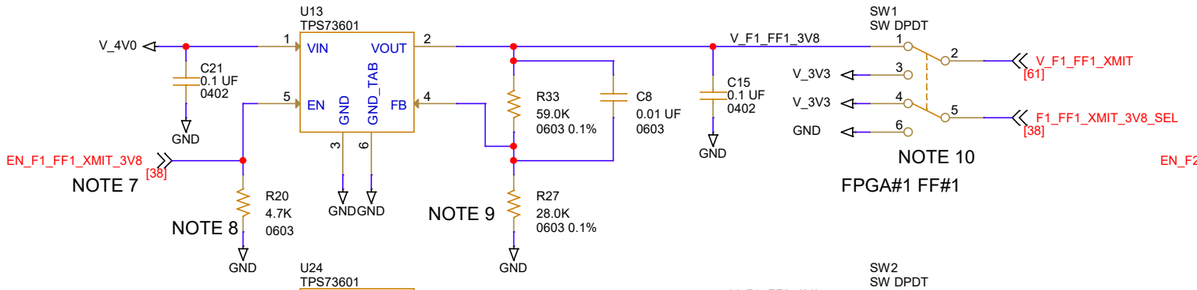
GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

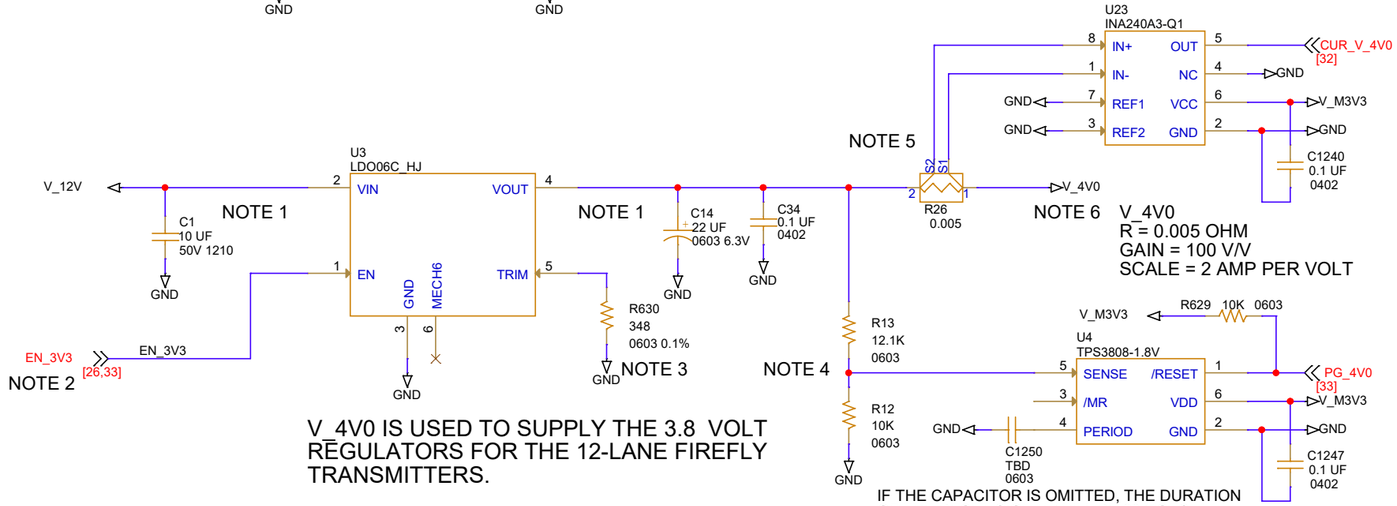
PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM v3		
Title: 3.06: POWER FPGA#2 GTY TRANSCEIVER		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 30 of 81	

3.07: POWER FOR FF X12 XMIT



THE TPS73601 REGULATORS ARE SET FOR 3.74 VOLTS. THE LABELS ALL CALL IT 3.8 VOLTS.



NOTE 1 THE LDO06C DOES NOT REQUIRE ANY EXTERNAL INPUT OR OUTPUT CAPACITORS.

NOTE 2 THE LDO06C IS ENABLED AT THE SAME TIME AS THE BOARD-WIDE 3.3V SUPPLY.

NOTE 3 LDO06C OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 4.0 VOLTS, R=0.347 kOHMS

NOTE 4 THE MONITORING CHIP EXPECTS 1.8 VOLTS AT THE INPUT, SO THE 4.0 VOLTS IS DIVIDED.

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

NOTE 6 V_4V0 IS ONLY CONNECTED ONTHIS PAGE, EXCEPT FOR MEASURING BY THE MCU ADC.

NOTE 7 THE TPS73601 REGULATOR SHOULD NOT BE ENABLED UNTIL THE FIREFLY TRANSMITTER TYPE HAS BEEN DETERMINED AND THE VOLTAGE SWITCH IS FOUND TO BE IN THE CORRECT POSITION.

NOTE 8 PULLDOWNS ARE NEEDED ON THE CONTROL INPUTS, SINCE THE I2C DRIVER DEVICES NEED TO BE CONFIGURED AS OUTPUTS BEFORE THEY CAN CONTOL THE LOGIC LEVEL. THE I2C DRIVERS HAVE A BUILT-IN 100K PULLUP.

NOTE 9 THE TPS73601 OUTPUT VOLTAGE IS CALCULATED BY:
VOUT = 1.204 * ((Rtop+Rbot)/Rbot)
IF Rtop = 59.0k AND Rbot=28K, THEN VOUT = 3.74 V

NOTE 10 THE SWITCH IS SHOWN IN THE POSITION TO PROVIDE 3.8 VOLTS TO THE FIREFLY TRANSMITTER. THE "*_3V8_SEL" SIGNAL WILL BE HIGH.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM v3		
Title: 3.07: POWER FOR FF X12 XMIT		
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Date: Wednesday, October 16, 2024	Sheet 31 of 81	

3.08: VOLT, CUR, TEMP MEASURE

TEST POINTS TO
MEASURE VOLTAGES

THE 12 VOLT SUPPLY
LEVEL IS DIVIDED BY 6

THE M3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 3.3 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

THE 4.0 VOLT SUPPLY
LEVEL IS DIVIDED BY 2

U70-5
TM4C1290NCPDT_NEW

THE VALUE OF "MCU_VREFA" SETS THE VOLTAGE THAT WILL CORRESPOND TO THE ADC FULL SCALE VALUE OF 4095. THE MINIMUM VOLTAGE IS 2.4 VOLTS.

THIS DESIGN USES 2.5 VOLTS FOR FULL SCALE.

U67
LT1790-2.5V

THESE ARE TEST POINTS FOR "GND", DISTRIBUTED ACROSS THE BOARD.

THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

Title	APOLLO CM v3
	3.08: VOLT, CUR, TEMP MEASURE
Size	
Document Number	6089-127
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Date:	Wednesday, October 16, 2024
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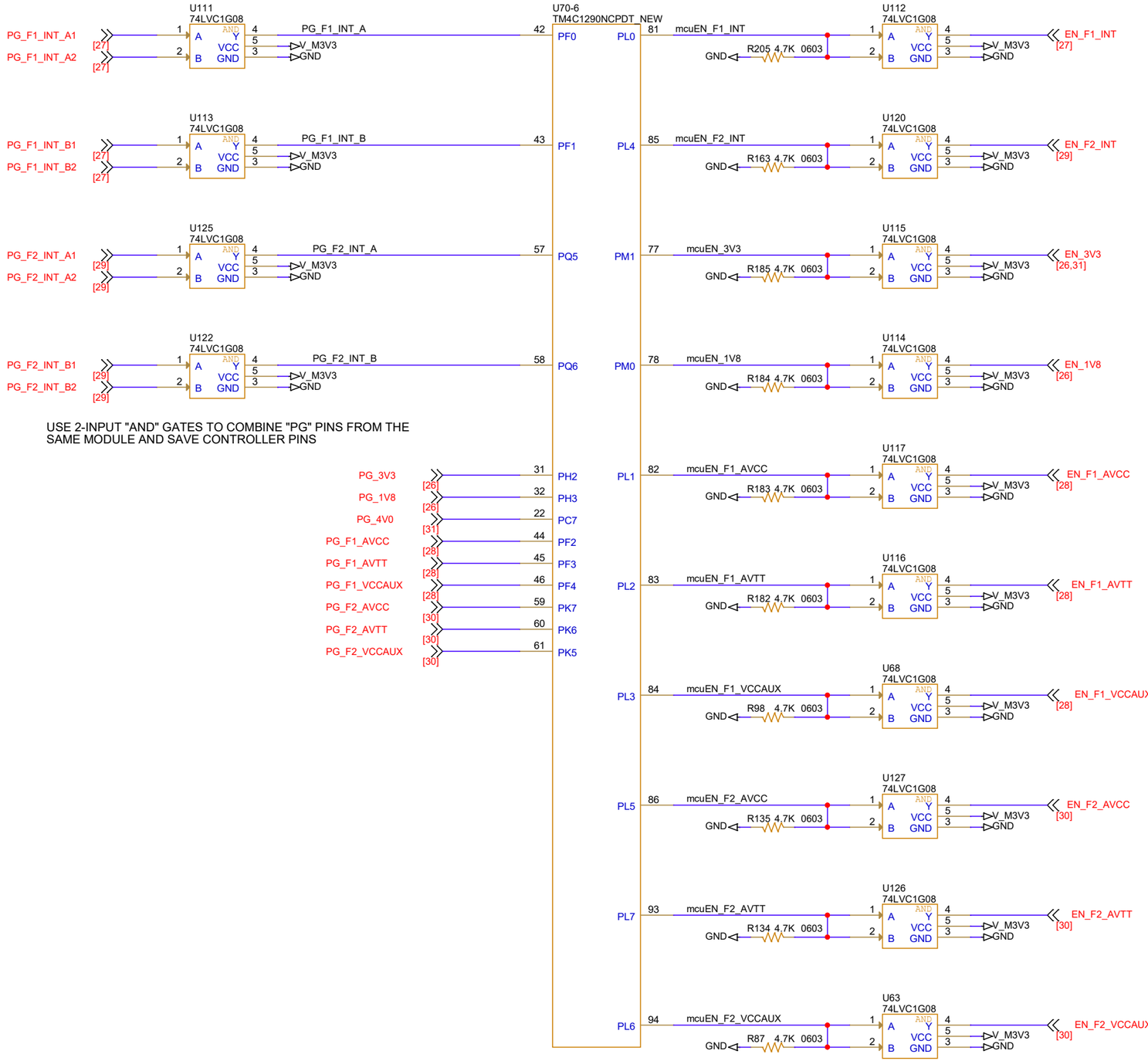
3.09: POWER CONTROL



APOLLO CM v3		
Title: 3.09: POWER CONTROL		
Size	Document Number: 6089-127	Rev: A
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4.01: I2C CONTROLLER

THE I2C PULLUPS ON THE MCU ARE POWERED FROM V_M3V3.

MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.

V_M3V3 R272 2.2K 0603, R270 2.2K 0603
V_M3V3 R360 2.2K 0603, R366 2.2K 0603
V_M3V3 R613 2.2K 0603, R627 2.2K 0603
V_M3V3 R604 2.2K 0603, R618 2.2K 0603
V_M3V3 R482 2.2K 0603, R483 2.2K 0603

U70-4
TM4C1290NCPDT_NEW

I2C_SCL1	49	PWR I2C
I2C_SDA1	50	
PQ0	5	
I2C_SCL2	51	CLOCKS I2C
I2C_SDA2	52	
PQ1	6	
I2C_SCL3	53	FPGA#2 OPTICS I2C
I2C_SDA3	54	
PQ2	11	
I2C_SCL4	55	FPGA#1 OPTICS I2C
I2C_SDA4	56	
PQ3	27	
I2C_SCL5	95	FPGA I2C
I2C_SDA5	96	
PH0	29	

PWR I2C: SDA_PWR TP14 1, SCL_PWR TP15 1
- I2C_SCL_PWR [35]
- I2C_SDA_PWR [35]
- /I2C_RESET_PWR [35]
- R256 10K 0603 V_M3V3

CLOCKS I2C: SDA_CLOCKS TP13 1, SCL_CLOCKS TP12 1
- I2C_SCL_CLOCKS [36]
- I2C_SDA_CLOCKS [36]
- /I2C_RESET_CLOCKS [36]
- R344 10K 0603 V_M3V3

FPGA#2 OPTICS I2C: SDA_OP2 TP1 1, SCL_OP2 TP2 1
- I2C_SCL_F2_OPTICS [39]
- I2C_SDA_F2_OPTICS [39]
- /I2C_RESET_F2_OPTICS [39]
- R594 10K 0603 V_M3V3

FPGA#1 OPTICS I2C: SDA_OP1 TP5 1, SCL_OP1 TP4 1
- I2C_SCL_F1_OPTICS [38]
- I2C_SDA_F1_OPTICS [38]
- /I2C_RESET_F1_OPTICS [38]
- R588 10K 0603 V_M3V3

FPGA I2C: SDA_FPGA TP6 1, SCL_FPGA TP7 1
- I2C_SCL_FPGAS [37]
- I2C_SDA_FPGAS [37]
- /I2C_RESET_FPGAS [37]
- R484 10K 0603 V_1V8

THE OUTPUTS THAT DRIVE THE "RESET" SIGNALS NEED TO BE OPEN-DRAIN.

PN0 107 ID_EEPROM_WP

U93
24CS512

V_M3V3	R280 10K 0603	
GND	R281 0 0603	3 A2
V_M3V3	R278 10K 0603	
GND	R279 0 0603	2 A1
V_M3V3	R276 10K 0603	
GND	R277 0 0603	1 A0
V_M3V3		8 VCC
V_M3V3		7 WP
GND		4 GND
		5 SDA
		6 SCL

C743 0.1 UF 0402 (V_M3V3 to GND)
R275 10K 0603 (V_M3V3 to WP)

THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS. IT ALSO CONTAINS CONFIGURATION FILES FOR THE SI5395 SYNTHESIZERS.

THE EEPROM IS CONNECTED TO THE I2C BUS THAT RUNS THE CLOCKING CHIPS.

R/W I2C ADDR = 0X50

SEC/CONF I2C ADDR = 0X58

24CS512 I2C ADDRESS:
EEPROM READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
SECURITY OR CONFIGURATION REGISTER
1 0 1 1 A2 A1 A0
RANGE 0X58 TO 0X5F

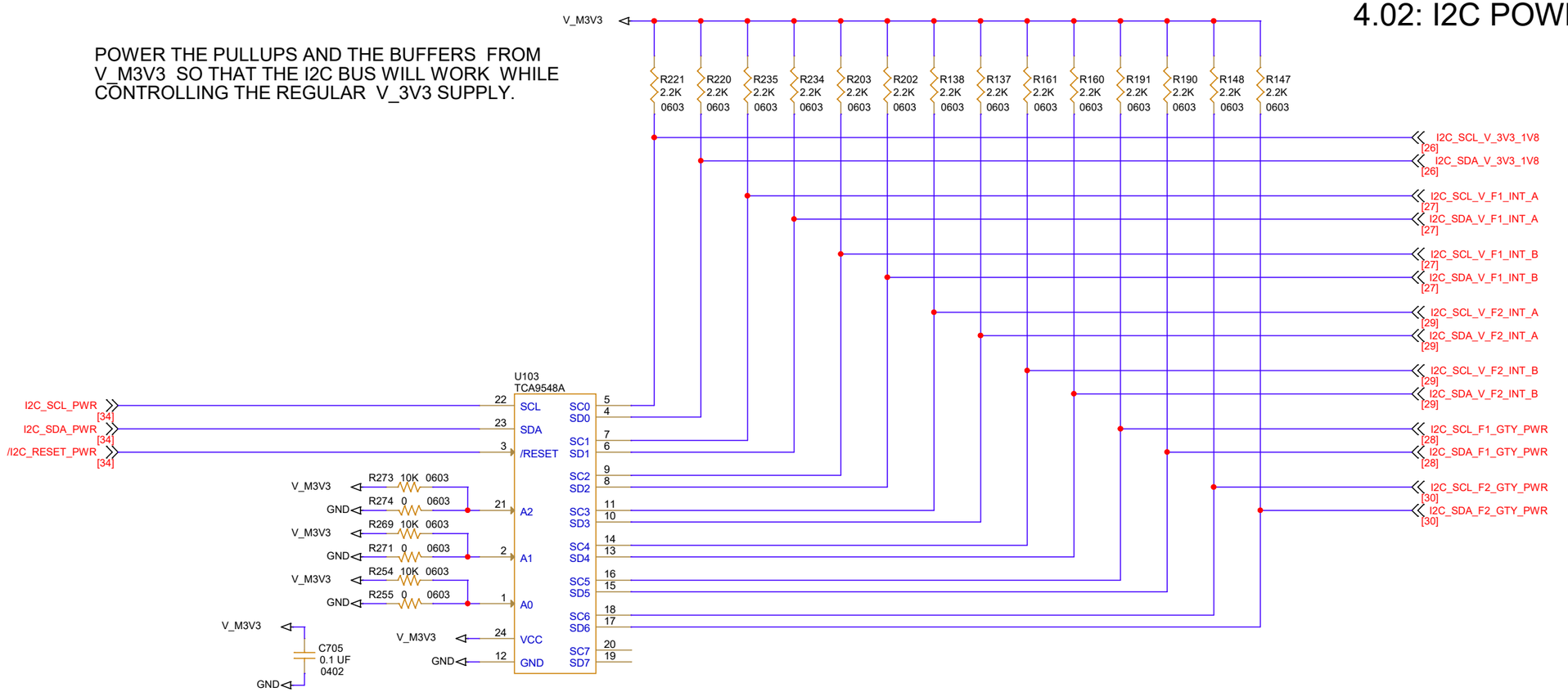
INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

APOLLO CM v3		
Title: 4.01: I2C CONTROLLER		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 34 of 81	

4.02: I2C POWER CONTROL

POWER THE PULLUPS AND THE BUFFERS FROM V_M3V3 SO THAT THE I2C BUS WILL WORK WHILE CONTROLLING THE REGULAR V_3V3 SUPPLY.



I2C ADDR = 0X70

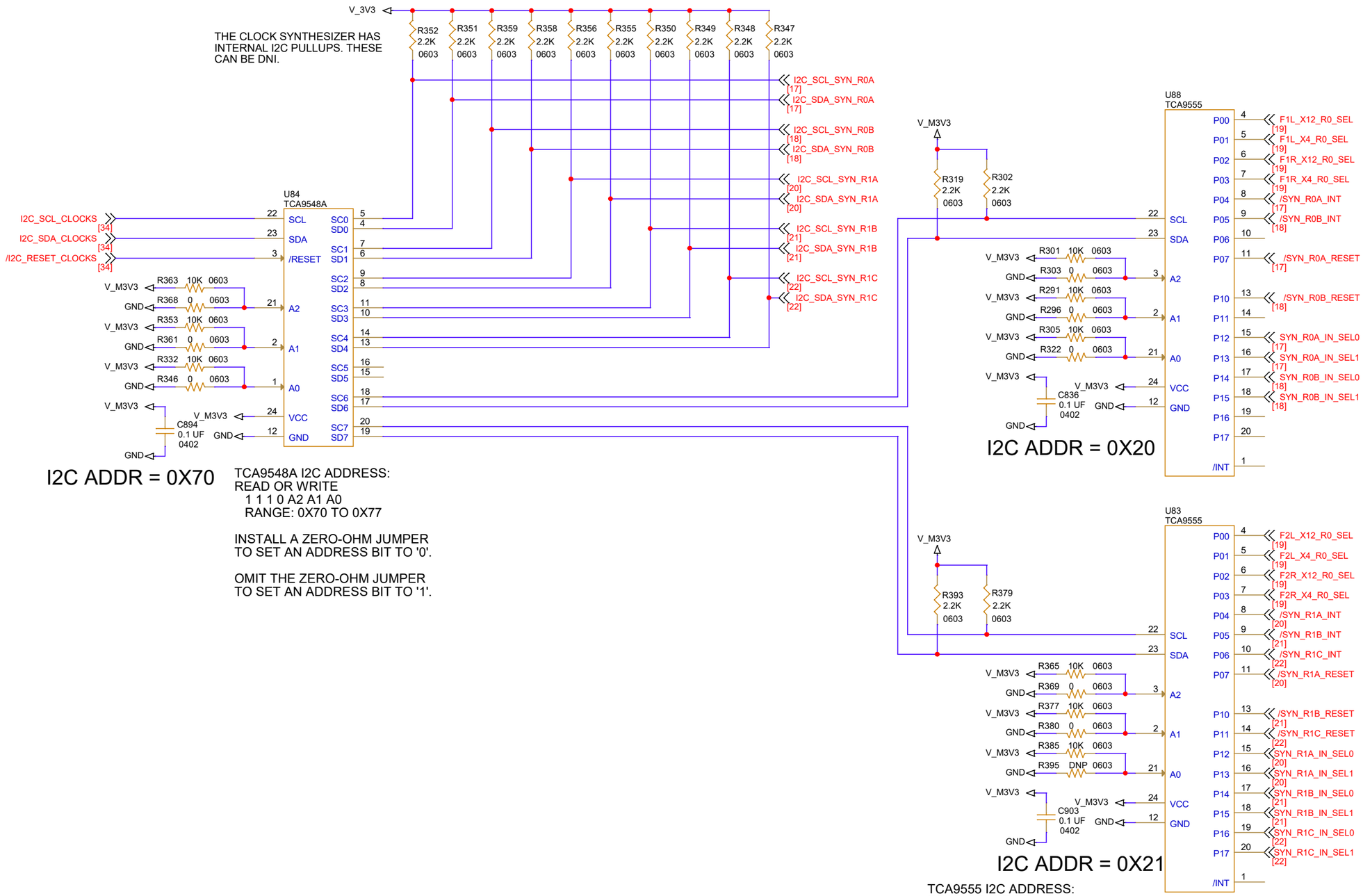
TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

APOLLO CM v3		
Title: 4.02: I2C POWER CONTROL		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 35 of 81	

4.03: I2C CLOCK CONTROL



APOLLO CM v3		
Title: 4.03: I2C CLOCK CONTROL		
Size	Document Number: 6089-127	Rev: A
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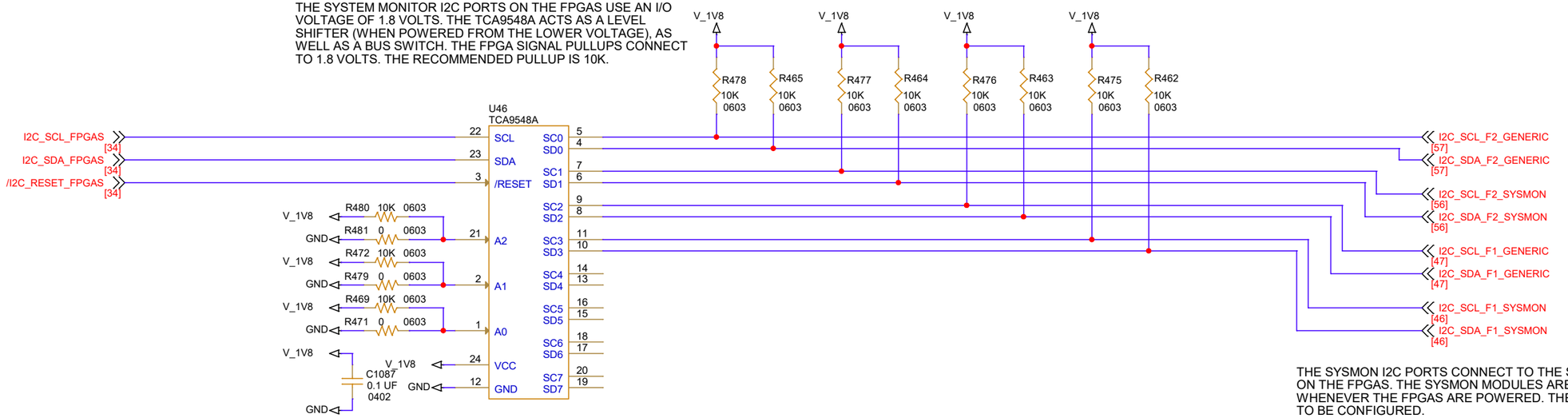
4.04: I2C FPGA INTERNALS

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER (WHEN POWERED FROM THE LOWER VOLTAGE), AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THE SYSMON I2C PORTS CONNECT TO THE SYSMON MODULE PINS ON THE FPGAS. THE SYSMON MODULES ARE AVAILABLE WHENEVER THE FPGAS ARE POWERED. THE FPGAS DO NOT HAVE TO BE CONFIGURED.

THE GENERIC I2C PORTS CONNECT TO I2C MODULES THAT ARE LOADED AS PART OF THE CONFIGURATION PROCESS. THEY ARE NOT AVAILABLE BEFORE THE FPGA HAS BEEN CONFIGURED.

THE GENERIC MODULES HAVE MORE CAPABILITY THAN THE SYSMON MODULES.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

APOLLO CM v3

Title: 4.04: I2C FPGA INTERNALS

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Date: Wednesday, October 16, 2024 Sheet 37 of 81

4.05: I2C FPGA#1 OPTICS

I2C_SCL_F1_OPTICS [34]
I2C_SDA_F1_OPTICS [34]
/I2C_RESET_F1_OPTICS [34]

U14
TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND
SC0/SD0, SC1/SD1, SC2/SD2, SC3/SD3, SC4/SD4, SC5/SD5, SC6/SD6, SC7/SD7

R610 10K 0603
R621 0 0603
R595 10K 0603
R601 0 0603
R585 10K 0603
R589 0 0603
C1244 0.1 UF 0402

I2C_SCL_F1_FF1_XMIT [61]
I2C_SDA_F1_FF1_XMIT [61]
I2C_SCL_F1_FF1_RECV [61]
I2C_SDA_F1_FF1_RECV [61]
I2C_SCL_F1_FF5_XCVR [65]
I2C_SDA_F1_FF5_XCVR [65]
I2C_SCL_F1_FF2_XMIT [62]
I2C_SDA_F1_FF2_XMIT [62]
I2C_SCL_F1_FF2_RECV [62]
I2C_SDA_F1_FF2_RECV [62]

I2C ADDR = 0X70

U15
TCA9555

SCL, SDA, A2, A1, A0, VCC, GND
P00, P01, P02, P03, P04, P05, P06, P07, P10, P11, P12, P13, P14, P15, P16, P17, /INT

R617 2.2K 0603
R602 2.2K 0603

R586 10K 0603
R590 0 0603
R596 10K 0603
R603 0 0603
R611 10K 0603
R622 0 0603
C1242 0.1 UF 0402

/F1_FF1_XMIT_INT [61]
/F1_FF1_RECV_INT [61]
/F1_FF2_XMIT_INT [62]
/F1_FF2_RECV_INT [62]
/F1_FF3_XMIT_INT [63]
/F1_FF3_RECV_INT [63]
/F1_FF4_XMIT_INT [64]
/F1_FF4_RECV_INT [64]

INPUT

/F1_FF1_XMIT_PRESENT [61]
/F1_FF1_RECV_PRESENT [61]
/F1_FF2_XMIT_PRESENT [62]
/F1_FF2_RECV_PRESENT [62]
/F1_FF3_XMIT_PRESENT [63]
/F1_FF3_RECV_PRESENT [63]
/F1_FF4_XMIT_PRESENT [64]
/F1_FF4_RECV_PRESENT [64]

INPUT

I2C ADDR = 0X20

I2C_SCL_F1_FF3_XMIT [63]
I2C_SDA_F1_FF3_XMIT [63]
I2C_SCL_F1_FF3_RECV [63]
I2C_SDA_F1_FF3_RECV [63]
I2C_SCL_F1_FF6_XCVR [66]
I2C_SDA_F1_FF6_XCVR [66]
I2C_SCL_F1_FF4_XMIT [64]
I2C_SDA_F1_FF4_XMIT [64]
I2C_SCL_F1_FF4_RECV [64]
I2C_SDA_F1_FF4_RECV [64]

U16
TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND
SC0/SD0, SC1/SD1, SC2/SD2, SC3/SD3, SC4/SD4, SC5/SD5, SC6/SD6, SC7/SD7

R612 10K 0603
R623 0 0603
R597 10K 0603
R605 0 0603
R587 10K 0603
R591 DNP 0603
C1241 0.1 UF 0402

I2C ADDR = 0X71

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

R619 2.2K 0603
R606 2.2K 0603

U17
TCA9555

SCL, SDA, A2, A1, A0, VCC, GND
P00, P01, P02, P03, P04, P05, P06, P07, P10, P11, P12, P13, P14, P15, P16, P17, /INT

R600 10K 0603
R609 0 0603
R620 10K 0603
R626 0 0603
R633 10K 0603
R636 DNP 0603
C1243 0.1 UF 0402

/F1_FF5_XCVR_INT [65]
/F1_FF6_XCVR_INT [66]
/F1_FF5_XCVR_PRESENT [65]
/F1_FF6_XCVR_PRESENT [66]

INPUT

/F1_FF_RESET [61,62,63,64,65,66]

OUTPUT

EN_F1_FF1_XMIT_3V8 [31]
EN_F1_FF2_XMIT_3V8 [31]
EN_F1_FF3_XMIT_3V8 [31]
EN_F1_FF4_XMIT_3V8 [31]

OUTPUT

F1_FF1_XMIT_3V8_SEL [31]
F1_FF2_XMIT_3V8_SEL [31]
F1_FF3_XMIT_3V8_SEL [31]
F1_FF4_XMIT_3V8_SEL [31]

INPUT

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

I2C ADDR = 0X21

I2C REGISTER PIN ASSIGNMENTS ARE SCRAMBLED COMPARED TO PREVIOUS CM VERSIONS

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4.06: I2C FPGA#2 OPTICS

I2C_SCL_F2_OPTICS [34]
I2C_SDA_F2_OPTICS [34]
/I2C_RESET_F2_OPTICS [34]

U1
TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND
SC0/SD0, SC1/SD1, SC2/SD2, SC3/SD3, SC4/SD4, SC5/SD5, SC6/SD6, SC7/SD7

I2C_SCL_F2_FF1_XMIT [69]
I2C_SDA_F2_FF1_XMIT [69]
I2C_SCL_F2_FF1_RECV [69]
I2C_SDA_F2_FF1_RECV [69]
I2C_SCL_F2_FF5_XCVR [73]
I2C_SDA_F2_FF5_XCVR [73]
I2C_SCL_F2_FF2_XMIT [70]
I2C_SDA_F2_FF2_XMIT [70]
I2C_SCL_F2_FF2_RECV [70]
I2C_SDA_F2_FF2_RECV [70]

R655 10K 0603 — V_M3V3
R658 0 0603 — GND
R648 10K 0603 — V_M3V3
R652 0 0603 — GND
R634 10K 0603 — V_M3V3
R637 0 0603 — GND
C1253 0.1 UF 0402

I2C ADDR = 0X70

V_M3V3
R657 2.2K 0603
R653 2.2K 0603

U2
TCA9555

SCL, SDA, A2, A1, A0, VCC, GND, /INT
P00 /F2_FF1_XMIT_INT [69]
P01 /F2_FF1_RECV_INT [69]
P02 /F2_FF2_XMIT_INT [70]
P03 /F2_FF2_RECV_INT [70]
P04 /F2_FF3_XMIT_INT [71]
P05 /F2_FF3_RECV_INT [71]
P06 /F2_FF4_XMIT_INT [72]
P07 /F2_FF4_RECV_INT [72]
INPUT

R635 10K 0603 — V_M3V3
R638 0 0603 — GND
R649 10K 0603 — V_M3V3
R654 0 0603 — GND
R656 10K 0603 — V_M3V3
R659 0 0603 — GND
C1254 0.1 UF 0402

I2C ADDR = 0X20

P10 /F2_FF1_XMIT_PRESENT [69]
P11 /F2_FF1_RECV_PRESENT [69]
P12 /F2_FF2_XMIT_PRESENT [70]
P13 /F2_FF2_RECV_PRESENT [70]
P14 /F2_FF3_XMIT_PRESENT [71]
P15 /F2_FF3_RECV_PRESENT [71]
P16 /F2_FF4_XMIT_PRESENT [72]
P17 /F2_FF4_RECV_PRESENT [72]
INPUT

I2C_SCL_F2_FF3_XMIT [71]
I2C_SDA_F2_FF3_XMIT [71]
I2C_SCL_F2_FF3_RECV [71]
I2C_SDA_F2_FF3_RECV [71]
I2C_SCL_F2_FF6_XCVR [74]
I2C_SDA_F2_FF6_XCVR [74]
I2C_SCL_F2_FF4_XMIT [72]
I2C_SDA_F2_FF4_XMIT [72]
I2C_SCL_F2_FF4_RECV [72]
I2C_SDA_F2_FF4_RECV [72]

U11
TCA9548A

SCL, SDA, /RESET, A2, A1, A0, VCC, GND
SC0/SD0, SC1/SD1, SC2/SD2, SC3/SD3, SC4/SD4, SC5/SD5, SC6/SD6, SC7/SD7

R624 10K 0603 — V_M3V3
R631 0 0603 — GND
R607 10K 0603 — V_M3V3
R614 0 0603 — GND
R592 10K 0603 — V_M3V3
R598 DNP 0603 — GND
C1245 0.1 UF 0402

I2C ADDR = 0X71

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

V_M3V3
R628 2.2K 0603
R615 2.2K 0603

U12
TCA9555

SCL, SDA, A2, A1, A0, VCC, GND, /INT
P00 /F2_FF5_XCVR_INT [73]
P01 /F2_FF6_XCVR_INT [74]
P02 /F2_FF5_XCVR_PRESENT [73]
P03 /F2_FF6_XCVR_PRESENT [74]
P04
P05
P06
P07 /F2_FF_RESET [69,70,71,72,73,74]
INPUT
OUTPUT

R593 10K 0603 — V_M3V3
R599 0 0603 — GND
R608 10K 0603 — V_M3V3
R616 0 0603 — GND
R625 10K 0603 — V_M3V3
R632 DNP 0603 — GND
C1246 0.1 UF 0402

I2C ADDR = 0X21

P10 EN_F2_FF1_XMIT_3V8 [31]
P11 EN_F2_FF2_XMIT_3V8 [31]
P12 EN_F2_FF3_XMIT_3V8 [31]
P13 EN_F2_FF4_XMIT_3V8 [31]
P14 F2_FF1_XMIT_3V8_SEL [31]
P15 F2_FF2_XMIT_3V8_SEL [31]
P16 F2_FF3_XMIT_3V8_SEL [31]
P17 F2_FF4_XMIT_3V8_SEL [31]
OUTPUT
INPUT

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

I2C REGISTER PIN ASSIGNMENTS ARE SCRAMBLED COMPARED TO PREVIOUS CM VERSIONS

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5.01: FPGA#1 GND

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A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

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AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

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B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

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C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

U77-5
FPGA_VU13P_A2577

T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND
GND	

GND

GND Y6 R441 10K 0603 V_M3V3 /F1_INSTALLED [23]

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F1_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM v3

Title: 5.01: FPGA#1 GND

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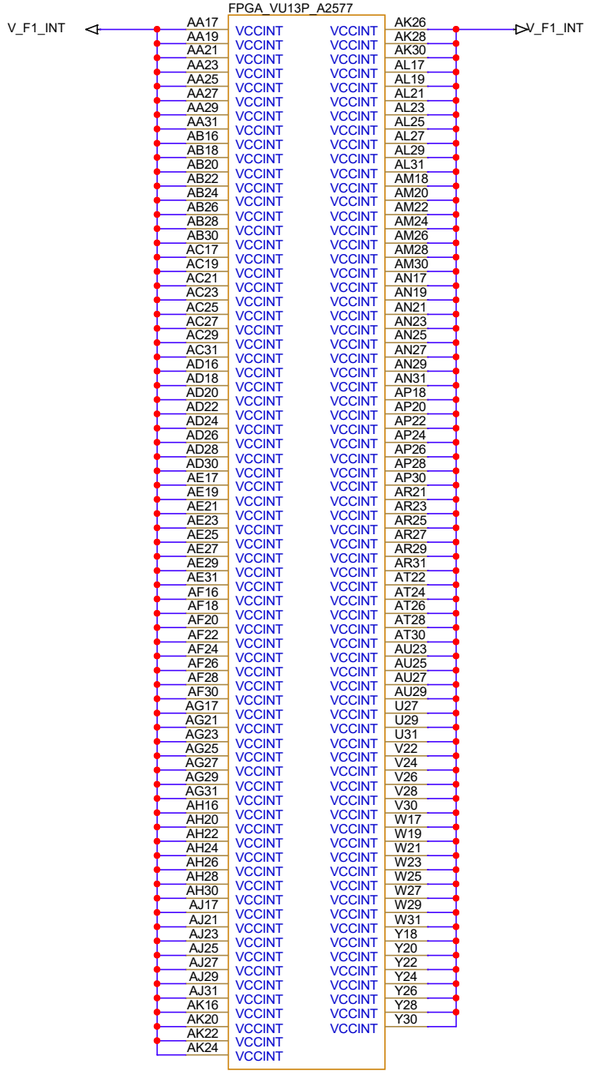
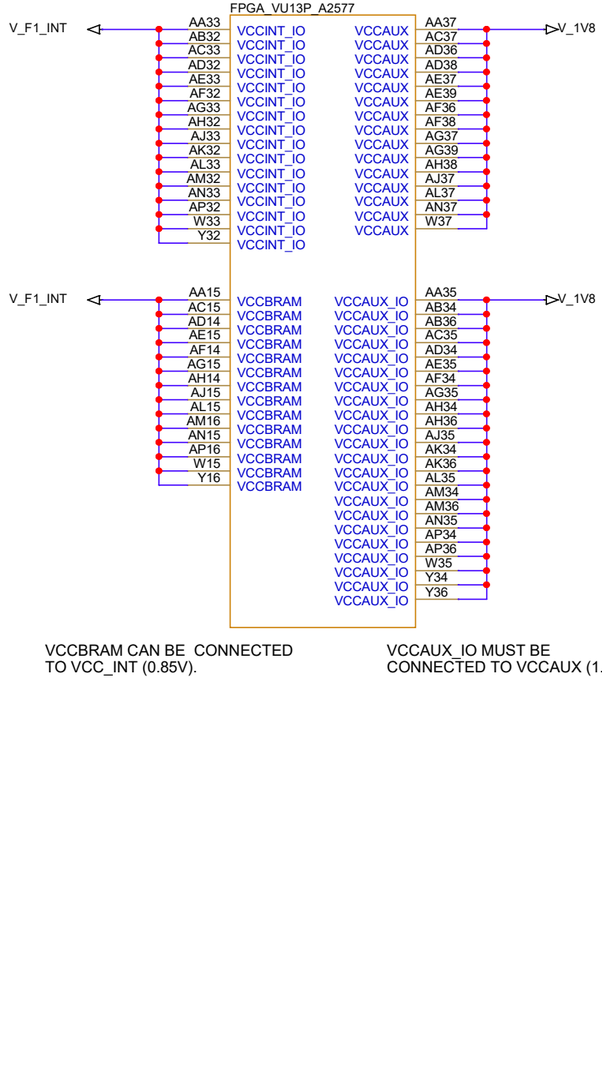
5.02: FPGA#1 POWER INTERNAL

VCCINT MUST BE 0.85V.

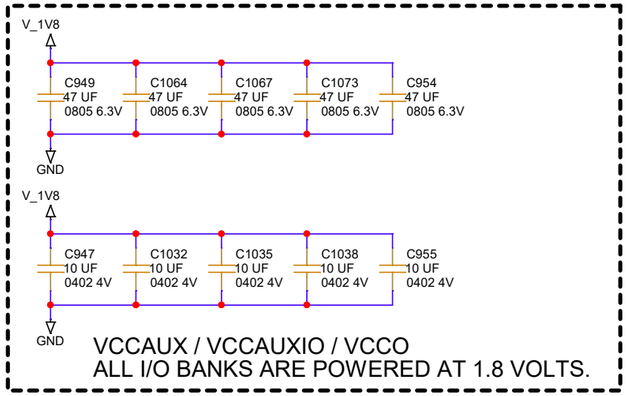


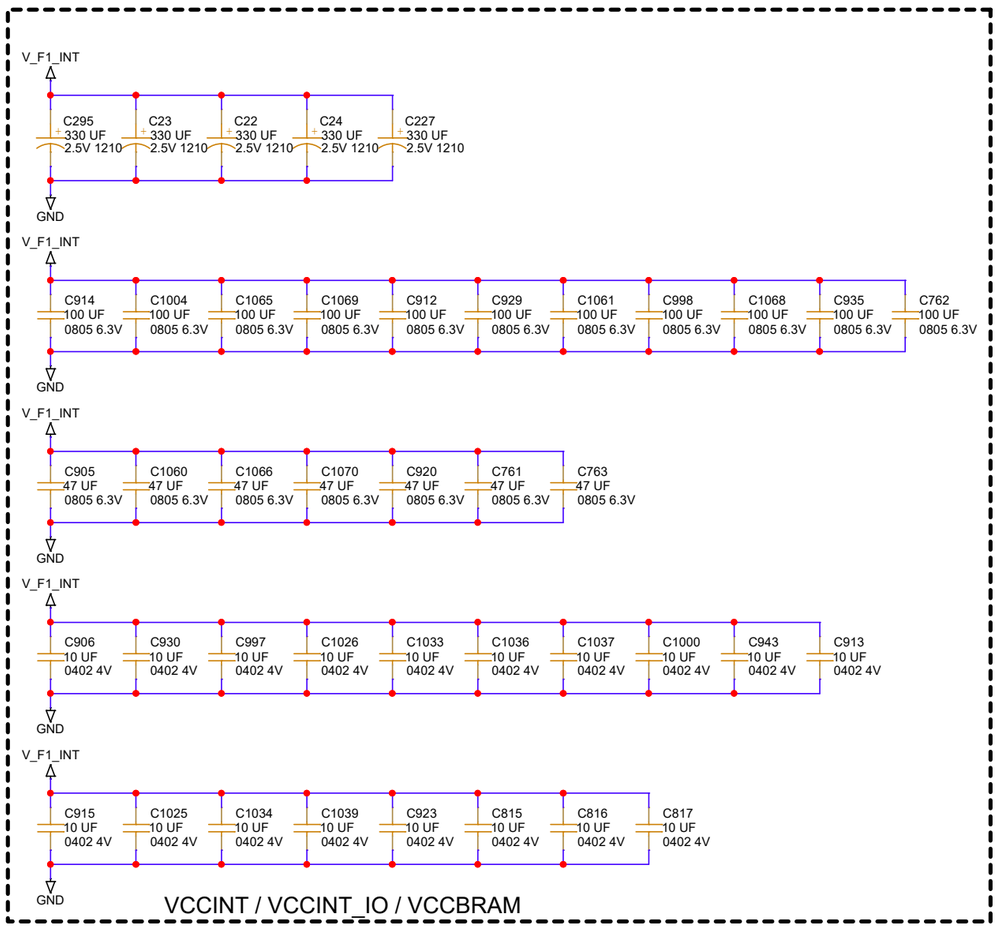
VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).



VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).





BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"UG583 UltraScale Architecture PCB Design"

APOLLO CM v3		
Title: 5.02: FPGA#1 POWER INTERNAL		
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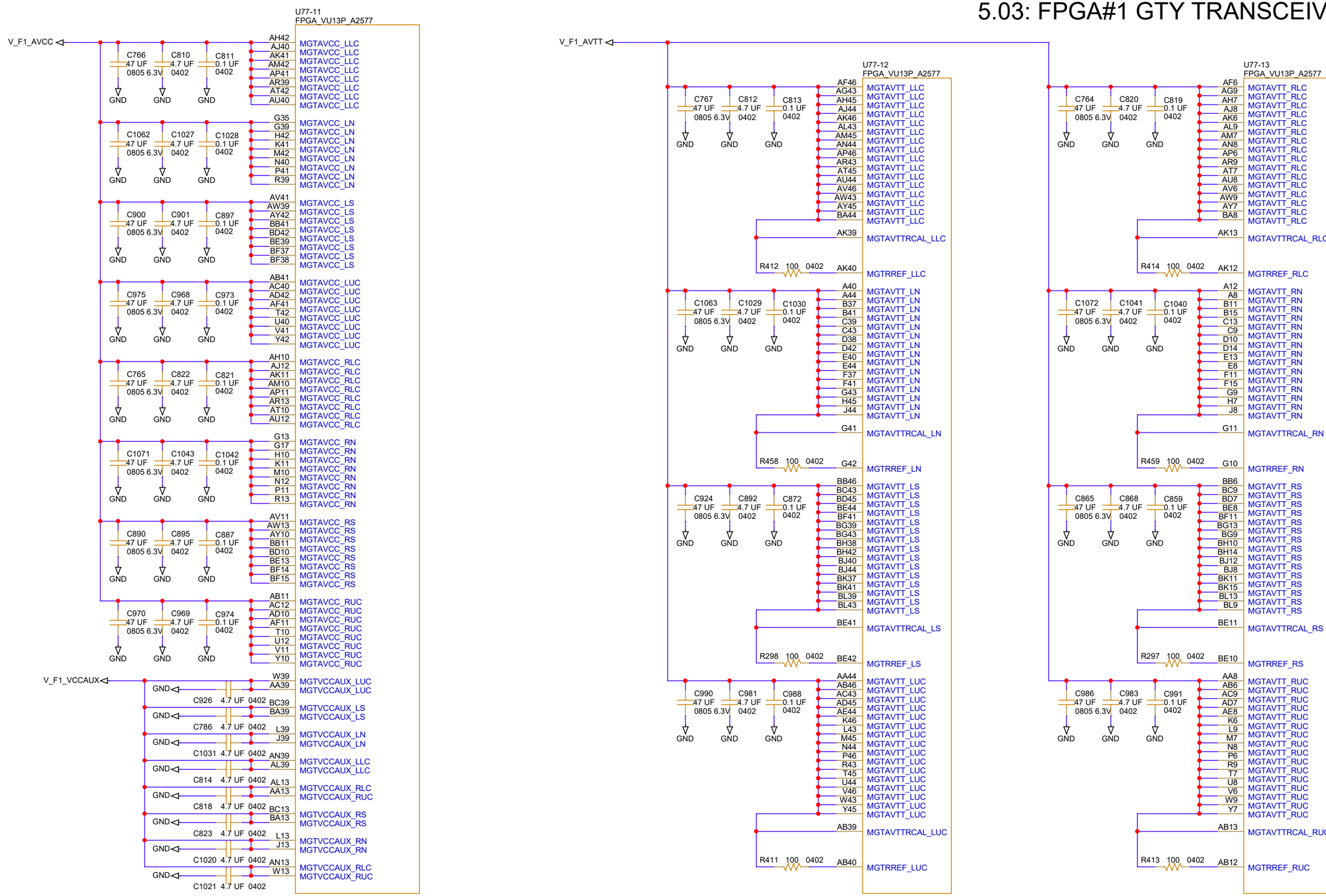
5.03: FPGA#1 GTY TRANSCEIVER POWER



REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM v3			
Title: 5.03: FPGA#1 GTY TRANSCEIVER POWER			
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5.04: FPGA#1 CONFIGURATION

MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

U77-10
FPGA_VU13P_A2577
BANK 0

V_F1_INT — R394 DNP 0402 — AC13 POR_OVERRIDE
GND — R397 0 0402 — AC13
GND — R428 0 0402 — P14 RSVDGND
V_1V8 — R436 DNP 0402 — M14 PUDC_B_0
GND — R433 0 0402 — M14
V_1V8 — R425 1K 0402 — V14 M2_0
V_1V8 — R420 DNP 0402 — Y14 M1_0
GND — R421 0 0402 — Y14
V_1V8 — R408 0 0402 — AB14 M0_0
GND — R410 DNP 0402 — AB14

VCCO_0: AE13, AG13 — V_1V8
C837 47 UF 0805 6.3V
R354 2.2K 0603
R370 4.7K 0603
R316 4.7K 0603

D00_MOSI_0: AY14
D01_DIN_0: AV14
D02_0: AT14
D03_0: AP14
RDWR_FCS_B_0: AM14
CCLK_0: AD13
PROGRAM_B_0: AK14
DONE_0: AJ13
INIT_B_0: T14
VBATT: BB14 — GND

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

R282 4.7K 0603 — V_1V8
R283 4.7K 0603 — V_1V8

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
VU13P 906,547,008

U85
MT25QU01

DQ0 15
DQ1 8
DQ2 9
DQ3 1
S# 7
CLK 16
DNU_3 3
DNU_4 4
DNU_5 5
DNU_6 6
DNU_11 11
DNU_12 12
DNU_13 13
DNU_14 14
VCC 2 — V_1V8
GND 10

C899 0.1 UF 0402

F1_CFG_DONE — /F1_CFG_DONE [23]
R389 4.7K 0603 — V_3V3
Q13 FET_N_1.8V

WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.

FPGA_CFG_FROM_FLASH [23,53] — Q15 FET_N_1.8V

R284 4.7K 0603 — V_1V8
F1_CFG_START [23] — Q14 FET_N_1.8V
R390 4.7K 0603 — GND

THE FPGA CAN BE REPROGRAMMED BY PULSING "F1_CFG_START" FROM THE MCU.

APOLLO CM v3		
Title: 5.04: FPGA#1 CONFIGURATION		
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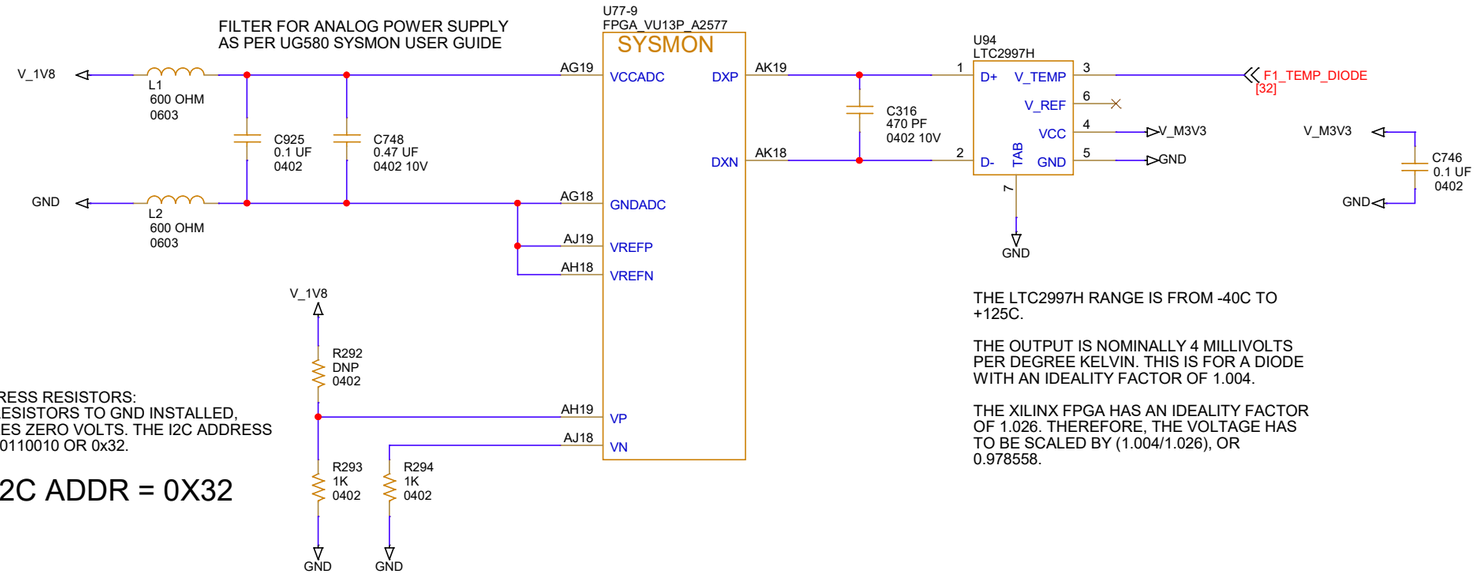
5.05: FPGA#1 SYSTEM MONITOR

FOR THE VU9P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0 AND SLR2.

FOR THE VU13P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0, SLR2, AND SLR3.

ONLY THE MASTER SLR IS ACCESSABLE FROM THE I2C CONNECTIONS.



SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

I2C ADDR = 0X32

THE LTC2997H RANGE IS FROM -40C TO +125C.

THE OUTPUT IS NOMINALLY 4 MILLIVOLTS PER DEGREE KELVIN. THIS IS FOR A DIODE WITH AN IDEALITY FACTOR OF 1.004.

THE XILINX FPGA HAS AN IDEALITY FACTOR OF 1.026. THEREFORE, THE VOLTAGE HAS TO BE SCALED BY (1.004/1.026), OR 0.978558.

APOLLO CM v3		
Title: 5.05: FPGA#1 SYSTEM MONITOR		
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5.06 FPGA#1 I/O SLR0

U77-14
FPGA_VU13P_A2577

BE20	IO_L10N_T1U_N7_QBC_AD4N_61	VCCO_61	AW27
BE21	IO_L10P_T1U_N6_QBC_AD4P_61	VCCO_61	AY24
BF22	IO_L11N_T1U_N9_GC_61	VCCO_61	BC25
BE22	IO_L11P_T1U_N8_GC_61	VCCO_61	BD22
BE23	IO_L12N_T1U_N11_GC_61	VCCO_61	BG23
BD23	IO_L12P_T1U_N10_GC_61	VCCO_61	BK24
BD24	IO_L13N_T2L_N1_GC_QBC_61	VREF_61	AV23
BD25	IO_L13P_T2L_N0_GC_QBC_61		
BC23	IO_L14N_T2L_N3_GC_61		
BC24	IO_L14P_T2L_N2_GC_61		
BB25	IO_L15N_T2L_N5_AD11N_61		
BB26	IO_L15P_T2L_N4_AD11P_61		
BD26	IO_L16N_T2U_N7_QBC_AD3N_61		
BC26	IO_L16P_T2U_N6_QBC_AD3P_61		
BA24	IO_L17N_T2U_N9_AD10N_61		
BA25	IO_L17P_T2U_N8_AD10P_61		
BC22	IO_L18N_T2U_N11_AD2N_61		
BB22	IO_L18P_T2U_N10_AD2P_61		
AW24	IO_L19N_T3L_N1_DBC_AD9N_61		
AW25	IO_L19P_T3L_N0_DBC_AD9P_61		
BL23	IO_L1N_T0L_N1_DBC_61		
BL24	IO_L1P_T0L_N0_DBC_61		
AW23	IO_L20N_T3L_N3_AD1N_61		
AV24	IO_L20P_T3L_N2_AD1P_61		
BA23	IO_L21N_T3L_N5_AD8N_61		
AY23	IO_L21P_T3L_N4_AD8P_61		
BA27	IO_L22N_T3U_N7_DBC_AD0N_61		
AY27	IO_L22P_T3U_N6_DBC_AD0P_61		
AY26	IO_L23N_T3U_N9_61		
AW26	IO_L23P_T3U_N8_61		
AV26	IO_L24N_T3U_N11_61		
AV27	IO_L24P_T3U_N10_61		
BL22	IO_L2N_T0L_N3_61		
BK22	IO_L2P_T0L_N2_61		
BJ24	IO_L3N_T0L_N5_AD15N_61		
BJ25	IO_L3P_T0L_N4_AD15P_61		
BK23	IO_L4N_T0U_N7_DBC_AD7N_61		
BJ23	IO_L4P_T0U_N6_DBC_AD7P_61		
BL25	IO_L5N_T0U_N9_AD14N_61		
BK25	IO_L5P_T0U_N8_AD14P_61		
BH23	IO_L6N_T0U_N11_AD6N_61		
BH24	IO_L6P_T0U_N10_AD6P_61		
BG24	IO_L7N_T1L_N1_QBC_AD13N_61		
BG25	IO_L7P_T1L_N0_QBC_AD13P_61		
BG22	IO_L8N_T1L_N3_AD5N_61		
BF23	IO_L8P_T1L_N2_AD5P_61		
BF24	IO_L9N_T1L_N5_AD12N_61		
BF25	IO_L9P_T1L_N4_AD12P_61		
BH22	IO_T0U_N12_VRP_61		
BE25	IO_T1U_N12_61		
BB24	IO_T2U_N12_61		
AY25	IO_T3U_N12_61		

V_1V8

OMIT "VREF" AND "VRP" RESISTORS
ON UNUSED I/O BANKS.

F1 LOGIC
TCDS 40MHZ INPUT

ac_nF1_TCDS40_CLK [21]
ac_pF1_TCDS40_CLK [21]
ac_nLHC_CLK_5 [13]
ac_pLHC_CLK_5 [13]

LHC_CLK
ALWAYS 40 MHZ

nF1_TEST_CONN_0 [49]
pF1_TEST_CONN_0 [49]

F1_TEST_CONN_5 [49]
F1_TEST_CONN_6 [49]

nF1_TEST_CONN_4 [49]
pF1_TEST_CONN_4 [49]
nF1_TEST_CONN_3 [49]
pF1_TEST_CONN_3 [49]
nF1_TEST_CONN_2 [49]
pF1_TEST_CONN_2 [49]
nF1_TEST_CONN_1 [49]
pF1_TEST_CONN_1 [49]

THIS IS THE 40 MHZ RECOVERED TCDS
CLOCK. USING BANK 62 KEEPS THIS
INTHE SAME SLR AS THE TCDS LOGIC.

bc_nF1_TCDS_RECOV_CLK [21]
bc_pF1_TCDS_RECOV_CLK [21]
nF2F1_SPARE2 [57]
pF2F1_SPARE2 [57]
nF2F1_SPARE1 [57]
pF2F1_SPARE1 [57]
nF2F1_SPARE0 [57]
pF2F1_SPARE0 [57]

GND R304 240 0402

U77-15
FPGA_VU13P_A2577

BH27	IO_L10N_T1U_N7_QBC_AD4N_62	VCCO_62	AV30
BH26	IO_L10P_T1U_N6_QBC_AD4P_62	VCCO_62	BA31
BF28	IO_L11N_T1U_N9_GC_62	VCCO_62	BB28
BF27	IO_L11P_T1U_N8_GC_62	VCCO_62	BE29
BE27	IO_L12N_T1U_N11_GC_62	VCCO_62	BF26
BE26	IO_L12P_T1U_N10_GC_62	VCCO_62	BH30
BD29	IO_L13N_T2L_N1_GC_QBC_62	VCCO_62	BJ27
BC28	IO_L13P_T2L_N0_GC_QBC_62	VREF_62	AV28
BE28	IO_L14N_T2L_N3_GC_62		
BD28	IO_L14P_T2L_N2_GC_62		
BE30	IO_L15N_T2L_N5_AD11N_62		
BD30	IO_L15P_T2L_N4_AD11P_62		
BC27	IO_L16N_T2U_N7_QBC_AD3N_62		
BB27	IO_L16P_T2U_N6_QBC_AD3P_62		
BC31	IO_L17N_T2U_N9_AD10N_62		
BB31	IO_L17P_T2U_N8_AD10P_62		
BC29	IO_L18N_T2U_N11_AD2N_62		
BB29	IO_L18P_T2U_N10_AD2P_62		
BA29	IO_L19N_T3L_N1_DBC_AD9N_62		
BA28	IO_L19P_T3L_N0_DBC_AD9P_62		
BJ28	IO_L1N_T0L_N1_DBC_62		
BH28	IO_L1P_T0L_N0_DBC_62		
AY28	IO_L20N_T3L_N3_AD1N_62		
AW28	IO_L20P_T3L_N2_AD1P_62		
BA30	IO_L21N_T3L_N5_AD8N_62		
AY30	IO_L21P_T3L_N4_AD8P_62		
AV31	IO_L22N_T3U_N7_DBC_AD0N_62		
AU31	IO_L22P_T3U_N6_DBC_AD0P_62		
AW29	IO_L23N_T3U_N9_62		
AV29	IO_L23P_T3U_N8_62		
AY31	IO_L24N_T3U_N11_62		
AW31	IO_L24P_T3U_N10_62		
BL28	IO_L2N_T0L_N3_62		
BL27	IO_L2P_T0L_N2_62		
BJ30	IO_L3N_T0L_N5_AD15N_62		
BJ29	IO_L3P_T0L_N4_AD15P_62		
BK28	IO_L4N_T0U_N7_DBC_AD7N_62		
BK27	IO_L4P_T0U_N6_DBC_AD7P_62		
BL30	IO_L5N_T0U_N9_AD14N_62		
BK30	IO_L5P_T0U_N8_AD14P_62		
BK26	IO_L6N_T0U_N11_AD6N_62		
BJ26	IO_L6P_T0U_N10_AD6P_62		
BG27	IO_L7N_T1L_N1_QBC_AD13N_62		
BG26	IO_L7P_T1L_N0_QBC_AD13P_62		
BG30	IO_L8N_T1L_N3_AD5N_62		
BF29	IO_L8P_T1L_N2_AD5P_62		
BH29	IO_L9N_T1L_N5_AD12N_62		
BG29	IO_L9P_T1L_N4_AD12P_62		
BL29	IO_T0U_N12_VRP_62		
BF30	IO_T1U_N12_62		
BB30	IO_T2U_N12_62		
AW30	IO_T3U_N12_62		

V_1V8

R364
1K
0402
GND

U77-16
FPGA_VU13P_A2577

BC36	IO_L10N_T1U_N7_QBC_AD4N_63	VCCO_63	AT36
BB36	IO_L10P_T1U_N6_QBC_AD4P_63	VCCO_63	AU33
BB35	IO_L11N_T1U_N9_GC_63	VCCO_63	AW37
BA35	IO_L11P_T1U_N8_GC_63	VCCO_63	AY34
BB34	IO_L12N_T1U_N11_GC_63	VCCO_63	BC35
BA34	IO_L12P_T1U_N10_GC_63	VCCO_63	BD32
AW36	IO_L13N_T2L_N1_GC_QBC_63	VREF_63	AR32
AW35	IO_L13P_T2L_N0_GC_QBC_63		
AY36	IO_L14N_T2L_N3_GC_63		
AY35	IO_L14P_T2L_N2_GC_63		
AV37	IO_L15N_T2L_N5_AD11N_63		
AV36	IO_L15P_T2L_N4_AD11P_63		
AV33	IO_L16N_T2U_N7_QBC_AD3N_63		
AV32	IO_L16P_T2U_N6_QBC_AD3P_63		
AW34	IO_L17N_T2U_N9_AD10N_63		
AW33	IO_L17P_T2U_N8_AD10P_63		
AY34	IO_L18N_T2U_N11_AD2N_63		
AU34	IO_L18P_T2U_N10_AD2P_63		
AU37	IO_L19N_T3L_N1_DBC_AD9N_63		
AU36	IO_L19P_T3L_N0_DBC_AD9P_63		
BE32	IO_L1N_T0L_N1_DBC_63		
BE31	IO_L1P_T0L_N0_DBC_63		
AU32	IO_L20N_T3L_N3_AD1N_63		
AT32	IO_L20P_T3L_N2_AD1P_63		
AR37	IO_L21N_T3L_N5_AD8N_63		
AR36	IO_L21P_T3L_N4_AD8P_63		
AT34	IO_L22N_T3U_N7_DBC_AD0N_63		
AT33	IO_L22P_T3U_N6_DBC_AD0P_63		
AT35	IO_L23N_T3U_N9_63		
AR35	IO_L23P_T3U_N8_63		
AR34	IO_L24N_T3U_N11_63		
AR33	IO_L24P_T3U_N10_63		
BC32	IO_L2N_T0L_N3_63		
BB32	IO_L2P_T0L_N2_63		
BA32	IO_L3N_T0L_N5_AD15N_63		
AY32	IO_L3P_T0L_N4_AD15P_63		
BA33	IO_L4N_T0U_N7_DBC_AD7N_63		
AY33	IO_L4P_T0U_N6_DBC_AD7P_63		
BD33	IO_L5N_T0U_N9_AD14N_63		
BC33	IO_L5P_T0U_N8_AD14P_63		
BD34	IO_L6N_T0U_N11_AD6N_63		
BC34	IO_L6P_T0U_N10_AD6P_63		
BD36	IO_L7N_T1L_N1_QBC_AD13N_63		
BD35	IO_L7P_T1L_N0_QBC_AD13P_63		
BD37	IO_L8N_T1L_N3_AD5N_63		
BC37	IO_L8P_T1L_N2_AD5P_63		
BB37	IO_L9N_T1L_N5_AD12N_63		
BA37	IO_L9P_T1L_N4_AD12P_63		
BD31	IO_T0U_N12_VRP_63		
AY37	IO_T1U_N12_63		
AU35	IO_T2U_N12_63		
AT37	IO_T3U_N12_63		

V_1V8

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

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Title: 5.06 FPGA#1 I/O SLR0			
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5.07 FPGA#1 I/O SLR1

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

U77-17
FPGA_VU13P_A2577

VCCO_65 AR19 — V_1V8
VCCO_65 AV20
VCCO_65 AW17
VCCO_65 BA21
VCCO_65 BB18
VCCO_65 BC15
VREF_65 AR20 — R384 1K 0402 — GND

I2C_SDA_F1_SYSMON [37] — BC16 65_L23N_PERSTN1_I2C_SDA
I2C_SCL_F1_SYSMON [37] — BB16 65_L23P_I2C_SCLK

BD15 65_L24N_DOUT_CSO_B
BD16 65_L24P_EMCCLK
BD17 65_L22N_DBC_AD0N_D05
BD18 65_L22P_DBC_AD0P_D04
BC17 65_L21N_AD8N_D07
BB17 65_L21P_AD8P_D06
BA18 65_L20N_AD1N_D09
BA19 65_L20P_AD1P_D08
BC18 65_L19N_DBC_AD9N_D11
BC19 65_L19P_DBC_AD9P_D10
AW15 65_L18N_AD2N_D13
AV16 65_L18P_AD2P_D12
BA15 65_L17N_AD10N_D15
AY15 65_L17P_AD10P_D14
AV17 65_L16N_QBC_AD3N_A01_D17
AU17 65_L16P_QBC_AD3P_A00_D16
AY16 65_L15N_AD11N_A03_D19
AW16 65_L15P_AD11P_A02_D18
BA17 65_L14N_GC_A05_D21
AY17 65_L14P_GC_A04_D20
AY18 65_L13N_GC_QBC_A07_D23
AW18 65_L13P_GC_QBC_A06_D22
AV19 65_L12N_GC_A09_D25
AU19 65_L12P_GC_A08_D24
AW19 65_L11N_GC_A11_D27
AW20 65_L11P_GC_A10_D26
AT18 65_L10N_QBC_AD4N_A13_D29
AR18 65_L10P_QBC_AD4P_A12_D28
AU20 65_L9N_AD12N_A15_D31
AU21 65_L9P_AD12P_A14_D30
AT19 65_L8N_AD5N_A17
AT20 65_L8P_AD5P_A16
AV21 65_L7N_QBC_AD13N_A19
AV22 65_L7P_QBC_AD13P_A18
BA20 65_L6N_AD6N_A21
AY20 65_L6P_AD6P_A20
BB19 65_L5N_AD14N_A23
BB20 65_L5P_AD14P_A22
AY21 65_L4N_DBC_AD7N_A25
AW21 65_L4P_DBC_AD7P_A24
BD19 65_L3N_AD15N_A27
BD20 65_L3P_AD15P_A26
BA22 65_L2N_FWE_FCS2_B
AY22 65_L2P_FOE_B
BC21 65_L1N_DBC_RS1
BB21 65_L1P_DBC_RS0
BB15 65_PERSTN0
AV18 65_CSI_ADV_B
AU22 65_SMBALERT
BD21 65_VRP_A28

GND — R357 240 0402 — BD21

U77-55
FPGA_VU13P_A2577

AR16 IO_L11N_T1U_N9_GC_66
AR17 IO_L11P_T1U_N8_GC_66
AU16 IO_L12N_T1U_N11_GC_66
AT17 IO_L12P_T1U_N10_GC_66
AT15 IO_T0U_N12_VRP_66
AU15 IO_T3U_N12_66

VCCO_66 AT16 — V_1V8
VREF_66 AR15 — R398 1K 0402 — GND

ac_nF1_XTAL_200 [16] — AU16
ac_pF1_XTAL_200 [16] — AT17
GND — R372 240 0402 — AT15

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5.08: FPGA#1 I/O SLR2

THESE ARE LOGIC-CIRCUIT CLOCKS SOURCED FROM AN ON-BOARD OSCILLATOR, EITHER DIRECTLY OR THROUGH A SYNTHESIZER. THEY MUST BE CONNECTED TO A GLOBAL CLOCK INPUT.

VERIFY THAT A GENERIC I2C BUS CAN BE CONNECTED HERE.

THE TRI-COLOR LED IS CONNECTED TO DIFFERENT PINS ON EACH FPGA, IN ORDER TO SIMPLIFY LAYOUT.

PIN B29 IS PULLED HIGH ON FPGA#1 AND IS TIED TO GND ON FPGA#2. IT ALLOWS THE FIRMWARE TO KNOW WHICH FPGA IT IS RUNNING IN.

THE "F2F1_SPARE" SIGNALS ARE OUTPUTS FROM F2 AND INPUTS TO F1.
THE "F1F2_SPARE" SIGNALS ARE OUTPUTS FROM F1 AND INPUTS TO F2.
THEY ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

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Title: 5.08: FPGA#1 I/O SLR2		
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5.09: FPGA#1 I/O SLR3

THE "F1_HDRnn" SIGNALS ARE CONNECTED FROM THE FPGA TO PADS ON THE BOTTOM SIDE OF THE BOARD. A 20-PIN HEADER CAN BE ATTACHED. THESE SIGNALS ARE FOR DEBUGGING, OR FUTURE USE. HDR01 AND HDR02 ARE CONNECTED TO CLOCK-CAPABLE INPUTS.

J8
CON20A

2	1	F1_HDR01	
4	3	F1_HDR02	
6	5	F1_HDR03	
8	7	F1_HDR04	
10	9	F1_HDR05	
12	11	F1_HDR06	
14	13	F1_HDR07	
16	15	F1_HDR08	
18	17	F1_HDR09	
20	19	F1_HDR10	

GND

U77-20
FPGA_VU13P_A2577

M31	IO_L10N_T1U_N7_QBC_AD4N_73		
N31	IO_L10P_T1U_N6_QBC_AD4P_73		
M27	IO_L11N_T1U_N9_GC_73		
N27	IO_L11P_T1U_N8_GC_73		
F1_HDR02	L29	IO_L12N_T1U_N11_GC_73	
F1_HDR01	L28	IO_L12P_T1U_N10_GC_73	
K28	IO_L13N_T2L_N1_GC_QBC_73		
K27	IO_L13P_T2L_N0_GC_QBC_73		
L27	IO_L14N_T2L_N3_GC_73		
M26	IO_L14P_T2L_N2_GC_73		
G26	IO_L15N_T2L_N5_AD11N_73		
G25	IO_L15P_T2L_N4_AD11P_73		
F27	IO_L16N_T2U_N7_QBC_AD3N_73		
G27	IO_L16P_T2U_N6_QBC_AD3P_73		
J26	IO_L17N_T2U_N9_AD10N_73		
K26	IO_L17P_T2U_N8_AD10P_73		
H26	IO_L18N_T2U_N11_AD2N_73		
J25	IO_L18P_T2U_N10_AD2P_73		
E25	IO_L19N_T3L_N1_DBC_AD9N_73		
F25	IO_L19P_T3L_N0_DBC_AD9P_73		
R30	IO_L1N_T0L_N1_DBC_73		
T30	IO_L1P_T0L_N0_DBC_73		
E27	IO_L20N_T3L_N3_AD1N_73		
E26	IO_L20P_T3L_N2_AD1P_73		
F1_HDR04	B26	IO_L21N_T3L_N5_AD8N_73	
F1_HDR03	C26	IO_L21P_T3L_N4_AD8P_73	
A27	IO_L22N_T3U_N7_DBC_AD0N_73		
B27	IO_L22P_T3U_N6_DBC_AD0P_73		
F1_HDR05	A25	IO_L23N_T3U_N9_73	
F1_HDR06	B25	IO_L23P_T3U_N8_73	
C27	IO_L24N_T3U_N11_73		
D26	IO_L24P_T3U_N10_73		
T29	IO_L2N_T0L_N3_73		
T28	IO_L2P_T0L_N2_73		
T27	IO_L3N_T0L_N5_AD15N_73		
U26	IO_L3P_T0L_N4_AD15P_73		
P28	IO_L4N_T0U_N7_DBC_AD7N_73		
R28	IO_L4P_T0U_N6_DBC_AD7P_73		
R27	IO_L5N_T0U_N9_AD14N_73		
R26	IO_L5P_T0U_N8_AD14P_73		
P30	IO_L6N_T0U_N11_AD6N_73		
P29	IO_L6P_T0U_N10_AD6P_73		
N26	IO_L7N_T1L_N1_QBC_AD13N_73		
P26	IO_L7P_T1L_N0_QBC_AD13P_73		
M30	IO_L8N_T1L_N3_AD5N_73		
M29	IO_L8P_T1L_N2_AD5P_73		
N29	IO_L9N_T1L_N5_AD12N_73		
N28	IO_L9P_T1L_N4_AD12P_73		
T31	IO_T0U_N12_VRP_73		
J28	IO_T1U_N12_73		
H27	IO_T2U_N12_73		
D25	IO_T3U_N12_73		

VCCO_73	C25	V_1V8	
VCCO_73	F26		
VCCO_73	J27		
VCCO_73	M28		
VCCO_73	R29		
VCCO_73	T26		
VREF_73	U25	R438 1K 0402	GND

GND
R437
240
0402

U77-21
FPGA_VU13P_A2577

H23	IO_L10N_T1U_N7_QBC_AD4N_74		
J23	IO_L10P_T1U_N6_QBC_AD4P_74		
J21	IO_L11N_T1U_N9_GC_74		
K21	IO_L11P_T1U_N8_GC_74		
K22	IO_L12N_T1U_N11_GC_74		
K23	IO_L12P_T1U_N10_GC_74		
L22	IO_L13N_T2L_N1_GC_QBC_74		
L23	IO_L13P_T2L_N0_GC_QBC_74		
M21	IO_L14N_T2L_N3_GC_74		
M22	IO_L14P_T2L_N2_GC_74		
L24	IO_L15N_T2L_N5_AD11N_74		
M25	IO_L15P_T2L_N4_AD11P_74		
M24	IO_L16N_T2U_N7_QBC_AD3N_74		
N24	IO_L16P_T2U_N6_QBC_AD3P_74		
N21	IO_L17N_T2U_N9_AD10N_74		
N22	IO_L17P_T2U_N8_AD10P_74		
K25	IO_L18N_T2U_N11_AD2N_74		
L25	IO_L18P_T2U_N10_AD2P_74		
T23	IO_L19N_T3L_N1_DBC_AD9N_74		
T24	IO_L19P_T3L_N0_DBC_AD9P_74		
D23	IO_L1N_T0L_N1_DBC_74		
E23	IO_L1P_T0L_N0_DBC_74		
R25	IO_L20N_T3L_N3_AD1N_74		
T25	IO_L20P_T3L_N2_AD1P_74		
U22	IO_L21N_T3L_N5_AD8N_74		
U23	IO_L21P_T3L_N4_AD8P_74		
P24	IO_L22N_T3U_N7_DBC_AD0N_74		
P25	IO_L22P_T3U_N6_DBC_AD0P_74		
R22	IO_L23N_T3U_N9_74		
T22	IO_L23P_T3U_N8_74		
P23	IO_L24N_T3U_N11_74		
R23	IO_L24P_T3U_N10_74		
F1_HDR08	B24	IO_L2N_T0L_N3_74	
C24	IO_L2P_T0L_N2_74		
F1_HDR09	A23	IO_L3N_T0L_N5_AD15N_74	
F1_HDR07	A24	IO_L3P_T0L_N4_AD15P_74	
E22	IO_L4N_T0U_N7_DBC_AD7N_74		
F22	IO_L4P_T0U_N6_DBC_AD7P_74		
C22	IO_L5N_T0U_N9_AD14N_74		
C23	IO_L5P_T0U_N8_AD14P_74		
F1_HDR10	A22	IO_L6N_T0U_N11_AD6N_74	
B22	IO_L6P_T0U_N10_AD6P_74		
G24	IO_L7N_T1L_N1_QBC_AD13N_74		
H24	IO_L7P_T1L_N0_QBC_AD13P_74		
F23	IO_L8N_T1L_N3_AD5N_74		
F24	IO_L8P_T1L_N2_AD5P_74		
G22	IO_L9N_T1L_N5_AD12N_74		
H22	IO_L9P_T1L_N4_AD12P_74		
D24	IO_T0U_N12_VRP_74		
J24	IO_T1U_N12_74		
N23	IO_T2U_N12_74		
P21	IO_T3U_N12_74		

VCCO_74	D22	V_1V8	
VCCO_74	G23		
VCCO_74	K24		
VCCO_74	L21		
VCCO_74	N25		
VCCO_74	P22		
VREF_74	U24	R439 1K 0402	GND

GND
R448
240
0402

U77-22
FPGA_VU13P_A2577

T19	IO_L10N_T1U_N7_QBC_AD4N_75		
T20	IO_L10P_T1U_N6_QBC_AD4P_75		
P18	IO_L11N_T1U_N9_GC_75		
P19	IO_L11P_T1U_N8_GC_75		
R17	IO_L12N_T1U_N11_GC_75		
R18	IO_L12P_T1U_N10_GC_75		
M17	IO_L13N_T2L_N1_GC_QBC_75		
N17	IO_L13P_T2L_N0_GC_QBC_75		
N18	IO_L14N_T2L_N3_GC_75		
N19	IO_L14P_T2L_N2_GC_75		
P15	IO_L15N_T2L_N5_AD11N_75		
P16	IO_L15P_T2L_N4_AD11P_75		
L19	IO_L16N_T2U_N7_QBC_AD3N_75		
M19	IO_L16P_T2U_N6_QBC_AD3P_75		
M16	IO_L17N_T2U_N9_AD10N_75		
N16	IO_L17P_T2U_N8_AD10P_75		
L17	IO_L18N_T2U_N11_AD2N_75		
L18	IO_L18P_T2U_N10_AD2P_75		
K15	IO_L19N_T3L_N1_DBC_AD9N_75		
K16	IO_L19P_T3L_N0_DBC_AD9P_75		
T15	IO_L1N_T0L_N1_DBC_75		
U15	IO_L1P_T0L_N0_DBC_75		
L15	IO_L20N_T3L_N3_AD1N_75		
M15	IO_L20P_T3L_N2_AD1P_75		
J15	IO_L21N_T3L_N5_AD8N_75		
J16	IO_L21P_T3L_N4_AD8P_75		
K17	IO_L22N_T3U_N7_DBC_AD0N_75		
K18	IO_L22P_T3U_N6_DBC_AD0P_75		
J18	IO_L23N_T3U_N9_75		
J19	IO_L23P_T3U_N8_75		
K20	IO_L24N_T3U_N11_75		
L20	IO_L24P_T3U_N10_75		
V18	IO_L2N_T0L_N3_75		
V19	IO_L2P_T0L_N2_75		
U16	IO_L3N_T0L_N5_AD15N_75		
U17	IO_L3P_T0L_N4_AD15P_75		
V16	IO_L4N_T0U_N7_DBC_AD7N_75		
V17	IO_L4P_T0U_N6_DBC_AD7P_75		
U19	IO_L5N_T0U_N9_AD14N_75		
U20	IO_L5P_T0U_N8_AD14P_75		
V15	IO_L6N_T0U_N11_AD6N_75		
W16	IO_L6P_T0U_N10_AD6P_75		
R15	IO_L7N_T1L_N1_QBC_AD13N_75		
R16	IO_L7P_T1L_N0_QBC_AD13P_75		
T17	IO_L8N_T1L_N3_AD5N_75		
T18	IO_L8P_T1L_N2_AD5P_75		
P20	IO_L9N_T1L_N5_AD12N_75		
R20	IO_L9P_T1L_N4_AD12P_75		
V21	IO_T0U_N12_VRP_75		
R21	IO_T1U_N12_75		
M20	IO_T2U_N12_75		
J20	IO_T3U_N12_75		

ac_nF1R_X12_R0_CLK	[19]		
ac_pF1R_X12_R0_CLK	[19]		
ac_nF1R_X4_R0_CLK	[19]		
ac_pF1R_X4_R0_CLK	[19]		

VCCO_75	J17	V_1V8	
VCCO_75	M18		
VCCO_75	N15		
VCCO_75	R19		
VCCO_75	T16		
VCCO_75	V20		
VREF_75	U21	R424 1K 0402	GND

GND
R419
240
0402

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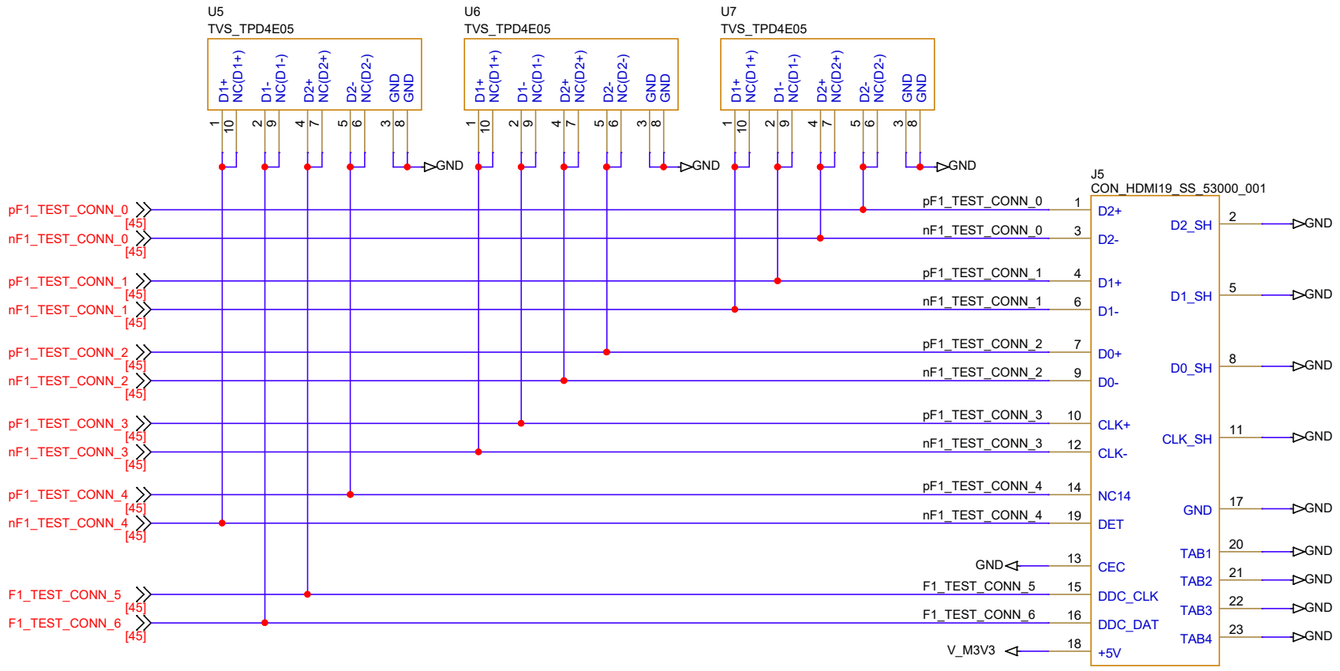
5.10: FPGA#1 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

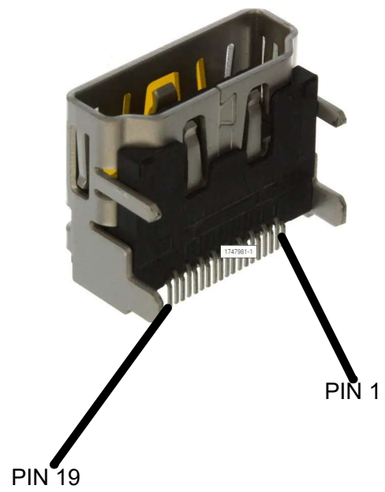
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

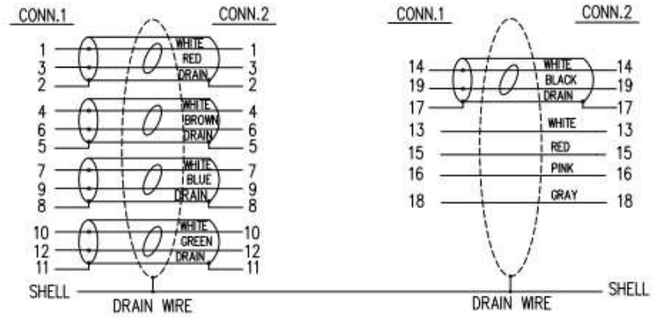
THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F1_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



PIN ASSIGNMENT





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6.01: FPGA#2 GND

U78-1
FPGA_VU13P_A2577

A13	GND	GND	AE12
A16	GND	GND	AE16
A17	GND	GND	AE18
A18	GND	GND	AE20
A21	GND	GND	AE22
A26	GND	GND	AE24
A31	GND	GND	AE26
A34	GND	GND	AE28
A35	GND	GND	AE3
A36	GND	GND	AE30
A39	GND	GND	AE32
A4	GND	GND	AE34
A43	GND	GND	AE36
A45	GND	GND	AE38
A48	GND	GND	AE4
A7	GND	GND	AE40
A9	GND	GND	AE43
AA12	GND	GND	AE47
AA14	GND	GND	AE48
AA16	GND	GND	AE49
AA18	GND	GND	AE5
AA20	GND	GND	AE9
AA22	GND	GND	AF1
AA24	GND	GND	AF10
AA26	GND	GND	AF12
AA28	GND	GND	AF15
AA3	GND	GND	AF17
AA30	GND	GND	AF19
AA32	GND	GND	AF2
AA34	GND	GND	AF21
AA36	GND	GND	AF23
AA38	GND	GND	AF25
AA4	GND	GND	AF27
AA40	GND	GND	AF29
AA43	GND	GND	AF31
AA47	GND	GND	AF33
AA48	GND	GND	AF35
AA49	GND	GND	AF37
AA5	GND	GND	AF39
AA9	GND	GND	AF40
AB1	GND	GND	AF42
AB10	GND	GND	AF45
AB15	GND	GND	AF47
AB17	GND	GND	AF5
AB19	GND	GND	AF50
AB2	GND	GND	AF51
AB21	GND	GND	AF7
AB23	GND	GND	AG12
AB25	GND	GND	AG16
AB27	GND	GND	AG20
AB29	GND	GND	AG22
AB31	GND	GND	AG24
AB33	GND	GND	AG26
AB35	GND	GND	AG28
AB37	GND	GND	AG3
AB38	GND	GND	AG30
AB42	GND	GND	AG32
AB45	GND	GND	AG34
AB47	GND	GND	AG36
AB5	GND	GND	AG38
AB50	GND	GND	AG4
AB51	GND	GND	AG40
AB7	GND	GND	AG44
AC14	GND	GND	AG47
AC16	GND	GND	AG48
AC18	GND	GND	AG49
AC20	GND	GND	AG5
AC22	GND	GND	AG8
AC24	GND	GND	AH1
AC26	GND	GND	AH11
AC28	GND	GND	AH12
AC3	GND	GND	AH15
AC30	GND	GND	AH17
AC32	GND	GND	AH2
AC34	GND	GND	AH21
AC36	GND	GND	AH23
AC38	GND	GND	AH25
AC39	GND	GND	AH27
AC4	GND	GND	AH29
AC44	GND	GND	AH31
AC47	GND	GND	AH33
AC48	GND	GND	AH35
AC49	GND	GND	AH37
AC5	GND	GND	AH39
AC8	GND	GND	AH40
AD1	GND	GND	AH41
AD11	GND	GND	AH46
AD12	GND	GND	AH47
AD15	GND	GND	AH5
AD17	GND	GND	AH50
AD19	GND	GND	AH51
AD2	GND	GND	AH6
AD21	GND	GND	AJ14
AD23	GND	GND	AJ16
AD25	GND	GND	AJ20
AD27	GND	GND	AJ22
AD29	GND	GND	AJ24
AD31	GND	GND	AJ26
AD33	GND	GND	AJ28
AD35	GND	GND	AJ3
AD37	GND	GND	AJ30
AD39	GND	GND	AJ32
AD40	GND	GND	AJ34
AD41	GND	GND	AJ36
AD46	GND	GND	AJ38
AD47	GND	GND	AJ39
AD5	GND	GND	AJ47
AD50	GND	GND	AJ43
AD51	GND	GND	AJ48
AD6	GND	GND	AJ4

GND GND

U78-2
FPGA_VU13P_A2577

AJ49	GND	GND	AP42
AJ5	GND	GND	AP45
AJ9	GND	GND	AP47
AK1	GND	GND	AP5
AK10	GND	GND	AP50
AK15	GND	GND	AP51
AK17	GND	GND	AP7
AK2	GND	GND	AR12
AK21	GND	GND	AR14
AK23	GND	GND	AR22
AK25	GND	GND	AR24
AK27	GND	GND	AR26
AK29	GND	GND	AR28
AK31	GND	GND	AR3
AK33	GND	GND	AR30
AK35	GND	GND	AR38
AK37	GND	GND	AR4
AK38	GND	GND	AR40
AK42	GND	GND	AR44
AK45	GND	GND	AR47
AK47	GND	GND	AR48
AK5	GND	GND	AR49
AK50	GND	GND	AR5
AK51	GND	GND	AR8
AK7	GND	GND	AT1
AL12	GND	GND	AT11
AL14	GND	GND	AT2
AL16	GND	GND	AT21
AL18	GND	GND	AT23
AL20	GND	GND	AT25
AL22	GND	GND	AT27
AL24	GND	GND	AT29
AL26	GND	GND	AT31
AL28	GND	GND	AT38
AL3	GND	GND	AT41
AL30	GND	GND	AT46
AL32	GND	GND	AT47
AL34	GND	GND	AT5
AL36	GND	GND	AT50
AL38	GND	GND	AT51
AL4	GND	GND	AT6
AL40	GND	GND	AU13
AL44	GND	GND	AU14
AL47	GND	GND	AU18
AL48	GND	GND	AU24
AL49	GND	GND	AU26
AL5	GND	GND	AU28
AL8	GND	GND	AU3
AM1	GND	GND	AU30
AM11	GND	GND	AU38
AM15	GND	GND	AU39
AM17	GND	GND	AU4
AM19	GND	GND	AU43
AM2	GND	GND	AU47
AM21	GND	GND	AU48
AM23	GND	GND	AU49
AM25	GND	GND	AU5
AM27	GND	GND	AU9
AM29	GND	GND	AV1
AM31	GND	GND	AV10
AM33	GND	GND	AV15
AM35	GND	GND	AV2
AM37	GND	GND	AV25
AM38	GND	GND	AV35
AM41	GND	GND	AV38
AM46	GND	GND	AV42
AM47	GND	GND	AV45
AM5	GND	GND	AV47
AM50	GND	GND	AV5
AM51	GND	GND	AV50
AM6	GND	GND	AV51
AN12	GND	GND	AV7
AN14	GND	GND	AW12
AN16	GND	GND	AW14
AN18	GND	GND	AW22
AN20	GND	GND	AW3
AN22	GND	GND	AW32
AN24	GND	GND	AW38
AN26	GND	GND	AW4
AN28	GND	GND	AW40
AN3	GND	GND	AW44
AN30	GND	GND	AW47
AN32	GND	GND	AW48
AN34	GND	GND	AW49
AN36	GND	GND	AW5
AN38	GND	GND	AW8
AN4	GND	GND	AY1
AN40	GND	GND	AY11
AN43	GND	GND	AY19
AN47	GND	GND	AY2
AN48	GND	GND	AY29
AN49	GND	GND	AY38
AN5	GND	GND	AY41
AN9	GND	GND	AY46
AP1	GND	GND	AY47
AP10	GND	GND	AY5
AP15	GND	GND	AY50
AP17	GND	GND	AY51
AP19	GND	GND	AY6
AP2	GND	GND	B10
AP21	GND	GND	B14
AP23	GND	GND	B16
AP25	GND	GND	B19
AP27	GND	GND	B20
AP29	GND	GND	B21
AP31	GND	GND	B23
AP33	GND	GND	B3
AP35	GND	GND	B31
AP37	GND	GND	B32
AP38	GND	GND	B33

GND GND

U78-3
FPGA_VU13P_A2577

B36	GND	GND	BG12
B38	GND	GND	BG16
B4	GND	GND	BG17
B42	GND	GND	BG18
B45	GND	GND	BG21
B46	GND	GND	BG28
B47	GND	GND	BG3
B48	GND	GND	BG31
B49	GND	GND	BG34
B5	GND	GND	BG35
B6	GND	GND	BG36
B7	GND	GND	BG4
BA12	GND	GND	BG40
BA14	GND	GND	BG44
BA16	GND	GND	BG45
BA26	GND	GND	BG48
BA3	GND	GND	BG49
BA36	GND	GND	BG7
BA38	GND	GND	BG8
BA4	GND	GND	BH1
BA40	GND	GND	BH11
BA43	GND	GND	BH15
BA47	GND	GND	BH16
BA48	GND	GND	BH19
BA49	GND	GND	BH2
BA5	GND	GND	BH20
BA9	GND	GND	BH21
BB1	GND	GND	BH25
BB10	GND	GND	BH31
BB2	GND	GND	BH32
BB23	GND	GND	BH33
BB33	GND	GND	BH36
BB38	GND	GND	BH37
BB42	GND	GND	BH41
BB45	GND	GND	BH45
BB47	GND	GND	BH46
BB5	GND	GND	BH47
BB50	GND	GND	BH5
BB51	GND	GND	BH50
BB7	GND	GND	BH51
BC12	GND	GND	BH6
BC14	GND	GND	BH7
BC20	GND	GND	BJ13
BC3	GND	GND	BJ16
BC30	GND	GND	BJ17
BC38	GND	GND	BJ18
BC4	GND	GND	BJ2
BC40	GND	GND	BJ21
BC44	GND	GND	BJ22
BC47	GND	GND	BJ3
BC48	GND	GND	BJ31
BC49	GND	GND	BJ34
BC5	GND	GND	BJ35
BC8	GND	GND	BJ36
BD1	GND	GND	BJ39
BD11	GND	GND	BJ4
BD14	GND	GND	BJ43
BD2	GND	GND	BJ45
BD27	GND	GND	BJ48
BD38	GND	GND	BJ49
BD41	GND	GND	BJ50
BD46	GND	GND	BJ7
BD47	GND	GND	BJ9
BD5	GND	GND	BK10
BD50	GND	GND	BK14
BD51	GND	GND	BK16
BD6	GND	GND	BK19
BE12	GND	GND	BK20
BE14	GND	GND	BK21
BE15	GND	GND	BK29
BE16	GND	GND	BK3
BE17	GND	GND	BK31
BE18	GND	GND	BK32
BE19	GND	GND	BK33
BE24	GND	GND	BK36
BE3	GND	GND	BK38
BE33	GND	GND	BK4
BE34	GND	GND	BK42
BE35	GND	GND	BK45
BE36	GND	GND	BK46
BE37	GND	GND	BK47
BE38	GND	GND	BK48
BE4	GND	GND	BK49
BE40	GND	GND	BK5
BE43	GND	GND	BK6
BE47	GND	GND	BK7
BE48	GND	GND	BL12
BE49	GND	GND	BL16
BE5	GND	GND	BL17
BE9	GND	GND	BL18
BF1	GND	GND	BL21
BF10	GND	GND	BL26
BF16	GND	GND	BL31
BF19	GND	GND	BL34
BF2	GND	GND	BL35
BF20	GND	GND	BL36
BF21	GND	GND	BL4
BF31	GND	GND	BL40
BF32	GND	GND	BL44
BF33	GND	GND	BL45
BF36	GND	GND	BL48
BF42	GND	GND	BL7
BF45	GND	GND	BL8
BF46	GND	GND	C12
BF47	GND	GND	C16
BF5	GND	GND	C17
BF50	GND	GND	C18
BF51	GND	GND	C2
BF6	GND	GND	C21
BF7	GND	GND	C3

GND GND

U78-4
FPGA_VU13P_A2577

C31	GND	GND	H35
C34	GND	GND	H36
C35	GND	GND	H37
C36	GND	GND	H38
C4	GND	GND	H41
C40	GND	GND	H46
C44	GND	GND	H47
C45	GND	GND	H5
C48	GND	GND	H50
C49	GND	GND	H51
C50	GND	GND	H6
C7	GND	GND	J12
C8	GND	GND	J14
D1	GND	GND	J22
D11	GND	GND	J3
D15	GND	GND	J38
D16	GND	GND	J4
D19	GND	GND	J40
D2	GND	GND	J43
D20	GND	GND	J47
D21	GND	GND	J48
D27	GND	GND	J49
D31	GND	GND	J5
D32	GND	GND	J9
D33	GND	GND	K1
D36	GND	GND	K10
D37	GND	GND	K14
D41	GND	GND	K19
D45	GND	GND	K2
D46	GND	GND	K29
D47	GND	GND	K38
D5	GND	GND	K42
D50	GND	GND	K45
D51	GND	GND	K47
D6	GND	GND	K5
D7	GND	GND	K50
E12	GND	GND	K51
E16	GND	GND	K7
E17	GND	GND	L12
E18	GND	GND	L14
E21	GND	GND	L16
E24	GND	GND	L26
E3	GND	GND	L3
E31	GND	GND	L36
E34	GND	GND	L38
E35	GND	GND	L4
E36	GND	GND	L40
E39	GND	GND	L44
E4	GND	GND	L47
E43	GND	GND	L48
E45	GND	GND	L49
E48	GND	GND	L5
E49	GND	GND	L8
E7	GND	GND	M1
E9	GND	GND	M11
F1	GND	GND	M2
F10	GND	GND	M23
F14	GND	GND	M33
F16	GND	GND	M38
F19	GND	GND	M41
F2	GND	GND	M46
F20	GND	GND	M47
F21	GND	GND	M5
F31	GND	GND	M50
F32	GND	GND	M51
F33	GND	GND	M6
F36	GND	GND	N13
F38	GND	GND	N14
F42	GND	GND	N20
F45	GND	GND	N3
F46	GND	GND	N30
F47	GND	GND	N38
F5	GND	GND	N39
F50	GND	GND	N4
F51	GND	GND	N43
F6	GND	GND	N47
F7	GND	GND	N48
G12	GND	GND	N49
G16	GND	GND	N5
G18	GND	GND	N9
G21	GND	GND	P1
G28	GND	GND	P10
G3	GND	GND	P17
G31	GND	GND	P2
G34	GND	GND	P27
G36	GND	GND	P37
G4	GND	GND	P38
G40	GND	GND	P42
G44	GND	GND	P45
G47	GND	GND	P47
G48	GND	GND	P5
G49	GND	GND	P50
G5	GND	GND	P51
G8	GND	GND	P7
H1	GND	GND	R12
H11	GND	GND	R14
H14	GND	GND	R24
H15	GND	GND	R3
H16	GND	GND	R34
H17	GND	GND	R38
H18	GND	GND	R4
H19	GND	GND	R40
H2	GND	GND	R44
H20	GND	GND	R47
H21	GND	GND	R48
H25	GND	GND	R49
H31	GND	GND	R5
H32	GND	GND	R8
H33	GND	GND	T1
H34	GND	GND	T11

GND GND

U78-5
FPGA_VU13P_A2577

T2	GND
T21	GND
T38	GND
T41	GND
T46	GND
T47	GND
T5	GND
T50	GND
T51	GND
T6	GND
U13	GND
U14	GND
U18	GND
U28	GND
U3	GND
U30	GND
U38	GND
U39	GND
U4	GND
U43	GND
U47	GND
U48	GND
U49	GND
U5	GND
U9	GND
V1	GND
V10	GND
V2	GND
V23	GND
V25	GND
V27	GND
V29	GND
V31	GND
V38	GND
V42	GND
V45	GND
V47	GND
V5	GND
V50	GND
V51	GND
V7	GND
W12	GND
W14	GND
W18	GND
W20	GND
W22	GND
W24	GND
W26	GND
W28	GND
W3	GND
W30	GND
W34	GND
W36	GND
W38	GND
W4	GND
W40	GND
W44	GND
W47	GND
W48	GND
W49	GND
W5	GND
W8	GND
Y1	GND
Y11	GND
Y15	GND
Y17	GND
Y19	GND
Y2	GND
Y21	GND
Y23	GND
Y25	GND
Y27	GND
Y29	GND
Y31	GND
Y33	GND
Y35	GND
Y37	GND
Y38	GND
Y41	GND
Y46	GND
Y47	GND
Y5	GND
Y50	GND
Y51	GND

GND

R442 10K 0603

V_M3V3

GND Y6

/F2_INSTALLED
[23]

IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F2_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM v3

Title
6.01: FPGA#2 GND

Size	Document Number	Rev
	6089-127	A

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6.02: FPGA#2 POWER INTERNAL

VCCINT MUST BE 0.85V.

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V_F2_INT

AA17	VCCINT	VCCINT	AK26
AA19	VCCINT	VCCINT	AK28
AA21	VCCINT	VCCINT	AK30
AA23	VCCINT	VCCINT	AL17
AA25	VCCINT	VCCINT	AL19
AA27	VCCINT	VCCINT	AL21
AA29	VCCINT	VCCINT	AL23
AA31	VCCINT	VCCINT	AL25
AB16	VCCINT	VCCINT	AL27
AB18	VCCINT	VCCINT	AL29
AB20	VCCINT	VCCINT	AL31
AB22	VCCINT	VCCINT	AM18
AB24	VCCINT	VCCINT	AM20
AB26	VCCINT	VCCINT	AM22
AB28	VCCINT	VCCINT	AM24
AB30	VCCINT	VCCINT	AM26
AC17	VCCINT	VCCINT	AM28
AC19	VCCINT	VCCINT	AM30
AC21	VCCINT	VCCINT	AN17
AC23	VCCINT	VCCINT	AN19
AC25	VCCINT	VCCINT	AN21
AC27	VCCINT	VCCINT	AN23
AC29	VCCINT	VCCINT	AN25
AC31	VCCINT	VCCINT	AN27
AD16	VCCINT	VCCINT	AN29
AD18	VCCINT	VCCINT	AN31
AD20	VCCINT	VCCINT	AP18
AD22	VCCINT	VCCINT	AP20
AD24	VCCINT	VCCINT	AP22
AD26	VCCINT	VCCINT	AP24
AD28	VCCINT	VCCINT	AP26
AD30	VCCINT	VCCINT	AP28
AE17	VCCINT	VCCINT	AP30
AE19	VCCINT	VCCINT	AR21
AE21	VCCINT	VCCINT	AR23
AE23	VCCINT	VCCINT	AR25
AE25	VCCINT	VCCINT	AR27
AE27	VCCINT	VCCINT	AR29
AE29	VCCINT	VCCINT	AR31
AE31	VCCINT	VCCINT	AT22
AF16	VCCINT	VCCINT	AT24
AF18	VCCINT	VCCINT	AT26
AF20	VCCINT	VCCINT	AT28
AF22	VCCINT	VCCINT	AT30
AF24	VCCINT	VCCINT	AU23
AF26	VCCINT	VCCINT	AU25
AF28	VCCINT	VCCINT	AU27
AF30	VCCINT	VCCINT	AU29
AG17	VCCINT	VCCINT	U27
AG21	VCCINT	VCCINT	U29
AG23	VCCINT	VCCINT	U31
AG25	VCCINT	VCCINT	V22
AG27	VCCINT	VCCINT	V24
AG29	VCCINT	VCCINT	V26
AG31	VCCINT	VCCINT	V28
AH16	VCCINT	VCCINT	V30
AH20	VCCINT	VCCINT	W17
AH22	VCCINT	VCCINT	W19
AH24	VCCINT	VCCINT	W21
AH26	VCCINT	VCCINT	W23
AH28	VCCINT	VCCINT	W25
AH30	VCCINT	VCCINT	W27
AJ17	VCCINT	VCCINT	W29
AJ21	VCCINT	VCCINT	W31
AJ23	VCCINT	VCCINT	Y18
AJ25	VCCINT	VCCINT	Y20
AJ27	VCCINT	VCCINT	Y22
AJ29	VCCINT	VCCINT	Y24
AJ31	VCCINT	VCCINT	Y26
AK16	VCCINT	VCCINT	Y28
AK20	VCCINT	VCCINT	Y30
AK22	VCCINT		
AK24	VCCINT		
	VCCINT		

VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).

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V_F2_INT

AA33	VCCINT_IO	VCCAUX	AA37
AB32	VCCINT_IO	VCCAUX	AC37
AC33	VCCINT_IO	VCCAUX	AD36
AD32	VCCINT_IO	VCCAUX	AD38
AE33	VCCINT_IO	VCCAUX	AE37
AF32	VCCINT_IO	VCCAUX	AE39
AG33	VCCINT_IO	VCCAUX	AF36
AH32	VCCINT_IO	VCCAUX	AF38
AJ33	VCCINT_IO	VCCAUX	AG37
AK32	VCCINT_IO	VCCAUX	AG39
AL33	VCCINT_IO	VCCAUX	AH38
AM32	VCCINT_IO	VCCAUX	AJ37
AN33	VCCINT_IO	VCCAUX	AL37
AP32	VCCINT_IO	VCCAUX	AN37
W33	VCCINT_IO	VCCAUX	W37
Y32	VCCINT_IO		
	VCCINT_IO		

VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

V_F2_INT

AA15	VCCBRAM	VCCAUX_IO	AA35
AC15	VCCBRAM	VCCAUX_IO	AB34
AD14	VCCBRAM	VCCAUX_IO	AB36
AE15	VCCBRAM	VCCAUX_IO	AC35
AF14	VCCBRAM	VCCAUX_IO	AD34
AG15	VCCBRAM	VCCAUX_IO	AE35
AH14	VCCBRAM	VCCAUX_IO	AF34
AJ15	VCCBRAM	VCCAUX_IO	AG35
AL15	VCCBRAM	VCCAUX_IO	AH34
AM16	VCCBRAM	VCCAUX_IO	AH36
AN15	VCCBRAM	VCCAUX_IO	AJ35
AP16	VCCBRAM	VCCAUX_IO	AK34
W15	VCCBRAM	VCCAUX_IO	AK36
Y16	VCCBRAM	VCCAUX_IO	AL35
	VCCBRAM	VCCAUX_IO	AM34
		VCCAUX_IO	AM36
		VCCAUX_IO	AN35
		VCCAUX_IO	AP34
		VCCAUX_IO	AP36
		VCCAUX_IO	W35
		VCCAUX_IO	Y34
		VCCAUX_IO	Y36

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).

V_1V8

C1076 47 UF 0805 6.3V
C1082 47 UF 0805 6.3V
C754 47 UF 0805 6.3V
C756 47 UF 0805 6.3V
C907 47 UF 0805 6.3V

GND

V_1V8

C1048 10 UF 0402 4V
C1023 10 UF 0402 4V
C804 10 UF 0402 4V
C799 10 UF 0402 4V
C908 10 UF 0402 4V

GND

VCCAUX / VCCAUXIO / VCCO
ALL I/O BANKS ARE POWERED AT 1.8 VOLTS.

V_F2_INT

C27 330 UF 2.5V 1210
C481 330 UF 2.5V 1210
C26 330 UF 2.5V 1210
C25 330 UF 2.5V 1210
C228 330 UF 2.5V 1210

GND

V_F2_INT

C958 100 UF 0805 6.3V
C948 100 UF 0805 6.3V
C931 100 UF 0805 6.3V
C916 100 UF 0805 6.3V
C1081 100 UF 0805 6.3V
C1080 100 UF 0805 6.3V
C1079 100 UF 0805 6.3V
C1078 100 UF 0805 6.3V
C755 100 UF 0805 6.3V
C1077 100 UF 0805 6.3V
C757 100 UF 0805 6.3V

GND

V_F2_INT

C957 47 UF 0805 6.3V
C944 47 UF 0805 6.3V
C921 47 UF 0805 6.3V
C911 47 UF 0805 6.3V
C753 47 UF 0805 6.3V
C752 47 UF 0805 6.3V
C751 47 UF 0805 6.3V

GND

V_F2_INT

C961 10 UF 0402 4V
C950 10 UF 0402 4V
C933 10 UF 0402 4V
C919 10 UF 0402 4V
C953 10 UF 0402 4V
C936 10 UF 0402 4V
C928 10 UF 0402 4V
C918 10 UF 0402 4V
C1053 10 UF 0402 4V
C1052 10 UF 0402 4V

GND

V_F2_INT

C1051 10 UF 0402 4V
C1022 10 UF 0402 4V
C803 10 UF 0402 4V
C771 10 UF 0402 4V
C768 10 UF 0402 4V
C800 10 UF 0402 4V
C1057 10 UF 0402 4V
C805 10 UF 0402 4V

GND

VCCINT / VCCINT_IO / VCCBRAM

BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"UG583 UltraScale Architecture PCB Design"

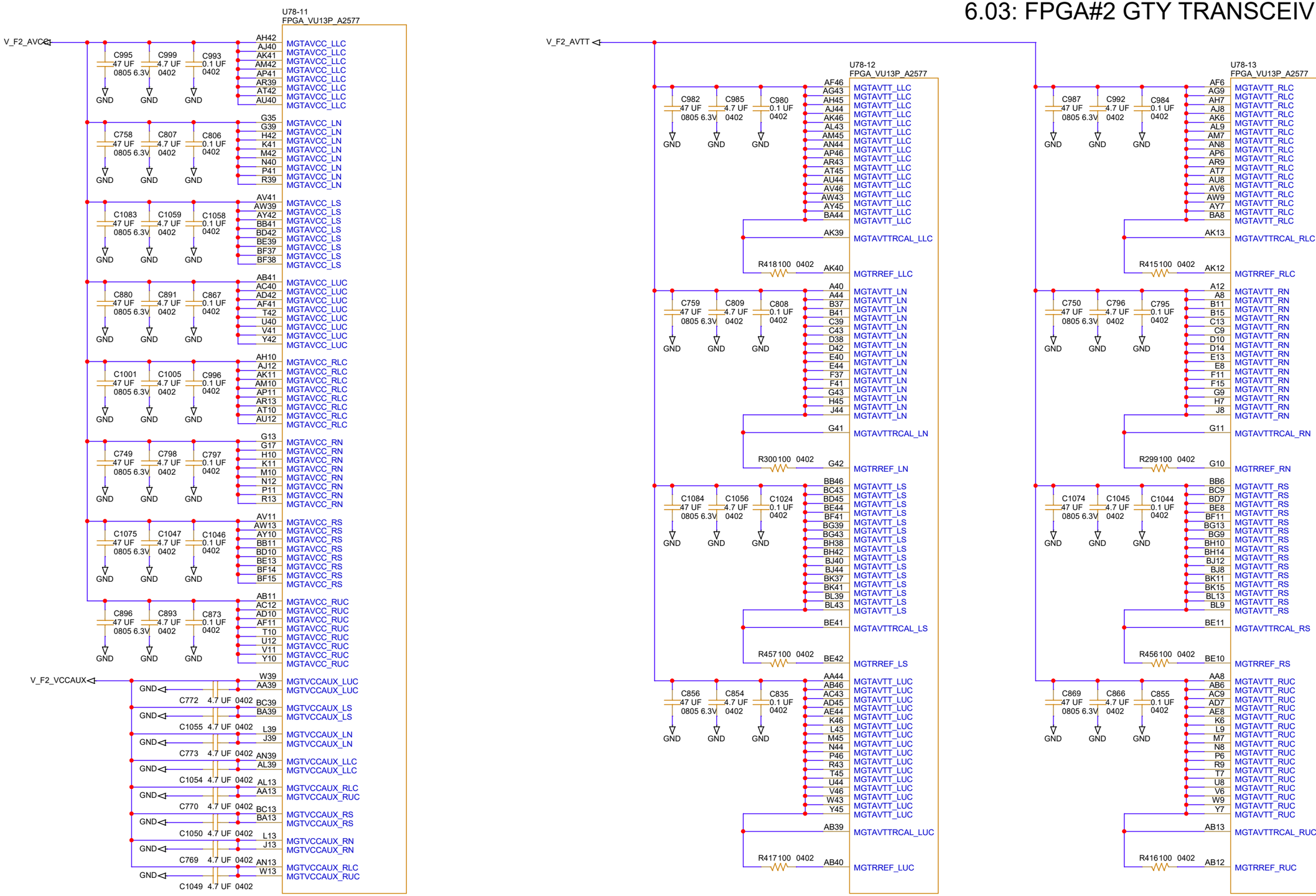
APOLLO CM v3

Title: 6.02: FPGA#2 POWER INTERNAL

Size	Document Number	Rev
	6089-127	A

Date: Wednesday, October 16, 2024 Sheet 51 of 81

6.03: FPGA#2 GTY TRANSCEIVER POWER



REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM v3			
Title: 6.03: FPGA#2 GTY TRANSCEIVER POWER			
Size	Document Number: 6089-127		Rev: A
Date: Wednesday, October 16, 2024	Sheet 52 of 81		

6.04: FPGA#2 CONFIGURATION

MUST BE TIED TO "VCCINT" OR "GND". DO NOT CONNECT TO "VCCO_0". CONNECT TO "GND" FOR STANDARD POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

WHEN "FPGA_CFG_FROM_FLASH" IS ASSERTED (HIGH), THE FPGA WILL BE ABLE TO BOOT FROM THE FLASH MEMORY. WHEN IT IS NEGATED (LOW), THE FPGA WILL ONLY BE ABLE TO BOOT FROM JTAG.

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

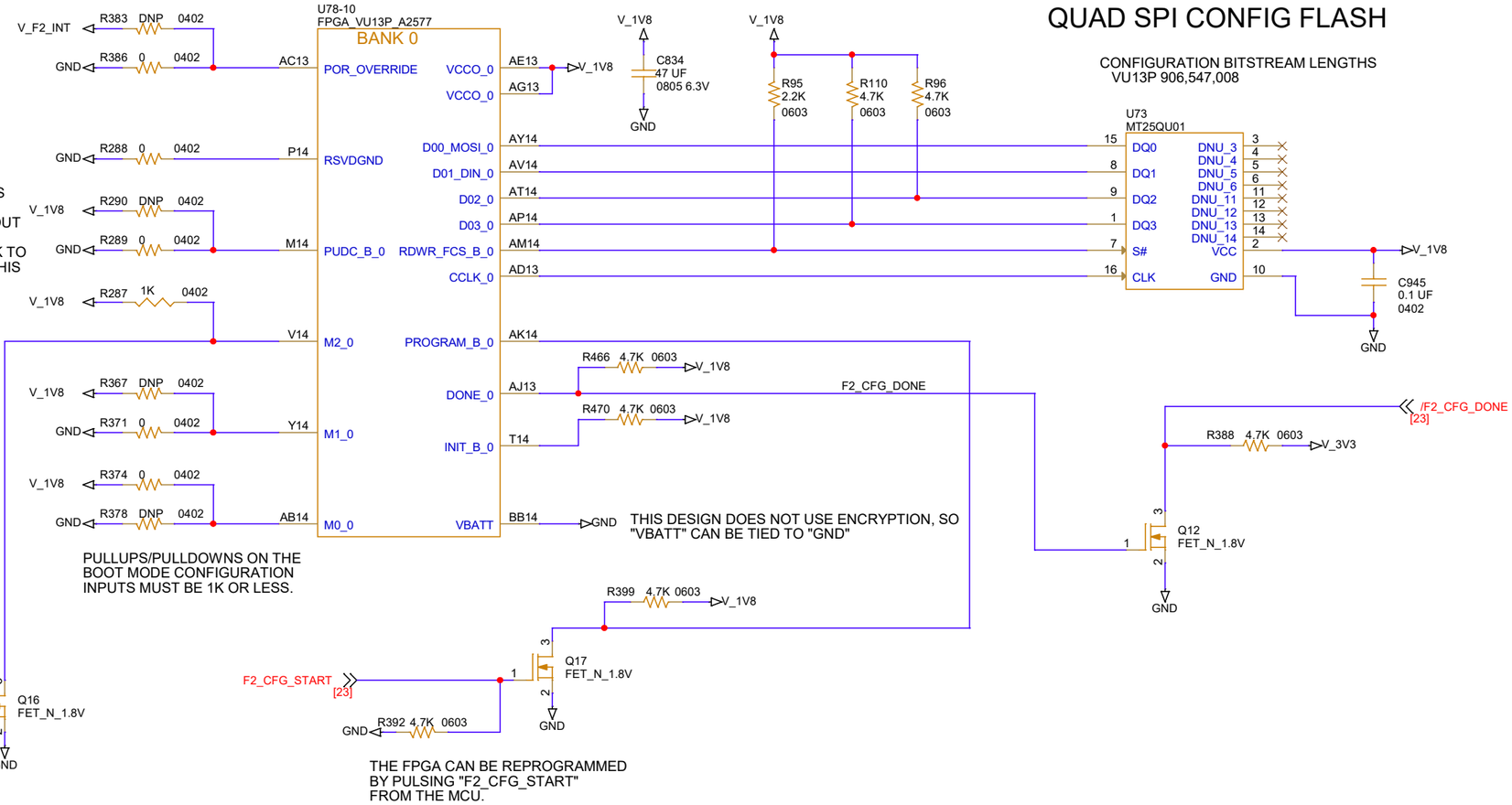
THE FPGA CAN BE REPROGRAMMED BY PULSING "F2_CFG_START" FROM THE MCU.

U78-10
FPGA_VU13P_A2577
BANK 0

QUAD SPI CONFIG FLASH

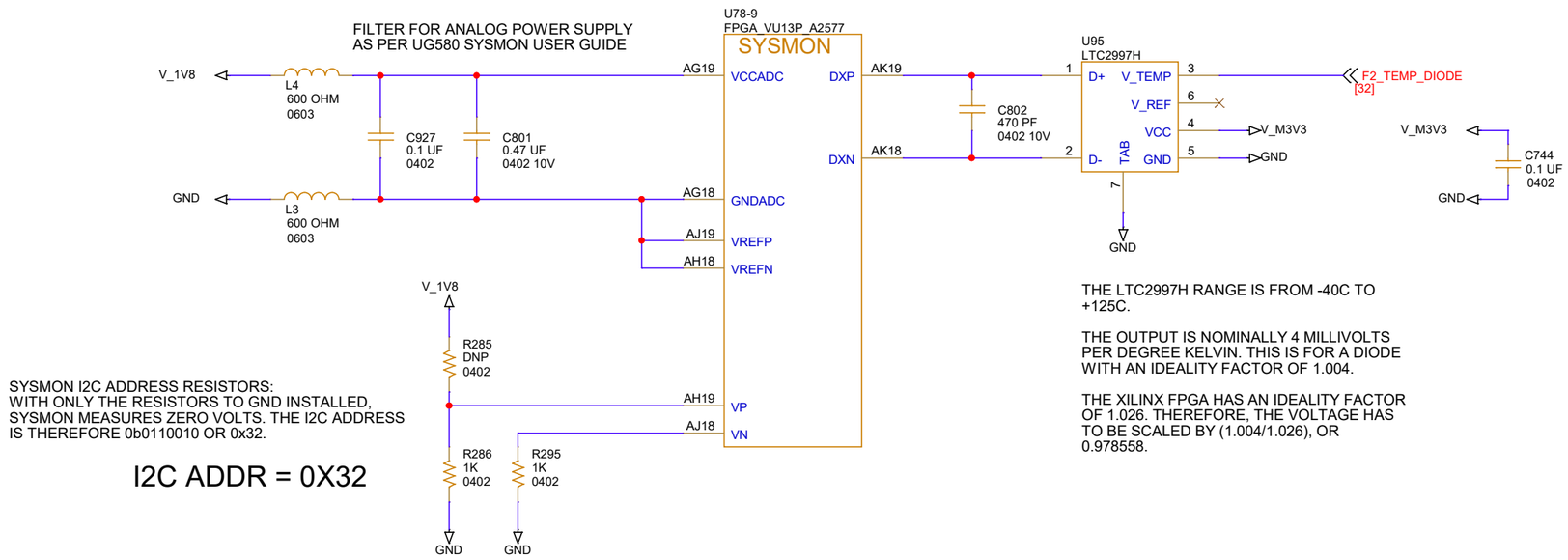
CONFIGURATION BITSTREAM LENGTHS
VU13P 906,547,008

U73
MT25QU01



APOLLO CM v3		
Title: 6.04: FPGA#2 CONFIGURATION		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 53 of 81	

6.05: FPGA#2 SYSTEM MONITOR



APOLLO CM v3		
Title: 6.05: FPGA#2 SYSTEM MONITOR		
Size	Document Number: 6089-127	Rev: A
Date: Wednesday, October 16, 2024	Sheet 54 of 81	

6.06 FPGA#2 I/O SLR0

U78-14
FPGA_VU13P_A2577

BE20	IO_L10N_T1U_N7_QBC_AD4N_61	VCCO_61	AW27
BE21	IO_L10P_T1U_N6_QBC_AD4P_61	VCCO_61	AY24
BF22	IO_L11N_T1U_N9_GC_61	VCCO_61	BC25
BE22	IO_L11P_T1U_N8_GC_61	VCCO_61	BD22
BE23	IO_L12N_T1U_N11_GC_61	VREF_61	BG23
BD23	IO_L12P_T1U_N10_GC_61		BK24
BD24	IO_L13N_T2L_N1_GC_QBC_61		AV23
BD25	IO_L13P_T2L_N0_GC_QBC_61		
BC23	IO_L14N_T2L_N3_GC_61		
BC24	IO_L14P_T2L_N2_GC_61		
BB25	IO_L15N_T2L_N5_AD11N_61		
BB26	IO_L15P_T2L_N4_AD11P_61		
BD26	IO_L16N_T2U_N7_QBC_AD3N_61		
BC26	IO_L16P_T2U_N6_QBC_AD3P_61		
BA24	IO_L17N_T2U_N9_AD10N_61		
BA25	IO_L17P_T2U_N8_AD10P_61		
BC22	IO_L18N_T2U_N11_AD2N_61		
BB22	IO_L18P_T2U_N10_AD2P_61		
AW24	IO_L19N_T3L_N1_DBC_AD9N_61		
AW25	IO_L19P_T3L_N0_DBC_AD9P_61		
BL23	IO_L1N_T0L_N1_DBC_61		
BL24	IO_L1P_T0L_N0_DBC_61		
AW23	IO_L20N_T3L_N3_AD1N_61		
AV24	IO_L20P_T3L_N2_AD1P_61		
BA23	IO_L21N_T3L_N5_AD8N_61		
AY23	IO_L21P_T3L_N4_AD8P_61		
BA27	IO_L22N_T3U_N7_DBC_AD0N_61		
AY27	IO_L22P_T3U_N6_DBC_AD0P_61		
AY26	IO_L23N_T3U_N9_61		
AW26	IO_L23P_T3U_N8_61		
AV26	IO_L24N_T3U_N11_61		
AV27	IO_L24P_T3U_N10_61		
BL22	IO_L2N_T0L_N3_61		
BK22	IO_L2P_T0L_N2_61		
BJ24	IO_L3N_T0L_N5_AD15N_61		
BJ25	IO_L3P_T0L_N4_AD15P_61		
BK23	IO_L4N_T0U_N7_DBC_AD7N_61		
BJ23	IO_L4P_T0U_N6_DBC_AD7P_61		
BL25	IO_L5N_T0U_N9_AD14N_61		
BK25	IO_L5P_T0U_N8_AD14P_61		
BH23	IO_L6N_T0U_N11_AD6N_61		
BH24	IO_L6P_T0U_N10_AD6P_61		
BG24	IO_L7N_T1L_N1_QBC_AD13N_61		
BG25	IO_L7P_T1L_N0_QBC_AD13P_61		
BG22	IO_L8N_T1L_N3_AD5N_61		
BF23	IO_L8P_T1L_N2_AD5P_61		
BF24	IO_L9N_T1L_N5_AD12N_61		
BF25	IO_L9P_T1L_N4_AD12P_61		
BH22	IO_T0U_N12_VRP_61		
BE25	IO_T1U_N12_61		
BB24	IO_T2U_N12_61		
AY25	IO_T3U_N12_61		

V_1V8

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

F2 LOGIC
TCDS 40MHZ INPUT

LHC_CLK
ALWAYS 40 MHZ

ac_nF2_TCDS40_CLK [21]
ac_pF2_TCDS40_CLK [21]
ac_nLHC_CLK_4 [13]
ac_pLHC_CLK_4 [13]

nF2_TEST_CONN_0 [59]
pF2_TEST_CONN_0 [59]

F2_TEST_CONN_5 [59]
F2_TEST_CONN_6 [59]

nF2_TEST_CONN_4 [59]
pF2_TEST_CONN_4 [59]
nF2_TEST_CONN_3 [59]
pF2_TEST_CONN_3 [59]
nF2_TEST_CONN_2 [59]
pF2_TEST_CONN_2 [59]
nF2_TEST_CONN_1 [59]
pF2_TEST_CONN_1 [59]

F2_LED_GREEN [23]
F2_LED_BLUE [23]

F2_LED_RED [23]

THE TRI-COLOR LED IS CONNECTED TO DIFFERENT PINS ON EACH FPGA, IN ORDER TO SIMPLIFY LAYOUT.

THe 40 MHZ RECOVERED TCDS CLOCK USES PINS BK26 AND BJ26 ON FPGA#1. THE CLOCK FROM FPGA#2 IS NOT USED ANYWHERE, BUT THE PINS ARE RESERVED.

nF1F2_SPARE2 [47]
pF1F2_SPARE2 [47]
nF1F2_SPARE1 [47]
pF1F2_SPARE1 [47]
nF1F2_SPARE0 [47]
pF1F2_SPARE0 [47]

GND — R455 240 0402

U78-15
FPGA_VU13P_A2577

BH27	IO_L10N_T1U_N7_QBC_AD4N_62	VCCO_62	AV30
BH26	IO_L10P_T1U_N6_QBC_AD4P_62	VCCO_62	BA31
BF28	IO_L11N_T1U_N9_GC_62	VCCO_62	BB28
BF27	IO_L11P_T1U_N8_GC_62	VCCO_62	BE29
BE27	IO_L12N_T1U_N11_GC_62	VCCO_62	BF26
BE26	IO_L12P_T1U_N10_GC_62	VCCO_62	BH30
BD29	IO_L13N_T2L_N1_GC_QBC_62	VCCO_62	BJ27
BC28	IO_L13P_T2L_N0_GC_QBC_62	VREF_62	AV28
BE28	IO_L14N_T2L_N3_GC_62		
BD28	IO_L14P_T2L_N2_GC_62		
BE30	IO_L15N_T2L_N5_AD11N_62		
BD30	IO_L15P_T2L_N4_AD11P_62		
BC27	IO_L16N_T2U_N7_QBC_AD3N_62		
BB27	IO_L16P_T2U_N6_QBC_AD3P_62		
BC31	IO_L17N_T2U_N9_AD10N_62		
BB31	IO_L17P_T2U_N8_AD10P_62		
BC29	IO_L18N_T2U_N11_AD2N_62		
BB29	IO_L18P_T2U_N10_AD2P_62		
BA29	IO_L19N_T3L_N1_DBC_AD9N_62		
BA28	IO_L19P_T3L_N0_DBC_AD9P_62		
BJ28	IO_L1N_T0L_N1_DBC_62		
BH28	IO_L1P_T0L_N0_DBC_62		
AY28	IO_L20N_T3L_N3_AD1N_62		
AW28	IO_L20P_T3L_N2_AD1P_62		
BA30	IO_L21N_T3L_N5_AD8N_62		
AY30	IO_L21P_T3L_N4_AD8P_62		
AV31	IO_L22N_T3U_N7_DBC_AD0N_62		
AU31	IO_L22P_T3U_N6_DBC_AD0P_62		
AW29	IO_L23N_T3U_N9_62		
AV29	IO_L23P_T3U_N8_62		
AY31	IO_L24N_T3U_N11_62		
AW31	IO_L24P_T3U_N10_62		
BL28	IO_L2N_T0L_N3_62		
BL27	IO_L2P_T0L_N2_62		
BJ30	IO_L3N_T0L_N5_AD15N_62		
BJ29	IO_L3P_T0L_N4_AD15P_62		
BK28	IO_L4N_T0U_N7_DBC_AD7N_62		
BK27	IO_L4P_T0U_N6_DBC_AD7P_62		
BL30	IO_L5N_T0U_N9_AD14N_62		
BK30	IO_L5P_T0U_N8_AD14P_62		
BK26	IO_L6N_T0U_N11_AD6N_62		
BJ26	IO_L6P_T0U_N10_AD6P_62		
BG27	IO_L7N_T1L_N1_QBC_AD13N_62		
BG26	IO_L7P_T1L_N0_QBC_AD13P_62		
BG30	IO_L8N_T1L_N3_AD5N_62		
BF29	IO_L8P_T1L_N2_AD5P_62		
BH29	IO_L9N_T1L_N5_AD12N_62		
BG29	IO_L9P_T1L_N4_AD12P_62		
BL29	IO_T0U_N12_VRP_62		
BF30	IO_T1U_N12_62		
BB30	IO_T2U_N12_62		
AW30	IO_T3U_N12_62		

V_1V8

R443 1K 0402 — GND

U78-16
FPGA_VU13P_A2577

BC36	IO_L10N_T1U_N7_QBC_AD4N_63	VCCO_63	AT36
BB36	IO_L10P_T1U_N6_QBC_AD4P_63	VCCO_63	AU33
BB35	IO_L11N_T1U_N9_GC_63	VCCO_63	AW37
BA35	IO_L11P_T1U_N8_GC_63	VCCO_63	AY34
BB34	IO_L12N_T1U_N11_GC_63	VCCO_63	BC35
BA34	IO_L12P_T1U_N10_GC_63	VCCO_63	BD32
AW36	IO_L13N_T2L_N1_GC_QBC_63	VREF_63	AR32
AW35	IO_L13P_T2L_N0_GC_QBC_63		
AY36	IO_L14N_T2L_N3_GC_63		
AY35	IO_L14P_T2L_N2_GC_63		
AV37	IO_L15N_T2L_N5_AD11N_63		
AV36	IO_L15P_T2L_N4_AD11P_63		
AV33	IO_L16N_T2U_N7_QBC_AD3N_63		
AV32	IO_L16P_T2U_N6_QBC_AD3P_63		
AW34	IO_L17N_T2U_N9_AD10N_63		
AW33	IO_L17P_T2U_N8_AD10P_63		
AV34	IO_L18N_T2U_N11_AD2N_63		
AU34	IO_L18P_T2U_N10_AD2P_63		
AU37	IO_L19N_T3L_N1_DBC_AD9N_63		
AU36	IO_L19P_T3L_N0_DBC_AD9P_63		
BE32	IO_L1N_T0L_N1_DBC_63		
BE31	IO_L1P_T0L_N0_DBC_63		
AU32	IO_L20N_T3L_N3_AD1N_63		
AT32	IO_L20P_T3L_N2_AD1P_63		
AR37	IO_L21N_T3L_N5_AD8N_63		
AR36	IO_L21P_T3L_N4_AD8P_63		
AT34	IO_L22N_T3U_N7_DBC_AD0N_63		
AT33	IO_L22P_T3U_N6_DBC_AD0P_63		
AT35	IO_L23N_T3U_N9_63		
AR35	IO_L23P_T3U_N8_63		
AR34	IO_L24N_T3U_N11_63		
AR33	IO_L24P_T3U_N10_63		
BC32	IO_L2N_T0L_N3_63		
BB32	IO_L2P_T0L_N2_63		
BA32	IO_L3N_T0L_N5_AD15N_63		
AY32	IO_L3P_T0L_N4_AD15P_63		
BA33	IO_L4N_T0U_N7_DBC_AD7N_63		
AY33	IO_L4P_T0U_N6_DBC_AD7P_63		
BD33	IO_L5N_T0U_N9_AD14N_63		
BC33	IO_L5P_T0U_N8_AD14P_63		
BD34	IO_L6N_T0U_N11_AD6N_63		
BC34	IO_L6P_T0U_N10_AD6P_63		
BD36	IO_L7N_T1L_N1_QBC_AD13N_63		
BD35	IO_L7P_T1L_N0_QBC_AD13P_63		
BD37	IO_L8N_T1L_N3_AD5N_63		
BC37	IO_L8P_T1L_N2_AD5P_63		
BB37	IO_L9N_T1L_N5_AD12N_63		
BA37	IO_L9P_T1L_N4_AD12P_63		
BD31	IO_T0U_N12_VRP_63		
AY37	IO_T1U_N12_63		
AU35	IO_T2U_N12_63		
AT37	IO_T3U_N12_63		

OMIT "VREF" AND "VRP" RESISTORS ON UNUSED I/O BANKS.

APOLLO CM v3			
Title: 6.06 FPGA#2 I/O SLR0			
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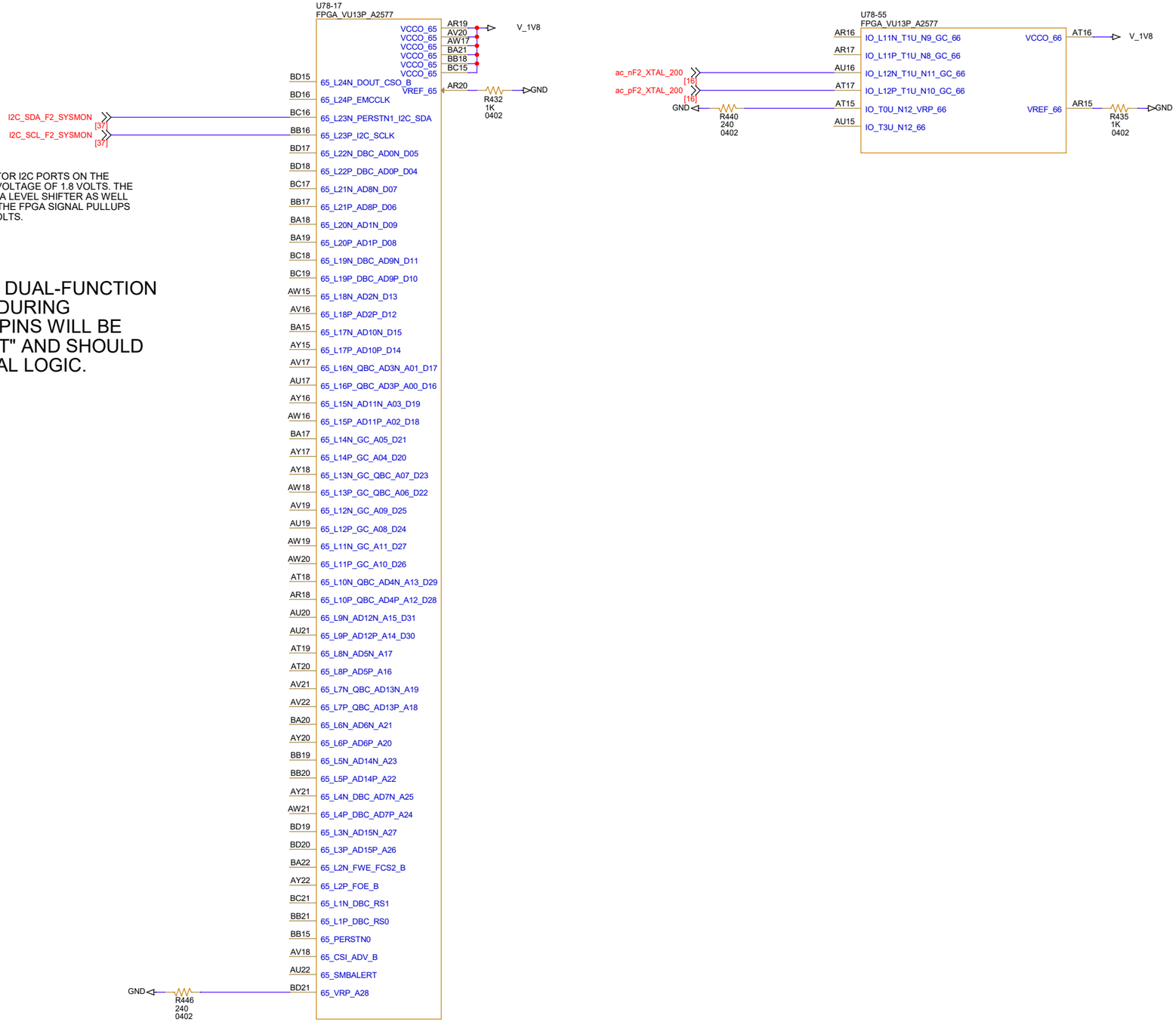
6.07 FPGA#2 I/O SLR1



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

APOLLO CM v3		
Title: 6.07 FPGA#2 I/O SLR1		
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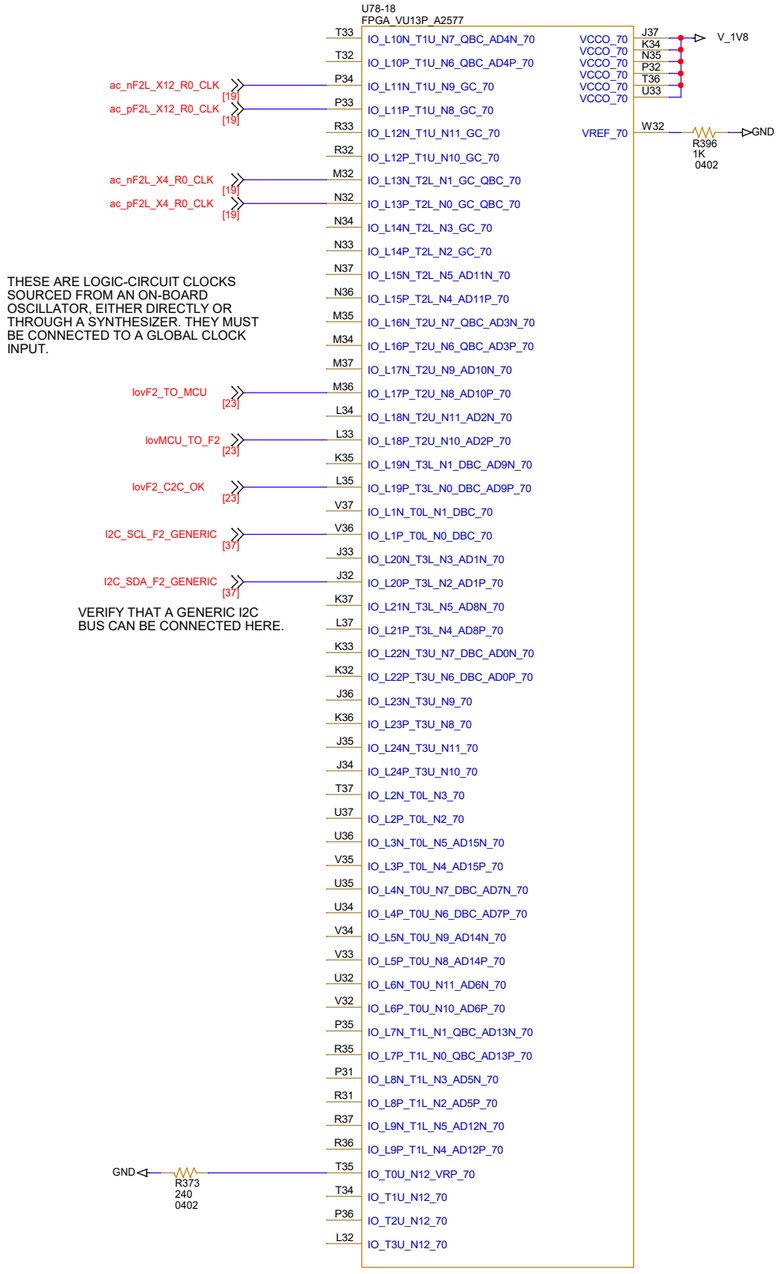
6.08: FPGA#2 I/O SLR2



THE "F2F1_SPARE" SIGNALS ARE OUTPUTS FROM F2 AND INPUTS TO F1.
THE "F1F2_SPARE" SIGNALS ARE OUTPUTS FROM F1 AND INPUTS TO F2.
THEY ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

APOLLO CM v3			
Title: 6.08: FPGA#2 I/O SLR2			
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6.09: FPGA#2 I/O SLR3

THE "F2_HDRnn" SIGNALS ARE CONNECTED FROM THE FPGA TO PADS ON THE BOTTOM SIDE OF THE BOARD. A 20-PIN HEADER CAN BE ATTACHED. THESE SIGNALS ARE FOR DEBUGGING, OR FUTURE USE. HDR01 AND HDR02 ARE CONNECTED TO CLOCK-CAPABLE INPUTS.

CON20A

J7

2	1	F2_HDR01	
4	3	F2_HDR02	
6	5	F2_HDR03	
8	7	F2_HDR04	
10	9	F2_HDR05	
12	11	F2_HDR06	
14	13	F2_HDR07	
16	15	F2_HDR08	
18	17	F2_HDR09	
20	19	F2_HDR10	

GND

U78-20
FPGA_VU13P_A2577

M31	IO_L10N_T1U_N7_QBC_AD4N_73		
N31	IO_L10P_T1U_N6_QBC_AD4P_73		
M27	IO_L11N_T1U_N9_GC_73		
N27	IO_L11P_T1U_N8_GC_73		
F2_HDR02 L29	IO_L12N_T1U_N11_GC_73		
F2_HDR01 L28	IO_L12P_T1U_N10_GC_73		
K28	IO_L13N_T2L_N1_GC_QBC_73		
K27	IO_L13P_T2L_N0_GC_QBC_73		
L27	IO_L14N_T2L_N3_GC_73		
M26	IO_L14P_T2L_N2_GC_73		
G26	IO_L15N_T2L_N5_AD11N_73		
G25	IO_L15P_T2L_N4_AD11P_73		
F27	IO_L16N_T2U_N7_QBC_AD3N_73		
G27	IO_L16P_T2U_N6_QBC_AD3P_73		
J26	IO_L17N_T2U_N9_AD10N_73		
K26	IO_L17P_T2U_N8_AD10P_73		
H26	IO_L18N_T2U_N11_AD2N_73		
J25	IO_L18P_T2U_N10_AD2P_73		
E25	IO_L19N_T3L_N1_DBC_AD9N_73		
F25	IO_L19P_T3L_N0_DBC_AD9P_73		
R30	IO_L1N_T0L_N1_DBC_73		
T30	IO_L1P_T0L_N0_DBC_73		
E27	IO_L20N_T3L_N3_AD1N_73		
E26	IO_L20P_T3L_N2_AD1P_73		
F2_HDR04 B26	IO_L21N_T3L_N5_AD8N_73		
F2_HDR03 C26	IO_L21P_T3L_N4_AD8P_73		
A27	IO_L22N_T3U_N7_DBC_AD0N_73		
B27	IO_L22P_T3U_N6_DBC_AD0P_73		
F2_HDR05 A25	IO_L23N_T3U_N9_73		
F2_HDR06 B25	IO_L23P_T3U_N8_73		
C27	IO_L24N_T3U_N11_73		
D26	IO_L24P_T3U_N10_73		
T29	IO_L2N_T0L_N3_73		
T28	IO_L2P_T0L_N2_73		
T27	IO_L3N_T0L_N5_AD15N_73		
U26	IO_L3P_T0L_N4_AD15P_73		
P28	IO_L4N_T0U_N7_DBC_AD7N_73		
R28	IO_L4P_T0U_N6_DBC_AD7P_73		
R27	IO_L5N_T0U_N9_AD14N_73		
R26	IO_L5P_T0U_N8_AD14P_73		
P30	IO_L6N_T0U_N11_AD6N_73		
P29	IO_L6P_T0U_N10_AD6P_73		
N26	IO_L7N_T1L_N1_QBC_AD13N_73		
P26	IO_L7P_T1L_N0_QBC_AD13P_73		
M30	IO_L8N_T1L_N3_AD5N_73		
M29	IO_L8P_T1L_N2_AD5P_73		
N29	IO_L9N_T1L_N5_AD12N_73		
N28	IO_L9P_T1L_N4_AD12P_73		
GND R382 240 0402 T31	IO_T0U_N12_VRP_73		
J28	IO_T1U_N12_73		
H27	IO_T2U_N12_73		
D25	IO_T3U_N12_73		
		VCCO_73 C25 F26 J27 M28 R29 T26	V_1V8
		VREF_73 U25 R376 1K 0402	GND

U78-21
FPGA_VU13P_A2577

H23	IO_L10N_T1U_N7_QBC_AD4N_74		
J23	IO_L10P_T1U_N6_QBC_AD4P_74		
J21	IO_L11N_T1U_N9_GC_74		
K21	IO_L11P_T1U_N8_GC_74		
K22	IO_L12N_T1U_N11_GC_74		
K23	IO_L12P_T1U_N10_GC_74		
L22	IO_L13N_T2L_N1_GC_QBC_74		
L23	IO_L13P_T2L_N0_GC_QBC_74		
M21	IO_L14N_T2L_N3_GC_74		
M22	IO_L14P_T2L_N2_GC_74		
L24	IO_L15N_T2L_N5_AD11N_74		
M25	IO_L15P_T2L_N4_AD11P_74		
M24	IO_L16N_T2U_N7_QBC_AD3N_74		
N24	IO_L16P_T2U_N6_QBC_AD3P_74		
N21	IO_L17N_T2U_N9_AD10N_74		
N22	IO_L17P_T2U_N8_AD10P_74		
K25	IO_L18N_T2U_N11_AD2N_74		
L25	IO_L18P_T2U_N10_AD2P_74		
T23	IO_L19N_T3L_N1_DBC_AD9N_74		
T24	IO_L19P_T3L_N0_DBC_AD9P_74		
D23	IO_L1N_T0L_N1_DBC_74		
E23	IO_L1P_T0L_N0_DBC_74		
R25	IO_L20N_T3L_N3_AD1N_74		
T25	IO_L20P_T3L_N2_AD1P_74		
U22	IO_L21N_T3L_N5_AD8N_74		
U23	IO_L21P_T3L_N4_AD8P_74		
P24	IO_L22N_T3U_N7_DBC_AD0N_74		
P25	IO_L22P_T3U_N6_DBC_AD0P_74		
R22	IO_L23N_T3U_N9_74		
T22	IO_L23P_T3U_N8_74		
P23	IO_L24N_T3U_N11_74		
R23	IO_L24P_T3U_N10_74		
F2_HDR08 B24	IO_L2N_T0L_N3_74		
C24	IO_L2P_T0L_N2_74		
F2_HDR09 A23	IO_L3N_T0L_N5_AD15N_74		
F2_HDR07 A24	IO_L3P_T0L_N4_AD15P_74		
E22	IO_L4N_T0U_N7_DBC_AD7N_74		
F22	IO_L4P_T0U_N6_DBC_AD7P_74		
C22	IO_L5N_T0U_N9_AD14N_74		
C23	IO_L5P_T0U_N8_AD14P_74		
F2_HDR10 A22	IO_L6N_T0U_N11_AD6N_74		
B22	IO_L6P_T0U_N10_AD6P_74		
G24	IO_L7N_T1L_N1_QBC_AD13N_74		
H24	IO_L7P_T1L_N0_QBC_AD13P_74		
F23	IO_L8N_T1L_N3_AD5N_74		
F24	IO_L8P_T1L_N2_AD5P_74		
G22	IO_L9N_T1L_N5_AD12N_74		
H22	IO_L9P_T1L_N4_AD12P_74		
GND R324 240 0402 D24	IO_T0U_N12_VRP_74		
J24	IO_T1U_N12_74		
N23	IO_T2U_N12_74		
P21	IO_T3U_N12_74		
		VCCO_74 D22 G23 K24 L21 N25 P22	V_1V8
		VREF_74 U24 R375 1K 0402	GND

U78-22
FPGA_VU13P_A2577

T19	IO_L10N_T1U_N7_QBC_AD4N_75		
T20	IO_L10P_T1U_N6_QBC_AD4P_75		
P18	IO_L11N_T1U_N9_GC_75		
P19	IO_L11P_T1U_N8_GC_75		
ac_nF2R_X12_R0_CLK [19] R17	IO_L12N_T1U_N11_GC_75		
ac_pF2R_X12_R0_CLK [19] R18	IO_L12P_T1U_N10_GC_75		
M17	IO_L13N_T2L_N1_GC_QBC_75		
N17	IO_L13P_T2L_N0_GC_QBC_75		
ac_nF2R_X4_R0_CLK [19] N18	IO_L14N_T2L_N3_GC_75		
ac_pF2R_X4_R0_CLK [19] N19	IO_L14P_T2L_N2_GC_75		
P15	IO_L15N_T2L_N5_AD11N_75		
P16	IO_L15P_T2L_N4_AD11P_75		
L19	IO_L16N_T2U_N7_QBC_AD3N_75		
M19	IO_L16P_T2U_N6_QBC_AD3P_75		
M16	IO_L17N_T2U_N9_AD10N_75		
N16	IO_L17P_T2U_N8_AD10P_75		
L17	IO_L18N_T2U_N11_AD2N_75		
L18	IO_L18P_T2U_N10_AD2P_75		
K15	IO_L19N_T3L_N1_DBC_AD9N_75		
K16	IO_L19P_T3L_N0_DBC_AD9P_75		
T15	IO_L1N_T0L_N1_DBC_75		
U15	IO_L1P_T0L_N0_DBC_75		
L15	IO_L20N_T3L_N3_AD1N_75		
M15	IO_L20P_T3L_N2_AD1P_75		
J15	IO_L21N_T3L_N5_AD8N_75		
J16	IO_L21P_T3L_N4_AD8P_75		
K17	IO_L22N_T3U_N7_DBC_AD0N_75		
K18	IO_L22P_T3U_N6_DBC_AD0P_75		
J18	IO_L23N_T3U_N9_75		
J19	IO_L23P_T3U_N8_75		
K20	IO_L24N_T3U_N11_75		
L20	IO_L24P_T3U_N10_75		
V18	IO_L2N_T0L_N3_75		
V19	IO_L2P_T0L_N2_75		
U16	IO_L3N_T0L_N5_AD15N_75		
U17	IO_L3P_T0L_N4_AD15P_75		
V16	IO_L4N_T0U_N7_DBC_AD7N_75		
V17	IO_L4P_T0U_N6_DBC_AD7P_75		
U19	IO_L5N_T0U_N9_AD14N_75		
U20	IO_L5P_T0U_N8_AD14P_75		
V15	IO_L6N_T0U_N11_AD6N_75		
W16	IO_L6P_T0U_N10_AD6P_75		
R15	IO_L7N_T1L_N1_QBC_AD13N_75		
R16	IO_L7P_T1L_N0_QBC_AD13P_75		
T17	IO_L8N_T1L_N3_AD5N_75		
T18	IO_L8P_T1L_N2_AD5P_75		
P20	IO_L9N_T1L_N5_AD12N_75		
R20	IO_L9P_T1L_N4_AD12P_75		
GND R387 240 0402 V21	IO_T0U_N12_VRP_75		
R21	IO_T1U_N12_75		
M20	IO_T2U_N12_75		
J20	IO_T3U_N12_75		
		VCCO_75 J17 M18 N15 R19 T16 V20	V_1V8
		VREF_75 U21 R381 1K 0402	GND

APOLLO CM v3	
Title	6.09: FPGA#2 I/O SLR3
Size	Document Number 6089-127 Rev A
Date: Wednesday, October 16, 2024	Sheet 58 of 81

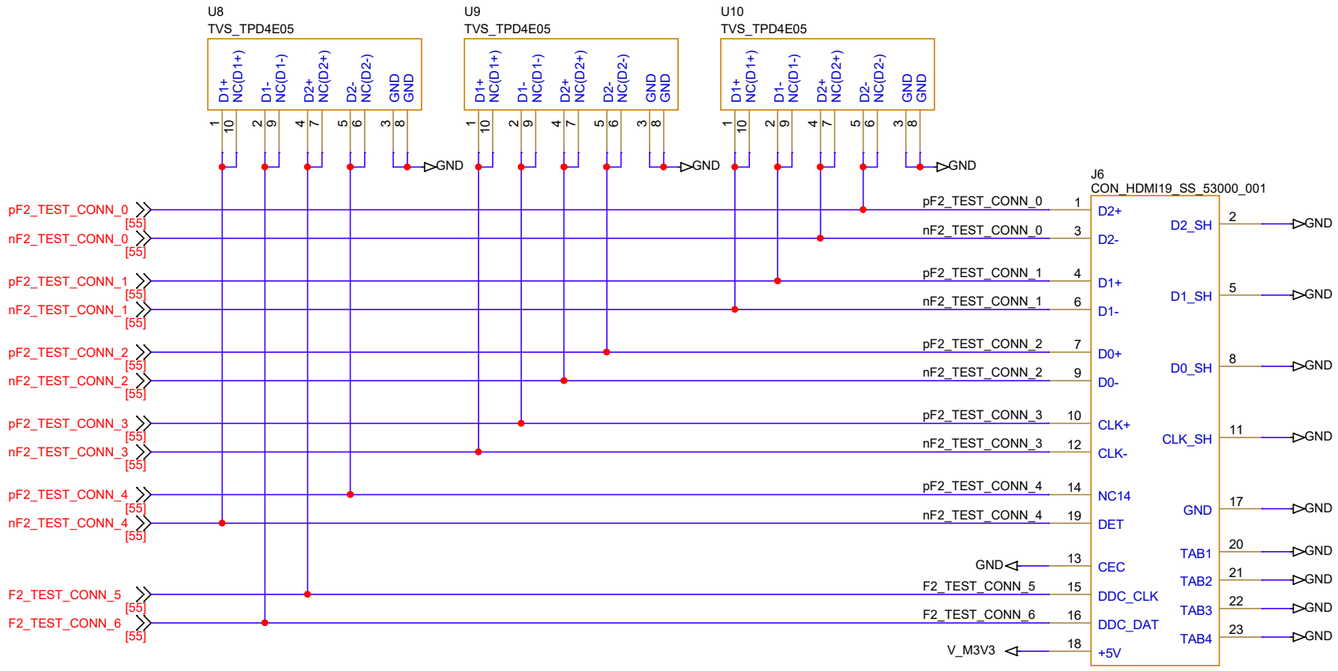
6.10 FPGA#2 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

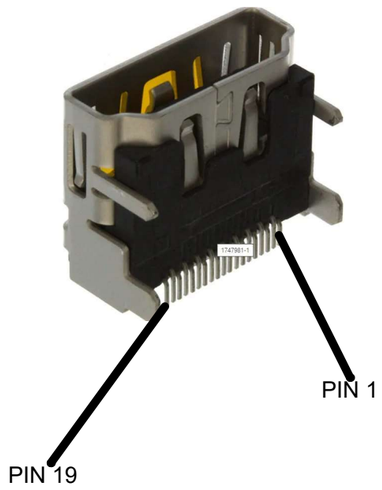
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

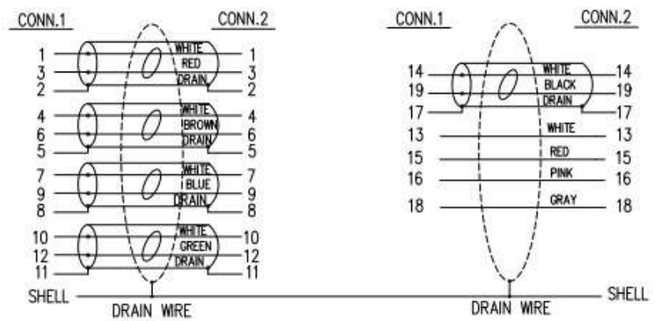
THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F2_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



PIN ASSIGNMENT





APOLLO CM v3		
Title: 6.10 FPGA#2 TEST CONNECTOR		
Size	Document Number: 6089-127	Rev: A
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QUAD "L" WIRING FOR FPGA#1 CAN BE FOUND ON SHEET 2.13: C2C AND TCDS QUADS

APOLLO CM v3			
Title: 7.01: FPGA#1 SM C2C ON QUAD L			
Size	Document Number: 6089-127		Rev: A
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7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_AD [19]
ac_nF1L_R0_AD [19]
ac_pF1L_R1_AD [21]
ac_nF1L_R1_AD [21]

U77-24 FPGA_VU13P_A2577 AC GTY QUAD 121

BB39 MGTREFCLK0P_121
BB40 MGTREFCLK0N_121
BA41 MGTREFCLK1P_121
BA42 MGTREFCLK1N_121

pF1_FF1_RECV11 BK34 / nF1_FF1_RECV11 BK35 — MGTYRXP0_121 / MGTYRXN0_121
pF1_FF1_XMIT11 BL37 / nF1_FF1_XMIT11 BL38 — MGTYTXP0_121 / MGTYTXN0_121
pF1_FF1_RECV10 BL32 / nF1_FF1_RECV10 BL33 — MGTYRXP1_121 / MGTYRXN1_121
pF1_FF1_XMIT10 BK39 / nF1_FF1_XMIT10 BK40 — MGTYTXP1_121 / MGTYTXN1_121
pF1_FF1_RECV9 BL46 / nF1_FF1_RECV9 BL47 — MGTYRXP2_121 / MGTYRXN2_121
pF1_FF1_XMIT9 BL41 / nF1_FF1_XMIT9 BL42 — MGTYTXP2_121 / MGTYTXN2_121
pF1_FF1_RECV8 BJ46 / nF1_FF1_RECV8 BJ47 — MGTYRXP3_121 / MGTYRXN3_121
pF1_FF1_XMIT8 BK43 / nF1_FF1_XMIT8 BK44 — MGTYTXP3_121 / MGTYTXN3_121

U77-25 FPGA_VU13P_A2577 AD GTY QUAD 122

AY39 MGTREFCLK0P_122
AY40 MGTREFCLK0N_122
AW41 MGTREFCLK1P_122
AW42 MGTREFCLK1N_122

pF1_FF1_RECV7 BH48 / nF1_FF1_RECV7 BH49 — MGTYRXP0_122 / MGTYRXN0_122
pF1_FF1_XMIT7 BG41 / nF1_FF1_XMIT7 BG42 — MGTYTXP0_122 / MGTYTXN0_122
pF1_FF1_RECV6 BG50 / nF1_FF1_RECV6 BG51 — MGTYRXP1_122 / MGTYRXN1_122
pF1_FF1_XMIT6 BJ41 / nF1_FF1_XMIT6 BJ42 — MGTYTXP1_122 / MGTYTXN1_122
pF1_FF1_RECV5 BG46 / nF1_FF1_RECV5 BG47 — MGTYRXP2_122 / MGTYRXN2_122
pF1_FF1_XMIT5 BH43 / nF1_FF1_XMIT5 BH44 — MGTYTXP2_122 / MGTYTXN2_122
pF1_FF1_RECV4 BF48 / nF1_FF1_RECV4 BF49 — MGTYRXP3_122 / MGTYRXN3_122
pF1_FF1_XMIT4 BF43 / nF1_FF1_XMIT4 BF44 — MGTYTXP3_122 / MGTYTXN3_122

U77-26 FPGA_VU13P_A2577 AE GTY QUAD 123

AV39 MGTREFCLK0P_123
AV40 MGTREFCLK0N_123
AU41 MGTREFCLK1P_123
AU42 MGTREFCLK1N_123

pF1_FF1_RECV3 BE50 / nF1_FF1_RECV3 BE51 — MGTYRXP0_123 / MGTYRXN0_123
pF1_FF1_XMIT3 BE45 / nF1_FF1_XMIT3 BE46 — MGTYTXP0_123 / MGTYTXN0_123
pF1_FF1_RECV2 BD48 / nF1_FF1_RECV2 BD49 — MGTYRXP1_123 / MGTYRXN1_123
pF1_FF1_XMIT2 BD43 / nF1_FF1_XMIT2 BD44 — MGTYTXP1_123 / MGTYTXN1_123
pF1_FF1_RECV1 BC50 / nF1_FF1_RECV1 BC51 — MGTYRXP2_123 / MGTYRXN2_123
pF1_FF1_XMIT1 BC45 / nF1_FF1_XMIT1 BC46 — MGTYTXP2_123 / MGTYTXN2_123
pF1_FF1_RECV0 BB48 / nF1_FF1_RECV0 BB49 — MGTYRXP3_123 / MGTYRXN3_123
pF1_FF1_XMIT0 BB43 / nF1_FF1_XMIT0 BB44 — MGTYTXP3_123 / MGTYTXN3_123

V_M3V3 — R505 3.3K 0603 — R506 3.3K 0603 — R508 2.2K 0603 — R507 2.2K 0603

U26-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F1_FF_RESET [38,61,62,63,64,65,66] — 6 /RESET — G1 G2
I2C_SDA_F1_FF1_XMIT [38] — 7 SDA
I2C_SCL_F1_FF1_XMIT [38] — 8 SCL
GND — 4 /SELECT
/F1_FF1_XMIT_INT [38] — 5 /INT
/F1_FF1_XMIT_PRESENT [38] — 3 /PRESENT
V_3V3 — 1 3.3V
V_F1_FF1_XMIT [31] — 10 3.8/3.3V (>=25G 3.8V, <=16G 3.3V)
9 RSVD
GND — 2 GND

C1088 22 UF 0603 6.3V — C1119 0.1 UF 0402 — L5 1.0 UH 0806 — C1152 22 UF 0603 6.3V — C1200 0.1 UF 0402
C1089 22 UF 0603 6.3V — C1120 0.1 UF 0402 — L6 1.0 UH 0806 — C1153 22 UF 0603 6.3V — C1201 0.1 UF 0402

U26-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

GND_B19 A19 — GND_A19 B19 — 0P A18 — 0N A17 — pF1_FF1_XMIT0 / nF1_FF1_XMIT0
GND_B16 A16 — GND_A16 B16 — 1P A18 — 1N A17 — pF1_FF1_XMIT1 / nF1_FF1_XMIT1
GND_B13 A13 — GND_A13 B13 — 2P B15 — 2N B14 — pF1_FF1_XMIT2 / nF1_FF1_XMIT2
GND_B10 A10 — GND_A10 B10 — 3P A15 — 3N A14 — pF1_FF1_XMIT3 / nF1_FF1_XMIT3
GND_B7 A7 — GND_A7 B7 — 4P B12 — 4N B11 — pF1_FF1_XMIT4 / nF1_FF1_XMIT4
GND_B4 A4 — GND_A4 B4 — 5P A12 — 5N A11 — pF1_FF1_XMIT5 / nF1_FF1_XMIT5
GND_B1 A1 — GND_A1 B1 — 6P B9 — 6N B8 — pF1_FF1_XMIT6 / nF1_FF1_XMIT6
7P A9 — 7N A8 — pF1_FF1_XMIT7 / nF1_FF1_XMIT7
8P B6 — 8N B5 — pF1_FF1_XMIT8 / nF1_FF1_XMIT8
9P A6 — 9N A5 — pF1_FF1_XMIT9 / nF1_FF1_XMIT9
10P B3 — 10N B2 — pF1_FF1_XMIT10 / nF1_FF1_XMIT10
11P A3 — 11N A2 — pF1_FF1_XMIT11 / nF1_FF1_XMIT11
GND

GND — 3 — 1 G1 2 G2 — 4 — VA6 VA5 VA4 VA3 VA2 VA1

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

V_M3V3 — R509 3.3K 0603 — R510 3.3K 0603 — R512 2.2K 0603 — R511 2.2K 0603

U27-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F1_FF_RESET [38,61,62,63,64,65,66] — 6 /RESET — G1 G2
I2C_SDA_F1_FF1_RECV [38] — 7 SDA
I2C_SCL_F1_FF1_RECV [38] — 8 SCL
GND — 4 /SELECT
/F1_FF1_RECV_INT [38] — 5 /INT
/F1_FF1_RECV_PRESENT [38] — 3 /PRESENT
V_3V3 — 1 3.3V
10 3.3V
9 RSVD
GND — 2 GND

C1108 22 UF 0603 6.3V — C1121 0.1 UF 0402 — L7 1.0 UH 0806 — C1154 22 UF 0603 6.3V — C1202 0.1 UF 0402
C1155 22 UF 0603 6.3V — C1203 0.1 UF 0402 — L8 1.0 UH 0806

U27-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

GND_B19 A19 — GND_A19 B19 — 0P A18 — 0N A17 — pF1_FF1_RECV0 / nF1_FF1_RECV0
GND_B16 A16 — GND_A16 B16 — 1P B18 — 1N B17 — pF1_FF1_RECV1 / nF1_FF1_RECV1
GND_B13 A13 — GND_A13 B13 — 2P A15 — 2N A14 — pF1_FF1_RECV2 / nF1_FF1_RECV2
GND_B10 A10 — GND_A10 B10 — 3P B15 — 3N B14 — pF1_FF1_RECV3 / nF1_FF1_RECV3
GND_B7 A7 — GND_A7 B7 — 4P A12 — 4N A11 — pF1_FF1_RECV4 / nF1_FF1_RECV4
GND_B4 A4 — GND_A4 B4 — 5P B12 — 5N B11 — pF1_FF1_RECV5 / nF1_FF1_RECV5
GND_B1 A1 — GND_A1 B1 — 6P A9 — 6N A8 — pF1_FF1_RECV6 / nF1_FF1_RECV6
7P B9 — 7N B8 — pF1_FF1_RECV7 / nF1_FF1_RECV7
8P A6 — 8N A5 — pF1_FF1_RECV8 / nF1_FF1_RECV8
9P B6 — 9N B5 — pF1_FF1_RECV9 / nF1_FF1_RECV9
10P A3 — 10N A2 — pF1_FF1_RECV10 / nF1_FF1_RECV10
11P B3 — 11N B2 — pF1_FF1_RECV11 / nF1_FF1_RECV11
GND

GND — 3 — 1 G1 2 G2 — 4 — VA12 VA11 VA10 VA9 VA8 VA7

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM v3	
Title	7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE
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7.03: FPGA#1 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_R [19]
ac_nF1L_R0_R [19]
ac_pF1L_R1_R [21]
ac_nF1L_R1_R [21]

U77-28 FPGA_VU13P_A2577 — GTY QUAD 125

AP39	MGTREFCLK0P_125	
AP40	MGTREFCLK0N_125	
AN41	MGTREFCLK1P_125	
AN42	MGTREFCLK1N_125	
pF1_FF2_RECV11	AU50	MGTYRXP0_125
nF1_FF2_RECV11	AU51	MGTYRXN0_125
pF1_FF2_XMIT11	AU45	MGTYTXP0_125
nF1_FF2_XMIT11	AU46	MGTYTXN0_125
pF1_FF2_RECV10	AT48	MGTYRXP1_125
nF1_FF2_RECV10	AT49	MGTYRXN1_125
pF1_FF2_XMIT10	AT43	MGTYTXP1_125
nF1_FF2_XMIT10	AT44	MGTYTXN1_125
pF1_FF2_RECV9	AR50	MGTYRXP2_125
nF1_FF2_RECV9	AR51	MGTYRXN2_125
pF1_FF2_XMIT9	AR45	MGTYTXP2_125
nF1_FF2_XMIT9	AR46	MGTYTXN2_125
pF1_FF2_RECV8	AP48	MGTYRXP3_125
nF1_FF2_RECV8	AP49	MGTYRXN3_125
pF1_FF2_XMIT8	AP43	MGTYTXP3_125
nF1_FF2_XMIT8	AP44	MGTYTXN3_125

U77-29 FPGA_VU13P_A2577 — GTY QUAD 126

AM39	MGTREFCLK0P_126	
AM40	MGTREFCLK0N_126	
AL41	MGTREFCLK1P_126	
AL42	MGTREFCLK1N_126	
pF1_FF2_RECV7	AN50	MGTYRXP0_126
nF1_FF2_RECV7	AN51	MGTYRXN0_126
pF1_FF2_XMIT7	AN45	MGTYTXP0_126
nF1_FF2_XMIT7	AN46	MGTYTXN0_126
pF1_FF2_RECV6	AM48	MGTYRXP1_126
nF1_FF2_RECV6	AM49	MGTYRXN1_126
pF1_FF2_XMIT6	AM43	MGTYTXP1_126
nF1_FF2_XMIT6	AM44	MGTYTXN1_126
pF1_FF2_RECV5	AL50	MGTYRXP2_126
nF1_FF2_RECV5	AL51	MGTYRXN2_126
pF1_FF2_XMIT5	AL45	MGTYTXP2_126
nF1_FF2_XMIT5	AL46	MGTYTXN2_126
pF1_FF2_RECV4	AK48	MGTYRXP3_126
nF1_FF2_RECV4	AK49	MGTYRXN3_126
pF1_FF2_XMIT4	AK43	MGTYTXP3_126
nF1_FF2_XMIT4	AK44	MGTYTXN3_126

U77-30 FPGA_VU13P_A2577 — GTY QUAD 127

AJ41	MGTREFCLK0P_127	
AJ42	MGTREFCLK0N_127	
AG41	MGTREFCLK1P_127	
AG42	MGTREFCLK1N_127	
pF1_FF2_RECV3	AJ50	MGTYRXP0_127
nF1_FF2_RECV3	AJ51	MGTYRXN0_127
pF1_FF2_XMIT3	AJ45	MGTYTXP0_127
nF1_FF2_XMIT3	AJ46	MGTYTXN0_127
pF1_FF2_RECV2	AH48	MGTYRXP1_127
nF1_FF2_RECV2	AH49	MGTYRXN1_127
pF1_FF2_XMIT2	AH43	MGTYTXP1_127
nF1_FF2_XMIT2	AH44	MGTYTXN1_127
pF1_FF2_RECV1	AG50	MGTYRXP2_127
nF1_FF2_RECV1	AG51	MGTYRXN2_127
pF1_FF2_XMIT1	AG45	MGTYTXP2_127
nF1_FF2_XMIT1	AG46	MGTYTXN2_127
pF1_FF2_RECV0	AF48	MGTYRXP3_127
nF1_FF2_RECV0	AF49	MGTYRXN3_127
pF1_FF2_XMIT0	AF43	MGTYTXP3_127
nF1_FF2_XMIT0	AF44	MGTYTXN3_127

U29-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F1_FF_RESET
[38,61,62,63,64,65,66]
I2C_SDA_F1_FF2_XMIT [38]
I2C_SCL_F1_FF2_XMIT [38]
/F1_FF2_XMIT_INT [38]
/F1_FF2_XMIT_PRESENT [38]
V_F1_FF2_XMIT [31]

V_M3V3: R517 3.3K 0603, R518 3.3K 0603, R520 2.2K 0603, R519 2.2K 0603
V_3V3: C1091 22 UF 0603 6.3V, C1124 0.1 UF 0402, L12 1.0 UH 0806, C1159 22 UF 0603 6.3V, C1206 0.1 UF 0402
V_F1_FF2_XMIT: C1092 22 UF 0603 6.3V, C1125 0.1 UF 0402, L13 1.0 UH 0806, C1160 22 UF 0603 6.3V, C1207 0.1 UF 0402

6	/RESET	G1 G2
7	SDA	
8	SCL	
4	/SELECT	
5	/INT	
3	/PRESENT	
1	3.3V	
10	3.8/3.3V >=25G 3.8V <=16G 3.3V	
9	RSVD	
2	GND	

U29-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19, A19	GND_B19, GND_A19	0P, 0N	B18, B17	pF1_FF2_XMIT0, nF1_FF2_XMIT0
		1P, 1N	A18, A17	pF1_FF2_XMIT1, nF1_FF2_XMIT1
B16, A16	GND_B16, GND_A16	2P, 2N	B15, B14	pF1_FF2_XMIT2, nF1_FF2_XMIT2
		3P, 3N	A15, A14	pF1_FF2_XMIT3, nF1_FF2_XMIT3
B13, A13	GND_B13, GND_A13	4P, 4N	B12, B11	pF1_FF2_XMIT4, nF1_FF2_XMIT4
		5P, 5N	A12, A11	pF1_FF2_XMIT5, nF1_FF2_XMIT5
B10, A10	GND_B10, GND_A10	6P, 6N	B9, B8	pF1_FF2_XMIT6, nF1_FF2_XMIT6
		7P, 7N	A9, A8	pF1_FF2_XMIT7, nF1_FF2_XMIT7
B7, A7	GND_B7, GND_A7	8P, 8N	B6, B5	pF1_FF2_XMIT8, nF1_FF2_XMIT8
		9P, 9N	A6, A5	pF1_FF2_XMIT9, nF1_FF2_XMIT9
B4, A4	GND_B4, GND_A4	10P, 10N	B3, B2	pF1_FF2_XMIT10, nF1_FF2_XMIT10
		11P, 11N	A3, A2	pF1_FF2_XMIT11, nF1_FF2_XMIT11
B1, A1	GND_B1, GND_A1			

GND; VA22, VA21, VA20, VA19, VA18, VA17

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U30-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F1_FF_RESET
[38,61,62,63,64,65,66]
I2C_SDA_F1_FF2_RECV [38]
I2C_SCL_F1_FF2_RECV [38]
/F1_FF2_RECV_INT [38]
/F1_FF2_RECV_PRESENT [38]

V_M3V3: R521 3.3K 0603, R522 3.3K 0603, R524 2.2K 0603, R523 2.2K 0603
V_3V3: C1110 22 UF 0603 6.3V, C1126 0.1 UF 0402, L14 1.0 UH 0806, C1161 22 UF 0603 6.3V, C1208 0.1 UF 0402
L15 1.0 UH 0806, C1162 22 UF 0603 6.3V, C1209 0.1 UF 0402

6	/RESET	G1 G2
7	SDA	
8	SCL	
4	/SELECT	
5	/INT	
3	/PRESENT	
1	3.3V	
10	3.3V	
9	RSVD	
2	GND	

U30-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19, A19	GND_B19, GND_A19	0P, 0N	A18, A17	pF1_FF2_RECV0, nF1_FF2_RECV0
		1P, 1N	B18, B17	pF1_FF2_RECV1, nF1_FF2_RECV1
B16, A16	GND_B16, GND_A16	2P, 2N	A15, A14	pF1_FF2_RECV2, nF1_FF2_RECV2
		3P, 3N	B15, B14	pF1_FF2_RECV3, nF1_FF2_RECV3
B13, A13	GND_B13, GND_A13	4P, 4N	A12, A11	pF1_FF2_RECV4, nF1_FF2_RECV4
		5P, 5N	B12, B11	pF1_FF2_RECV5, nF1_FF2_RECV5
B10, A10	GND_B10, GND_A10	6P, 6N	A9, A8	pF1_FF2_RECV6, nF1_FF2_RECV6
		7P, 7N	B9, B8	pF1_FF2_RECV7, nF1_FF2_RECV7
B7, A7	GND_B7, GND_A7	8P, 8N	A6, A5	pF1_FF2_RECV8, nF1_FF2_RECV8
		9P, 9N	B6, B5	pF1_FF2_RECV9, nF1_FF2_RECV9
B4, A4	GND_B4, GND_A4	10P, 10N	A3, A2	pF1_FF2_RECV10, nF1_FF2_RECV10
		11P, 11N	B3, B2	pF1_FF2_RECV11, nF1_FF2_RECV11
B1, A1	GND_B1, GND_A1			

GND; VA28, VA27, VA26, VA25, VA24, VA23

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3			
Title: 7.03: FPGA#1 FF#2 X12 ON QUADS Q R S			
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7.04: FPGA#1 FF#3 X12 ON QUADS T U V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_U [19]
ac_nF1L_R0_U [19]
ac_pF1L_R1_U [21]
ac_nF1L_R1_U [21]

V_M3V3
R525 3.3K 0603
R526 3.3K 0603
R528 2.2K 0603
R527 2.2K 0603

U31-1
FIREFLY_XMIT_X12
FIREFLY XMIT X12

/F1_FF_RESET [38,61,62,63,64,65,66]
I2C_SDA_F1_FF3_XMIT [38]
I2C_SCL_F1_FF3_XMIT [38]
/F1_FF3_XMIT_INT [38]
/F1_FF3_XMIT_PRESENT [38]
V_3V3
V_F1_FF3_XMIT [31]

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.8/3.3V (>=25G 3.8V, <=16G 3.3V), RSVD, GND, G1, G2

C1111 22 UF 0603 6.3V
C1128 0.1 UF 0402
L16 1.0 UH 0806
C1163 22 UF 0603 6.3V
C1210 0.1 UF 0402
C1093 22 UF 0603 6.3V
C1127 0.1 UF 0402
L17 1.0 UH 0806
C1164 22 UF 0603 6.3V
C1211 0.1 UF 0402

U31-2
FIREFLY_XMIT_X12
FIREFLY XMIT X12

VA34, VA33, VA32, VA31, VA30, VA29

pF1_FF3_XMIT0 / nF1_FF3_XMIT0
pF1_FF3_XMIT1 / nF1_FF3_XMIT1
pF1_FF3_XMIT2 / nF1_FF3_XMIT2
pF1_FF3_XMIT3 / nF1_FF3_XMIT3
pF1_FF3_XMIT4 / nF1_FF3_XMIT4
pF1_FF3_XMIT5 / nF1_FF3_XMIT5
pF1_FF3_XMIT6 / nF1_FF3_XMIT6
pF1_FF3_XMIT7 / nF1_FF3_XMIT7
pF1_FF3_XMIT8 / nF1_FF3_XMIT8
pF1_FF3_XMIT9 / nF1_FF3_XMIT9
pF1_FF3_XMIT10 / nF1_FF3_XMIT10
pF1_FF3_XMIT11 / nF1_FF3_XMIT11

U77-31
FPGA_VU13P_A2577
T GTY QUAD 128

MGTREFCLK0P_128 / MGTREFCLK0N_128 (AE41 / AE42)
MGTREFCLK1P_128 / MGTREFCLK1N_128 (AC41 / AC42)

pF1_FF3_RECV11 AE50 / nF1_FF3_RECV11 AE51 — MGTYRXP0_128 / MGTYRXN0_128
pF1_FF3_XMIT11 AE45 / nF1_FF3_XMIT11 AE46 — MGTYTXP0_128 / MGTYTXN0_128
pF1_FF3_RECV10 AD48 / nF1_FF3_RECV10 AD49 — MGTYRXP1_128 / MGTYRXN1_128
pF1_FF3_XMIT10 AD43 / nF1_FF3_XMIT10 AD44 — MGTYTXP1_128 / MGTYTXN1_128
pF1_FF3_RECV9 AC50 / nF1_FF3_RECV9 AC51 — MGTYRXP2_128 / MGTYRXN2_128
pF1_FF3_XMIT9 AC45 / nF1_FF3_XMIT9 AC46 — MGTYTXP2_128 / MGTYTXN2_128
pF1_FF3_RECV8 AB48 / nF1_FF3_RECV8 AB49 — MGTYRXP3_128 / MGTYRXN3_128
pF1_FF3_XMIT8 AB43 / nF1_FF3_XMIT8 AB44 — MGTYTXP3_128 / MGTYTXN3_128

U77-32
FPGA_VU13P_A2577
U GTY QUAD 129

MGTREFCLK0P_129 / MGTREFCLK0N_129 (AA41 / AA42)
MGTREFCLK1P_129 / MGTREFCLK1N_129 (Y39 / Y40)

pF1_FF3_RECV7 AA50 / nF1_FF3_RECV7 AA51 — MGTYRXP0_129 / MGTYRXN0_129
pF1_FF3_XMIT7 AA45 / nF1_FF3_XMIT7 AA46 — MGTYTXP0_129 / MGTYTXN0_129
pF1_FF3_RECV6 Y48 / nF1_FF3_RECV6 Y49 — MGTYRXP1_129 / MGTYRXN1_129
pF1_FF3_XMIT6 Y43 / nF1_FF3_XMIT6 Y44 — MGTYTXP1_129 / MGTYTXN1_129
pF1_FF3_RECV5 W50 / nF1_FF3_RECV5 W51 — MGTYRXP2_129 / MGTYRXN2_129
pF1_FF3_XMIT5 W45 / nF1_FF3_XMIT5 W46 — MGTYTXP2_129 / MGTYTXN2_129
pF1_FF3_RECV4 V48 / nF1_FF3_RECV4 V49 — MGTYRXP3_129 / MGTYRXN3_129
pF1_FF3_XMIT4 V43 / nF1_FF3_XMIT4 V44 — MGTYTXP3_129 / MGTYTXN3_129

V_M3V3
R529 3.3K 0603
R530 3.3K 0603
R532 2.2K 0603
R531 2.2K 0603

U32-1
FIREFLY_RECV_X12
FIREFLY RECV X12

/F1_FF_RESET [38,61,62,63,64,65,66]
I2C_SDA_F1_FF3_RECV [38]
I2C_SCL_F1_FF3_RECV [38]
/F1_FF3_RECV_INT [38]
/F1_FF3_RECV_PRESENT [38]
V_3V3

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, RSVD, GND, G1, G2

C1094 22 UF 0603 6.3V
C1129 0.1 UF 0402
L18 1.0 UH 0806
C1165 22 UF 0603 6.3V
C1212 0.1 UF 0402
L19 1.0 UH 0806
C1166 22 UF 0603 6.3V
C1213 0.1 UF 0402

U32-2
FIREFLY_RECV_X12
FIREFLY RECV X12

VA40, VA39, VA38, VA37, VA36, VA35

pF1_FF3_RECV0 / nF1_FF3_RECV0
pF1_FF3_RECV1 / nF1_FF3_RECV1
pF1_FF3_RECV2 / nF1_FF3_RECV2
pF1_FF3_RECV3 / nF1_FF3_RECV3
pF1_FF3_RECV4 / nF1_FF3_RECV4
pF1_FF3_RECV5 / nF1_FF3_RECV5
pF1_FF3_RECV6 / nF1_FF3_RECV6
pF1_FF3_RECV7 / nF1_FF3_RECV7
pF1_FF3_RECV8 / nF1_FF3_RECV8
pF1_FF3_RECV9 / nF1_FF3_RECV9
pF1_FF3_RECV10 / nF1_FF3_RECV10
pF1_FF3_RECV11 / nF1_FF3_RECV11

U77-33
FPGA_VU13P_A2577
V GTY QUAD 130

MGTREFCLK0P_130 / MGTREFCLK0N_130 (W41 / W42)
MGTREFCLK1P_130 / MGTREFCLK1N_130 (V39 / V40)

pF1_FF3_RECV3 U50 / nF1_FF3_RECV3 U51 — MGTYRXP0_130 / MGTYRXN0_130
pF1_FF3_XMIT3 U45 / nF1_FF3_XMIT3 U46 — MGTYTXP0_130 / MGTYTXN0_130
pF1_FF3_RECV2 T48 / nF1_FF3_RECV2 T49 — MGTYRXP1_130 / MGTYRXN1_130
pF1_FF3_XMIT2 T43 / nF1_FF3_XMIT2 T44 — MGTYTXP1_130 / MGTYTXN1_130
pF1_FF3_RECV1 R50 / nF1_FF3_RECV1 R51 — MGTYRXP2_130 / MGTYRXN2_130
pF1_FF3_XMIT1 R45 / nF1_FF3_XMIT1 R46 — MGTYTXP2_130 / MGTYTXN2_130
pF1_FF3_RECV0 P48 / nF1_FF3_RECV0 P49 — MGTYRXP3_130 / MGTYRXN3_130
pF1_FF3_XMIT0 P43 / nF1_FF3_XMIT0 P44 — MGTYTXP3_130 / MGTYTXN3_130

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

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7.05: FPGA#1 FF#4 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_Y [19]
ac_nF1L_R0_Y [19]
ac_pF1L_R1_Y [21]
ac_nF1L_R1_Y [21]

U77-35 FPGA_VU13P_A2577 — X — GTY QUAD 132

R41 MGTREFCLK0P_132
R42 MGTREFCLK0N_132
P39 MGTREFCLK1P_132
P40 MGTREFCLK1N_132

pF1_FF4_RECV11 J50 — MGTYRXP0_132
nF1_FF4_RECV11 J51 — MGTYRXN0_132
pF1_FF4_XMIT11 J45 — MGTYTXP0_132
nF1_FF4_XMIT11 J46 — MGTYTXN0_132
pF1_FF4_RECV10 H48 — MGTYRXP1_132
nF1_FF4_RECV10 H49 — MGTYRXN1_132
pF1_FF4_XMIT10 H43 — MGTYTXP1_132
nF1_FF4_XMIT10 H44 — MGTYTXN1_132
pF1_FF4_RECV9 G50 — MGTYRXP2_132
nF1_FF4_RECV9 G51 — MGTYRXN2_132
pF1_FF4_XMIT9 G45 — MGTYTXP2_132
nF1_FF4_XMIT9 G46 — MGTYTXN2_132
pF1_FF4_RECV8 F48 — MGTYRXP3_132
nF1_FF4_RECV8 F49 — MGTYRXN3_132
pF1_FF4_XMIT8 F43 — MGTYTXP3_132
nF1_FF4_XMIT8 F44 — MGTYTXN3_132

U77-36 FPGA_VU13P_A2577 — Y — GTY QUAD 133

N41 MGTREFCLK0P_133
N42 MGTREFCLK0N_133
M39 MGTREFCLK1P_133
M40 MGTREFCLK1N_133

pF1_FF4_RECV7 E50 — MGTYRXP0_133
nF1_FF4_RECV7 E51 — MGTYRXN0_133
pF1_FF4_XMIT7 D43 — MGTYTXP0_133
nF1_FF4_XMIT7 D44 — MGTYTXN0_133
pF1_FF4_RECV6 D48 — MGTYRXP1_133
nF1_FF4_RECV6 D49 — MGTYRXN1_133
pF1_FF4_XMIT6 B43 — MGTYTXP1_133
nF1_FF4_XMIT6 B44 — MGTYTXN1_133
pF1_FF4_RECV5 E46 — MGTYRXP2_133
nF1_FF4_RECV5 E47 — MGTYRXN2_133
pF1_FF4_XMIT5 C41 — MGTYTXP2_133
nF1_FF4_XMIT5 C42 — MGTYTXN2_133
pF1_FF4_RECV4 C46 — MGTYRXP3_133
nF1_FF4_RECV4 C47 — MGTYRXN3_133
pF1_FF4_XMIT4 E41 — MGTYTXP3_133
nF1_FF4_XMIT4 E42 — MGTYTXN3_133

U77-37 FPGA_VU13P_A2577 — Z — GTY QUAD 134

L41 MGTREFCLK0P_134
L42 MGTREFCLK0N_134
K39 MGTREFCLK1P_134
K40 MGTREFCLK1N_134

pF1_FF4_RECV3 A46 — MGTYRXP0_134
nF1_FF4_RECV3 A47 — MGTYRXN0_134
pF1_FF4_XMIT3 A41 — MGTYTXP0_134
nF1_FF4_XMIT3 A42 — MGTYTXN0_134
pF1_FF4_RECV2 A32 — MGTYRXP1_134
nF1_FF4_RECV2 A33 — MGTYRXN1_134
pF1_FF4_XMIT2 B39 — MGTYTXP1_134
nF1_FF4_XMIT2 B40 — MGTYTXN1_134
pF1_FF4_RECV1 B34 — MGTYRXP2_134
nF1_FF4_RECV1 B35 — MGTYRXN2_134
pF1_FF4_XMIT1 A37 — MGTYTXP2_134
nF1_FF4_XMIT1 A38 — MGTYTXN2_134
pF1_FF4_RECV0 C32 — MGTYRXP3_134
nF1_FF4_RECV0 C33 — MGTYRXN3_134
pF1_FF4_XMIT0 C37 — MGTYTXP3_134
nF1_FF4_XMIT0 C38 — MGTYTXN3_134

U34-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F1_FF_RESET [38,61,62,63,64,65,66] — /RESET (G1, G2)
I2C_SDA_F1_FF4_XMIT [38] — SDA
I2C_SCL_F1_FF4_XMIT [38] — SCL
GND — /SELECT
/F1_FF4_XMIT_INT [38] — /INT
/F1_FF4_XMIT_PRESENT [38] — /PRESENT
V_3V3 — 3.3V
V_F1_FF4_XMIT [31] — 3.8/3.3V (>=25G 3.8V, <=16G 3.3V)
RSVD
GND
<Implementation>

V_M3V3: R537 3.3K 0603, R538 3.3K 0603, R540 2.2K 0603, R539 2.2K 0603
V_3V3: L23 1.0 UH 0806, L24 1.0 UH 0806
C1096 22 UF 0603 6.3V, C1132 0.1 UF 0402, C1170 22 UF 0603 6.3V, C1216 0.1 UF 0402
C1097 22 UF 0603 6.3V, C1133 0.1 UF 0402, C1171 22 UF 0603 6.3V, C1217 0.1 UF 0402

U34-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

GND_B19 (B19, A19) — 0P/0N — pF1_FF4_XMIT0 (B18, B17) / nF1_FF4_XMIT0
GND_B16 (B16, A16) — 1P/1N — pF1_FF4_XMIT1 (A18, A17) / nF1_FF4_XMIT1
GND_B13 (B13, A13) — 2P/2N — pF1_FF4_XMIT2 (B15, B14) / nF1_FF4_XMIT2
GND_B10 (B10, A10) — 3P/3N — pF1_FF4_XMIT3 (A15, A14) / nF1_FF4_XMIT3
GND_B7 (B7, A7) — 4P/4N — pF1_FF4_XMIT4 (B12, B11) / nF1_FF4_XMIT4
GND_B4 (B4, A4) — 5P/5N — pF1_FF4_XMIT5 (A12, A11) / nF1_FF4_XMIT5
GND_B1 (B1, A1) — 6P/6N — pF1_FF4_XMIT6 (B9, B8) / nF1_FF4_XMIT6
7P/7N — pF1_FF4_XMIT7 (A9, A8) / nF1_FF4_XMIT7
8P/8N — pF1_FF4_XMIT8 (B6, B5) / nF1_FF4_XMIT8
9P/9N — pF1_FF4_XMIT9 (A6, A5) / nF1_FF4_XMIT9
10P/10N — pF1_FF4_XMIT10 (B3, B2) / nF1_FF4_XMIT10
11P/11N — pF1_FF4_XMIT11 (A3, A2) / nF1_FF4_XMIT11

GND — VA50, VA49, VA48, VA47, VA46, VA45

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U35-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F1_FF_RESET [38,61,62,63,64,65,66] — /RESET (G1, G2)
I2C_SDA_F1_FF4_RECV [38] — SDA
I2C_SCL_F1_FF4_RECV [38] — SCL
GND — /SELECT
/F1_FF4_RECV_INT [38] — /INT
/F1_FF4_RECV_PRESENT [38] — /PRESENT
V_3V3 — 3.3V
3.3V
RSVD
GND
<Implementation>

V_M3V3: R541 3.3K 0603, R542 3.3K 0603, R544 2.2K 0603, R543 2.2K 0603
V_3V3: L25 1.0 UH 0806, L26 1.0 UH 0806
C1113 22 UF 0603 6.3V, C1134 0.1 UF 0402, C1172 22 UF 0603 6.3V, C1218 0.1 UF 0402
C1173 22 UF 0603 6.3V, C1219 0.1 UF 0402

U35-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

GND_B19 (B19, A19) — 0P/0N — pF1_FF4_RECV0 (A18, A17) / nF1_FF4_RECV0
GND_B16 (B16, A16) — 1P/1N — pF1_FF4_RECV1 (B18, B17) / nF1_FF4_RECV1
GND_B13 (B13, A13) — 2P/2N — pF1_FF4_RECV2 (A15, A14) / nF1_FF4_RECV2
GND_B10 (B10, A10) — 3P/3N — pF1_FF4_RECV3 (B15, B14) / nF1_FF4_RECV3
GND_B7 (B7, A7) — 4P/4N — pF1_FF4_RECV4 (A12, A11) / nF1_FF4_RECV4
GND_B4 (B4, A4) — 5P/5N — pF1_FF4_RECV5 (B12, B11) / nF1_FF4_RECV5
GND_B1 (B1, A1) — 6P/6N — pF1_FF4_RECV6 (A9, A8) / nF1_FF4_RECV6
7P/7N — pF1_FF4_RECV7 (B9, B8) / nF1_FF4_RECV7
8P/8N — pF1_FF4_RECV8 (A6, A5) / nF1_FF4_RECV8
9P/9N — pF1_FF4_RECV9 (B6, B5) / nF1_FF4_RECV9
10P/10N — pF1_FF4_RECV10 (A3, A2) / nF1_FF4_RECV10
11P/11N — pF1_FF4_RECV11 (B3, B2) / nF1_FF4_RECV11

GND — VA56, VA55, VA54, VA53, VA52, VA51

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3		
Title: 7.05: FPGA#1 FF#4 X12 ON QUADS X Y Z		
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7.06: FPGA#1 FF#5 X4 ON QUAD AF

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

U77-27
FPGA_VU13P_A2577
AF GTY QUAD 124

ac_pF1L_R0_AF [19]
ac_nF1L_R0_AF [19]
ac_pF1L_R1_AF [20]
ac_nF1L_R1_AF [20]

AT39 MGTREFCLK0P_124
AT40 MGTREFCLK0N_124
AR41 MGTREFCLK1P_124
AR42 MGTREFCLK1N_124

pF1_FF5_RECV0 BA50 MGTYRXP0_124
nF1_FF5_RECV0 BA51 MGTYRXN0_124
pF1_FF5_XMIT0 BA45 MGTYTXP0_124
nF1_FF5_XMIT0 BA46 MGTYTXN0_124
pF1_FF5_RECV1 AY48 MGTYRXP1_124
nF1_FF5_RECV1 AY49 MGTYRXN1_124
pF1_FF5_XMIT1 AY43 MGTYTXP1_124
nF1_FF5_XMIT1 AY44 MGTYTXN1_124
pF1_FF5_RECV2 AW50 MGTYRXP2_124
nF1_FF5_RECV2 AW51 MGTYRXN2_124
pF1_FF5_XMIT2 AW45 MGTYTXP2_124
nF1_FF5_XMIT2 AW46 MGTYTXN2_124
pF1_FF5_RECV3 AV48 MGTYRXP3_124
nF1_FF5_RECV3 AV49 MGTYRXN3_124
pF1_FF5_XMIT3 AV43 MGTYTXP3_124
nF1_FF5_XMIT3 AV44 MGTYTXN3_124

V_M3V3 R513 3.3K 0603 R514 3.3K 0603 R516 2.2K 0603 R515 2.2K 0603

U28-1
FIREFLY_XCVR_X4
FIREFLY XCVR X4

/F1_FF_RESET [38,61,62,63,64,66] → /RESET (G1 G2)
I2C_SDA_F1_FF5_XCVR [38] → SDA
I2C_SCL_F1_FF5_XCVR [38] → SCL
GND → /SELECT
/F1_FF5_XCVR_INT [38] → /INT
/F1_FF5_XCVR_PRESENT [38] → /PRESENT
V_3V3 → 3.3V
V_3V3 → 3.3V
V_1V8 → 1.8V
GND → GND

C1109 22 UF 0603 6.3V, C1123 0.1 UF 0402, L9 1.0 UH 0806, C1156 22 UF 0603 6.3V, C1204 0.1 UF 0402
L11 1.0 UH 0806, C1158 22 UF 0603 6.3V, C1205 0.1 UF 0402
C1090 22 UF 0603 6.3V, C1122 0.1 UF 0402, L10 1.0 UH 0806, C1157 22 UF 0603 6.3V, C1196 0.1 UF 0402

U28-2
FIREFLY_XCVR_X4
FIREFLY XCVR X4

GND_B19 A19, GND_A19 RX1P B17 pF1_FF5_RECV0, RX1N B18 nF1_FF5_RECV0
RX2P B17 pF1_FF5_RECV1, RX2N A18 nF1_FF5_RECV1
GND_B16 A16, GND_A16 RX3P B14 pF1_FF5_RECV2, RX3N B15 nF1_FF5_RECV2
RX4P A14 pF1_FF5_RECV3, RX4N A15 nF1_FF5_RECV3
GND_B13 A13, GND_A13
GND_B7 A7, GND_A7 TX4P B6 pF1_FF5_XMIT3, TX4N B5 nF1_FF5_XMIT3
TX3P A6 pF1_FF5_XMIT2, TX3N A5 nF1_FF5_XMIT2
GND_B4 A4, GND_A4 TX2P B3 pF1_FF5_XMIT1, TX2N B2 nF1_FF5_XMIT1
TX1P A3 pF1_FF5_XMIT0, TX1N A2 nF1_FF5_XMIT0
GND_B1 A1, GND_A1

GND VA16, GND VA15, GND VA14, GND VA13

R489 49p9 0402 B12 RESVD_B12
R488 49p9 0402 B11 RESVD_B11
R487 49p9 0402 B10 RESVD_B10
R486 49p9 0402 B9 RESVD_B9
R485 49p9 0402 B8 RESVD_B8
R43 49p9 0402 A12 RESVD_A12
R42 49p9 0402 A11 RESVD_A11
R41 49p9 0402 A10 RESVD_A10
R40 49p9 0402 A9 RESVD_A9
R39 49p9 0402 A8 RESVD_A8

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

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Title: 7.06: FPGA#1 FF#5 X4 ON QUAD AF
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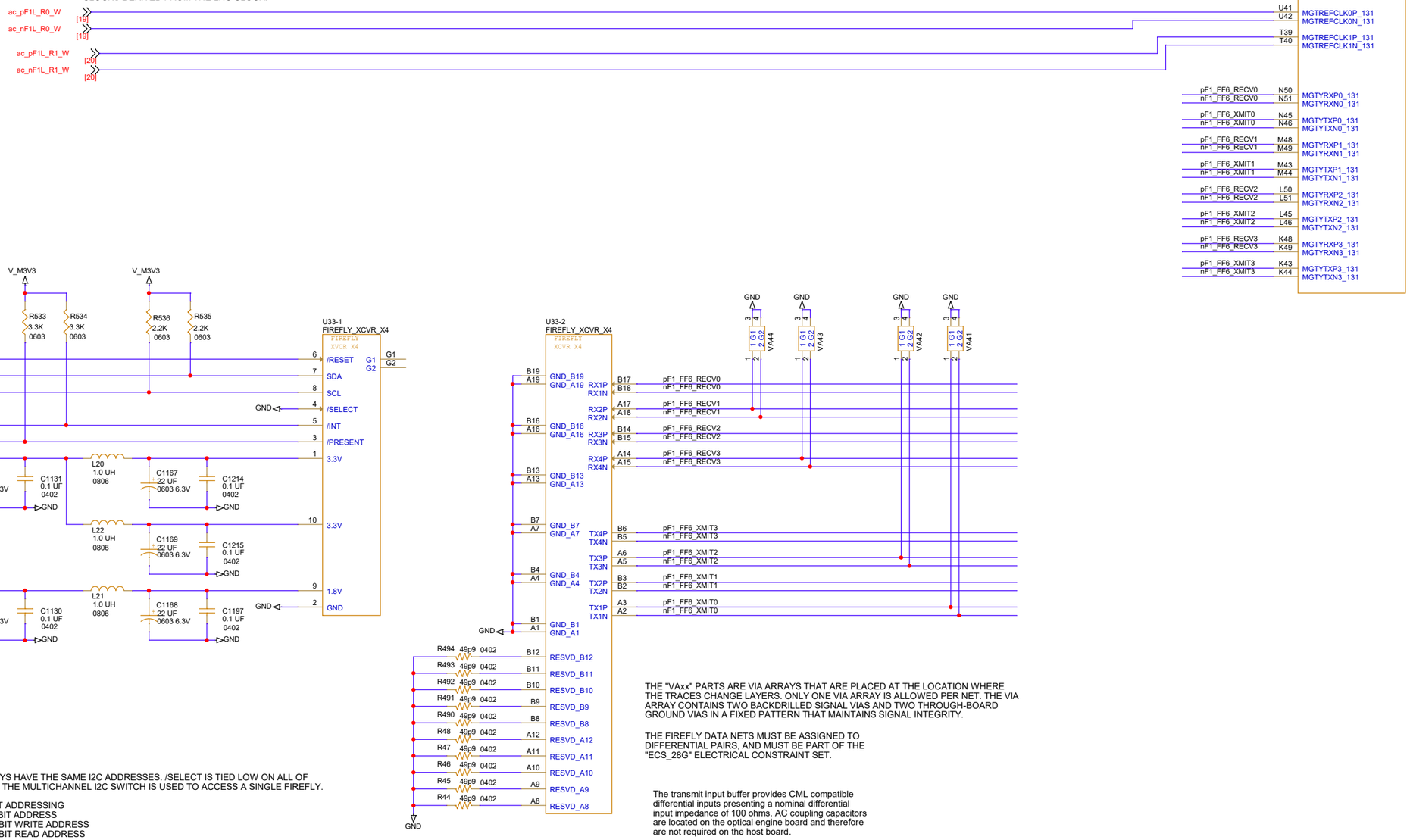
7.07: FPGA#1 FF#6 X4 ON QUAD W

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM v3

Title: 7.07: FPGA#1 FF#6 X4 ON QUAD W

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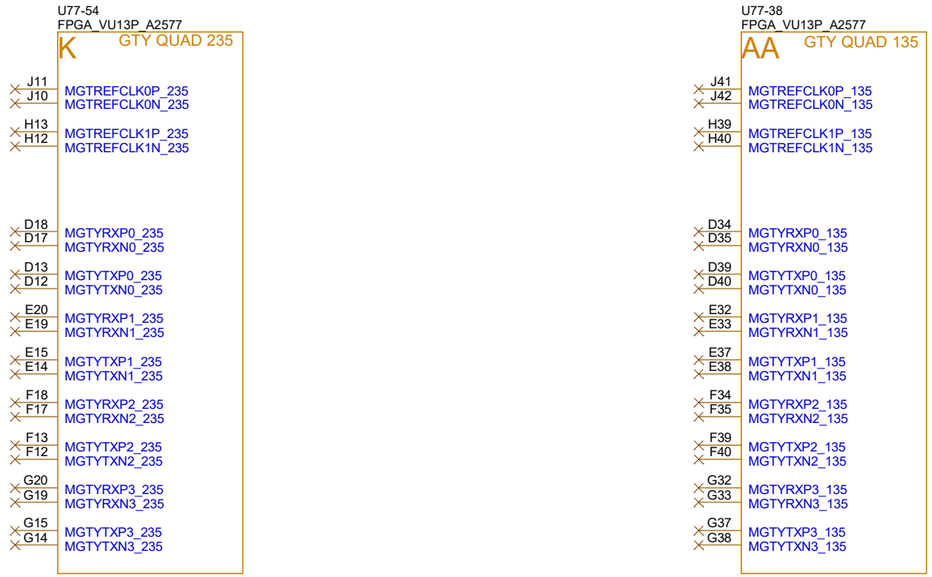
7.08: FPGA#1 UNUSED QUADS K, AA



APOLLO CM v3		
Title: 7.08: FPGA#1 UNUSED QUADS K, AA		
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QUAD "L" WIRING FOR FPGA#2 CAN BE FOUND ON SHEET 2.13: C2C AND TCDS QUADS

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Title
8.01: FPGA#2 SM C2C ON QUAD L

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8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_AD [19]
ac_nF2L_R0_AD [19]
ac_pF2L_R1_AD [21]
ac_nF2L_R1_AD [21]

U78-24 FPGA_VU13P_A2577 AC GTY QUAD 121

BB39 MGTREFCLK0P_121
BB40 MGTREFCLK0N_121
BA41 MGTREFCLK1P_121
BA42 MGTREFCLK1N_121

pF2_FF1_RECV11 BK34 / nF2_FF1_RECV11 BK35 — MGTYRXP0_121 / MGTYRXN0_121
pF2_FF1_XMIT11 BL37 / nF2_FF1_XMIT11 BL38 — MGTYTXP0_121 / MGTYTXN0_121
pF2_FF1_RECV10 BL32 / nF2_FF1_RECV10 BL33 — MGTYRXP1_121 / MGTYRXN1_121
pF2_FF1_XMIT10 BK39 / nF2_FF1_XMIT10 BK40 — MGTYTXP1_121 / MGTYTXN1_121
pF2_FF1_RECV9 BL46 / nF2_FF1_RECV9 BL47 — MGTYRXP2_121 / MGTYRXN2_121
pF2_FF1_XMIT9 BL41 / nF2_FF1_XMIT9 BL42 — MGTYTXP2_121 / MGTYTXN2_121
pF2_FF1_RECV8 BJ46 / nF2_FF1_RECV8 BJ47 — MGTYRXP3_121 / MGTYRXN3_121
pF2_FF1_XMIT8 BK43 / nF2_FF1_XMIT8 BK44 — MGTYTXP3_121 / MGTYTXN3_121

U78-25 FPGA_VU13P_A2577 AD GTY QUAD 122

AY39 MGTREFCLK0P_122
AY40 MGTREFCLK0N_122
AW41 MGTREFCLK1P_122
AW42 MGTREFCLK1N_122

pF2_FF1_RECV7 BH48 / nF2_FF1_RECV7 BH49 — MGTYRXP0_122 / MGTYRXN0_122
pF2_FF1_XMIT7 BG41 / nF2_FF1_XMIT7 BG42 — MGTYTXP0_122 / MGTYTXN0_122
pF2_FF1_RECV6 BG50 / nF2_FF1_RECV6 BG51 — MGTYRXP1_122 / MGTYRXN1_122
pF2_FF1_XMIT6 BJ41 / nF2_FF1_XMIT6 BJ42 — MGTYTXP1_122 / MGTYTXN1_122
pF2_FF1_RECV5 BG46 / nF2_FF1_RECV5 BG47 — MGTYRXP2_122 / MGTYRXN2_122
pF2_FF1_XMIT5 BH43 / nF2_FF1_XMIT5 BH44 — MGTYTXP2_122 / MGTYTXN2_122
pF2_FF1_RECV4 BF48 / nF2_FF1_RECV4 BF49 — MGTYRXP3_122 / MGTYRXN3_122
pF2_FF1_XMIT4 BF43 / nF2_FF1_XMIT4 BF44 — MGTYTXP3_122 / MGTYTXN3_122

U78-26 FPGA_VU13P_A2577 AE GTY QUAD 123

AV39 MGTREFCLK0P_123
AV40 MGTREFCLK0N_123
AU41 MGTREFCLK1P_123
AU42 MGTREFCLK1N_123

pF2_FF1_RECV3 BE50 / nF2_FF1_RECV3 BE51 — MGTYRXP0_123 / MGTYRXN0_123
pF2_FF1_XMIT3 BE45 / nF2_FF1_XMIT3 BE46 — MGTYTXP0_123 / MGTYTXN0_123
pF2_FF1_RECV2 BD48 / nF2_FF1_RECV2 BD49 — MGTYRXP1_123 / MGTYRXN1_123
pF2_FF1_XMIT2 BD43 / nF2_FF1_XMIT2 BD44 — MGTYTXP1_123 / MGTYTXN1_123
pF2_FF1_RECV1 BC50 / nF2_FF1_RECV1 BC51 — MGTYRXP2_123 / MGTYRXN2_123
pF2_FF1_XMIT1 BC45 / nF2_FF1_XMIT1 BC46 — MGTYTXP2_123 / MGTYTXN2_123
pF2_FF1_RECV0 BB48 / nF2_FF1_RECV0 BB49 — MGTYRXP3_123 / MGTYRXN3_123
pF2_FF1_XMIT0 BB43 / nF2_FF1_XMIT0 BB44 — MGTYTXP3_123 / MGTYTXN3_123

V_M3V3
R545 3.3K 0603
R546 3.3K 0603
R548 2.2K 0603
R547 2.2K 0603

U36-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F2_FF_RESET [39,69,70,71,72,73,74] → /RESET (6), G1, G2
I2C_SDA_F2_FF1_XMIT [39] → SDA (7)
I2C_SCL_F2_FF1_XMIT [39] → SCL (8)
GND → /SELECT (4)
/F2_FF1_XMIT_INT [39] → /INT (5)
/F2_FF1_XMIT_PRESENT [39] → /PRESENT (3)
V_3V3 → 3.3V (1)
C1098 22 UF 0603 6.3V; C1135 0.1 UF 0402; L27 1.0 UH 0806; C1174 22 UF 0603 6.3V; C1220 0.1 UF 0402
V_F2_FF1_XMIT [31] → 3.8/3.3V (10) >=25G 3.8V <=16G 3.3V
C1099 22 UF 0603 6.3V; C1136 0.1 UF 0402; L28 1.0 UH 0806; C1175 22 UF 0603 6.3V; C1221 0.1 UF 0402
RSVD (9)
GND (2)

U36-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 A19	GND_B19 GND_A19	0P 0N	B18 A18 pF2_FF1_XMIT0 / B17 A17 nF2_FF1_XMIT0
		1P 1N	A18 A17 pF2_FF1_XMIT1 / nF2_FF1_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14 pF2_FF1_XMIT2 / nF2_FF1_XMIT2
		3P 3N	A15 A14 pF2_FF1_XMIT3 / nF2_FF1_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11 pF2_FF1_XMIT4 / nF2_FF1_XMIT4
		5P 5N	A12 A11 pF2_FF1_XMIT5 / nF2_FF1_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8 pF2_FF1_XMIT6 / nF2_FF1_XMIT6
		7P 7N	A9 A8 pF2_FF1_XMIT7 / nF2_FF1_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5 pF2_FF1_XMIT8 / nF2_FF1_XMIT8
		9P 9N	A6 A5 pF2_FF1_XMIT9 / nF2_FF1_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2 pF2_FF1_XMIT10 / nF2_FF1_XMIT10
		11P 11N	A3 A2 pF2_FF1_XMIT11 / nF2_FF1_XMIT11
B1 A1	GND_B1 GND_A1		

GND; 1 G1 2 G2 VA62; VA61; VA60; VA59; VA58; VA57

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

V_M3V3
R549 3.3K 0603
R550 3.3K 0603
R552 2.2K 0603
R551 2.2K 0603

U37-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F2_FF_RESET [39,69,70,71,72,73,74] → /RESET (6), G1, G2
I2C_SDA_F2_FF1_RECV [39] → SDA (7)
I2C_SCL_F2_FF1_RECV [39] → SCL (8)
GND → /SELECT (4)
/F2_FF1_RECV_INT [39] → /INT (5)
/F2_FF1_RECV_PRESENT [39] → /PRESENT (3)
V_3V3 → 3.3V (1)
C1114 22 UF 0603 6.3V; C1137 0.1 UF 0402; L29 1.0 UH 0806; C1176 22 UF 0603 6.3V; C1222 0.1 UF 0402
3.3V (10)
L30 1.0 UH 0806; C1177 22 UF 0603 6.3V; C1223 0.1 UF 0402
RSVD (9)
GND (2)

U37-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17 pF2_FF1_RECV0 / nF2_FF1_RECV0
		1P 1N	B18 B17 pF2_FF1_RECV1 / nF2_FF1_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14 pF2_FF1_RECV2 / nF2_FF1_RECV2
		3P 3N	B15 B14 pF2_FF1_RECV3 / nF2_FF1_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11 pF2_FF1_RECV4 / nF2_FF1_RECV4
		5P 5N	B12 B11 pF2_FF1_RECV5 / nF2_FF1_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8 pF2_FF1_RECV6 / nF2_FF1_RECV6
		7P 7N	B9 B8 pF2_FF1_RECV7 / nF2_FF1_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5 pF2_FF1_RECV8 / nF2_FF1_RECV8
		9P 9N	B6 B5 pF2_FF1_RECV9 / nF2_FF1_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2 pF2_FF1_RECV10 / nF2_FF1_RECV10
		11P 11N	B3 B2 pF2_FF1_RECV11 / nF2_FF1_RECV11
B1 A1	GND_B1 GND_A1		

GND; 1 G1 2 G2 VA68; VA67; VA66; VA65; VA64; VA63

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3

Title: 8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

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8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_R [19]
ac_nF2L_R0_R [19]
ac_pF2L_R1_R [21]
ac_nF2L_R1_R [21]

U78-28 FPGA_VU13P_A2577 — GTY QUAD 125 (Q)

	AP39	MGTREFCLK0P_125
	AP40	MGTREFCLK0N_125
	AN41	MGTREFCLK1P_125
	AN42	MGTREFCLK1N_125
pF2_FF2_RECV11	AU50	MGTYRXP0_125
nF2_FF2_RECV11	AU51	MGTYRXN0_125
pF2_FF2_XMIT11	AU45	MGTYTXP0_125
nF2_FF2_XMIT11	AU46	MGTYTXN0_125
pF2_FF2_RECV10	AT48	MGTYRXP1_125
nF2_FF2_RECV10	AT49	MGTYRXN1_125
pF2_FF2_XMIT10	AT43	MGTYTXP1_125
nF2_FF2_XMIT10	AT44	MGTYTXN1_125
pF2_FF2_RECV9	AR50	MGTYRXP2_125
nF2_FF2_RECV9	AR51	MGTYRXN2_125
pF2_FF2_XMIT9	AR45	MGTYTXP2_125
nF2_FF2_XMIT9	AR46	MGTYTXN2_125
pF2_FF2_RECV8	AP48	MGTYRXP3_125
nF2_FF2_RECV8	AP49	MGTYRXN3_125
pF2_FF2_XMIT8	AP43	MGTYTXP3_125
nF2_FF2_XMIT8	AP44	MGTYTXN3_125

U78-29 FPGA_VU13P_A2577 — GTY QUAD 126 (R)

	AM39	MGTREFCLK0P_126
	AM40	MGTREFCLK0N_126
	AL41	MGTREFCLK1P_126
	AL42	MGTREFCLK1N_126
pF2_FF2_RECV7	AN50	MGTYRXP0_126
nF2_FF2_RECV7	AN51	MGTYRXN0_126
pF2_FF2_XMIT7	AN45	MGTYTXP0_126
nF2_FF2_XMIT7	AN46	MGTYTXN0_126
pF2_FF2_RECV6	AM48	MGTYRXP1_126
nF2_FF2_RECV6	AM49	MGTYRXN1_126
pF2_FF2_XMIT6	AM43	MGTYTXP1_126
nF2_FF2_XMIT6	AM44	MGTYTXN1_126
pF2_FF2_RECV5	AL50	MGTYRXP2_126
nF2_FF2_RECV5	AL51	MGTYRXN2_126
pF2_FF2_XMIT5	AL45	MGTYTXP2_126
nF2_FF2_XMIT5	AL46	MGTYTXN2_126
pF2_FF2_RECV4	AK48	MGTYRXP3_126
nF2_FF2_RECV4	AK49	MGTYRXN3_126
pF2_FF2_XMIT4	AK43	MGTYTXP3_126
nF2_FF2_XMIT4	AK44	MGTYTXN3_126

U78-30 FPGA_VU13P_A2577 — GTY QUAD 127 (S)

	AJ41	MGTREFCLK0P_127
	AJ42	MGTREFCLK0N_127
	AG41	MGTREFCLK1P_127
	AG42	MGTREFCLK1N_127
pF2_FF2_RECV3	AJ50	MGTYRXP0_127
nF2_FF2_RECV3	AJ51	MGTYRXN0_127
pF2_FF2_XMIT3	AJ45	MGTYTXP0_127
nF2_FF2_XMIT3	AJ46	MGTYTXN0_127
pF2_FF2_RECV2	AH48	MGTYRXP1_127
nF2_FF2_RECV2	AH49	MGTYRXN1_127
pF2_FF2_XMIT2	AH43	MGTYTXP1_127
nF2_FF2_XMIT2	AH44	MGTYTXN1_127
pF2_FF2_RECV1	AG50	MGTYRXP2_127
nF2_FF2_RECV1	AG51	MGTYRXN2_127
pF2_FF2_XMIT1	AG45	MGTYTXP2_127
nF2_FF2_XMIT1	AG46	MGTYTXN2_127
pF2_FF2_RECV0	AF48	MGTYRXP3_127
nF2_FF2_RECV0	AF49	MGTYRXN3_127
pF2_FF2_XMIT0	AF43	MGTYTXP3_127
nF2_FF2_XMIT0	AF44	MGTYTXN3_127

U39-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F2_FF_RESET	[39,69,70,71,72,73,74]	6 /RESET (G1 G2)
I2C_SDA_F2_FF2_XMIT	[39]	7 SDA
I2C_SCL_F2_FF2_XMIT	[39]	8 SCL
		4 /SELECT (GND)
/F2_FF2_XMIT_INT	[39]	5 /INT
/F2_FF2_XMIT_PRESENT	[39]	3 /PRESENT
V_3V3		1 3.3V
V_F2_FF2_XMIT	[31]	10 3.8/3.3V (>=25G 3.8V, <=16G 3.3V)
		9 RSVD
		2 GND

V_M3V3 — R557 3.3K 0603; R558 3.3K 0603; R560 2.2K 0603; R559 2.2K 0603

V_3V3 — L34 1.0 UH 0806; C1101 22 UF 0603 6.3V; C1140 0.1 UF 0402; C1181 22 UF 0603 6.3V; C1226 0.1 UF 0402

V_F2_FF2_XMIT — L35 1.0 UH 0806; C1102 22 UF 0603 6.3V; C1141 0.1 UF 0402; C1182 22 UF 0603 6.3V; C1227 0.1 UF 0402

U39-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19	GND_B19	0P	pF2_FF2_XMIT0
A19	GND_A19	0N	nF2_FF2_XMIT0
		1P	pF2_FF2_XMIT1
B16	GND_B16	1N	nF2_FF2_XMIT1
A16	GND_A16	2P	pF2_FF2_XMIT2
		2N	nF2_FF2_XMIT2
B13	GND_B13	3P	pF2_FF2_XMIT3
A13	GND_A13	3N	nF2_FF2_XMIT3
		4P	pF2_FF2_XMIT4
B10	GND_B10	4N	nF2_FF2_XMIT4
A10	GND_A10	5P	pF2_FF2_XMIT5
		5N	nF2_FF2_XMIT5
B7	GND_B7	6P	pF2_FF2_XMIT6
A7	GND_A7	6N	nF2_FF2_XMIT6
		7P	pF2_FF2_XMIT7
B4	GND_B4	7N	nF2_FF2_XMIT7
A4	GND_A4	8P	pF2_FF2_XMIT8
		8N	nF2_FF2_XMIT8
B1	GND_B1	9P	pF2_FF2_XMIT9
A1	GND_A1	9N	nF2_FF2_XMIT9
		10P	pF2_FF2_XMIT10
		10N	nF2_FF2_XMIT10
		11P	pF2_FF2_XMIT11
		11N	nF2_FF2_XMIT11

GND — 1 G1 2 G2 VA78; VA77; VA76; VA75; VA74; VA73

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

V_M3V3 — R561 3.3K 0603; R562 3.3K 0603; R564 2.2K 0603; R563 2.2K 0603

U40-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F2_FF_RESET	[39,69,70,71,72,73,74]	6 /RESET (G1 G2)
I2C_SDA_F2_FF2_RECV	[39]	7 SDA
I2C_SCL_F2_FF2_RECV	[39]	8 SCL
		4 /SELECT (GND)
/F2_FF2_RECV_INT	[39]	5 /INT
/F2_FF2_RECV_PRESENT	[39]	3 /PRESENT
V_3V3		1 3.3V
		10 3.3V
		9 RSVD
		2 GND

V_3V3 — L36 1.0 UH 0806; C1116 22 UF 0603 6.3V; C1142 0.1 UF 0402; C1183 22 UF 0603 6.3V; C1228 0.1 UF 0402

L37 1.0 UH 0806; C1184 22 UF 0603 6.3V; C1229 0.1 UF 0402

U40-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19	GND_B19	0P	pF2_FF2_RECV0
A19	GND_A19	0N	nF2_FF2_RECV0
		1P	pF2_FF2_RECV1
B16	GND_B16	1N	nF2_FF2_RECV1
A16	GND_A16	2P	pF2_FF2_RECV2
		2N	nF2_FF2_RECV2
B13	GND_B13	3P	pF2_FF2_RECV3
A13	GND_A13	3N	nF2_FF2_RECV3
		4P	pF2_FF2_RECV4
B10	GND_B10	4N	nF2_FF2_RECV4
A10	GND_A10	5P	pF2_FF2_RECV5
		5N	nF2_FF2_RECV5
B7	GND_B7	6P	pF2_FF2_RECV6
A7	GND_A7	6N	nF2_FF2_RECV6
		7P	pF2_FF2_RECV7
B4	GND_B4	7N	nF2_FF2_RECV7
A4	GND_A4	8P	pF2_FF2_RECV8
		8N	nF2_FF2_RECV8
B1	GND_B1	9P	pF2_FF2_RECV9
A1	GND_A1	9N	nF2_FF2_RECV9
		10P	pF2_FF2_RECV10
		10N	nF2_FF2_RECV10
		11P	pF2_FF2_RECV11
		11N	nF2_FF2_RECV11

GND — 1 G1 2 G2 VA84; VA83; VA82; VA81; VA80; VA79

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3

Title: 8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

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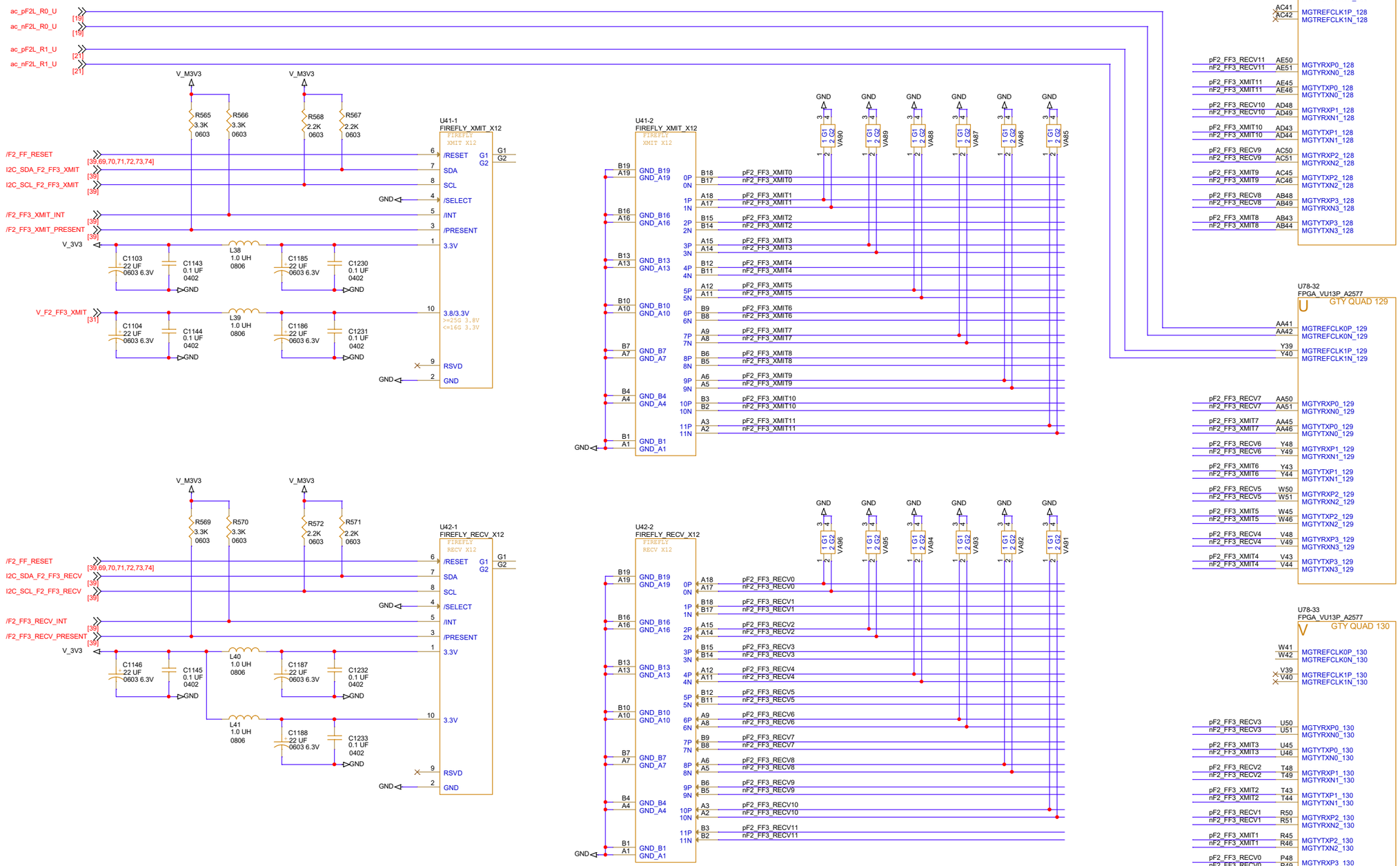
8.04: FPGA#2 FF#3 X12 ON QUADS T U V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

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Title	8.04: FPGA#2 FF#3 X12 ON QUADS T U V
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8.05: FPGA#2 FF#4 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_Y [19]
ac_nF2L_R0_Y [19]
ac_pF2L_R1_Y [21]
ac_nF2L_R1_Y [21]

U78-35 FPGA_VU13P_A2577 — X — GTY QUAD 132

R41 MGTREFCLK0P_132
R42 MGTREFCLK0N_132
P39 MGTREFCLK1P_132
P40 MGTREFCLK1N_132

pF2_FF4_RECV11 J50 — MGTYRXP0_132
nF2_FF4_RECV11 J51 — MGTYRXN0_132
pF2_FF4_XMIT11 J45 — MGTYTXP0_132
nF2_FF4_XMIT11 J46 — MGTYTXN0_132
pF2_FF4_RECV10 H48 — MGTYRXP1_132
nF2_FF4_RECV10 H49 — MGTYRXN1_132
pF2_FF4_XMIT10 H43 — MGTYTXP1_132
nF2_FF4_XMIT10 H44 — MGTYTXN1_132
pF2_FF4_RECV9 G50 — MGTYRXP2_132
nF2_FF4_RECV9 G51 — MGTYRXN2_132
pF2_FF4_XMIT9 G45 — MGTYTXP2_132
nF2_FF4_XMIT9 G46 — MGTYTXN2_132
pF2_FF4_RECV8 F48 — MGTYRXP3_132
nF2_FF4_RECV8 F49 — MGTYRXN3_132
pF2_FF4_XMIT8 F43 — MGTYTXP3_132
nF2_FF4_XMIT8 F44 — MGTYTXN3_132

U78-36 FPGA_VU13P_A2577 — Y — GTY QUAD 133

N41 MGTREFCLK0P_133
N42 MGTREFCLK0N_133
M39 MGTREFCLK1P_133
M40 MGTREFCLK1N_133

pF2_FF4_RECV7 E50 — MGTYRXP0_133
nF2_FF4_RECV7 E51 — MGTYRXN0_133
pF2_FF4_XMIT7 D43 — MGTYTXP0_133
nF2_FF4_XMIT7 D44 — MGTYTXN0_133
pF2_FF4_RECV6 D48 — MGTYRXP1_133
nF2_FF4_RECV6 D49 — MGTYRXN1_133
pF2_FF4_XMIT6 B43 — MGTYTXP1_133
nF2_FF4_XMIT6 B44 — MGTYTXN1_133
pF2_FF4_RECV5 E46 — MGTYRXP2_133
nF2_FF4_RECV5 E47 — MGTYRXN2_133
pF2_FF4_XMIT5 C41 — MGTYTXP2_133
nF2_FF4_XMIT5 C42 — MGTYTXN2_133
pF2_FF4_RECV4 C46 — MGTYRXP3_133
nF2_FF4_RECV4 C47 — MGTYRXN3_133
pF2_FF4_XMIT4 E41 — MGTYTXP3_133
nF2_FF4_XMIT4 E42 — MGTYTXN3_133

U78-37 FPGA_VU13P_A2577 — Z — GTY QUAD 134

L41 MGTREFCLK0P_134
L42 MGTREFCLK0N_134
K39 MGTREFCLK1P_134
K40 MGTREFCLK1N_134

pF2_FF4_RECV3 A46 — MGTYRXP0_134
nF2_FF4_RECV3 A47 — MGTYRXN0_134
pF2_FF4_XMIT3 A41 — MGTYTXP0_134
nF2_FF4_XMIT3 A42 — MGTYTXN0_134
pF2_FF4_RECV2 A32 — MGTYRXP1_134
nF2_FF4_RECV2 A33 — MGTYRXN1_134
pF2_FF4_XMIT2 B39 — MGTYTXP1_134
nF2_FF4_XMIT2 B40 — MGTYTXN1_134
pF2_FF4_RECV1 B34 — MGTYRXP2_134
nF2_FF4_RECV1 B35 — MGTYRXN2_134
pF2_FF4_XMIT1 A37 — MGTYTXP2_134
nF2_FF4_XMIT1 A38 — MGTYTXN2_134
pF2_FF4_RECV0 C32 — MGTYRXP3_134
nF2_FF4_RECV0 C33 — MGTYRXN3_134
pF2_FF4_XMIT0 C37 — MGTYTXP3_134
nF2_FF4_XMIT0 C38 — MGTYTXN3_134

V_M3V3
R577 3.3K 0603
R578 3.3K 0603
R580 2.2K 0603
R579 2.2K 0603

U44-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

/F2_FF_RESET
I2C_SDA_F2_FF4_XMIT [39,69,70,71,72,73,74]
I2C_SCL_F2_FF4_XMIT [39]
/F2_FF4_XMIT_INT [39]
/F2_FF4_XMIT_PRESENT [39]
V_3V3
V_F2_FF4_XMIT [31]

6 /RESET G1 G2
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.8/3.3V >=25G 3.8V <=16G 3.3V
9 RSVD
GND 2 GND

C1106 22 UF 0603 6.3V
C1149 0.1 UF 0402
L45 1.0 UH 0806
C1192 22 UF 0603 6.3V
C1236 0.1 UF 0402
C1107 22 UF 0603 6.3V
C1150 0.1 UF 0402
L46 1.0 UH 0806
C1193 22 UF 0603 6.3V
C1237 0.1 UF 0402

U44-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17 — pF2_FF4_XMIT0 nF2_FF4_XMIT0
		1P 1N	A18 A17 — pF2_FF4_XMIT1 nF2_FF4_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 B14 — pF2_FF4_XMIT2 nF2_FF4_XMIT2
		3P 3N	A15 A14 — pF2_FF4_XMIT3 nF2_FF4_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 B11 — pF2_FF4_XMIT4 nF2_FF4_XMIT4
		5P 5N	A12 A11 — pF2_FF4_XMIT5 nF2_FF4_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 B8 — pF2_FF4_XMIT6 nF2_FF4_XMIT6
		7P 7N	A9 A8 — pF2_FF4_XMIT7 nF2_FF4_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 B5 — pF2_FF4_XMIT8 nF2_FF4_XMIT8
		9P 9N	A6 A5 — pF2_FF4_XMIT9 nF2_FF4_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 B2 — pF2_FF4_XMIT10 nF2_FF4_XMIT10
		11P 11N	A3 A2 — pF2_FF4_XMIT11 nF2_FF4_XMIT11
B1 A1	GND_B1 GND_A1		

GND — 1 G1 2 G2 — VA106 VA105 VA104 VA103 VA102 VA101

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

V_M3V3
R581 3.3K 0603
R582 3.3K 0603
R584 2.2K 0603
R583 2.2K 0603

U45-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)

/F2_FF_RESET
I2C_SDA_F2_FF4_RECV [39,69,70,71,72,73,74]
I2C_SCL_F2_FF4_RECV [39]
/F2_FF4_RECV_INT [39]
/F2_FF4_RECV_PRESENT [39]
V_3V3

6 /RESET G1 G2
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 RSVD
GND 2 GND

C1118 22 UF 0603 6.3V
C1151 0.1 UF 0402
L47 1.0 UH 0806
C1194 22 UF 0603 6.3V
C1238 0.1 UF 0402
L48 1.0 UH 0806
C1195 22 UF 0603 6.3V
C1239 0.1 UF 0402

U45-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17 — pF2_FF4_RECV0 nF2_FF4_RECV0
		1P 1N	B18 B17 — pF2_FF4_RECV1 nF2_FF4_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14 — pF2_FF4_RECV2 nF2_FF4_RECV2
		3P 3N	B15 B14 — pF2_FF4_RECV3 nF2_FF4_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11 — pF2_FF4_RECV4 nF2_FF4_RECV4
		5P 5N	B12 B11 — pF2_FF4_RECV5 nF2_FF4_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8 — pF2_FF4_RECV6 nF2_FF4_RECV6
		7P 7N	B9 B8 — pF2_FF4_RECV7 nF2_FF4_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5 — pF2_FF4_RECV8 nF2_FF4_RECV8
		9P 9N	B6 B5 — pF2_FF4_RECV9 nF2_FF4_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2 — pF2_FF4_RECV10 nF2_FF4_RECV10
		11P 11N	B3 B2 — pF2_FF4_RECV11 nF2_FF4_RECV11
B1 A1	GND_B1 GND_A1		

GND — 1 G1 2 G2 — VA112 VA111 VA110 VA109 VA108 VA107

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3

Title: 8.05: FPGA#2 FF#4 X12 ON QUADS X Y Z

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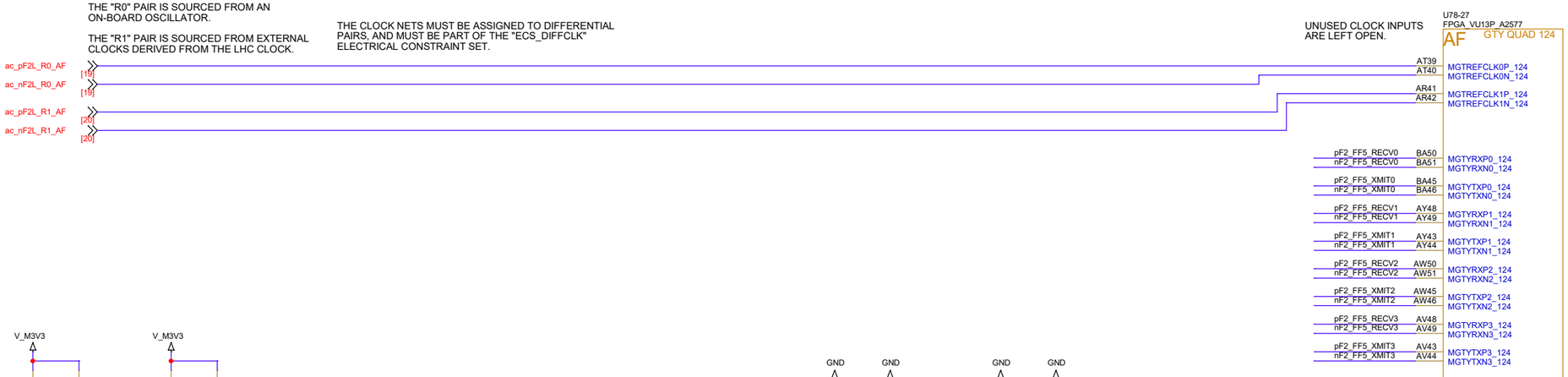
8.06: FPGA#2 FF#5 X4 ON QUAD AF

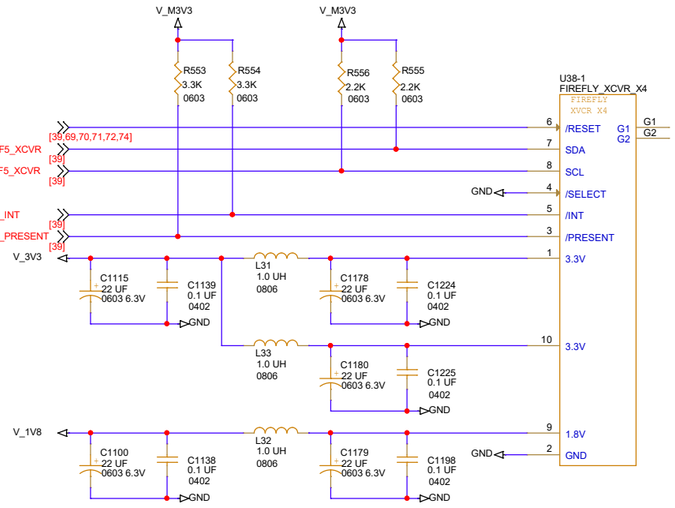
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

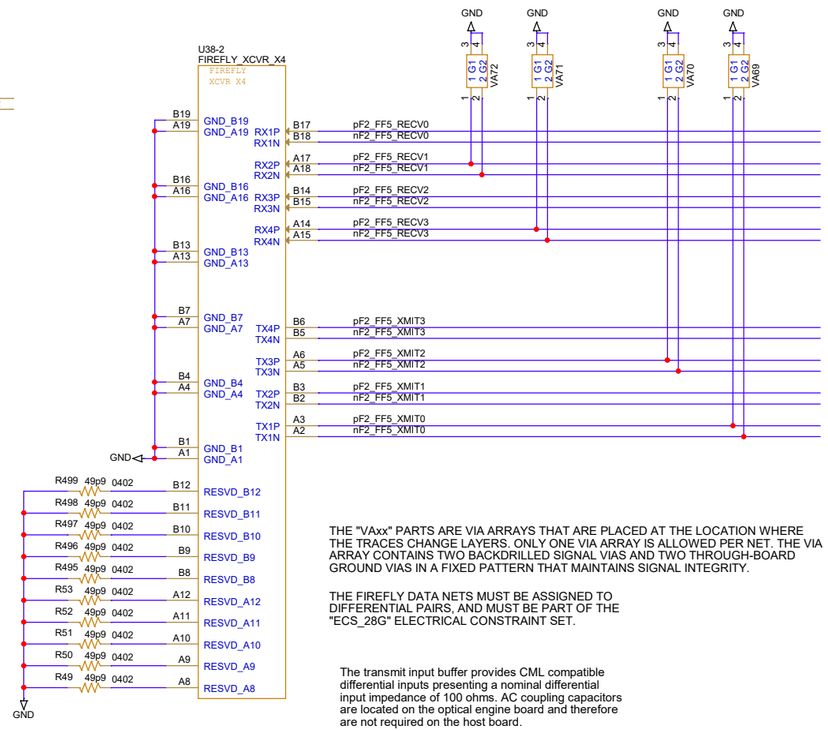
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM v3		
Title: 8.06: FPGA#2 FF#5 X4 ON QUAD AF		
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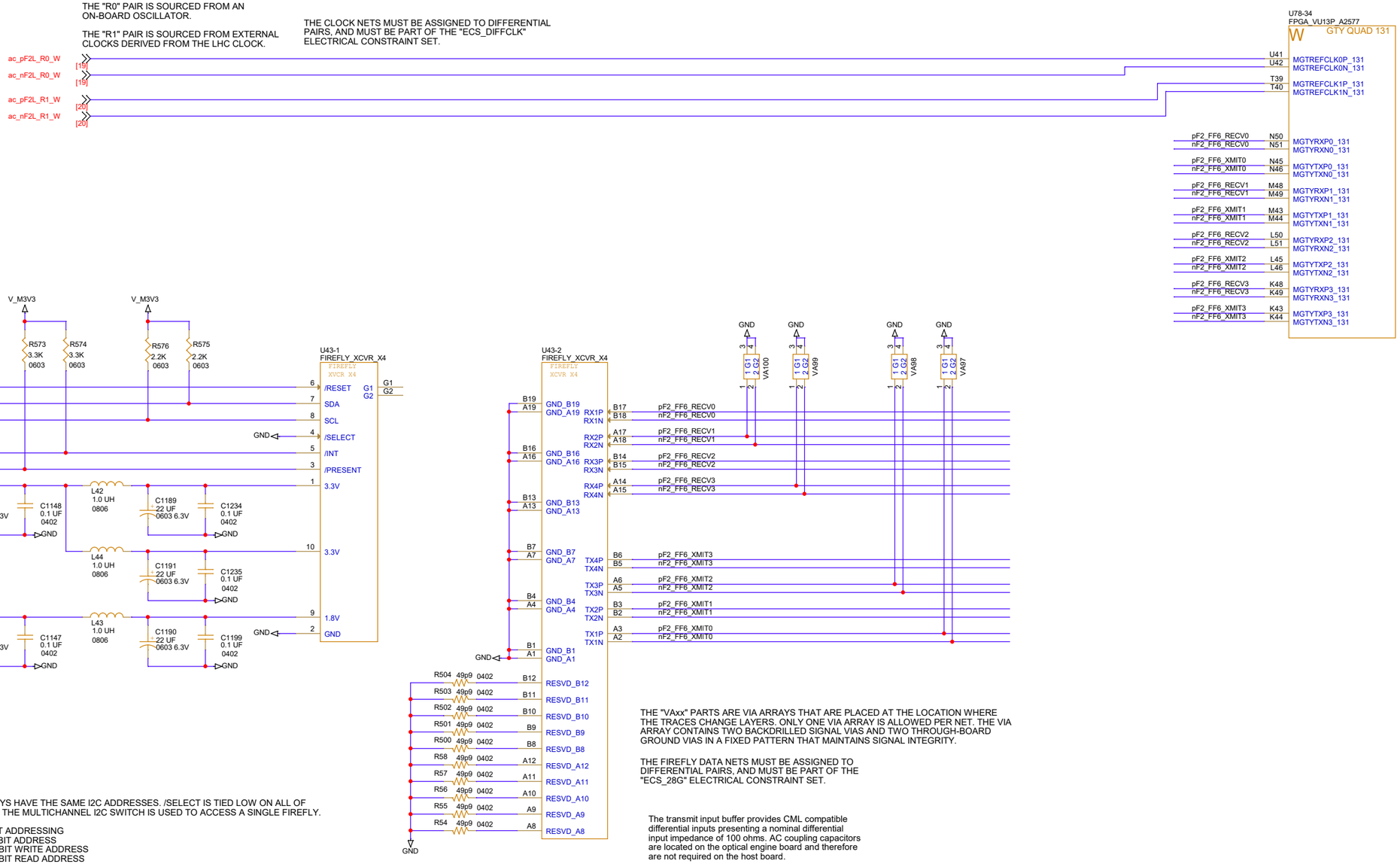
8.07: FPGA#2 FF#6 X4 ON QUAD W

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM v3

Title: 8.07: FPGA#2 FF#6 X4 ON QUAD W

Size | Document Number: 6089-127 | Rev: A

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8.08: FPGA#2 UNUSED QUADS K, AA

U78-54
FPGA_VU13P_A2577

K GTY QUAD 235

J11	MGTREFCLK0P_235
J10	MGTREFCLK0N_235
H13	MGTREFCLK1P_235
H12	MGTREFCLK1N_235
D18	MGTYRXP0_235
D17	MGTYRXN0_235
D13	MGTYTXP0_235
D12	MGTYTXN0_235
E20	MGTYRXP1_235
E19	MGTYRXN1_235
E15	MGTYTXP1_235
E14	MGTYTXN1_235
F18	MGTYRXP2_235
F17	MGTYRXN2_235
F13	MGTYTXP2_235
F12	MGTYTXN2_235
G20	MGTYRXP3_235
G19	MGTYRXN3_235
G15	MGTYTXP3_235
G14	MGTYTXN3_235

U78-38
FPGA_VU13P_A2577

AA GTY QUAD 135

J41	MGTREFCLK0P_135
J42	MGTREFCLK0N_135
H39	MGTREFCLK1P_135
H40	MGTREFCLK1N_135
D34	MGTYRXP0_135
D35	MGTYRXN0_135
D39	MGTYTXP0_135
D40	MGTYTXN0_135
E32	MGTYRXP1_135
E33	MGTYRXN1_135
E37	MGTYTXP1_135
E38	MGTYTXN1_135
F34	MGTYRXP2_135
F35	MGTYRXN2_135
F39	MGTYTXP2_135
F40	MGTYTXN2_135
G32	MGTYRXP3_135
G33	MGTYRXN3_135
G37	MGTYTXP3_135
G38	MGTYTXN3_135

APOLLO CM v3

Title
8.08: FPGA#2 UNUSED QUADS K, AA

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9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-40
FPGA_VU13P_A2577
GTY QUAD 221 — M

MGTREFCLK0P_221	BB13	
MGTREFCLK0N_221	BB12	
MGTREFCLK1P_221	BA11	
MGTREFCLK1N_221	BA10	
MGTYRXP0_221	BK18	pF1_M_RECV0
MGTYRXN0_221	BK17	nF1_M_RECV0
MGTYTXP0_221	BL15	pF1_M_XMIT0
MGTYTXN0_221	BL14	nF1_M_XMIT0
MGTYRXP1_221	BL20	pF1_M_RECV1
MGTYRXN1_221	BL19	nF1_M_RECV1
MGTYTXP1_221	BK13	pF1_M_XMIT1
MGTYTXN1_221	BK12	nF1_M_XMIT1
MGTYRXP2_221	BL6	pF1_M_RECV2
MGTYRXN2_221	BL5	nF1_M_RECV2
MGTYTXP2_221	BL11	pF1_M_XMIT2
MGTYTXN2_221	BL10	nF1_M_XMIT2
MGTYRXP3_221	BJ6	pF1_M_RECV3
MGTYRXN3_221	BJ5	nF1_M_RECV3
MGTYTXP3_221	BK9	pF1_M_XMIT3
MGTYTXN3_221	BK8	nF1_M_XMIT3

pF1_M_RECV0	C300	0.1 UF	0402	pF2_J_XMIT0
nF1_M_RECV0				nF2_J_XMIT0
	C299	0.1 UF	0402	
pF1_M_RECV1	C302	0.1 UF	0402	pF2_J_XMIT1
nF1_M_RECV1				nF2_J_XMIT1
	C301	0.1 UF	0402	
pF1_M_RECV2	C298	0.1 UF	0402	pF2_J_XMIT2
nF1_M_RECV2				nF2_J_XMIT2
	C297	0.1 UF	0402	
pF1_M_RECV3	C296	0.1 UF	0402	pF2_J_XMIT3
nF1_M_RECV3				nF2_J_XMIT3
	C315	0.1 UF	0402	

pF1_M_XMIT0	C310	0.1 UF	0402	pF2_J_RECV0
nF1_M_XMIT0				nF2_J_RECV0
	C309	0.1 UF	0402	
pF1_M_XMIT1	C308	0.1 UF	0402	pF2_J_RECV1
nF1_M_XMIT1				nF2_J_RECV1
	C307	0.1 UF	0402	
pF1_M_XMIT2	C306	0.1 UF	0402	pF2_J_RECV2
nF1_M_XMIT2				nF2_J_RECV2
	C305	0.1 UF	0402	
pF1_M_XMIT3	C304	0.1 UF	0402	pF2_J_RECV3
nF1_M_XMIT3				nF2_J_RECV3
	C303	0.1 UF	0402	

U77-41
FPGA_VU13P_A2577
GTY QUAD 222 — N

MGTREFCLK0P_222	AY13	ac_pF1R_R0_N [19]
MGTREFCLK0N_222	AY12	ac_nF1R_R0_N [19]
MGTREFCLK1P_222	AW11	ac_pF1R_R1_N [22]
MGTREFCLK1N_222	AW10	ac_nF1R_R1_N [22]
MGTYRXP0_222	BH4	pF1_N_RECV0
MGTYRXN0_222	BH3	nF1_N_RECV0
MGTYTXP0_222	BG11	pF1_N_XMIT0
MGTYTXN0_222	BG10	nF1_N_XMIT0
MGTYRXP1_222	BG2	pF1_N_RECV1
MGTYRXN1_222	BG1	nF1_N_RECV1
MGTYTXP1_222	BJ11	pF1_N_XMIT1
MGTYTXN1_222	BJ10	nF1_N_XMIT1
MGTYRXP2_222	BG6	pF1_N_RECV2
MGTYRXN2_222	BG5	nF1_N_RECV2
MGTYTXP2_222	BH9	pF1_N_XMIT2
MGTYTXN2_222	BH8	nF1_N_XMIT2
MGTYRXP3_222	BF4	pF1_N_RECV3
MGTYRXN3_222	BF3	nF1_N_RECV3
MGTYTXP3_222	BF9	pF1_N_XMIT3
MGTYTXN3_222	BF8	nF1_N_XMIT3

pF1_N_RECV0	C286	0.1 UF	0402	pF2_I_XMIT0
nF1_N_RECV0				nF2_I_XMIT0
	C285	0.1 UF	0402	
pF1_N_RECV1	C282	0.1 UF	0402	pF2_I_XMIT1
nF1_N_RECV1				nF2_I_XMIT1
	C281	0.1 UF	0402	
pF1_N_RECV2	C284	0.1 UF	0402	pF2_I_XMIT2
nF1_N_RECV2				nF2_I_XMIT2
	C283	0.1 UF	0402	
pF1_N_RECV3	C280	0.1 UF	0402	pF2_I_XMIT3
nF1_N_RECV3				nF2_I_XMIT3
	C279	0.1 UF	0402	

pF1_N_XMIT0	C290	0.1 UF	0402	pF2_I_RECV0
nF1_N_XMIT0				nF2_I_RECV0
	C289	0.1 UF	0402	
pF1_N_XMIT1	C294	0.1 UF	0402	pF2_I_RECV1
nF1_N_XMIT1				nF2_I_RECV1
	C293	0.1 UF	0402	
pF1_N_XMIT2	C292	0.1 UF	0402	pF2_I_RECV2
nF1_N_XMIT2				nF2_I_RECV2
	C291	0.1 UF	0402	
pF1_N_XMIT3	C288	0.1 UF	0402	pF2_I_RECV3
nF1_N_XMIT3				nF2_I_RECV3
	C287	0.1 UF	0402	

U77-42
FPGA_VU13P_A2577
GTY QUAD 223 — O

MGTREFCLK0P_223	AV13	
MGTREFCLK0N_223	AV12	
MGTREFCLK1P_223	AU11	
MGTREFCLK1N_223	AU10	
MGTYRXP0_223	BE2	pF1_O_RECV0
MGTYRXN0_223	BE1	nF1_O_RECV0
MGTYTXP0_223	BE7	pF1_O_XMIT0
MGTYTXN0_223	BE6	nF1_O_XMIT0
MGTYRXP1_223	BD4	pF1_O_RECV1
MGTYRXN1_223	BD3	nF1_O_RECV1
MGTYTXP1_223	BD9	pF1_O_XMIT1
MGTYTXN1_223	BD8	nF1_O_XMIT1
MGTYRXP2_223	BC2	pF1_O_RECV2
MGTYRXN2_223	BC1	nF1_O_RECV2
MGTYTXP2_223	BC7	pF1_O_XMIT2
MGTYTXN2_223	BC6	nF1_O_XMIT2
MGTYRXP3_223	BB4	pF1_O_RECV3
MGTYRXN3_223	BB3	nF1_O_RECV3
MGTYTXP3_223	BB9	pF1_O_XMIT3
MGTYTXN3_223	BB8	nF1_O_XMIT3

pF1_O_RECV0	C266	0.1 UF	0402	pF2_H_XMIT0
nF1_O_RECV0				nF2_H_XMIT0
	C265	0.1 UF	0402	
pF1_O_RECV1	C264	0.1 UF	0402	pF2_H_XMIT1
nF1_O_RECV1				nF2_H_XMIT1
	C263	0.1 UF	0402	
pF1_O_RECV2	C262	0.1 UF	0402	pF2_H_XMIT2
nF1_O_RECV2				nF2_H_XMIT2
	C261	0.1 UF	0402	
pF1_O_RECV3	C260	0.1 UF	0402	pF2_H_XMIT3
nF1_O_RECV3				nF2_H_XMIT3
	C259	0.1 UF	0402	

pF1_O_XMIT0	C274	0.1 UF	0402	pF2_H_RECV0
nF1_O_XMIT0				nF2_H_RECV0
	C273	0.1 UF	0402	
pF1_O_XMIT1	C272	0.1 UF	0402	pF2_H_RECV1
nF1_O_XMIT1				nF2_H_RECV1
	C271	0.1 UF	0402	
pF1_O_XMIT2	C270	0.1 UF	0402	pF2_H_RECV2
nF1_O_XMIT2				nF2_H_RECV2
	C269	0.1 UF	0402	
pF1_O_XMIT3	C268	0.1 UF	0402	pF2_H_RECV3
nF1_O_XMIT3				nF2_H_RECV3
	C267	0.1 UF	0402	

FPGA#2

U78-53
FPGA_VU13P_A2577
GTY QUAD 234 — J

MGTREFCLK0P_234	L11	
MGTREFCLK0N_234	L10	
MGTREFCLK1P_234	K13	
MGTREFCLK1N_234	K12	
MGTYRXP0_234	A6	pF2_J_RECV3
MGTYRXN0_234	A5	nF2_J_RECV3
MGTYTXP0_234	A11	pF2_J_XMIT3
MGTYTXN0_234	A10	nF2_J_XMIT3
MGTYRXP1_234	A20	pF2_J_RECV2
MGTYRXN1_234	A19	nF2_J_RECV2
MGTYTXP1_234	B13	pF2_J_XMIT2
MGTYTXN1_234	B12	nF2_J_XMIT2
MGTYRXP2_234	B18	pF2_J_RECV1
MGTYRXN2_234	B17	nF2_J_RECV1
MGTYTXP2_234	A15	pF2_J_XMIT1
MGTYTXN2_234	A14	nF2_J_XMIT1
MGTYRXP3_234	C20	pF2_J_RECV0
MGTYRXN3_234	C19	nF2_J_RECV0
MGTYTXP3_234	C15	pF2_J_XMIT0
MGTYTXN3_234	C14	nF2_J_XMIT0

U78-52
FPGA_VU13P_A2577
GTY QUAD 233 — I

ac_pF2R_R0_I	[19]	
ac_nF2R_R0_I	[19]	N11
		N10
ac_pF2R_R1_I	[22]	M13
ac_nF2R_R1_I	[22]	M12
MGTREFCLK0P_233		
MGTREFCLK0N_233		
MGTREFCLK1P_233		
MGTREFCLK1N_233		
MGTYRXP0_233	E2	pF2_I_RECV3
MGTYRXN0_233	E1	nF2_I_RECV3
MGTYTXP0_233	D9	pF2_I_XMIT3
MGTYTXN0_233	D8	nF2_I_XMIT3
MGTYRXP1_233	D4	pF2_I_RECV2
MGTYRXN1_233	D3	nF2_I_RECV2
MGTYTXP1_233	B9	pF2_I_XMIT2
MGTYTXN1_233	B8	nF2_I_XMIT2
MGTYRXP2_233	E6	pF2_I_RECV1
MGTYRXN2_233	E5	nF2_I_RECV1
MGTYTXP2_233	C11	pF2_I_XMIT1
MGTYTXN2_233	C10	nF2_I_XMIT1
MGTYRXP3_233	C6	pF2_I_RECV0
MGTYRXN3_233	C5	nF2_I_RECV0
MGTYTXP3_233	E11	pF2_I_XMIT0
MGTYTXN3_233	E10	nF2_I_XMIT0

U78-51
FPGA_VU13P_A2577
GTY QUAD 232 — H

MGTREFCLK0P_232	R11	
MGTREFCLK0N_232	R10	
MGTREFCLK1P_232	P13	
MGTREFCLK1N_232	P12	
MGTYRXP0_232	J2	pF2_H_RECV3
MGTYRXN0_232	J1	nF2_H_RECV3
MGTYTXP0_232	J7	pF2_H_XMIT3
MGTYTXN0_232	J6	nF2_H_XMIT3
MGTYRXP1_232	H4	pF2_H_RECV2
MGTYRXN1_232	H3	nF2_H_RECV2
MGTYTXP1_232	H9	pF2_H_XMIT2
MGTYTXN1_232	H8	nF2_H_XMIT2
MGTYRXP2_232	G2	pF2_H_RECV1
MGTYRXN2_232	G1	nF2_H_RECV1
MGTYTXP2_232	G7	pF2_H_XMIT1
MGTYTXN2_232	G6	nF2_H_XMIT1
MGTYRXP3_232	F4	pF2_H_RECV0
MGTYRXN3_232	F3	nF2_H_RECV0
MGTYTXP3_232	F9	pF2_H_XMIT0
MGTYTXN3_232	F8	nF2_H_XMIT0

APOLLO CM v3			
Title: 9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H			
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9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-44
FPGA_VU13P_A2577
GTY QUAD 225 A

MGTREFCLK0P_225	AP13		
MGTREFCLK0N_225	AP12		
MGTREFCLK1P_225	AN11		
MGTREFCLK1N_225	AN10		
MGTYRXP0_225	AU2	pF1_A_RECV0	pF2_F_XMIT0
MGTYRXN0_225	AU1	nF1_A_RECV0	nF2_F_XMIT0
MGTYTXP0_225	AU7	pF1_A_XMIT0	pF2_F_RECV0
MGTYTXN0_225	AU6	nF1_A_XMIT0	nF2_F_RECV0
MGTYRXP1_225	AT4	pF1_A_RECV1	pF2_F_XMIT1
MGTYRXN1_225	AT3	nF1_A_RECV1	nF2_F_XMIT1
MGTYTXP1_225	AT9	pF1_A_XMIT1	pF2_F_RECV1
MGTYTXN1_225	AT8	nF1_A_XMIT1	nF2_F_RECV1
MGTYRXP2_225	AR2	pF1_A_RECV2	pF2_F_XMIT2
MGTYRXN2_225	AR1	nF1_A_RECV2	nF2_F_XMIT2
MGTYTXP2_225	AR7	pF1_A_XMIT2	pF2_F_RECV2
MGTYTXN2_225	AR6	nF1_A_XMIT2	nF2_F_RECV2
MGTYRXP3_225	AP4	pF1_A_RECV3	pF2_F_XMIT3
MGTYRXN3_225	AP3	nF1_A_RECV3	nF2_F_XMIT3
MGTYTXP3_225	AP9	pF1_A_XMIT3	pF2_F_RECV3
MGTYTXN3_225	AP8	nF1_A_XMIT3	nF2_F_RECV3

pF1_A_RECV0	C224 0.1 UF 0402	pF2_F_XMIT0	
nF1_A_RECV0		nF2_F_XMIT0	
	C223 0.1 UF 0402		
pF1_A_RECV1	C222 0.1 UF 0402	pF2_F_XMIT1	
nF1_A_RECV1		nF2_F_XMIT1	
	C221 0.1 UF 0402		
pF1_A_RECV2	C220 0.1 UF 0402	pF2_F_XMIT2	
nF1_A_RECV2		nF2_F_XMIT2	
	C219 0.1 UF 0402		
pF1_A_RECV3	C218 0.1 UF 0402	pF2_F_XMIT3	
nF1_A_RECV3		nF2_F_XMIT3	
	C217 0.1 UF 0402		

pF1_A_XMIT0	C232 0.1 UF 0402	pF2_F_RECV0	
nF1_A_XMIT0		nF2_F_RECV0	
	C231 0.1 UF 0402		
pF1_A_XMIT1	C230 0.1 UF 0402	pF2_F_RECV1	
nF1_A_XMIT1		nF2_F_RECV1	
	C229 0.1 UF 0402		
pF1_A_XMIT2	C234 0.1 UF 0402	pF2_F_RECV2	
nF1_A_XMIT2		nF2_F_RECV2	
	C233 0.1 UF 0402		
pF1_A_XMIT3	C226 0.1 UF 0402	pF2_F_RECV3	
nF1_A_XMIT3		nF2_F_RECV3	
	C225 0.1 UF 0402		

FPGA#2

U78-49
FPGA_VU13P_A2577
GTY QUAD 230 F

MGTREFCLK0P_230	W11		
MGTREFCLK0N_230	W10		
MGTREFCLK1P_230	V13		
MGTREFCLK1N_230	V12		
MGTYRXP0_230	U2	pF2_F_RECV3	
MGTYRXN0_230	U1	nF2_F_RECV3	
MGTYTXP0_230	U7	pF2_F_XMIT3	
MGTYTXN0_230	U6	nF2_F_XMIT3	
MGTYRXP1_230	T4	pF2_F_RECV2	
MGTYRXN1_230	T3	nF2_F_RECV2	
MGTYTXP1_230	T9	pF2_F_XMIT2	
MGTYTXN1_230	T8	nF2_F_XMIT2	
MGTYRXP2_230	R2	pF2_F_RECV1	
MGTYRXN2_230	R1	nF2_F_RECV1	
MGTYTXP2_230	R7	pF2_F_XMIT1	
MGTYTXN2_230	R6	nF2_F_XMIT1	
MGTYRXP3_230	P4	pF2_F_RECV0	
MGTYRXN3_230	P3	nF2_F_RECV0	
MGTYTXP3_230	P9	pF2_F_XMIT0	
MGTYTXN3_230	P8	nF2_F_XMIT0	

U77-45
FPGA_VU13P_A2577
GTY QUAD 226 B

MGTREFCLK0P_226	AM13	ac_pF1R_R0_B [19]	
MGTREFCLK0N_226	AM12	ac_nF1R_R0_B [19]	
MGTREFCLK1P_226	AL11	ac_pF1R_R1_B [22]	
MGTREFCLK1N_226	AL10	ac_nF1R_R1_B [22]	
MGTYRXP0_226	AN2	pF1_B_RECV0	pF2_E_XMIT0
MGTYRXN0_226	AN1	nF1_B_RECV0	nF2_E_XMIT0
MGTYTXP0_226	AN7	pF1_B_XMIT0	pF2_E_RECV0
MGTYTXN0_226	AN6	nF1_B_XMIT0	nF2_E_RECV0
MGTYRXP1_226	AM4	pF1_B_RECV1	pF2_E_XMIT1
MGTYRXN1_226	AM3	nF1_B_RECV1	nF2_E_XMIT1
MGTYTXP1_226	AM9	pF1_B_XMIT1	pF2_E_RECV1
MGTYTXN1_226	AM8	nF1_B_XMIT1	nF2_E_RECV1
MGTYRXP2_226	AL2	pF1_B_RECV2	pF2_E_XMIT2
MGTYRXN2_226	AL1	nF1_B_RECV2	nF2_E_XMIT2
MGTYTXP2_226	AL7	pF1_B_XMIT2	pF2_E_RECV2
MGTYTXN2_226	AL6	nF1_B_XMIT2	nF2_E_RECV2
MGTYRXP3_226	AK4	pF1_B_RECV3	pF2_E_XMIT3
MGTYRXN3_226	AK3	nF1_B_RECV3	nF2_E_XMIT3
MGTYTXP3_226	AK9	pF1_B_XMIT3	pF2_E_RECV3
MGTYTXN3_226	AK8	nF1_B_XMIT3	nF2_E_RECV3

pF1_B_RECV0	C208 0.1 UF 0402	pF2_E_XMIT0	
nF1_B_RECV0		nF2_E_XMIT0	
	C207 0.1 UF 0402		
pF1_B_RECV1	C206 0.1 UF 0402	pF2_E_XMIT1	
nF1_B_RECV1		nF2_E_XMIT1	
	C205 0.1 UF 0402		
pF1_B_RECV2	C204 0.1 UF 0402	pF2_E_XMIT2	
nF1_B_RECV2		nF2_E_XMIT2	
	C203 0.1 UF 0402		
pF1_B_RECV3	C202 0.1 UF 0402	pF2_E_XMIT3	
nF1_B_RECV3		nF2_E_XMIT3	
	C201 0.1 UF 0402		

pF1_B_XMIT0	C216 0.1 UF 0402	pF2_E_RECV0	
nF1_B_XMIT0		nF2_E_RECV0	
	C215 0.1 UF 0402		
pF1_B_XMIT1	C214 0.1 UF 0402	pF2_E_RECV1	
nF1_B_XMIT1		nF2_E_RECV1	
	C213 0.1 UF 0402		
pF1_B_XMIT2	C212 0.1 UF 0402	pF2_E_RECV2	
nF1_B_XMIT2		nF2_E_RECV2	
	C211 0.1 UF 0402		
pF1_B_XMIT3	C210 0.1 UF 0402	pF2_E_RECV3	
nF1_B_XMIT3		nF2_E_RECV3	
	C209 0.1 UF 0402		

U78-48
FPGA_VU13P_A2577
GTY QUAD 229 E

ac_pF2R_R0_E	[19]		
ac_nF2R_R0_E	[19]	AA11	
ac_pF2R_R1_E	[22]	Y13	
ac_nF2R_R1_E	[22]	Y12	
MGTREFCLK0P_229	AA11		
MGTREFCLK0N_229	AA10		
MGTREFCLK1P_229	Y13		
MGTREFCLK1N_229	Y12		
MGTYRXP0_229	AA2	pF2_E_RECV3	
MGTYRXN0_229	AA1	nF2_E_RECV3	
MGTYTXP0_229	AA7	pF2_E_XMIT3	
MGTYTXN0_229	AA6	nF2_E_XMIT3	
MGTYRXP1_229	Y4	pF2_E_RECV2	
MGTYRXN1_229	Y3	nF2_E_RECV2	
MGTYTXP1_229	Y9	pF2_E_XMIT2	
MGTYTXN1_229	Y8	nF2_E_XMIT2	
MGTYRXP2_229	W2	pF2_E_RECV1	
MGTYRXN2_229	W1	nF2_E_RECV1	
MGTYTXP2_229	W7	pF2_E_XMIT1	
MGTYTXN2_229	W6	nF2_E_XMIT1	
MGTYRXP3_229	V4	pF2_E_RECV0	
MGTYRXN3_229	V3	nF2_E_RECV0	
MGTYTXP3_229	V9	pF2_E_XMIT0	
MGTYTXN3_229	V8	nF2_E_XMIT0	

U77-46
FPGA_VU13P_A2577
GTY QUAD 227 C

MGTREFCLK0P_227	AJ11		
MGTREFCLK0N_227	AJ10		
MGTREFCLK1P_227	AG11		
MGTREFCLK1N_227	AG10		
MGTYRXP0_227	AJ2	pF1_C_RECV0	pF2_D_XMIT0
MGTYRXN0_227	AJ1	nF1_C_RECV0	nF2_D_XMIT0
MGTYTXP0_227	AJ7	pF1_C_XMIT0	pF2_D_RECV0
MGTYTXN0_227	AJ6	nF1_C_XMIT0	nF2_D_RECV0
MGTYRXP1_227	AH4	pF1_C_RECV1	pF2_D_XMIT1
MGTYRXN1_227	AH3	nF1_C_RECV1	nF2_D_XMIT1
MGTYTXP1_227	AH9	pF1_C_XMIT1	pF2_D_RECV1
MGTYTXN1_227	AH8	nF1_C_XMIT1	nF2_D_RECV1
MGTYRXP2_227	AG2	pF1_C_RECV2	pF2_D_XMIT2
MGTYRXN2_227	AG1	nF1_C_RECV2	nF2_D_XMIT2
MGTYTXP2_227	AG7	pF1_C_XMIT2	pF2_D_RECV2
MGTYTXN2_227	AG6	nF1_C_XMIT2	nF2_D_RECV2
MGTYRXP3_227	AF4	pF1_C_RECV3	pF2_D_XMIT3
MGTYRXN3_227	AF3	nF1_C_RECV3	nF2_D_XMIT3
MGTYTXP3_227	AF9	pF1_C_XMIT3	pF2_D_RECV3
MGTYTXN3_227	AF8	nF1_C_XMIT3	nF2_D_RECV3

pF1_C_RECV0	C188 0.1 UF 0402	pF2_D_XMIT0	
nF1_C_RECV0		nF2_D_XMIT0	
	C187 0.1 UF 0402		
pF1_C_RECV1	C186 0.1 UF 0402	pF2_D_XMIT1	
nF1_C_RECV1		nF2_D_XMIT1	
	C185 0.1 UF 0402		
pF1_C_RECV2	C184 0.1 UF 0402	pF2_D_XMIT2	
nF1_C_RECV2		nF2_D_XMIT2	
	C183 0.1 UF 0402		
pF1_C_RECV3	C182 0.1 UF 0402	pF2_D_XMIT3	
nF1_C_RECV3		nF2_D_XMIT3	
	C181 0.1 UF 0402		

pF1_C_XMIT0	C196 0.1 UF 0402	pF2_D_RECV0	
nF1_C_XMIT0		nF2_D_RECV0	
	C195 0.1 UF 0402		
pF1_C_XMIT1	C194 0.1 UF 0402	pF2_D_RECV1	
nF1_C_XMIT1		nF2_D_RECV1	
	C193 0.1 UF 0402		
pF1_C_XMIT2	C192 0.1 UF 0402	pF2_D_RECV2	
nF1_C_XMIT2		nF2_D_RECV2	
	C191 0.1 UF 0402		
pF1_C_XMIT3	C190 0.1 UF 0402	pF2_D_RECV3	
nF1_C_XMIT3		nF2_D_RECV3	
	C189 0.1 UF 0402		

U78-47
FPGA_VU13P_A2577
GTY QUAD 228 D

MGTREFCLK0P_228	AE11		
MGTREFCLK0N_228	AE10		
MGTREFCLK1P_228	AC11		
MGTREFCLK1N_228	AC10		
MGTYRXP0_228	AE2	pF2_D_RECV3	
MGTYRXN0_228	AE1	nF2_D_RECV3	
MGTYTXP0_228	AE7	pF2_D_XMIT3	
MGTYTXN0_228	AE6	nF2_D_XMIT3	
MGTYRXP1_228	AD4	pF2_D_RECV2	
MGTYRXN1_228	AD3	nF2_D_RECV2	
MGTYTXP1_228	AD9	pF2_D_XMIT2	
MGTYTXN1_228	AD8	nF2_D_XMIT2	
MGTYRXP2_228	AC2	pF2_D_RECV1	
MGTYRXN2_228	AC1	nF2_D_RECV1	
MGTYTXP2_228	AC7	pF2_D_XMIT1	
MGTYTXN2_228	AC6	nF2_D_XMIT1	
MGTYRXP3_228	AB4	pF2_D_RECV0	
MGTYRXN3_228	AB3	nF2_D_RECV0	
MGTYTXP3_228	AB9	pF2_D_XMIT0	
MGTYTXN3_228	AB8	nF2_D_XMIT0	

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Title: 9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

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9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-51
FPGA_VU13P_A2577
GTY QUAD 232 H

MGTREFCLK0P_232	R11		
MGTREFCLK0N_232	R10		
MGTREFCLK1P_232	P13		
MGTREFCLK1N_232	P12		
MGTYRXP0_232	J2	pF1_H_RECV0	pF1_H_RECV0 → C91 0.1 UF 0402 → pF2_O_XMIT0
MGTYRXN0_232	J1	nF1_H_RECV0	nF1_H_RECV0 → C91 0.1 UF 0402 → nF2_O_XMIT0
MGTYTXP0_232	J7	pF1_H_XMIT0	pF1_H_XMIT0 → C99 0.1 UF 0402 → pF2_O_RECV0
MGTYTXN0_232	J6	nF1_H_XMIT0	nF1_H_XMIT0 → C99 0.1 UF 0402 → nF2_O_RECV0
MGTYRXP1_232	H4	pF1_H_RECV1	pF1_H_RECV1 → C89 0.1 UF 0402 → pF2_O_XMIT1
MGTYRXN1_232	H3	nF1_H_RECV1	nF1_H_RECV1 → C89 0.1 UF 0402 → nF2_O_XMIT1
MGTYTXP1_232	H9	pF1_H_XMIT1	pF1_H_XMIT1 → C97 0.1 UF 0402 → pF2_O_RECV1
MGTYTXN1_232	H8	nF1_H_XMIT1	nF1_H_XMIT1 → C97 0.1 UF 0402 → nF2_O_RECV1
MGTYRXP2_232	G2	pF1_H_RECV2	pF1_H_RECV2 → C87 0.1 UF 0402 → pF2_O_XMIT2
MGTYRXN2_232	G1	nF1_H_RECV2	nF1_H_RECV2 → C87 0.1 UF 0402 → nF2_O_XMIT2
MGTYTXP2_232	G7	pF1_H_XMIT2	pF1_H_XMIT2 → C101 0.1 UF 0402 → pF2_O_RECV2
MGTYTXN2_232	G6	nF1_H_XMIT2	nF1_H_XMIT2 → C101 0.1 UF 0402 → nF2_O_RECV2
MGTYRXP3_232	F4	pF1_H_RECV3	pF1_H_RECV3 → C85 0.1 UF 0402 → pF2_O_XMIT3
MGTYRXN3_232	F3	nF1_H_RECV3	nF1_H_RECV3 → C85 0.1 UF 0402 → nF2_O_XMIT3
MGTYTXP3_232	F9	pF1_H_XMIT3	pF1_H_XMIT3 → C93 0.1 UF 0402 → pF2_O_RECV3
MGTYTXN3_232	F8	nF1_H_XMIT3	nF1_H_XMIT3 → C93 0.1 UF 0402 → nF2_O_RECV3

C84 0.1 UF 0402
C92 0.1 UF 0402

U77-52
FPGA_VU13P_A2577
GTY QUAD 233 I

MGTREFCLK0P_233	N11	ac_pF1R_R0_I [19]	
MGTREFCLK0N_233	N10	ac_nF1R_R0_I [19]	
MGTREFCLK1P_233	M13	ac_pF1R_R1_I [22]	
MGTREFCLK1N_233	M12	ac_nF1R_R1_I [22]	
MGTYRXP0_233	E2	pF1_I_RECV0	pF1_I_RECV0 → C71 0.1 UF 0402 → pF2_N_XMIT0
MGTYRXN0_233	E1	nF1_I_RECV0	nF1_I_RECV0 → C71 0.1 UF 0402 → nF2_N_XMIT0
MGTYTXP0_233	D9	pF1_I_XMIT0	pF1_I_XMIT0 → C79 0.1 UF 0402 → pF2_N_RECV0
MGTYTXN0_233	D8	nF1_I_XMIT0	nF1_I_XMIT0 → C79 0.1 UF 0402 → nF2_N_RECV0
MGTYRXP1_233	D4	pF1_I_RECV1	pF1_I_RECV1 → C69 0.1 UF 0402 → pF2_N_XMIT1
MGTYRXN1_233	D3	nF1_I_RECV1	nF1_I_RECV1 → C69 0.1 UF 0402 → nF2_N_XMIT1
MGTYTXP1_233	B9	pF1_I_XMIT1	pF1_I_XMIT1 → C77 0.1 UF 0402 → pF2_N_RECV1
MGTYTXN1_233	B8	nF1_I_XMIT1	nF1_I_XMIT1 → C77 0.1 UF 0402 → nF2_N_RECV1
MGTYRXP2_233	E6	pF1_I_RECV2	pF1_I_RECV2 → C64 0.1 UF 0402 → pF2_N_XMIT2
MGTYRXN2_233	E5	nF1_I_RECV2	nF1_I_RECV2 → C64 0.1 UF 0402 → nF2_N_XMIT2
MGTYTXP2_233	C11	pF1_I_XMIT2	pF1_I_XMIT2 → C74 0.1 UF 0402 → pF2_N_RECV2
MGTYTXN2_233	C10	nF1_I_XMIT2	nF1_I_XMIT2 → C74 0.1 UF 0402 → nF2_N_RECV2
MGTYRXP3_233	C6	pF1_I_RECV3	pF1_I_RECV3 → C66 0.1 UF 0402 → pF2_N_XMIT3
MGTYRXN3_233	C5	nF1_I_RECV3	nF1_I_RECV3 → C66 0.1 UF 0402 → nF2_N_XMIT3
MGTYTXP3_233	E11	pF1_I_XMIT3	pF1_I_XMIT3 → C72 0.1 UF 0402 → pF2_N_RECV3
MGTYTXN3_233	E10	nF1_I_XMIT3	nF1_I_XMIT3 → C72 0.1 UF 0402 → nF2_N_RECV3

C68 0.1 UF 0402
C65 0.1 UF 0402
C67 0.1 UF 0402
C76 0.1 UF 0402
C78 0.1 UF 0402
C75 0.1 UF 0402
C73 0.1 UF 0402

U77-53
FPGA_VU13P_A2577
GTY QUAD 234 J

MGTREFCLK0P_234	L11		
MGTREFCLK0N_234	L10		
MGTREFCLK1P_234	K13		
MGTREFCLK1N_234	K12		
MGTYRXP0_234	A6	pF1_J_RECV0	pF1_J_RECV0 → C54 0.1 UF 0402 → pF2_M_XMIT0
MGTYRXN0_234	A5	nF1_J_RECV0	nF1_J_RECV0 → C54 0.1 UF 0402 → nF2_M_XMIT0
MGTYTXP0_234	A11	pF1_J_XMIT0	pF1_J_XMIT0 → C62 0.1 UF 0402 → pF2_M_RECV0
MGTYTXN0_234	A10	nF1_J_XMIT0	nF1_J_XMIT0 → C62 0.1 UF 0402 → nF2_M_RECV0
MGTYRXP1_234	A20	pF1_J_RECV1	pF1_J_RECV1 → C52 0.1 UF 0402 → pF2_M_XMIT1
MGTYRXN1_234	A19	nF1_J_RECV1	nF1_J_RECV1 → C52 0.1 UF 0402 → nF2_M_XMIT1
MGTYTXP1_234	B13	pF1_J_XMIT1	pF1_J_XMIT1 → C60 0.1 UF 0402 → pF2_M_RECV1
MGTYTXN1_234	B12	nF1_J_XMIT1	nF1_J_XMIT1 → C60 0.1 UF 0402 → nF2_M_RECV1
MGTYRXP2_234	B18	pF1_J_RECV2	pF1_J_RECV2 → C50 0.1 UF 0402 → pF2_M_XMIT2
MGTYRXN2_234	B17	nF1_J_RECV2	nF1_J_RECV2 → C50 0.1 UF 0402 → nF2_M_XMIT2
MGTYTXP2_234	A15	pF1_J_XMIT2	pF1_J_XMIT2 → C56 0.1 UF 0402 → pF2_M_RECV2
MGTYTXN2_234	A14	nF1_J_XMIT2	nF1_J_XMIT2 → C56 0.1 UF 0402 → nF2_M_RECV2
MGTYRXP3_234	C20	pF1_J_RECV3	pF1_J_RECV3 → C48 0.1 UF 0402 → pF2_M_XMIT3
MGTYRXN3_234	C19	nF1_J_RECV3	nF1_J_RECV3 → C48 0.1 UF 0402 → nF2_M_XMIT3
MGTYTXP3_234	C15	pF1_J_XMIT3	pF1_J_XMIT3 → C58 0.1 UF 0402 → pF2_M_RECV3
MGTYTXN3_234	C14	nF1_J_XMIT3	nF1_J_XMIT3 → C58 0.1 UF 0402 → nF2_M_RECV3

C55 0.1 UF 0402
C53 0.1 UF 0402
C51 0.1 UF 0402
C49 0.1 UF 0402
C63 0.1 UF 0402
C61 0.1 UF 0402
C57 0.1 UF 0402
C59 0.1 UF 0402

FPGA#2

U78-42
FPGA_VU13P_A2577
GTY QUAD 223 O

MGTREFCLK0P_223	AV13		
MGTREFCLK0N_223	AV12		
MGTREFCLK1P_223	AU11		
MGTREFCLK1N_223	AU10		
MGTYRXP0_223	BE2	pF2_O_RECV3	
MGTYRXN0_223	BE1	nF2_O_RECV3	
MGTYTXP0_223	BE7	pF2_O_XMIT3	
MGTYTXN0_223	BE6	nF2_O_XMIT3	
MGTYRXP1_223	BD4	pF2_O_RECV2	
MGTYRXN1_223	BD3	nF2_O_RECV2	
MGTYTXP1_223	BD9	pF2_O_XMIT2	
MGTYTXN1_223	BD8	nF2_O_XMIT2	
MGTYRXP2_223	BC2	pF2_O_RECV1	
MGTYRXN2_223	BC1	nF2_O_RECV1	
MGTYTXP2_223	BC7	pF2_O_XMIT1	
MGTYTXN2_223	BC6	nF2_O_XMIT1	
MGTYRXP3_223	BB4	pF2_O_RECV0	
MGTYRXN3_223	BB3	nF2_O_RECV0	
MGTYTXP3_223	BB9	pF2_O_XMIT0	
MGTYTXN3_223	BB8	nF2_O_XMIT0	

U78-41
FPGA_VU13P_A2577
GTY QUAD 222 N

MGTREFCLK0P_222	AY13	ac_pF2R_R0_N [19]	
MGTREFCLK0N_222	AY12	ac_nF2R_R0_N [19]	
MGTREFCLK1P_222	AW11	ac_pF2R_R1_N [22]	
MGTREFCLK1N_222	AW10	ac_nF2R_R1_N [22]	
MGTYRXP0_222	BH4	pF2_N_RECV3	
MGTYRXN0_222	BH3	nF2_N_RECV3	
MGTYTXP0_222	BG11	pF2_N_XMIT3	
MGTYTXN0_222	BG10	nF2_N_XMIT3	
MGTYRXP1_222	BG2	pF2_N_RECV2	
MGTYRXN1_222	BG1	nF2_N_RECV2	
MGTYTXP1_222	BJ11	pF2_N_XMIT2	
MGTYTXN1_222	BJ10	nF2_N_XMIT2	
MGTYRXP2_222	BG6	pF2_N_RECV1	
MGTYRXN2_222	BG5	nF2_N_RECV1	
MGTYTXP2_222	BH9	pF2_N_XMIT1	
MGTYTXN2_222	BH8	nF2_N_XMIT1	
MGTYRXP3_222	BF4	pF2_N_RECV0	
MGTYRXN3_222	BF3	nF2_N_RECV0	
MGTYTXP3_222	BF9	pF2_N_XMIT0	
MGTYTXN3_222	BF8	nF2_N_XMIT0	

U78-40
FPGA_VU13P_A2577
GTY QUAD 221 M

MGTREFCLK0P_221	BB13		
MGTREFCLK0N_221	BB12		
MGTREFCLK1P_221	BA11		
MGTREFCLK1N_221	BA10		
MGTYRXP0_221	BK18	pF2_M_RECV3	
MGTYRXN0_221	BK17	nF2_M_RECV3	
MGTYTXP0_221	BL15	pF2_M_XMIT3	
MGTYTXN0_221	BL14	nF2_M_XMIT3	
MGTYRXP1_221	BL20	pF2_M_RECV2	
MGTYRXN1_221	BL19	nF2_M_RECV2	
MGTYTXP1_221	BK13	pF2_M_XMIT2	
MGTYTXN1_221	BK12	nF2_M_XMIT2	
MGTYRXP2_221	BL6	pF2_M_RECV1	
MGTYRXN2_221	BL5	nF2_M_RECV1	
MGTYTXP2_221	BL11	pF2_M_XMIT1	
MGTYTXN2_221	BL10	nF2_M_XMIT1	
MGTYRXP3_221	BJ6	pF2_M_RECV0	
MGTYRXN3_221	BJ5	nF2_M_RECV0	
MGTYTXP3_221	BK9	pF2_M_XMIT0	
MGTYTXN3_221	BK8	nF2_M_XMIT0	

APOLLO CM v3			
Title: 9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M			
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9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-47
FPGA_VU13P_A2577
GTY QUAD 228 D

MGTREFCLK0P_228	AE11		
MGTREFCLK0N_228	AE10		
MGTREFCLK1P_228	AC11		
MGTREFCLK1N_228	AC10		
MGTYRXP0_228	AE2	pF1_D_RECV0	pF1_D_RECV0 — C170 0.1 UF 0402 — pF2_C_XMIT0 — pF2_C_XMIT0
MGTYRXN0_228	AE1	nF1_D_RECV0	nF1_D_RECV0 — C169 0.1 UF 0402 — nF2_C_XMIT0 — nF2_C_XMIT0
MGTYTXP0_228	AE7	pF1_D_XMIT0	pF1_D_XMIT0 — C178 0.1 UF 0402 — pF2_C_RECV0 — pF2_C_RECV0
MGTYTXN0_228	AE6	nF1_D_XMIT0	nF1_D_XMIT0 — C177 0.1 UF 0402 — nF2_C_RECV0 — nF2_C_RECV0
MGTYRXP1_228	AD4	pF1_D_RECV1	pF1_D_RECV1 — C168 0.1 UF 0402 — pF2_C_XMIT1 — pF2_C_XMIT1
MGTYRXN1_228	AD3	nF1_D_RECV1	nF1_D_RECV1 — C167 0.1 UF 0402 — nF2_C_XMIT1 — nF2_C_XMIT1
MGTYTXP1_228	AD9	pF1_D_XMIT1	pF1_D_XMIT1 — C176 0.1 UF 0402 — pF2_C_RECV1 — pF2_C_RECV1
MGTYTXN1_228	AD8	nF1_D_XMIT1	nF1_D_XMIT1 — C175 0.1 UF 0402 — nF2_C_RECV1 — nF2_C_RECV1
MGTYRXP2_228	AC2	pF1_D_RECV2	pF1_D_RECV2 — C166 0.1 UF 0402 — pF2_C_XMIT2 — pF2_C_XMIT2
MGTYRXN2_228	AC1	nF1_D_RECV2	nF1_D_RECV2 — C165 0.1 UF 0402 — nF2_C_XMIT2 — nF2_C_XMIT2
MGTYTXP2_228	AC7	pF1_D_XMIT2	pF1_D_XMIT2 — C174 0.1 UF 0402 — pF2_C_RECV2 — pF2_C_RECV2
MGTYTXN2_228	AC6	nF1_D_XMIT2	nF1_D_XMIT2 — C173 0.1 UF 0402 — nF2_C_RECV2 — nF2_C_RECV2
MGTYRXP3_228	AB4	pF1_D_RECV3	pF1_D_RECV3 — C164 0.1 UF 0402 — pF2_C_XMIT3 — pF2_C_XMIT3
MGTYRXN3_228	AB3	nF1_D_RECV3	nF1_D_RECV3 — C163 0.1 UF 0402 — nF2_C_XMIT3 — nF2_C_XMIT3
MGTYTXP3_228	AB9	pF1_D_XMIT3	pF1_D_XMIT3 — C172 0.1 UF 0402 — pF2_C_RECV3 — pF2_C_RECV3
MGTYTXN3_228	AB8	nF1_D_XMIT3	nF1_D_XMIT3 — C171 0.1 UF 0402 — nF2_C_RECV3 — nF2_C_RECV3

U77-48
FPGA_VU13P_A2577
GTY QUAD 229 E

MGTREFCLK0P_229	AA11	ac_pF1R_R0_E [19]	
MGTREFCLK0N_229	AA10	ac_nF1R_R0_E [19]	
MGTREFCLK1P_229	Y13	ac_pF1R_R1_E [22]	
MGTREFCLK1N_229	Y12	ac_nF1R_R1_E [22]	
MGTYRXP0_229	AA2	pF1_E_RECV0	pF1_E_RECV0 — C151 0.1 UF 0402 — pF2_B_XMIT0 — pF2_B_XMIT0
MGTYRXN0_229	AA1	nF1_E_RECV0	nF1_E_RECV0 — C150 0.1 UF 0402 — nF2_B_XMIT0 — nF2_B_XMIT0
MGTYTXP0_229	AA7	pF1_E_XMIT0	pF1_E_XMIT0 — C159 0.1 UF 0402 — pF2_B_RECV0 — pF2_B_RECV0
MGTYTXN0_229	AA6	nF1_E_XMIT0	nF1_E_XMIT0 — C158 0.1 UF 0402 — nF2_B_RECV0 — nF2_B_RECV0
MGTYRXP1_229	Y4	pF1_E_RECV1	pF1_E_RECV1 — C149 0.1 UF 0402 — pF2_B_XMIT1 — pF2_B_XMIT1
MGTYRXN1_229	Y3	nF1_E_RECV1	nF1_E_RECV1 — C148 0.1 UF 0402 — nF2_B_XMIT1 — nF2_B_XMIT1
MGTYTXP1_229	Y9	pF1_E_XMIT1	pF1_E_XMIT1 — C157 0.1 UF 0402 — pF2_B_RECV1 — pF2_B_RECV1
MGTYTXN1_229	Y8	nF1_E_XMIT1	nF1_E_XMIT1 — C156 0.1 UF 0402 — nF2_B_RECV1 — nF2_B_RECV1
MGTYRXP2_229	W2	pF1_E_RECV2	pF1_E_RECV2 — C147 0.1 UF 0402 — pF2_B_XMIT2 — pF2_B_XMIT2
MGTYRXN2_229	W1	nF1_E_RECV2	nF1_E_RECV2 — C146 0.1 UF 0402 — nF2_B_XMIT2 — nF2_B_XMIT2
MGTYTXP2_229	W7	pF1_E_XMIT2	pF1_E_XMIT2 — C155 0.1 UF 0402 — pF2_B_RECV2 — pF2_B_RECV2
MGTYTXN2_229	W6	nF1_E_XMIT2	nF1_E_XMIT2 — C154 0.1 UF 0402 — nF2_B_RECV2 — nF2_B_RECV2
MGTYRXP3_229	V4	pF1_E_RECV3	pF1_E_RECV3 — C145 0.1 UF 0402 — pF2_B_XMIT3 — pF2_B_XMIT3
MGTYRXN3_229	V3	nF1_E_RECV3	nF1_E_RECV3 — C144 0.1 UF 0402 — nF2_B_XMIT3 — nF2_B_XMIT3
MGTYTXP3_229	V9	pF1_E_XMIT3	pF1_E_XMIT3 — C153 0.1 UF 0402 — pF2_B_RECV3 — pF2_B_RECV3
MGTYTXN3_229	V8	nF1_E_XMIT3	nF1_E_XMIT3 — C152 0.1 UF 0402 — nF2_B_RECV3 — nF2_B_RECV3

U77-49
FPGA_VU13P_A2577
GTY QUAD 230 F

MGTREFCLK0P_230	W11		
MGTREFCLK0N_230	W10		
MGTREFCLK1P_230	V13		
MGTREFCLK1N_230	V12		
MGTYRXP0_230	U2	pF1_F_RECV0	pF1_F_RECV0 — C131 0.1 UF 0402 — pF2_A_XMIT0 — pF2_A_XMIT0
MGTYRXN0_230	U1	nF1_F_RECV0	nF1_F_RECV0 — C130 0.1 UF 0402 — nF2_A_XMIT0 — nF2_A_XMIT0
MGTYTXP0_230	U7	pF1_F_XMIT0	pF1_F_XMIT0 — C139 0.1 UF 0402 — pF2_A_RECV0 — pF2_A_RECV0
MGTYTXN0_230	U6	nF1_F_XMIT0	nF1_F_XMIT0 — C138 0.1 UF 0402 — nF2_A_RECV0 — nF2_A_RECV0
MGTYRXP1_230	T4	pF1_F_RECV1	pF1_F_RECV1 — C129 0.1 UF 0402 — pF2_A_XMIT1 — pF2_A_XMIT1
MGTYRXN1_230	T3	nF1_F_RECV1	nF1_F_RECV1 — C128 0.1 UF 0402 — nF2_A_XMIT1 — nF2_A_XMIT1
MGTYTXP1_230	T9	pF1_F_XMIT1	pF1_F_XMIT1 — C137 0.1 UF 0402 — pF2_A_RECV1 — pF2_A_RECV1
MGTYTXN1_230	T8	nF1_F_XMIT1	nF1_F_XMIT1 — C136 0.1 UF 0402 — nF2_A_RECV1 — nF2_A_RECV1
MGTYRXP2_230	R2	pF1_F_RECV2	pF1_F_RECV2 — C127 0.1 UF 0402 — pF2_A_XMIT2 — pF2_A_XMIT2
MGTYRXN2_230	R1	nF1_F_RECV2	nF1_F_RECV2 — C126 0.1 UF 0402 — nF2_A_XMIT2 — nF2_A_XMIT2
MGTYTXP2_230	R7	pF1_F_XMIT2	pF1_F_XMIT2 — C135 0.1 UF 0402 — pF2_A_RECV2 — pF2_A_RECV2
MGTYTXN2_230	R6	nF1_F_XMIT2	nF1_F_XMIT2 — C134 0.1 UF 0402 — nF2_A_RECV2 — nF2_A_RECV2
MGTYRXP3_230	P4	pF1_F_RECV3	pF1_F_RECV3 — C125 0.1 UF 0402 — pF2_A_XMIT3 — pF2_A_XMIT3
MGTYRXN3_230	P3	nF1_F_RECV3	nF1_F_RECV3 — C124 0.1 UF 0402 — nF2_A_XMIT3 — nF2_A_XMIT3
MGTYTXP3_230	P9	pF1_F_XMIT3	pF1_F_XMIT3 — C133 0.1 UF 0402 — pF2_A_RECV3 — pF2_A_RECV3
MGTYTXN3_230	P8	nF1_F_XMIT3	nF1_F_XMIT3 — C132 0.1 UF 0402 — nF2_A_RECV3 — nF2_A_RECV3

FPGA#2

U78-46
FPGA_VU13P_A2577
GTY QUAD 227 C

MGTREFCLK0P_227	AJ11		
MGTREFCLK0N_227	AJ10		
MGTREFCLK1P_227	AG11		
MGTREFCLK1N_227	AG10		
MGTYRXP0_227	AJ2	pF2_C_RECV3	
MGTYRXN0_227	AJ1	nF2_C_RECV3	
MGTYTXP0_227	AJ7	pF2_C_XMIT3	
MGTYTXN0_227	AJ6	nF2_C_XMIT3	
MGTYRXP1_227	AH4	pF2_C_RECV2	
MGTYRXN1_227	AH3	nF2_C_RECV2	
MGTYTXP1_227	AH9	pF2_C_XMIT2	
MGTYTXN1_227	AH8	nF2_C_XMIT2	
MGTYRXP2_227	AG2	pF2_C_RECV1	
MGTYRXN2_227	AG1	nF2_C_RECV1	
MGTYTXP2_227	AG7	pF2_C_XMIT1	
MGTYTXN2_227	AG6	nF2_C_XMIT1	
MGTYRXP3_227	AF4	pF2_C_RECV0	
MGTYRXN3_227	AF3	nF2_C_RECV0	
MGTYTXP3_227	AF9	pF2_C_XMIT0	
MGTYTXN3_227	AF8	nF2_C_XMIT0	

U78-45
FPGA_VU13P_A2577
GTY QUAD 226 B

MGTREFCLK0P_226	AM13	ac_pF2R_R0_B [19]	
MGTREFCLK0N_226	AM12	ac_nF2R_R0_B [19]	
MGTREFCLK1P_226	AL11	ac_pF2R_R1_B [22]	
MGTREFCLK1N_226	AL10	ac_nF2R_R1_B [22]	
MGTYRXP0_226	AN2	pF2_B_RECV3	
MGTYRXN0_226	AN1	nF2_B_RECV3	
MGTYTXP0_226	AN7	pF2_B_XMIT3	
MGTYTXN0_226	AN6	nF2_B_XMIT3	
MGTYRXP1_226	AM4	pF2_B_RECV2	
MGTYRXN1_226	AM3	nF2_B_RECV2	
MGTYTXP1_226	AM9	pF2_B_XMIT2	
MGTYTXN1_226	AM8	nF2_B_XMIT2	
MGTYRXP2_226	AL2	pF2_B_RECV1	
MGTYRXN2_226	AL1	nF2_B_RECV1	
MGTYTXP2_226	AL7	pF2_B_XMIT1	
MGTYTXN2_226	AL6	nF2_B_XMIT1	
MGTYRXP3_226	AK4	pF2_B_RECV0	
MGTYRXN3_226	AK3	nF2_B_RECV0	
MGTYTXP3_226	AK9	pF2_B_XMIT0	
MGTYTXN3_226	AK8	nF2_B_XMIT0	

U78-44
FPGA_VU13P_A2577
GTY QUAD 225 A

MGTREFCLK0P_225	AP13		
MGTREFCLK0N_225	AP12		
MGTREFCLK1P_225	AN11		
MGTREFCLK1N_225	AN10		
MGTYRXP0_225	AU2	pF2_A_RECV3	
MGTYRXN0_225	AU1	nF2_A_RECV3	
MGTYTXP0_225	AU7	pF2_A_XMIT3	
MGTYTXN0_225	AU6	nF2_A_XMIT3	
MGTYRXP1_225	AT4	pF2_A_RECV2	
MGTYRXN1_225	AT3	nF2_A_RECV2	
MGTYTXP1_225	AT9	pF2_A_XMIT2	
MGTYTXN1_225	AT8	nF2_A_XMIT2	
MGTYRXP2_225	AR2	pF2_A_RECV1	
MGTYRXN2_225	AR1	nF2_A_RECV1	
MGTYTXP2_225	AR7	pF2_A_XMIT1	
MGTYTXN2_225	AR6	nF2_A_XMIT1	
MGTYRXP3_225	AP4	pF2_A_RECV0	
MGTYRXN3_225	AP3	nF2_A_RECV0	
MGTYTXP3_225	AP9	pF2_A_XMIT0	
MGTYTXN3_225	AP8	nF2_A_XMIT0	

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9.05: F1 QUAD G_P TO F2 QUAD P_G

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-50
FPGA_VU13P_A2577
GTY QUAD 231 G

MGTREFCLK0P_231	U11	ac_pF1R_R0_G [19]	
MGTREFCLK0N_231	U10	ac_nF1R_R0_G [19]	
MGTREFCLK1P_231	T13	ac_pF1R_R1_G [22]	
MGTREFCLK1N_231	T12	ac_nF1R_R1_G [22]	
MGTYRXP0_231	N2	pF1_G_RECV0	
MGTYRXN0_231	N1	nF1_G_RECV0	
MGTYTXP0_231	N7	pF1_G_XMIT0	
MGTYTXN0_231	N6	nF1_G_XMIT0	
MGTYRXP1_231	M4	pF1_G_RECV1	
MGTYRXN1_231	M3	nF1_G_RECV1	
MGTYTXP1_231	M9	pF1_G_XMIT1	
MGTYTXN1_231	M8	nF1_G_XMIT1	
MGTYRXP2_231	L2	pF1_G_RECV2	
MGTYRXN2_231	L1	nF1_G_RECV2	
MGTYTXP2_231	L7	pF1_G_XMIT2	
MGTYTXN2_231	L6	nF1_G_XMIT2	
MGTYRXP3_231	K4	pF1_G_RECV3	
MGTYRXN3_231	K3	nF1_G_RECV3	
MGTYTXP3_231	K9	pF1_G_XMIT3	
MGTYTXN3_231	K8	nF1_G_XMIT3	

pF1_G_RECV0	C112 0.1 UF 0402	pF2_P_XMIT0	
nF1_G_RECV0	C111 0.1 UF 0402	nF2_P_XMIT0	
pF1_G_RECV1	C110 0.1 UF 0402	pF2_P_XMIT1	
nF1_G_RECV1	C109 0.1 UF 0402	nF2_P_XMIT1	
pF1_G_RECV2	C108 0.1 UF 0402	pF2_P_XMIT2	
nF1_G_RECV2	C107 0.1 UF 0402	nF2_P_XMIT2	
pF1_G_RECV3	C106 0.1 UF 0402	pF2_P_XMIT3	
nF1_G_RECV3	C105 0.1 UF 0402	nF2_P_XMIT3	

pF1_G_XMIT0	C120 0.1 UF 0402	pF2_P_RECV0	
nF1_G_XMIT0	C119 0.1 UF 0402	nF2_P_RECV0	
pF1_G_XMIT1	C118 0.1 UF 0402	pF2_P_RECV1	
nF1_G_XMIT1	C117 0.1 UF 0402	nF2_P_RECV1	
pF1_G_XMIT2	C116 0.1 UF 0402	pF2_P_RECV2	
nF1_G_XMIT2	C115 0.1 UF 0402	nF2_P_RECV2	
pF1_G_XMIT3	C114 0.1 UF 0402	pF2_P_RECV3	
nF1_G_XMIT3	C113 0.1 UF 0402	nF2_P_RECV3	

FPGA#2

U78-43
FPGA_VU13P_A2577
P GTY QUAD 224

ac_pF2R_R0_P	[19]	AT13	MGTREFCLK0P_224
ac_nF2R_R0_P	[19]	AT12	MGTREFCLK0N_224
ac_pF2R_R1_P	[22]	AR11	MGTREFCLK1P_224
ac_nF2R_R1_P	[22]	AR10	MGTREFCLK1N_224
pF2_P_RECV3		BA2	MGTYRXP0_224
nF2_P_RECV3		BA1	MGTYRXN0_224
pF2_P_XMIT3		BA7	MGTYTXP0_224
nF2_P_XMIT3		BA6	MGTYTXN0_224
pF2_P_RECV2		AY4	MGTYRXP1_224
nF2_P_RECV2		AY3	MGTYRXN1_224
pF2_P_XMIT2		AY9	MGTYTXP1_224
nF2_P_XMIT2		AY8	MGTYTXN1_224
pF2_P_RECV1		AW2	MGTYRXP2_224
nF2_P_RECV1		AW1	MGTYRXN2_224
pF2_P_XMIT1		AW7	MGTYTXP2_224
nF2_P_XMIT1		AW6	MGTYTXN2_224
pF2_P_RECV0		AV4	MGTYRXP3_224
nF2_P_RECV0		AV3	MGTYRXN3_224
pF2_P_XMIT0		AV9	MGTYTXP3_224
nF2_P_XMIT0		AV8	MGTYTXN3_224

U77-43
FPGA_VU13P_A2577
GTY QUAD 224 P

MGTREFCLK0P_224	AT13	ac_pF1R_R0_P [19]	
MGTREFCLK0N_224	AT12	ac_nF1R_R0_P [19]	
MGTREFCLK1P_224	AR11	ac_pF1R_R1_P [22]	
MGTREFCLK1N_224	AR10	ac_nF1R_R1_P [22]	
MGTYRXP0_224	BA2	pF1_P_RECV0	
MGTYRXN0_224	BA1	nF1_P_RECV0	
MGTYTXP0_224	BA7	pF1_P_XMIT0	
MGTYTXN0_224	BA6	nF1_P_XMIT0	
MGTYRXP1_224	AY4	pF1_P_RECV1	
MGTYRXN1_224	AY3	nF1_P_RECV1	
MGTYTXP1_224	AY9	pF1_P_XMIT1	
MGTYTXN1_224	AY8	nF1_P_XMIT1	
MGTYRXP2_224	AW2		
MGTYRXN2_224	AW1		
MGTYTXP2_224	AW7		
MGTYTXN2_224	AW6		
MGTYRXP3_224	AV4		
MGTYRXN3_224	AV3		
MGTYTXP3_224	AV9		
MGTYTXN3_224	AV8		

pF1_P_RECV0	C256 0.1 UF 0402	pF2_G_XMIT0	
nF1_P_RECV0	C255 0.1 UF 0402	nF2_G_XMIT0	
pF1_P_RECV1	C258 0.1 UF 0402	pF2_G_XMIT1	
nF1_P_RECV1	C257 0.1 UF 0402	nF2_G_XMIT1	

pF1_P_XMIT0	C251 0.1 UF 0402	pF2_G_RECV0	
nF1_P_XMIT0	C252 0.1 UF 0402	nF2_G_RECV0	
pF1_P_XMIT1	C254 0.1 UF 0402	pF2_G_RECV1	
nF1_P_XMIT1	C253 0.1 UF 0402	nF2_G_RECV1	

THERE IS ONLY SPACE ON THE PCB FOR 8 CAPACITORS. THIS SUPPORTS TWO OF THE FOUR TRANSMIT/RECEIVE PAIRS.

U78-50
FPGA_VU13P_A2577
G GTY QUAD 231

ac_pF2R_R0_G	[19]	U11	MGTREFCLK0P_231
ac_nF2R_R0_G	[19]	U10	MGTREFCLK0N_231
ac_pF2R_R1_G	[22]	T13	MGTREFCLK1P_231
ac_nF2R_R1_G	[22]	T12	MGTREFCLK1N_231
pF2_G_RECV1		N2	MGTYRXP0_231
nF2_G_RECV1		N1	MGTYRXN0_231
pF2_G_XMIT1		N7	MGTYTXP0_231
nF2_G_XMIT1		N6	MGTYTXN0_231
pF2_G_RECV0		M4	MGTYRXP1_231
nF2_G_RECV0		M3	MGTYRXN1_231
pF2_G_XMIT0		M9	MGTYTXP1_231
nF2_G_XMIT0		M8	MGTYTXN1_231
		L2	MGTYRXP2_231
		L1	MGTYRXN2_231
		L7	MGTYTXP2_231
		L6	MGTYTXN2_231
		K4	MGTYRXP3_231
		K3	MGTYRXN3_231
		K9	MGTYTXP3_231
		K8	MGTYTXN3_231

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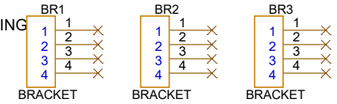
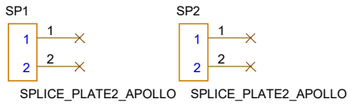
9.99: MECHANICAL PARTS

THESE SHAPES DEFINE MECHANICAL OBJECTS
THAT SHOULD BE IN THE BILL OF MATERIALS.

BRACKETS FOR SUPPORTING A SUB-FRONT PANEL



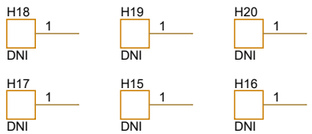
THESE SHAPES DEFINE HOLES AND KEEPOUT AREAS FOR THE SPLICE PLATES.



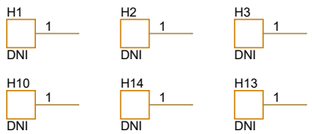
THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINK

THESE HOLES ARE FOR MOUNTING THE LGA80D HEATSINK

THESE STANDOFFS ARE FOR MOUNTING THE BOTTOM COVER. THE STANDOFF IS SOLDERED TO THE BOTTOM SIDE OF THE BOARD.



THESE STANDOFFS ARE FOR MOUNTING THE TOP COVER. THE STANDOFF IS SCREWED FROM THE BOTTOM SIDE OF THE BOARD.



H21 THRU H28 ARE FOR MOUNTING STANDOFFS FOR THE FPGA HEATSINKS. THE HOLES ARE PART OF THE FOOTPRINT, SO DISCRETE PARTS DO NOT APPEAR ON THE SCHEMATIC.

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