THESE STANDOFFS ARE FOR MOUNTING THE BOTTOM COVER. THE STANDOFF IS SOLDERED TO THE BOTTOM SIDE OF THE BOARD.

H4 DNI, H1 DNI, H5 DNI, H2 DNI, H3 DNI

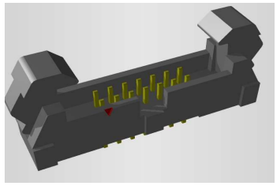
LEDS 1.9V @ 2MA

GND — LED1 GREEN — R7 0603 1% 698 — V_3V3

3V3_POWER

LED2 GREEN — R23 0603 1% 5.1K — V_12V

12V_POWER



THE FPGA JTAG REFERENCE IS 3.3 VOLTS.

THIS CONNECTOR IS FOR A XILINX JTAG PROGRAMMER WITH A 14-PIN 2-MM CONNECTOR.

FPGA JTAG

V_3V3, J22, CON_2X7_VERT

SM_JTAG_TMS, SM_JTAG_TCK, SM_JTAG_TDO, SM_JTAG_TDI, GND

BENCHTOP POWER INLET

J1 CON4: +12V, GND — V_12V — GND

P3 ET60S-D02-3-08-000

THESE ARE THE SIGNAL NAMES ON THE SMv2

PWR_GOOD	1-1	01	CM_TO_SM_PWR_OK
TMS	1-2	02	SM_JTAG_TMS
TDO	1-3	03	SM_JTAG_TDO
TX_IPMC	1-4	04	SM_IPMC_TX
TX_ZYNQ	1-5	05	SM_ZYNQ_TX
SENSE_SDA	1-6	06	SM_IPMC_I2C_SDA
PWR_EN	1-7	07	SM_SOFT_PWR_EN
FPGA_GPIO0	1-8	08	SM_ZYNQ_I2C_SCL
FPGA_GPIO1	2-1	09	SM_ZYNQ_GPIO1
GND_LOGIC	2-2	10	GND
GND_LOGIC	2-3	11	GND
FPGA_GPIO2	2-4	12	SM_ZYNQ_GPIO2
GND_LOGIC	2-5	13	GND
CPLD_GPIO0	2-6	14	SM_CPLD_GPIO0
GND_LOGIC	2-7	15	GND
CPLD_GPIO1	2-8	16	SM_CPLD_GPIO1
EN	3-1	17	SM_TO_CM_PWR_EN
TCK	3-2	18	SM_JTAG_TCK
TDI	3-3	19	SM_JTAG_TDI
RX_IPMC	3-4	20	SM_IPMC_RX
RX_ZYNQ	3-5	21	SM_ZYNQ_RX
SENSE_SCL	3-6	22	SM_IPMC_I2C_SCL
MON_RX	3-7	23	SM_ZYNQ_I2C_SDA
/PS_RST	3-8	24	

/PS_RST IS NOT USED IN THIS DESIGN

V_3V3 — SW1 SW SPST — R25 4.7K 0603 1% — R28 4.7K — R29 47K 0603 1% — GND

THE CM NEEDS A HI LEVEL ON "SM_TO_CM_PWR_EN" IN ORDER TO BOOT THE MCU. THIS CAN COME FROM EITHER THE SWITCH CONNECTED TO 3.3V, OR FROM A CONTROL LINE ON THE USB-TO-I2C CABLE.

CABLE_SM_TO_CM_PWR_EN, /F1_FF_RESET [4]

CM_TO_SM_PWR_OK, CABLE_SM_SOFT_PWR_EN

ZYNQ UART

THESE CONNECTORS ARE FOR A STANDALONE USB-TO-UART CABLE. SEE DIGIKEY 768-1015 (FTDI TTL-232R-3V3). THE FACTORY CONNECTOR NEEDS TO BE REPLACED WITH A 6-PIN 2MM PLUG, DIGIKEY 277-5955.

J20 JUMP_2X2: SM_ZYNQ_RX, SM_ZYNQ_TX — GND — J27 CON6

IPMC UART

J21 JUMP_2X2: SM_IPMC_RX, SM_IPMC_TX — GND — J28 CON6

ZYNQ I2C

THESE CONNECTORS ARE FOR A USB-TO-I2C CABLE. SEE DIGIKEY 768-1106 (FTDI TTL-232R-3V3). THE FACTORY CONNECTOR NEEDS TO BE REPLACED WITH A 10-PIN 2MM PLUG, DIGIKEY 277-5982.

J11 JUMP_2X2: SM_ZYNQ_I2C_SCL, SM_ZYNQ_I2C_SDA — J19 CON10

J12 JUMP_2X2: SM_ZYNQ_GPIO1, SM_ZYNQ_GPIO2

J13 JUMP_2X2: SM_CPLD_GPIO0, SM_CPLD_GPIO1 — GND

THE FIREFLY I2C SIGNALS ALWAYS USE THIS CABLE CONNECTOR.

I2C_SCL_F1_FF5_XCVR [4], I2C_SDA_F1_FF5_XCVR [4]

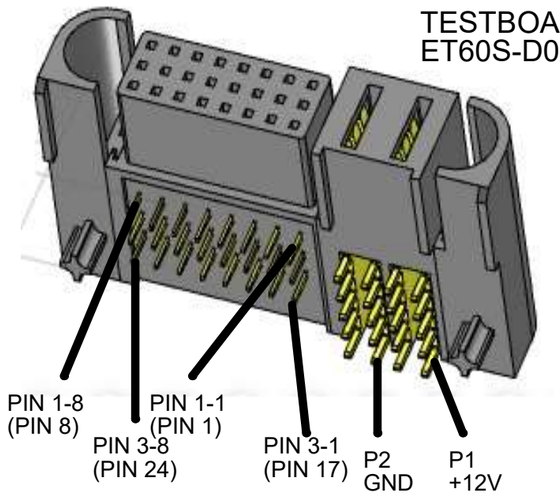
IPMC I2C

J8 JUMP_2X2: SM_IPMC_I2C_SCL, SM_IPMC_I2C_SDA — J18 CON10

J9 JUMP_2X2: CABLE_SM_TO_CM_PWR_EN, /F1_FF_RESET [4]

J10 JUMP_2X2: CM_TO_SM_PWR_OK, CABLE_SM_SOFT_PWR_EN — GND

TESTBOARD (SM) CONNECTOR ET60S-D02-3-08-000-L-R1-S



SW SPST — R51 4.7K 0603 1% — V_3V3 — SW2

CABLE_SM_SOFT_PWR_EN

U6 74LVC1G32: A, B, Y, VCC, GND — SM_SOFT_PWR_EN — V_3V3 — GND

THE CM NEEDS A HI LEVEL ON "SM_SOFT_PWR_EN" IN ORDER FOR THE BOOTED MCU TO TURN ON THE DC-DC CONVERTERS. THIS CAN COME FROM EITHER THE SWITCH CONNECTED TO 3.3V, OR FROM A CONTROL LINE ON THE USB-TO-I2C CABLE.

R22 47K 0603 1% — R24 47K 0603 1% — GND

TO CONNECT THE SIGNALS TO THE CABLE CONNECTOR, INSTALL A JUMPER FROM PIN#1 TO PIN#2 AND ANOTHER JUMPER FROM PIN#3 TO PIN#4.

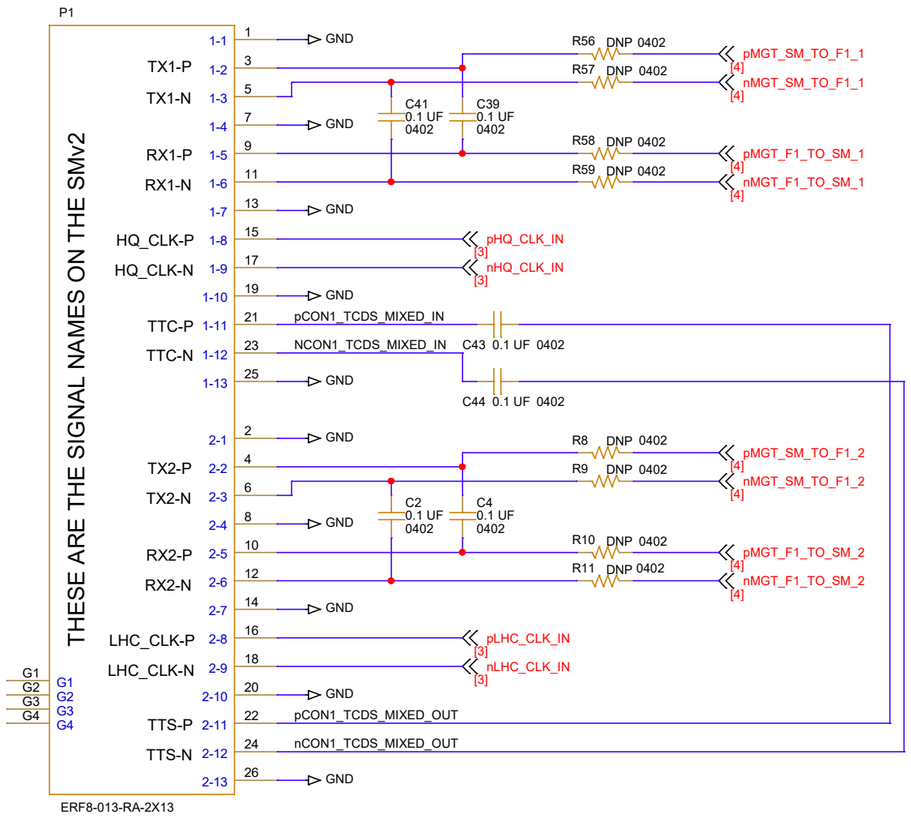
TO LOOP THE SIGNALS BACK TO THE CM, INSTALL A JUMPER FROM PIN#1 TO PIN#3.

TO CONNECT THE SIGNALS ELSEWHERE, USE WIREWRAP WIRE.

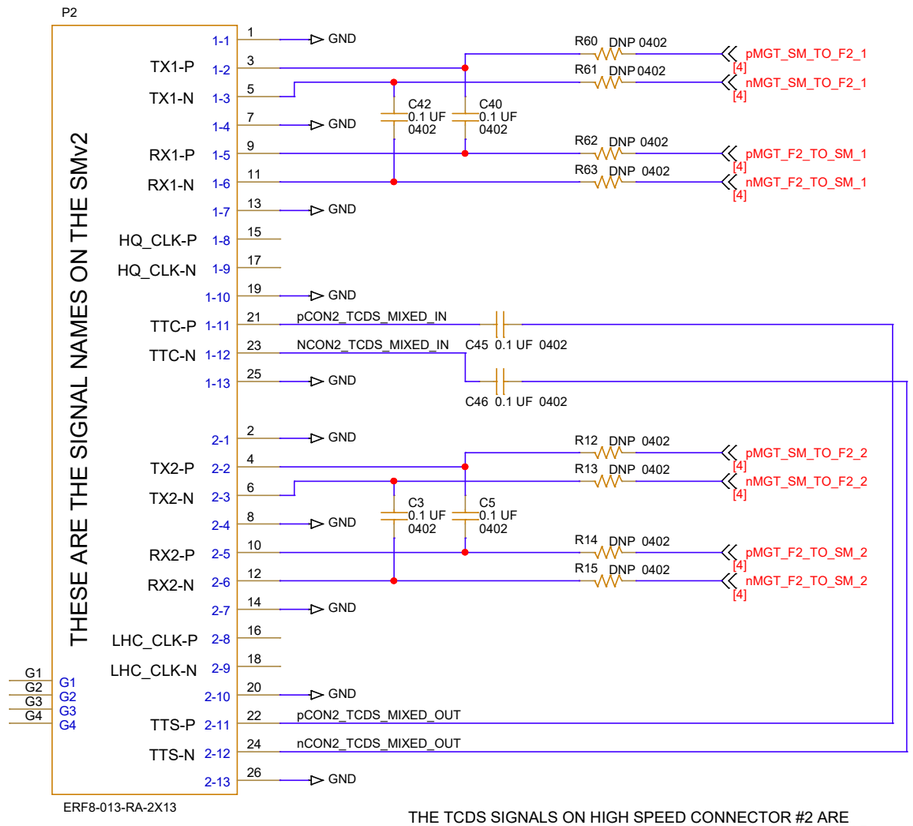
APOLLO CM V3 TEST BOARD		
Title: 01: POWER CONNECTOR		
Size	Document Number: 6089-126	Rev: A
Date: Thursday, October 24, 2024	Sheet 6 of 6	

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. AC COUPLING CAPACITORS ARE ASSUMED TO BE ON THE SM.

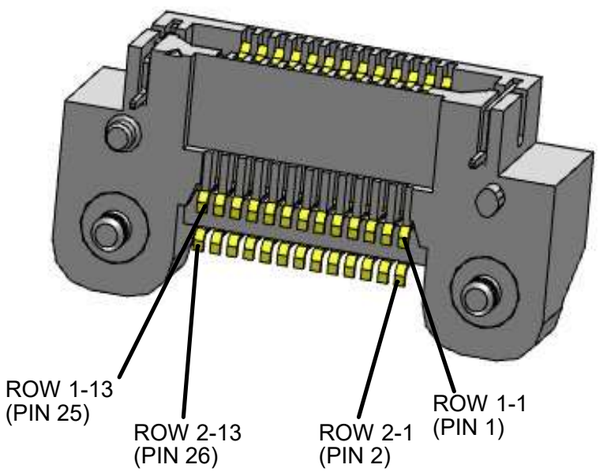
FPGA#1 AND BACKPLANE CLOCK SIGNALS



FPGA#2 SIGNALS



THE TCDS SIGNALS ON HIGH SPEED CONNECTOR #2 ARE LABELED "MIXED" BECAUSE THEY CAN EITHER BE REGULAR TCDS SIGNALS WHEN THE SM IS THE TCDS ENDPOINT, OR THEY CAN BE REPEATED TCDS SIGNALS WHEN FPGA#1 IS THE TCDS ENDPOINT.



ERF8-013-01-L-D-RA-TR

TO LOOP THE GIGABIT TRANSMIT SIGNALS FROM THE CM BACK TO THE RECEIVE SIGNALS, INSTALL THE COUPLING CAPACITORS AND OMIT THE SERIES ZERO-OHM RESISTORS.

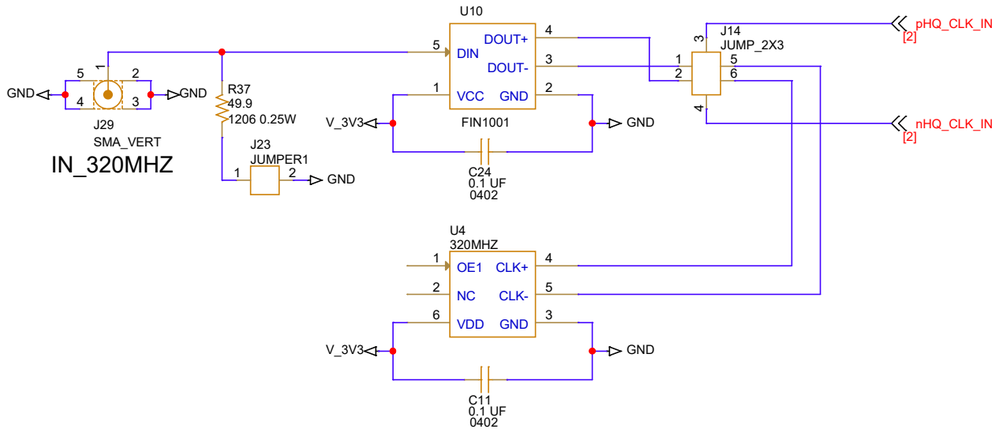
TO USE THE FIREFLY SITE, OMIT THE COUPLING CAPACITORS AND INSTALL THE SERIES ZERO-OHM RESISTORS.

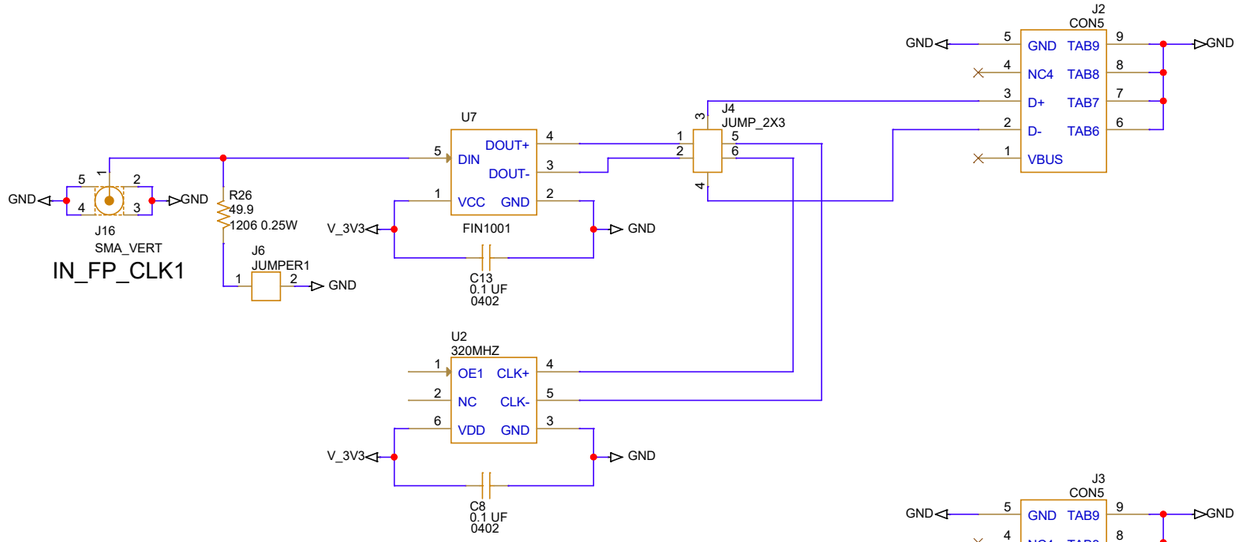
APOLLO CM V3 TEST BOARD

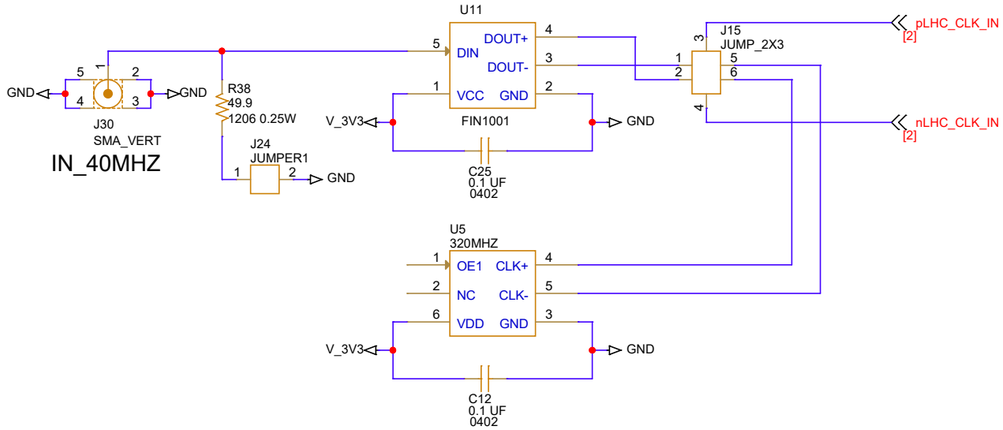
Title: 02: HIGH SPEED CONNECTORS

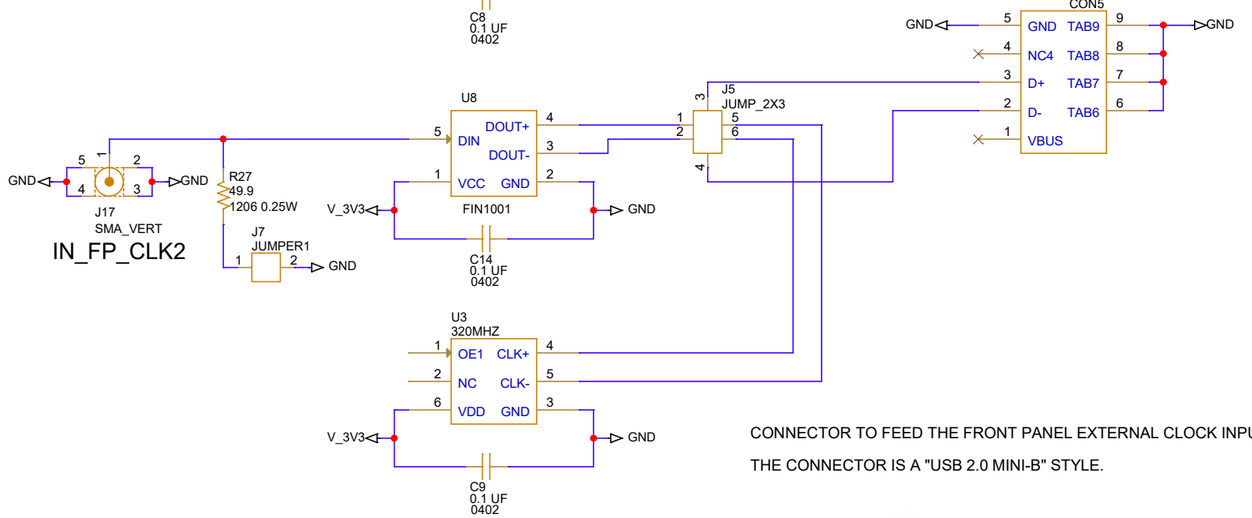
Size	Document Number	Rev
	6089-126	A

Date: Thursday, October 24, 2024 Sheet 6 of 6



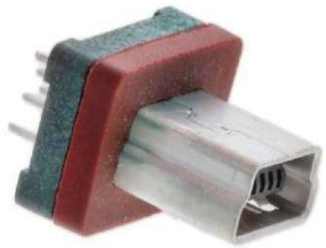




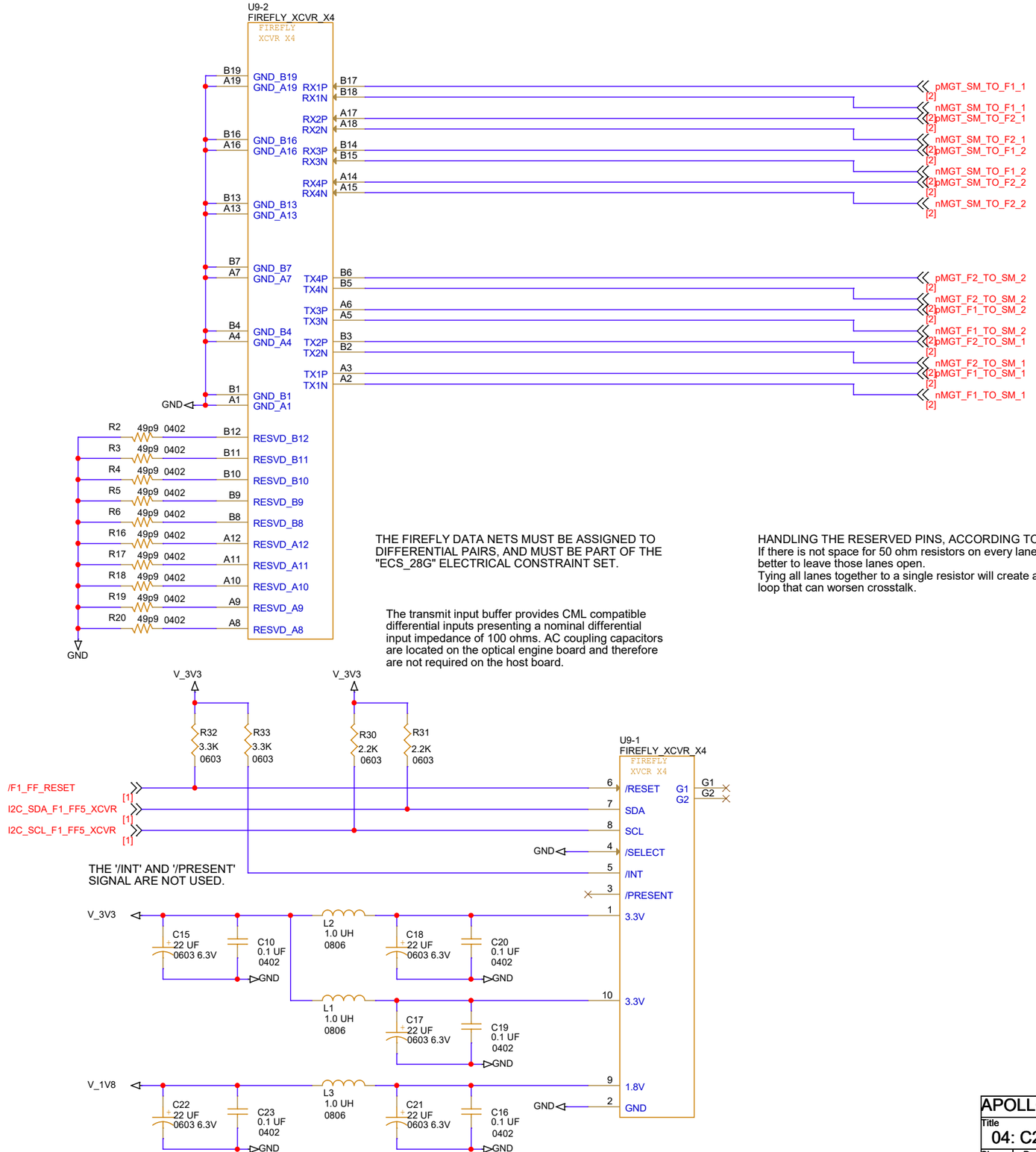


CONNECTOR TO FEED THE FRONT PANEL EXTERNAL CLOCK INPUT..

THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE.



APOLLO CM V3 TEST BOARD		
Title: 03: CLOCKING		
Size	Document Number: 6089-126	Rev: A
Date: Thursday, October 24, 2024	Sheet 6 of 6	



APOLLO CM V3 TEST BOARD		
Title: 04: C2C FIREFLY		
Size	Document Number: 6089-126	Rev: A
Date: Thursday, October 24, 2024	Sheet 6 of 6	

NOTES:

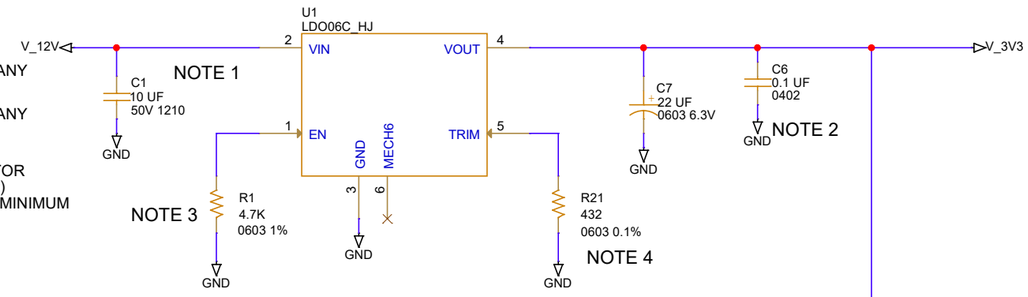
NOTE 1 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL INPUT CAPACITORS.

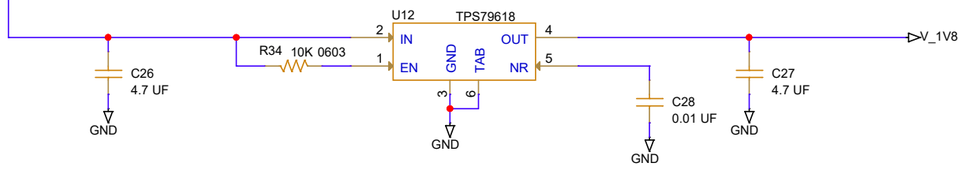
NOTE 2 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL OUTPUT CAPACITORS.

NOTE 3 UNDERVOLTAGE LOCKOUT RESISTOR
R = 14.81 * (6.81 / ((6.81*Ven) - 18.16))
A 4.7K RESISTOR GIVES 5.8 VOLTS MINIMUM TURNON VOLTAGE

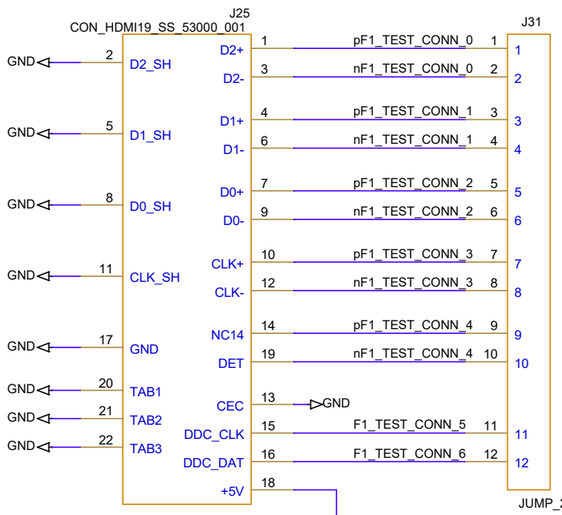
NOTE 4

OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 3.3 VOLTS, R = 436 OHMS (IF R=432 THEN V=3.327)

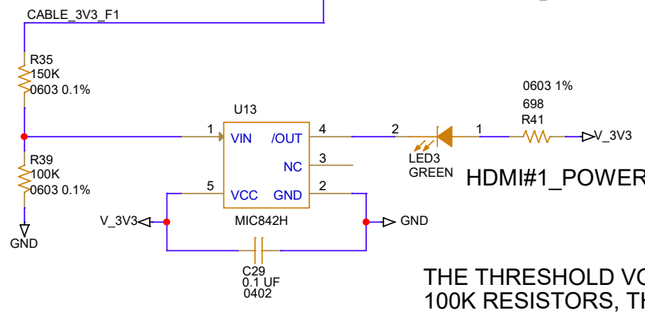


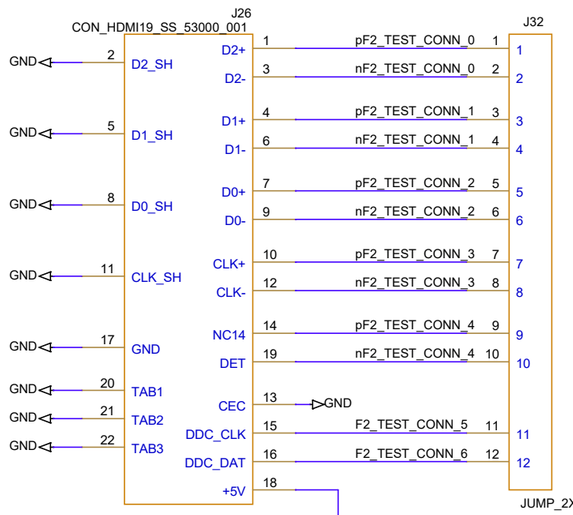


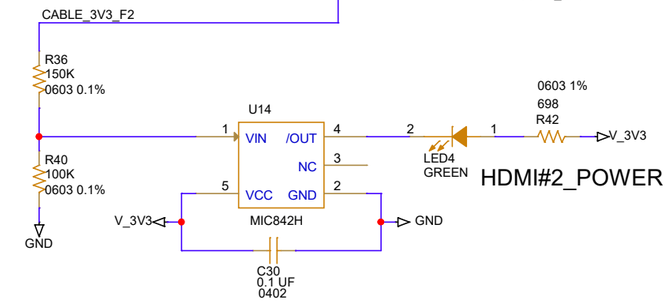
APOLLO CM V3 TEST BOARD		
Title: 05: POWER SUPPLY		
Size	Document Number: 6089-126	Rev: A
Date: Thursday, October 24, 2024	Sheet 6 of 6	



EVEN AND ODD ARE ON OPPOSITE SIDES. JUMPER EVEN-TO-ODD TO LOOP BACK SIGNALS WITHIN A PAIR. JUMPER ADJACENT EVENS AND ODDS TO LOOP BACK DIFFERENTIAL PAIRS



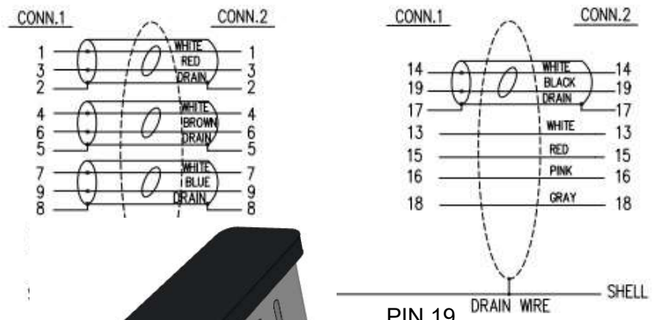


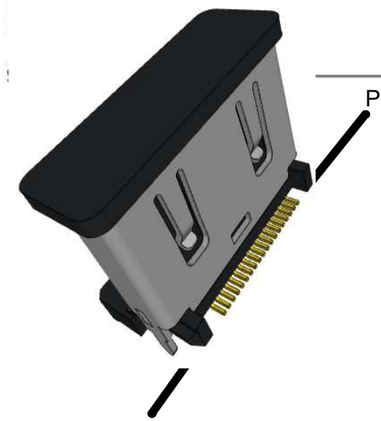


THE THRESHOLD VOLTAGE IS 1.240V. WITH 150K AND 100K RESISTORS, THE OUTPUT WILL GO LOW WHEN THE INPUT EXCEEDS 3.12 VOLTS.

LIMIT THE OUTPUT CURRENT TO LESS THAN 2 MA.

PIN ASSIGNMENT





USING AN HDMI CABLE, THIS CONNECTOR MATES TO THE HDMI CONNECTOR LOCATED ON THE FRONT PANEL OF THE CM. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

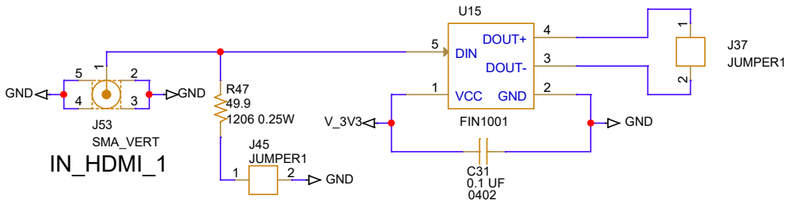
THE "F1_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.

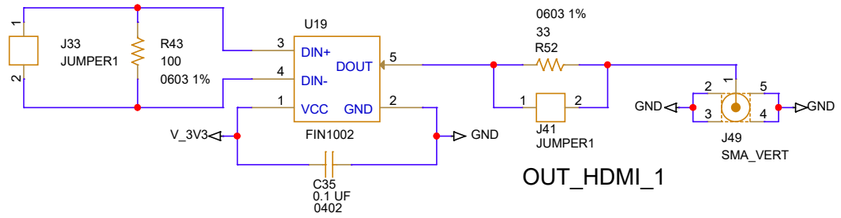
APOLLO CM V3 TEST BOARD

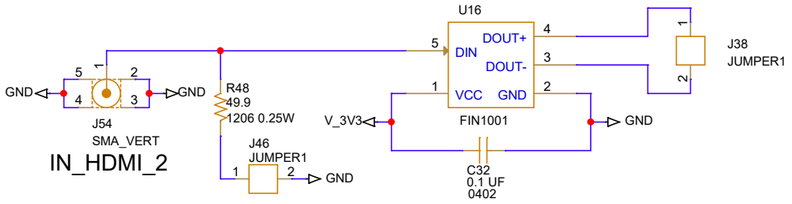
Title: 06: HDMI TEST CONNECTORS

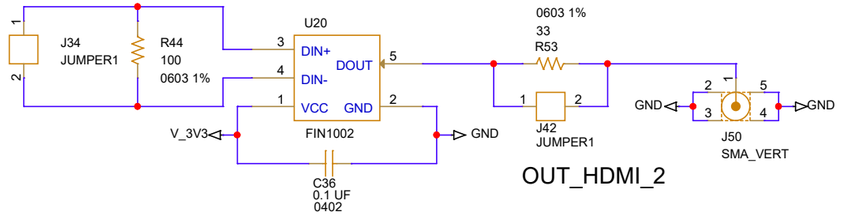
Size | Document Number: 6089-126 | Rev: A

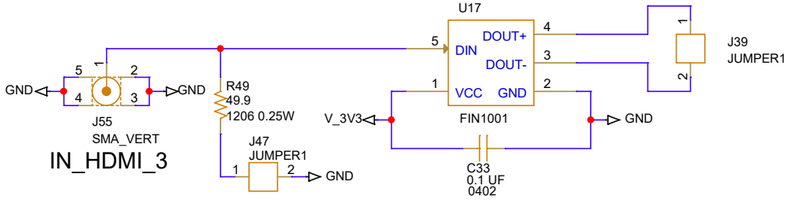
Date: Tuesday, October 29, 2024 | Sheet 6 of 6

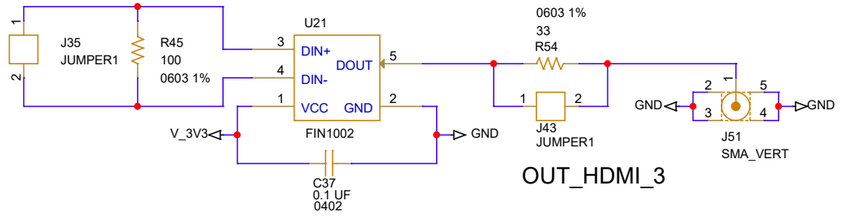


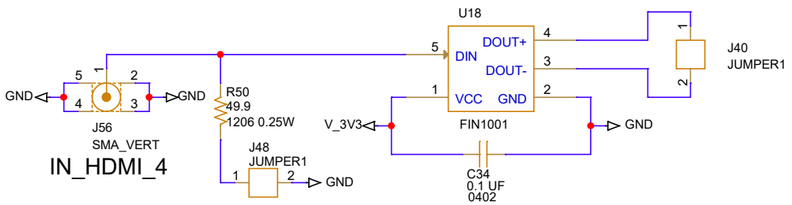


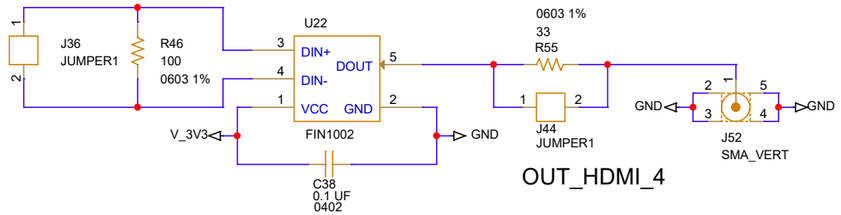












THE DIFFERENTIAL PAIRS IN THE CABLE CAN BE CONNECTED TO INPUT BUFFERS OR TO OUTPUT BUFFERS WITH WIRE-WRAP CONNECTIONS TO THE JUMPER POSTS.

THE INPUTS CAN BE EITHER HIGH-IMPEDANCE OR 50-OHM TERMINATED.

THE OUTPUT DRIVERS ARE LIMITED TO 8 MA, SO OPTIONAL SOURCE-SERIES TERMINATION IS PROVIDED.

APOLLO CM V3 TEST BOARD		
Title: 07: HDMI BUFFERS		
Size	Document Number: 6089-126	Rev: A
Date: Thursday, October 24, 2024	Sheet 6 of 6	