

THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE. ON ANY PAGE, THE NUMBER OF THE CONNECTING PAGE(S) IS SHOWN IN A SMALL NUMBER BELOW THE SIGNAL NAME. PAGE NUMBERS CAN BE FOUND IN SMALL TYPE AT THE BOTTOM OF THE TITLE BLOCK.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY. THE SECTIONS ARE:  
1: NOTES AND BLOCK DIAGRAMS  
2: OFF-BOARD SIGNALS (SM AND FRONT PANEL), GLOBAL CLOCKING, C2C AND TCDS  
3: POWER SOURCES AND CONTROLS  
4: I2C CONTROLS  
5: FPGA#1 POWER AND SIGNAL (NON-MGT)  
6: FPGA#2 POWER AND SIGNAL (NON-MGT)  
7: FPGA#1 GTY TRANSCEIVERS FOR FIREFLY  
8: FPGA#2 GTY TRANSCEIVERS FOR FIREFLY  
9: BETWEEN-FPGA GTY TRANSCEIVERS  
9.99: MECHANICAL PARTS

These are some general signal naming conventions:

- 1) Signals connected to the FPGAs contain either "F1" or "F2".
- 2) Signals connected to the Service Module contain "SM".
- 3) Signals connected to the Front Panel contain "FP".
- 4) Signal names starting with “PG” are “Power Good” signals from power modules.
- 5) Signal names starting with “EN” are “Enable” signals to turn on power modules.
- 6) GTY reference clock names indicate FPGA followed by side (F1L, F1R, F2L, F2R), then the reference clock (R0 or R1), finishing with the sequence order (1 thru 7).
- 7) Power source names start with "V\_", then the voltage with the letter "V" as a decimal point. (V\_3V3 is a 3.3 volt source)
- 8) The MCU I/Os are 3.3 volt and the FPGA I/Os are 1.8 volt. Level shifters are used for the conversion. Signal names on the FPGA side are prefaced with "lov" (low voltage) and signals on the MCU side are prefaced with "hiv" (high voltage).

Make JPG pictures for the block diagrams by displaying them in a PowerPoint slide show that fills the screen. Do a "print screen", then paste it in "paint". Crop, save file, and insert picture.

## TO DO:

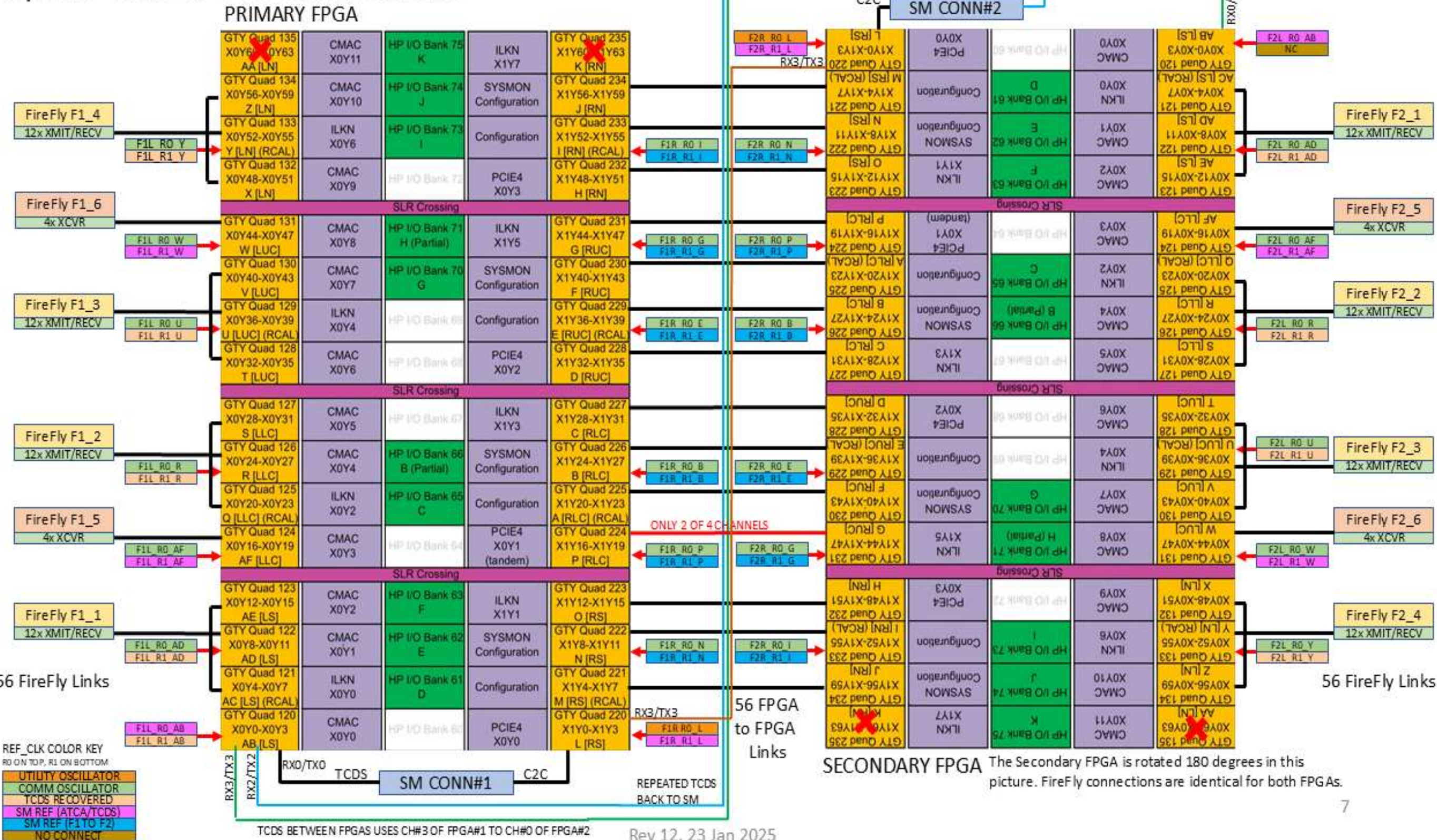
- Consider making page numbers larger
- Update MCU code with new scale factor for 12V current reading
- Update MCU code to accomodate reassigned pins on I2C register chips
- Make design notes on the 5 synth pages match

APOLLO CM v3			
Title			
1.01: NOTES			
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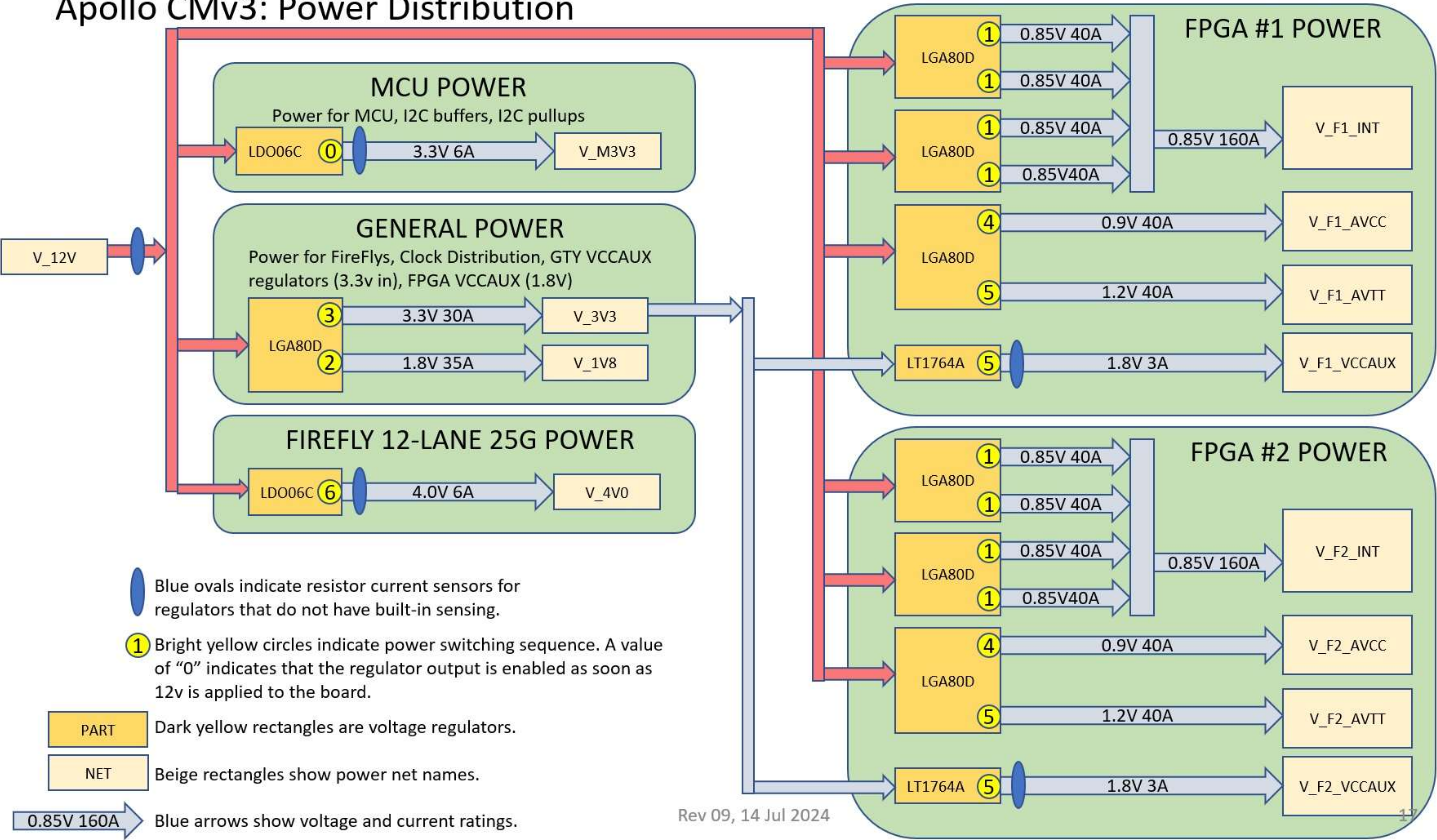


Apollo CMv3: GTY connections





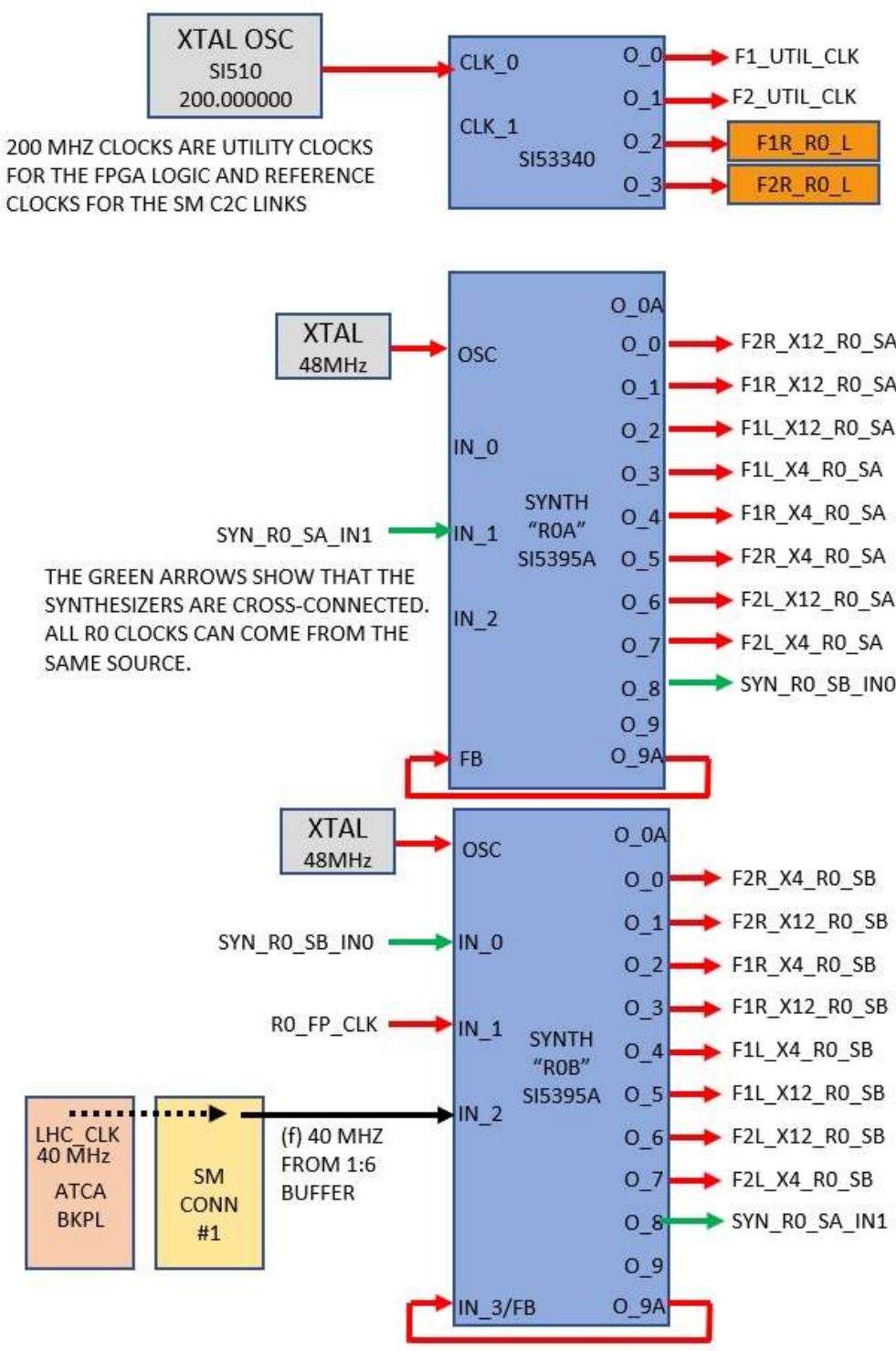
# Apollo CMv3: Power Distribution



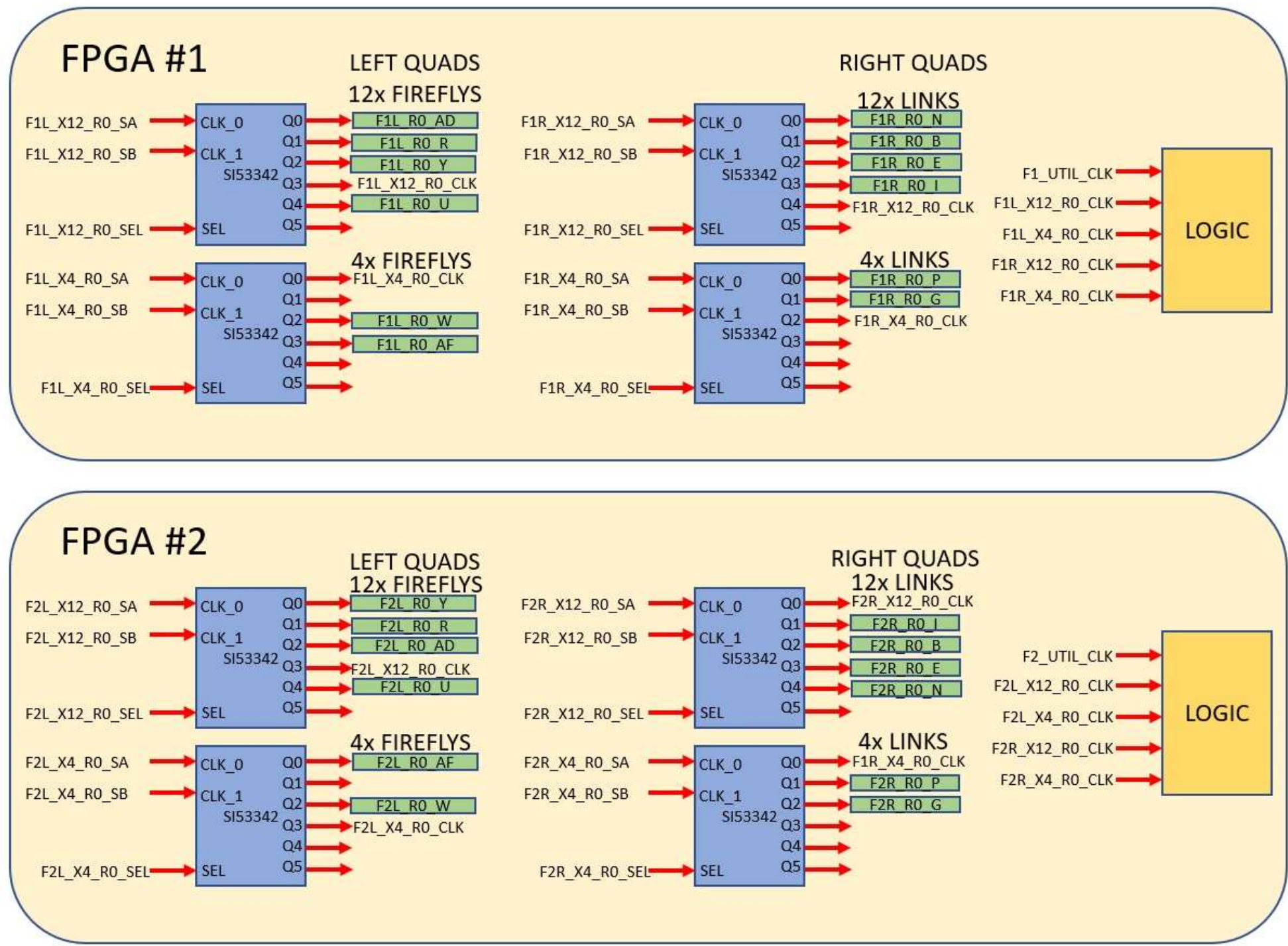
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# Apollo CMv3: Utility Clock / Reference Clock 0 (R0) Distribution



THE REFERENCE CLOCK 0 SYNTHESIZER "B" CAN BE DRIVEN BY A LOCAL CRYSTAL, THE OUTPUT OF SYNTHESIZER "A", THE 40 MHZ LHC CLOCK FROM THE BACKPLANE, OR THE OPTIONAL FRONT PANEL CONNECTOR. THE LHC CLOCK WOULD BE USED FOR SYSTEM-WIDE SYNCHRONOUS COMMUNICATION.

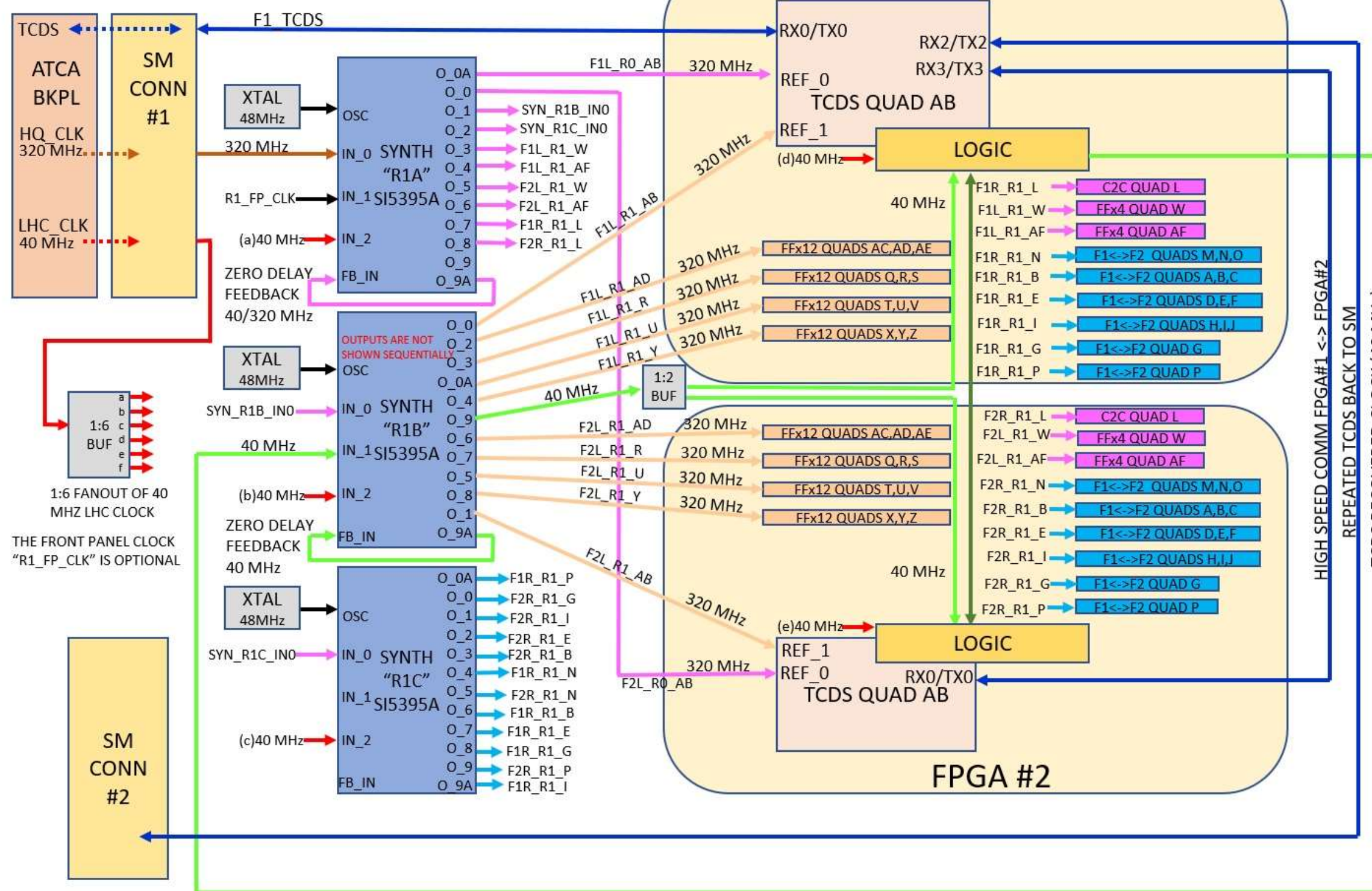


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# Apollo CMv3: External Clock Sources

## ATCA Clock and TCDS Clock/Data



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- GBIT TCDS CLOCK/DATA COMBINED
  - LHC 40 MHz ATCA CLOCK
 

This is the 40 MHz clock passed from the ATCA backplane through the SM. It is fanned out through a 1:6 buffer. The frequency of this clock changes when the LHC is ramping.
  - LHC 320 MHz ATCA CLOCK
 

This is the 320 MHz clock passed from the ATCA backplane through the SM. The frequency of this clock changes when the LHC is ramping.
  - 320 MHz REF CLOCK
 

If the top synthesizer is using the clock on "IN\_0", then these 320 MHz clocks all have zero phase offset relative to the incoming LHC REFERENCE CLOCK signal.
  - 40 MHz TCDS RECOVERED CLOCK
 

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.
  - 320 MHz TCDS RECOVERED CLOCK
 

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.
  - FPGA TO FPGA R1 CLOCK
 

These clocks drive the R1 reference for the FPGA quads that connect to the other FPGA. The frequency follows the 320 MHz REF CLOCK.
  - TTC/TTS DATA/CONTROL
 

These signals possibly contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.
  - OTHER CLOCKS
 

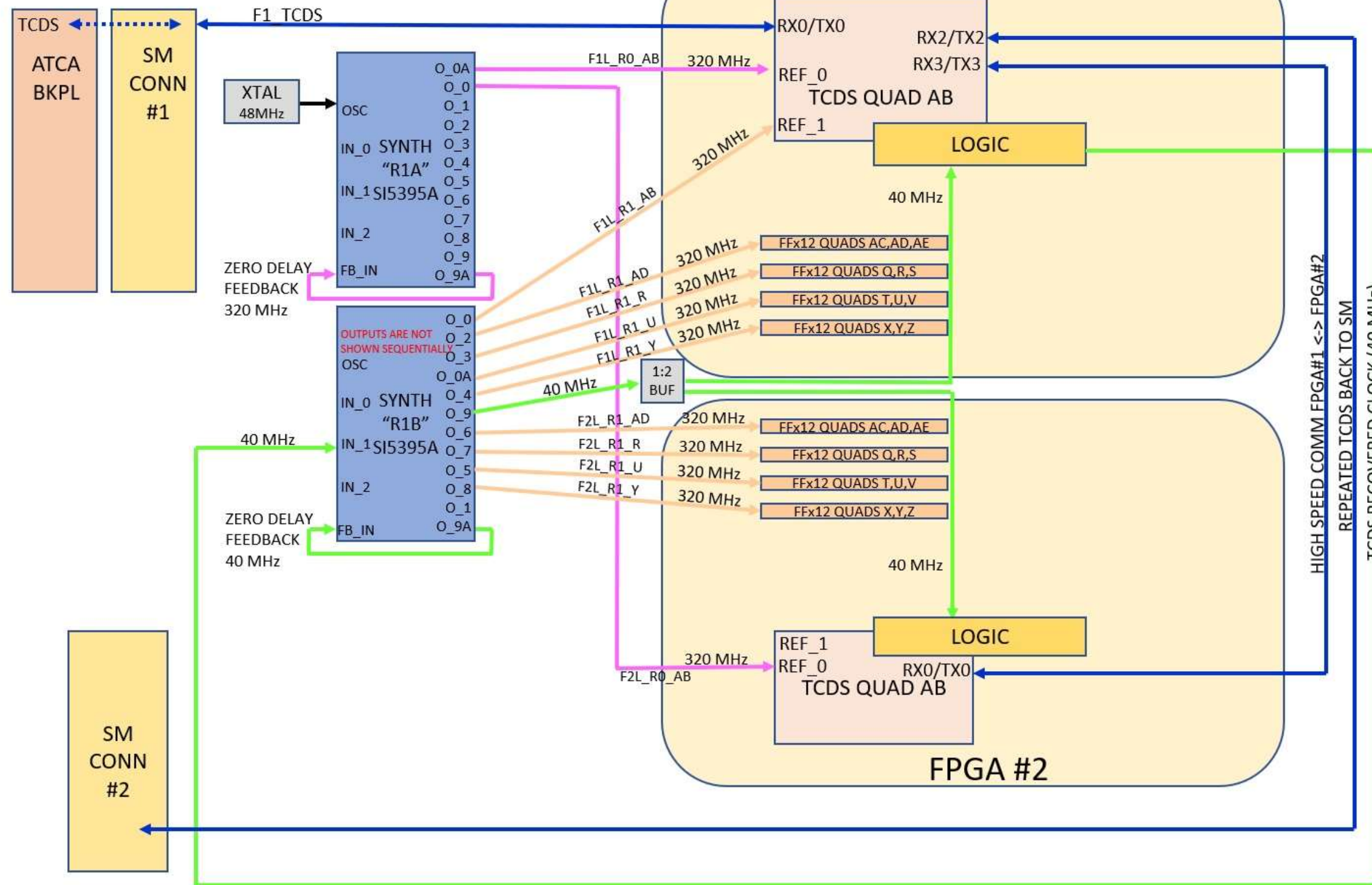
These include the front panel inputs and outputs of various crystal oscillators. These can be used for testing or for adding flexibility to the synthesizer outputs.
- GTU QUADS**
- FFx12 QUADS 12-lane FireFlies. For the IT-DTC, these will be detector facing.
  - FFx4 QUADS 4-lane FireFlies.
  - F1<->F2 QUADS Connections between the two FPGAs.
  - TCDS QUAD Dedicated for TCDS function.



# Apollo CMv3: Full TCDS2

Oscillator provides 320 MHz to extract 40 MHz from TCDS2 stream

FPGA #1

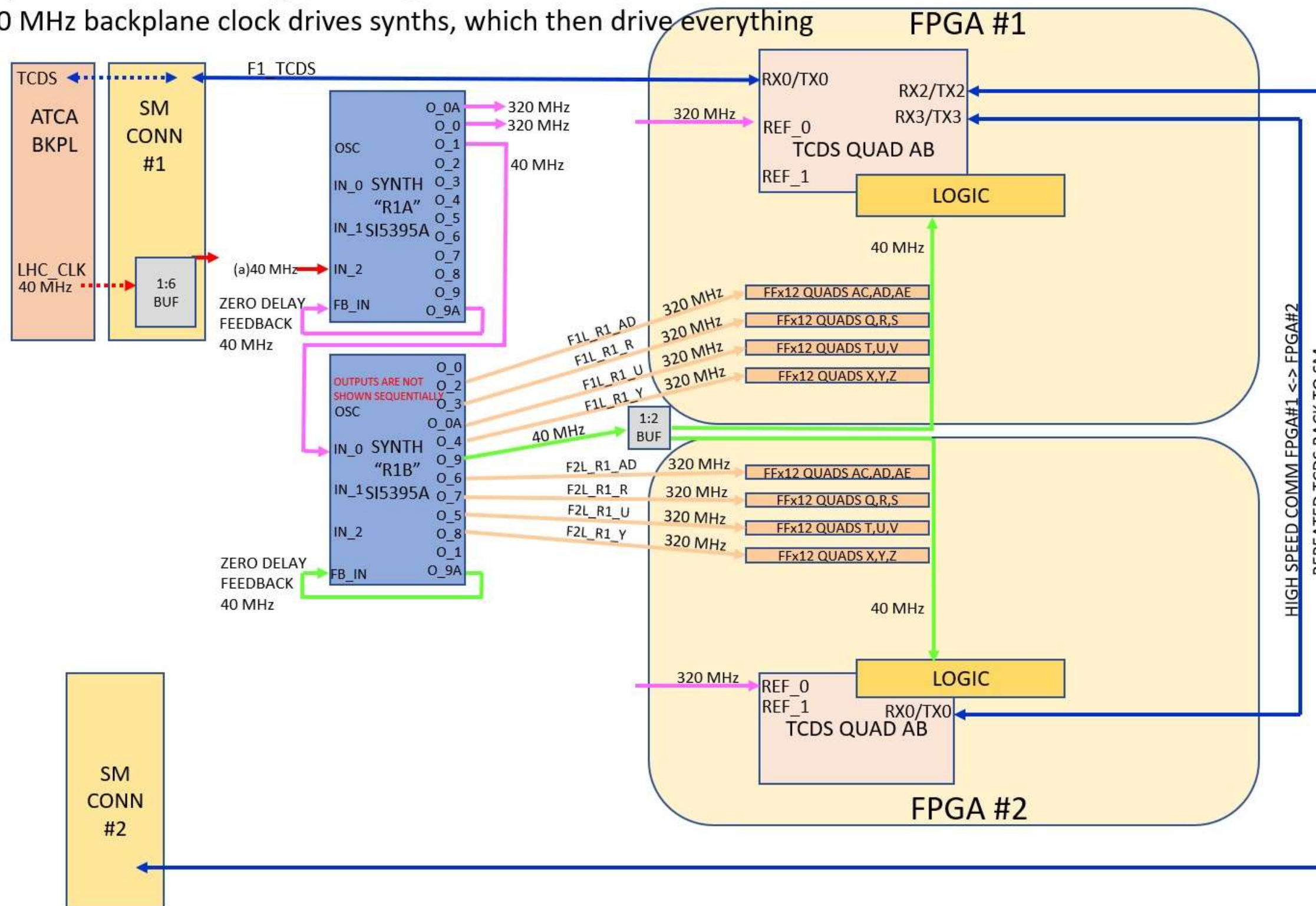


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# Apollo CMv3: Lightweight TCDS2 "A"

40 MHz backplane clock drives synths, which then drive everything

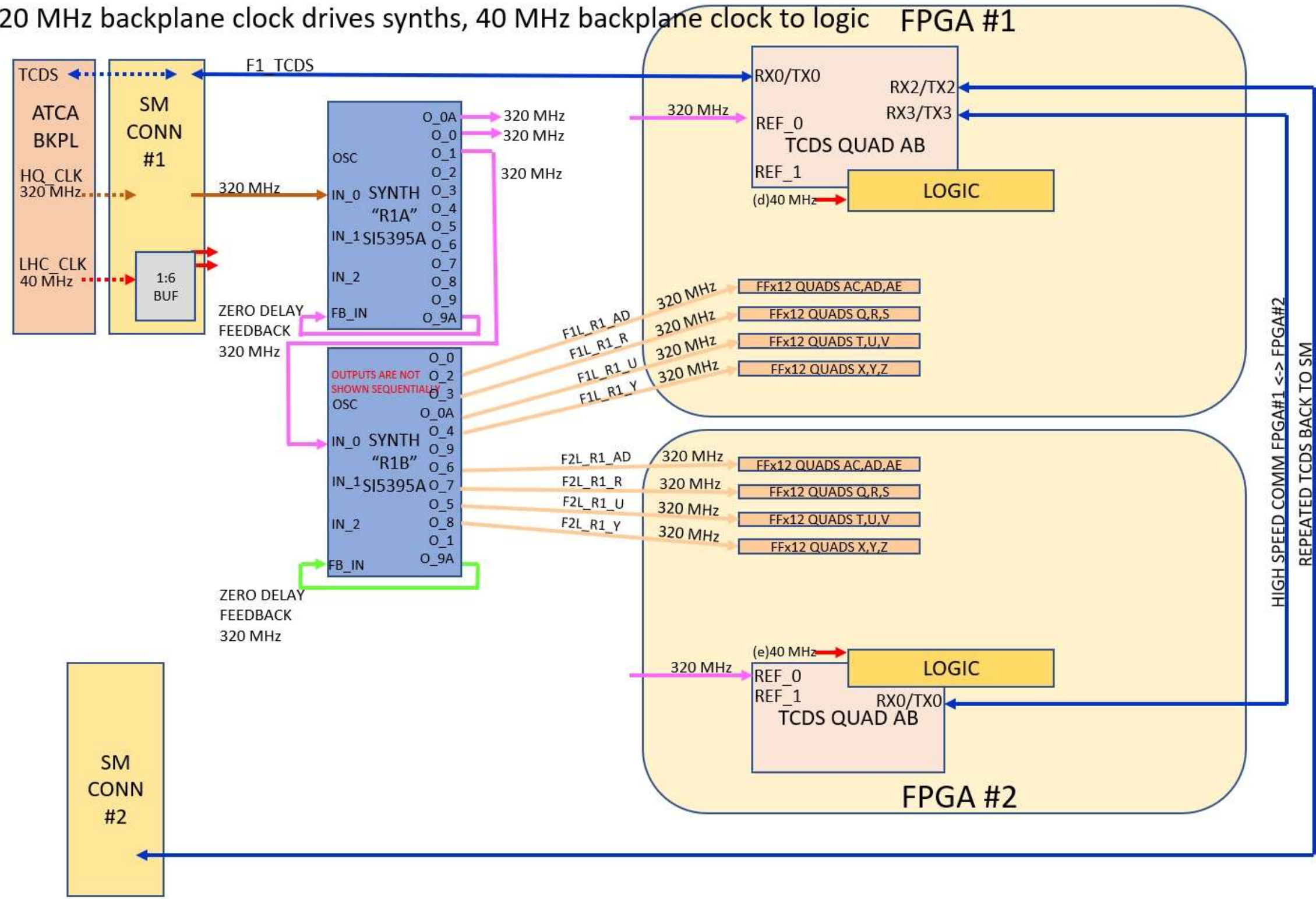


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# Apollo CMv3: Lightweight TCDS2 "B"

320 MHz backplane clock drives synths, 40 MHz backplane clock to logic

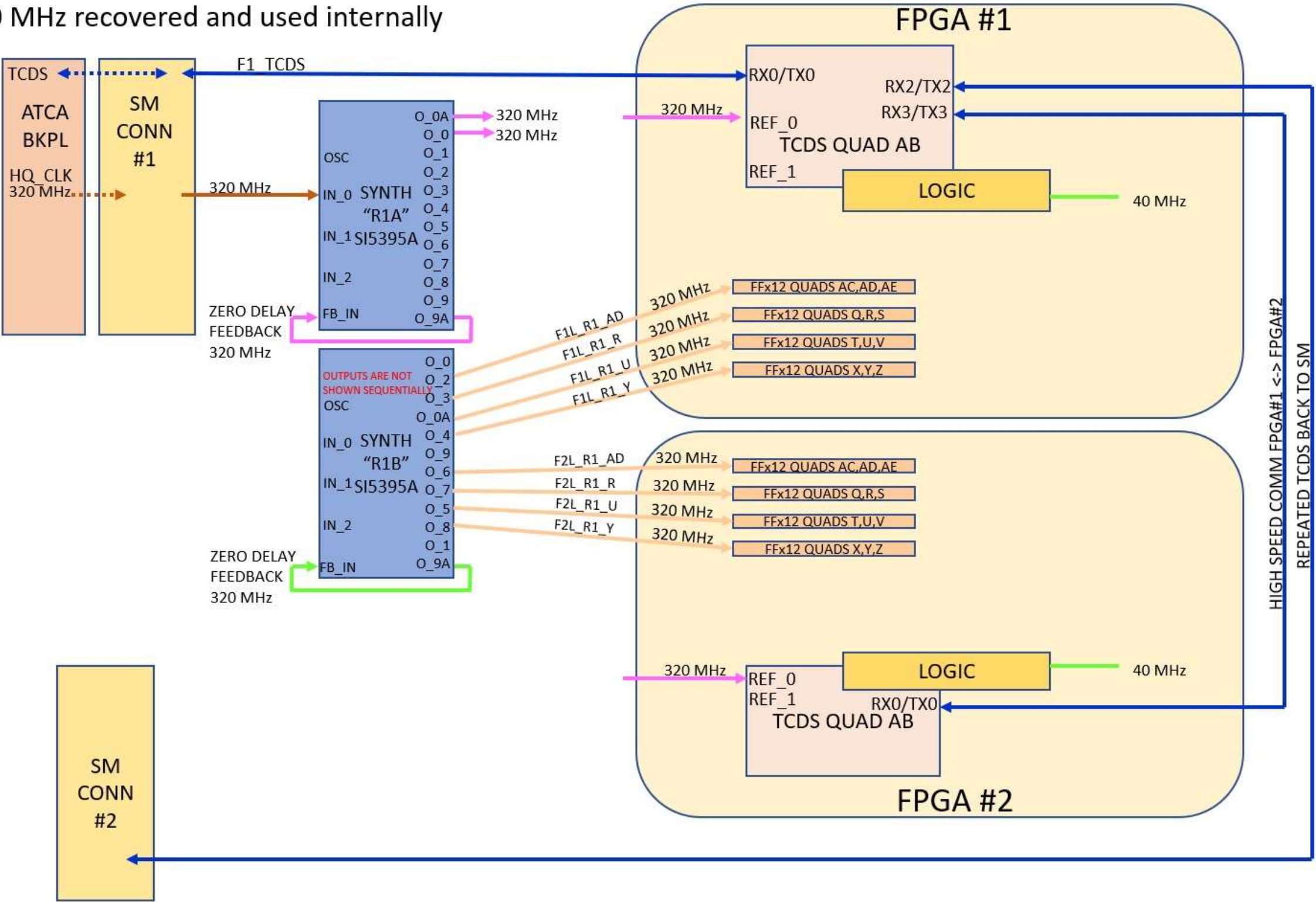


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# Apollo CMv3: Lightweight TCDS2 "C"

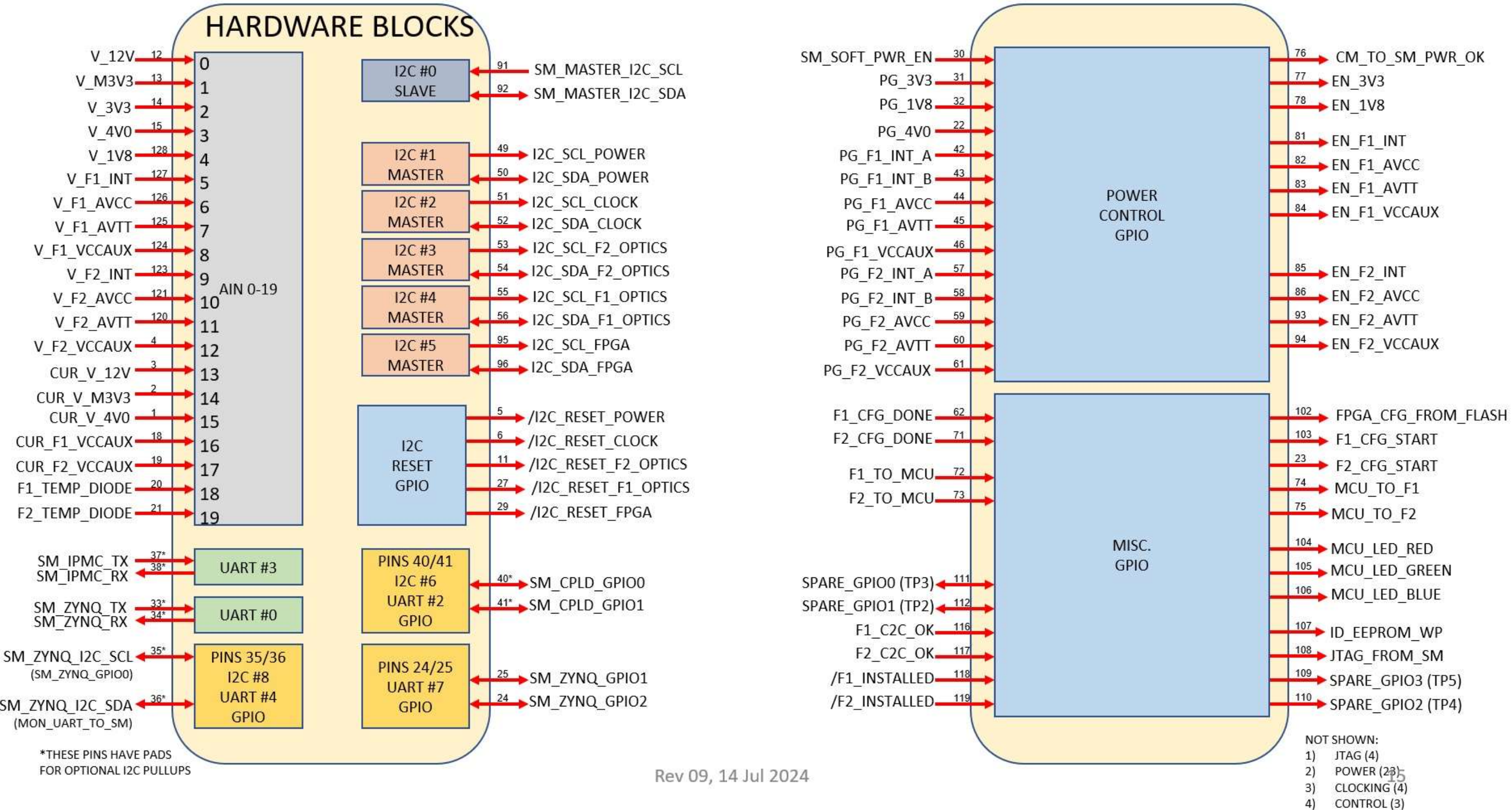
40 MHz recovered and used internally



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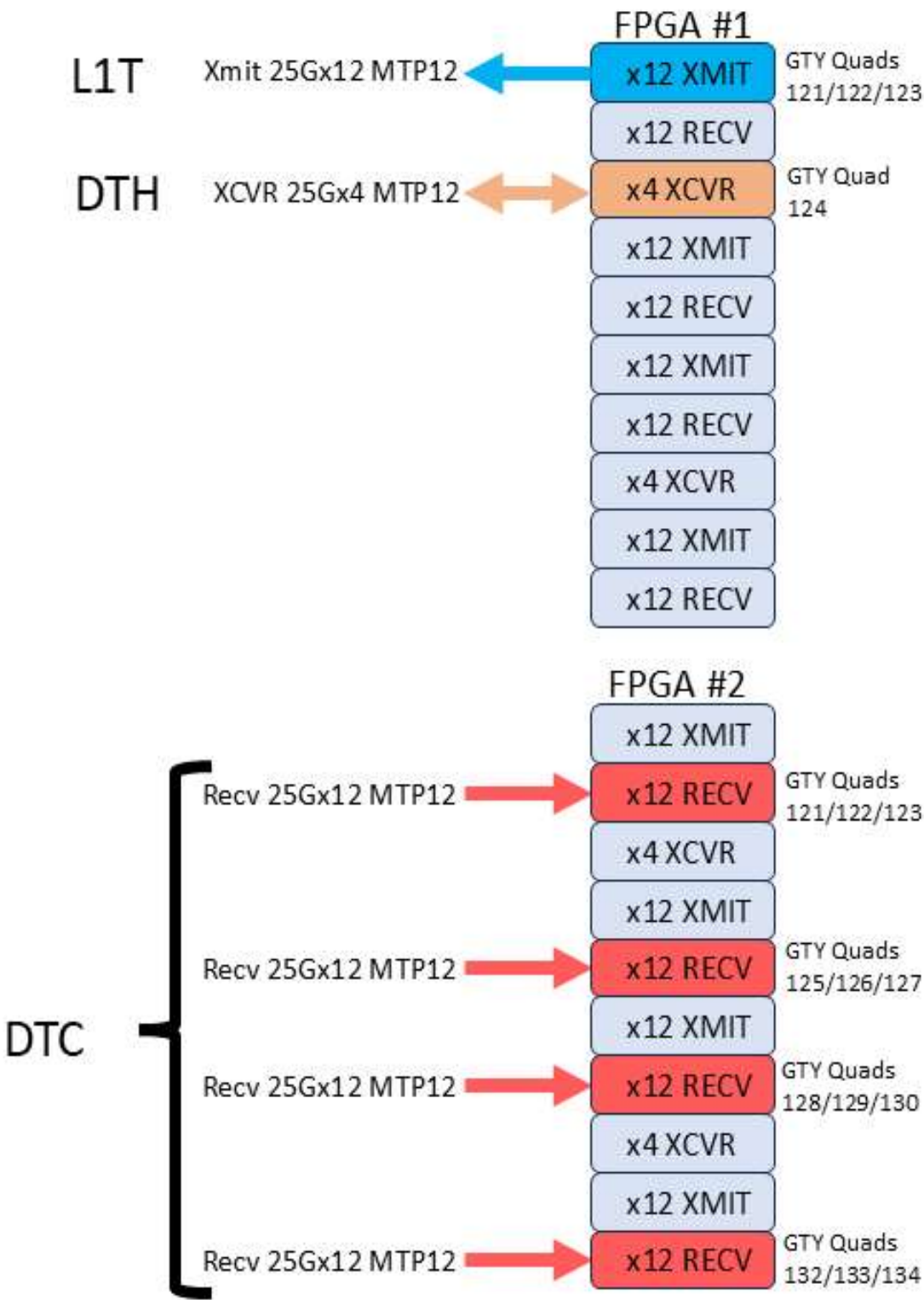
# Apollo CMv3: MCU Connections and Internal Resources



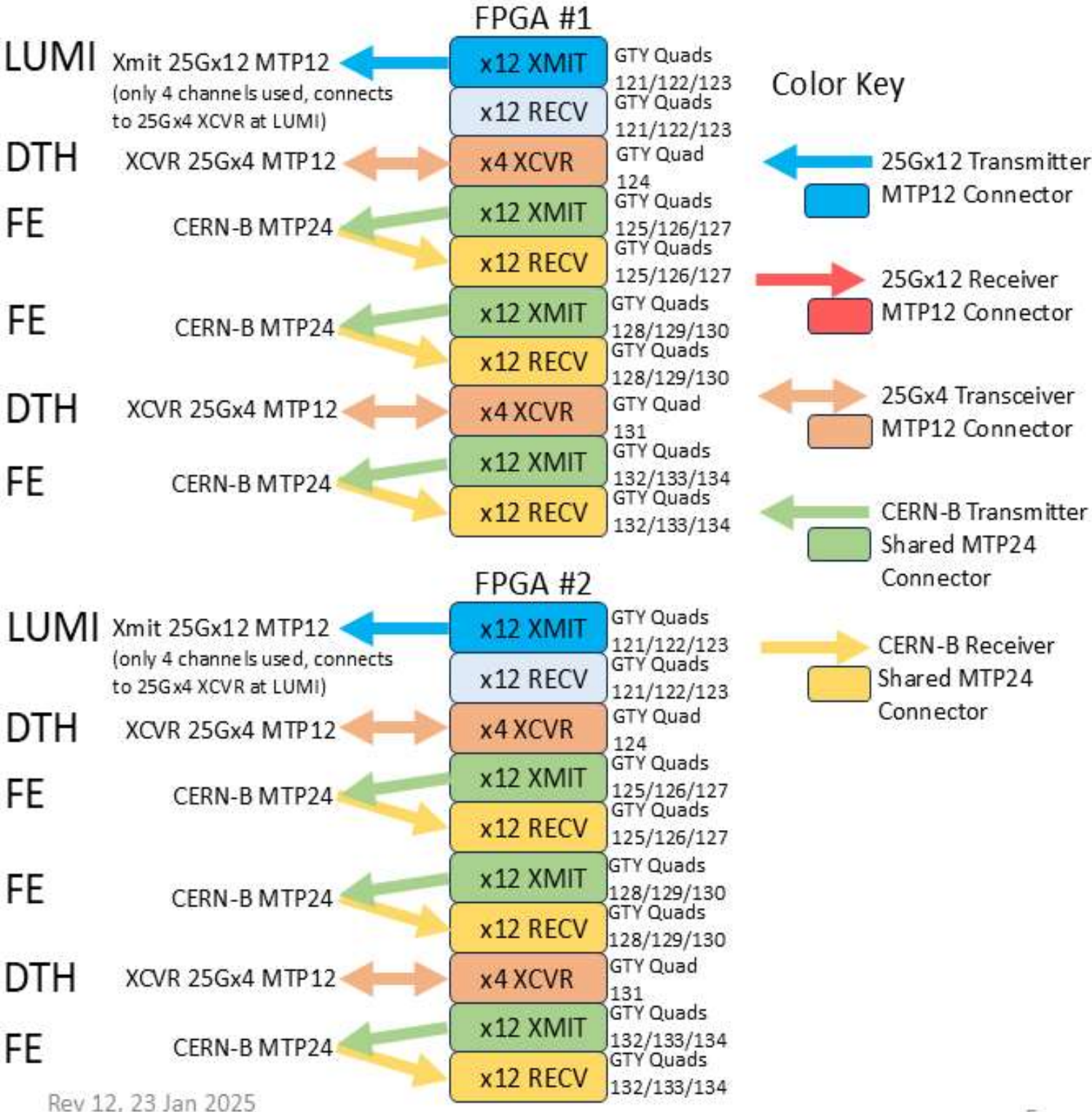
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OT-TF FireFly Site Usage



IT-DTC FireFly Site Usage

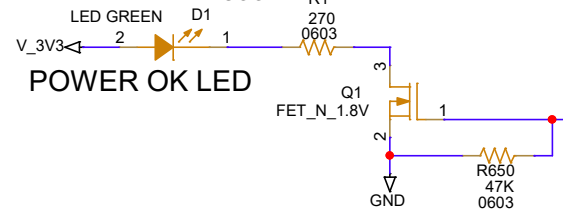


Rev 12, 23 Jan 2025



## 2.01: SM POWER AND CONTROL CONNECTOR

THE "POWER\_OK" SIGNAL WILL BE ASSERTED WHEN THE MCU HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

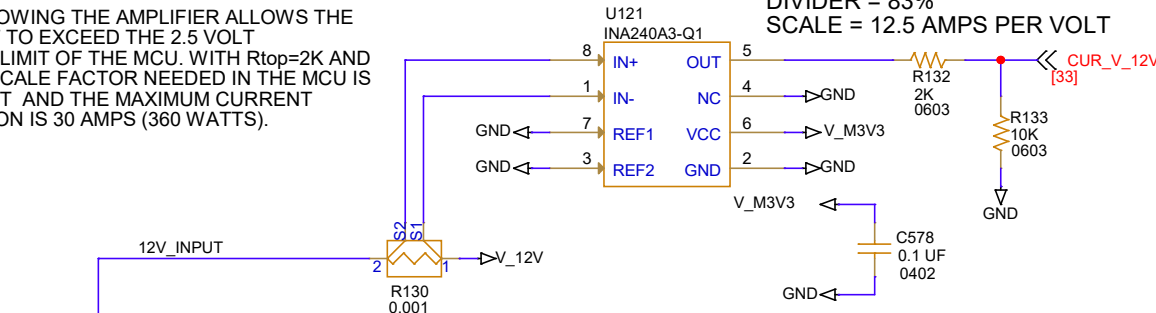


POWER OK LED

V\_12V  
R = 0.001 OHM  
GAIN = 100 V/V  
DIVIDER = 83%  
SCALE = 12.5 AMPS PER VOLT

THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 1 MILLIOHMS AND A CURRENT OF 30 AMPS WILL PRODUCE A VOLTAGE OF 30 MILLIVOLTS. THE SENSE AMPLIFIER HAS A GAIN OF 100, YIELDING 3.0 VOLTS AT 30 AMPS. THIS EQUALS 360 WATTS.

THIS DIVIDER FOLLOWING THE AMPLIFIER ALLOWS THE AMPLIFIER OUTPUT TO EXCEED THE 2.5 VOLT FULL-SCALE INPUT LIMIT OF THE MCU. WITH Rtop=2K AND Rbottom=10K, THE SCALE FACTOR NEEDED IN THE MCU IS 12.5 AMPS PER VOLT AND THE MAXIMUM CURRENT BEFORE SATURATION IS 30 AMPS (360 WATTS).



I2C0 IS A SLAVE INTERFACE. IT IS CONNECTED TO THE IPMC ON THE SM.

I2C8 CAN BE A MASTER OR A SLAVE. IT IS USED TO GET MONITORING DATA INTO THE ZYNQ. ON CMv1, THIS IS THE UART#4 PATH. IT IS CONNECTED TO THE ZYNQ ON THE SM.

I2C6 IS AVAILABLE FOR FUTURE USE. IT IS CONNECTED TO THE CPLD ON THE SM. PULLUPS ARE NOT INSTALLED.

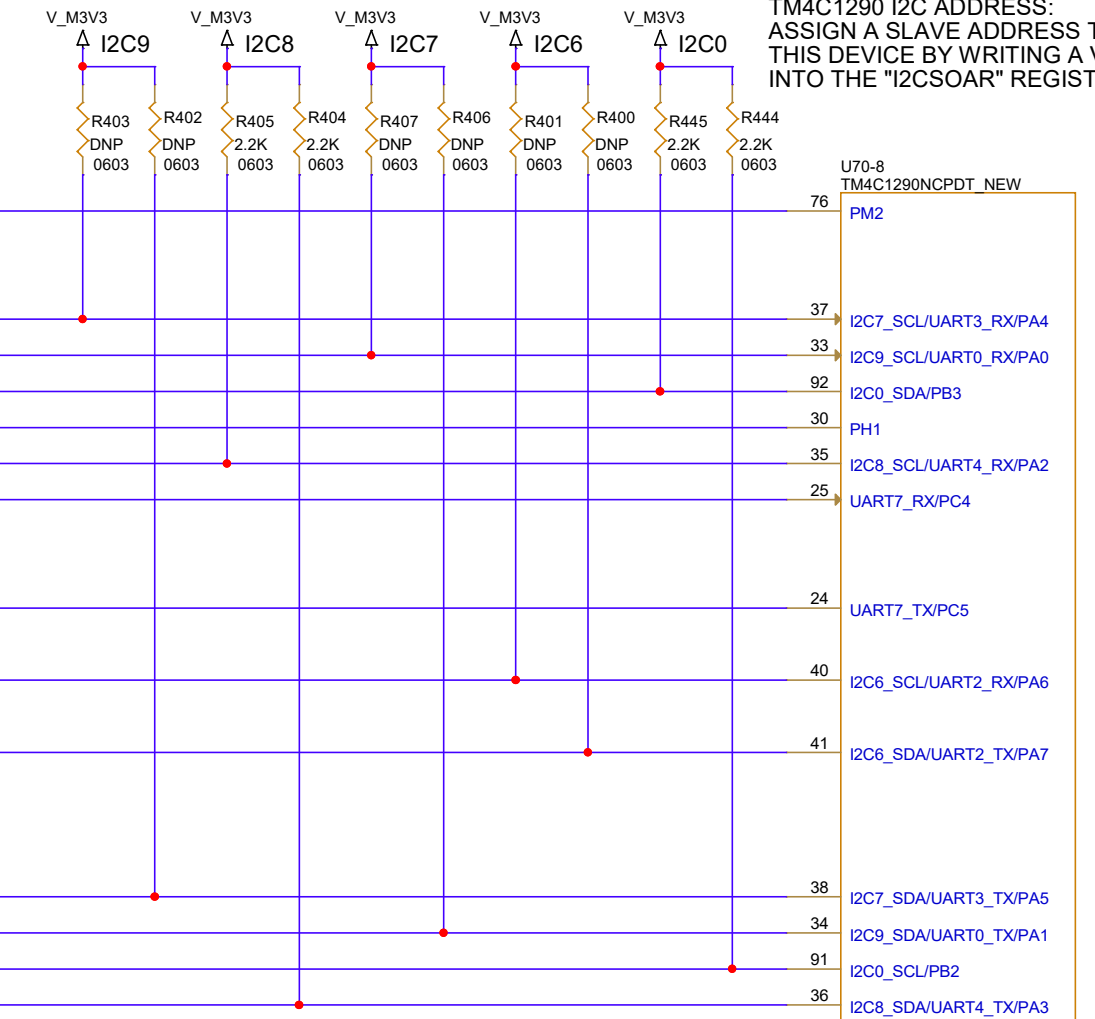
THE I2C7 PINS ARE INITIALLY USED FOR UART#3 CONNECTIONS TO THE IPMC ON THE SM. PULLUPS ARE NOT INSTALLED.

THE I2C9 PINS ARE INITIALLY USED FOR UART#0 CONNECTIONS TO THE ZYNQ ON THE SM. THIS PROVIDES A BOOTLOADER FUNCTION FOR THE MCU. PULLUPS ARE NOT INSTALLED.

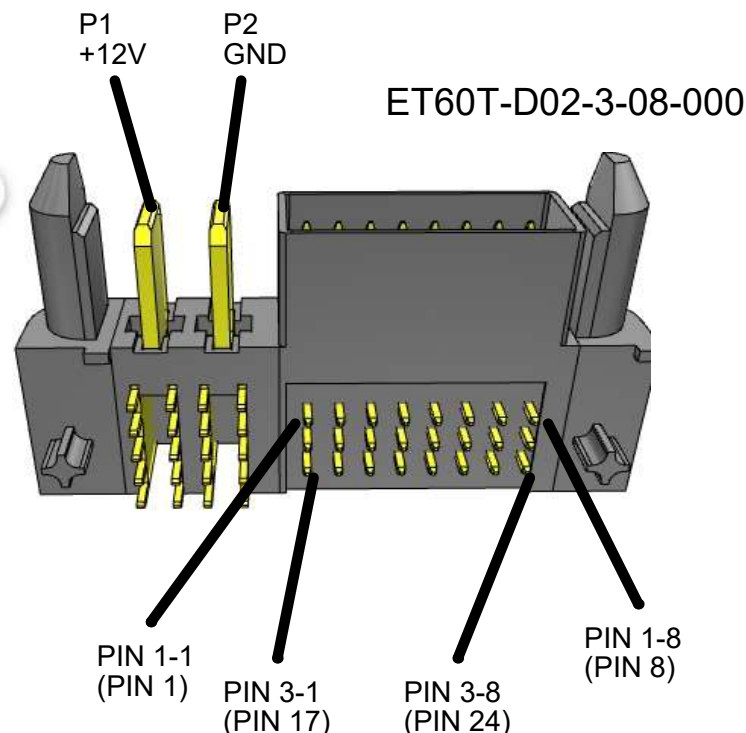
IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH. IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

### TM4C SLAVE I2C ADDR = 0X40

TM4C1290 I2C ADDRESS:  
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.



FOR STANDALONE USB-TO-UART CONNECTION, USE DIGIKEY 768-1015 (FTDI TTL-232R-3V3). CONNECT IT TO AN ADAPTER THAT PLUGS INTO CONNECTOR P1. USE PIN 5 (SM\_ZYNQ\_TX) AND PIN 21 (SM\_ZYNG\_RX).



THESE ARE THE SIGNAL NAMES ON THE SMv2

/PS\_RST IS NOT USED IN THIS DESIGN

ZERO-OHM RESISTORS ON PIN 4 AND PIN 20 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES.

THE SAME IS TRUE FOR THE RESISTORS ON PIN 5 AND PIN 21.

IN ROW 2, PINS 1, 4, 6, AND 8 ARE "GND" ON SMv1. A CMv3 BOARD MUST BE ABLE TO TOLERATE A HARD GND CONNECTION ON THESE PINS IN CASE IT IS CONNECTED TO AN SMv1.

IF THE MCU IS DRIVING AN OUTPUT HIGH, AND THE SIGNAL IS SHORTED TO GND, A 270 OHM RESISTOR WILL LIMIT THE CURRENT TO 12 MA. THE RESISTOR POWER WILL BE 0.04 WATTS.

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Title  
2.01: SM POWER AND CONTROL CONNECTOR

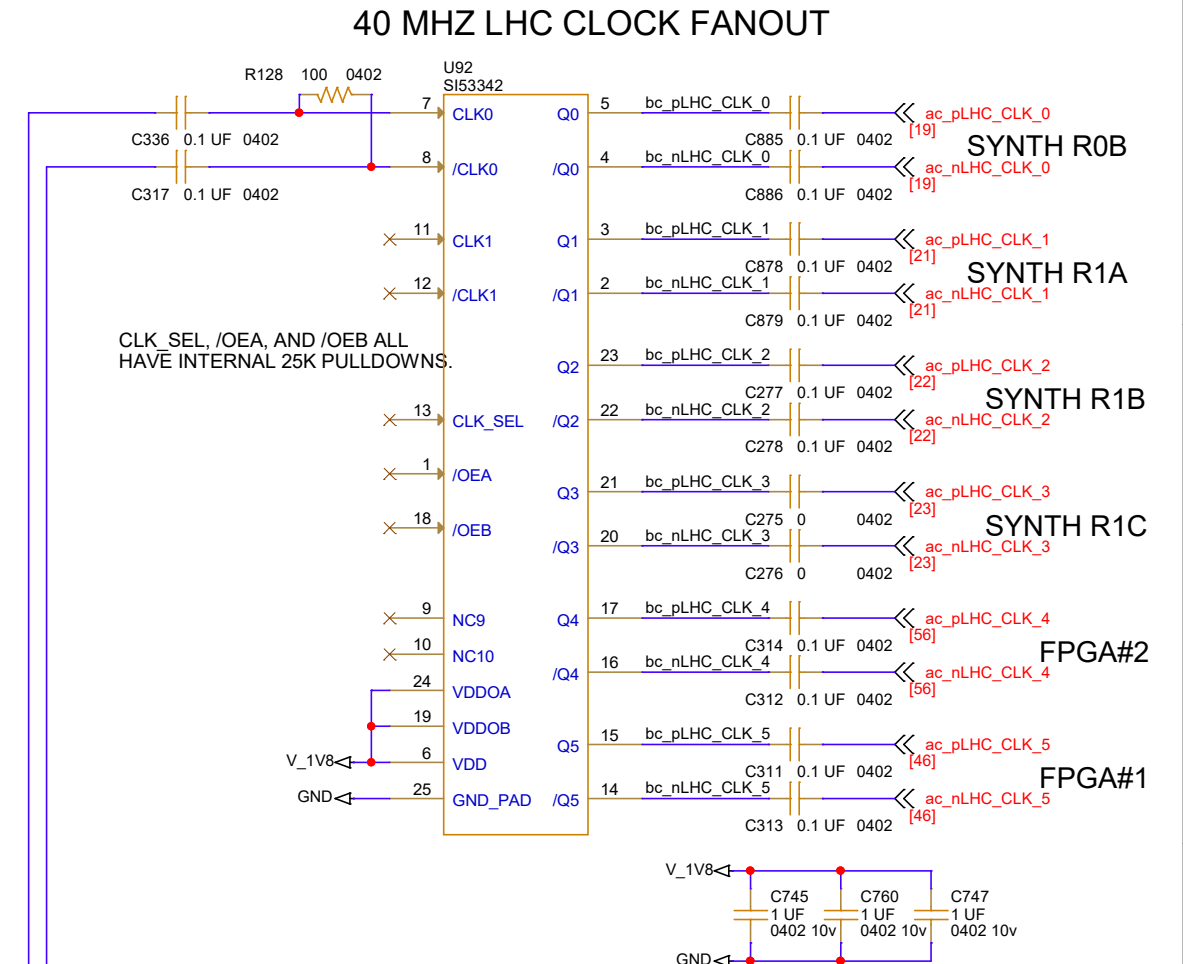
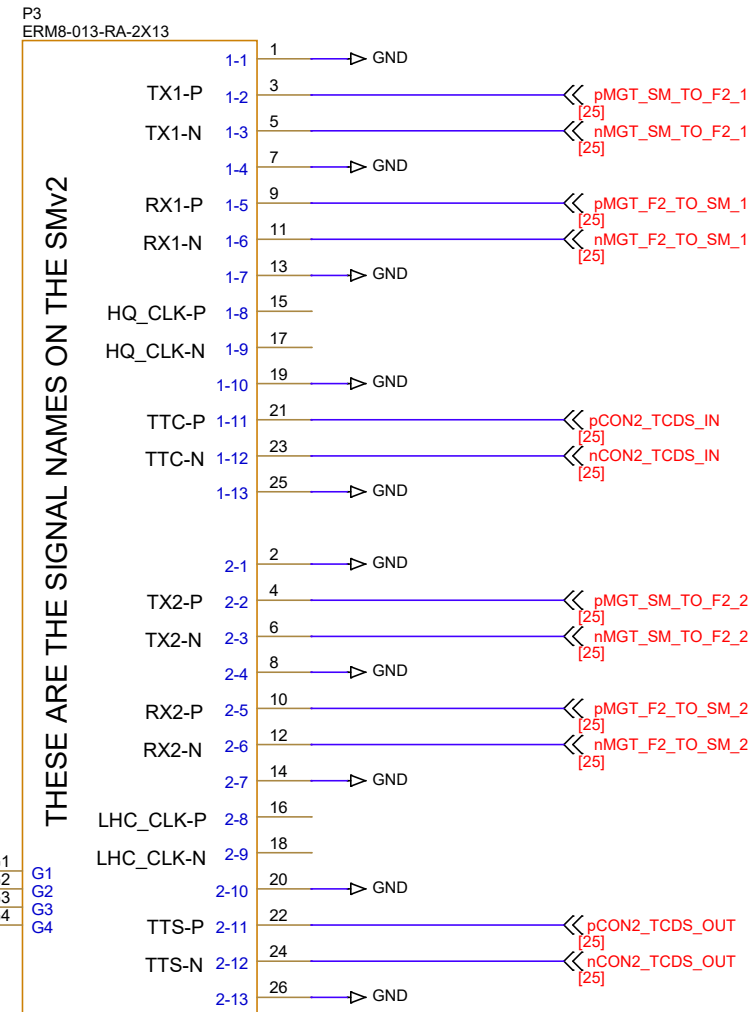
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## 2.02: SM HIGH SPEED CONNECTORS

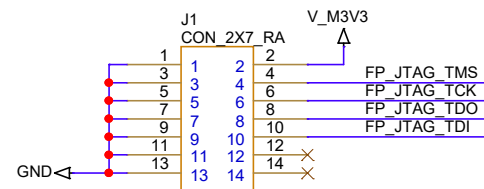
## FPGA#2 SIGNALS





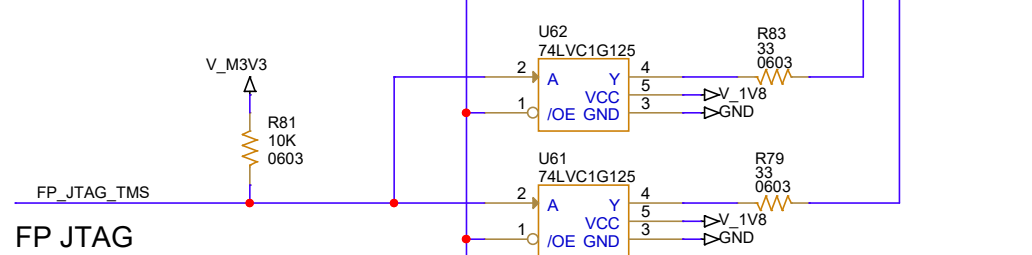
## 2.03: MCU AND FPGA JTAG

THE FPGA JTAG REFERENCE IS 3.3 VOLTS.

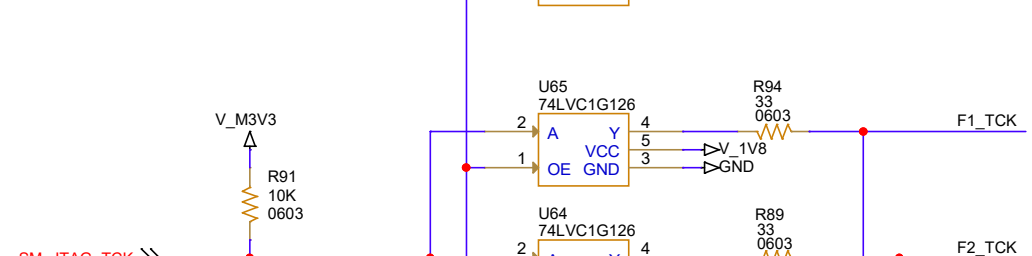


### FRONT PANEL FPGA JTAG

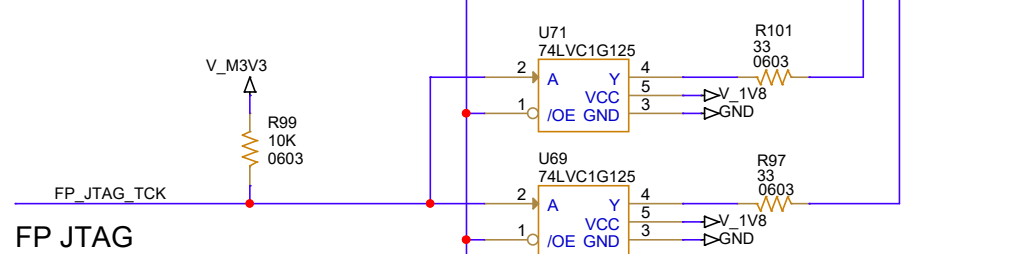
#### SM JTAG



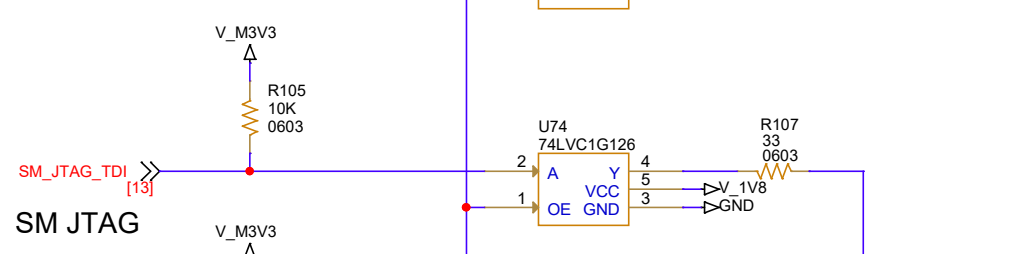
#### FP JTAG



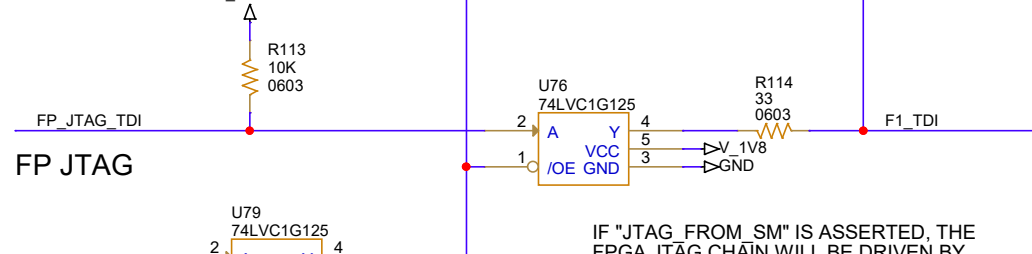
#### SM JTAG



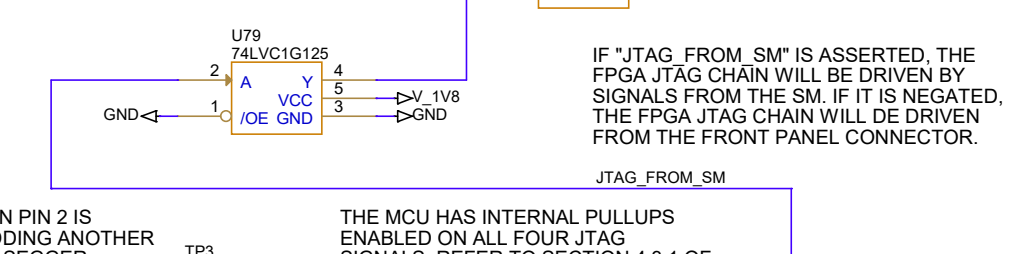
#### FP JTAG



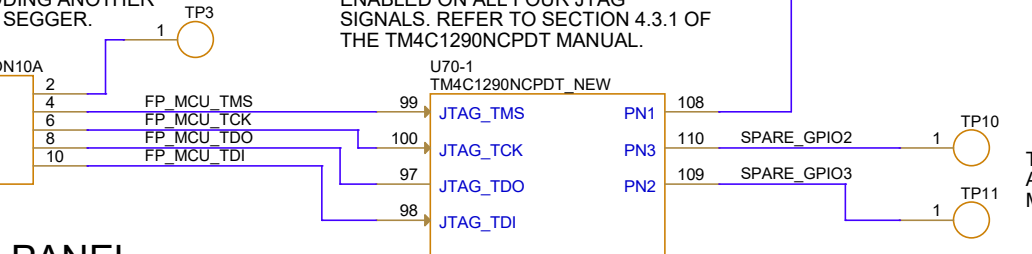
#### SM JTAG



#### FP JTAG



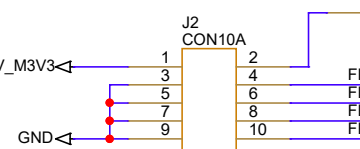
#### SM JTAG



#### FP JTAG



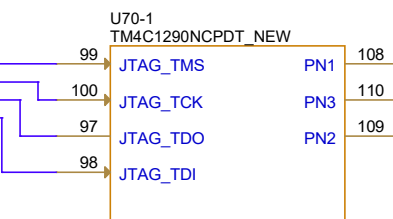
THE TEST POINT ON PIN 2 IS AVAILABLE FOR ADDING ANOTHER SIGNAL FROM THE SEGGER.



### FRONT PANEL MCU JTAG

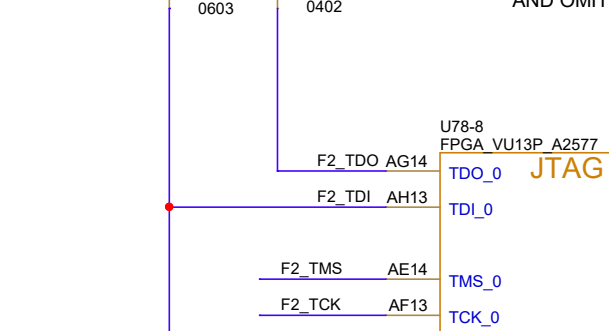
THE MCU CAN BE RUN IN "JTAG" MODE OR "ARM SWD" MODE.

THE MCU HAS INTERNAL PULLUPS ENABLED ON ALL FOUR JTAG SIGNALS. REFER TO SECTION 4.3.1 OF THE TM4C1290NCPDT MANUAL.



IF "JTAG\_FROM\_SM" IS ASSERTED, THE FPGA JTAG CHAIN WILL BE DRIVEN BY SIGNALS FROM THE SM. IF IT IS NEGATED, THE FPGA JTAG CHAIN WILL BE DRIVEN FROM THE FRONT PANEL CONNECTOR.

#### BYPASS

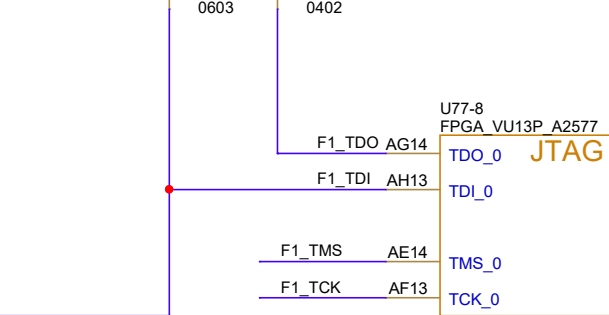


#### FPGA#2 JTAG BYPASS

IF THE FPGA IS INSTALLED AND PART OF THE JTAG CHAIN, INSTALL 0.0 OHM AT "IN CHAIN" SITE, AND OMIT 0.0 OHM AT "BYPASS" SITE.

IF THE FPGA IS NOT INSTALLED, INSTALL 0.0 OHM AT "BYPASS" SITE, AND OMIT 0.0 OHM AT "IN CHAIN" SITE.

#### BYPASS



#### FPGA#1 JTAG BYPASS

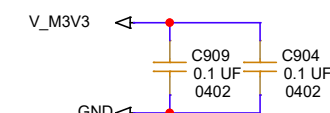
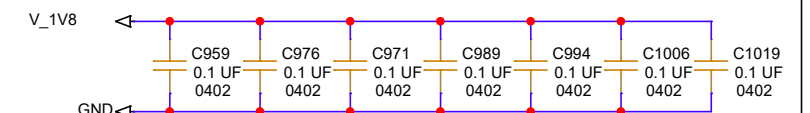
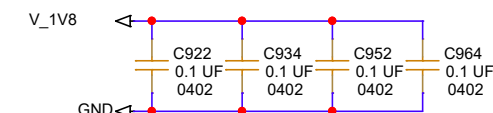
### FPGA#2

### FPGA#1

#### FP JTAG

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE SM OR THE EXTERNAL PROGRAMMER.

#### SM JTAG



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#### 2.03: MCU AND FPGA JTAG

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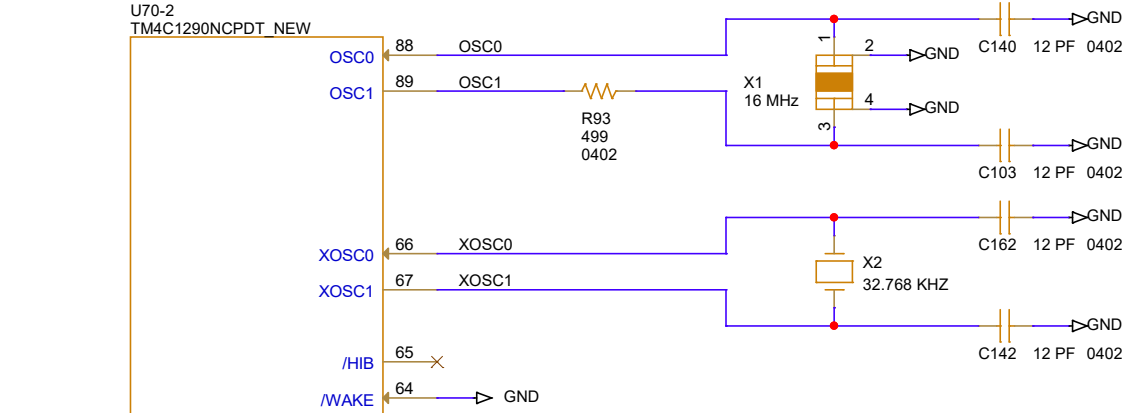
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2.04: MCU I/O AND POWER



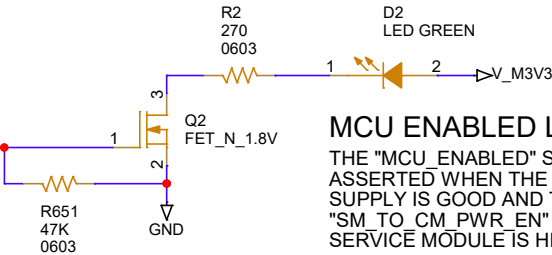
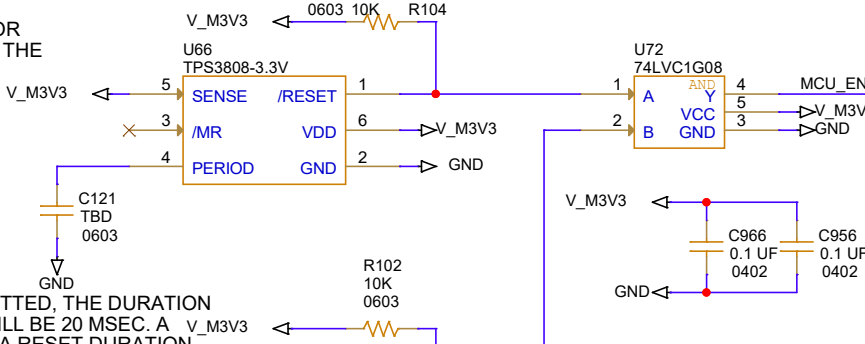
AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "/WAKE" PIN GET TIED TO GND AND "/HIB" IS NC.

THE ACTIVE-LO "/RESET" INPUT WILL BE ASSERTED WHEN EITHER OF THE FOLLOWING ARE TRUE:  
1) POWER HAS JUST BEEN APPLIED  
2) THE SERVICE MODULE IS ATTACHED AND IS HOLDING "SM\_TO\_CM\_PWR\_EN" LO.

IF THE SERVICE MODULE IS NOT ATTACHED, THE PULLUP RESISTOR ON "SM\_TO\_CM\_PWR\_EN" WILL ASSERT THAT SIGNAL AND ALLOW THE BOARD TO POWER UP.

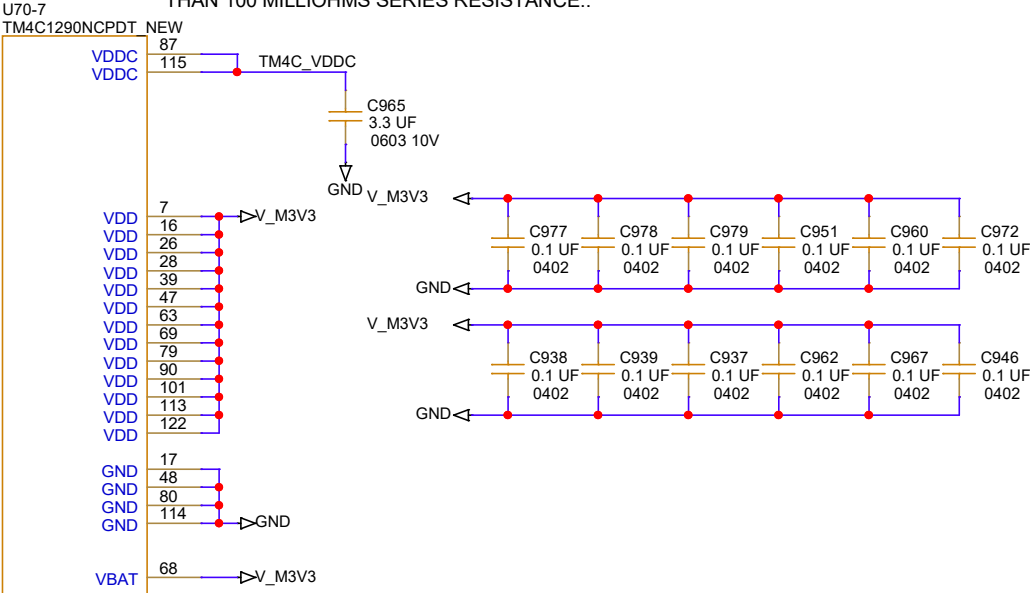
IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

SM\_TO\_CM\_PWR\_EN [13]



MCU ENABLED LED  
THE "MCU\_ENABLED" SIGNAL WILL BE ASSERTED WHEN THE 3.3V MANAGEMENT SUPPLY IS GOOD AND THE "SM\_TO\_CM\_PWR\_EN" SIGNAL FROM THE SERVICE MODULE IS HIGH.

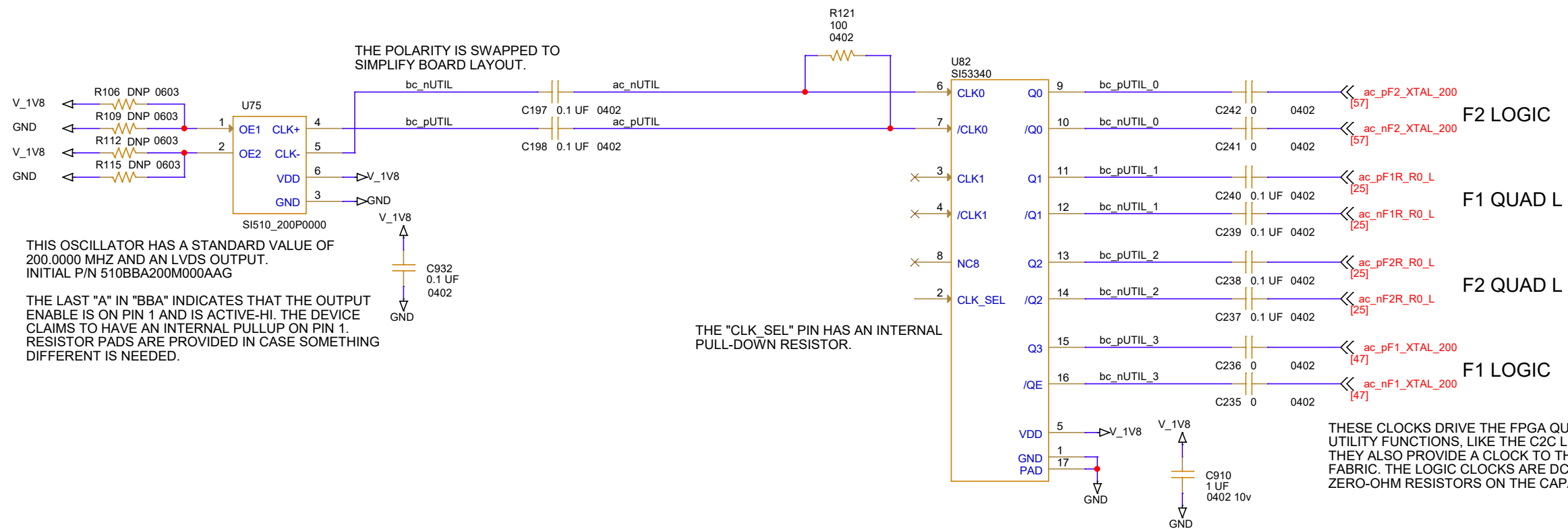
AS PER TABLE 26.15 OF THE TM4C1290 MANUAL, THE "VDDC" PINS GET TIED TOGETHER AND CONNECTED TO A CAPACITOR BETWEEN 2.5 UF AND 4 UF WITH LESS THAN 100 MILLIOHMS SERIES RESISTANCE..



AS PER TABLE 25.7 OF THE TM4C1290 MANUAL, THE UNUSED "VBAT" PIN GET TIED TO VDD.

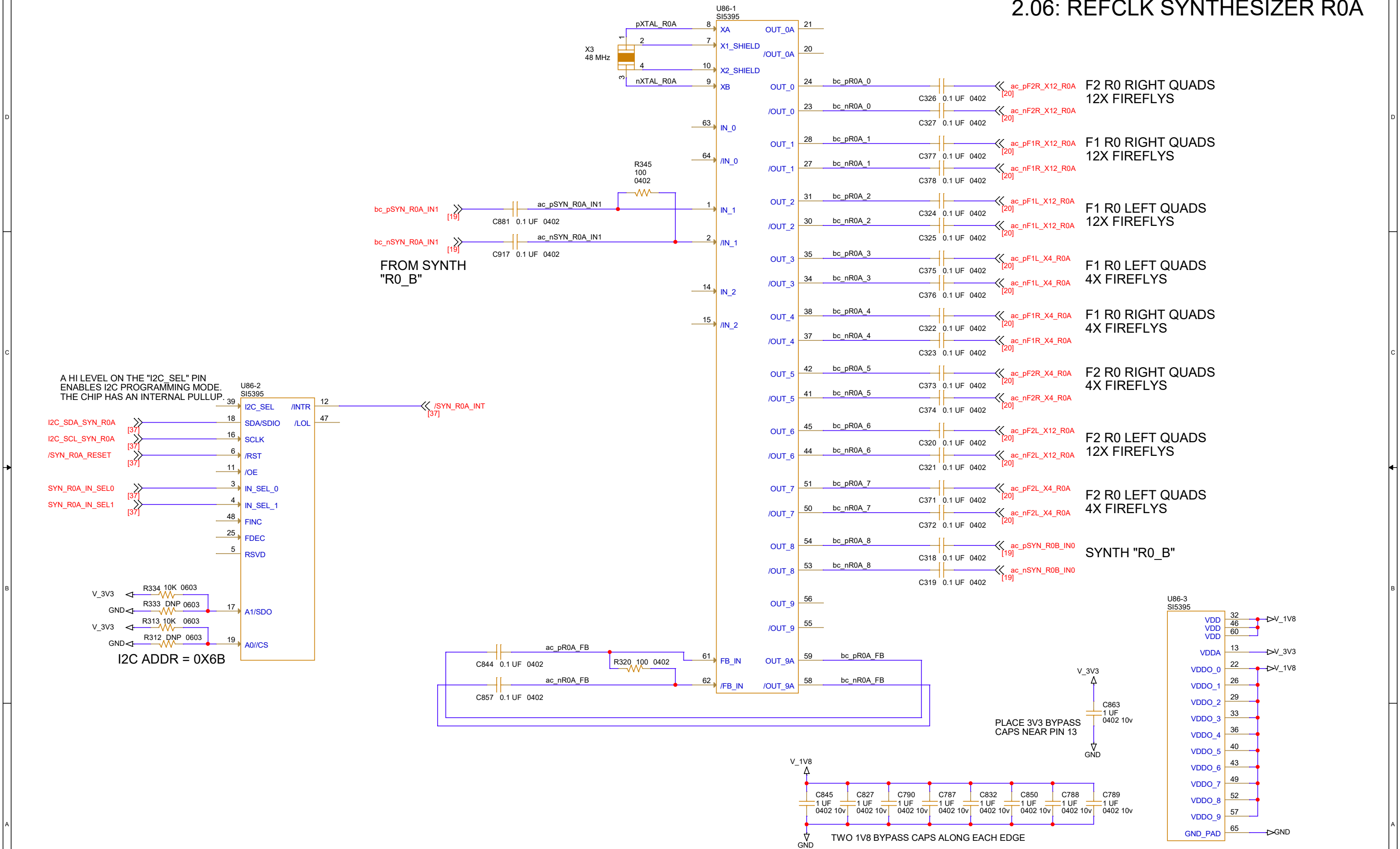


## 2.05: UTILITY CLOCK



THESE CLOCKS DRIVE THE FPGA QUADS USED FOR UTILITY FUNCTIONS, LIKE THE C2C LINK TO THE SM. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC. THE LOGIC CLOCKS ARE DC-COUPLED, WITH ZERO-OHM RESISTORS ON THE CAPACITOR PADS.

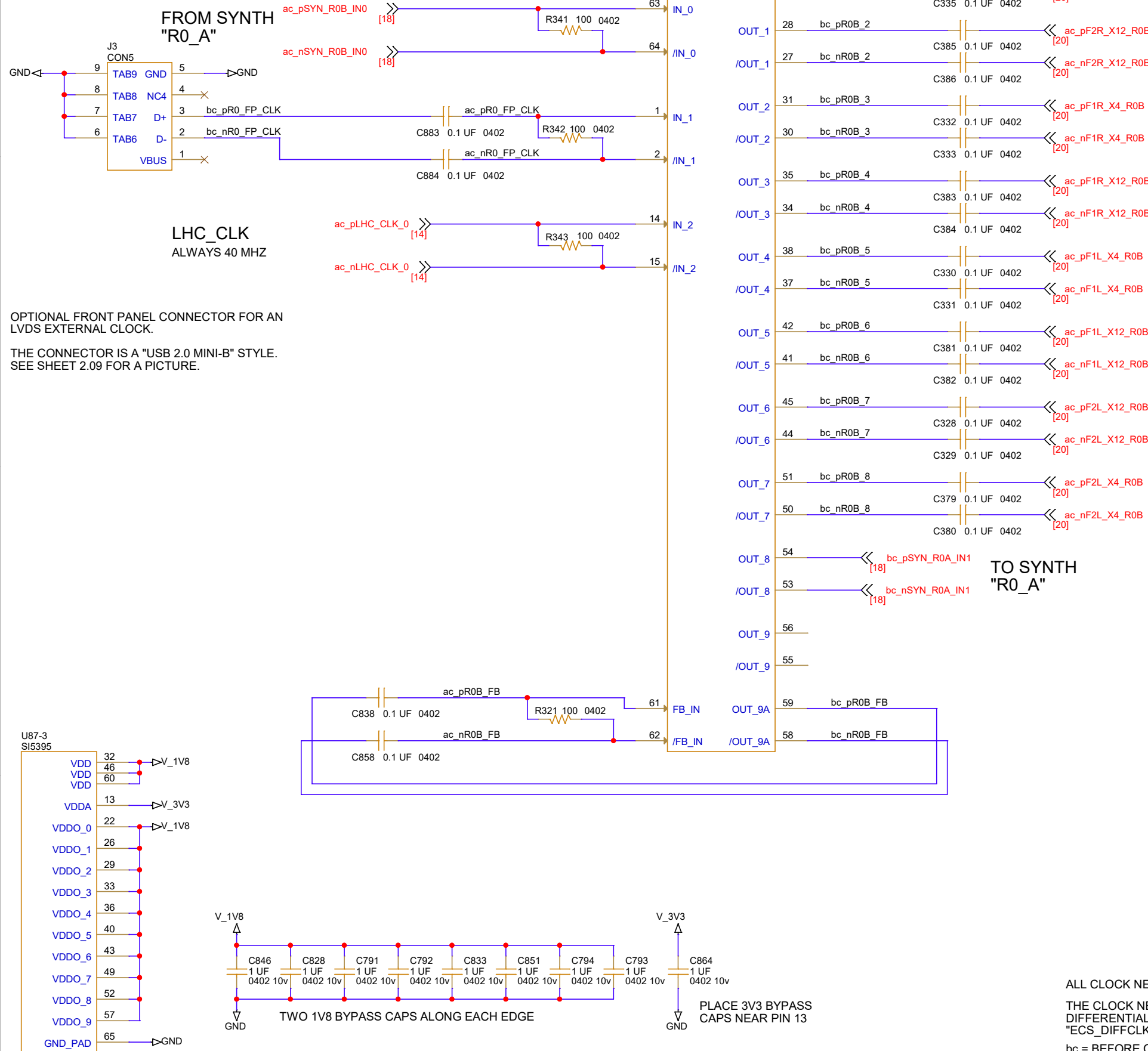
2.06: REFCLK SYNTHESIZER R0A





## 2.07: REFCLK SYNTHESIZER R0B

THE REFERENCE CLOCK 0 SYNTHESIZER "B" CAN BE DRIVEN BY A LOCAL CRYSTAL, THE OUTPUT OF SYNTHESIZER "A", THE 40 MHZ LHC CLOCK FROM THE BACKPLANE, OR THE OPTIONAL FRONT PANEL CONNECTOR. THE LHC CLOCK WOULD BE USED FOR SYSTEM-WIDE SYNCHRONOUS COMMUNICATION.



F2 R0 RIGHT QUADS  
4X FIREFLYS

F2 R0 RIGHT QUADS  
12X FIREFLYS

F1 R0 RIGHT QUADS  
4X FIREFLYS

F1 R0 RIGHT QUADS  
12X FIREFLYS

F1 R0 LEFT QUADS  
4X FIREFLYS

F1 R0 LEFT QUADS  
12X FIREFLYS

F2 R0 LEFT QUADS  
12X FIREFLYS

F2 R0 LEFT QUADS  
4X FIREFLYS

A HI LEVEL ON THE "I2C\_SEL" PIN  
ENABLES I2C PROGRAMMING MODE.  
THE CHIP HAS AN INTERNAL PULLUP.

A LOW LEVEL ON THE "/OE" PIN WILL  
ENABLE THE OUTPUTS. THE CHIP  
HAS AN INTERNAL PULLDOWN.

THE "FINC" AND "FDEC" PINS HAVE  
INTERNAL PULLDOWNS AND CAN  
BE LEFT UNCONNECTED.

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO  
DIFFERENTIAL PAIRS, AND MUST BE PART OF THE  
"ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

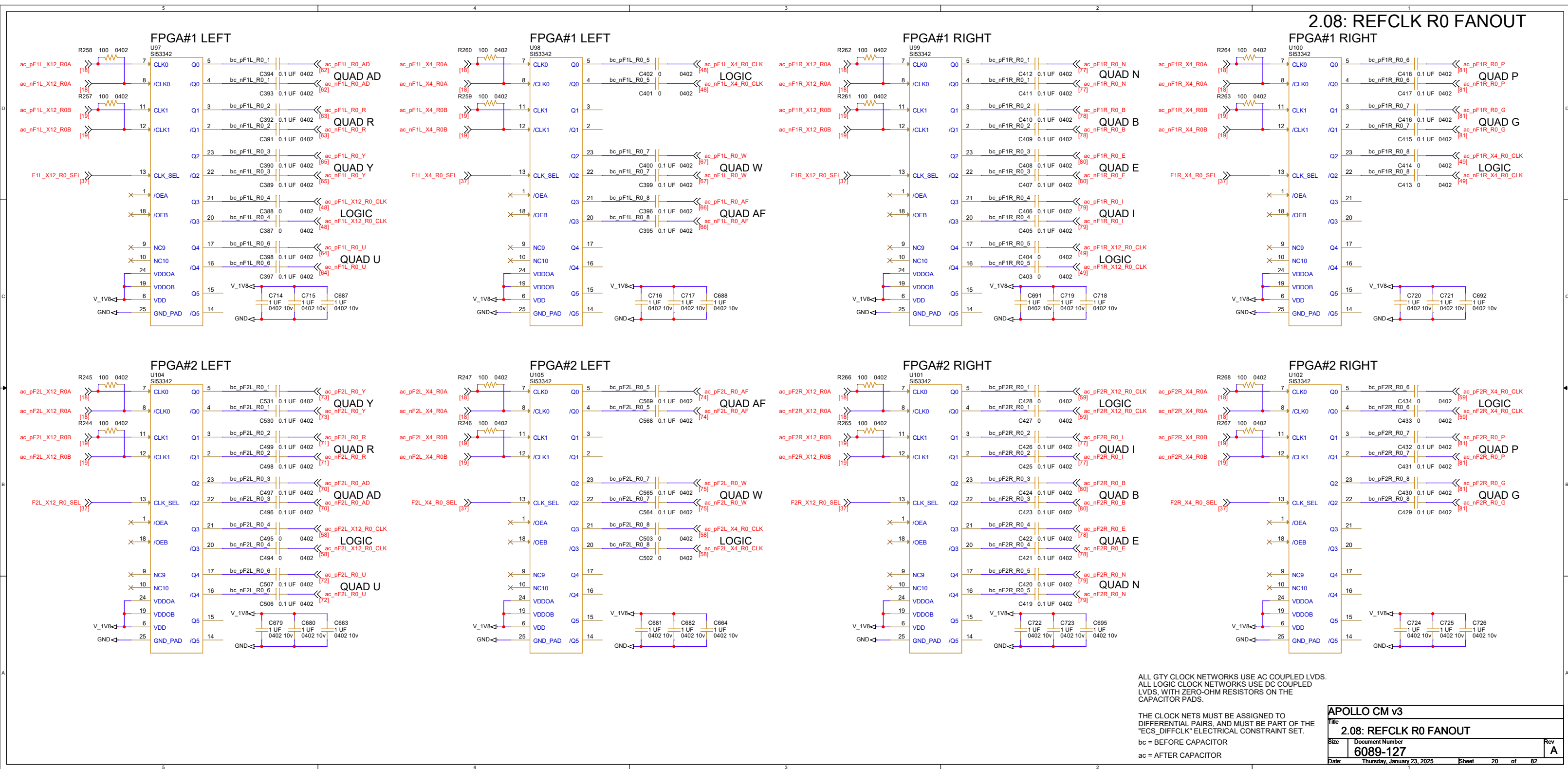
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2.07: REFCLK SYNTHESIZER R0B

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## 2.09: REFCLK SYNTHESIZER R1A

F1 QUAD AB  
(TCDS QUAD)

F2 QUAD AB  
(TCDS QUAD)

SYN R1B IN0

SYN R1C IN0

F1 QUAD W

F1 QUAD AF

F2 QUAD W

F2 QUAD AF

F1 QUAD L  
(C2C/TCDS QUAD)

F2 QUAD L  
(C2C/TCDS QUAD)

OUTPUTS 9 AND 9A MUST BE  
THE SAME FREQUENCY.

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO  
DIFFERENTIAL PAIRS, AND MUST BE PART OF THE  
"ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

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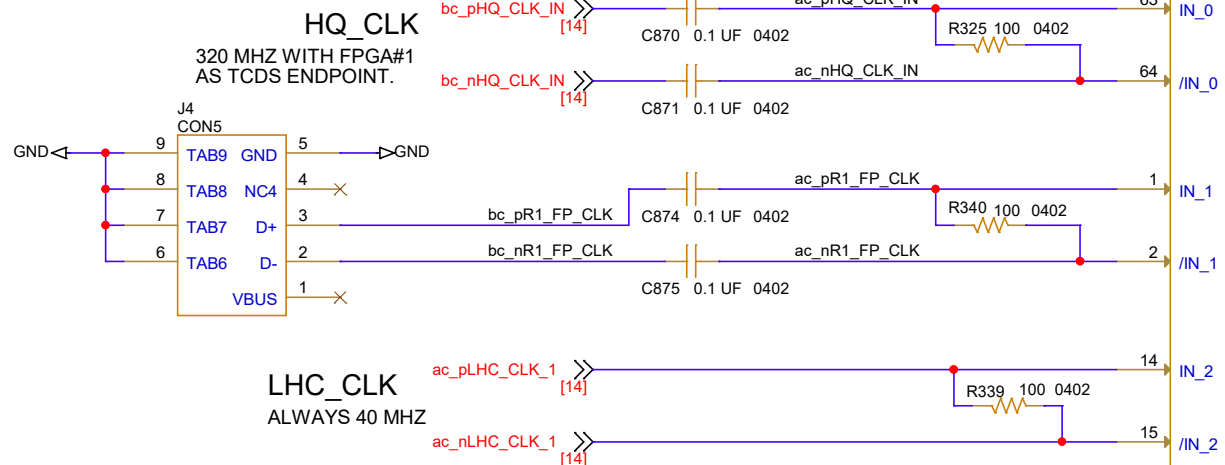
Title  
2.09: REFCLK SYNTHESIZER R1A

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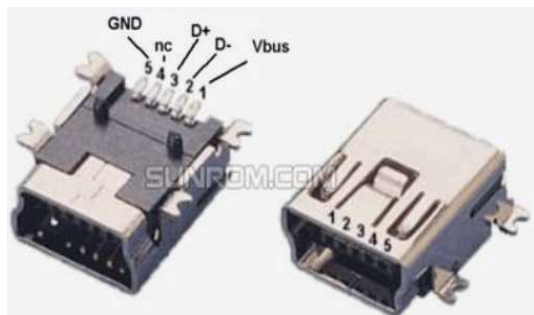
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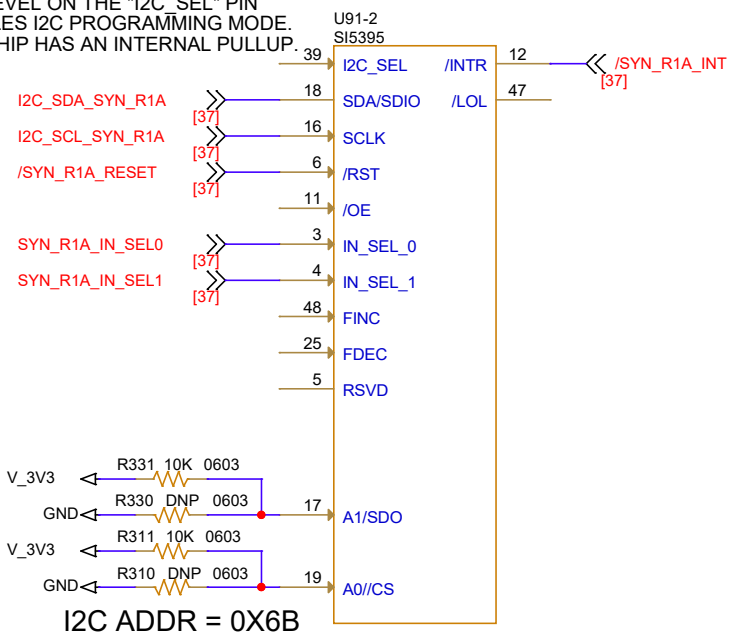


OPTIONAL FRONT PANEL CONNECTOR FOR AN LVDS  
EXTERNAL CLOCK.

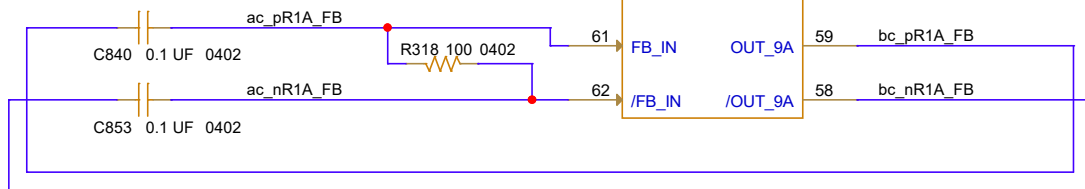
THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE.



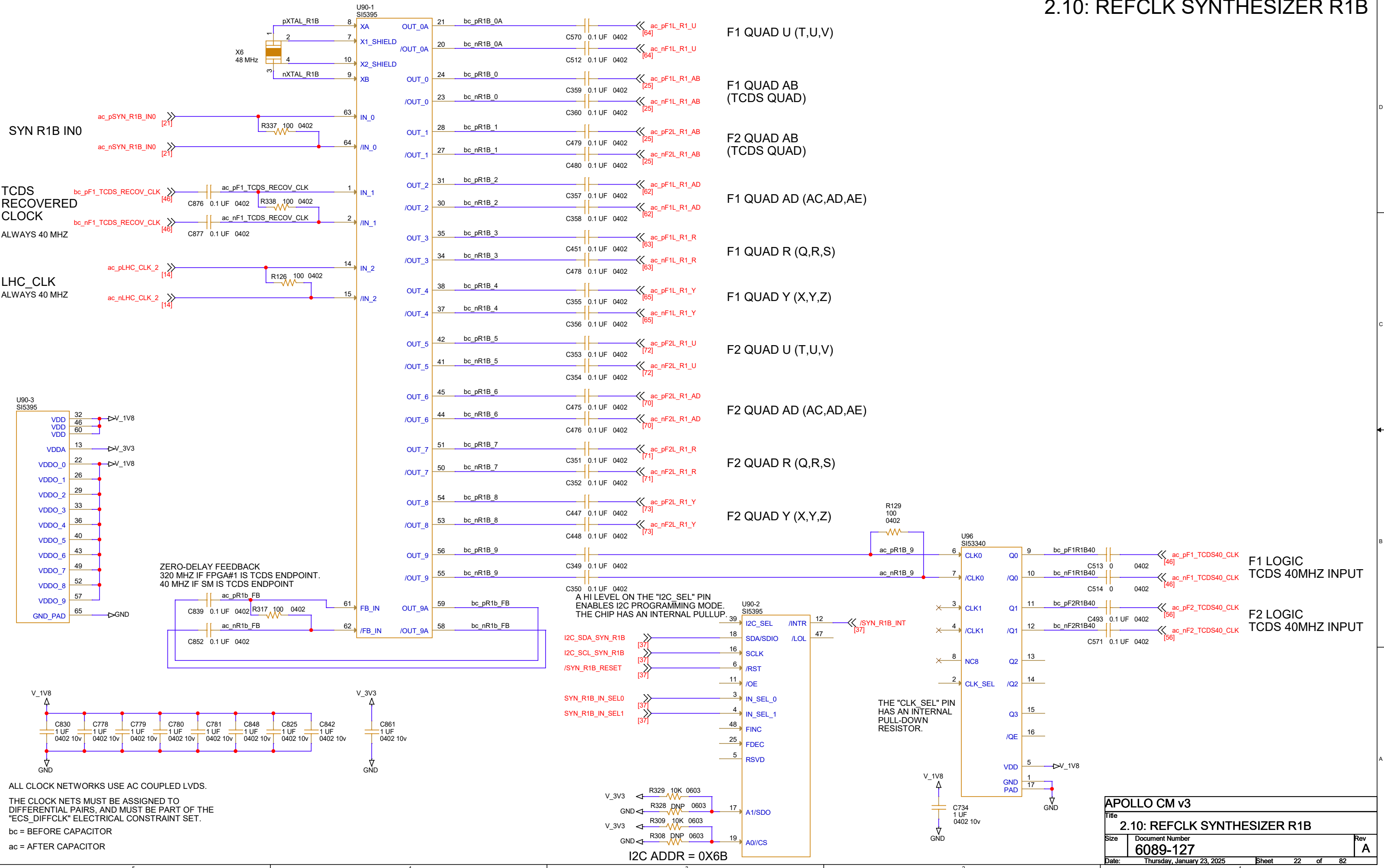
A HI LEVEL ON THE "I2C\_SEL" PIN  
ENABLES I2C PROGRAMMING MODE.  
THE CHIP HAS AN INTERNAL PULLUP.



ZERO-DELAY FEEDBACK  
320 MHZ WITH FPGA#1 AS TCDS ENDPOINT.

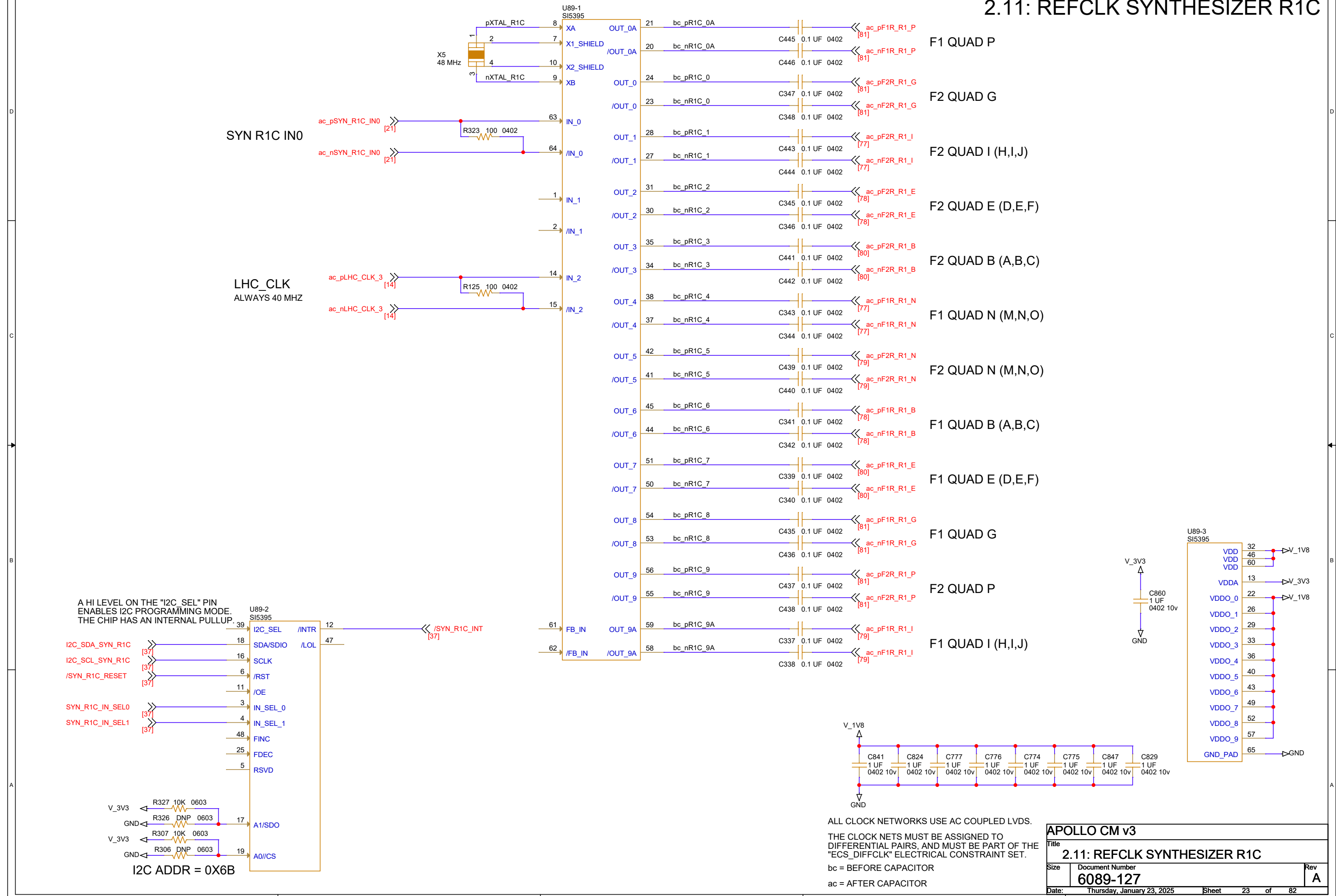


2.10: REFCLK SYNTHESIZER R1B

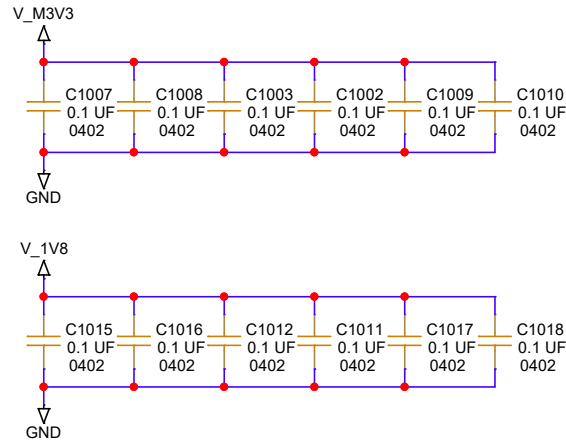
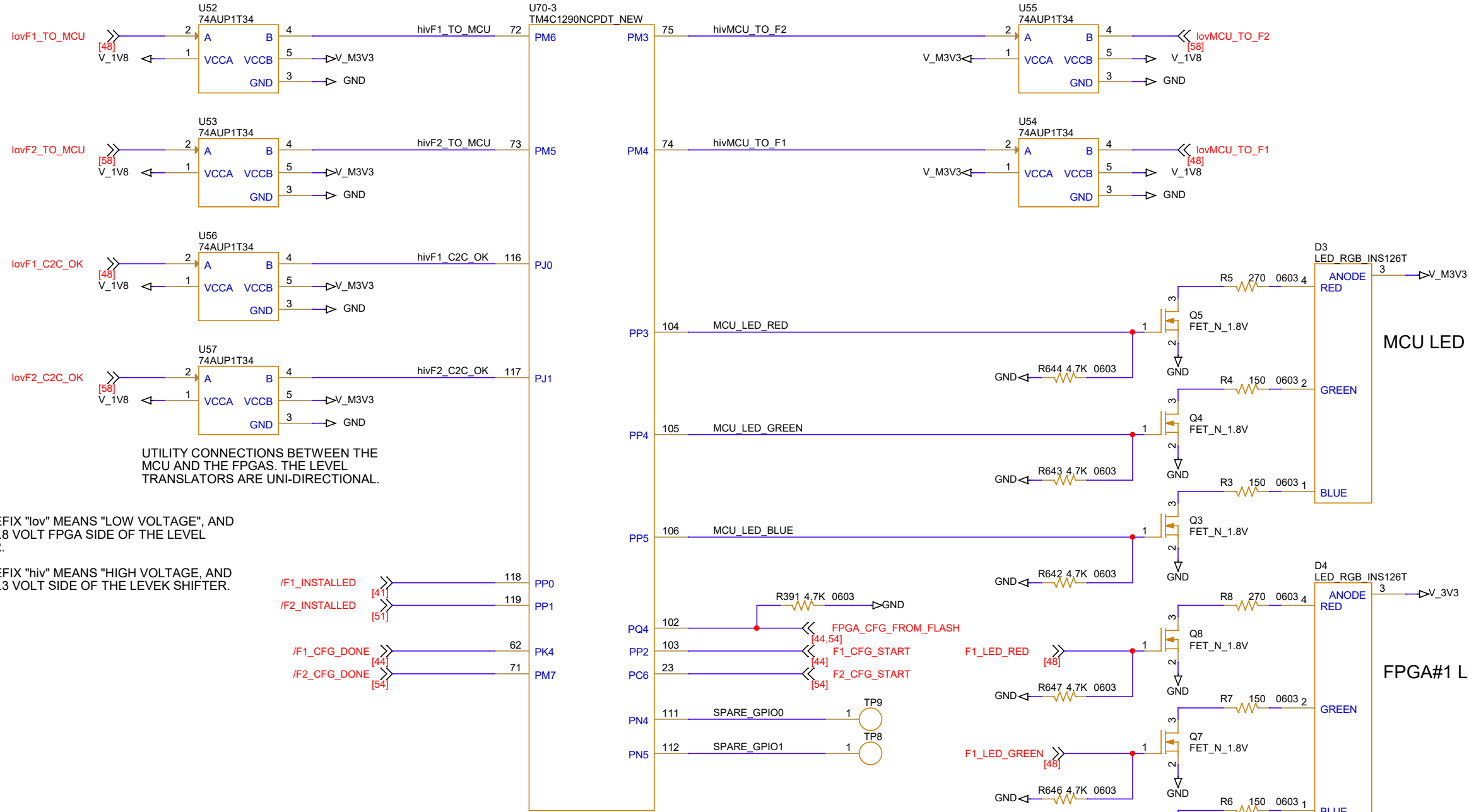




## 2.11: REFCLK SYNTHESIZER R1C



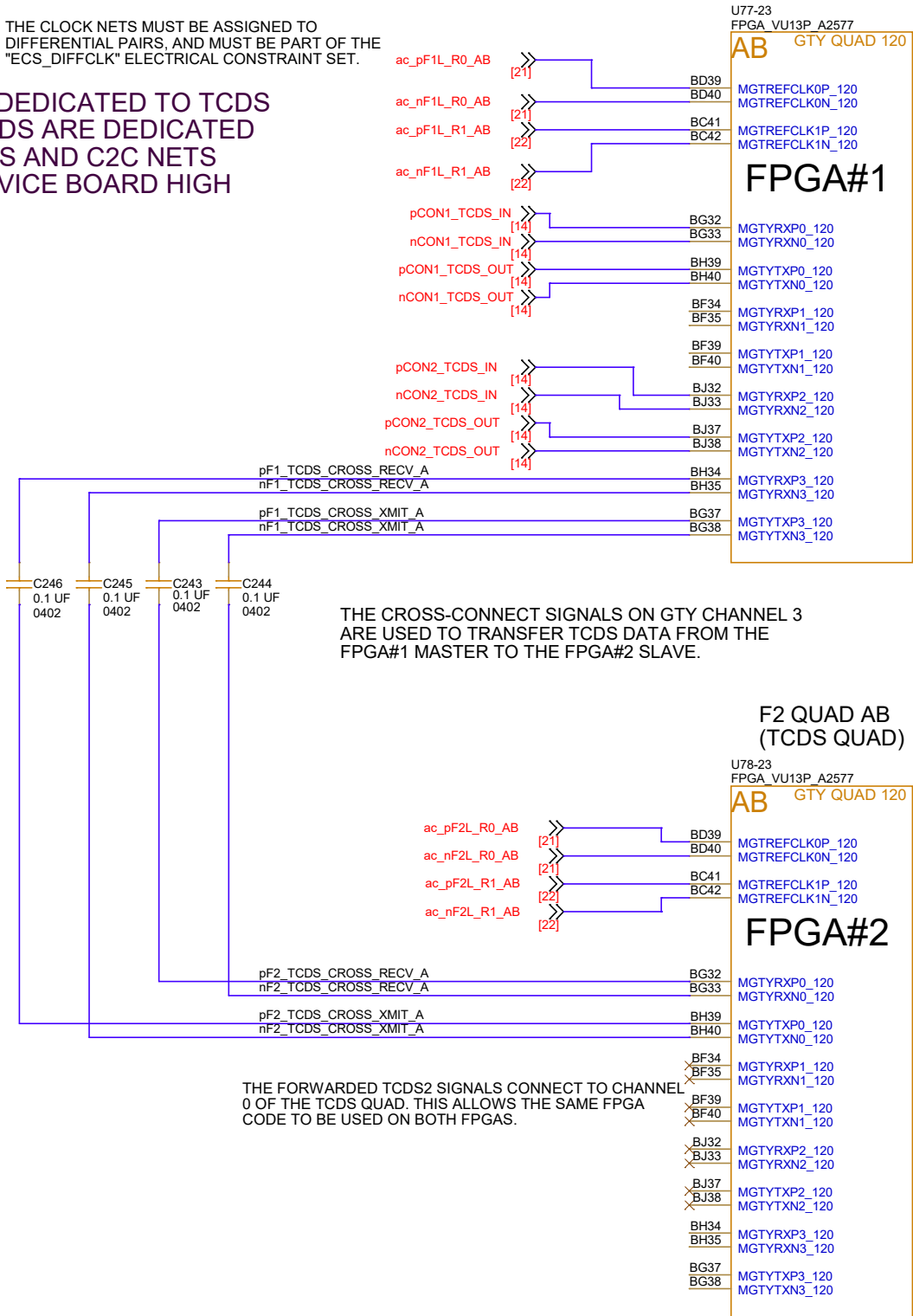
2.12: LEDS AND LEVEL SHIFTERS





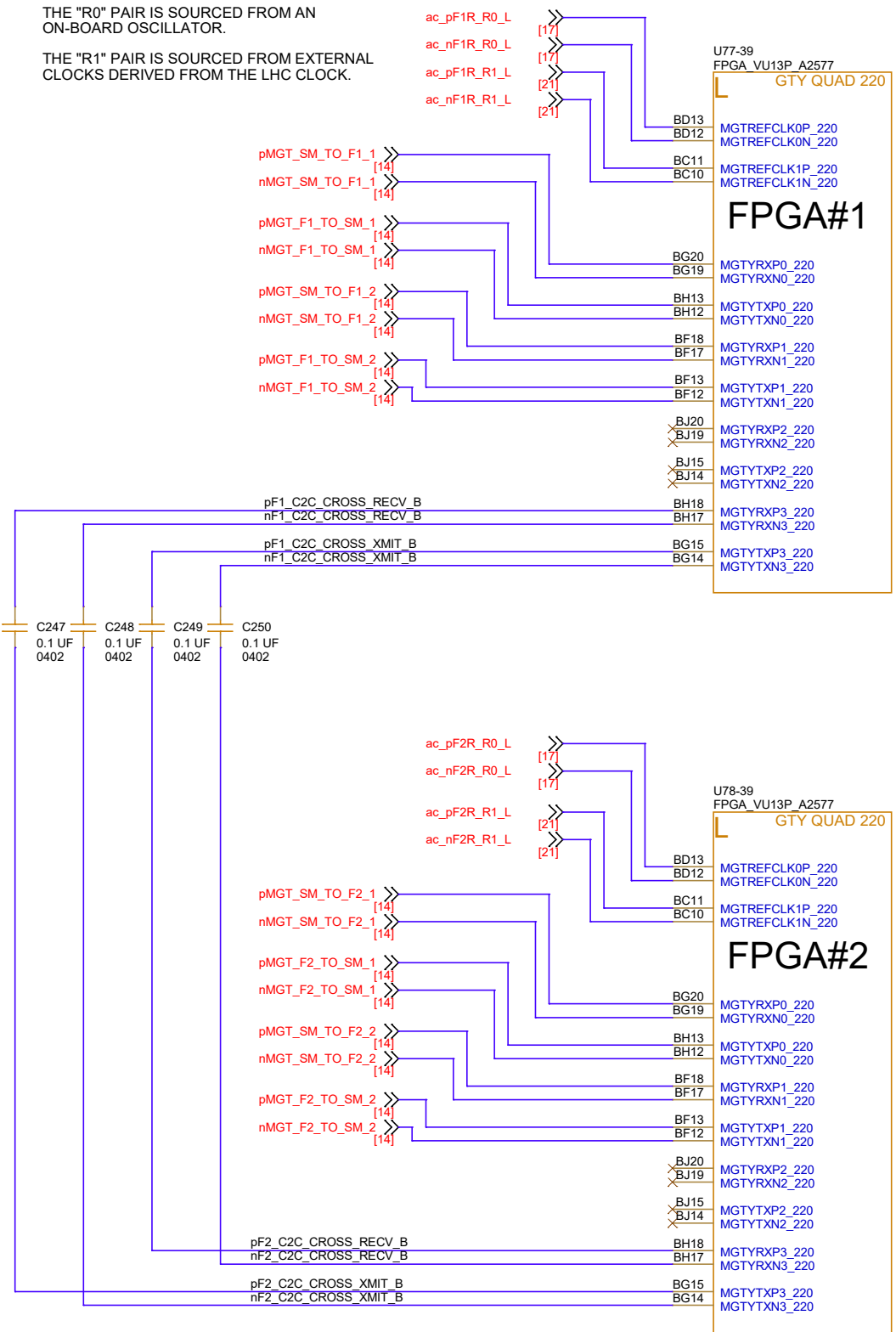
2.13: C2C AND TCDS QUADS

THE "AB" QUADS ARE DEDICATED TO TCDS SIGNALS. THE "L" QUADS ARE DEDICATED TO C2C SIGNALS. TCDS AND C2C NETS COME FROM THE SERVICE BOARD HIGH SPEED CONNECTORS

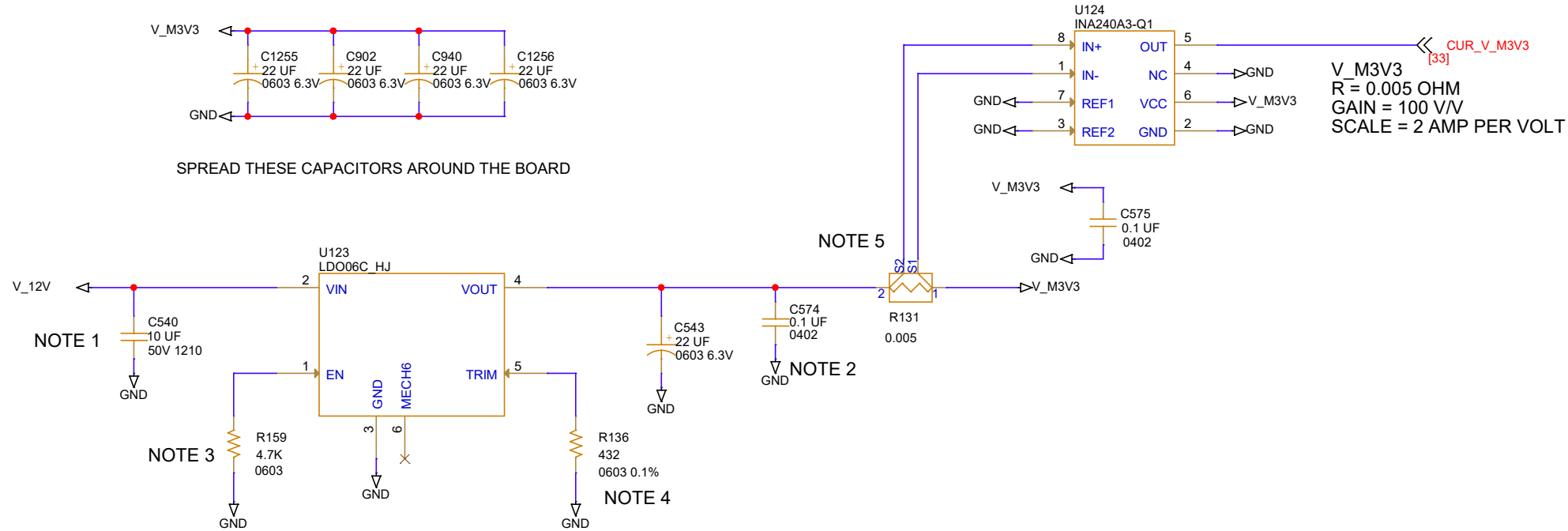


THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.



3.01: POWER MANAGEMENT M3V3



GENERAL NOTES:

V\_M3V3 IS THE "MANAGEMENT" POWER. IT PROVIDES POWER TO THE POWER SEQUENCING CIRCUIT. IT IS ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

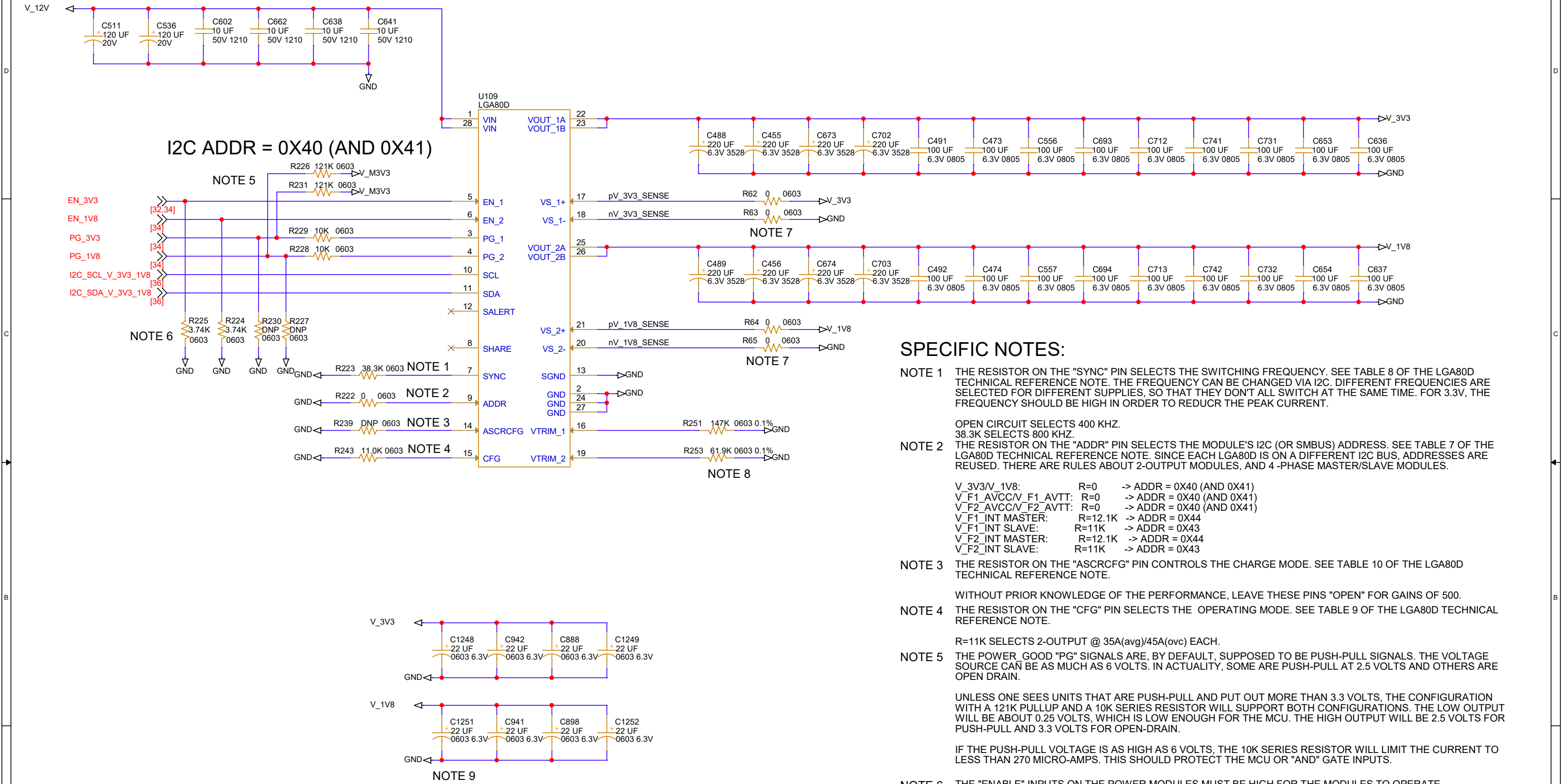
UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

- NOTE 1 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL INPUT CAPACITORS.
- NOTE 2 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL OUTPUT CAPACITORS.
- NOTE 3 UNDERVOLTAGE LOCKOUT RESISTOR  
 $R = 14.81 * (6.81 / ((6.81 * V_{en}) - 18.16))$   
A 4.7K RESISTOR GIVES 5.8 VOLTS MINIMUM TURNON VOLTAGE
- NOTE 4 OUTPUT SETPOINT RESISTOR  
 $R = 1.182 / (V_{OUT} - 0.591)$   
FOR 3.3 VOLTS, R = 436 OHMS (IF R=432 THEN V=3.327)
- NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.
- THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

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3.01: POWER MANAGEMENT M3V3			
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SPECIFIC NOTES:

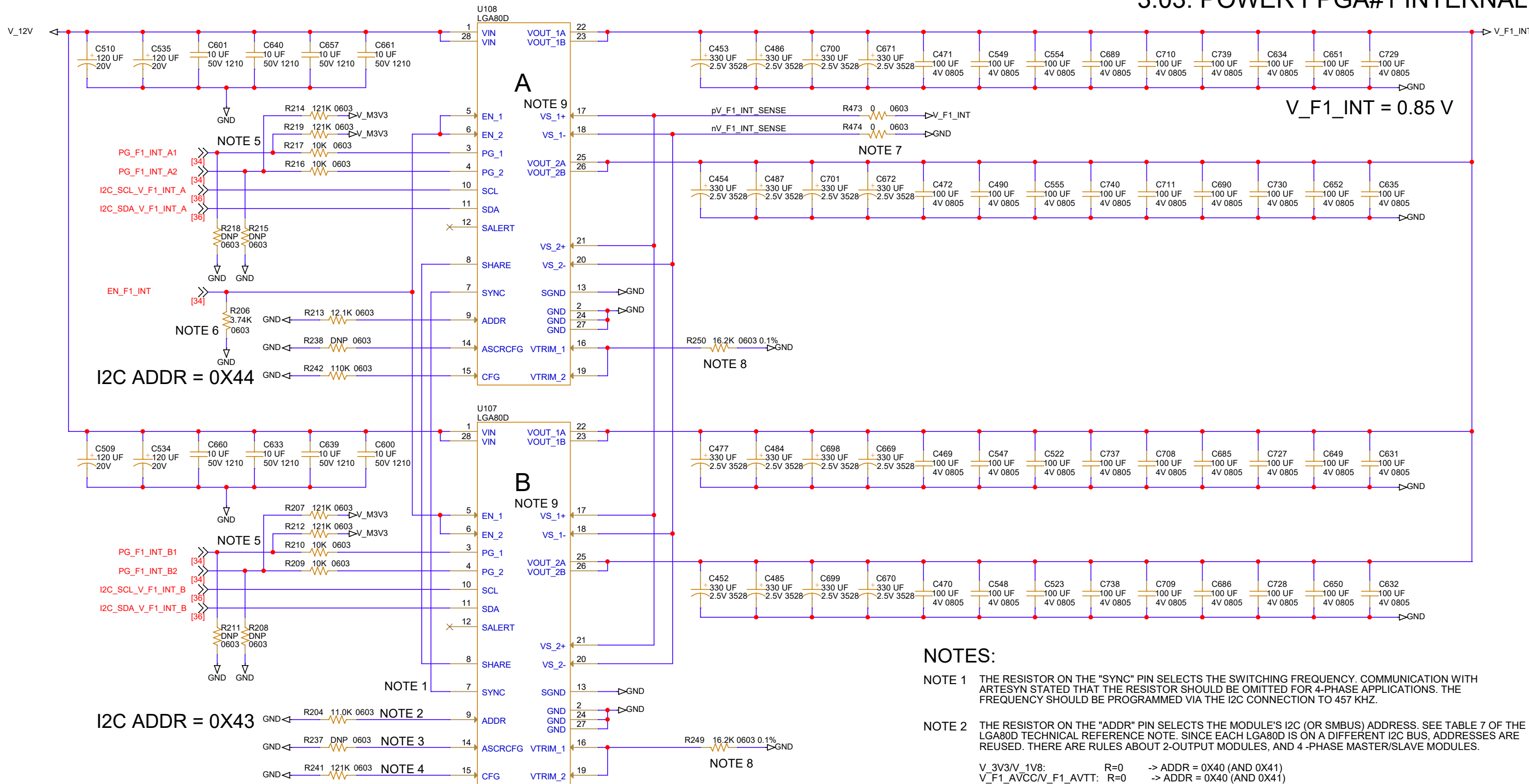
- NOTE 1** THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME. FOR 3.3V, THE FREQUENCY SHOULD BE HIGH IN ORDER TO REDUCR THE PEAK CURRENT.
- OPEN CIRCUIT SELECTS 400 KHZ.  
38.3K SELECTS 800 KHZ.
- NOTE 2** THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.
- V\_3V3/V\_1V8: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_AVCC/V\_F1\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F2\_AVCC/V\_F2\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F1\_INT SLAVE: R=11K -> ADDR = 0X43  
V\_F2\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F2\_INT SLAVE: R=11K -> ADDR = 0X43
- NOTE 3** THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.
- NOTE 4** THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- R=11K SELECTS 2-OUTPUT @ 35A(avg)/45A(ovc) EACH.
- NOTE 5** THE POWER\_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.
- UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.
- IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.
- NOTE 6** THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.
- THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.
- NOTE 7** PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.
- NOTE 8** RSET = 147K FOR 3.3V  
RSET = 61.9K FOR 1.8V
- NOTE 9** SPREAD THESE CAPACITORS AROUND THE BOARD

GENERAL NOTES:

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

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3.02: POWER GLOBAL 3.3V AND 1.8V		
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### 3.03: POWER FPGA#1 INTERNAL



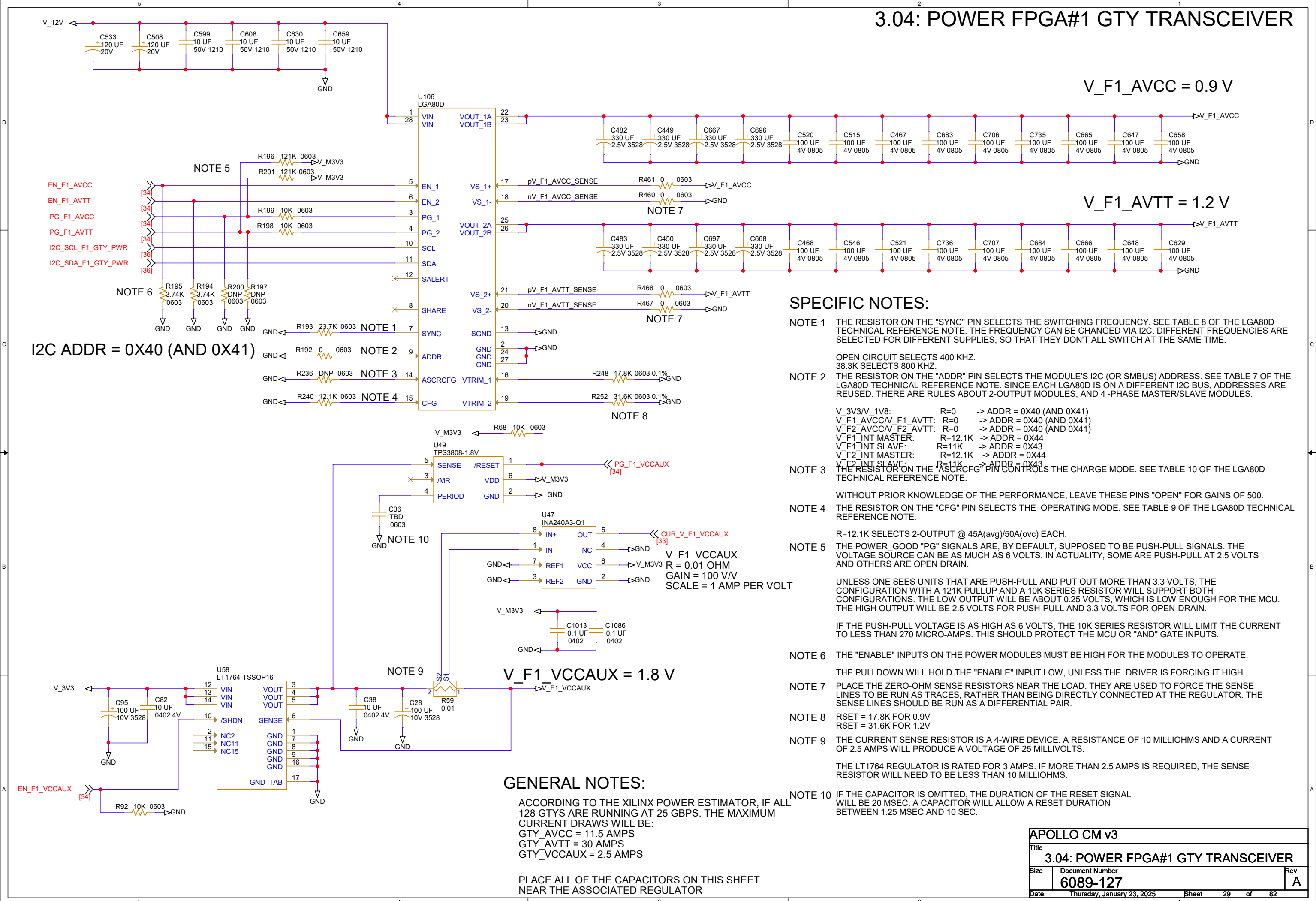
#### NOTES:

- NOTE 1** THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.
- NOTE 2** THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4-PHASE MASTER/SLAVE MODULES.
- V\_3V3/V\_1V8: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_AVCC/V\_F1\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F2\_AVCC/V\_F2\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F1\_INT SLAVE: R=11K -> ADDR = 0X43  
V\_F2\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F2\_INT SLAVE: R=11K -> ADDR = 0X43
- NOTE 3** THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- ARTESYN COMMUNICATION SPECIFIED 10K.
- NOTE 4** THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

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3.04: POWER FPGA#1 GTY TRANSCEIVER



SPECIFIC NOTES:

- NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.
- OPEN CIRCUIT SELECTS 400 KHZ.  
38.3K SELECTS 800 KHZ.
- NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/S�AVE MODULES.
- V\_3V3/V\_1V8: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_AVCC/V\_F1\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F2\_AVCC/V\_F2\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F1\_INT SLAVE: R=11K -> ADDR = 0X43  
V\_F2\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F2\_INT SLAVE: R=11K -> ADDR = 0X43
- NOTE 3 THE RESISTOR ON THE "ASRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.
- NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.
- NOTE 5 THE POWER\_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.
- UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.
- IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.
- NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.
- THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.
- NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.
- NOTE 8 RSET = 17.8K FOR 0.9V  
RSET = 31.6K FOR 1.2V
- NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.
- THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.
- NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

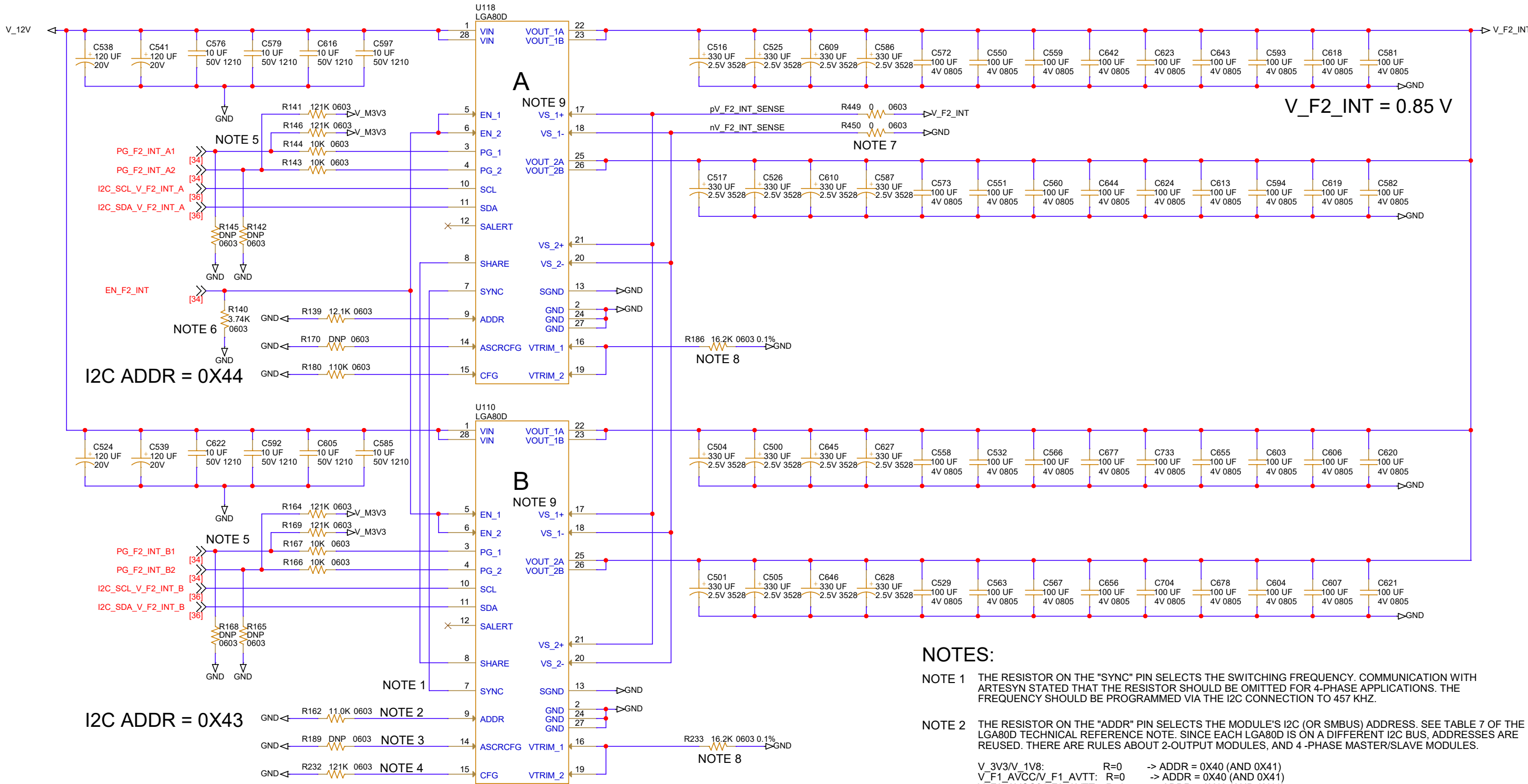
GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:  
GTY\_AVCC = 11.5 AMPS  
GTY\_AVTT = 30 AMPS  
GTY\_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

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### 3.05: POWER FPGA#2 INTERNAL



#### NOTES:

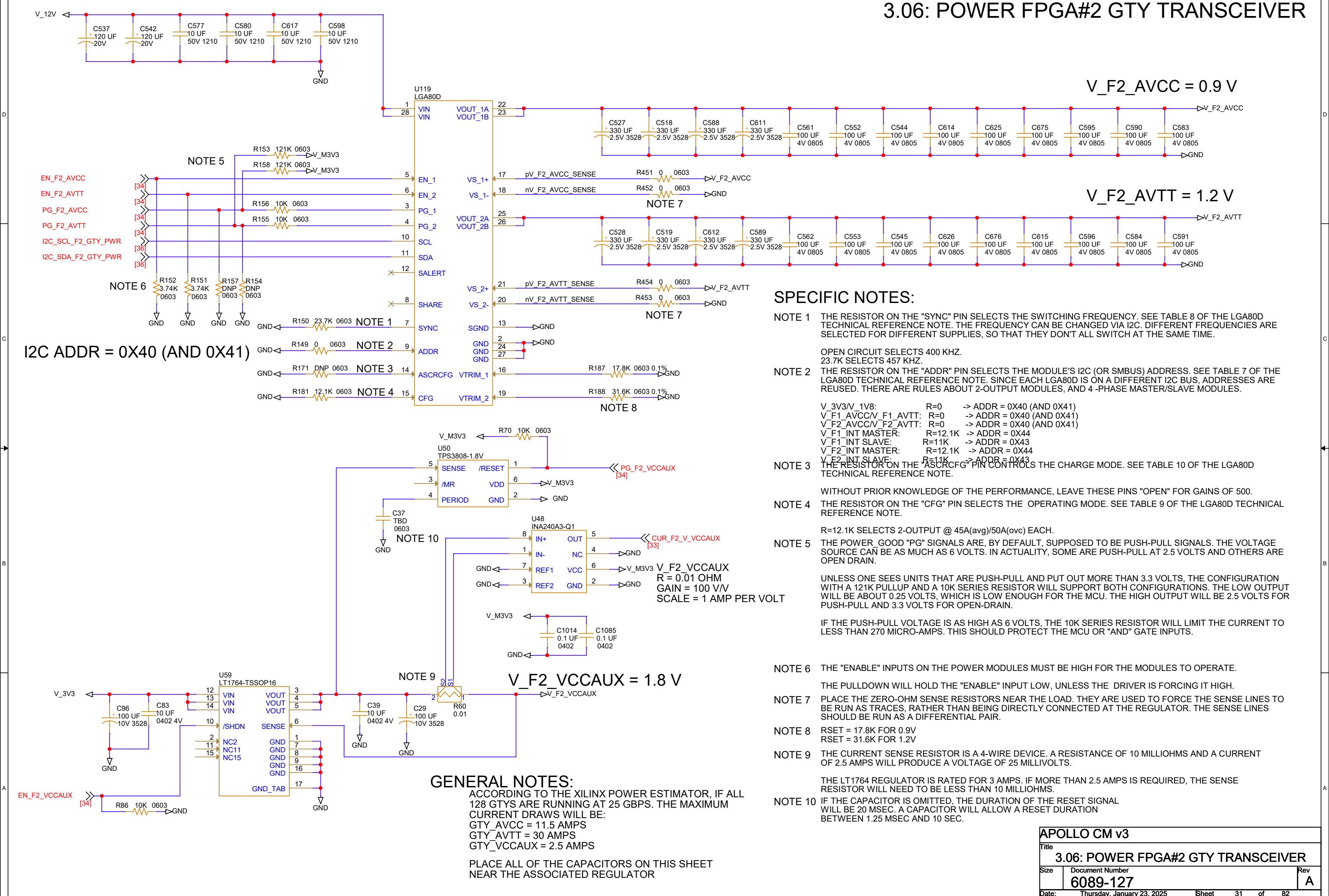
- NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.
- NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/S�AVE MODULES.
- V\_3V3/V\_1V8: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_AVCC/V\_F1\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F2\_AVCC/V\_F2\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F1\_INT SLAVE: R=11K -> ADDR = 0X43  
V\_F2\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F2\_INT SLAVE: R=11K -> ADDR = 0X43
- NOTE 3 THE RESISTOR ON THE "ASRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- ARTESYN COMMUNICATION SPECIFIED 10K.
- NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

- NOTE 5 THE POWER\_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.
- UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.
- IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.
- NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.
- THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.
- NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.
- NOTE 8 RSET = 16.2K FOR 0.85V
- NOTE 9 THE MASTER IS LABELED "A". THE SLAVE IS LABELED "B".

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3.06: POWER FPGA#2 GTY TRANSCEIVER



I2C ADDR = 0X40 (AND 0X41)

V\_F2\_AVCC = 0.9 V

V\_F2\_AVTT = 1.2 V

V\_F2\_VCCAUX = 1.8 V

SPECIFIC NOTES:

- NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.
- OPEN CIRCUIT SELECTS 400 KHZ.  
23.7K SELECTS 457 KHZ.
- NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.
- V\_3V3/V\_1V8: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_AVCC/V\_F1\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F2\_AVCC/V\_F2\_AVTT: R=0 -> ADDR = 0X40 (AND 0X41)  
V\_F1\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F1\_INT SLAVE: R=11K -> ADDR = 0X43  
V\_F2\_INT MASTER: R=12.1K -> ADDR = 0X44  
V\_F2\_INT SLAVE: R=11K -> ADDR = 0X43
- NOTE 3 THE RESISTOR ON THE "ASRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.
- NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.
- R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.
- NOTE 5 THE POWER\_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.
- UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.
- IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.
- NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.
- THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.
- NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.
- NOTE 8 RSET = 17.8K FOR 0.9V  
RSET = 31.6K FOR 1.2V
- NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.
- THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.
- NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

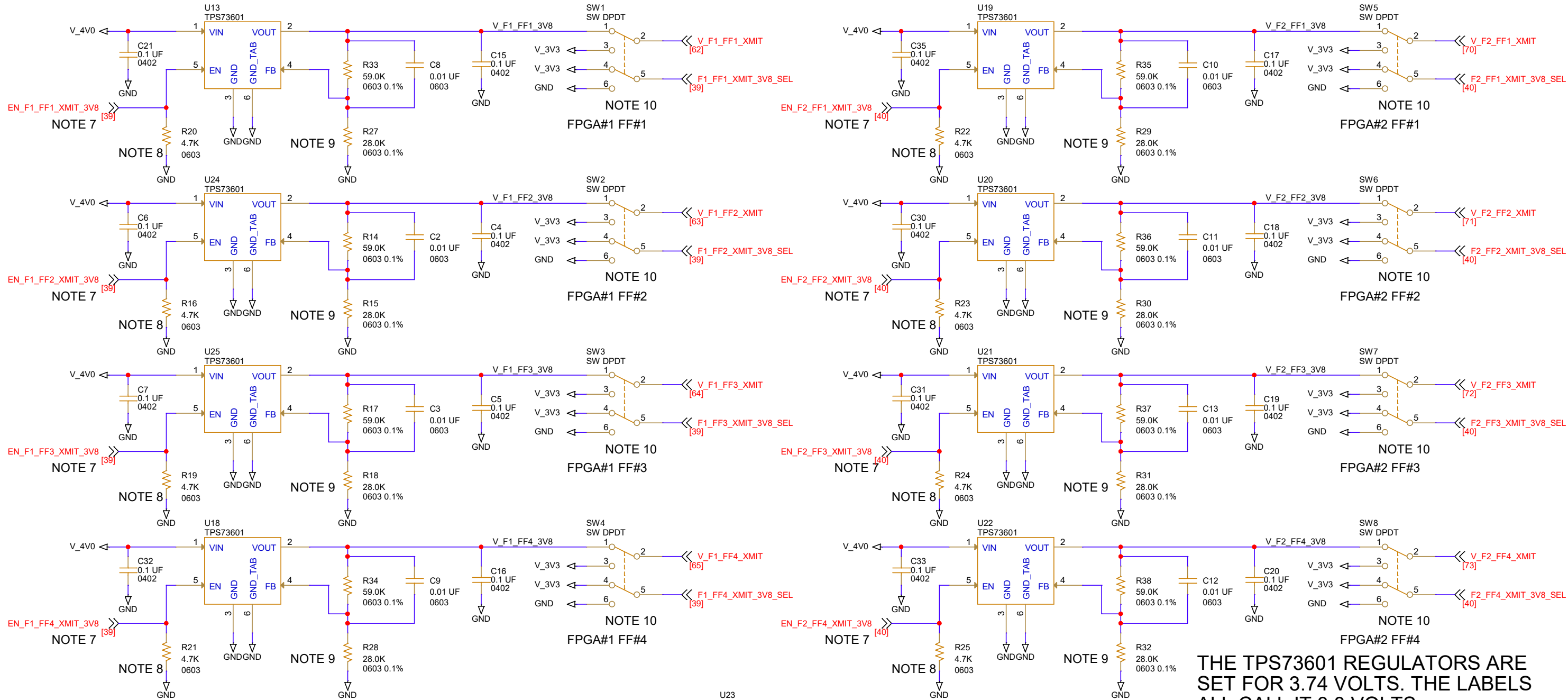
GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:  
GTY\_AVCC = 11.5 AMPS  
GTY\_AVTT = 30 AMPS  
GTY\_VCCAUX = 2.5 AMPS

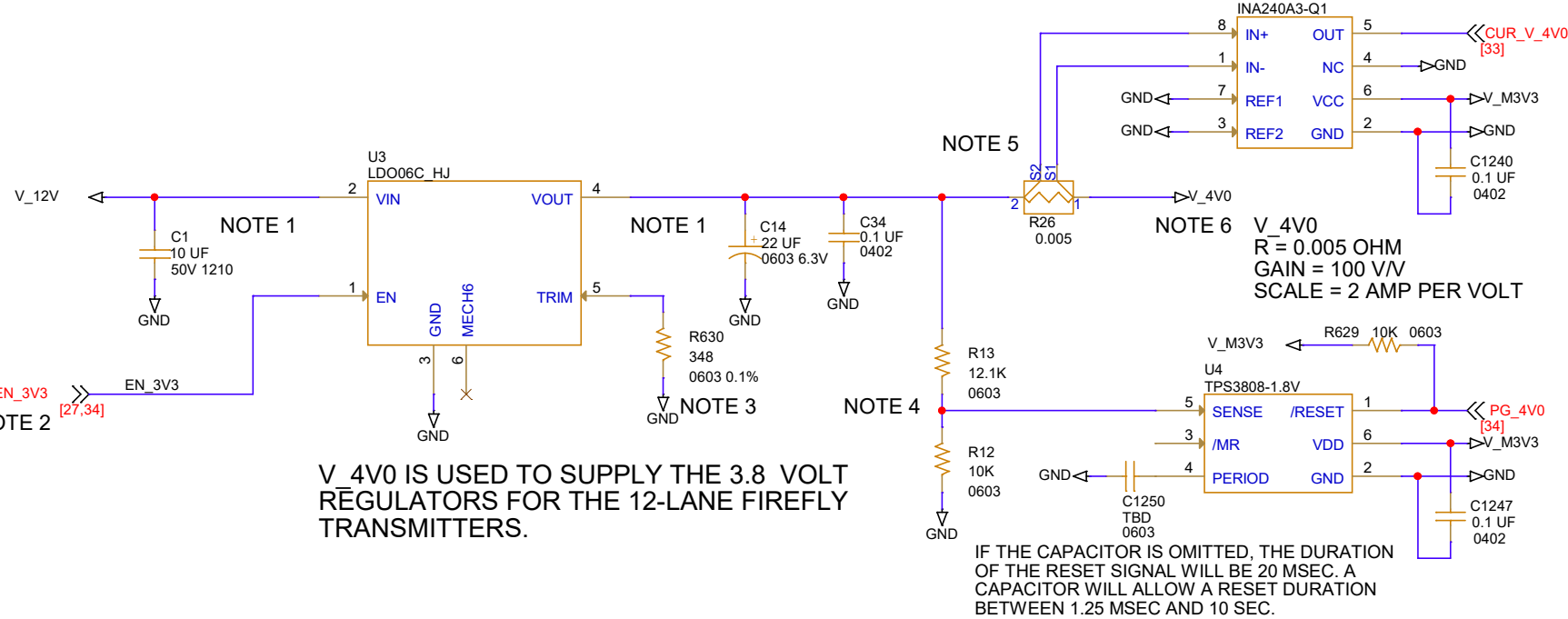
PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

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### 3.07: POWER FOR FF X12 XMIT



THE TPS73601 REGULATORS ARE SET FOR 3.74 VOLTS. THE LABELS ALL CALL IT 3.8 VOLTS.



- NOTE 1 THE LDO06C DOES NOT REQUIRE ANY EXTERNAL INPUT OR OUTPUT CAPACITORS.
- NOTE 2 THE LDO06C IS ENABLED AT THE SAME TIME AS THE BOARD-WIDE 3.3V SUPPLY.
- NOTE 3 LDO06C OUTPUT SETPOINT RESISTOR  
 $R = 1.182 / (V_{OUT} - 0.591)$   
FOR 4.0 VOLTS,  $R = 0.347$  KOHMS
- NOTE 4 THE MONITORING CHIP EXPECTS 1.8 VOLTS AT THE INPUT, SO THE 4.0 VOLTS IS DIVIDED.
- NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.
- NOTE 6 THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.
- NOTE 7 V\_4V0 IS ONLY CONNECTED ONTHIS PAGE, EXCEPT FOR MEASURING BY THE MCU ADC.
- NOTE 8 THE TPS73601 REGULATOR SHOULD NOT BE ENABLED UNTIL THE FIREFLY TRANSMITTER TYPE HAS BEEN DETERMINED AND THE VOLTAGE SWITCH IS FOUND TO BE IN THE CORRECT POSITION.
- NOTE 9 PULLDOWNS ARE NEEDED ON THE CONTROL INPUTS, SINCE THE I2C DRIVER DEVICES NEED TO BE CONFIGURED AS OUTPUTS BEFORE THEY CAN CONTOL THE LOGIC LEVEL. THE I2C DRIVERS HAVE A BUILT-IN 100K PULLUP.
- NOTE 10 THE TPS73601 OUTPUT VOLTAGE IS CALCULATED BY:  
 $V_{OUT} = 1.204 * ((R_{top} + R_{bot}) / R_{bot})$   
IF  $R_{top} = 59.0k$  AND  $R_{bot} = 28k$ , THEN  $V_{OUT} = 3.74$  V
- NOTE 11 THE SWITCH IS SHOWN IN THE POSITION TO PROVIDE 3.8 VOLTS TO THE FIREFLY TRANSMITTER. THE "3V8\_SEL" SIGNAL WILL BE HIGH.

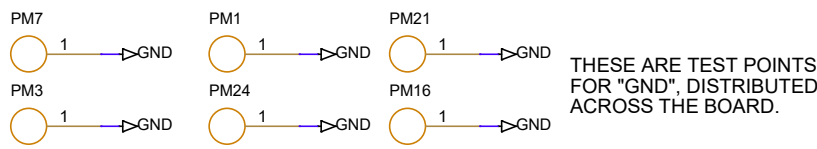
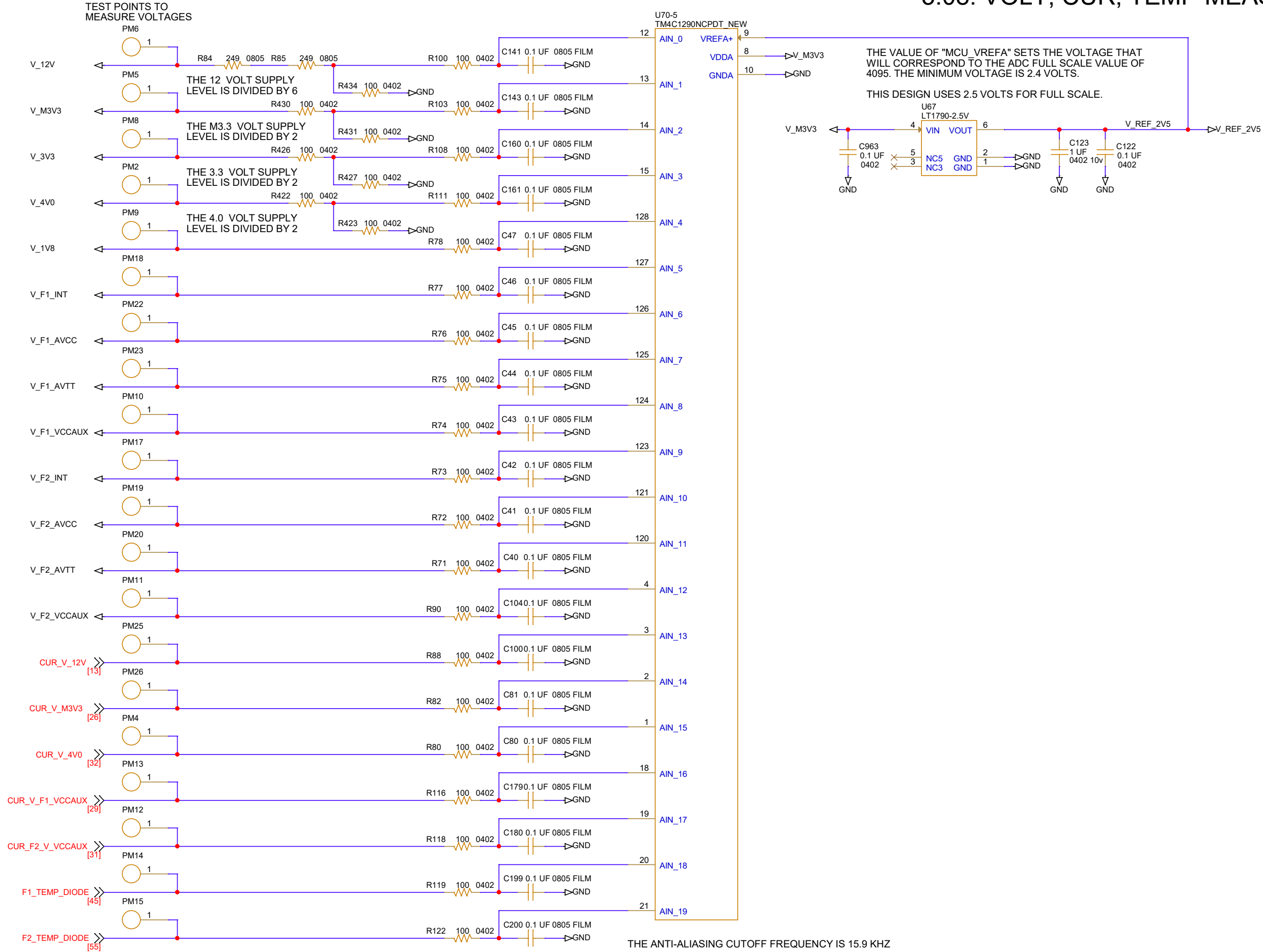
V\_4V0 IS USED TO SUPPLY THE 3.8 VOLT REGULATORS FOR THE 12-LANE FIREFLY TRANSMITTERS.

IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

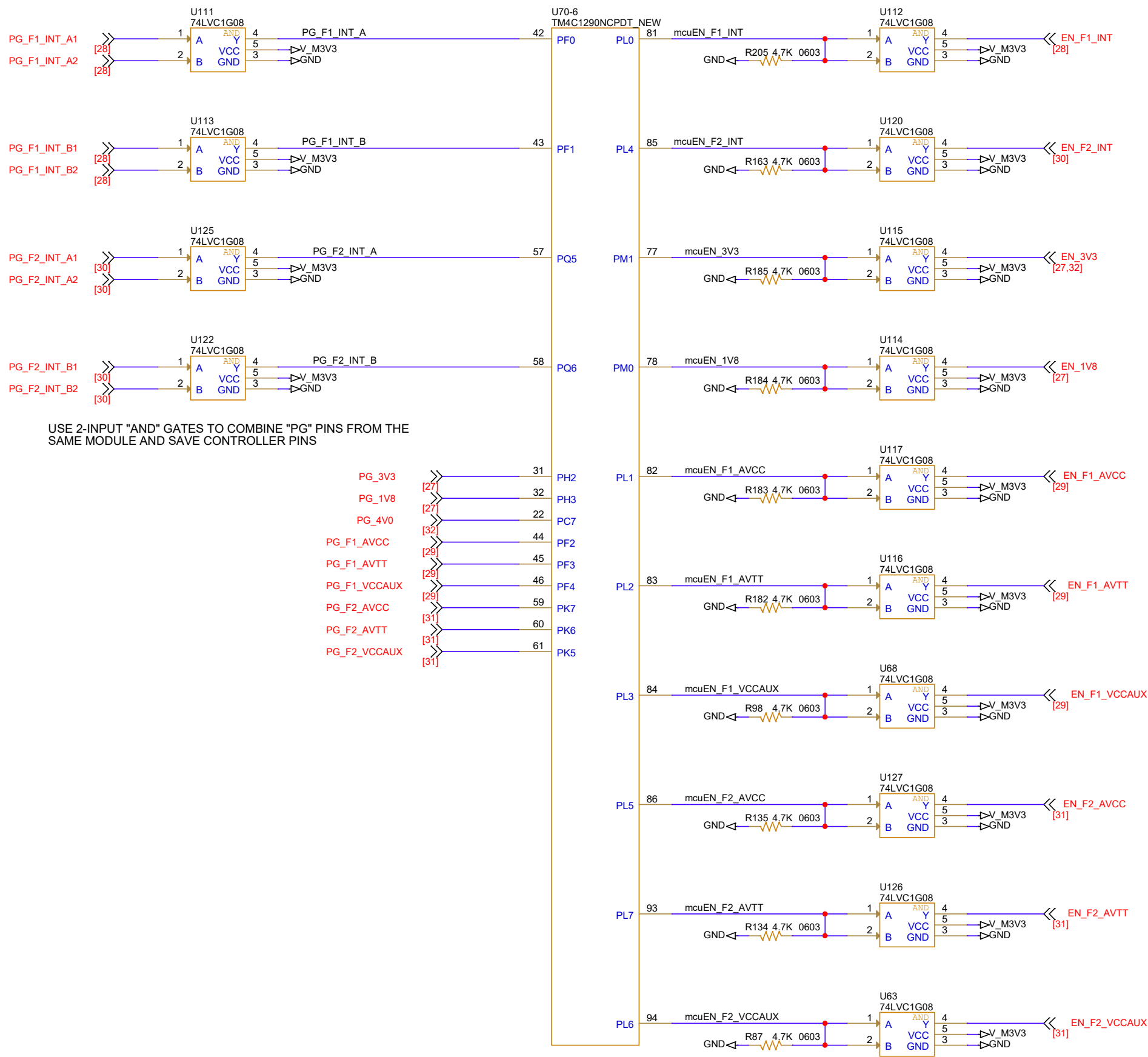
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Title		
3.07: POWER FOR FF X12 XMIT		
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3.08: VOLT, CUR, TEMP MEASURE



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Title			
3.08: VOLT, CUR, TEMP MEASURE			
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THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN V\_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

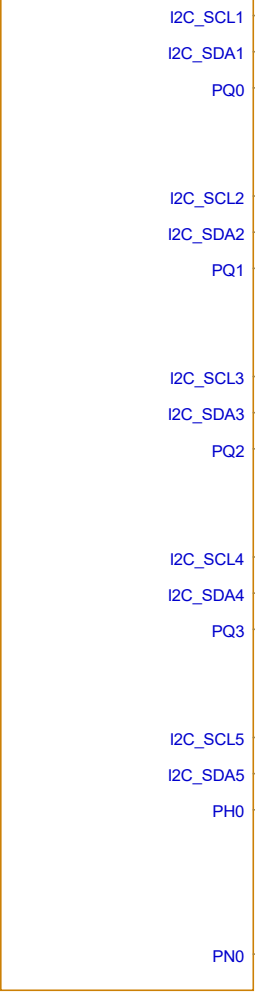


4.01: I2C CONTROLLER

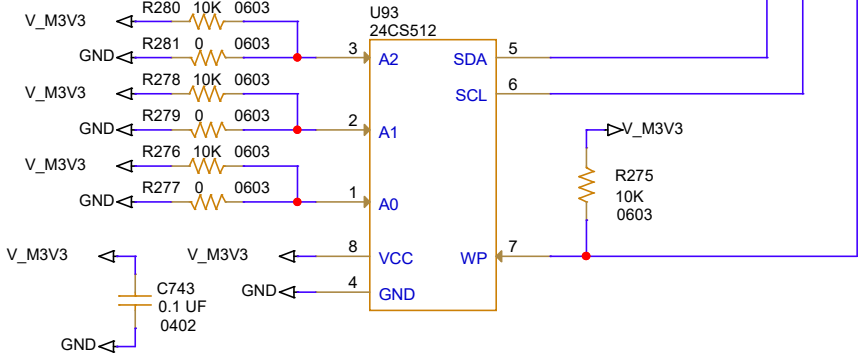
MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.

THE I2C PULLUPS ON THE MCU ARE POWERED FROM V\_M3V3.

U70-4  
TM4C1290NCPDT\_NEW



THE OUTPUTS THAT DRIVE THE "RESET" SIGNALS NEED TO BE OPEN-DRAIN.



THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS. IT ALSO CONTAINS CONFIGURATION FILES FOR THE SI5395 SYNTHESIZERS.

THE EEPROM IS CONNECTED TO THE I2C BUS THAT RUNS THE CLOCKING CHIPS.

R/W I2C ADDR = 0X50

SEC/CONF I2C ADDR = 0X58

24CS512 I2C ADDRESS:  
EEPROM READ OR WRITE  
1 0 1 0 A2 A1 A0  
RANGE: 0X50 TO 0X57  
SECURITY OR CONFIGURATION REGISTER  
1 0 1 1 A2 A1 A0  
RANGE 0X58 TO 0X5F

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

PWR I2C

CLOCKS I2C

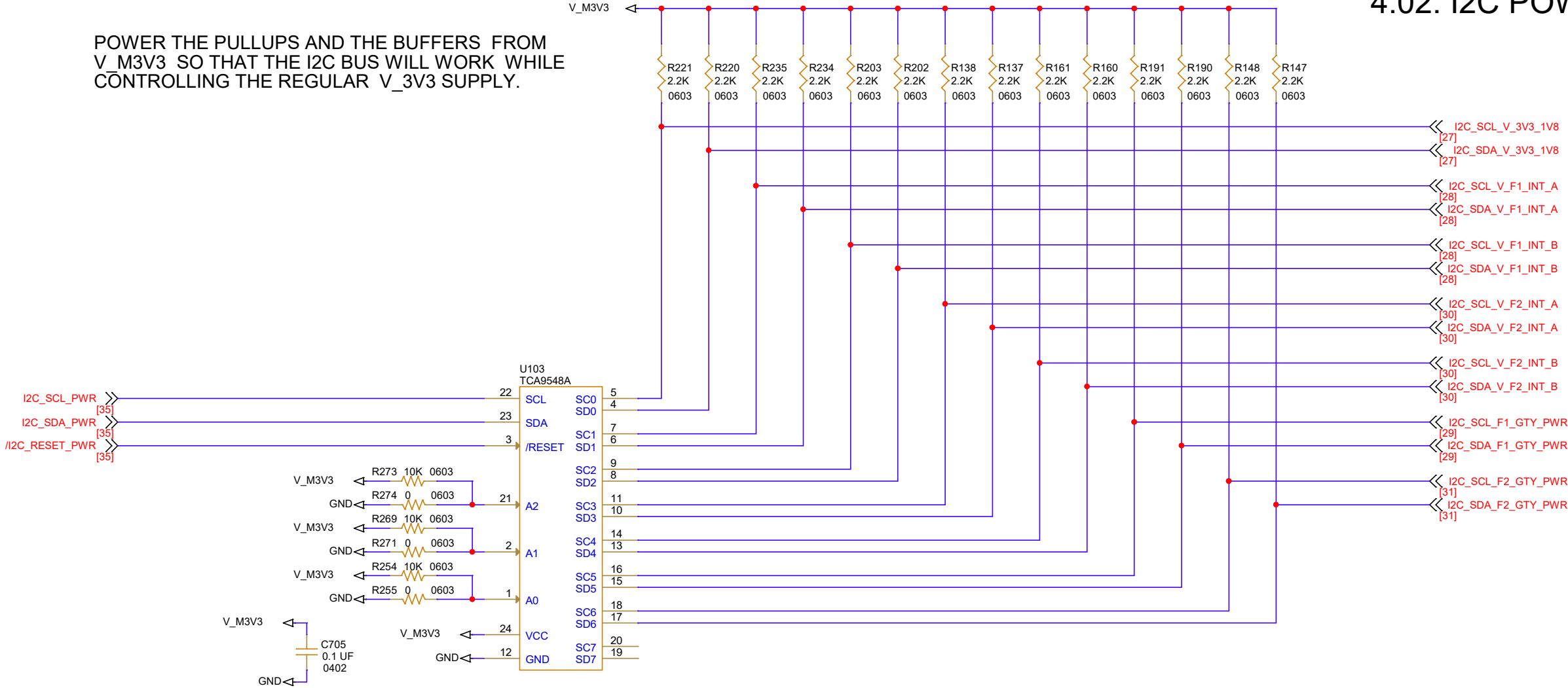
FPGA#2 OPTICS I2C

FPGA#1 OPTICS I2C

FPGA I2C

4.02: I2C POWER CONTROL

POWER THE PULLUPS AND THE BUFFERS FROM V\_M3V3 SO THAT THE I2C BUS WILL WORK WHILE CONTROLLING THE REGULAR V\_3V3 SUPPLY.



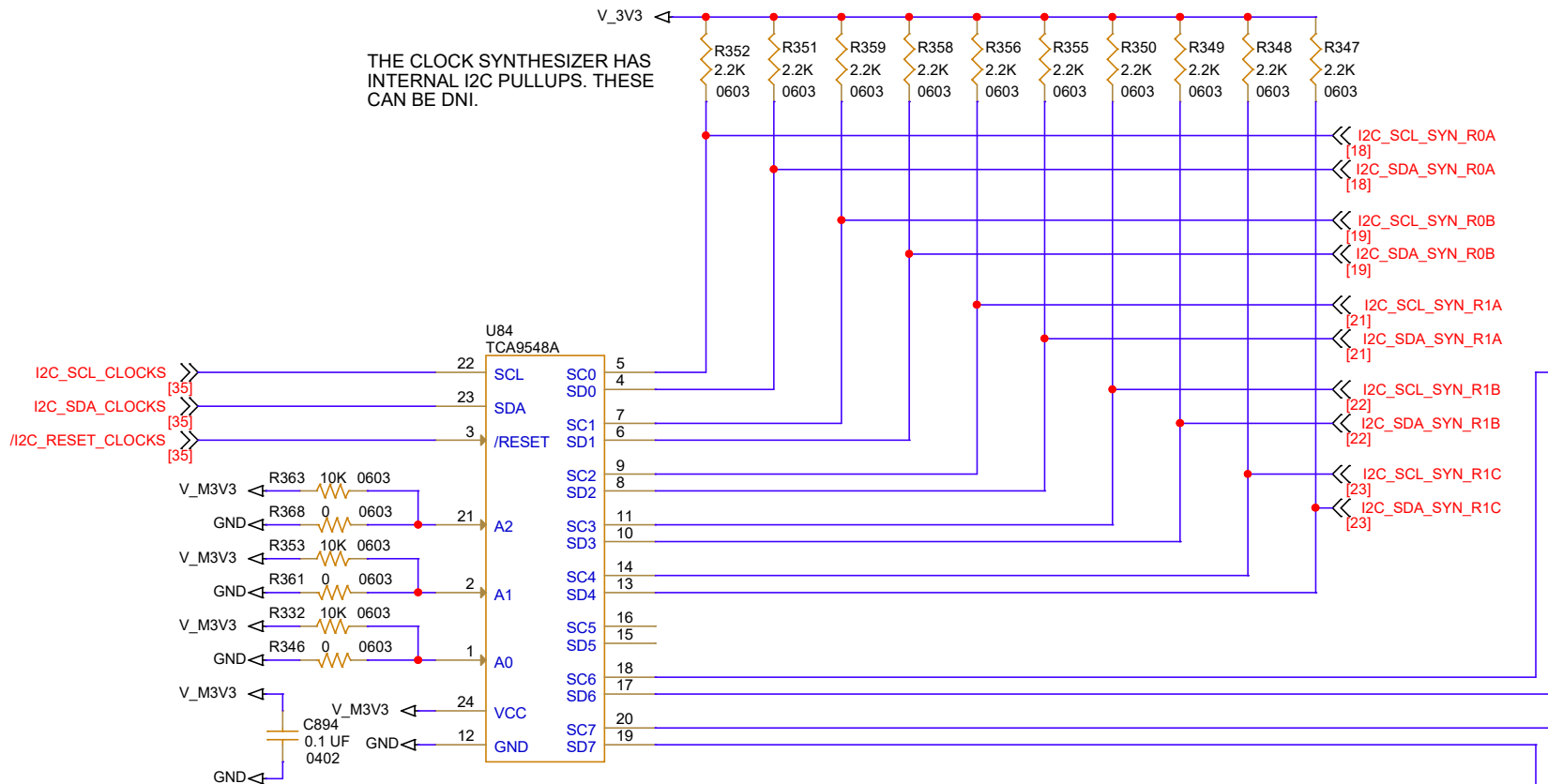
I2C ADDR = 0X70

TCA9548A I2C ADDRESS:  
READ OR WRITE  
1 1 1 0 A2 A1 A0  
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '1'.

4.03: I2C CLOCK CONTROL



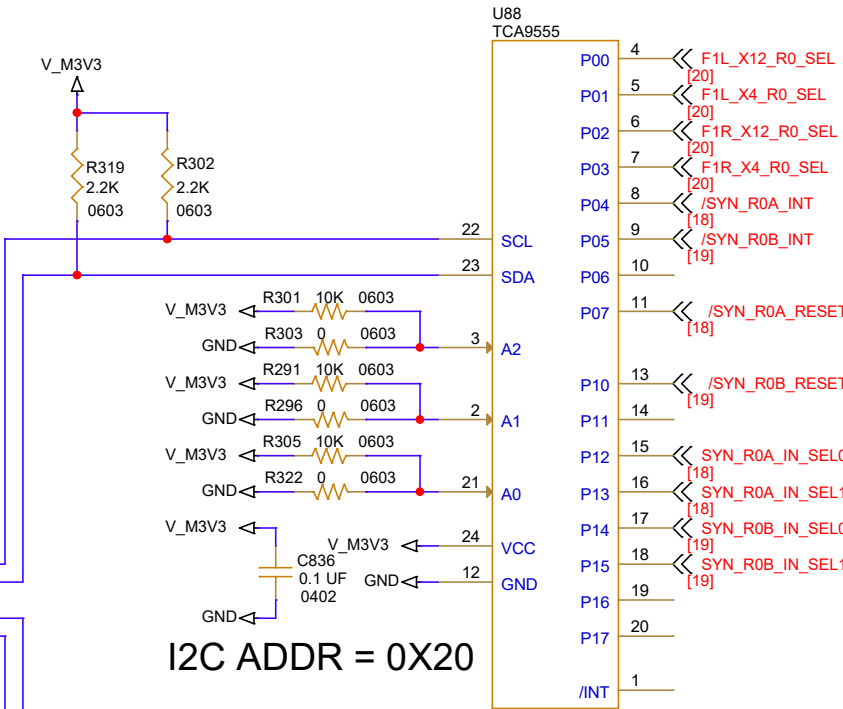
THE CLOCK SYNTHESIZER HAS  
INTERNAL I2C PULLUPS. THESE  
CAN BE DNI.

I2C ADDR = 0X70

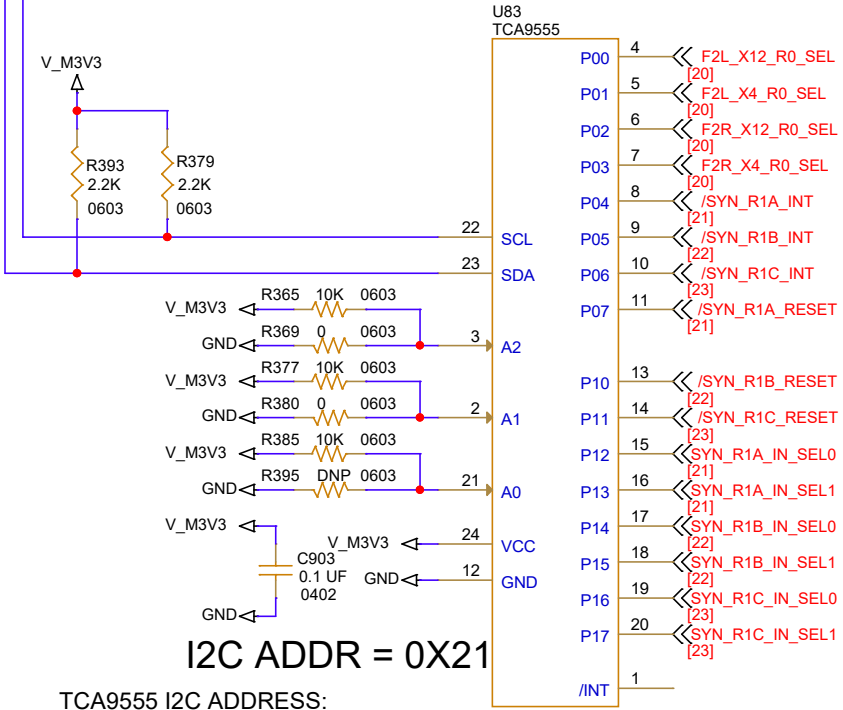
TCA9548A I2C ADDRESS:  
READ OR WRITE  
1 1 1 0 A2 A1 A0  
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '1'.



I2C ADDR = 0X20



I2C ADDR = 0X21

TCA9555 I2C ADDRESS:  
READ OR WRITE  
0 1 0 0 A2 A1 A0  
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '1'.  
RANGE: 0X30 TO 0X37

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Title  
4.03: I2C CLOCK CONTROL

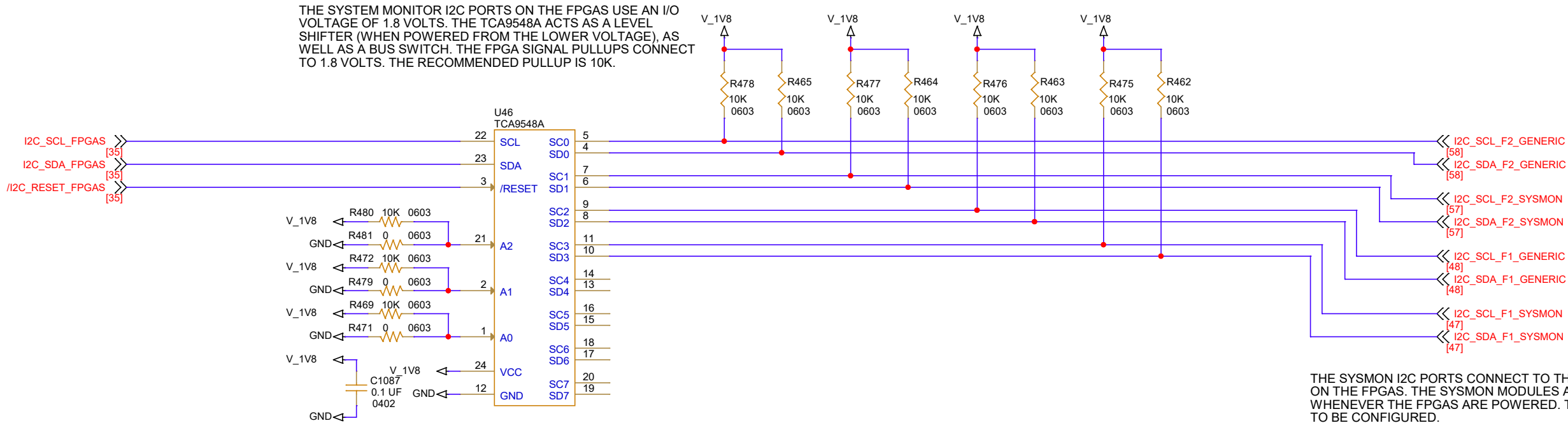
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4.04: I2C FPGA INTERNALS



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:  
READ OR WRITE  
1 1 1 0 A2 A1 A0  
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER  
TO SET AN ADDRESS BIT TO '1'.

THE SYSMON I2C PORTS CONNECT TO THE SYSMON MODULE PINS ON THE FPGAS. THE SYSMON MODULES ARE AVAILABLE WHENEVER THE FPGAS ARE POWERED. THE FPGAS DO NOT HAVE TO BE CONFIGURED.

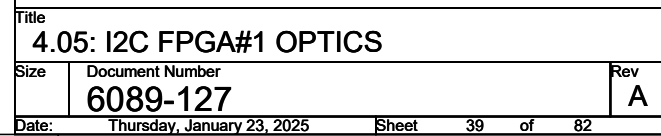
THE GENERIC I2C PORTS CONNECT TO I2C MODULES THAT ARE LOADED AS PART OF THE CONFIGURATION PROCESS. THEY ARE NOT AVAILABLE BEFORE THE FPGA HAS BEEN CONFIGURED.

THE GENERIC MODULES HAVE MORE CAPABILITY THAN THE SYSMON MODULES.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

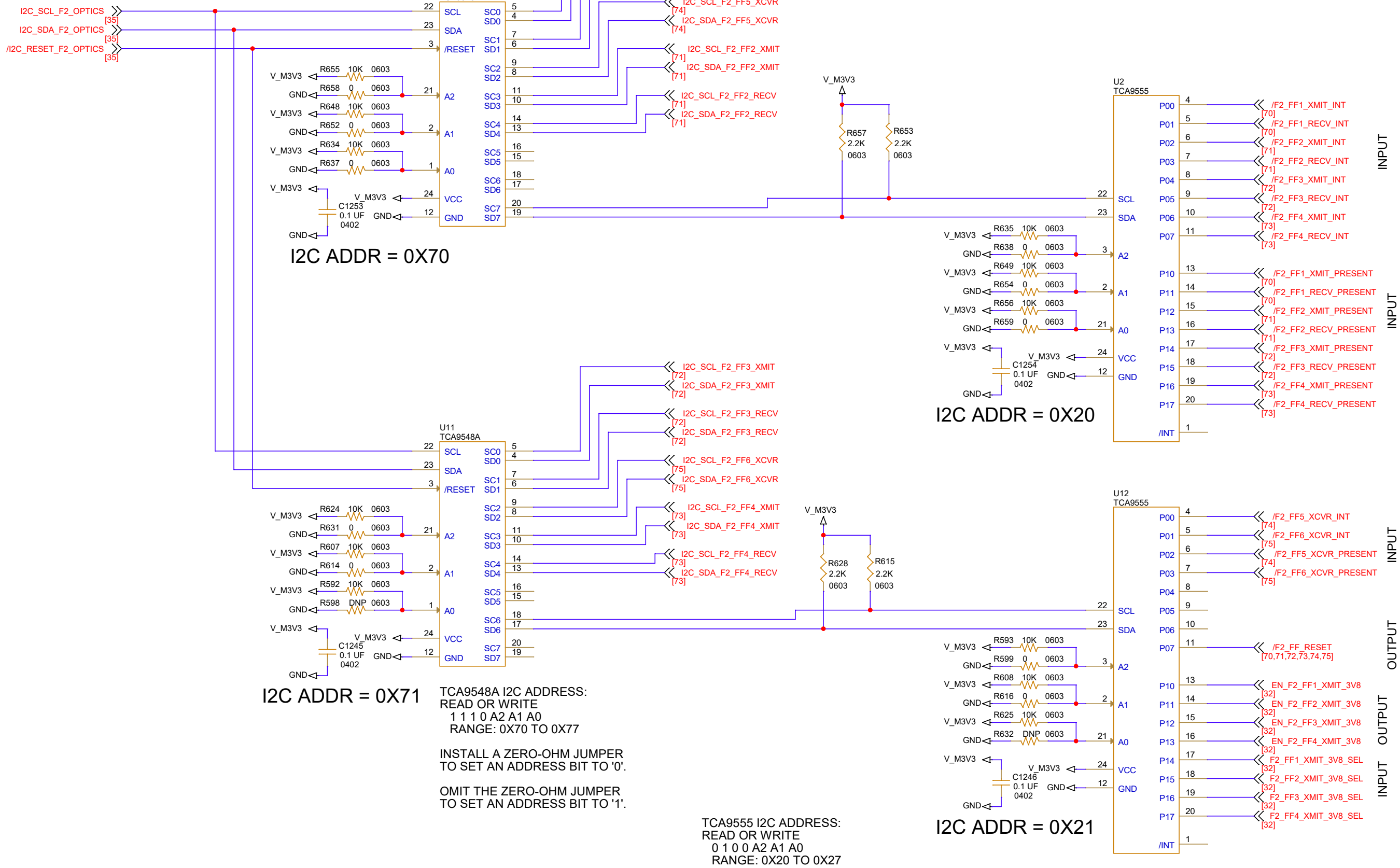
APOLLO CM v3		
Title		
4.04: I2C FPGA INTERNALS		
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I2C REGISTER PIN ASSIGNMENTS ARE SCRAMBLED COMPARED TO PREVIOUS CM VERSIONS

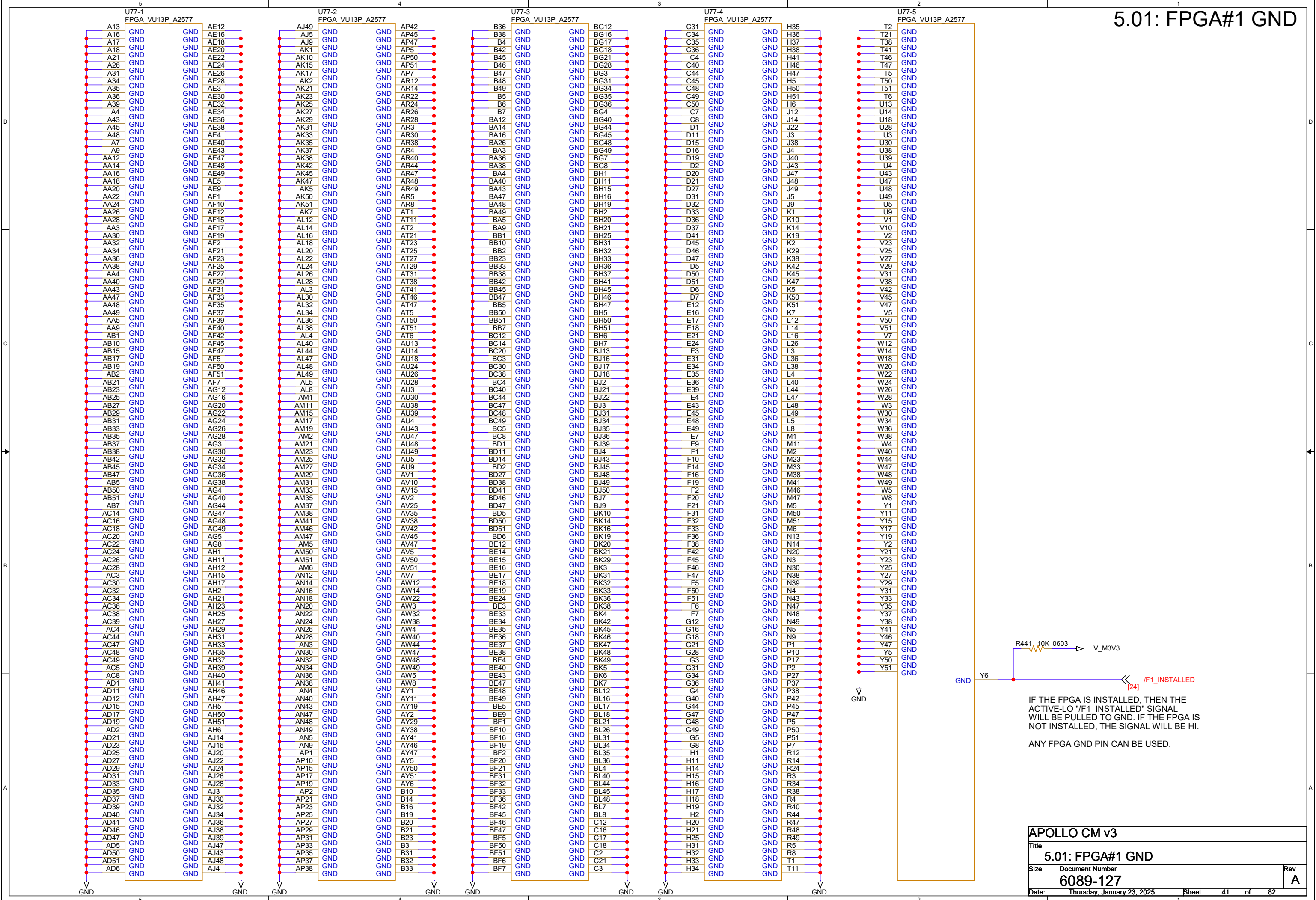
4.06: I2C FPGA#2 OPTICS



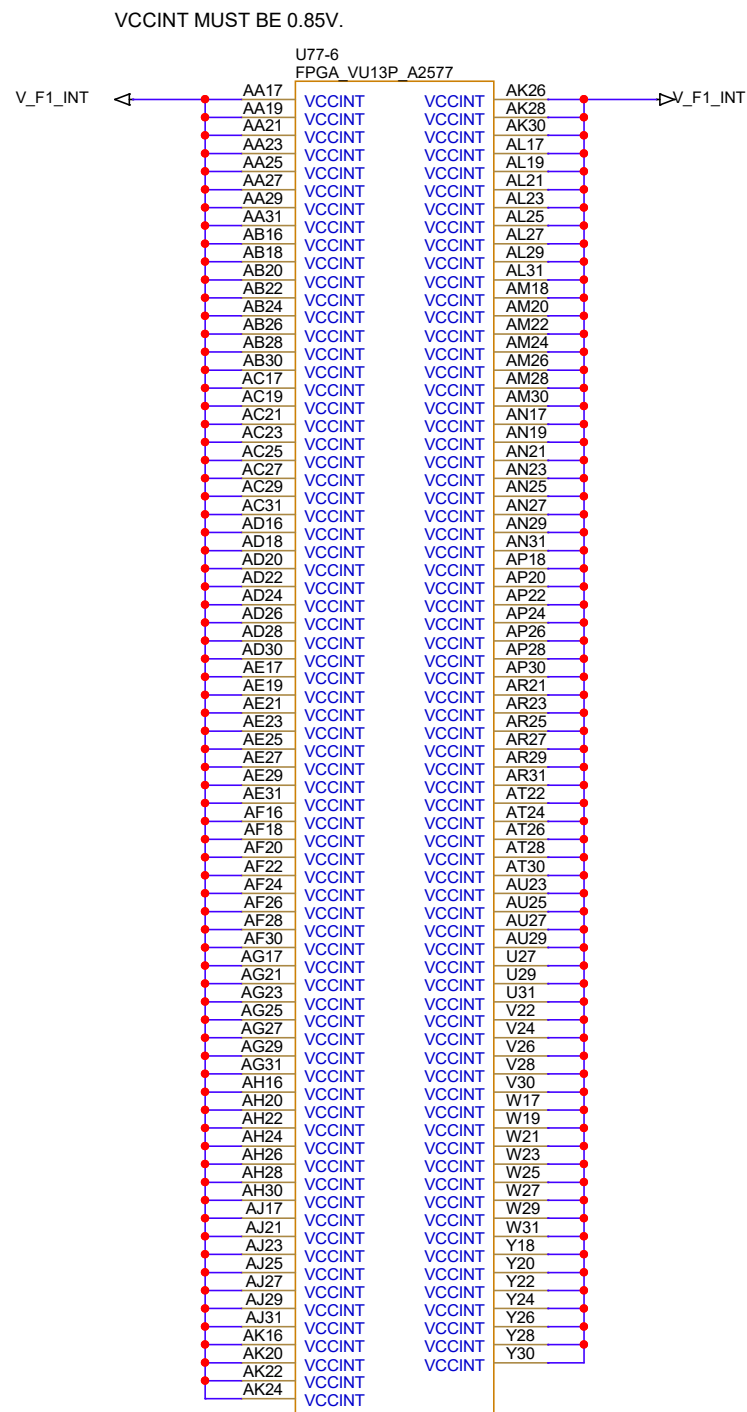
I2C REGISTER PIN ASSIGNMENTS ARE SCRAMBLED COMPARED TO PREVIOUS CM VERSIONS



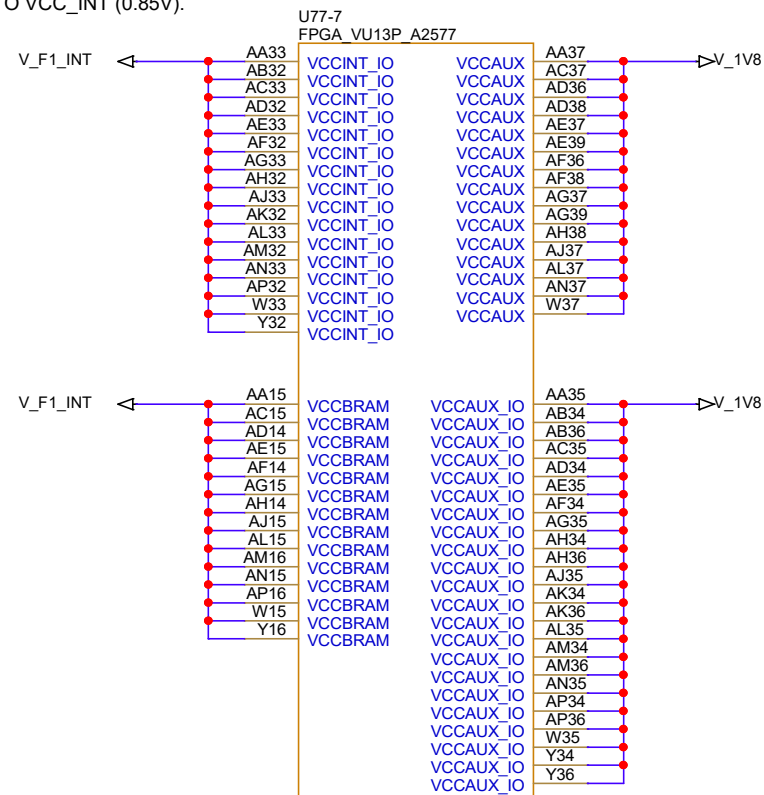
5.01: FPGA#1 GND



## 5.02: FPGA#1 POWER INTERNAL

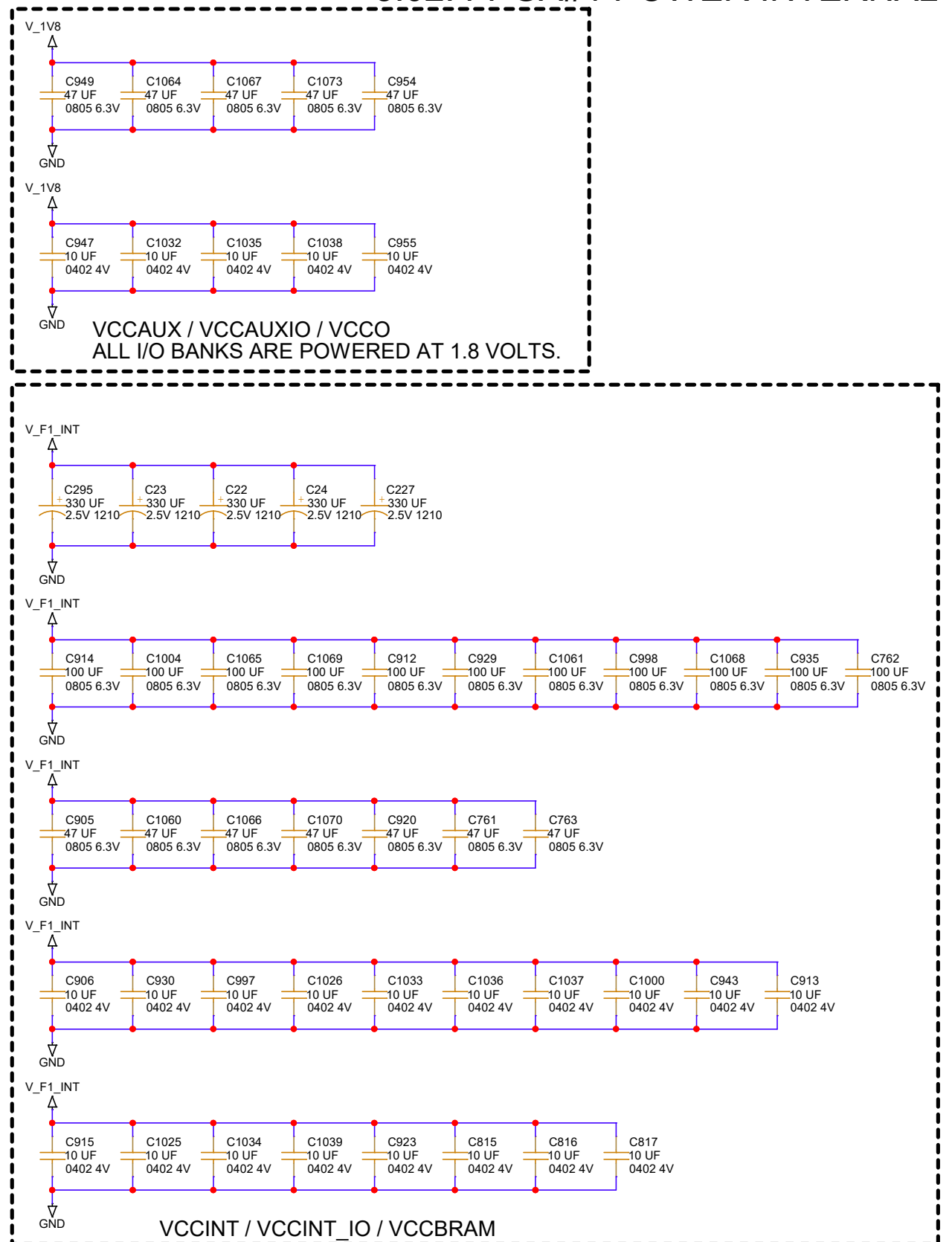


VCCINT\_IO MUST BE CONNECTED TO VCC\_INT (0.85V).



VCCBRAM CAN BE CONNECTED TO VCC\_INT (0.85V).

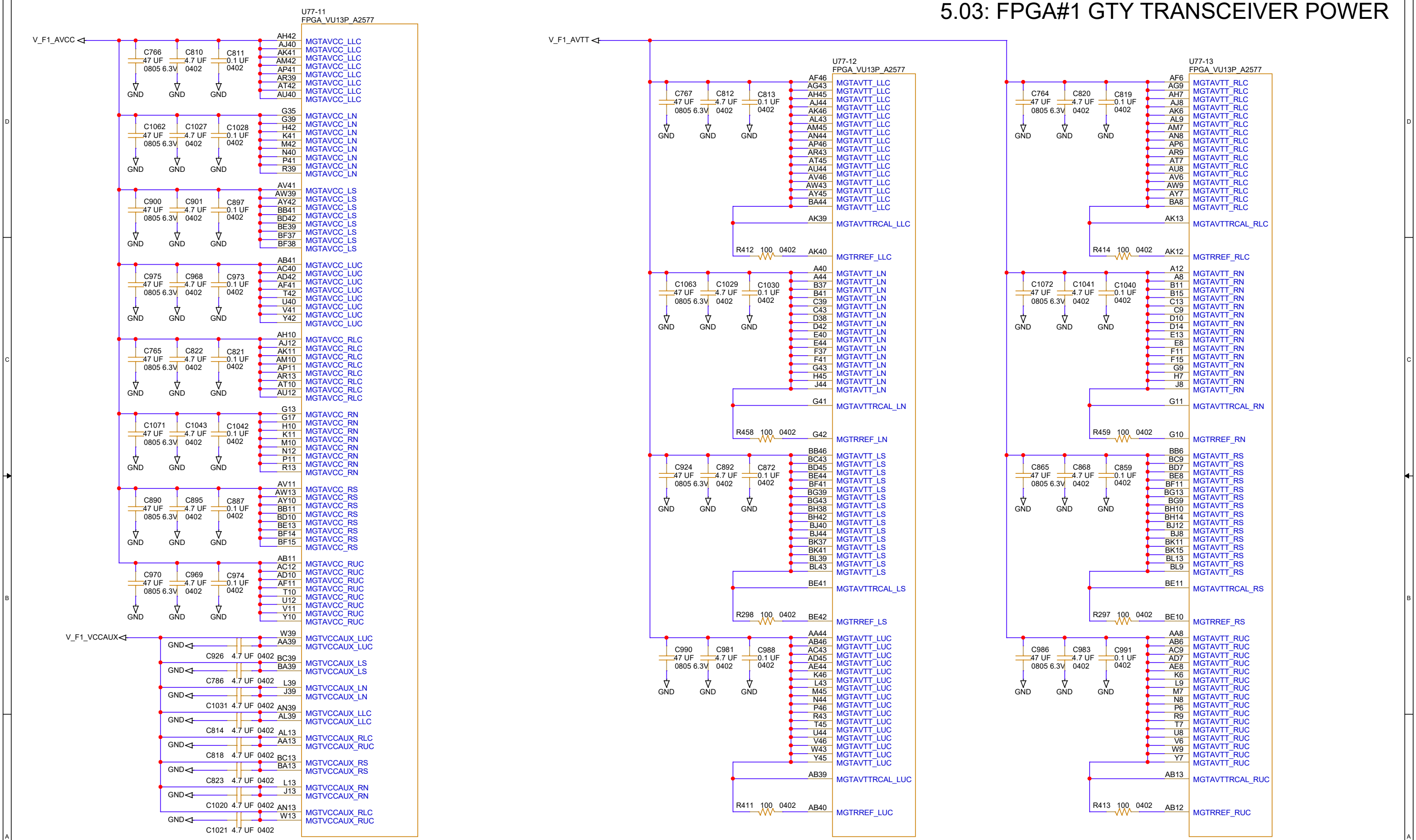
VCCAUX\_IO MUST BE  
CONNECTED TO VCCAUX (1.8V).



## BYPASS CAPACITOR VALUES AND QUANTITIES FROM "UG583 UltraScale Architecture PCB Design"

<b>APOLLO CM v3</b>			
Title			
<b>5.02: FPGA#1 POWER INTERNAL</b>			
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5.03: FPGA#1 GTY TRANSCEIVER POWER



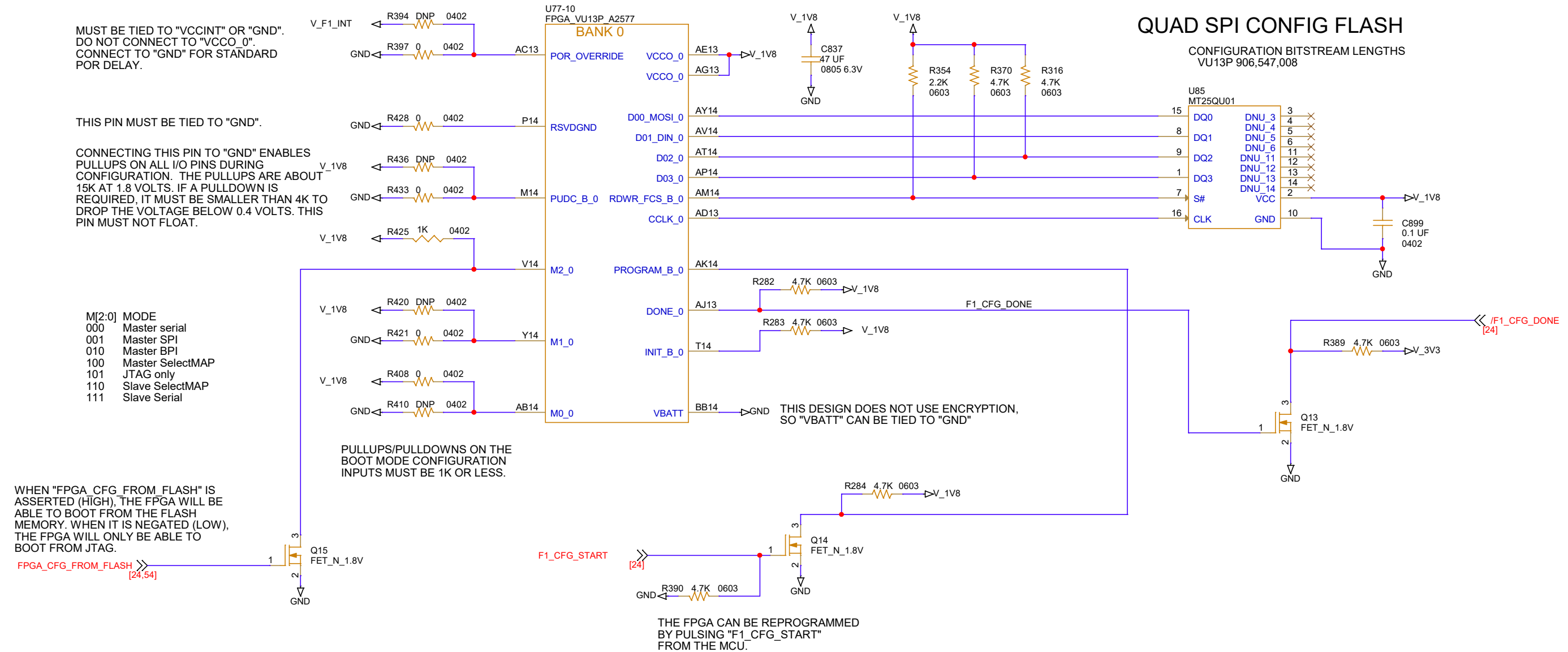
REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM v3			
Title			
5.03: FPGA#1 GTY TRANSCEIVER POWER			
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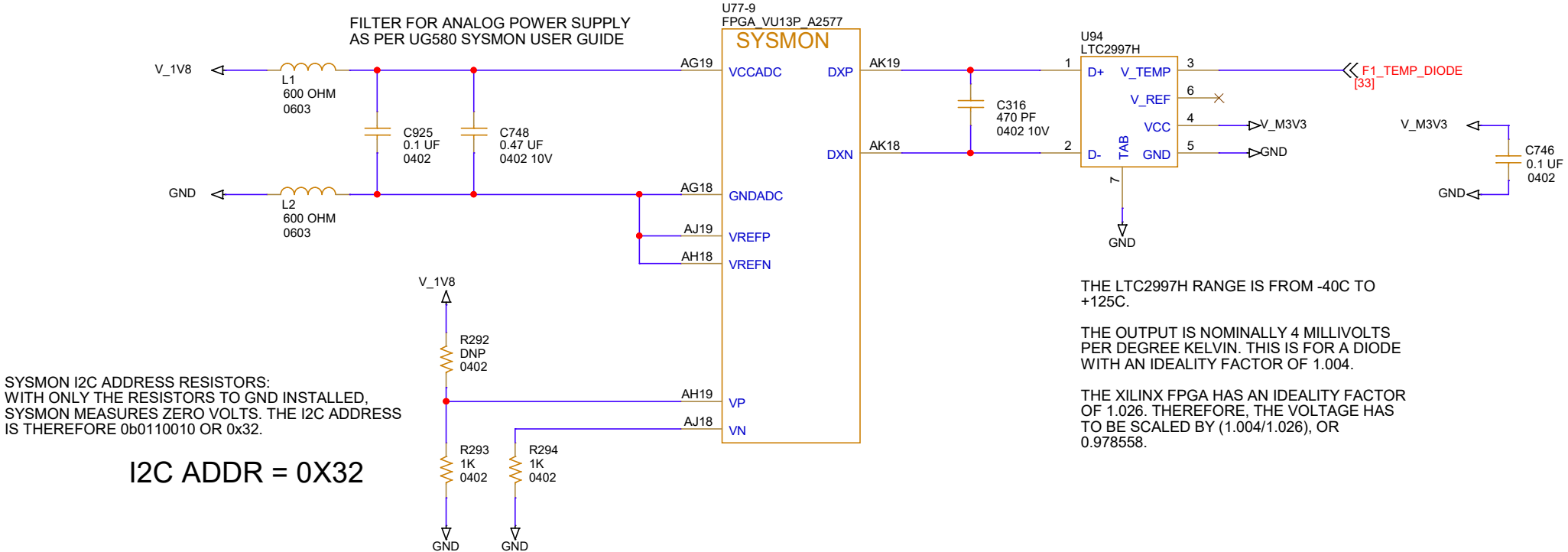
## 5.04: FPGA#1 CONFIGURATION

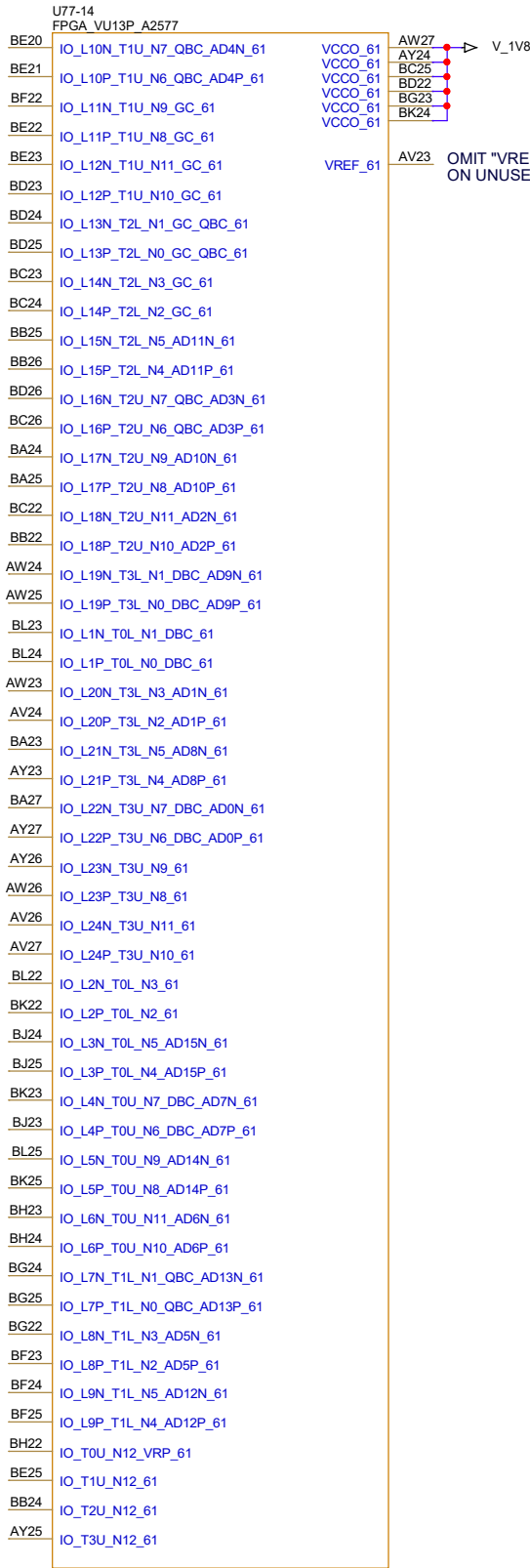


FOR THE VU9P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0 AND SLR2.

FOR THE VU13P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0, SLR2, AND SLR3.

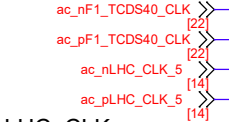
ONLY THE MASTER SLR IS ACCESSABLE FROM THE I2C CONNECTIONS.



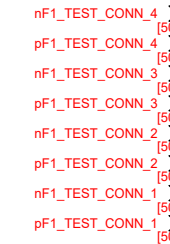
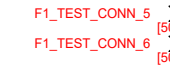
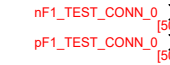


OMIT "VREF" AND "VRP" RESISTORS  
ON UNUSED I/O BANKS.

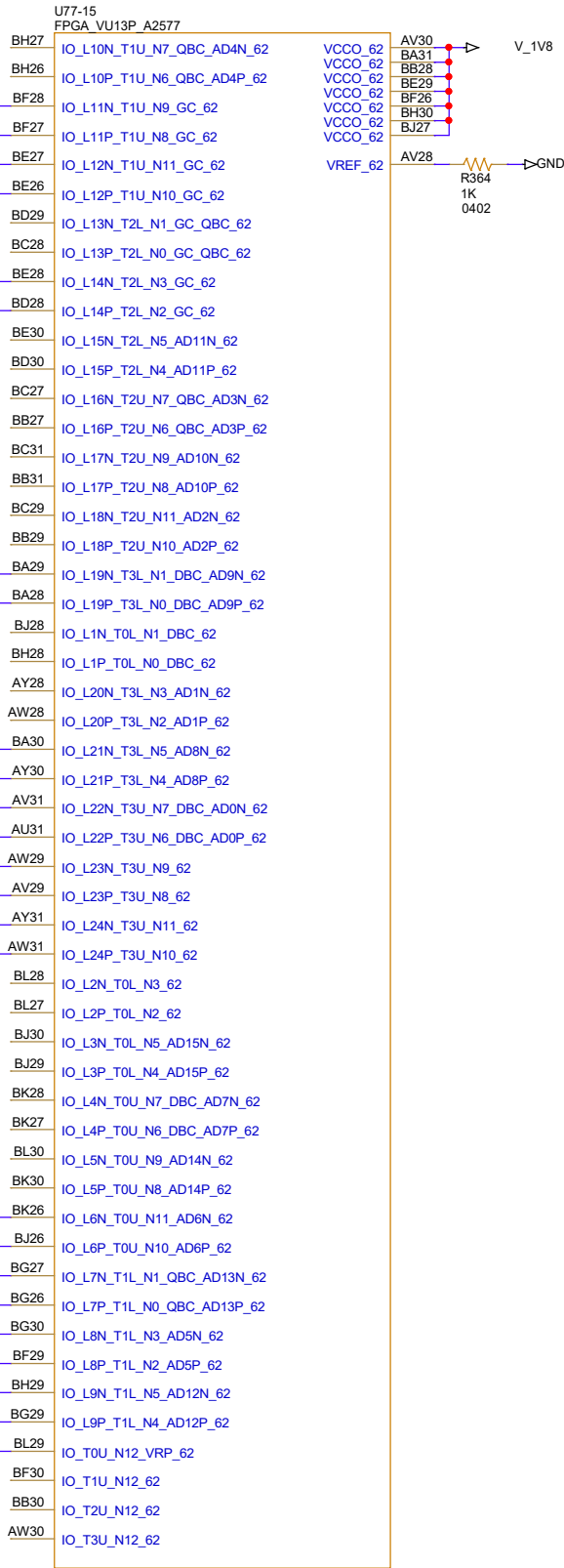
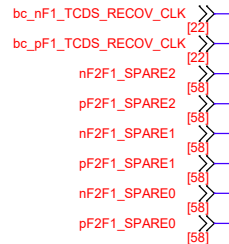
F1 LOGIC  
TCDS 40MHZ INPUT



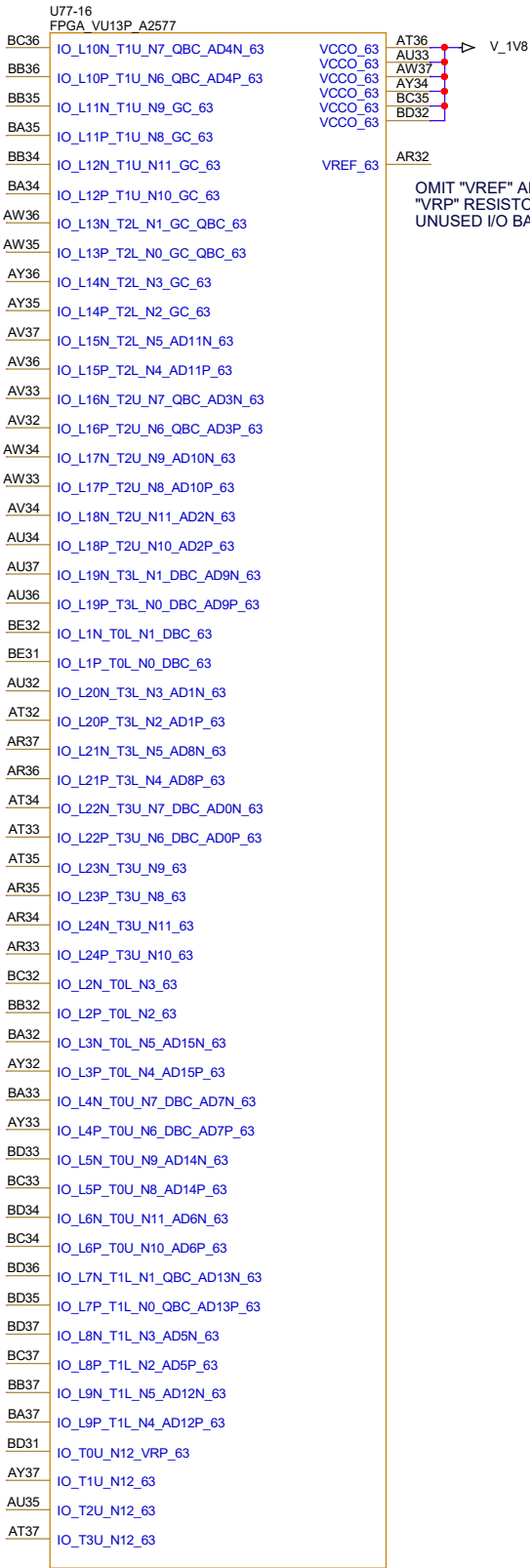
LHC\_CLK  
ALWAYS 40 MHZ



THIS IS THE 40 MHZ RECOVERED TCDS  
CLOCK. USING BANK 62 KEEPS THIS  
INTHE SAME SLR AS THE TCDS LOGIC.



OMIT "VREF" AND  
"VRP" RESISTORS ON  
UNUSED I/O BANKS.



OMIT "VREF" AND  
"VRP" RESISTORS ON  
UNUSED I/O BANKS.

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Title  
5.06 FPGA#1 I/O SLR0

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THE SYSTEM MONITOR I2C PORTS ON THE  
FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE  
TCA9548A ACTS AS A LEVEL SHIFTER AS WELL  
AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS  
CONNECT TO 1.8 VOLTS.

I2C\_SDA\_F1\_SYSMON [38]  
I2C\_SCL\_F1\_SYSMON [38]

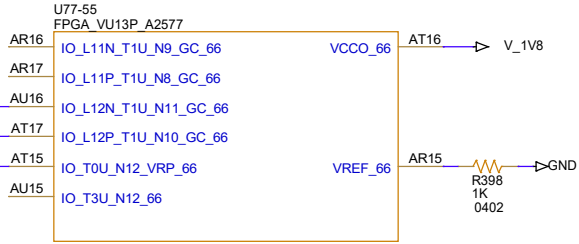
BANK 65 CONTAINS MANY DUAL-FUNCTION  
PINS THAT CAN BE USED DURING  
CONFIGURATION. THOSE PINS WILL BE  
MARKED AS "NO CONNECT" AND SHOULD  
NOT BE USED FOR NORMAL LOGIC.

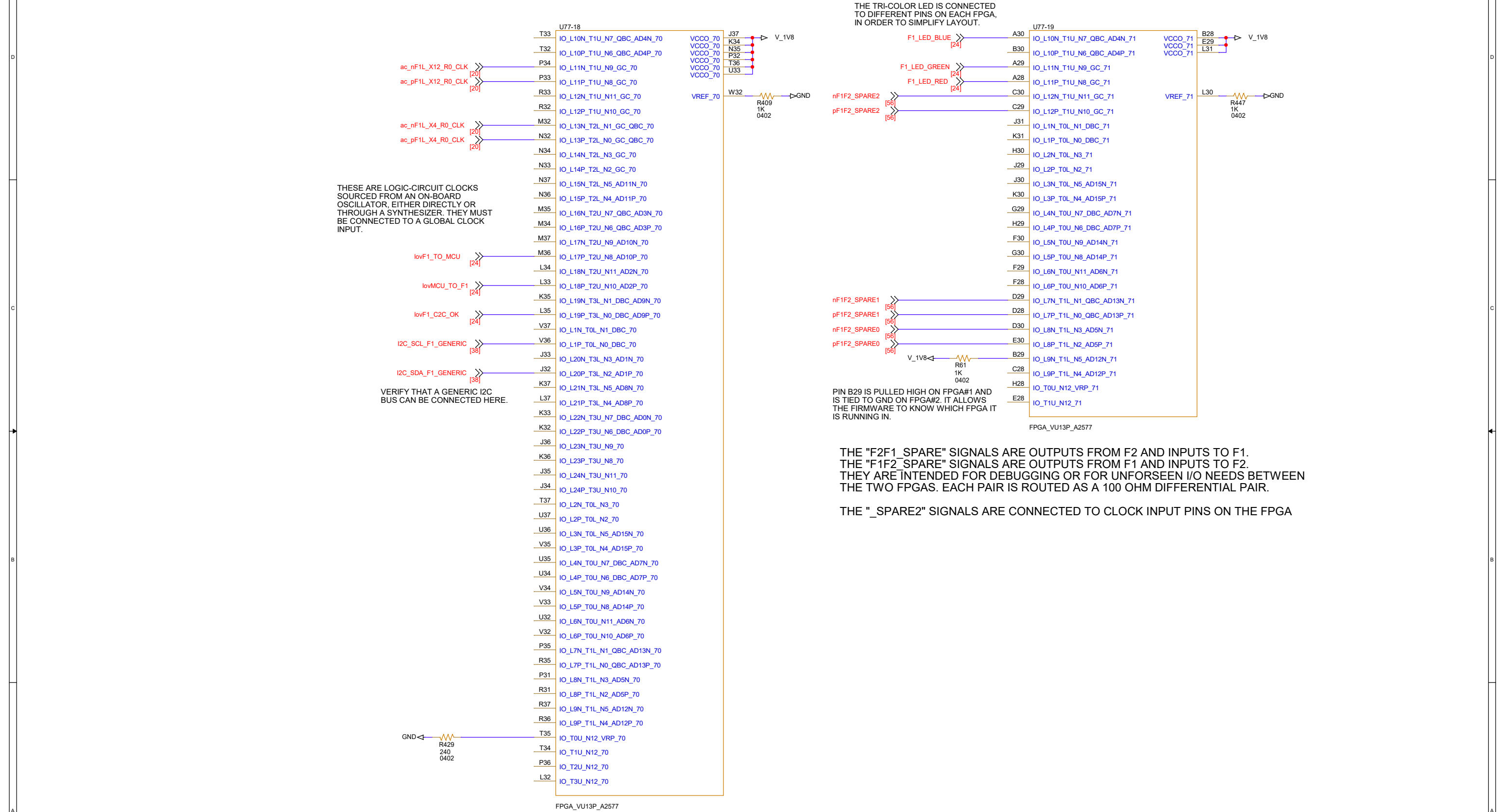
GND< R357  
240  
0402



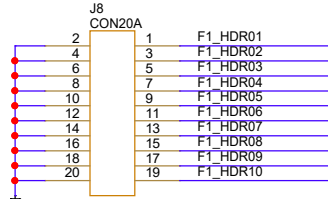
ac\_nF1\_XTAL\_200 [17]  
ac\_pF1\_XTAL\_200 [17]  
GND

R372  
240  
0402

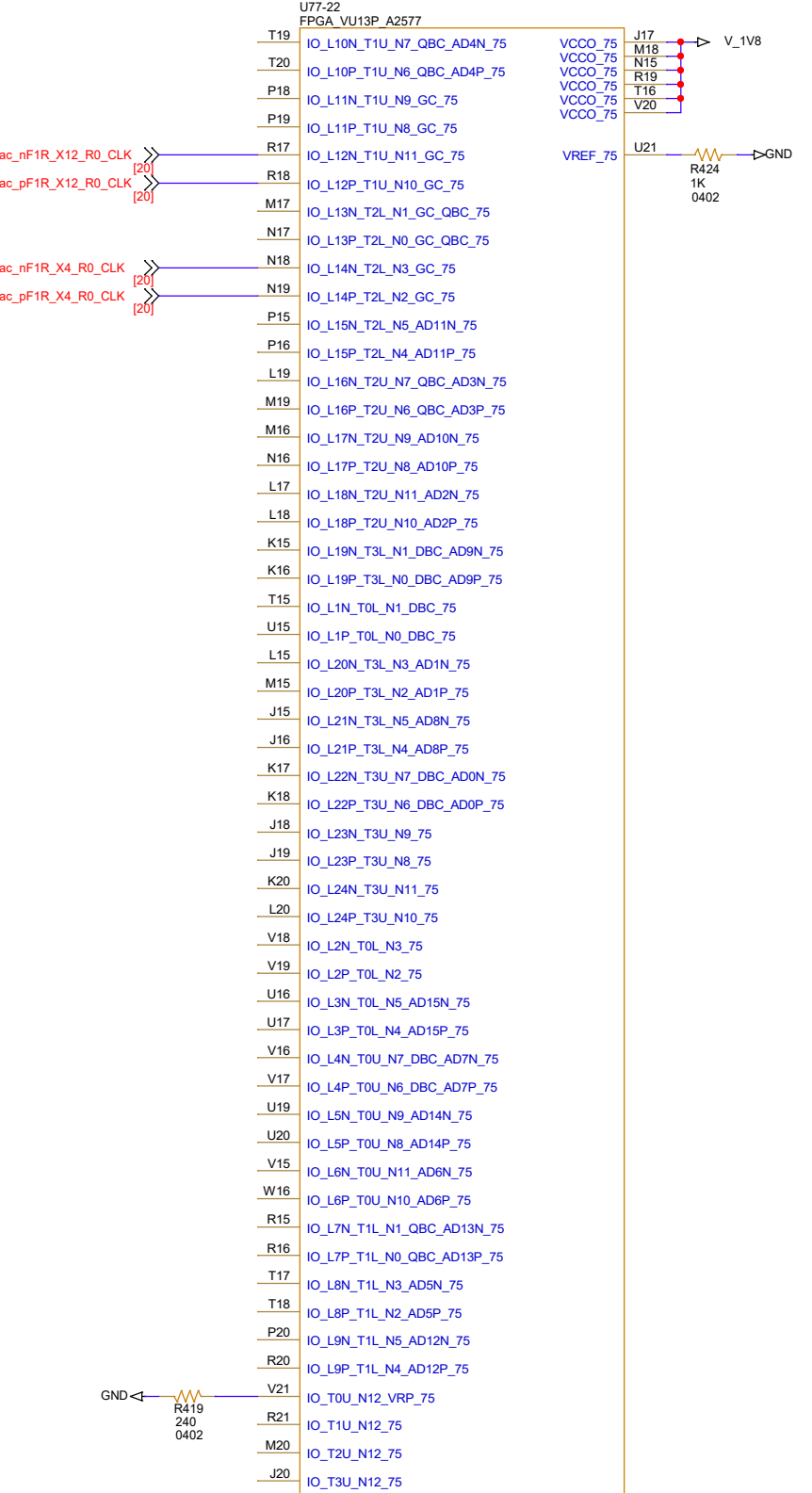
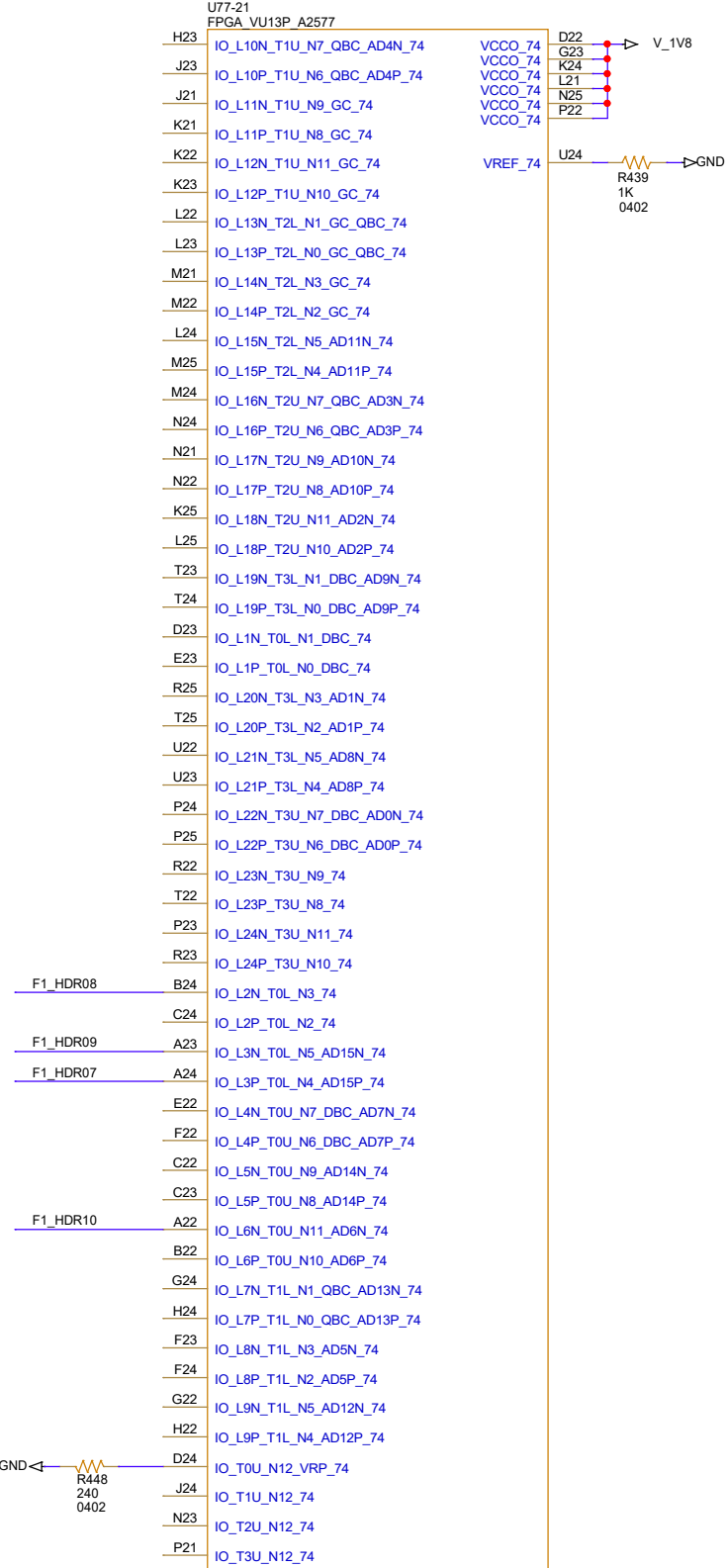
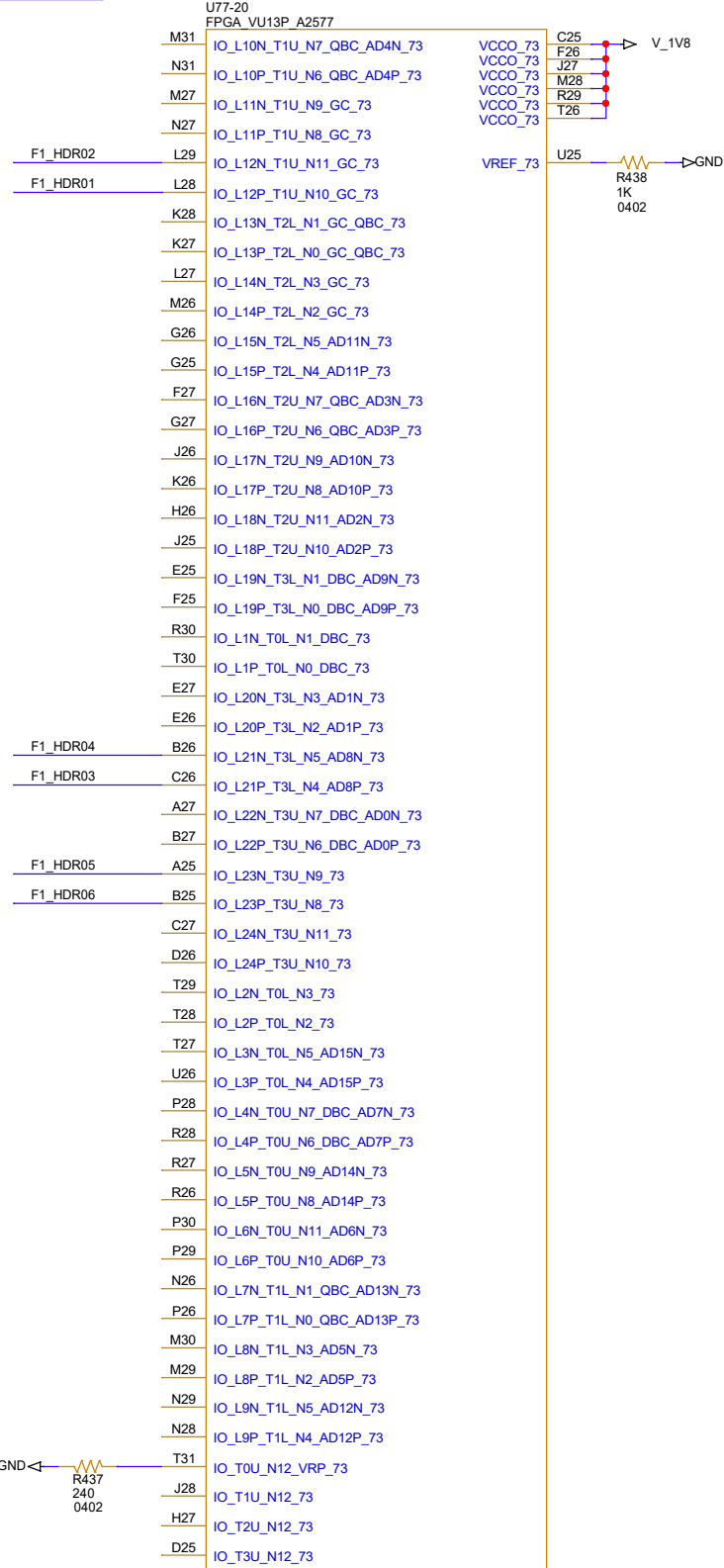




## 5.09: FPGA#1 I/O SLR3



THE "F1\_HDRnn" SIGNALS ARE CONNECTED FROM THE FPGA TO PADS ON THE BOTTOM SIDE OF THE BOARD. A 20-PIN HEADER CAN BE ATTACHED. THESE SIGNALS ARE FOR DEBUGGING, OR FUTURE USE. HDR01 AND HDR02 ARE CONNECTED TO CLOCK-CAPABLE INPUTS.



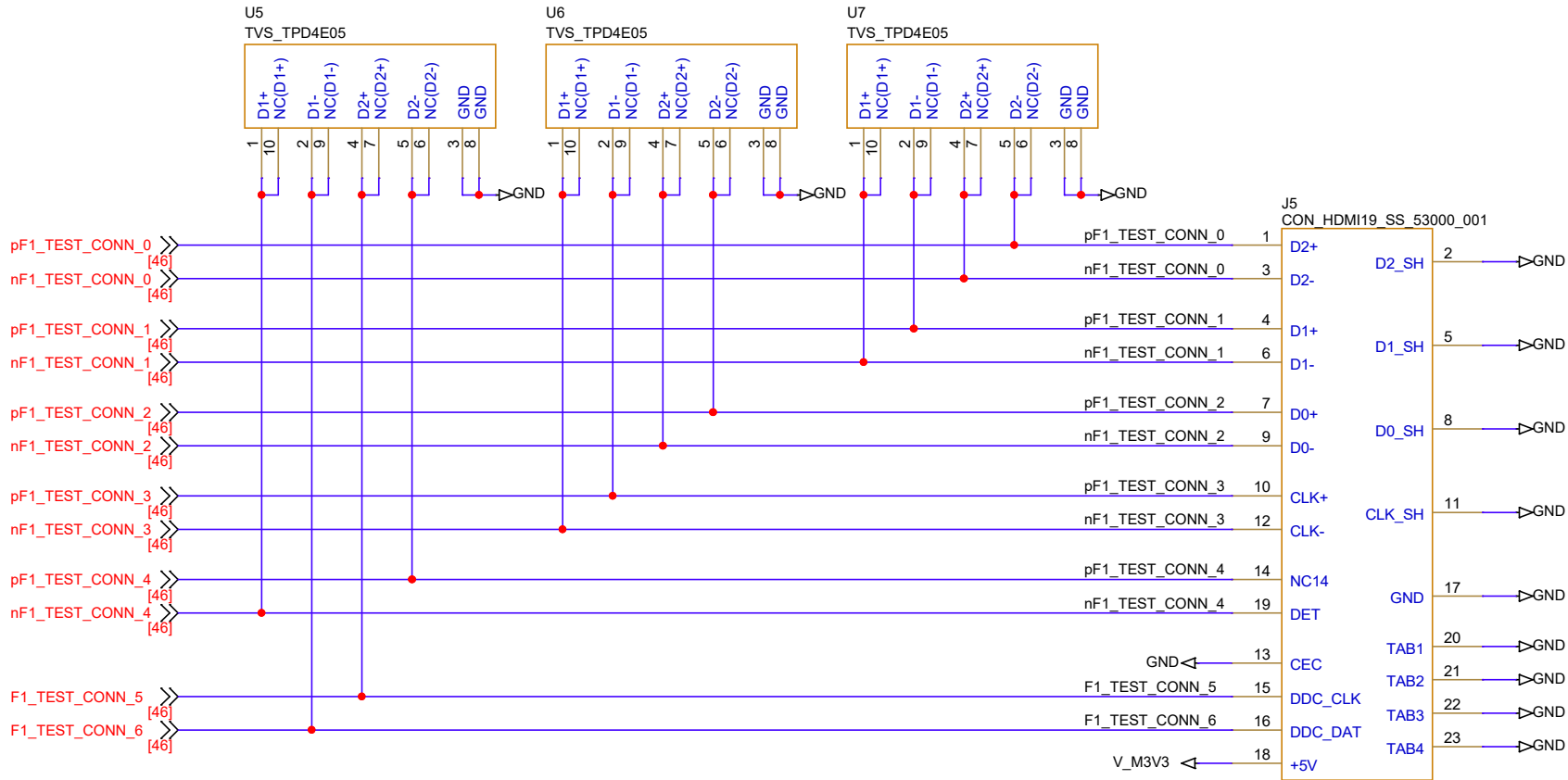


THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

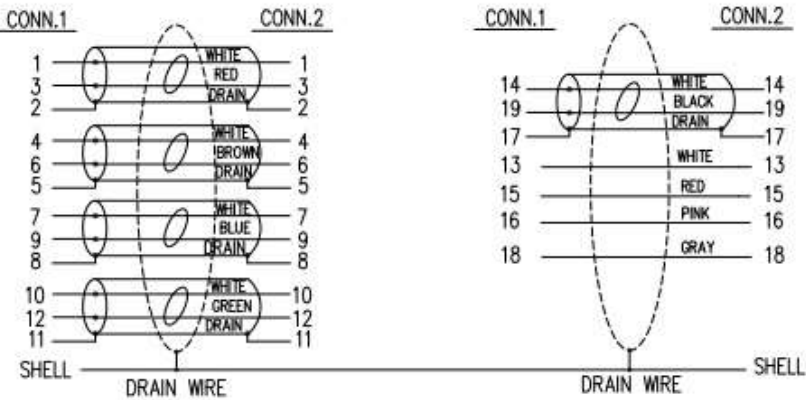
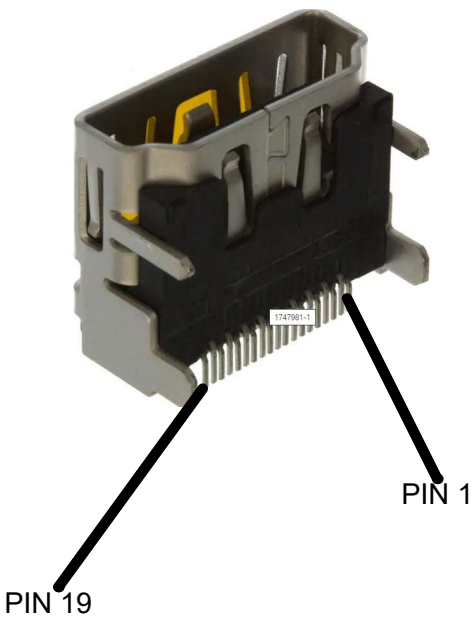
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

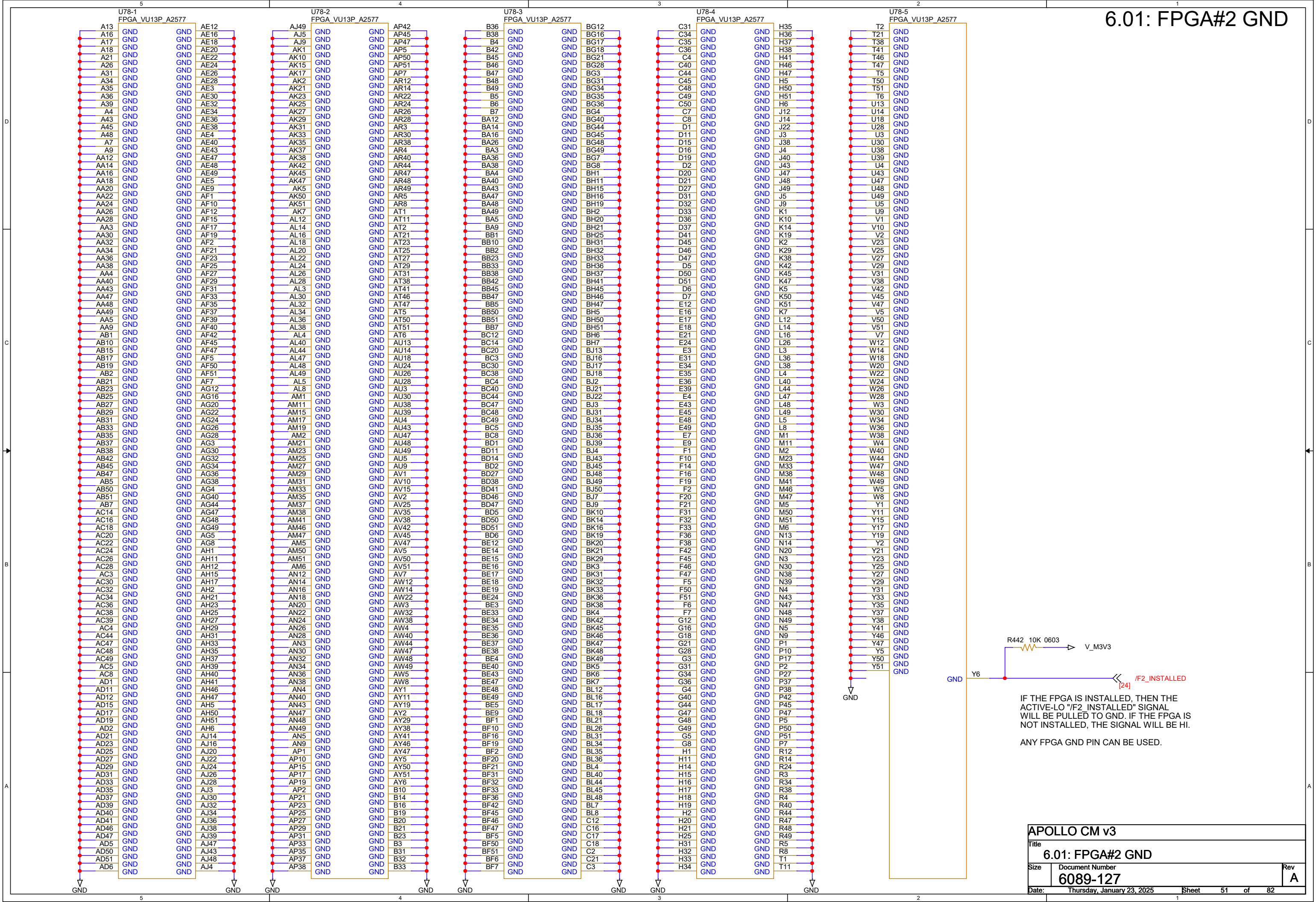
THE "F1\_TEST\_CONN\_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.

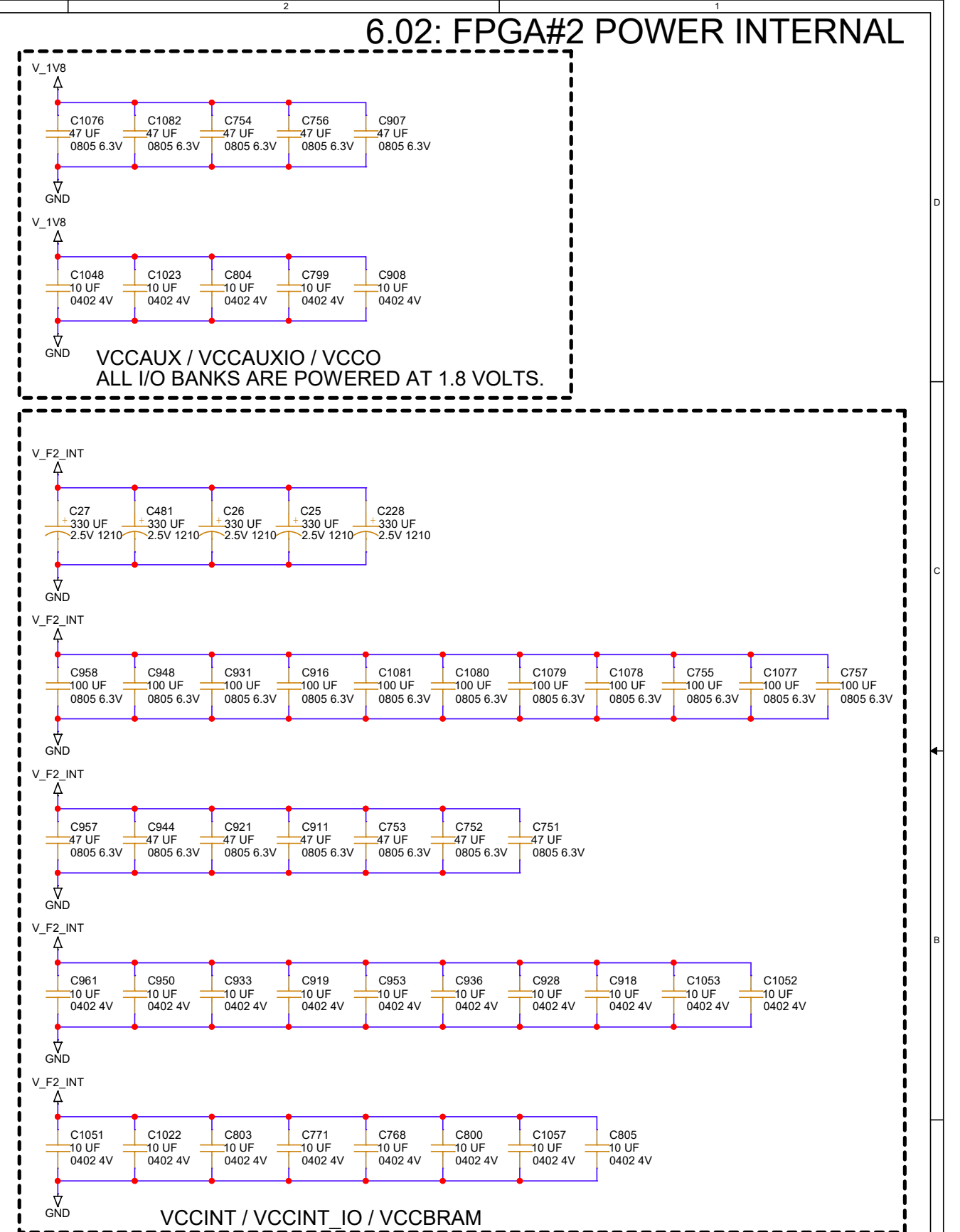
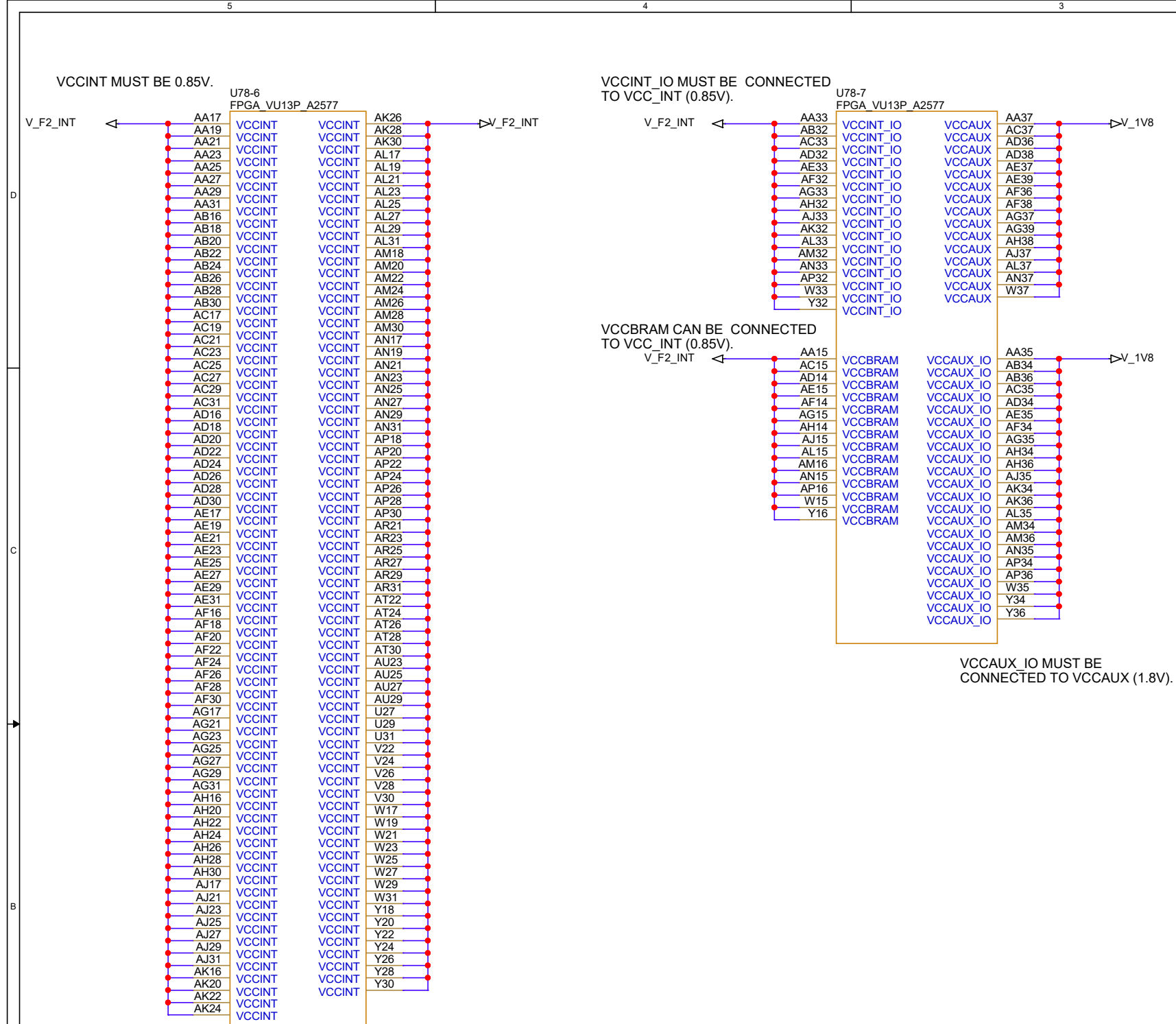


PIN ASSIGNMENT



6.01: FPGA#2 GND

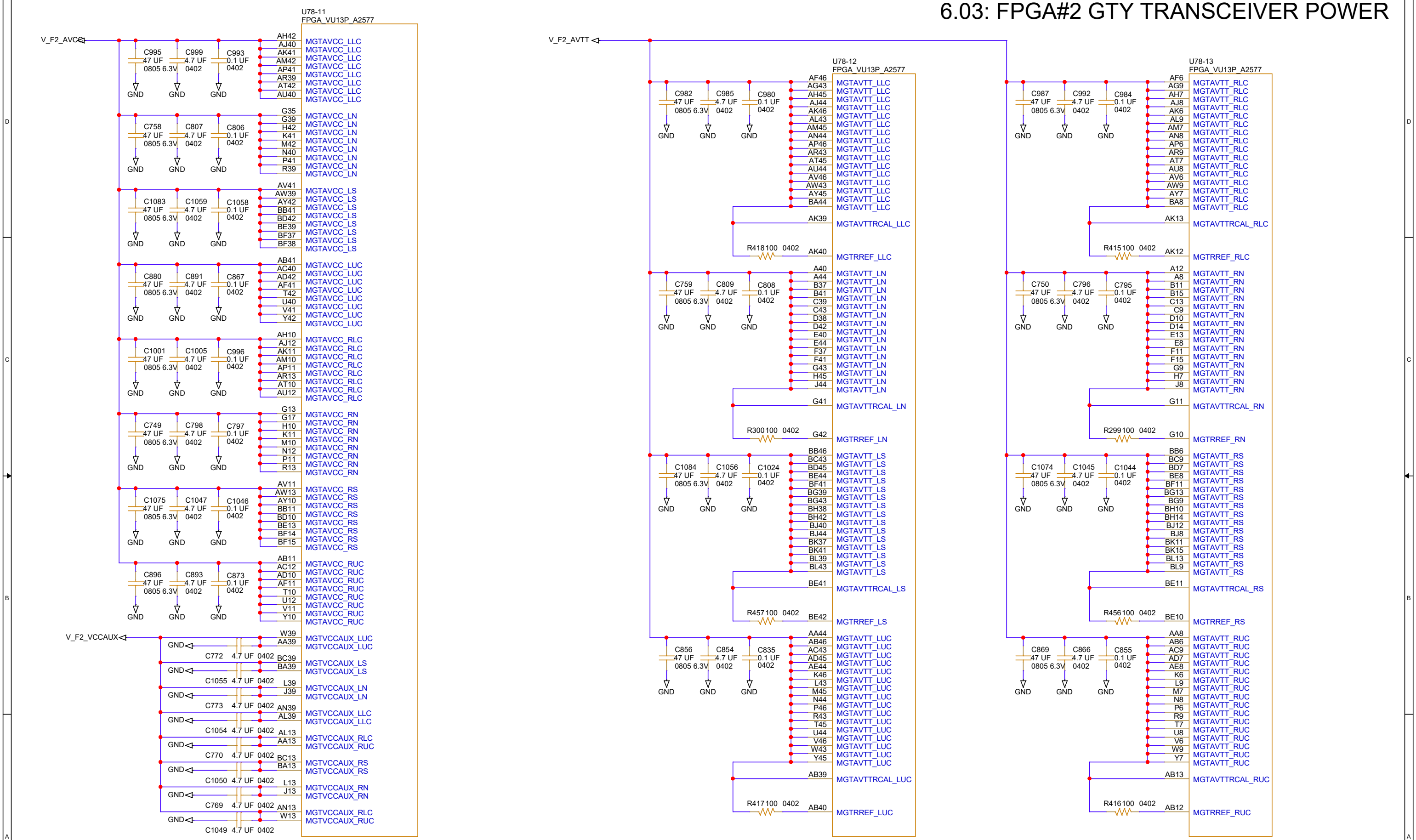




## BYPASS CAPACITOR VALUES AND QUANTITIES FROM "UG583 UltraScale Architecture PCB Design"



6.03: FPGA#2 GTY TRANSCEIVER POWER

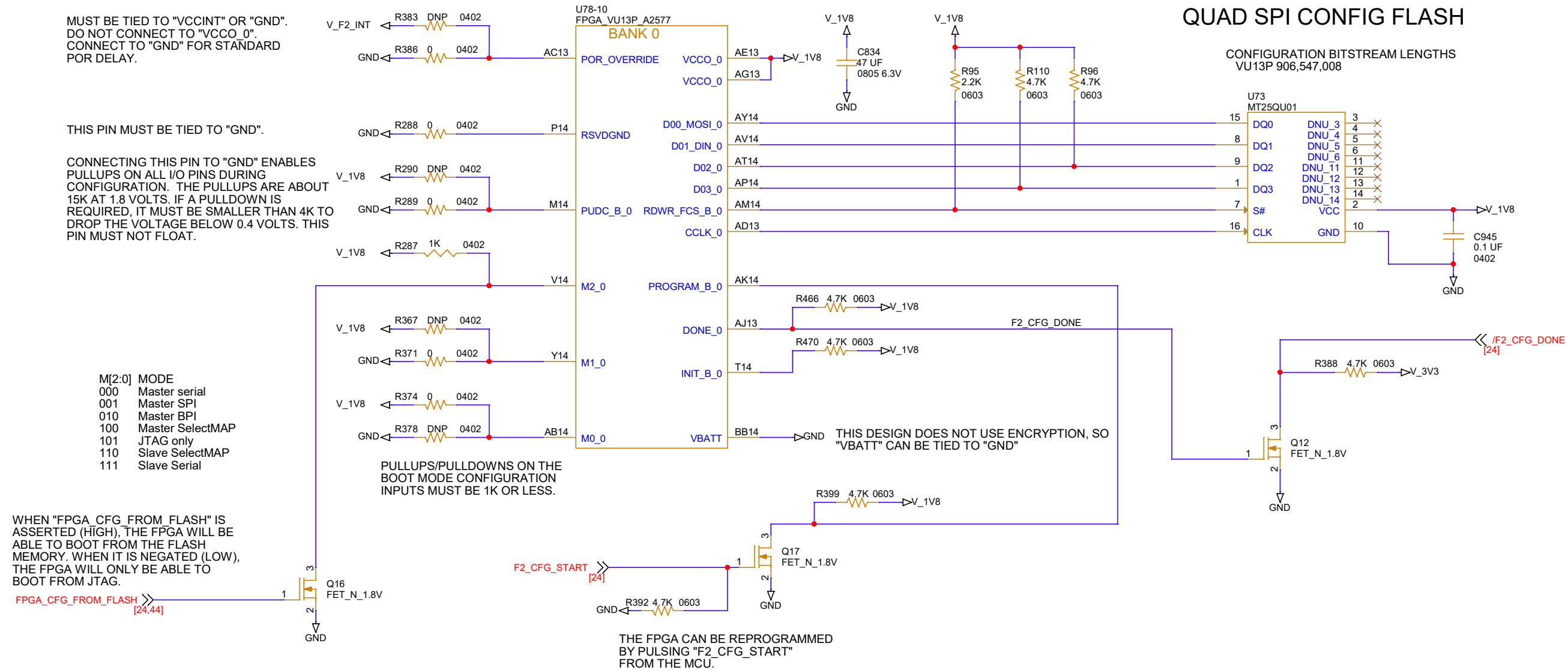


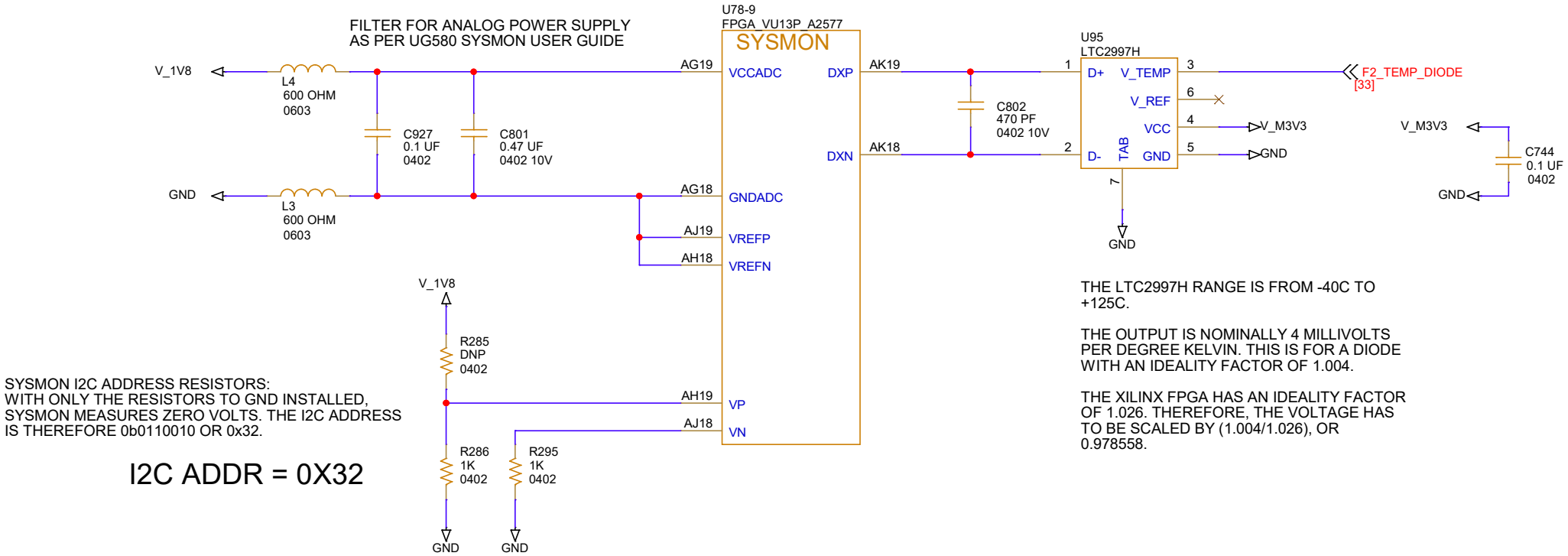
REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

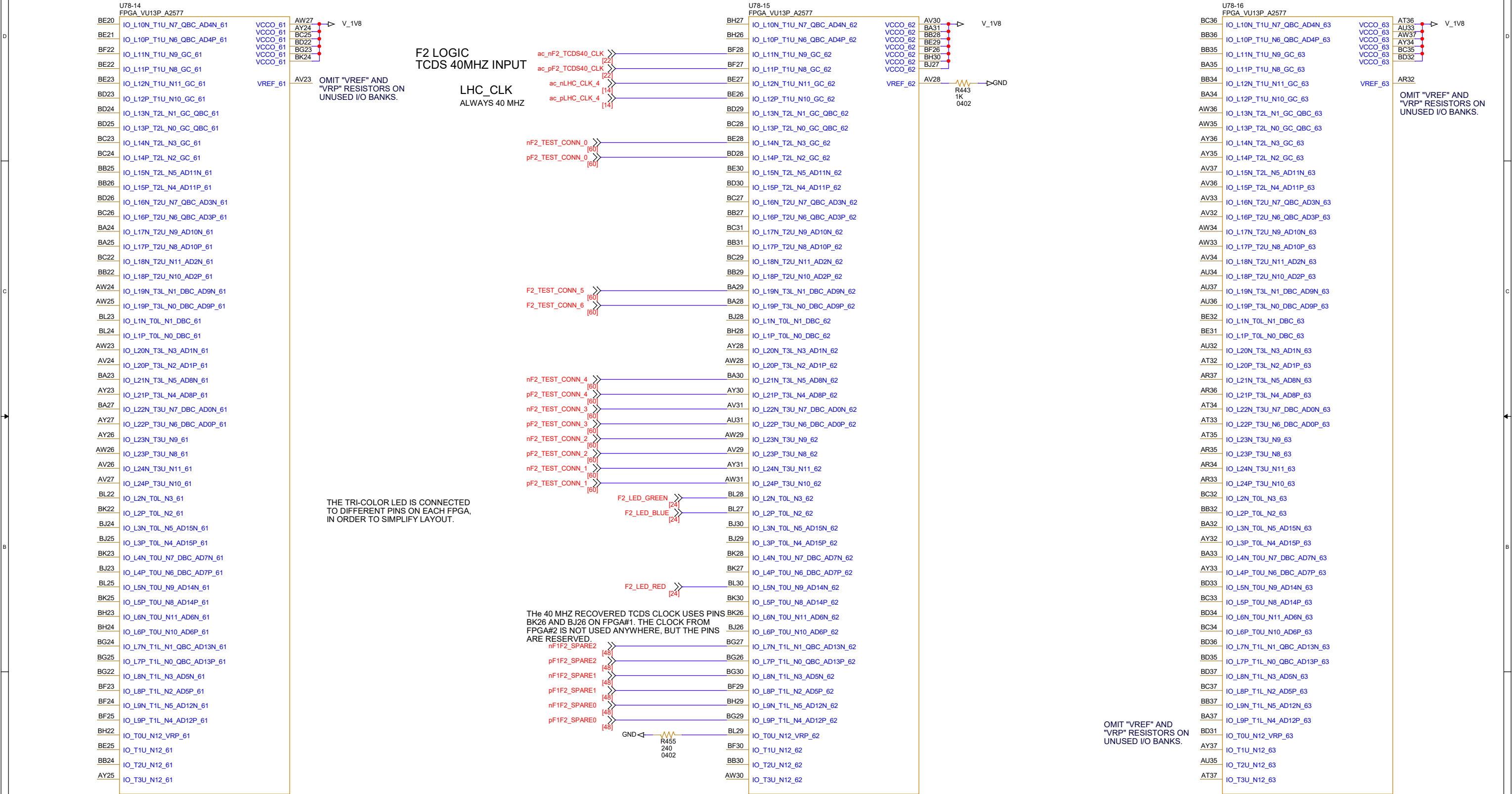
APOLLO CM v3			
Title			
6.03: FPGA#2 GTY TRANSCEIVER POWER			
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## 6.04: FPGA#2 CONFIGURATION









D

C

B

A

D

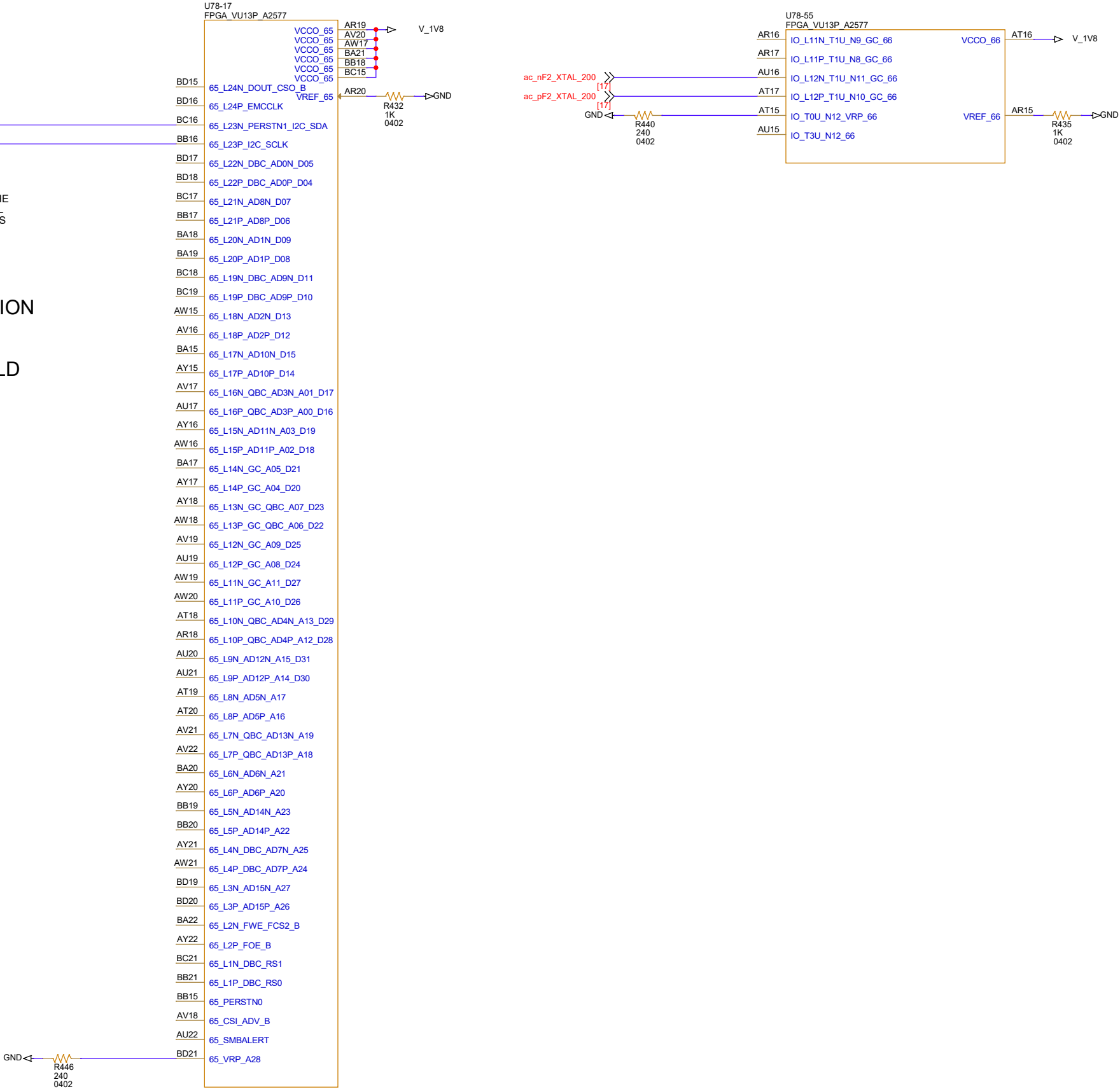
C

B

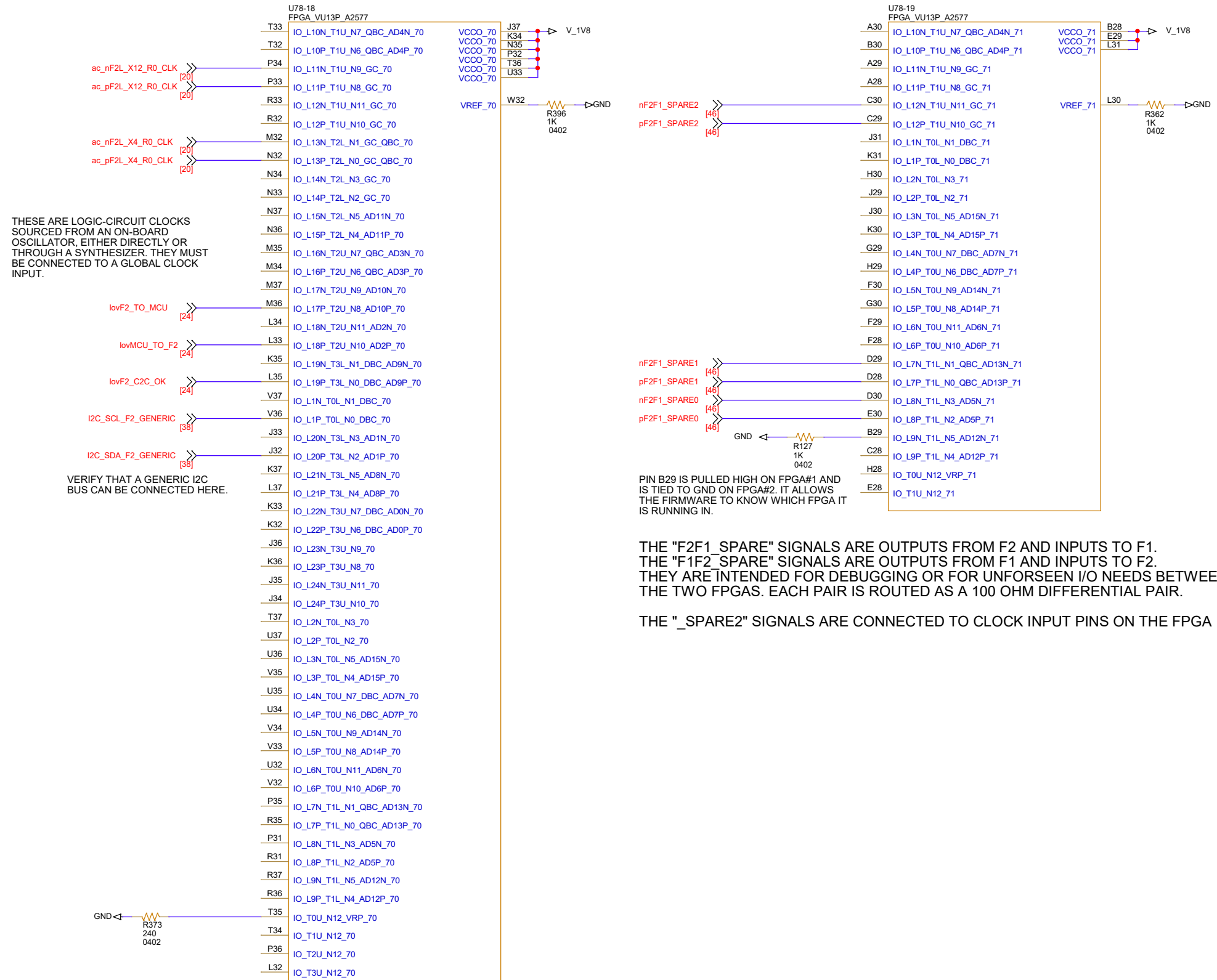
A

THE SYSTEM MONITOR I2C PORTS ON THE  
FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE  
TCA9548A ACTS AS A LEVEL SHIFTER AS WELL  
AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS  
CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION  
PINS THAT CAN BE USED DURING  
CONFIGURATION. THOSE PINS WILL BE  
MARKED AS "NO CONNECT" AND SHOULD  
NOT BE USED FOR NORMAL LOGIC.

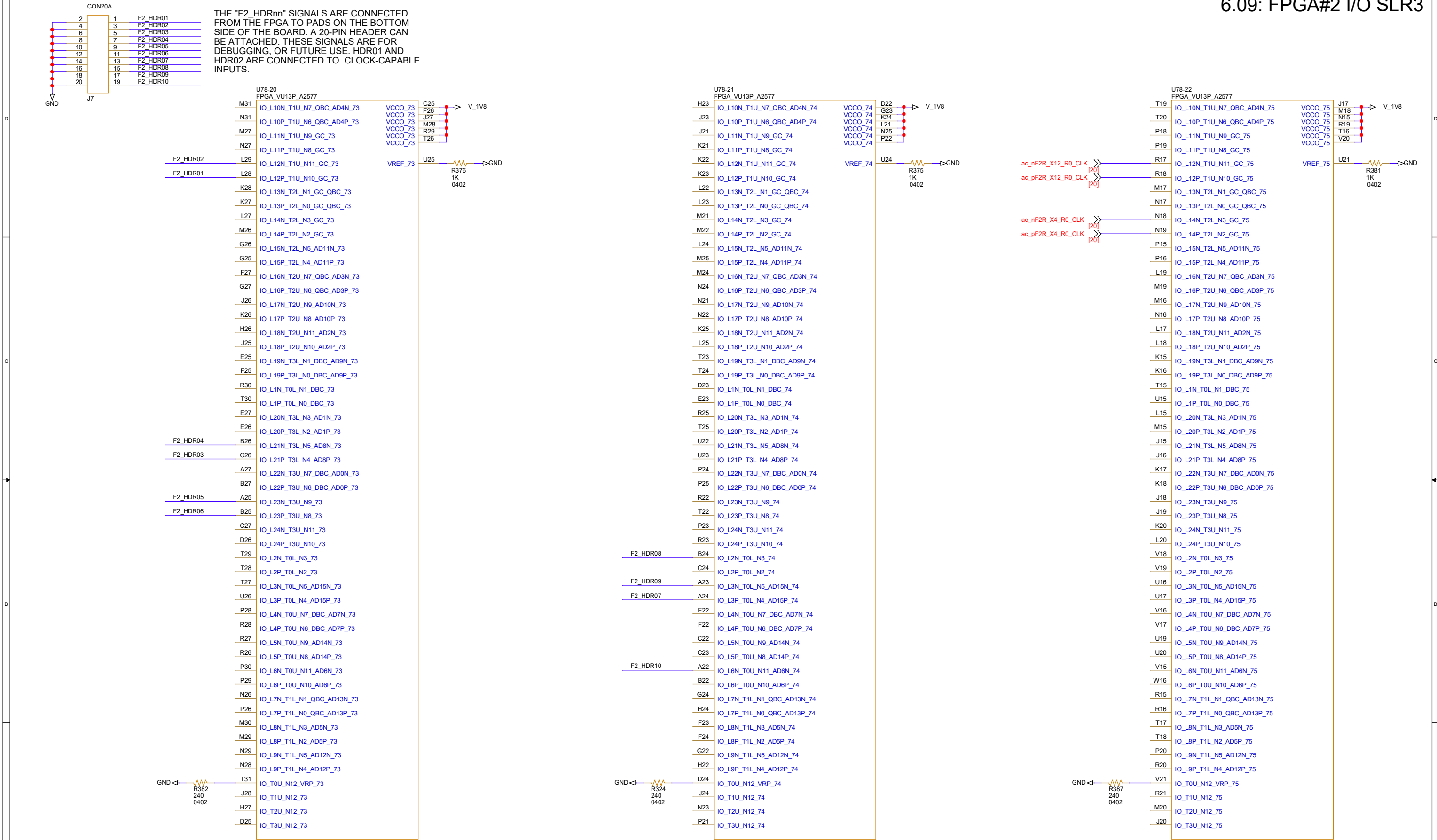


## 6.08: FPGA#2 I/O SLR2





6.09: FPGA#2 I/O SLR3

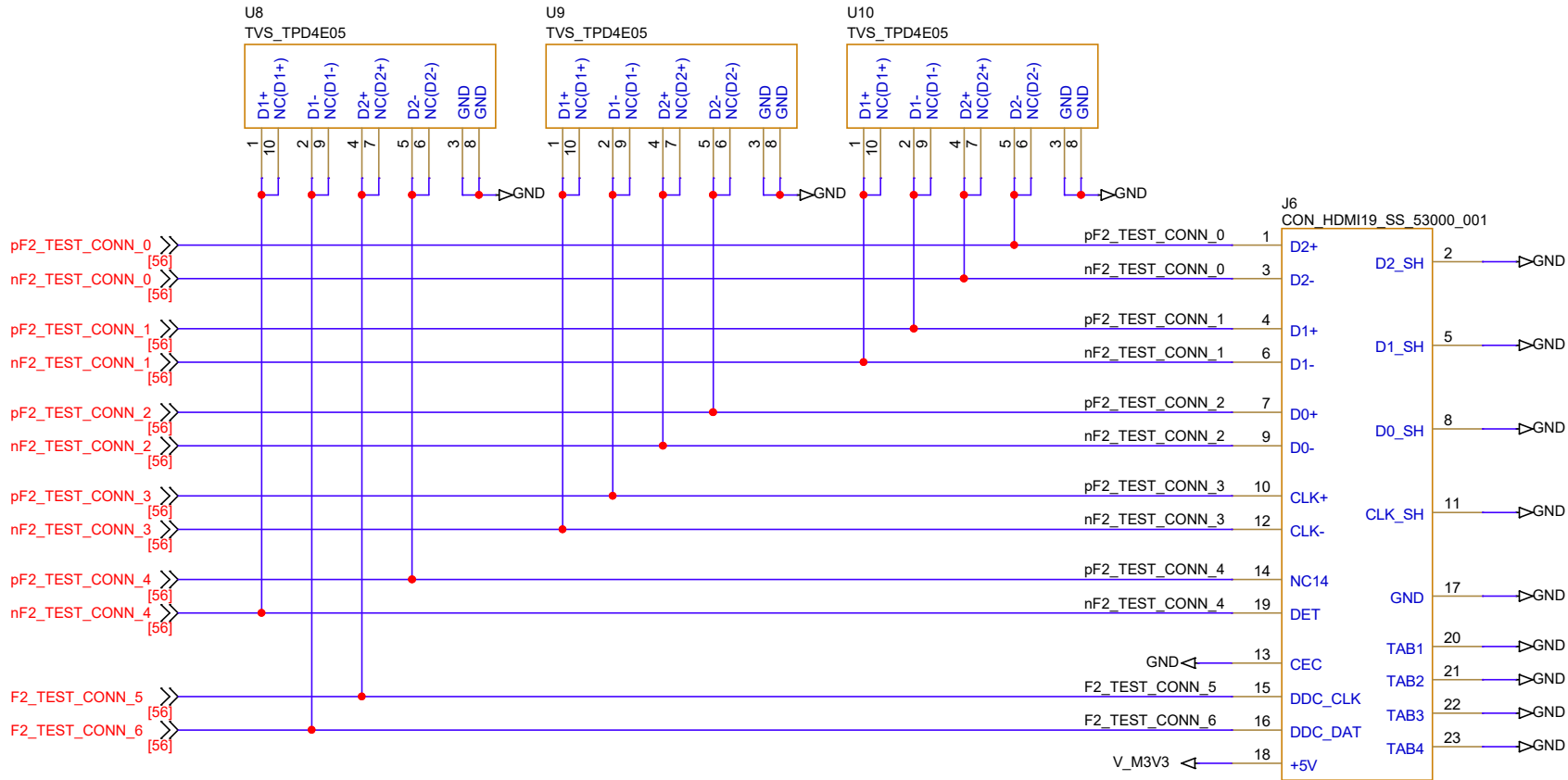


THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

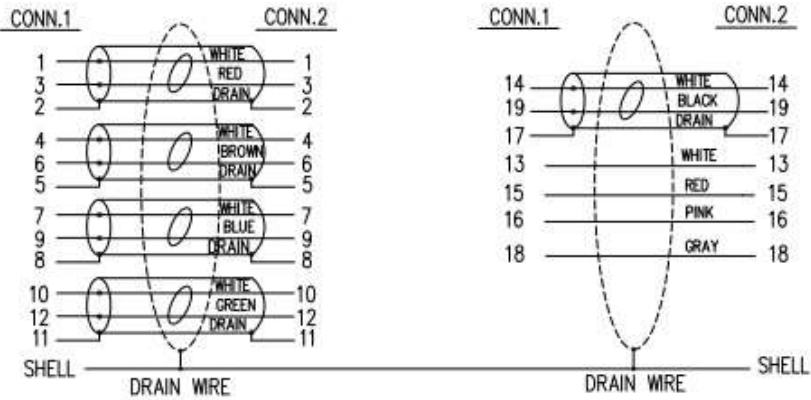
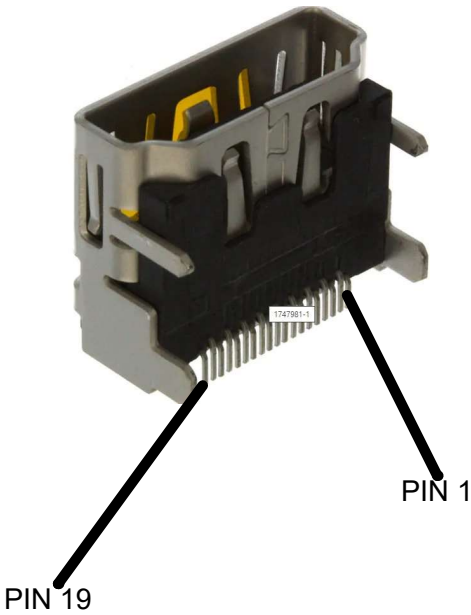
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F2\_TEST\_CONN\_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



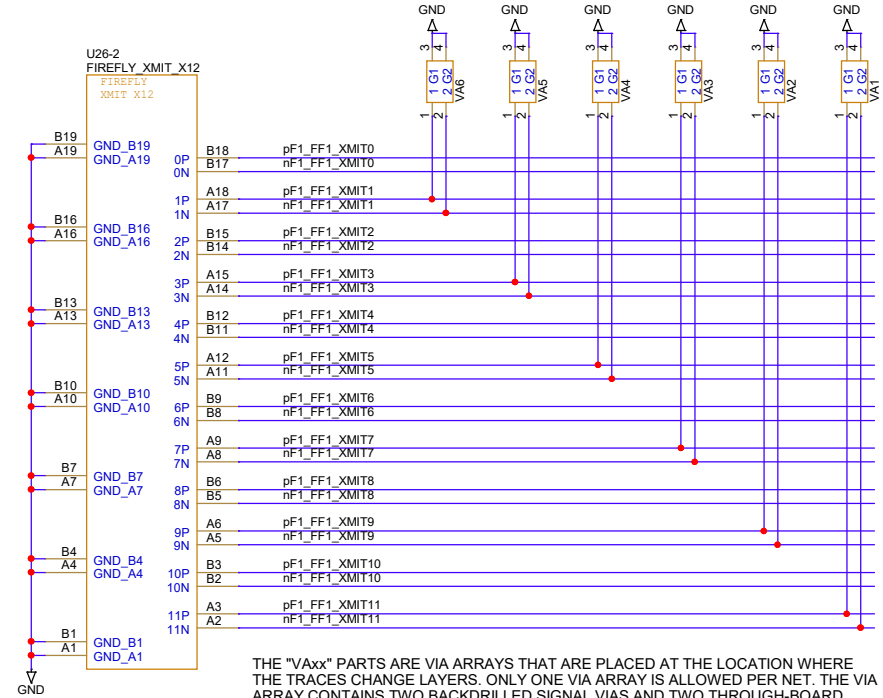
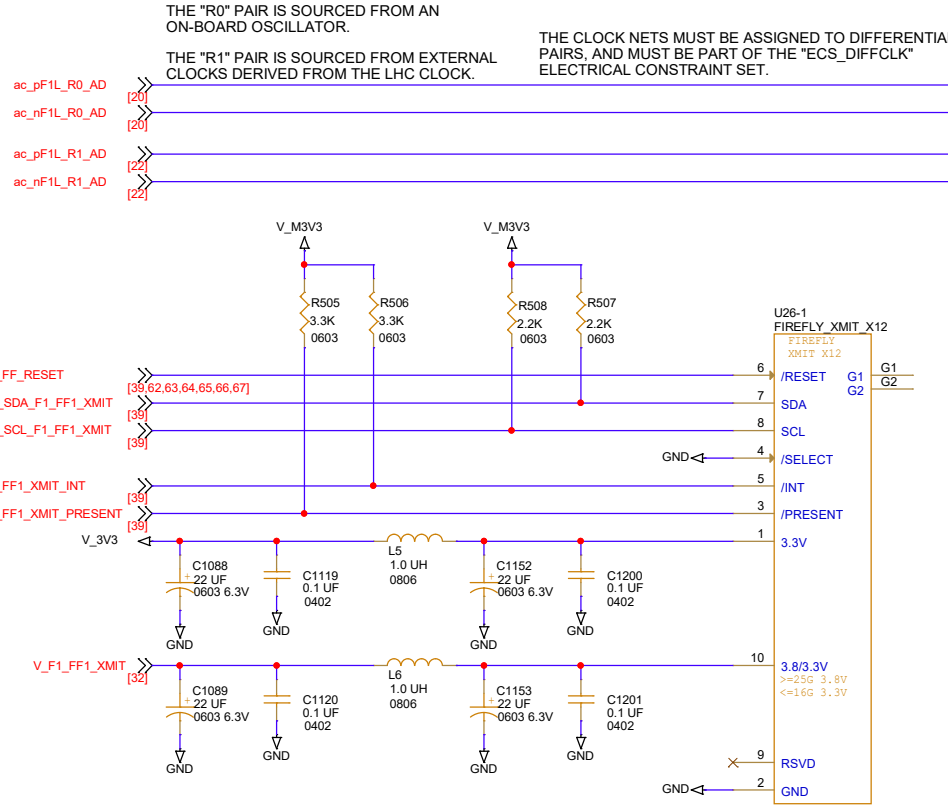
PIN ASSIGNMENT



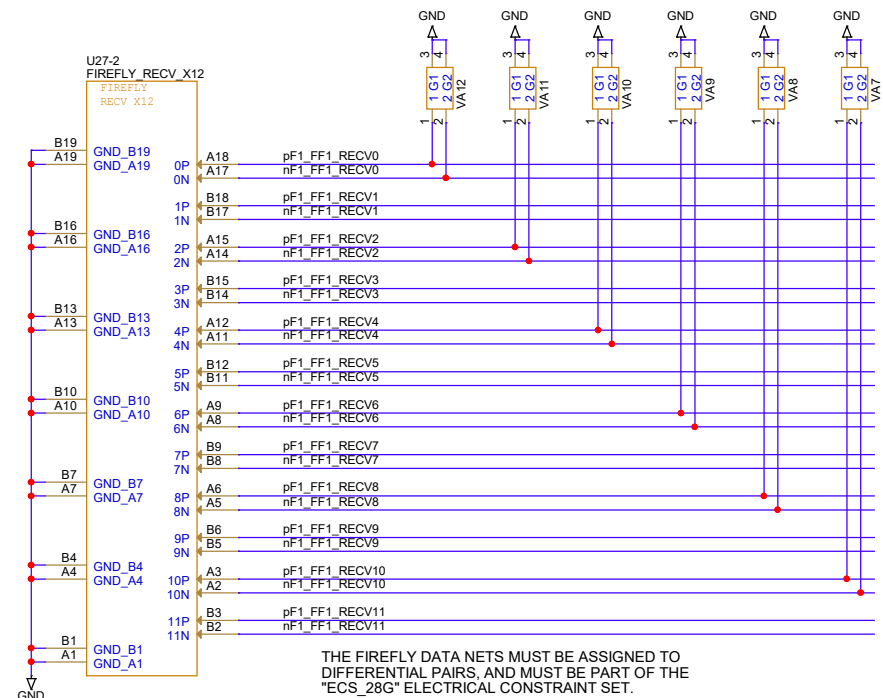
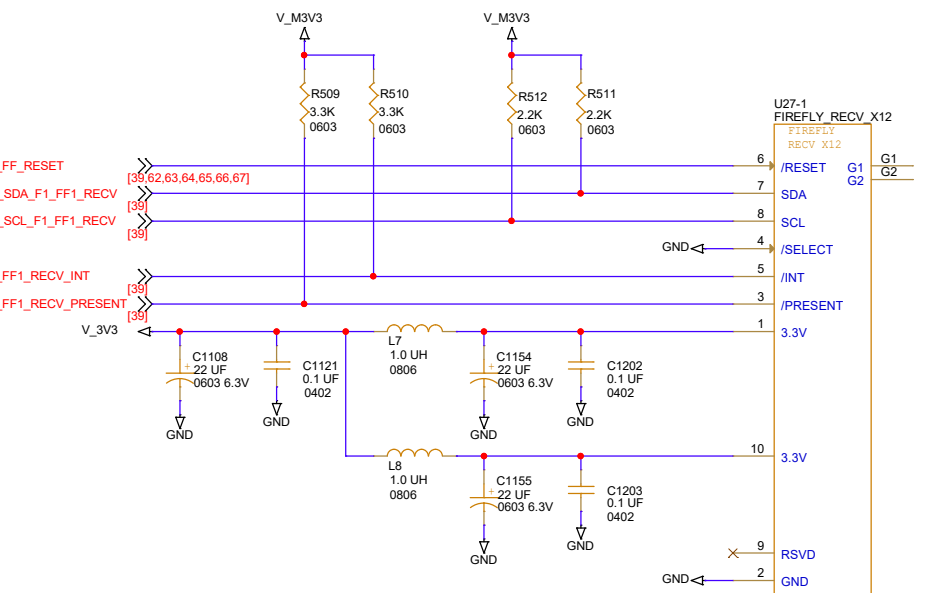
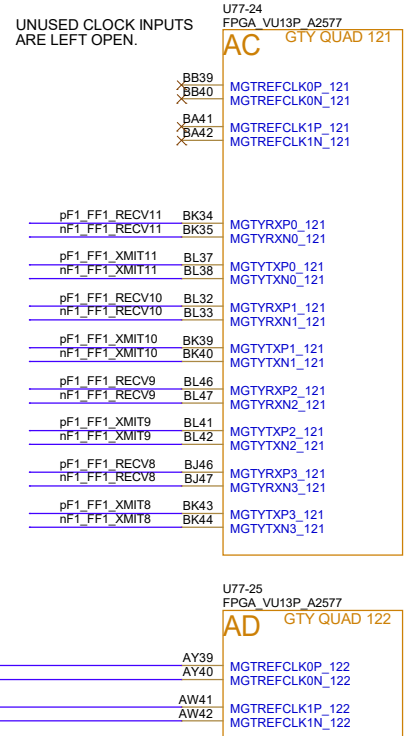
QUAD "L" WIRING FOR FPGA#1 CAN BE FOUND ON SHEET 2.13: C2C AND TCDS QUADS



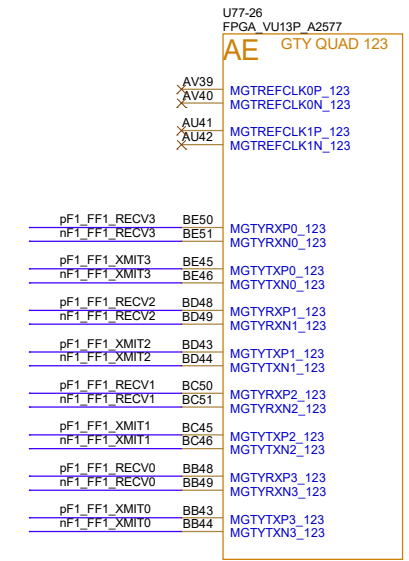
7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE



THE "Vaxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

RCV PORT ADDRESSING  
0x54 = 7 BIT ADDRESS  
0xA8 = 8 BIT WRITE ADDRESS  
0xA9 = 8 BIT READ ADDRESS

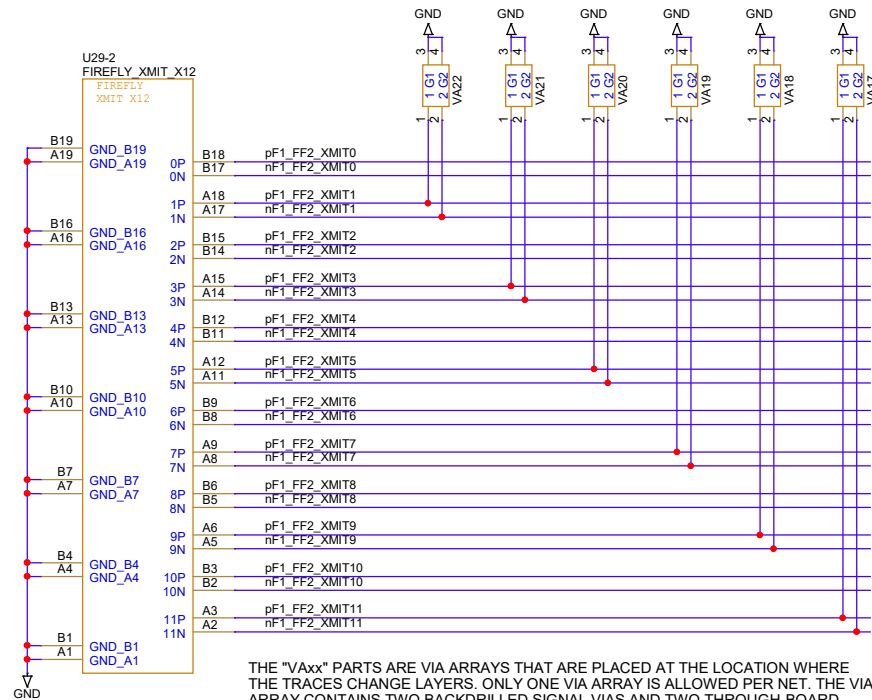
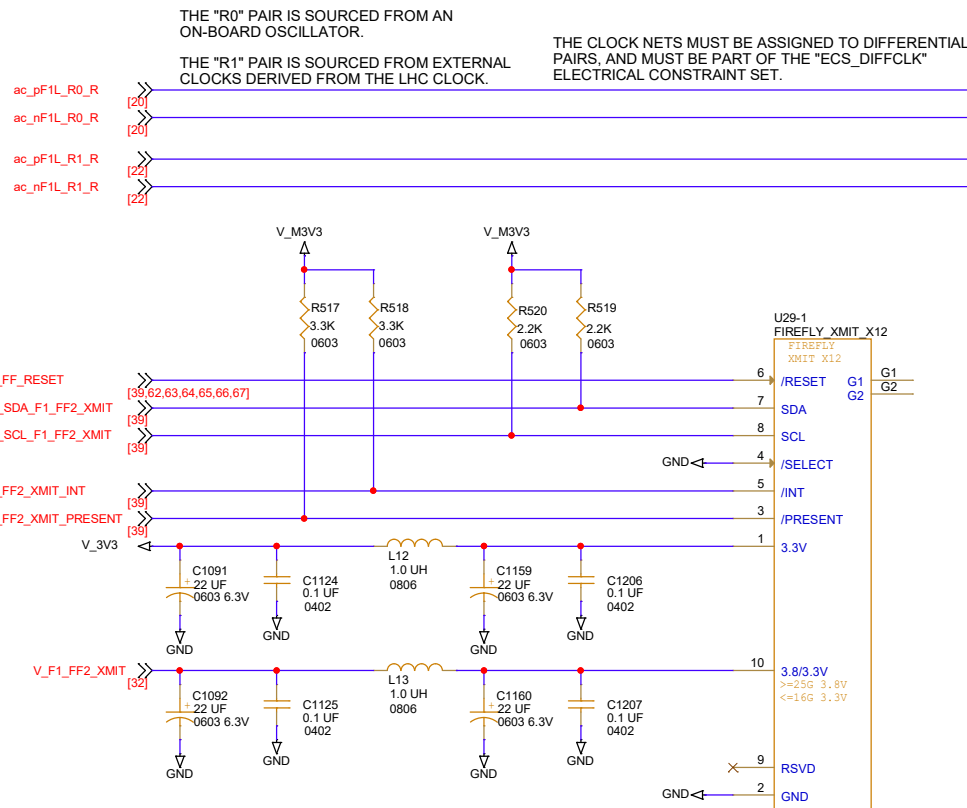
THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

7.03: FPGA#1 FF#2 X12 ON QUADS Q R S



THE "Vaxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

U77-28  
FPGA\_VU13P\_A2577  
Q GTY QUAD 125

AP39	MGTREFCLK0P_125
AP40	MGTREFCLK0N_125
AN41	MGTREFCLK1P_125
AN42	MGTREFCLK1N_125

pF1_FF2_RECV11	AU50	MGTYRXPO_125
nF1_FF2_RECV11	AU51	MGTYRXNO_125
pF1_FF2_XMIT11	AU45	MGTYTXPO_125
nF1_FF2_XMIT11	AU46	MGTYTXNO_125
pF1_FF2_RECV10	AT48	MGTYRXPI_125
nF1_FF2_RECV10	AT49	MGTYRXNI_125
pF1_FF2_XMIT10	AT43	MGTYTXPI_125
nF1_FF2_XMIT10	AT44	MGTYTXNI_125
pF1_FF2_RECV9	AR50	MGTYRXP2_125
nF1_FF2_RECV9	AR51	MGTYRXN2_125
pF1_FF2_XMIT9	AR45	MGTYTXP2_125
nF1_FF2_XMIT9	AR46	MGTYTXN2_125
pF1_FF2_RECV8	AP48	MGTYRXP3_125
nF1_FF2_RECV8	AP49	MGTYRXN3_125
pF1_FF2_XMIT8	AP43	MGTYTXP3_125
nF1_FF2_XMIT8	AP44	MGTYTXN3_125

U77-29  
FPGA\_VU13P\_A2577  
R GTY QUAD 126

AM39	MGTREFCLK0P_126
AM40	MGTREFCLK0N_126
AL41	MGTREFCLK1P_126
AL42	MGTREFCLK1N_126

pF1_FF2_RECV7	AN50	MGTYRXPO_126
nF1_FF2_RECV7	AN51	MGTYRXNO_126
pF1_FF2_XMIT7	AN45	MGTYTXPO_126
nF1_FF2_XMIT7	AN46	MGTYTXNO_126
pF1_FF2_RECV6	AM48	MGTYRXPI_126
nF1_FF2_RECV6	AM49	MGTYRXNI_126
pF1_FF2_XMIT6	AM43	MGTYTXPI_126
nF1_FF2_XMIT6	AM44	MGTYTXNI_126
pF1_FF2_RECV5	AL50	MGTYRXP2_126
nF1_FF2_RECV5	AL51	MGTYRXN2_126
pF1_FF2_XMIT5	AL45	MGTYTXP2_126
nF1_FF2_XMIT5	AL46	MGTYTXN2_126
pF1_FF2_RECV4	AK48	MGTYRXP3_126
nF1_FF2_RECV4	AK49	MGTYRXN3_126
pF1_FF2_XMIT4	AK43	MGTYTXP3_126
nF1_FF2_XMIT4	AK44	MGTYTXN3_126

U77-30  
FPGA\_VU13P\_A2577  
S GTY QUAD 127

AJ41	MGTREFCLK0P_127
AJ42	MGTREFCLK0N_127
AG41	MGTREFCLK1P_127
AG42	MGTREFCLK1N_127

pF1_FF2_RECV3	AJ50	MGTYRXPO_127
nF1_FF2_RECV3	AJ51	MGTYRXNO_127
pF1_FF2_XMIT3	AJ45	MGTYTXPO_127
nF1_FF2_XMIT3	AJ46	MGTYTXNO_127
pF1_FF2_RECV2	AH48	MGTYRXPI_127
nF1_FF2_RECV2	AH49	MGTYRXNI_127
pF1_FF2_XMIT2	AH43	MGTYTXPI_127
nF1_FF2_XMIT2	AH44	MGTYTXNI_127
pF1_FF2_RECV1	AG50	MGTYRXP2_127
nF1_FF2_RECV1	AG51	MGTYRXN2_127
pF1_FF2_XMIT1	AG45	MGTYTXP2_127
nF1_FF2_XMIT1	AG46	MGTYTXN2_127
pF1_FF2_RECV0	AF48	MGTYRXP3_127
nF1_FF2_RECV0	AF49	MGTYRXN3_127
pF1_FF2_XMIT0	AF43	MGTYTXP3_127
nF1_FF2_XMIT0	AF44	MGTYTXN3_127

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

RCV PORT ADDRESSING  
0x54 = 7 BIT ADDRESS  
0xA8 = 8 BIT WRITE ADDRESS  
0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

# 7.04: FPGA#1 FF#3 X12 ON QUADS T U V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

U77-31  
FPGA\_VU13P\_A2577

GTU QUAD 128

AE41  
AE42  
AC41  
AC42  
MGTYRXP0\_128  
MGTYRXN0\_128  
MGTYRXP1\_128  
MGTYRXN1\_128

pF1\_FF3\_RECV11 AE50  
nF1\_FF3\_RECV11 AE51  
MGTYRXP0\_128  
MGTYRXN0\_128  
pF1\_FF3\_XMIT11 AE45  
nF1\_FF3\_XMIT11 AE46  
MGTYTXP0\_128  
MGTYTXN0\_128  
pF1\_FF3\_RECV10 AD48  
nF1\_FF3\_RECV10 AD49  
MGTYRXP1\_128  
MGTYRXN1\_128  
pF1\_FF3\_XMIT10 AD43  
nF1\_FF3\_XMIT10 AD44  
MGTYTXP1\_128  
MGTYTXN1\_128  
pF1\_FF3\_RECV9 AC50  
nF1\_FF3\_RECV9 AC51  
MGTYRXP2\_128  
MGTYRXN2\_128  
pF1\_FF3\_XMIT9 AC45  
nF1\_FF3\_XMIT9 AC46  
MGTYTXP2\_128  
MGTYTXN2\_128  
pF1\_FF3\_RECV8 AB48  
nF1\_FF3\_RECV8 AB49  
MGTYRXP3\_128  
MGTYRXN3\_128  
pF1\_FF3\_XMIT8 AB43  
nF1\_FF3\_XMIT8 AB44  
MGTYTXP3\_128  
MGTYTXN3\_128

U77-32  
FPGA\_VU13P\_A2577

GTU QUAD 129

AA41  
AA42  
Y39  
Y40  
MGTYRXP0\_129  
MGTYRXN0\_129  
MGTYRXP1\_129  
MGTYRXN1\_129

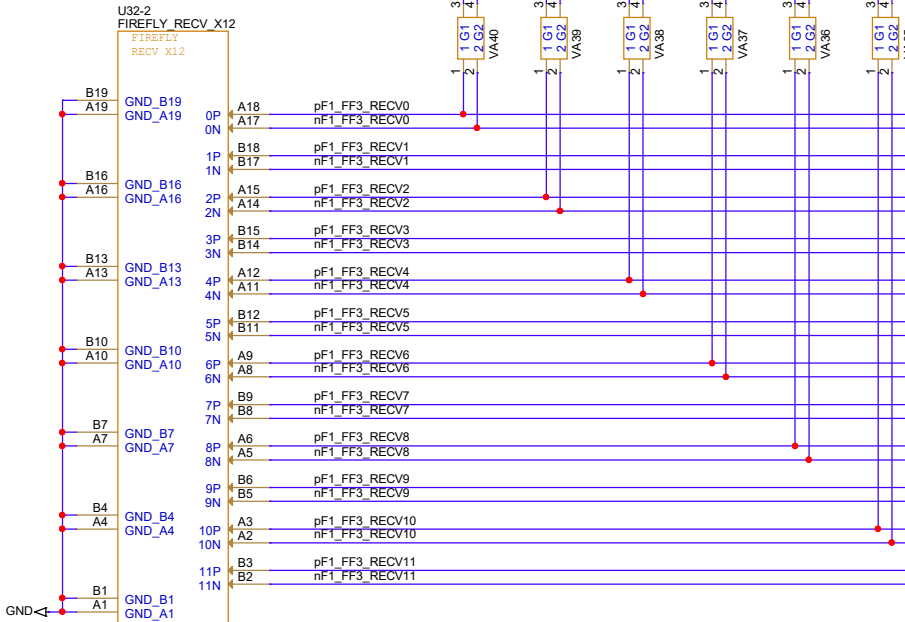
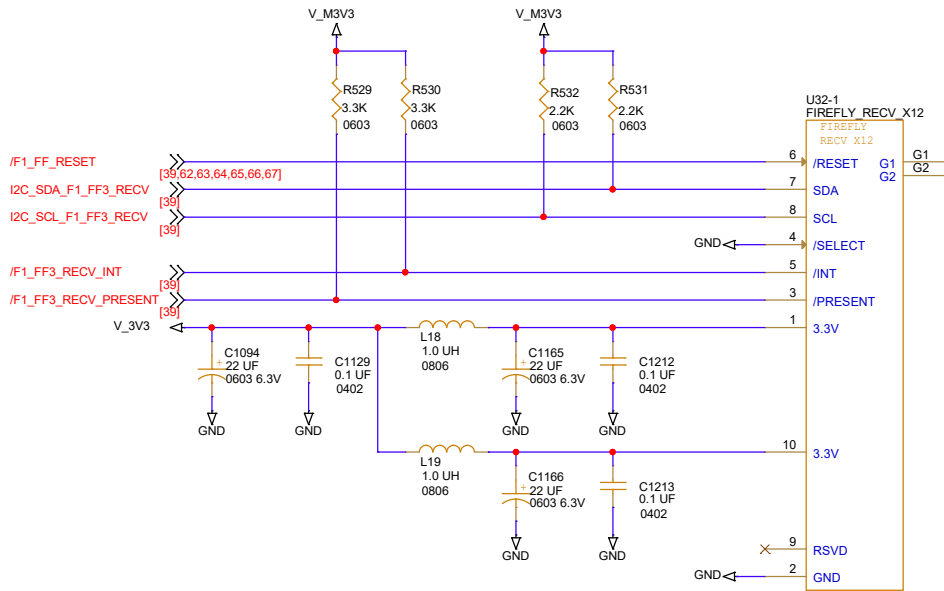
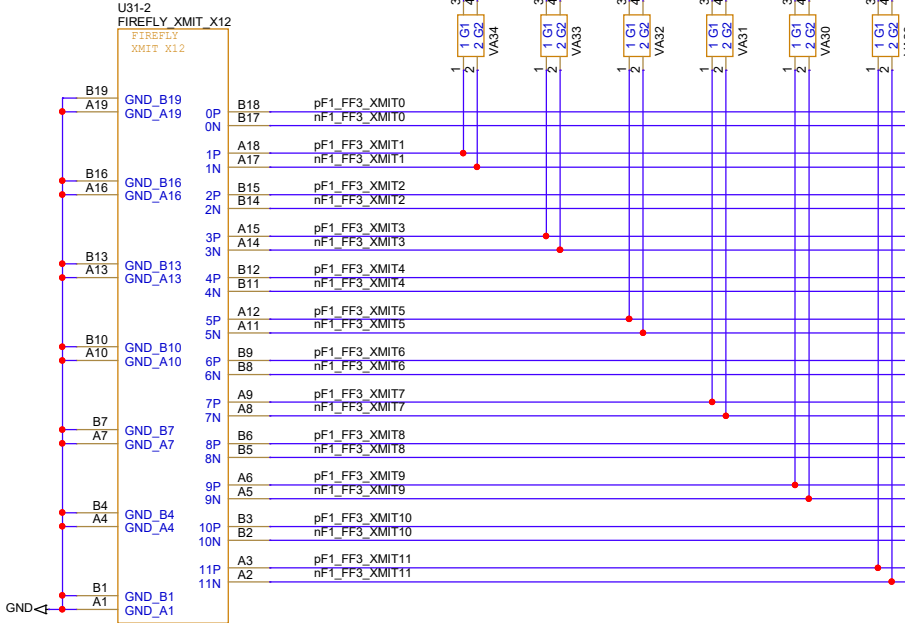
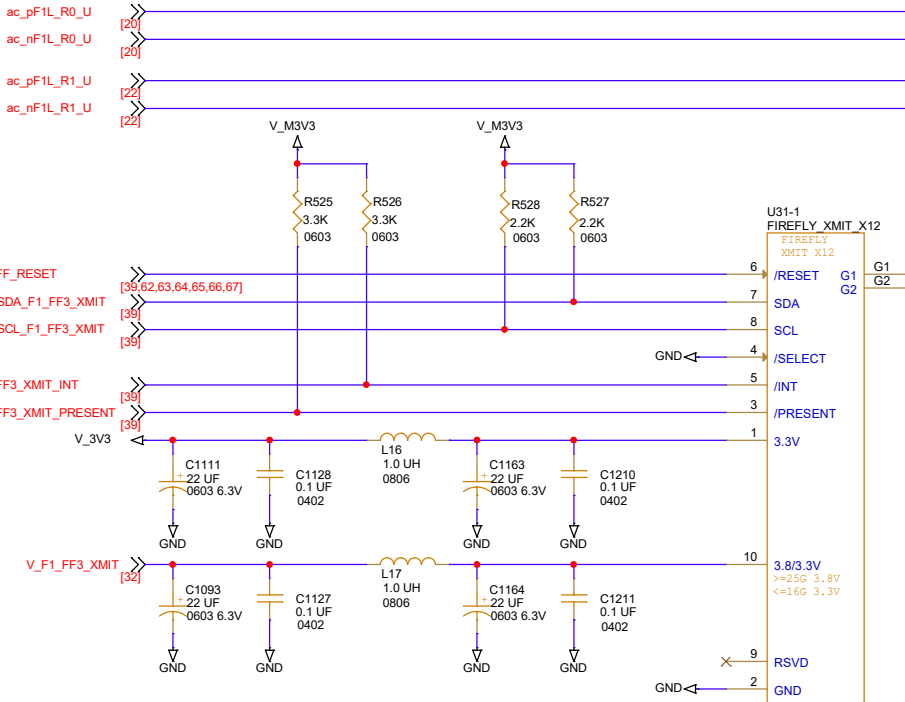
pF1\_FF3\_RECV7 AA50  
nF1\_FF3\_RECV7 AA51  
MGTYRXP0\_129  
MGTYRXN0\_129  
pF1\_FF3\_XMIT7 AA45  
nF1\_FF3\_XMIT7 AA46  
MGTYTXP0\_129  
MGTYTXN0\_129  
pF1\_FF3\_RECV6 Y48  
nF1\_FF3\_RECV6 Y49  
MGTYRXP1\_129  
MGTYRXN1\_129  
pF1\_FF3\_XMIT6 Y43  
nF1\_FF3\_XMIT6 Y44  
MGTYTXP1\_129  
MGTYTXN1\_129  
pF1\_FF3\_RECV5 W50  
nF1\_FF3\_RECV5 W51  
MGTYRXP2\_129  
MGTYRXN2\_129  
pF1\_FF3\_XMIT5 W45  
nF1\_FF3\_XMIT5 W46  
MGTYTXP2\_129  
MGTYTXN2\_129  
pF1\_FF3\_RECV4 V48  
nF1\_FF3\_RECV4 V49  
MGTYRXP3\_129  
MGTYRXN3\_129  
pF1\_FF3\_XMIT4 V43  
nF1\_FF3\_XMIT4 V44  
MGTYTXP3\_129  
MGTYTXN3\_129

U77-33  
FPGA\_VU13P\_A2577

GTU QUAD 130

W41  
W42  
V39  
V40  
MGTYRXP0\_130  
MGTYRXN0\_130  
MGTYRXP1\_130  
MGTYRXN1\_130

pF1\_FF3\_RECV3 U50  
nF1\_FF3\_RECV3 U51  
MGTYRXP0\_130  
MGTYRXN0\_130  
pF1\_FF3\_XMIT3 U45  
nF1\_FF3\_XMIT3 U46  
MGTYTXP0\_130  
MGTYTXN0\_130  
pF1\_FF3\_RECV2 T48  
nF1\_FF3\_RECV2 T49  
MGTYRXP1\_130  
MGTYRXN1\_130  
pF1\_FF3\_XMIT2 T43  
nF1\_FF3\_XMIT2 T44  
MGTYTXP1\_130  
MGTYTXN1\_130  
pF1\_FF3\_RECV1 R50  
nF1\_FF3\_RECV1 R51  
MGTYRXP2\_130  
MGTYRXN2\_130  
pF1\_FF3\_XMIT1 R45  
nF1\_FF3\_XMIT1 R46  
MGTYTXP2\_130  
MGTYTXN2\_130  
pF1\_FF3\_RECV0 P48  
nF1\_FF3\_RECV0 P49  
MGTYRXP3\_130  
MGTYRXN3\_130  
pF1\_FF3\_XMIT0 P43  
nF1\_FF3\_XMIT0 P44  
MGTYTXP3\_130  
MGTYTXN3\_130



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "Vaxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM v3

Title			
7.04: FPGA#1 FF#3 X12 ON QUADS T U V			
Size	Document Number		Re
	6089-127		
Date:	Thursday, January 23, 2025	Sheet	64 of 82

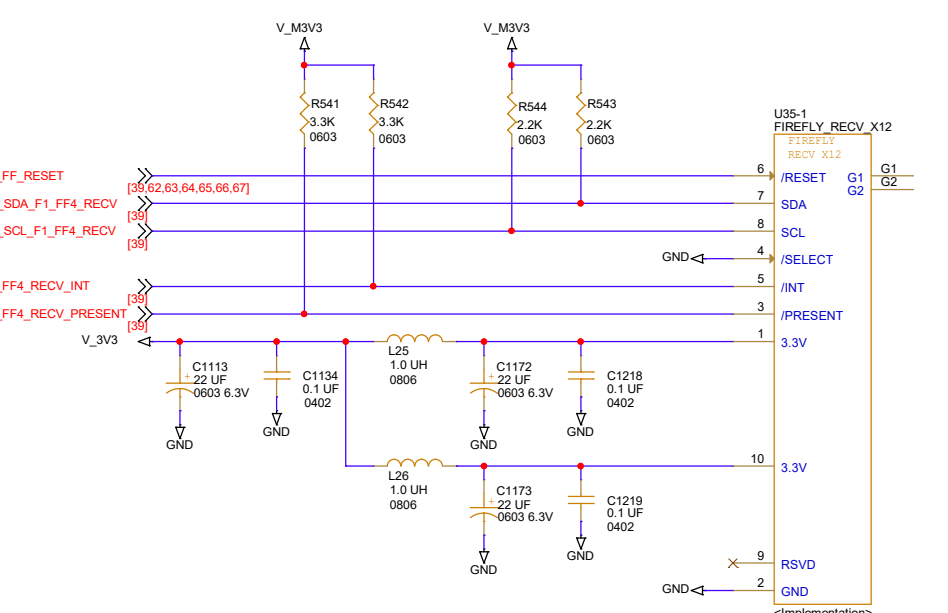
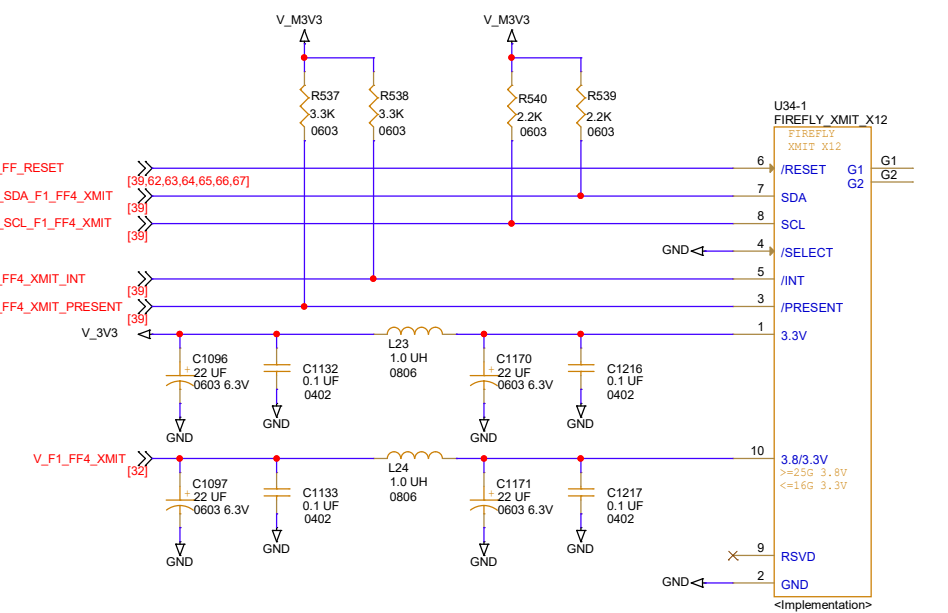


7.05: FPGA#1 FF#4 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

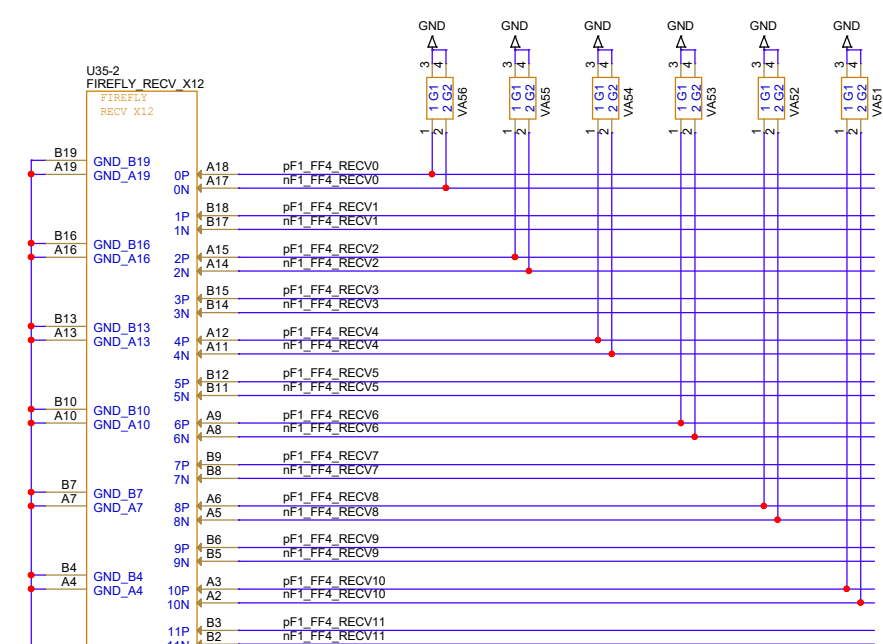
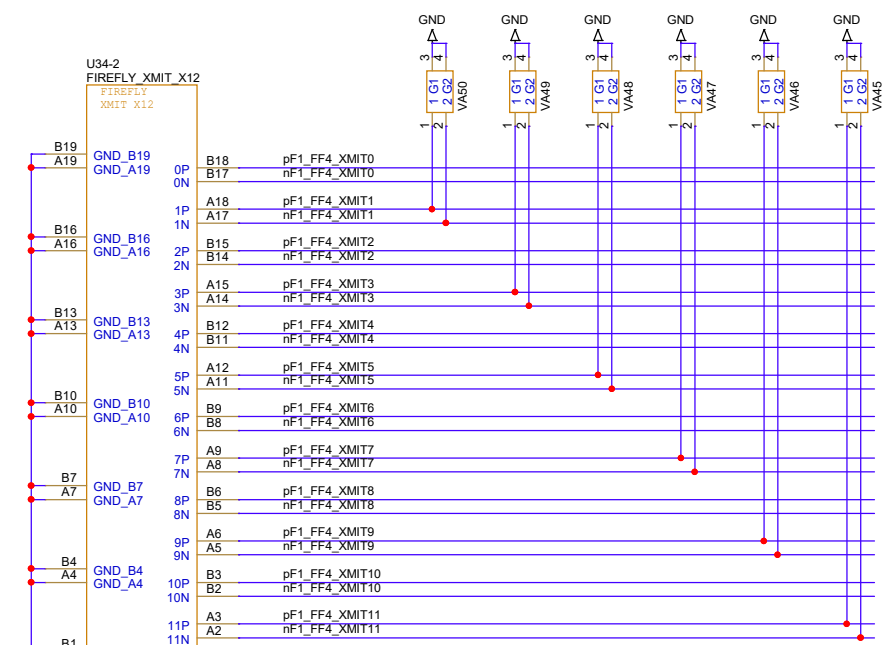
XMIT PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING  
0x54 = 7 BIT ADDRESS  
0xA8 = 8 BIT WRITE ADDRESS  
0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

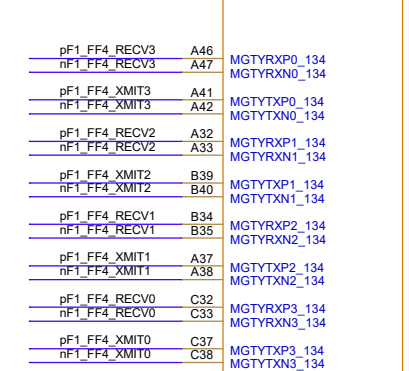
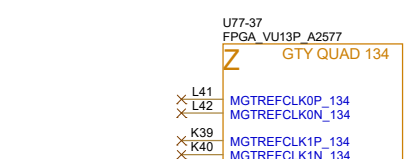
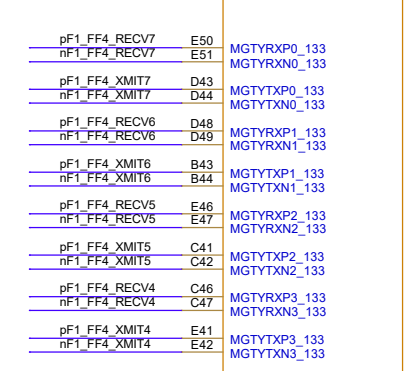
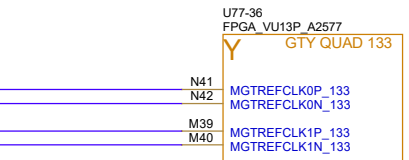
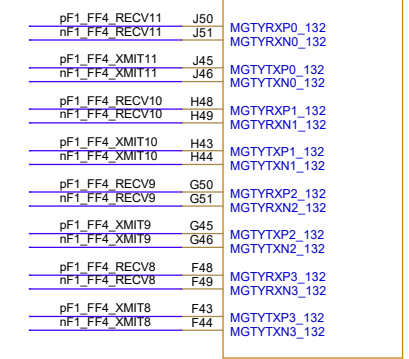


THE "Vaxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

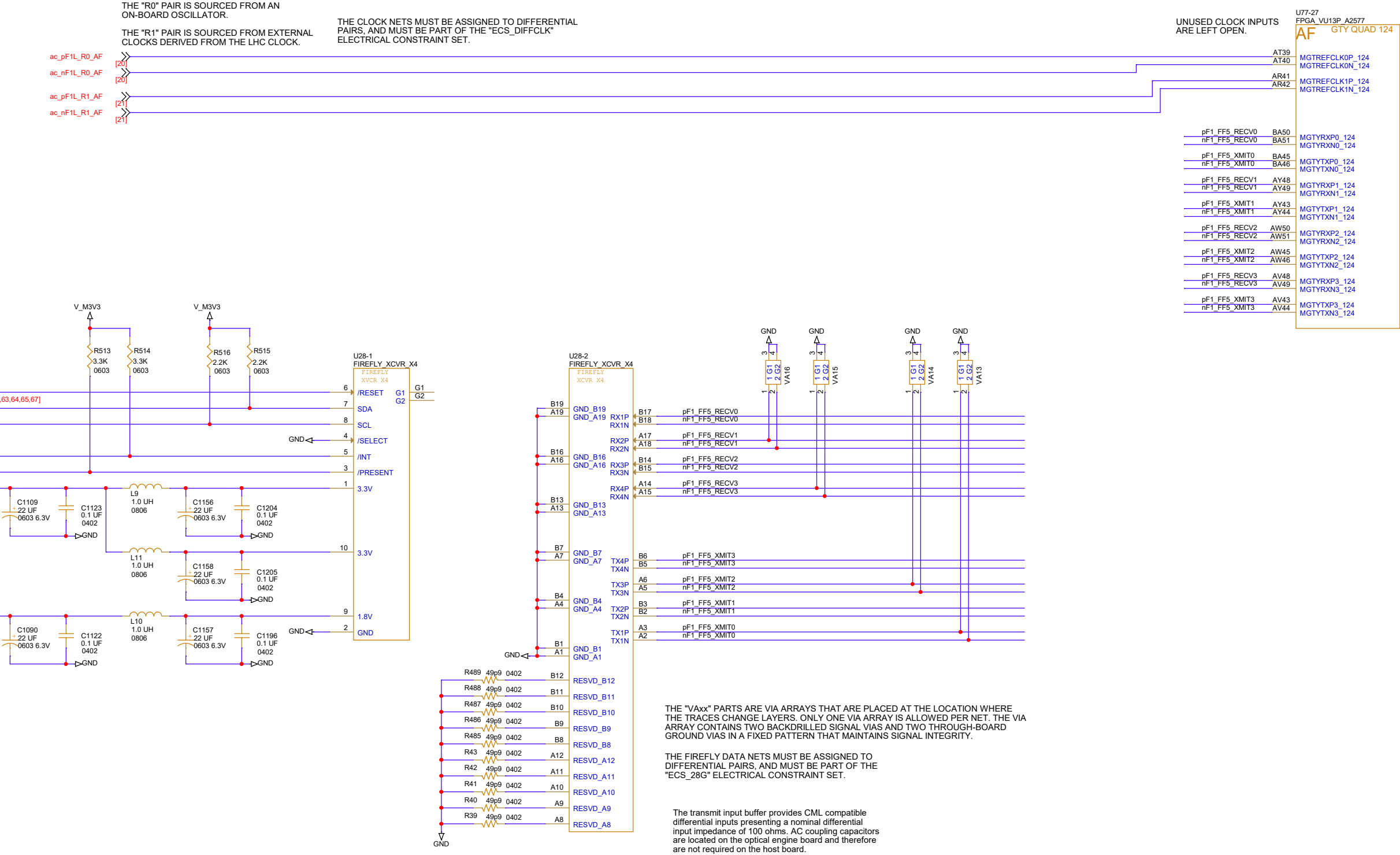
THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



7.06: FPGA#1 FF#5 X4 ON QUAD AF



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

7.07: FPGA#1 FF#6 X4 ON QUAD W

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

ac\_pF1L\_R0\_W [20]

ac\_nF1L\_R0\_W [20]

ac\_pF1L\_R1\_W [21]

ac\_nF1L\_R1\_W [21]

U77-34  
FPGA\_VU13P\_A2577  
W GTY QUAD 131

U41 MGTREFCLK0P\_131

U42 MGTREFCLK0N\_131

T39 MGTREFCLK1P\_131

T40 MGTREFCLK1N\_131

pF1\_FF6\_RECV0 N50 MGTYRX0\_131

nF1\_FF6\_RECV0 N51 MGTYRXN0\_131

pF1\_FF6\_XMIT0 N45 MGTYTXP0\_131

nF1\_FF6\_XMIT0 N46 MGTYTXN0\_131

pF1\_FF6\_RECV1 M48 MGTYRX1\_131

nF1\_FF6\_RECV1 M49 MGTYRXN1\_131

pF1\_FF6\_XMIT1 M43 MGTYTXP1\_131

nF1\_FF6\_XMIT1 M44 MGTYTXN1\_131

pF1\_FF6\_RECV2 L50 MGTYRX2\_131

nF1\_FF6\_RECV2 L51 MGTYRXN2\_131

pF1\_FF6\_XMIT2 L45 MGTYTXP2\_131

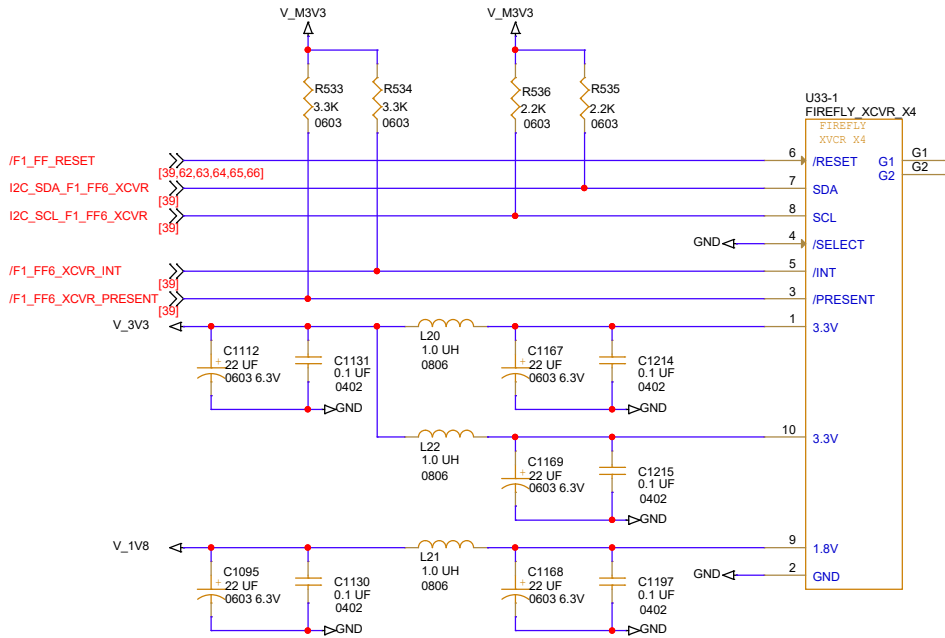
nF1\_FF6\_XMIT2 L46 MGTYTXN2\_131

pF1\_FF6\_RECV3 K48 MGTYRX3\_131

nF1\_FF6\_RECV3 K49 MGTYRXN3\_131

pF1\_FF6\_XMIT3 K43 MGTYTXP3\_131

nF1\_FF6\_XMIT3 K44 MGTYTXN3\_131



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING

0x50 = 7 BIT ADDRESS

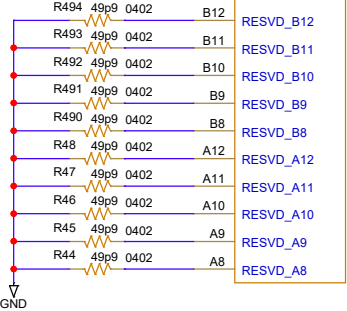
0xA0 = 8 BIT WRITE ADDRESS

0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.



HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:

If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.

Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAXX" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM v3

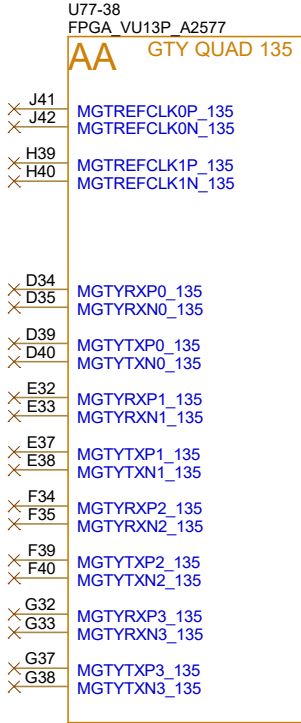
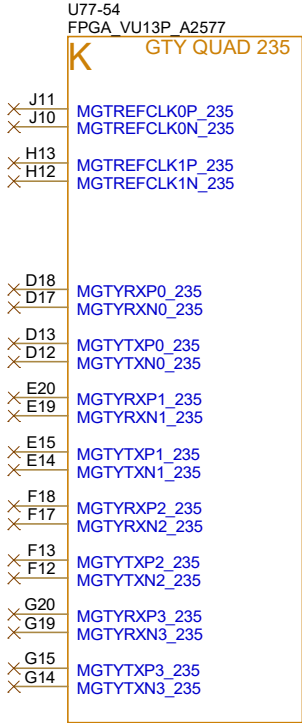
Title 7.07: FPGA#1 FF#6 X4 ON QUAD W

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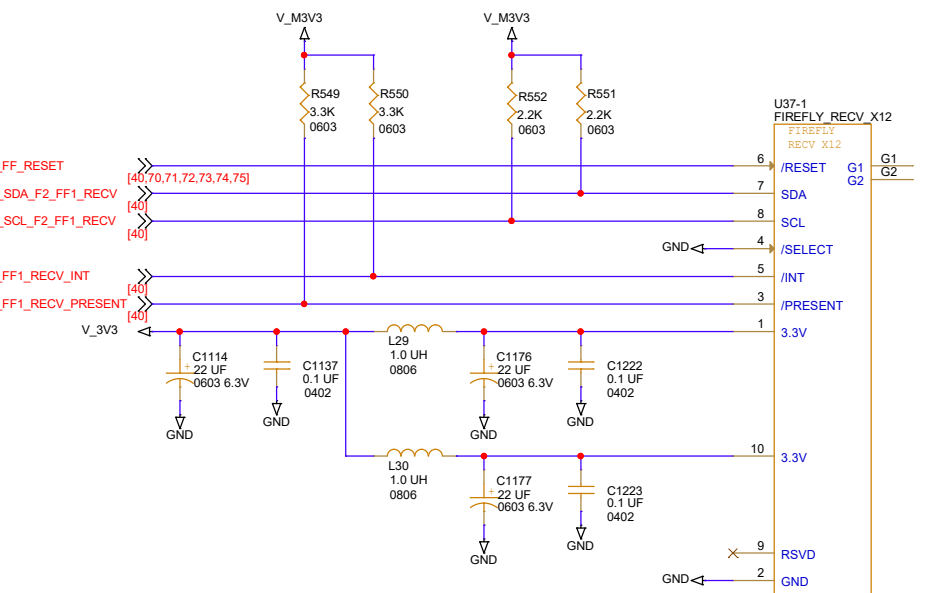
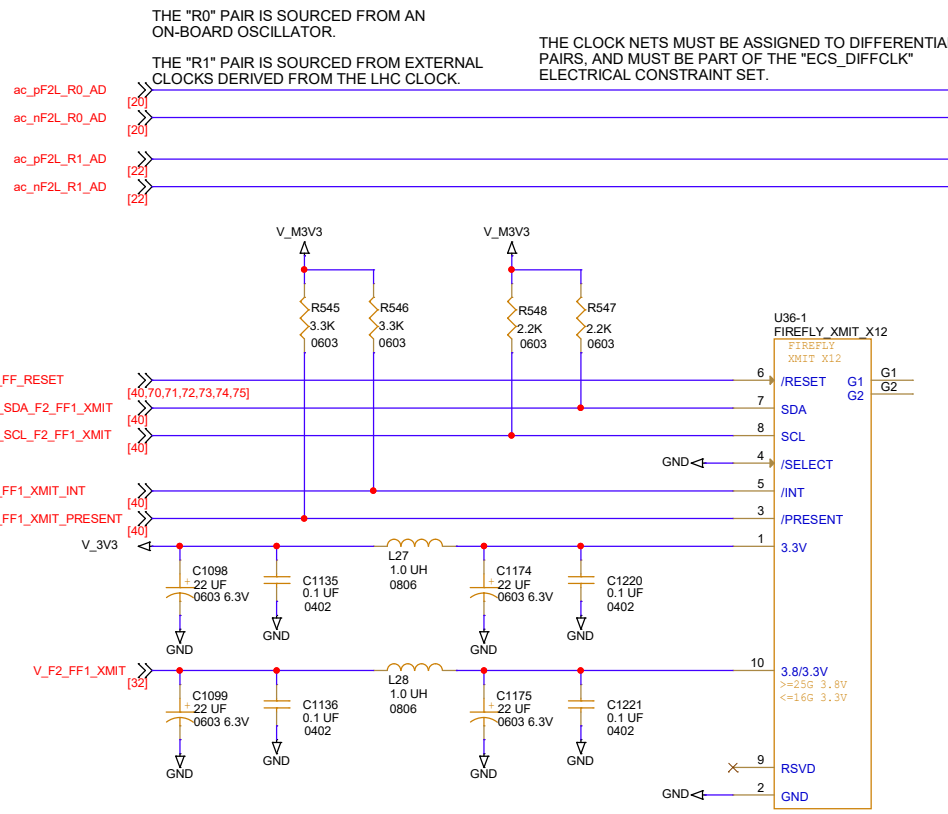




QUAD "L" WIRING FOR FPGA#2 CAN BE FOUND ON SHEET 2.13: C2C AND TCDS QUADS

APOLLO CM v3		
Title		
8.01: FPGA#2 SM C2C ON QUAD L		
Size	Document Number	Rev
	6089-127	A
Date:	Thursday, January 23, 2025	Sheet 69 of 82

8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

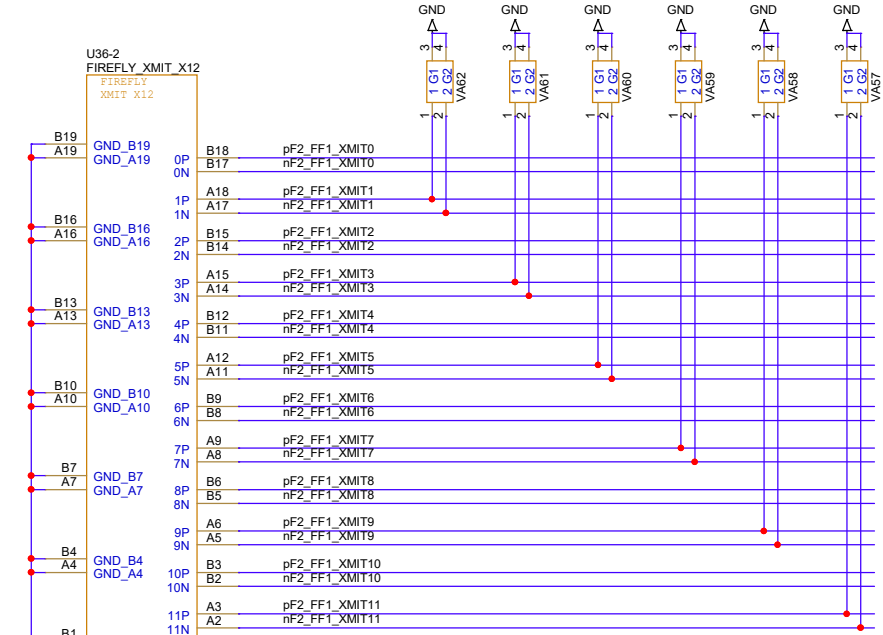
XMIT PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING  
0x54 = 7 BIT ADDRESS  
0xA8 = 8 BIT WRITE ADDRESS  
0xA9 = 8 BIT READ ADDRESS

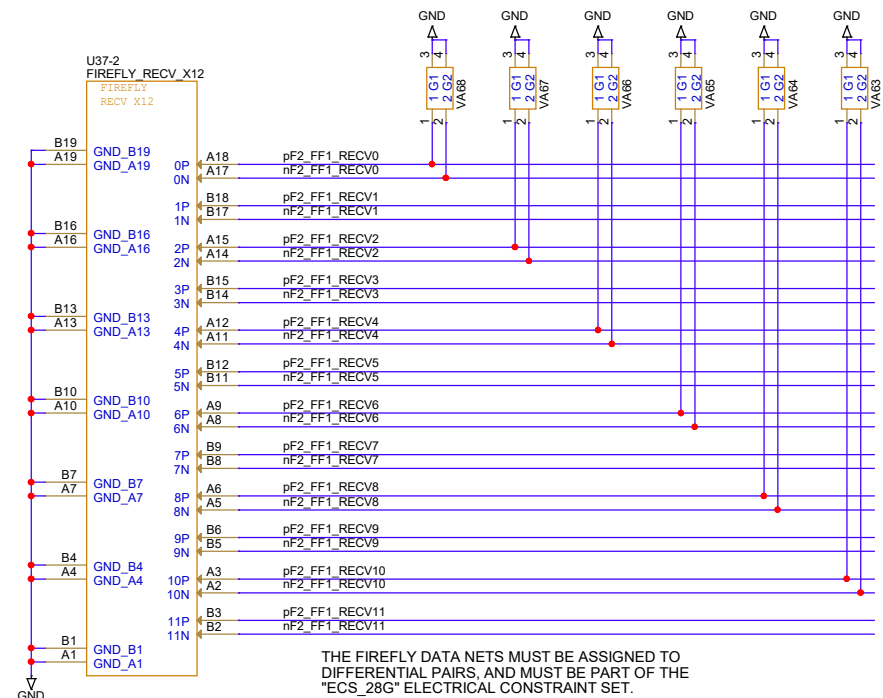
THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.



THE "Vaxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

U78-24  
FPGA\_VU13P\_A2577  
AC GTY QUAD 121

BB39	MGTYRX0P_121
BB40	MGTYRXN0_121
BA41	MGTYRX0P_121
BA42	MGTYRXN0_121

pF2_FF1_RECV11	BK34	MGTYRX0P_121
nF2_FF1_RECV11	BK35	MGTYRXN0_121
pF2_FF1_XMIT11	BL37	MGTYTX0P_121
nF2_FF1_XMIT11	BL38	MGTYTXN0_121
pF2_FF1_RECV10	BL32	MGTYRX0P_121
nF2_FF1_RECV10	BL33	MGTYRXN0_121
pF2_FF1_XMIT10	BK39	MGTYTX0P_121
nF2_FF1_XMIT10	BK40	MGTYTXN0_121
pF2_FF1_RECV9	BL46	MGTYRX0P_121
nF2_FF1_RECV9	BL47	MGTYRXN0_121
pF2_FF1_XMIT9	BL41	MGTYTX0P_121
nF2_FF1_XMIT9	BL42	MGTYTXN0_121
pF2_FF1_RECV8	BJ46	MGTYRX0P_121
nF2_FF1_RECV8	BJ47	MGTYRXN0_121
pF2_FF1_XMIT8	BK43	MGTYTX0P_121
nF2_FF1_XMIT8	BK44	MGTYTXN0_121

U78-25  
FPGA\_VU13P\_A2577  
AD GTY QUAD 122

AY39	MGTYRX0P_122
AY40	MGTYRXN0_122
AW41	MGTYRX0P_122
AW42	MGTYRXN0_122

pF2_FF1_RECV7	BH48	MGTYRX0P_122
nF2_FF1_RECV7	BH49	MGTYRXN0_122
pF2_FF1_XMIT7	BG41	MGTYTX0P_122
nF2_FF1_XMIT7	BG42	MGTYTXN0_122
pF2_FF1_RECV6	BG50	MGTYRX0P_122
nF2_FF1_RECV6	BG51	MGTYRXN0_122
pF2_FF1_XMIT6	BJ41	MGTYTX0P_122
nF2_FF1_XMIT6	BJ42	MGTYTXN0_122
pF2_FF1_RECV5	BG46	MGTYRX0P_122
nF2_FF1_RECV5	BG47	MGTYRXN0_122
pF2_FF1_XMIT5	BH43	MGTYTX0P_122
nF2_FF1_XMIT5	BH44	MGTYTXN0_122
pF2_FF1_RECV4	BF48	MGTYRX0P_122
nF2_FF1_RECV4	BF49	MGTYRXN0_122
pF2_FF1_XMIT4	BF43	MGTYTX0P_122
nF2_FF1_XMIT4	BF44	MGTYTXN0_122

U78-26  
FPGA\_VU13P\_A2577  
AE GTY QUAD 123

AV39	MGTYRX0P_123
AV40	MGTYRXN0_123
AU41	MGTYRX0P_123
AU42	MGTYRXN0_123

pF2_FF1_RECV3	BE50	MGTYRX0P_123
nF2_FF1_RECV3	BE51	MGTYRXN0_123
pF2_FF1_XMIT3	BE45	MGTYTX0P_123
nF2_FF1_XMIT3	BE46	MGTYTXN0_123
pF2_FF1_RECV2	BD48	MGTYRX0P_123
nF2_FF1_RECV2	BD49	MGTYRXN0_123
pF2_FF1_XMIT2	BD43	MGTYTX0P_123
nF2_FF1_XMIT2	BD44	MGTYTXN0_123
pF2_FF1_RECV1	BC50	MGTYRX0P_123
nF2_FF1_RECV1	BC51	MGTYRXN0_123
pF2_FF1_XMIT1	BC45	MGTYTX0P_123
nF2_FF1_XMIT1	BC46	MGTYTXN0_123
pF2_FF1_RECV0	BB48	MGTYRX0P_123
nF2_FF1_RECV0	BB49	MGTYRXN0_123
pF2_FF1_XMIT0	BB43	MGTYTX0P_123
nF2_FF1_XMIT0	BB44	MGTYTXN0_123

8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

U78-28  
FPGA\_VU13P\_A2577  
Q  
GTU QUAD 125

AP39	MGTREFCLK0P_125
AP40	MGTREFCLK0N_125
AN41	MGTREFCLK1P_125
AN42	MGTREFCLK1N_125

pF2_FF2_RECV11	AU50	MGTYRXP0_125
nF2_FF2_RECV11	AU51	MGTYRXN0_125
pF2_FF2_XMIT11	AU45	MGTYTXP0_125
nF2_FF2_XMIT11	AU46	MGTYTXN0_125
pF2_FF2_RECV10	AT48	MGTYRXP1_125
nF2_FF2_RECV10	AT49	MGTYRXN1_125
pF2_FF2_XMIT10	AT43	MGTYTXP1_125
nF2_FF2_XMIT10	AT44	MGTYTXN1_125
pF2_FF2_RECV9	AR50	MGTYRXP2_125
nF2_FF2_RECV9	AR51	MGTYRXN2_125
pF2_FF2_XMIT9	AR45	MGTYTXP2_125
nF2_FF2_XMIT9	AR46	MGTYTXN2_125
pF2_FF2_RECV8	AP48	MGTYRXP3_125
nF2_FF2_RECV8	AP49	MGTYRXN3_125
pF2_FF2_XMIT8	AP43	MGTYTXP3_125
nF2_FF2_XMIT8	AP44	MGTYTXN3_125

U78-29  
FPGA\_VU13P\_A2577  
R  
GTU QUAD 126

AM39	MGTREFCLK0P_126
AM40	MGTREFCLK0N_126
AL41	MGTREFCLK1P_126
AL42	MGTREFCLK1N_126

pF2_FF2_RECV7	AN50	MGTYRXP0_126
nF2_FF2_RECV7	AN51	MGTYRXN0_126
pF2_FF2_XMIT7	AN45	MGTYTXP0_126
nF2_FF2_XMIT7	AN46	MGTYTXN0_126
pF2_FF2_RECV6	AM48	MGTYRXP1_126
nF2_FF2_RECV6	AM49	MGTYRXN1_126
pF2_FF2_XMIT6	AM43	MGTYTXP1_126
nF2_FF2_XMIT6	AM44	MGTYTXN1_126
pF2_FF2_RECV5	AL50	MGTYRXP2_126
nF2_FF2_RECV5	AL51	MGTYRXN2_126
pF2_FF2_XMIT5	AL45	MGTYTXP2_126
nF2_FF2_XMIT5	AL46	MGTYTXN2_126
pF2_FF2_RECV4	AK48	MGTYRXP3_126
nF2_FF2_RECV4	AK49	MGTYRXN3_126
pF2_FF2_XMIT4	AK43	MGTYTXP3_126
nF2_FF2_XMIT4	AK44	MGTYTXN3_126

U78-30  
FPGA\_VU13P\_A2577  
S  
GTU QUAD 127

AJ41	MGTREFCLK0P_127
AJ42	MGTREFCLK0N_127
AG41	MGTREFCLK1P_127
AG42	MGTREFCLK1N_127

pF2_FF2_RECV3	AJ50	MGTYRXP0_127
nF2_FF2_RECV3	AJ51	MGTYRXN0_127
pF2_FF2_XMIT3	AJ45	MGTYTXP0_127
nF2_FF2_XMIT3	AJ46	MGTYTXN0_127
pF2_FF2_RECV2	AH48	MGTYRXP1_127
nF2_FF2_RECV2	AH49	MGTYRXN1_127
pF2_FF2_XMIT2	AH43	MGTYTXP1_127
nF2_FF2_XMIT2	AH44	MGTYTXN1_127
pF2_FF2_RECV1	AG50	MGTYRXP2_127
nF2_FF2_RECV1	AG51	MGTYRXN2_127
pF2_FF2_XMIT1	AG45	MGTYTXP2_127
nF2_FF2_XMIT1	AG46	MGTYTXN2_127
pF2_FF2_RECV0	AF48	MGTYRXP3_127
nF2_FF2_RECV0	AF49	MGTYRXN3_127
pF2_FF2_XMIT0	AF43	MGTYTXP3_127
nF2_FF2_XMIT0	AF44	MGTYTXN3_127

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING  
0x54 = 7 BIT ADDRESS  
0xA8 = 8 BIT WRITE ADDRESS  
0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "Vaxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

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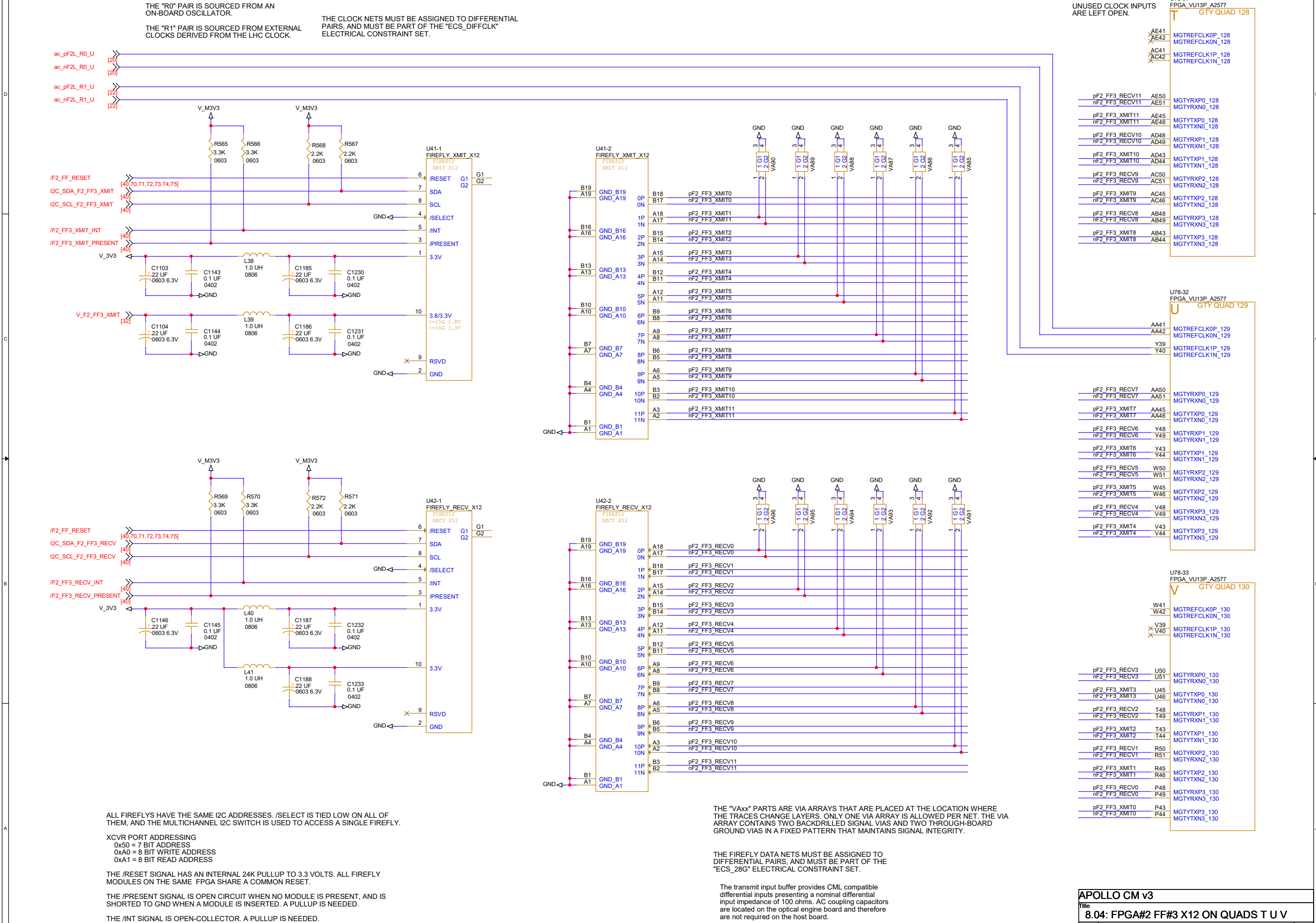
Title  
8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

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#### 8.04: FPGA#2 FF#3 X12 ON QUADS T U V



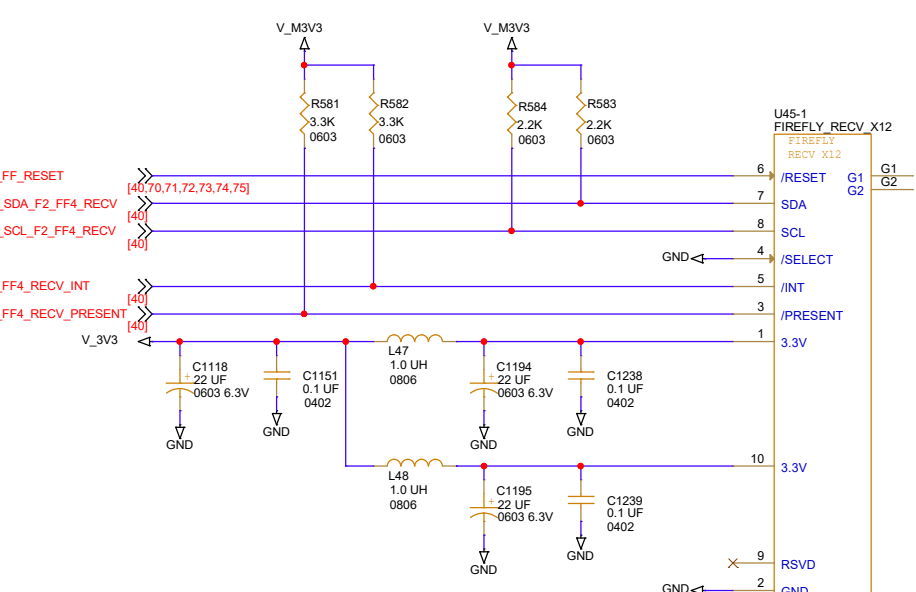
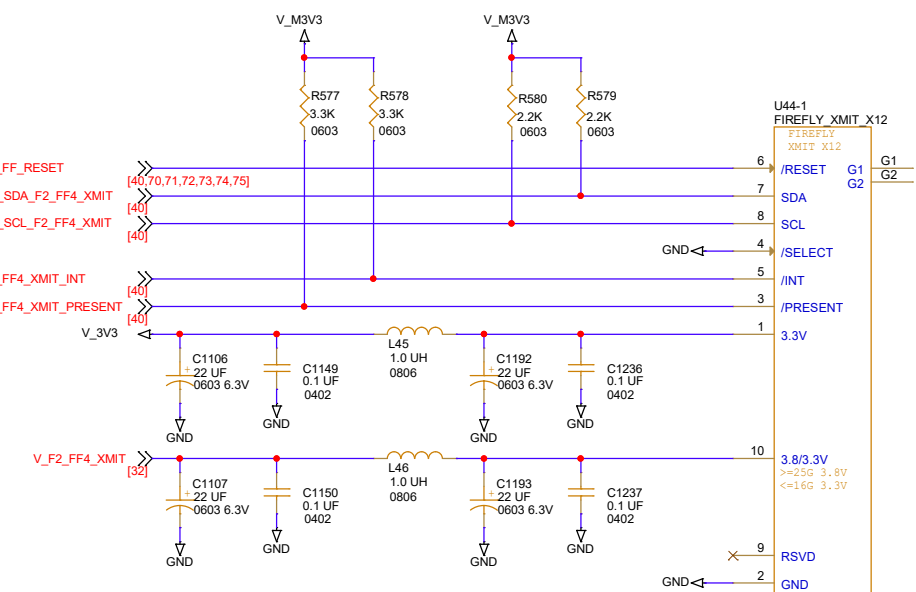


8.05: FPGA#2 FF#4 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

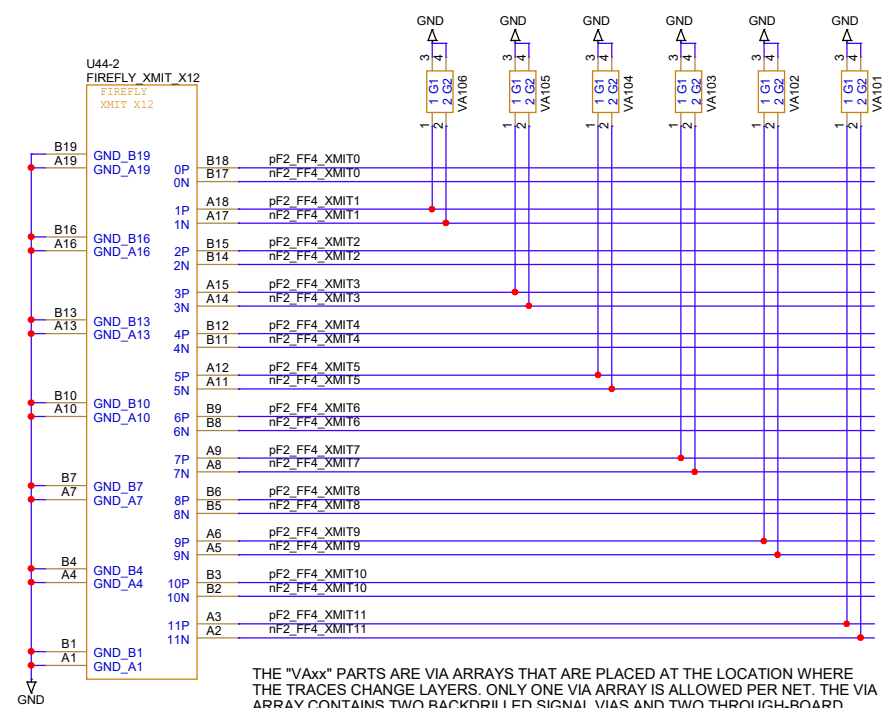
XMIT PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING  
0x54 = 7 BIT ADDRESS  
0xA8 = 8 BIT WRITE ADDRESS  
0xA9 = 8 BIT READ ADDRESS

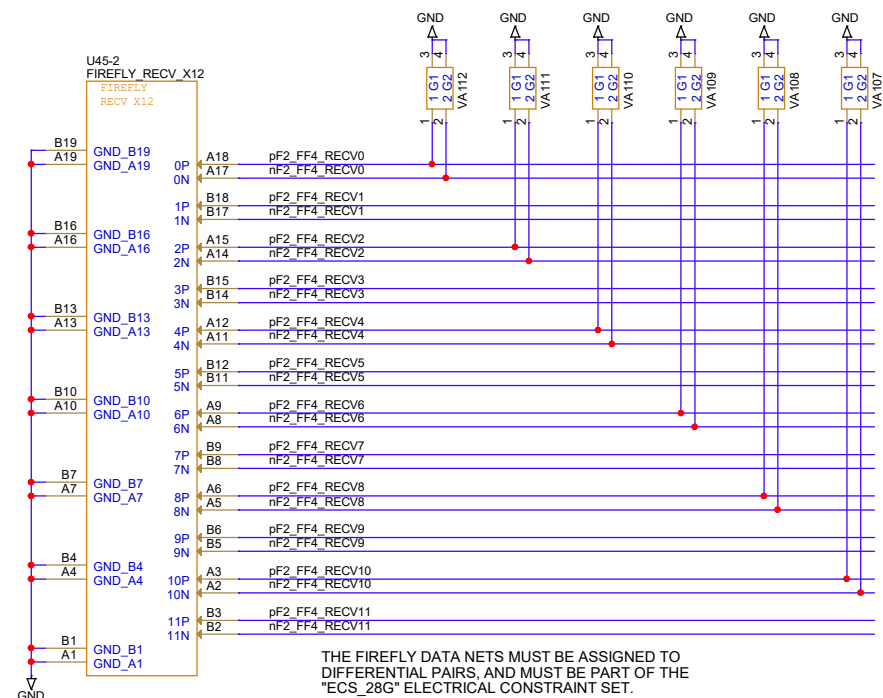
THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.



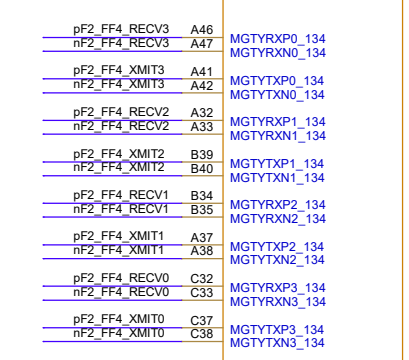
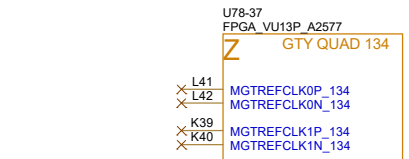
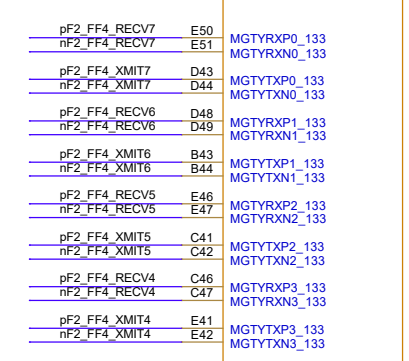
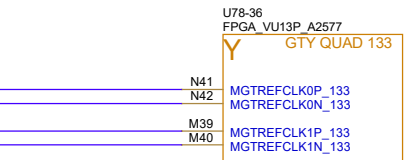
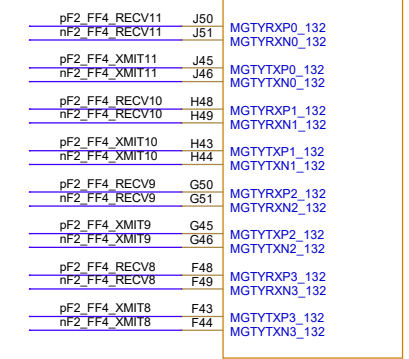
THE "Vaxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



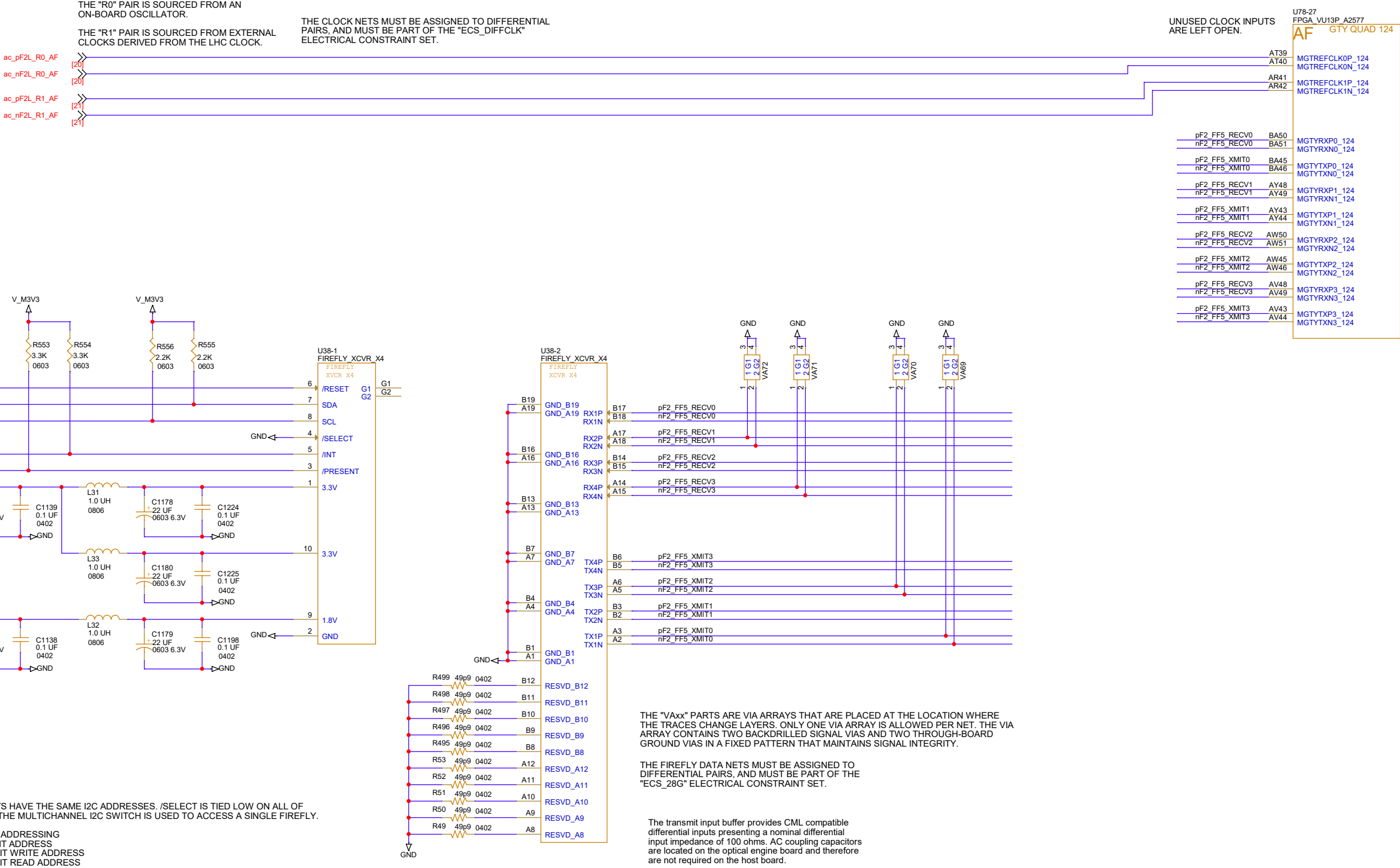
THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



8.06: FPGA#2 FF#5 X4 ON QUAD AF



APOLLO CM v3

Title  
8.06: FPGA#2 FF#5 X4 ON QUAD AF

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THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

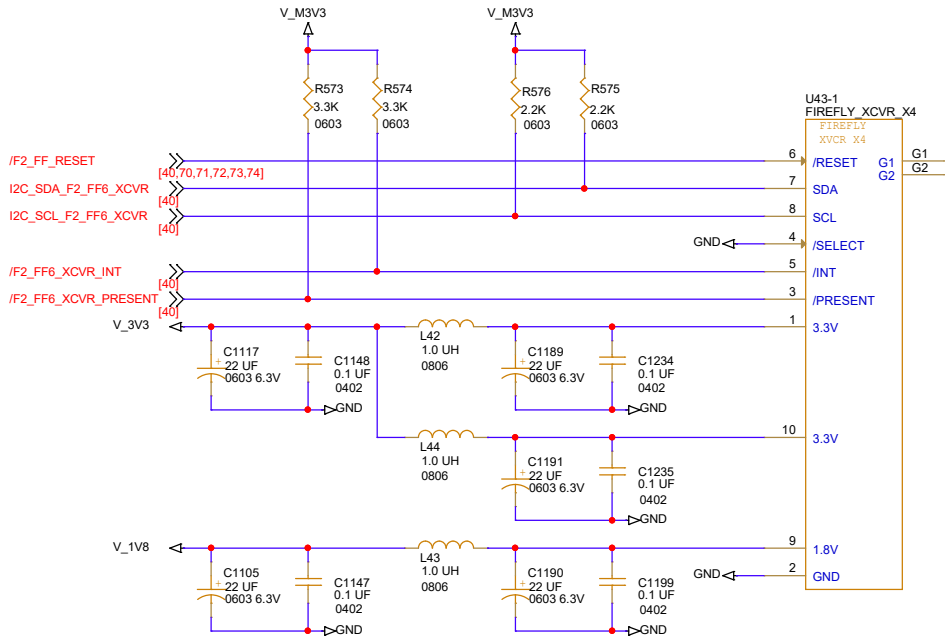
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

ac\_pF2L\_R0\_W [20]  
ac\_nF2L\_R0\_W [20]  
ac\_pF2L\_R1\_W [21]  
ac\_nF2L\_R1\_W [21]

U78-34  
FPGA\_VU13P\_A2577  
W GTY QUAD 131

U41 MGTREFCLK0P\_131  
U42 MGTREFCLK0N\_131  
T39 MGTREFCLK1P\_131  
T40 MGTREFCLK1N\_131

pF2\_FF6\_RECV0 N50 MGTYRX0\_131  
nF2\_FF6\_RECV0 N51 MGTYRXN0\_131  
pF2\_FF6\_XMIT0 N45 MGTYTXP0\_131  
nF2\_FF6\_XMIT0 N46 MGTYTXN0\_131  
pF2\_FF6\_RECV1 M48 MGTYRX1\_131  
nF2\_FF6\_RECV1 M49 MGTYRXN1\_131  
pF2\_FF6\_XMIT1 M43 MGTYTXP1\_131  
nF2\_FF6\_XMIT1 M44 MGTYTXN1\_131  
pF2\_FF6\_RECV2 L50 MGTYRX2\_131  
nF2\_FF6\_RECV2 L51 MGTYRXN2\_131  
pF2\_FF6\_XMIT2 L45 MGTYTXP2\_131  
nF2\_FF6\_XMIT2 L46 MGTYTXN2\_131  
pF2\_FF6\_RECV3 K48 MGTYRX3\_131  
nF2\_FF6\_RECV3 K49 MGTYRXN3\_131  
pF2\_FF6\_XMIT3 K43 MGTYTXP3\_131  
nF2\_FF6\_XMIT3 K44 MGTYTXN3\_131



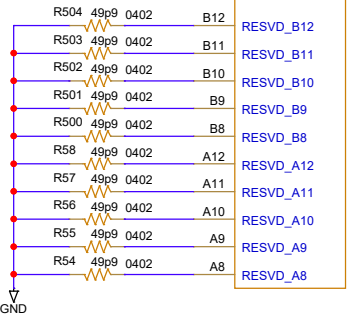
ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING  
0x50 = 7 BIT ADDRESS  
0xA0 = 8 BIT WRITE ADDRESS  
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

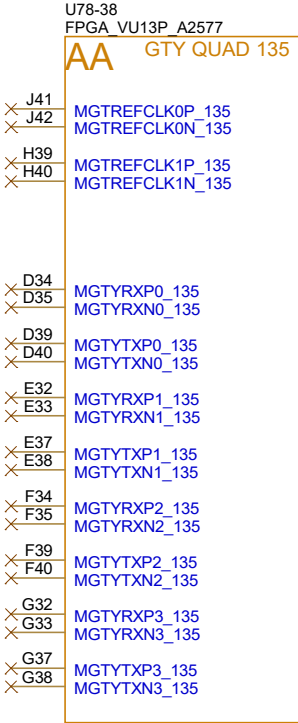
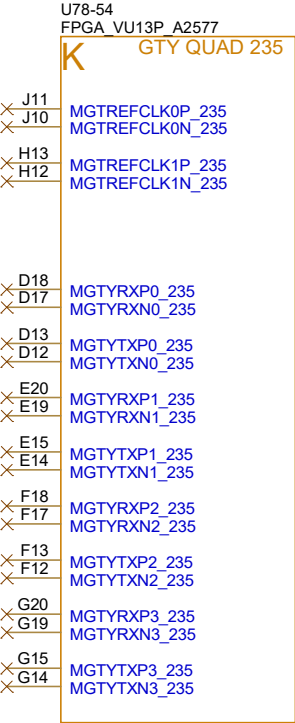


HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:  
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.  
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAXX" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.





FPGA#1

U77-40  
FPGA\_VU13P\_A2577  
GTY QUAD 221

MGTREFCLK0P\_221  
MGTREFCLK0N\_221  
MGTREFCLK1P\_221  
MGTREFCLK1N\_221

BB13  
BB12  
BA11  
BA10

MGTYRXPO\_221  
MGTYRXNO\_221  
MGTYTXPO\_221  
MGTYTXNO\_221  
MGTYRXP1\_221  
MGTYRXN1\_221  
MGTYTXP1\_221  
MGTYTXN1\_221  
MGTYRXP2\_221  
MGTYRXN2\_221  
MGTYTXP2\_221  
MGTYTXN2\_221  
MGTYRXP3\_221  
MGTYRXN3\_221  
MGTYTXP3\_221  
MGTYTXN3\_221

BK18 pF1\_M\_RECV0  
BK17 nF1\_M\_RECV0  
BL15 pF1\_M\_XMIT0  
BL14 nF1\_M\_XMIT0  
BL20 pF1\_M\_RECV1  
BL19 nF1\_M\_RECV1  
BK13 pF1\_M\_XMIT1  
BK12 nF1\_M\_XMIT1  
BL6 pF1\_M\_RECV2  
BL5 nF1\_M\_RECV2  
BL11 pF1\_M\_XMIT2  
BL10 nF1\_M\_XMIT2  
BJ6 pF1\_M\_RECV3  
BJ5 nF1\_M\_RECV3  
BK9 pF1\_M\_XMIT3  
BK8 nF1\_M\_XMIT3

pF1\_M\_RECV0  
nF1\_M\_RECV0  
C300 0.1 UF 0402  
pF2\_J\_XMIT0  
nF2\_J\_XMIT0  
C299 0.1 UF 0402  
pF1\_M\_RECV1  
nF1\_M\_RECV1  
C302 0.1 UF 0402  
pF2\_J\_XMIT1  
nF2\_J\_XMIT1  
C301 0.1 UF 0402  
pF1\_M\_RECV2  
nF1\_M\_RECV2  
C298 0.1 UF 0402  
pF2\_J\_XMIT2  
nF2\_J\_XMIT2  
C297 0.1 UF 0402  
pF1\_M\_RECV3  
nF1\_M\_RECV3  
C296 0.1 UF 0402  
pF2\_J\_XMIT3  
nF2\_J\_XMIT3  
C315 0.1 UF 0402

pF1\_M\_XMIT0  
nF1\_M\_XMIT0  
C310 0.1 UF 0402  
pF2\_J\_RECV0  
nF2\_J\_RECV0  
C309 0.1 UF 0402  
pF1\_M\_XMIT1  
nF1\_M\_XMIT1  
C308 0.1 UF 0402  
pF2\_J\_RECV1  
nF2\_J\_RECV1  
C307 0.1 UF 0402  
pF1\_M\_XMIT2  
nF1\_M\_XMIT2  
C306 0.1 UF 0402  
pF2\_J\_RECV2  
nF2\_J\_RECV2  
C305 0.1 UF 0402  
pF1\_M\_XMIT3  
nF1\_M\_XMIT3  
C304 0.1 UF 0402  
pF2\_J\_RECV3  
nF2\_J\_RECV3  
C303 0.1 UF 0402

pF2\_J\_RECV3  
nF2\_J\_RECV3  
A6  
A5  
pF2\_J\_XMIT3  
nF2\_J\_XMIT3  
A11  
A10  
pF2\_J\_RECV2  
nF2\_J\_RECV2  
A20  
A19  
pF2\_J\_XMIT2  
nF2\_J\_XMIT2  
B13  
B12  
pF2\_J\_RECV1  
nF2\_J\_RECV1  
B18  
B17  
pF2\_J\_XMIT1  
nF2\_J\_XMIT1  
A15  
A14  
pF2\_J\_RECV0  
nF2\_J\_RECV0  
C20  
C19  
pF2\_J\_XMIT0  
nF2\_J\_XMIT0  
C15  
C14

FPGA#2

U78-53  
FPGA\_VU13P\_A2577  
GTY QUAD 234

L11  
L10  
K13  
K12

MGTREFCLK0P\_234  
MGTREFCLK0N\_234  
MGTREFCLK1P\_234  
MGTREFCLK1N\_234

MGTYRXPO\_234  
MGTYRXNO\_234  
MGTYTXPO\_234  
MGTYTXNO\_234  
MGTYRXP1\_234  
MGTYRXN1\_234  
MGTYTXP1\_234  
MGTYTXN1\_234  
MGTYRXP2\_234  
MGTYRXN2\_234  
MGTYTXP2\_234  
MGTYTXN2\_234  
MGTYRXP3\_234  
MGTYRXN3\_234  
MGTYTXP3\_234  
MGTYTXN3\_234

U77-41  
FPGA\_VU13P\_A2577  
GTY QUAD 222

MGTREFCLK0P\_222  
MGTREFCLK0N\_222  
MGTREFCLK1P\_222  
MGTREFCLK1N\_222

AY13 ac\_pF1R\_R0\_N  
AY12 ac\_nF1R\_R0\_N  
AW11 ac\_pF1R\_R1\_N  
AW10 ac\_nF1R\_R1\_N

MGTYRXPO\_222  
MGTYRXNO\_222  
MGTYTXPO\_222  
MGTYTXNO\_222  
MGTYRXP1\_222  
MGTYRXN1\_222  
MGTYTXP1\_222  
MGTYTXN1\_222  
MGTYRXP2\_222  
MGTYRXN2\_222  
MGTYTXP2\_222  
MGTYTXN2\_222  
MGTYRXP3\_222  
MGTYRXN3\_222  
MGTYTXP3\_222  
MGTYTXN3\_222

BH4 pF1\_N\_RECV0  
BH3 nF1\_N\_RECV0  
BG11 pF1\_N\_XMIT0  
BG10 nF1\_N\_XMIT0  
BG2 pF1\_N\_RECV1  
BG1 nF1\_N\_RECV1  
BJ11 pF1\_N\_XMIT1  
BJ10 nF1\_N\_XMIT1  
BG6 pF1\_N\_RECV2  
BG5 nF1\_N\_RECV2  
BH9 pF1\_N\_XMIT2  
BH8 nF1\_N\_XMIT2  
BF4 pF1\_N\_RECV3  
BF3 nF1\_N\_RECV3  
BF9 pF1\_N\_XMIT3  
BF8 nF1\_N\_XMIT3

pF1\_N\_RECV0  
nF1\_N\_RECV0  
C286 0.1 UF 0402  
pF2\_I\_XMIT0  
nF2\_I\_XMIT0  
C285 0.1 UF 0402  
pF1\_N\_RECV1  
nF1\_N\_RECV1  
C282 0.1 UF 0402  
pF2\_I\_XMIT1  
nF2\_I\_XMIT1  
C281 0.1 UF 0402  
pF1\_N\_RECV2  
nF1\_N\_RECV2  
C284 0.1 UF 0402  
pF2\_I\_XMIT2  
nF2\_I\_XMIT2  
C283 0.1 UF 0402  
pF1\_N\_RECV3  
nF1\_N\_RECV3  
C280 0.1 UF 0402  
pF2\_I\_XMIT3  
nF2\_I\_XMIT3  
C279 0.1 UF 0402

pF1\_N\_XMIT0  
nF1\_N\_XMIT0  
C290 0.1 UF 0402  
pF2\_I\_RECV0  
nF2\_I\_RECV0  
C289 0.1 UF 0402  
pF1\_N\_XMIT1  
nF1\_N\_XMIT1  
C294 0.1 UF 0402  
pF2\_I\_RECV1  
nF2\_I\_RECV1  
C293 0.1 UF 0402  
pF1\_N\_XMIT2  
nF1\_N\_XMIT2  
C292 0.1 UF 0402  
pF2\_I\_RECV2  
nF2\_I\_RECV2  
C291 0.1 UF 0402  
pF1\_N\_XMIT3  
nF1\_N\_XMIT3  
C288 0.1 UF 0402  
pF2\_I\_RECV3  
nF2\_I\_RECV3  
C287 0.1 UF 0402

ac\_pF2R\_R0\_I  
ac\_nF2R\_R0\_I  
ac\_pF2R\_R1\_I  
ac\_nF2R\_R1\_I

pF2\_I\_RECV3  
nF2\_I\_RECV3  
E2  
E1  
pF2\_I\_XMIT3  
nF2\_I\_XMIT3  
D9  
D8  
pF2\_I\_RECV2  
nF2\_I\_RECV2  
D4  
D3  
pF2\_I\_XMIT2  
nF2\_I\_XMIT2  
B9  
B8  
pF2\_I\_RECV1  
nF2\_I\_RECV1  
E6  
E5  
pF2\_I\_XMIT1  
nF2\_I\_XMIT1  
C11  
C10  
pF2\_I\_RECV0  
nF2\_I\_RECV0  
C6  
C5  
pF2\_I\_XMIT0  
nF2\_I\_XMIT0  
E11  
E10

U78-52  
FPGA\_VU13P\_A2577  
GTY QUAD 233

MGTREFCLK0P\_233  
MGTREFCLK0N\_233  
MGTREFCLK1P\_233  
MGTREFCLK1N\_233

MGTYRXPO\_233  
MGTYRXNO\_233  
MGTYTXPO\_233  
MGTYTXNO\_233  
MGTYRXP1\_233  
MGTYRXN1\_233  
MGTYTXP1\_233  
MGTYTXN1\_233  
MGTYRXP2\_233  
MGTYRXN2\_233  
MGTYTXP2\_233  
MGTYTXN2\_233  
MGTYRXP3\_233  
MGTYRXN3\_233  
MGTYTXP3\_233  
MGTYTXN3\_233

U77-42  
FPGA\_VU13P\_A2577  
GTY QUAD 223

MGTREFCLK0P\_223  
MGTREFCLK0N\_223  
MGTREFCLK1P\_223  
MGTREFCLK1N\_223

AV13  
AV12  
AU11  
AU10

MGTYRXPO\_223  
MGTYRXNO\_223  
MGTYTXPO\_223  
MGTYTXNO\_223  
MGTYRXP1\_223  
MGTYRXN1\_223  
MGTYTXP1\_223  
MGTYTXN1\_223  
MGTYRXP2\_223  
MGTYRXN2\_223  
MGTYTXP2\_223  
MGTYTXN2\_223  
MGTYRXP3\_223  
MGTYRXN3\_223  
MGTYTXP3\_223  
MGTYTXN3\_223

BE2 pF1\_O\_RECV0  
BE1 nF1\_O\_RECV0  
BE7 pF1\_O\_XMIT0  
BE6 nF1\_O\_XMIT0  
BD4 pF1\_O\_RECV1  
BD3 nF1\_O\_RECV1  
BD9 pF1\_O\_XMIT1  
BD8 nF1\_O\_XMIT1  
BC2 pF1\_O\_RECV2  
BC1 nF1\_O\_RECV2  
BC7 pF1\_O\_XMIT2  
BC6 nF1\_O\_XMIT2  
BB4 pF1\_O\_RECV3  
BB3 nF1\_O\_RECV3  
BB9 pF1\_O\_XMIT3  
BB8 nF1\_O\_XMIT3

pF1\_O\_RECV0  
nF1\_O\_RECV0  
C266 0.1 UF 0402  
pF2\_H\_XMIT0  
nF2\_H\_XMIT0  
C265 0.1 UF 0402  
pF1\_O\_RECV1  
nF1\_O\_RECV1  
C264 0.1 UF 0402  
pF2\_H\_XMIT1  
nF2\_H\_XMIT1  
C263 0.1 UF 0402  
pF1\_O\_RECV2  
nF1\_O\_RECV2  
C262 0.1 UF 0402  
pF2\_H\_XMIT2  
nF2\_H\_XMIT2  
C261 0.1 UF 0402  
pF1\_O\_RECV3  
nF1\_O\_RECV3  
C260 0.1 UF 0402  
pF2\_H\_XMIT3  
nF2\_H\_XMIT3  
C259 0.1 UF 0402

pF1\_O\_XMIT0  
nF1\_O\_XMIT0  
C274 0.1 UF 0402  
pF2\_H\_RECV0  
nF2\_H\_RECV0  
C273 0.1 UF 0402  
pF1\_O\_XMIT1  
nF1\_O\_XMIT1  
C272 0.1 UF 0402  
pF2\_H\_RECV1  
nF2\_H\_RECV1  
C271 0.1 UF 0402  
pF1\_O\_XMIT2  
nF1\_O\_XMIT2  
C270 0.1 UF 0402  
pF2\_H\_RECV2  
nF2\_H\_RECV2  
C269 0.1 UF 0402  
pF1\_O\_XMIT3  
nF1\_O\_XMIT3  
C268 0.1 UF 0402  
pF2\_H\_RECV3  
nF2\_H\_RECV3  
C267 0.1 UF 0402

pF2\_H\_RECV3  
nF2\_H\_RECV3  
J2  
J1  
pF2\_H\_XMIT3  
nF2\_H\_XMIT3  
J7  
J6  
pF2\_H\_RECV2  
nF2\_H\_RECV2  
H4  
H3  
pF2\_H\_XMIT2  
nF2\_H\_XMIT2  
H9  
H8  
pF2\_H\_RECV1  
nF2\_H\_RECV1  
G2  
G1  
pF2\_H\_XMIT1  
nF2\_H\_XMIT1  
G7  
G6  
pF2\_H\_RECV0  
nF2\_H\_RECV0  
F4  
F3  
pF2\_H\_XMIT0  
nF2\_H\_XMIT0  
F9  
F8

U78-51  
FPGA\_VU13P\_A2577  
GTY QUAD 232

R11  
R10  
P13  
P12

MGTREFCLK0P\_232  
MGTREFCLK0N\_232  
MGTREFCLK1P\_232  
MGTREFCLK1N\_232

MGTYRXPO\_232  
MGTYRXNO\_232  
MGTYTXPO\_232  
MGTYTXNO\_232  
MGTYRXP1\_232  
MGTYRXN1\_232  
MGTYTXP1\_232  
MGTYTXN1\_232  
MGTYRXP2\_232  
MGTYRXN2\_232  
MGTYTXP2\_232  
MGTYTXN2\_232  
MGTYRXP3\_232  
MGTYRXN3\_232  
MGTYTXP3\_232  
MGTYTXN3\_232

APOLLO CM v3

Title			
9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H			
Size	Document Number		Rev
	6089-127		A
Date:	Thursday, January 23, 2025	Sheet	77 of 82

9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

FPGA#1

U77-44  
FPGA\_VU13P\_A2577  
GTY QUAD 225

MGTREFCLK0P\_225  
MGTREFCLK0N\_225  
MGTREFCLK1P\_225  
MGTREFCLK1N\_225

AP13  
AP12  
AN11  
AN10

MGTYRXP0\_225  
MGTYRXN0\_225  
MGTYTXP0\_225  
MGTYTXN0\_225  
MGTYRXP1\_225  
MGTYRXN1\_225  
MGTYTXP1\_225  
MGTYTXN1\_225  
MGTYRXP2\_225  
MGTYRXN2\_225  
MGTYTXP2\_225  
MGTYTXN2\_225  
MGTYRXP3\_225  
MGTYRXN3\_225  
MGTYTXP3\_225  
MGTYTXN3\_225

AU2 pF1\_A\_RECV0  
AU1 nF1\_A\_RECV0  
AU7 pF1\_A\_XMIT0  
AU6 nF1\_A\_XMIT0  
AT4 pF1\_A\_RECV1  
AT3 nF1\_A\_RECV1  
AT9 pF1\_A\_XMIT1  
AT8 nF1\_A\_XMIT1  
AR2 pF1\_A\_RECV2  
AR1 nF1\_A\_RECV2  
AR7 pF1\_A\_XMIT2  
AR6 nF1\_A\_XMIT2  
AP4 pF1\_A\_RECV3  
AP3 nF1\_A\_RECV3  
AP9 pF1\_A\_XMIT3  
AP8 nF1\_A\_XMIT3

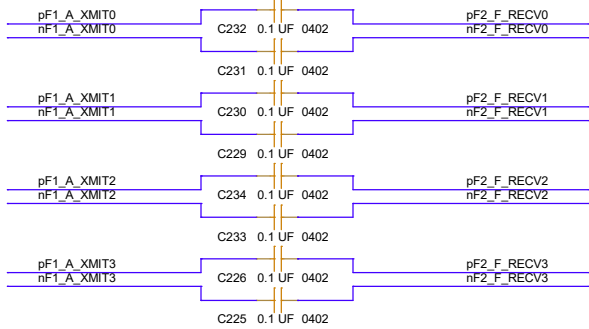
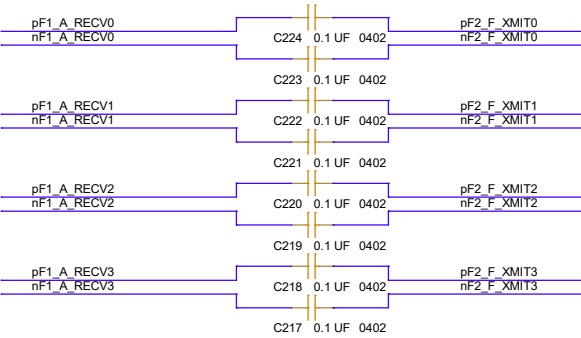
UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.



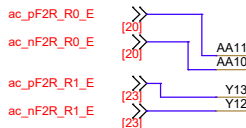
FPGA#2

U78-49  
FPGA\_VU13P\_A2577  
GTY QUAD 230

W11  
W10  
V13  
V12

MGTYRXP0\_230  
MGTYRXN0\_230  
MGTYTXP0\_230  
MGTYTXN0\_230  
MGTYRXP1\_230  
MGTYRXN1\_230  
MGTYTXP1\_230  
MGTYTXN1\_230  
MGTYRXP2\_230  
MGTYRXN2\_230  
MGTYTXP2\_230  
MGTYTXN2\_230  
MGTYRXP3\_230  
MGTYRXN3\_230  
MGTYTXP3\_230  
MGTYTXN3\_230

U2 pF2\_F\_RECV3  
U1 nF2\_F\_RECV3  
U7 pF2\_F\_XMIT3  
U6 nF2\_F\_XMIT3  
T4 pF2\_F\_RECV2  
T3 nF2\_F\_RECV2  
T9 pF2\_F\_XMIT2  
T8 nF2\_F\_XMIT2  
R2 pF2\_F\_RECV1  
R1 nF2\_F\_RECV1  
R7 pF2\_F\_XMIT1  
R6 nF2\_F\_XMIT1  
P4 pF2\_F\_RECV0  
P3 nF2\_F\_RECV0  
P9 pF2\_F\_XMIT0  
P8 nF2\_F\_XMIT0



MGTYRXP0\_229  
MGTYRXN0\_229  
MGTYTXP0\_229  
MGTYTXN0\_229  
MGTYRXP1\_229  
MGTYRXN1\_229  
MGTYTXP1\_229  
MGTYTXN1\_229  
MGTYRXP2\_229  
MGTYRXN2\_229  
MGTYTXP2\_229  
MGTYTXN2\_229  
MGTYRXP3\_229  
MGTYRXN3\_229  
MGTYTXP3\_229  
MGTYTXN3\_229

AA2 pF2\_E\_RECV3  
AA1 nF2\_E\_RECV3  
AA7 pF2\_E\_XMIT3  
AA6 nF2\_E\_XMIT3  
Y4 pF2\_E\_RECV2  
Y3 nF2\_E\_RECV2  
Y9 pF2\_E\_XMIT2  
Y8 nF2\_E\_XMIT2  
W2 pF2\_E\_RECV1  
W1 nF2\_E\_RECV1  
W7 pF2\_E\_XMIT1  
W6 nF2\_E\_XMIT1  
V4 pF2\_E\_RECV0  
V3 nF2\_E\_RECV0  
V9 pF2\_E\_XMIT0  
V8 nF2\_E\_XMIT0

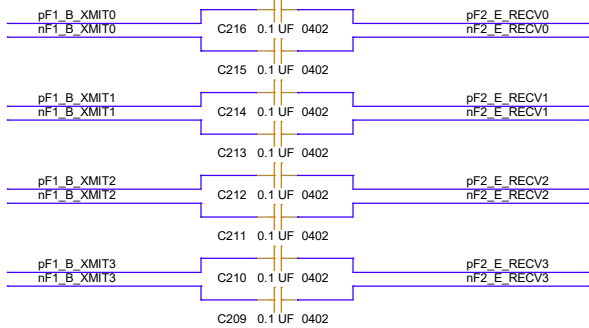
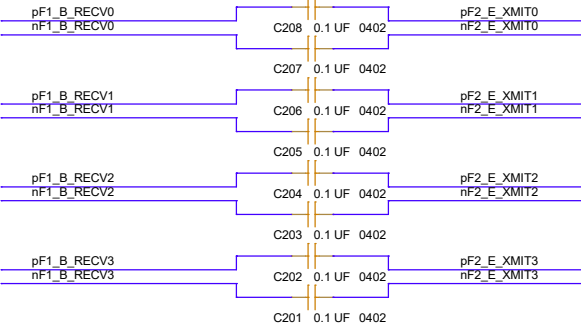
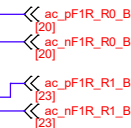
U77-45  
FPGA\_VU13P\_A2577  
GTY QUAD 226

MGTREFCLK0P\_226  
MGTREFCLK0N\_226  
MGTREFCLK1P\_226  
MGTREFCLK1N\_226

AM13  
AM12  
AL11  
AL10

MGTYRXP0\_226  
MGTYRXN0\_226  
MGTYTXP0\_226  
MGTYTXN0\_226  
MGTYRXP1\_226  
MGTYRXN1\_226  
MGTYTXP1\_226  
MGTYTXN1\_226  
MGTYRXP2\_226  
MGTYRXN2\_226  
MGTYTXP2\_226  
MGTYTXN2\_226  
MGTYRXP3\_226  
MGTYRXN3\_226  
MGTYTXP3\_226  
MGTYTXN3\_226

AN2 pF1\_B\_RECV0  
AN1 nF1\_B\_RECV0  
AN7 pF1\_B\_XMIT0  
AN6 nF1\_B\_XMIT0  
AM4 pF1\_B\_RECV1  
AM3 nF1\_B\_RECV1  
AM9 pF1\_B\_XMIT1  
AM8 nF1\_B\_XMIT1  
AL2 pF1\_B\_RECV2  
AL1 nF1\_B\_RECV2  
AL7 pF1\_B\_XMIT2  
AL6 nF1\_B\_XMIT2  
AK4 pF1\_B\_RECV3  
AK3 nF1\_B\_RECV3  
AK9 pF1\_B\_XMIT3  
AK8 nF1\_B\_XMIT3



U78-48  
FPGA\_VU13P\_A2577  
GTY QUAD 229

AA11  
AA10  
Y13  
Y12

U78-47  
FPGA\_VU13P\_A2577  
GTY QUAD 228

AE11  
AE10  
AC11  
AC10

MGTYRXP0\_228  
MGTYRXN0\_228  
MGTYTXP0\_228  
MGTYTXN0\_228  
MGTYRXP1\_228  
MGTYRXN1\_228  
MGTYTXP1\_228  
MGTYTXN1\_228  
MGTYRXP2\_228  
MGTYRXN2\_228  
MGTYTXP2\_228  
MGTYTXN2\_228  
MGTYRXP3\_228  
MGTYRXN3\_228  
MGTYTXP3\_228  
MGTYTXN3\_228

AE2 pF2\_D\_RECV3  
AE1 nF2\_D\_RECV3  
AE7 pF2\_D\_XMIT3  
AE6 nF2\_D\_XMIT3  
AD4 pF2\_D\_RECV2  
AD3 nF2\_D\_RECV2  
AD9 pF2\_D\_XMIT2  
AD8 nF2\_D\_XMIT2  
AC2 pF2\_D\_RECV1  
AC1 nF2\_D\_RECV1  
AC7 pF2\_D\_XMIT1  
AC6 nF2\_D\_XMIT1  
AB4 pF2\_D\_RECV0  
AB3 nF2\_D\_RECV0  
AB9 pF2\_D\_XMIT0  
AB8 nF2\_D\_XMIT0

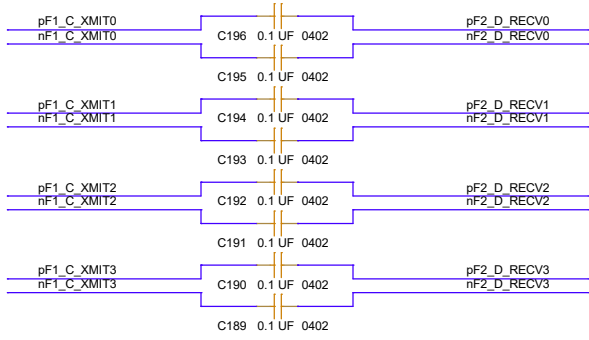
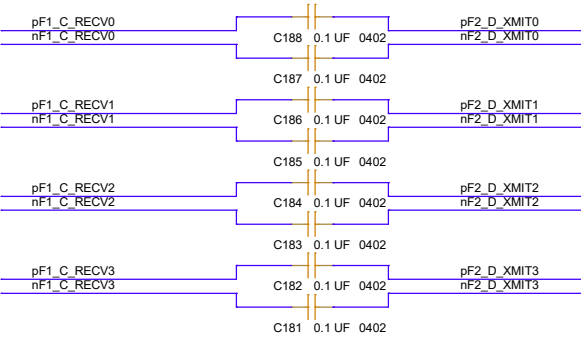
U77-46  
FPGA\_VU13P\_A2577  
GTY QUAD 227

MGTREFCLK0P\_227  
MGTREFCLK0N\_227  
MGTREFCLK1P\_227  
MGTREFCLK1N\_227

AJ11  
AJ10  
AG11  
AG10

MGTYRXP0\_227  
MGTYRXN0\_227  
MGTYTXP0\_227  
MGTYTXN0\_227  
MGTYRXP1\_227  
MGTYRXN1\_227  
MGTYTXP1\_227  
MGTYTXN1\_227  
MGTYRXP2\_227  
MGTYRXN2\_227  
MGTYTXP2\_227  
MGTYTXN2\_227  
MGTYRXP3\_227  
MGTYRXN3\_227  
MGTYTXP3\_227  
MGTYTXN3\_227

AJ2 pF1\_C\_RECV0  
AJ1 nF1\_C\_RECV0  
AJ7 pF1\_C\_XMIT0  
AJ6 nF1\_C\_XMIT0  
AH4 pF1\_C\_RECV1  
AH3 nF1\_C\_RECV1  
AH9 pF1\_C\_XMIT1  
AH8 nF1\_C\_XMIT1  
AG2 pF1\_C\_RECV2  
AG1 nF1\_C\_RECV2  
AG7 pF1\_C\_XMIT2  
AG6 nF1\_C\_XMIT2  
AF4 pF1\_C\_RECV3  
AF3 nF1\_C\_RECV3  
AF9 pF1\_C\_XMIT3  
AF8 nF1\_C\_XMIT3



APOLLO CM v3

Title			
9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D			
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FPGA#1

U77-51  
FPGA\_VU13P\_A2577  
GTY QUAD 232

MGTREFCLK0P\_232  
MGTREFCLK0N\_232  
MGTREFCLK1P\_232  
MGTREFCLK1N\_232

R11  
R10  
P13  
P12

MGTYRXP0\_232  
MGTYRXN0\_232  
MGTYXP0\_232  
MGTYXN0\_232  
MGTYRXP1\_232  
MGTYRXN1\_232  
MGTYXP1\_232  
MGTYXN1\_232  
MGTYRXP2\_232  
MGTYRXN2\_232  
MGTYXP2\_232  
MGTYXN2\_232  
MGTYRXP3\_232  
MGTYRXN3\_232  
MGTYXP3\_232  
MGTYXN3\_232

J2 pF1\_H\_RECV0  
J1 nF1\_H\_RECV0  
J7 pF1\_H\_XMIT0  
J6 nF1\_H\_XMIT0  
H4 pF1\_H\_RECV1  
H3 nF1\_H\_RECV1  
H9 pF1\_H\_XMIT1  
H8 nF1\_H\_XMIT1  
G2 pF1\_H\_RECV2  
G1 nF1\_H\_RECV2  
G7 pF1\_H\_XMIT2  
G6 nF1\_H\_XMIT2  
F4 pF1\_H\_RECV3  
F3 nF1\_H\_RECV3  
F9 pF1\_H\_XMIT3  
F8 nF1\_H\_XMIT3

pF1\_H\_RECV0  
nF1\_H\_RECV0  
C91 0.1 UF 0402  
pF2\_O\_XMIT0  
nF2\_O\_XMIT0  
C90 0.1 UF 0402  
pF1\_H\_RECV1  
nF1\_H\_RECV1  
C89 0.1 UF 0402  
pF2\_O\_XMIT1  
nF2\_O\_XMIT1  
C88 0.1 UF 0402  
pF1\_H\_RECV2  
nF1\_H\_RECV2  
C87 0.1 UF 0402  
pF2\_O\_XMIT2  
nF2\_O\_XMIT2  
C86 0.1 UF 0402  
pF1\_H\_RECV3  
nF1\_H\_RECV3  
C85 0.1 UF 0402  
pF2\_O\_XMIT3  
nF2\_O\_XMIT3  
C84 0.1 UF 0402

pF1\_H\_XMIT0  
nF1\_H\_XMIT0  
C99 0.1 UF 0402  
pF2\_O\_RECV0  
nF2\_O\_RECV0  
C98 0.1 UF 0402  
pF1\_H\_XMIT1  
nF1\_H\_XMIT1  
C97 0.1 UF 0402  
pF2\_O\_RECV1  
nF2\_O\_RECV1  
C102 0.1 UF 0402  
pF1\_H\_XMIT2  
nF1\_H\_XMIT2  
C101 0.1 UF 0402  
pF2\_O\_RECV2  
nF2\_O\_RECV2  
C94 0.1 UF 0402  
pF1\_H\_XMIT3  
nF1\_H\_XMIT3  
C93 0.1 UF 0402  
pF2\_O\_RECV3  
nF2\_O\_RECV3  
C92 0.1 UF 0402

pF2\_O\_RECV3  
nF2\_O\_RECV3  
BE2  
BE1  
pF2\_O\_XMIT3  
nF2\_O\_XMIT3  
BE7  
BE6  
pF2\_O\_RECV2  
nF2\_O\_RECV2  
BD4  
BD3  
pF2\_O\_XMIT2  
nF2\_O\_XMIT2  
BD9  
BD8  
pF2\_O\_RECV1  
nF2\_O\_RECV1  
BC2  
BC1  
pF2\_O\_XMIT1  
nF2\_O\_XMIT1  
BC7  
BC6  
pF2\_O\_RECV0  
nF2\_O\_RECV0  
BB4  
BB3  
pF2\_O\_XMIT0  
nF2\_O\_XMIT0  
BB9  
BB8

FPGA#2

U78-42  
FPGA\_VU13P\_A2577  
GTY QUAD 223

AV13  
AV12  
AU11  
AU10

MGTREFCLK0P\_223  
MGTREFCLK0N\_223  
MGTREFCLK1P\_223  
MGTREFCLK1N\_223

MGTYRXP0\_223  
MGTYRXN0\_223  
MGTYXP0\_223  
MGTYXN0\_223  
MGTYRXP1\_223  
MGTYRXN1\_223  
MGTYXP1\_223  
MGTYXN1\_223  
MGTYRXP2\_223  
MGTYRXN2\_223  
MGTYXP2\_223  
MGTYXN2\_223  
MGTYRXP3\_223  
MGTYRXN3\_223  
MGTYXP3\_223  
MGTYXN3\_223

ac\_pF2R\_R0\_N  
ac\_nF2R\_R0\_N  
ac\_pF2R\_R1\_N  
ac\_nF2R\_R1\_N

pF2\_N\_RECV3  
nF2\_N\_RECV3  
BH4  
BH3  
pF2\_N\_XMIT3  
nF2\_N\_XMIT3  
BG11  
BG10  
pF2\_N\_RECV2  
nF2\_N\_RECV2  
BG2  
BG1  
pF2\_N\_XMIT2  
nF2\_N\_XMIT2  
BJ11  
BJ10  
pF2\_N\_RECV1  
nF2\_N\_RECV1  
BG6  
BG5  
pF2\_N\_XMIT1  
nF2\_N\_XMIT1  
BH9  
BH8  
pF2\_N\_RECV0  
nF2\_N\_RECV0  
BF4  
BF3  
pF2\_N\_XMIT0  
nF2\_N\_XMIT0  
BF9  
BF8

MGTREFCLK0P\_222  
MGTREFCLK0N\_222  
MGTREFCLK1P\_222  
MGTREFCLK1N\_222

MGTYRXP0\_222  
MGTYRXN0\_222  
MGTYXP0\_222  
MGTYXN0\_222  
MGTYRXP1\_222  
MGTYRXN1\_222  
MGTYXP1\_222  
MGTYXN1\_222  
MGTYRXP2\_222  
MGTYRXN2\_222  
MGTYXP2\_222  
MGTYXN2\_222  
MGTYRXP3\_222  
MGTYRXN3\_222  
MGTYXP3\_222  
MGTYXN3\_222

U77-52  
FPGA\_VU13P\_A2577  
GTY QUAD 233

MGTREFCLK0P\_233  
MGTREFCLK0N\_233  
MGTREFCLK1P\_233  
MGTREFCLK1N\_233

N11  
N10  
M13  
M12

MGTYRXP0\_233  
MGTYRXN0\_233  
MGTYXP0\_233  
MGTYXN0\_233  
MGTYRXP1\_233  
MGTYRXN1\_233  
MGTYXP1\_233  
MGTYXN1\_233  
MGTYRXP2\_233  
MGTYRXN2\_233  
MGTYXP2\_233  
MGTYXN2\_233  
MGTYRXP3\_233  
MGTYRXN3\_233  
MGTYXP3\_233  
MGTYXN3\_233

E2 pF1\_I\_RECV0  
E1 nF1\_I\_RECV0  
D9 pF1\_I\_XMIT0  
D8 nF1\_I\_XMIT0  
D4 pF1\_I\_RECV1  
D3 nF1\_I\_RECV1  
B9 pF1\_I\_XMIT1  
B8 nF1\_I\_XMIT1  
E6 pF1\_I\_RECV2  
E5 nF1\_I\_RECV2  
C11 pF1\_I\_XMIT2  
C10 nF1\_I\_XMIT2  
C6 pF1\_I\_RECV3  
C5 nF1\_I\_RECV3  
E11 pF1\_I\_XMIT3  
E10 nF1\_I\_XMIT3

pF1\_I\_RECV0  
nF1\_I\_RECV0  
C71 0.1 UF 0402  
pF2\_N\_XMIT0  
nF2\_N\_XMIT0  
C70 0.1 UF 0402  
pF1\_I\_RECV1  
nF1\_I\_RECV1  
C69 0.1 UF 0402  
pF2\_N\_XMIT1  
nF2\_N\_XMIT1  
C68 0.1 UF 0402  
pF1\_I\_RECV2  
nF1\_I\_RECV2  
C64 0.1 UF 0402  
pF2\_N\_XMIT2  
nF2\_N\_XMIT2  
C65 0.1 UF 0402  
pF1\_I\_RECV3  
nF1\_I\_RECV3  
C66 0.1 UF 0402  
pF2\_N\_XMIT3  
nF2\_N\_XMIT3  
C67 0.1 UF 0402

pF1\_I\_XMIT0  
nF1\_I\_XMIT0  
C79 0.1 UF 0402  
pF2\_N\_RECV0  
nF2\_N\_RECV0  
C78 0.1 UF 0402  
pF1\_I\_XMIT1  
nF1\_I\_XMIT1  
C77 0.1 UF 0402  
pF2\_N\_RECV1  
nF2\_N\_RECV1  
C76 0.1 UF 0402  
pF1\_I\_XMIT2  
nF1\_I\_XMIT2  
C74 0.1 UF 0402  
pF2\_N\_RECV2  
nF2\_N\_RECV2  
C75 0.1 UF 0402  
pF1\_I\_XMIT3  
nF1\_I\_XMIT3  
C72 0.1 UF 0402  
pF2\_N\_RECV3  
nF2\_N\_RECV3  
C73 0.1 UF 0402

BB13  
BB12  
BA11  
BA10

MGTREFCLK0P\_221  
MGTREFCLK0N\_221  
MGTREFCLK1P\_221  
MGTREFCLK1N\_221

MGTYRXP0\_221  
MGTYRXN0\_221  
MGTYXP0\_221  
MGTYXN0\_221  
MGTYRXP1\_221  
MGTYRXN1\_221  
MGTYXP1\_221  
MGTYXN1\_221  
MGTYRXP2\_221  
MGTYRXN2\_221  
MGTYXP2\_221  
MGTYXN2\_221  
MGTYRXP3\_221  
MGTYRXN3\_221  
MGTYXP3\_221  
MGTYXN3\_221

U77-53  
FPGA\_VU13P\_A2577  
GTY QUAD 234

MGTREFCLK0P\_234  
MGTREFCLK0N\_234  
MGTREFCLK1P\_234  
MGTREFCLK1N\_234

L11  
L10  
K13  
K12

MGTYRXP0\_234  
MGTYRXN0\_234  
MGTYXP0\_234  
MGTYXN0\_234  
MGTYRXP1\_234  
MGTYRXN1\_234  
MGTYXP1\_234  
MGTYXN1\_234  
MGTYRXP2\_234  
MGTYRXN2\_234  
MGTYXP2\_234  
MGTYXN2\_234  
MGTYRXP3\_234  
MGTYRXN3\_234  
MGTYXP3\_234  
MGTYXN3\_234

A6 pF1\_J\_RECV0  
A5 nF1\_J\_RECV0  
A11 pF1\_J\_XMIT0  
A10 nF1\_J\_XMIT0  
A20 pF1\_J\_RECV1  
A19 nF1\_J\_RECV1  
B13 pF1\_J\_XMIT1  
B12 nF1\_J\_XMIT1  
B18 pF1\_J\_RECV2  
B17 nF1\_J\_RECV2  
A15 pF1\_J\_XMIT2  
A14 nF1\_J\_XMIT2  
C20 pF1\_J\_RECV3  
C19 nF1\_J\_RECV3  
C15 pF1\_J\_XMIT3  
C14 nF1\_J\_XMIT3

pF1\_J\_RECV0  
nF1\_J\_RECV0  
C54 0.1 UF 0402  
pF2\_M\_XMIT0  
nF2\_M\_XMIT0  
C55 0.1 UF 0402  
pF1\_J\_RECV1  
nF1\_J\_RECV1  
C52 0.1 UF 0402  
pF2\_M\_XMIT1  
nF2\_M\_XMIT1  
C53 0.1 UF 0402  
pF1\_J\_RECV2  
nF1\_J\_RECV2  
C50 0.1 UF 0402  
pF2\_M\_XMIT2  
nF2\_M\_XMIT2  
C51 0.1 UF 0402  
pF1\_J\_RECV3  
nF1\_J\_RECV3  
C48 0.1 UF 0402  
pF2\_M\_XMIT3  
nF2\_M\_XMIT3  
C49 0.1 UF 0402

pF1\_J\_XMIT0  
nF1\_J\_XMIT0  
C62 0.1 UF 0402  
pF2\_M\_RECV0  
nF2\_M\_RECV0  
C63 0.1 UF 0402  
pF1\_J\_XMIT1  
nF1\_J\_XMIT1  
C60 0.1 UF 0402  
pF2\_M\_RECV1  
nF2\_M\_RECV1  
C61 0.1 UF 0402  
pF1\_J\_XMIT2  
nF1\_J\_XMIT2  
C56 0.1 UF 0402  
pF2\_M\_RECV2  
nF2\_M\_RECV2  
C57 0.1 UF 0402  
pF1\_J\_XMIT3  
nF1\_J\_XMIT3  
C58 0.1 UF 0402  
pF2\_M\_RECV3  
nF2\_M\_RECV3  
C59 0.1 UF 0402

pF2\_M\_RECV3  
nF2\_M\_RECV3  
BK18  
BK17  
pF2\_M\_XMIT3  
nF2\_M\_XMIT3  
BL15  
BL14  
pF2\_M\_RECV2  
nF2\_M\_RECV2  
BL20  
BL19  
pF2\_M\_XMIT2  
nF2\_M\_XMIT2  
BK13  
BK12  
pF2\_M\_RECV1  
nF2\_M\_RECV1  
BL6  
BL5  
pF2\_M\_XMIT1  
nF2\_M\_XMIT1  
BL11  
BL10  
pF2\_M\_RECV0  
nF2\_M\_RECV0  
BJ6  
BJ5  
pF2\_M\_XMIT0  
nF2\_M\_XMIT0  
BK9  
BK8

U78-40  
FPGA\_VU13P\_A2577  
GTY QUAD 221

BB13  
BB12  
BA11  
BA10

MGTREFCLK0P\_221  
MGTREFCLK0N\_221  
MGTREFCLK1P\_221  
MGTREFCLK1N\_221

MGTYRXP0\_221  
MGTYRXN0\_221  
MGTYXP0\_221  
MGTYXN0\_221  
MGTYRXP1\_221  
MGTYRXN1\_221  
MGTYXP1\_221  
MGTYXN1\_221  
MGTYRXP2\_221  
MGTYRXN2\_221  
MGTYXP2\_221  
MGTYXN2\_221  
MGTYRXP3\_221  
MGTYRXN3\_221  
MGTYXP3\_221  
MGTYXN3\_221

APOLLO CM v3

Title			
9.03: F1 QUADS H, I, J TO F2 QUADS O, N, M			
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9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A

FPGA#1

U77-47  
FPGA\_VU13P\_A2577  
GTY QUAD 228

MGTREFCLK0P\_228  
MGTREFCLK0N\_228  
MGTREFCLK1P\_228  
MGTREFCLK1N\_228

AE11  
AE10  
AC11  
AC10

MGTYRXPO\_228  
MGTYRXNO\_228  
MGTYTXPO\_228  
MGTYTXNO\_228  
MGTYRXPI\_228  
MGTYRXNI\_228  
MGTYTXPI\_228  
MGTYTXNI\_228  
MGTYRXPI\_228  
MGTYRXNI\_228  
MGTYTXPI\_228  
MGTYTXNI\_228  
MGTYRXPI\_228  
MGTYRXNI\_228  
MGTYTXPI\_228  
MGTYTXNI\_228  
MGTYRXPI\_228  
MGTYRXNI\_228  
MGTYTXPI\_228  
MGTYTXNI\_228

AE2 pF1\_D\_RECV0  
AE1 nF1\_D\_RECV0  
AE7 pF1\_D\_XMIT0  
AE6 nF1\_D\_XMIT0  
AD4 pF1\_D\_RECV1  
AD3 nF1\_D\_RECV1  
AD9 pF1\_D\_XMIT1  
AD8 nF1\_D\_XMIT1  
AC2 pF1\_D\_RECV2  
AC1 nF1\_D\_RECV2  
AC7 pF1\_D\_XMIT2  
AC6 nF1\_D\_XMIT2  
AB4 pF1\_D\_RECV3  
AB3 nF1\_D\_RECV3  
AB9 pF1\_D\_XMIT3  
AB8 nF1\_D\_XMIT3

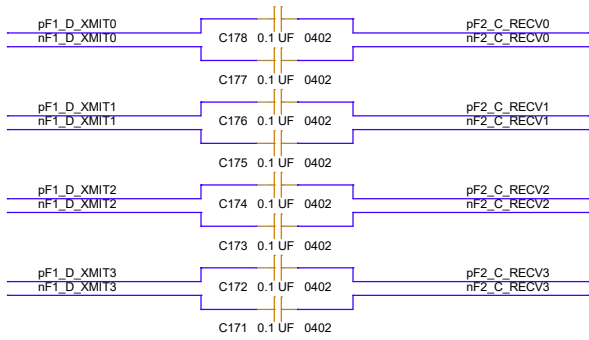
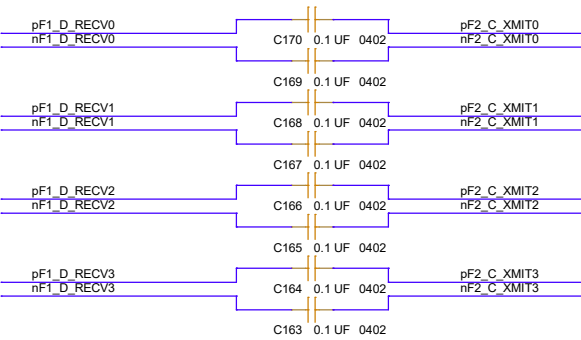
UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.



FPGA#2

U78-46  
FPGA\_VU13P\_A2577  
GTY QUAD 227

AJ11  
AJ10  
AG11  
AG10

MGTYRXPO\_227  
MGTYRXNO\_227  
MGTYTXPO\_227  
MGTYTXNO\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227

pF2\_C\_RECV3  
nF2\_C\_RECV3  
pF2\_C\_XMIT3  
nF2\_C\_XMIT3  
pF2\_C\_RECV2  
nF2\_C\_RECV2  
pF2\_C\_XMIT2  
nF2\_C\_XMIT2  
pF2\_C\_RECV1  
nF2\_C\_RECV1  
pF2\_C\_XMIT1  
nF2\_C\_XMIT1  
pF2\_C\_RECV0  
nF2\_C\_RECV0  
pF2\_C\_XMIT0  
nF2\_C\_XMIT0

MGTREFCLK0P\_227  
MGTREFCLK0N\_227  
MGTREFCLK1P\_227  
MGTREFCLK1N\_227

MGTYRXPO\_227  
MGTYRXNO\_227  
MGTYTXPO\_227  
MGTYTXNO\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227  
MGTYRXPI\_227  
MGTYRXNI\_227  
MGTYTXPI\_227  
MGTYTXNI\_227

pF2\_C\_RECV3  
nF2\_C\_RECV3  
pF2\_C\_XMIT3  
nF2\_C\_XMIT3  
pF2\_C\_RECV2  
nF2\_C\_RECV2  
pF2\_C\_XMIT2  
nF2\_C\_XMIT2  
pF2\_C\_RECV1  
nF2\_C\_RECV1  
pF2\_C\_XMIT1  
nF2\_C\_XMIT1  
pF2\_C\_RECV0  
nF2\_C\_RECV0  
pF2\_C\_XMIT0  
nF2\_C\_XMIT0

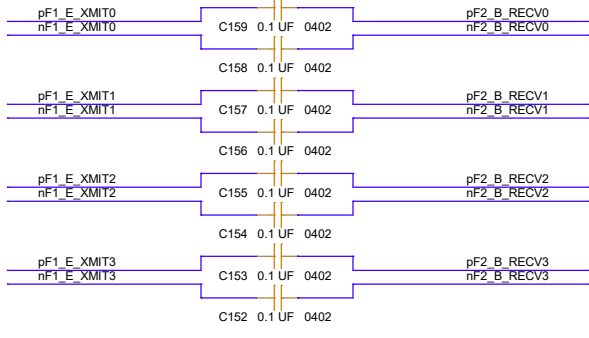
ac\_pF2R\_R0\_B  
ac\_nF2R\_R0\_B  
ac\_pF2R\_R1\_B  
ac\_nF2R\_R1\_B

MGTYRXPO\_226  
MGTYRXNO\_226  
MGTYTXPO\_226  
MGTYTXNO\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226

AM13  
AM12  
AL11  
AL10

MGTREFCLK0P\_226  
MGTREFCLK0N\_226  
MGTREFCLK1P\_226  
MGTREFCLK1N\_226

MGTYRXPO\_226  
MGTYRXNO\_226  
MGTYTXPO\_226  
MGTYTXNO\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226



pF2\_B\_RECV3  
nF2\_B\_RECV3  
pF2\_B\_XMIT3  
nF2\_B\_XMIT3  
pF2\_B\_RECV2  
nF2\_B\_RECV2  
pF2\_B\_XMIT2  
nF2\_B\_XMIT2  
pF2\_B\_RECV1  
nF2\_B\_RECV1  
pF2\_B\_XMIT1  
nF2\_B\_XMIT1  
pF2\_B\_RECV0  
nF2\_B\_RECV0  
pF2\_B\_XMIT0  
nF2\_B\_XMIT0

MGTYRXPO\_226  
MGTYRXNO\_226  
MGTYTXPO\_226  
MGTYTXNO\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226  
MGTYRXPI\_226  
MGTYRXNI\_226  
MGTYTXPI\_226  
MGTYTXNI\_226

U77-48  
FPGA\_VU13P\_A2577  
GTY QUAD 229

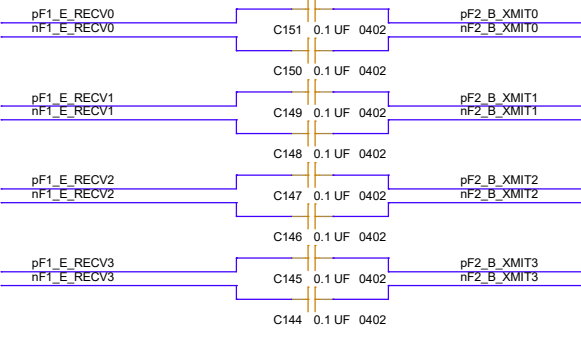
MGTREFCLK0P\_229  
MGTREFCLK0N\_229  
MGTREFCLK1P\_229  
MGTREFCLK1N\_229

AA11  
AA10  
Y13  
Y12

MGTYRXPO\_229  
MGTYRXNO\_229  
MGTYTXPO\_229  
MGTYTXNO\_229  
MGTYRXPI\_229  
MGTYRXNI\_229  
MGTYTXPI\_229  
MGTYTXNI\_229  
MGTYRXPI\_229  
MGTYRXNI\_229  
MGTYTXPI\_229  
MGTYTXNI\_229  
MGTYRXPI\_229  
MGTYRXNI\_229  
MGTYTXPI\_229  
MGTYTXNI\_229  
MGTYRXPI\_229  
MGTYRXNI\_229  
MGTYTXPI\_229  
MGTYTXNI\_229

AA2 pF1\_E\_RECV0  
AA1 nF1\_E\_RECV0  
AA7 pF1\_E\_XMIT0  
AA6 nF1\_E\_XMIT0  
Y4 pF1\_E\_RECV1  
Y3 nF1\_E\_RECV1  
Y9 pF1\_E\_XMIT1  
Y8 nF1\_E\_XMIT1  
W2 pF1\_E\_RECV2  
W1 nF1\_E\_RECV2  
W7 pF1\_E\_XMIT2  
W6 nF1\_E\_XMIT2  
V4 pF1\_E\_RECV3  
V3 nF1\_E\_RECV3  
V9 pF1\_E\_XMIT3  
V8 nF1\_E\_XMIT3

ac\_pF1R\_R0\_E  
ac\_nF1R\_R0\_E  
ac\_pF1R\_R1\_E  
ac\_nF1R\_R1\_E



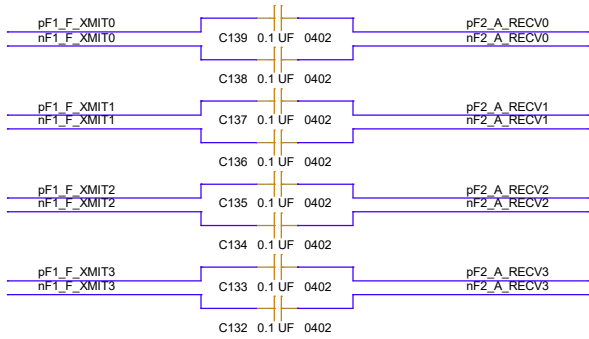
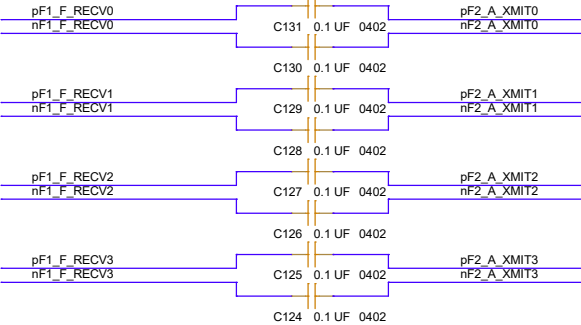
U77-49  
FPGA\_VU13P\_A2577  
GTY QUAD 230

MGTREFCLK0P\_230  
MGTREFCLK0N\_230  
MGTREFCLK1P\_230  
MGTREFCLK1N\_230

W11  
W10  
V13  
V12

MGTYRXPO\_230  
MGTYRXNO\_230  
MGTYTXPO\_230  
MGTYTXNO\_230  
MGTYRXPI\_230  
MGTYRXNI\_230  
MGTYTXPI\_230  
MGTYTXNI\_230  
MGTYRXPI\_230  
MGTYRXNI\_230  
MGTYTXPI\_230  
MGTYTXNI\_230  
MGTYRXPI\_230  
MGTYRXNI\_230  
MGTYTXPI\_230  
MGTYTXNI\_230  
MGTYRXPI\_230  
MGTYRXNI\_230  
MGTYTXPI\_230  
MGTYTXNI\_230

U2 pF1\_F\_RECV0  
U1 nF1\_F\_RECV0  
U7 pF1\_F\_XMIT0  
U6 nF1\_F\_XMIT0  
T4 pF1\_F\_RECV1  
T3 nF1\_F\_RECV1  
T9 pF1\_F\_XMIT1  
T8 nF1\_F\_XMIT1  
R2 pF1\_F\_RECV2  
R1 nF1\_F\_RECV2  
R7 pF1\_F\_XMIT2  
R6 nF1\_F\_XMIT2  
P4 pF1\_F\_RECV3  
P3 nF1\_F\_RECV3  
P9 pF1\_F\_XMIT3  
P8 nF1\_F\_XMIT3



U78-44  
FPGA\_VU13P\_A2577  
GTY QUAD 225

AP13  
AP12  
AN11  
AN10

MGTYRXPO\_225  
MGTYRXNO\_225  
MGTYTXPO\_225  
MGTYTXNO\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225

pF2\_A\_RECV3  
nF2\_A\_RECV3  
pF2\_A\_XMIT3  
nF2\_A\_XMIT3  
pF2\_A\_RECV2  
nF2\_A\_RECV2  
pF2\_A\_XMIT2  
nF2\_A\_XMIT2  
pF2\_A\_RECV1  
nF2\_A\_RECV1  
pF2\_A\_XMIT1  
nF2\_A\_XMIT1  
pF2\_A\_RECV0  
nF2\_A\_RECV0  
pF2\_A\_XMIT0  
nF2\_A\_XMIT0

MGTREFCLK0P\_225  
MGTREFCLK0N\_225  
MGTREFCLK1P\_225  
MGTREFCLK1N\_225

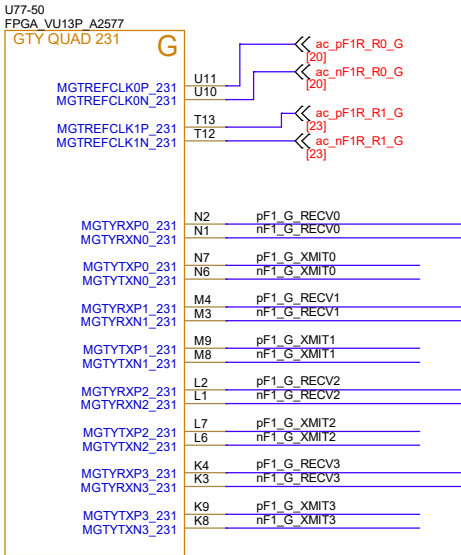
MGTYRXPO\_225  
MGTYRXNO\_225  
MGTYTXPO\_225  
MGTYTXNO\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225  
MGTYRXPI\_225  
MGTYRXNI\_225  
MGTYTXPI\_225  
MGTYTXNI\_225

APOLLO CM v3

9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A			
Size	Document Number	Rev	
	6089-127	A	
Date:	Thursday, January 23, 2025	Sheet	80 of 82



FPGA#1

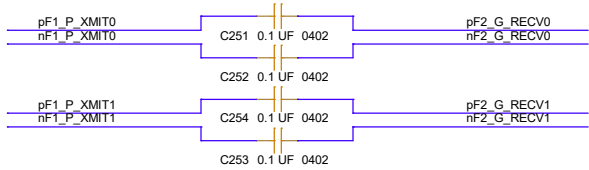
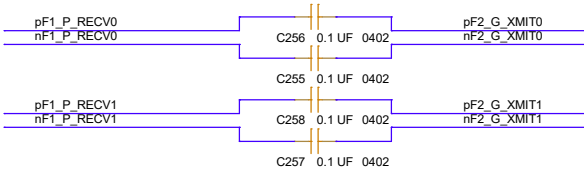
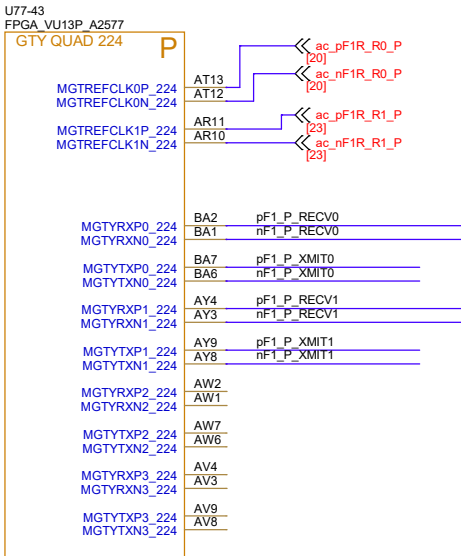
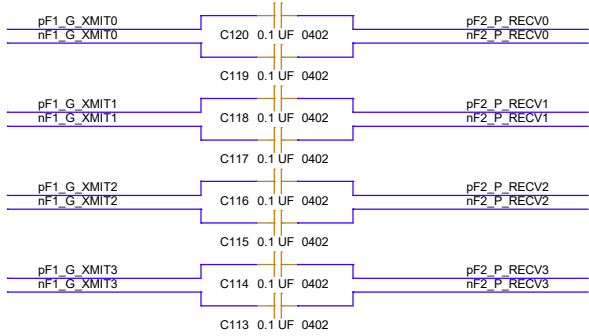
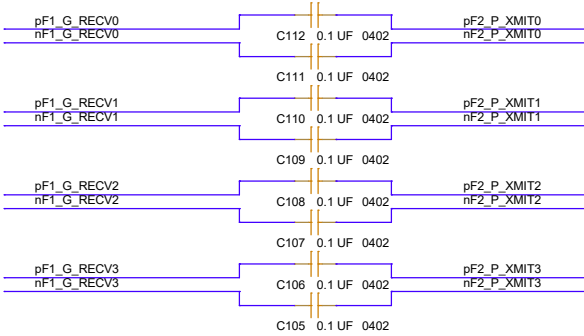


UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_DIFFCLK" ELECTRICAL CONSTRAINT SET.  
THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS\_28G" ELECTRICAL CONSTRAINT SET.

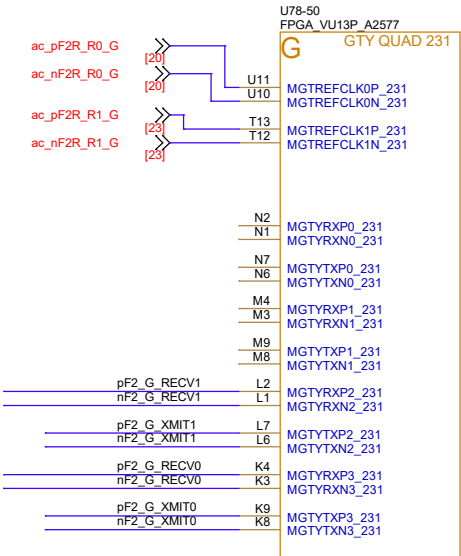
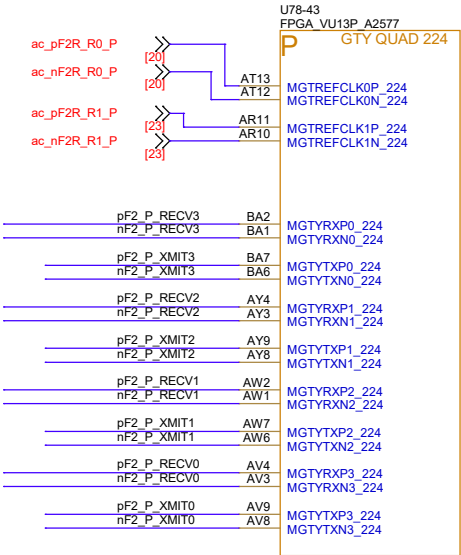
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.



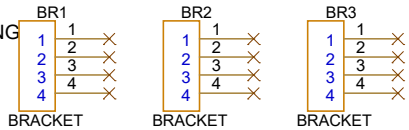
THERE IS ONLY SPACE ON THE PCB FOR 8 CAPACITORS. THIS SUPPORTS TWO OF THE FOUR TRANSMIT/RECEIVE PAIRS.

FPGA#2

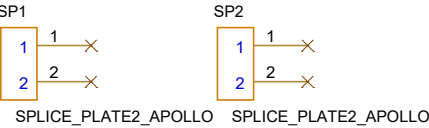


THESE SHAPES DEFINE MECHANICAL OBJECTS THAT SHOULD BE IN THE BILL OF MATERIALS.

BRACKETS FOR SUPPORTING A SUB-FRONT PANEL



THESE SHAPES DEFINE HOLES AND KEEPOUT AREAS FOR THE SPLICE PLATES.



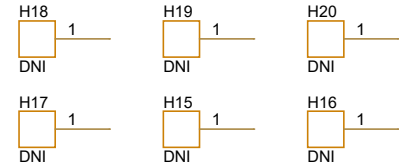
THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINK



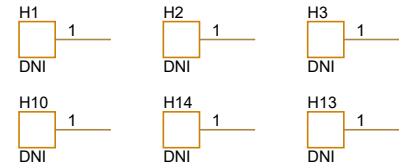
THESE HOLES ARE FOR MOUNTING THE LGA80D HEATSINK



THESE STANDOFFS ARE FOR MOUNTING THE BOTTOM COVER. THE STANDOFF IS SOLDERED TO THE BOTTOM SIDE OF THE BOARD.



THESE STANDOFFS ARE FOR MOUNTING THE TOP COVER. THE STANDOFF IS SCREWED FROM THE BOTTOM SIDE OF THE BOARD.



H21 THRU H28 ARE FOR MOUNTING STANDOFFS FOR THE FPGA HEATSINKS. THE HOLES ARE PART OF THE FOOTPRINT, SO DISCRETE PARTS DO NOT APPEAR ON THE SCHEMATIC.