THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE. ON ANY PAGE, THE NUMBER OF THE CONNECTING PAGE(S) IS SHOWN IN A SMALL NUMBER BELOW THE SIGNAL NAME. PAGE NUMBERS CAN BE FOUND IN SMALL TYPE AT THE BOTTOM OF THE TITLE BLOCK.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY. THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: OFF-BOARD SIGNALS (SM AND FRONT PANEL), GLOBAL CLOCKING
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: FPGA#1 POWER AND SIGNAL (NON-MGT)
6: FPGA#2 POWER AND SIGNAL (NON-MGT)
7: FPGA#1 GTY TRANSCEIVERS (MOSTLY FIREFLY)
8: FPGA#2 GTY TRANSCEIVERS (MOSTLY FIREFLY)
9: BETWEEN-FPGA GTY TRANSCEIVERS

These are some general signal naming conventions:

1) Signals connected to the FPGAs contain either "F1" or "F2".

2) Signals connected to the Service Module contain "SM".

3) Signals connected to the Front Panel contain "FP".

4) Signal names starting with “PG” are “Power Good” signals from power modules.

5) Signal names starting with “EN” are “Enable” signals to turn on power modules.

6) GTY reference clock names indicate FPGA followed by side (F1L, F1R, F2L, F2R), then the reference clock (R0 or R1), finishing with the sequence order (1 thru 7).

7) Power source names start with "V_", then the voltage with the letter "V" as a decimal point. (V_3V3 is a 3.3 volt source)

8) The MCU I/Os are 3.3 volt and the FPGA I/Os are 1.8 volt. Level shifters are used for the conversion. Signal names on the FPGA side are prefaced with "lov" (low voltage) and signals on the MCU side are prefaced with "hiv" (high voltage).

Make JPG pictures for the block diagrams by displaying them in a PowerPoint slide show that fills the screen. Do a "print screen", then paste it in "paint". Crop, save file, and insert picture.

TO DO:

Consider making page numbers larger

Update MCU code with new scale factor for 12V current reading

Update FPGA pin constraint file

Make design notes on the 5 synth pages match

APOLLO CM v3		
Title: 1.01: NOTES		
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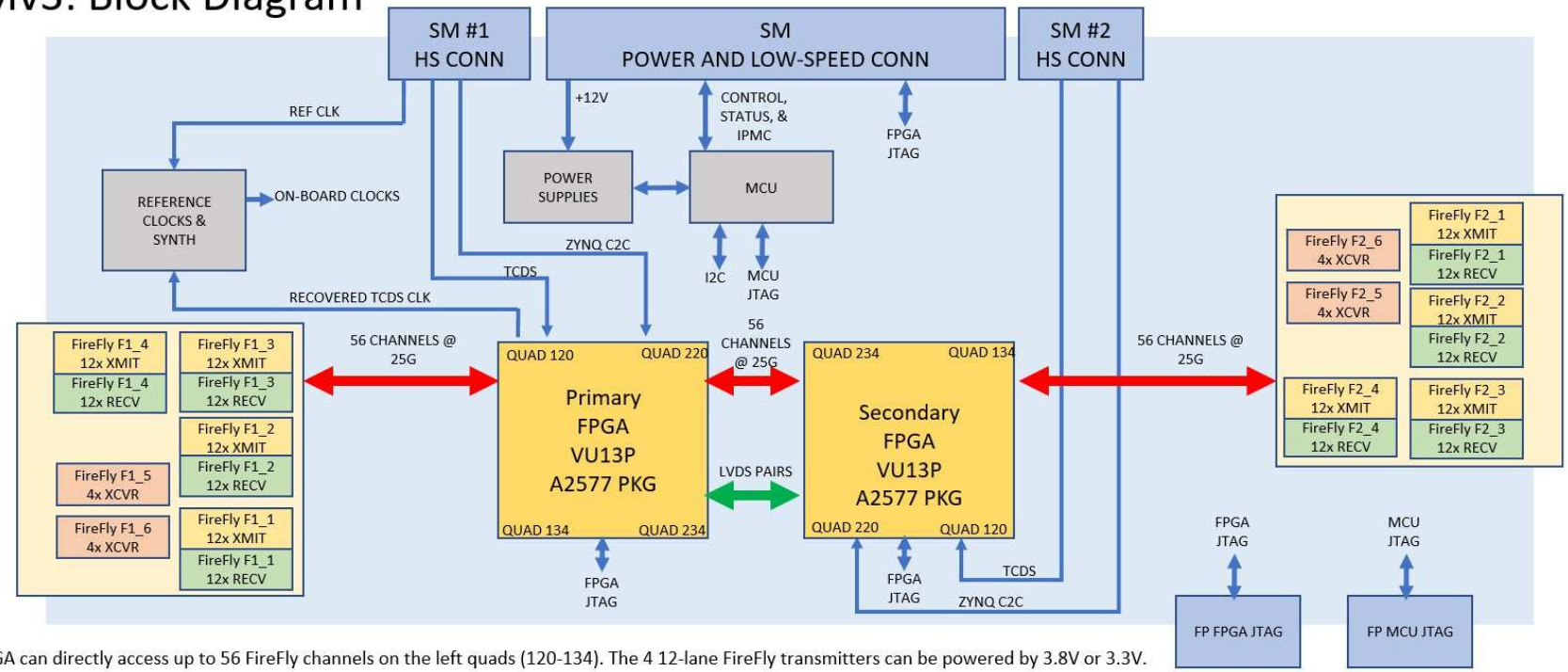
Apollo CMv3: Block Diagram



- Each FPGA can directly access up to 56 FireFly channels on the left quads (120-134). The 4 12-lane FireFly transmitters can be powered by 3.8V or 3.3V.
- 56 GTY links are provided between the FPGA sites on the right quads (220-234). These are AC-coupled.
- Other I/O:
  - 2 GTY links for chip-to-chip (or PCI) from each FPGA to the Zynq on the SM (Service Module).
  - 1 GTY link for TCDS from each FPGA to the SM
  - 1 GTY link for TCDS support between FPGAs
  - 6 LVDS pairs between the FPGA sites.
  - 5 LVDS pairs plus 2 single-ended wires from each FPGA site to front panel HDMI-style connectors. For diagnostics or unforeseen I/O needs.
  - 4 LVDS pairs plus 2 single-ended wires from each FPGA site to a 20-pin 1-mm pitch header on the bottom side of the board.
- The MCU and the FPGAs have independent JTAG chains. The FPGA JTAG chain can be accessed from the SM or from the front panel. The MCU JTAG only has front panel access. The MCU code can be changed from an SM serial port.
- The recovered TCDS clock is only available from the primary FPGA.

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APOLLO CM v3		
Title: 1.02: BLOCK DIAGRAM		
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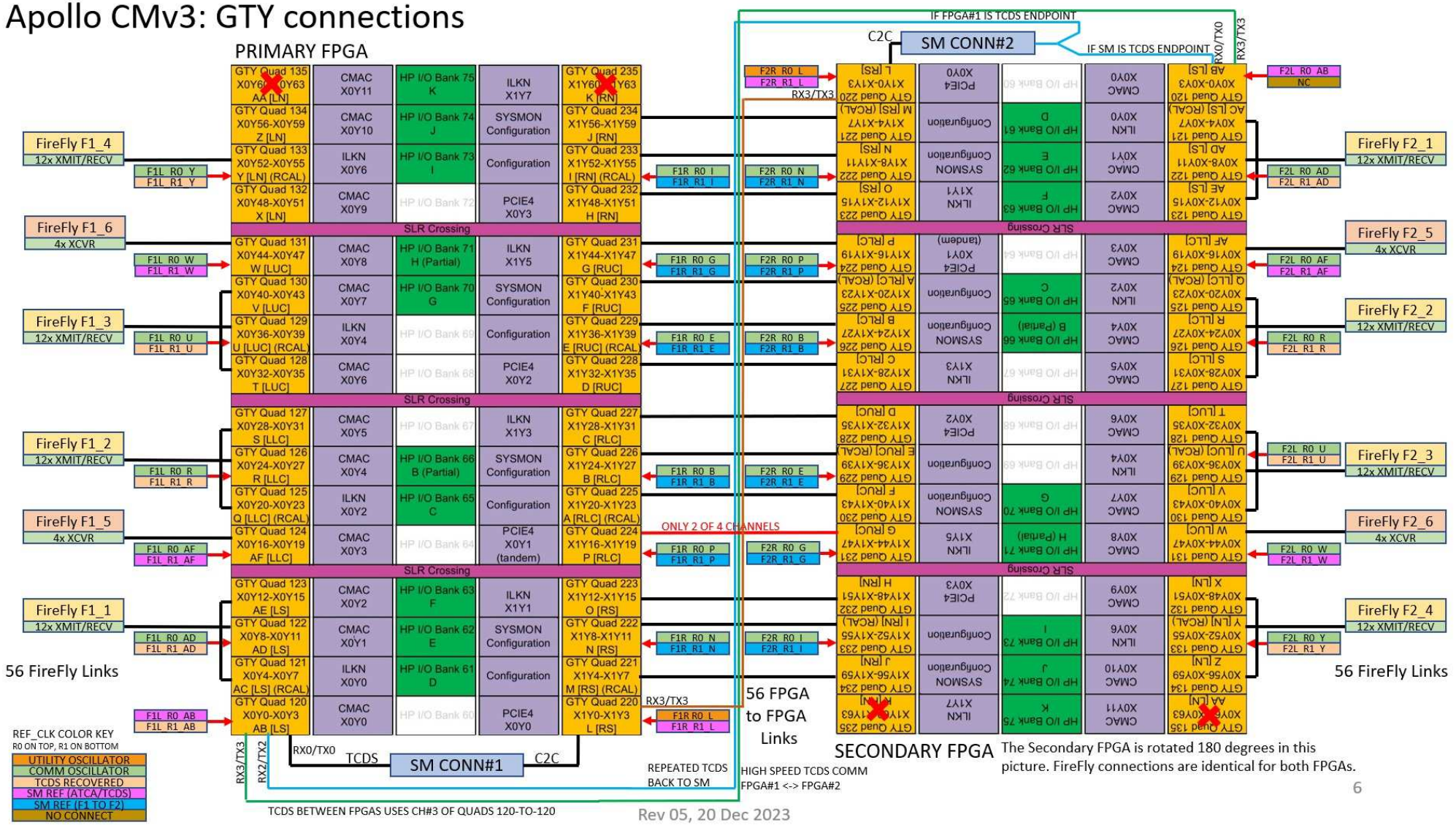
Apollo CMv3: GTY connections



APOLLO CM v3			
Title: 1.03: GTY CONNECTIONS			
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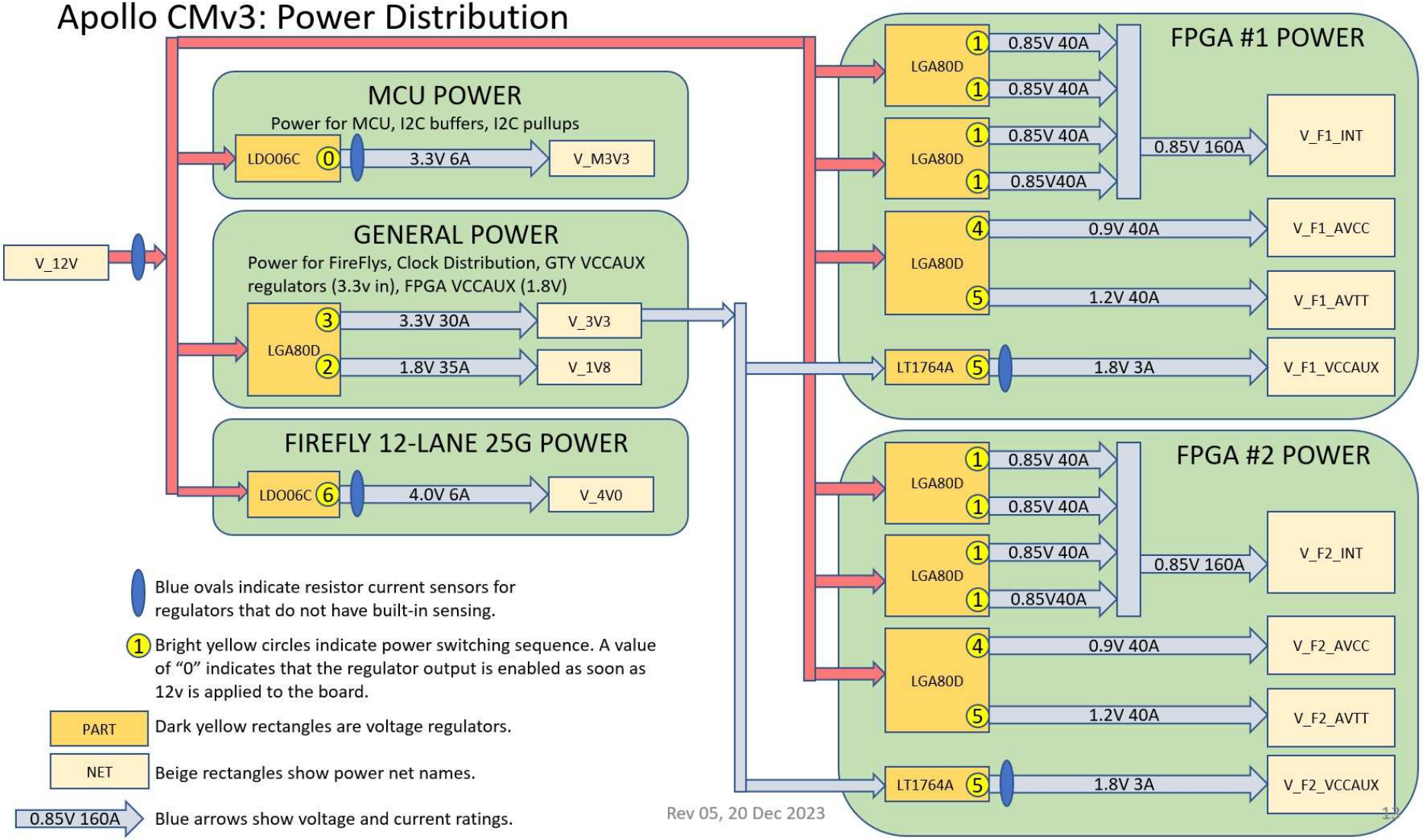
Apollo CMv3: Power Distribution



Blue ovals indicate resistor current sensors for regulators that do not have built-in sensing.

(1) Bright yellow circles indicate power switching sequence. A value of "0" indicates that the regulator output is enabled as soon as 12v is applied to the board.

PART — Dark yellow rectangles are voltage regulators.

NET — Beige rectangles show power net names.

0.85V 160A — Blue arrows show voltage and current ratings.

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APOLLO CM v3		
Title: 1.04: POWER		
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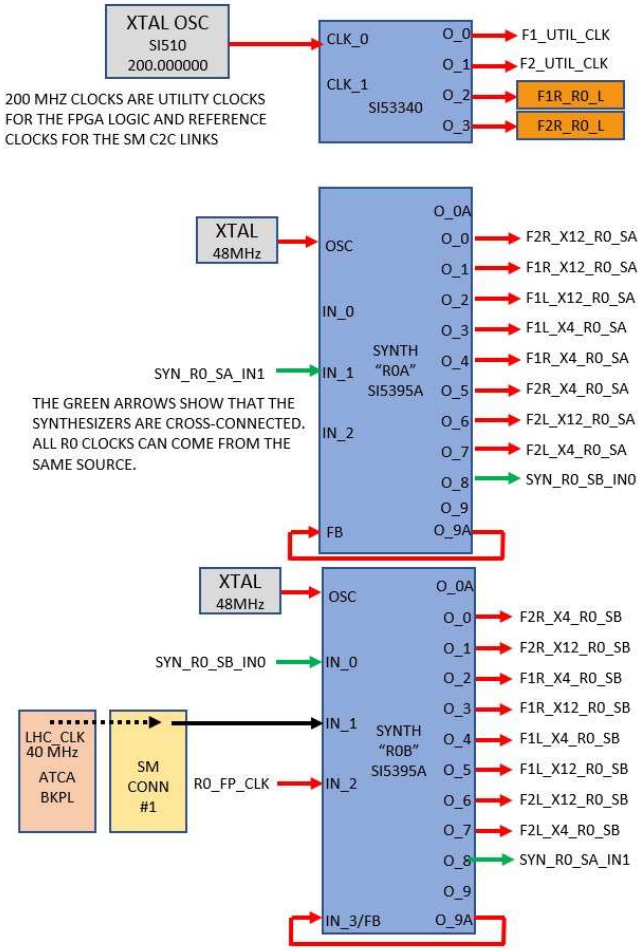
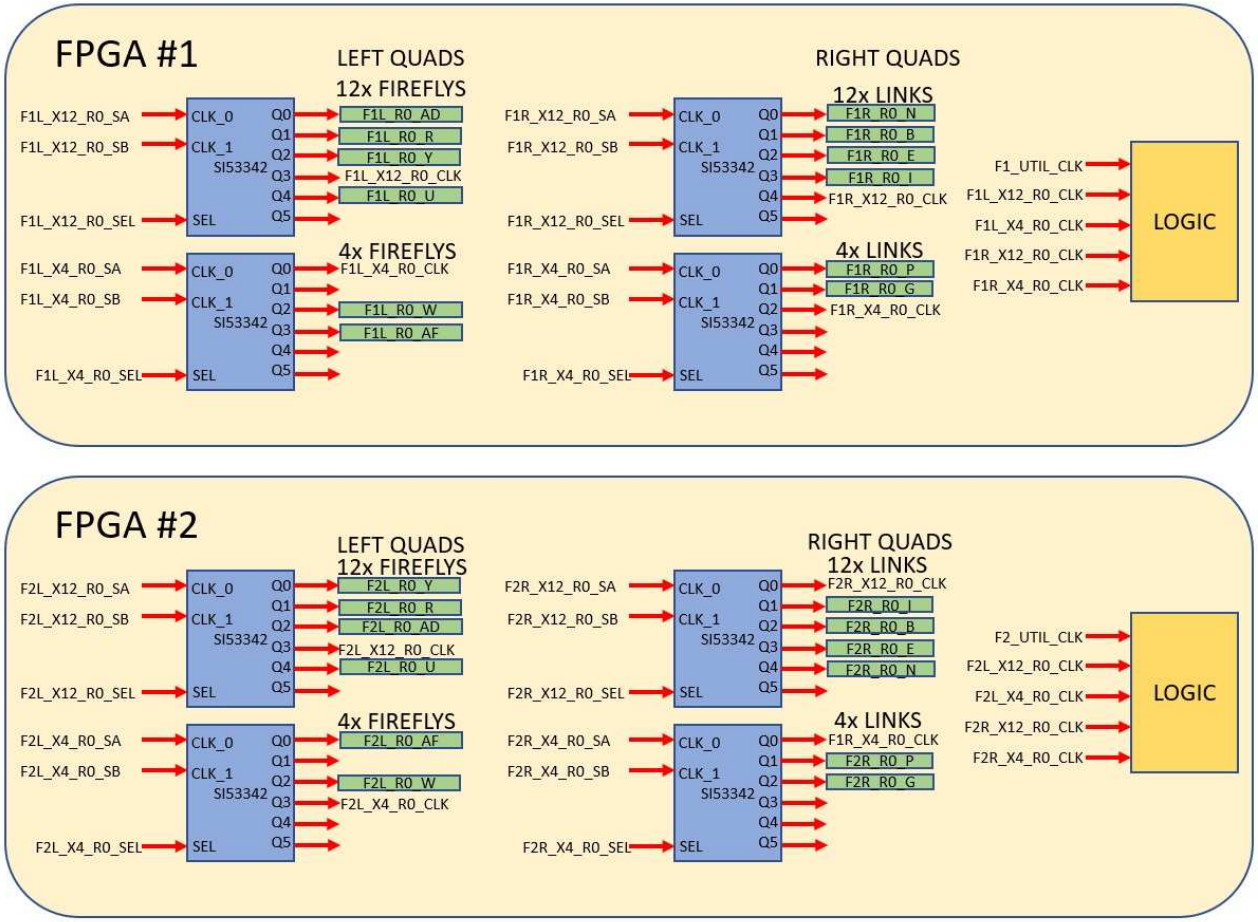
Apollo CMv3: Utility Clock / Reference Clock 0 (R0) Distribution





Rev 05, 20 Dec 2023

APOLLO CM v3		
Title: 1.05: R0 SYNTH CLOCKS		
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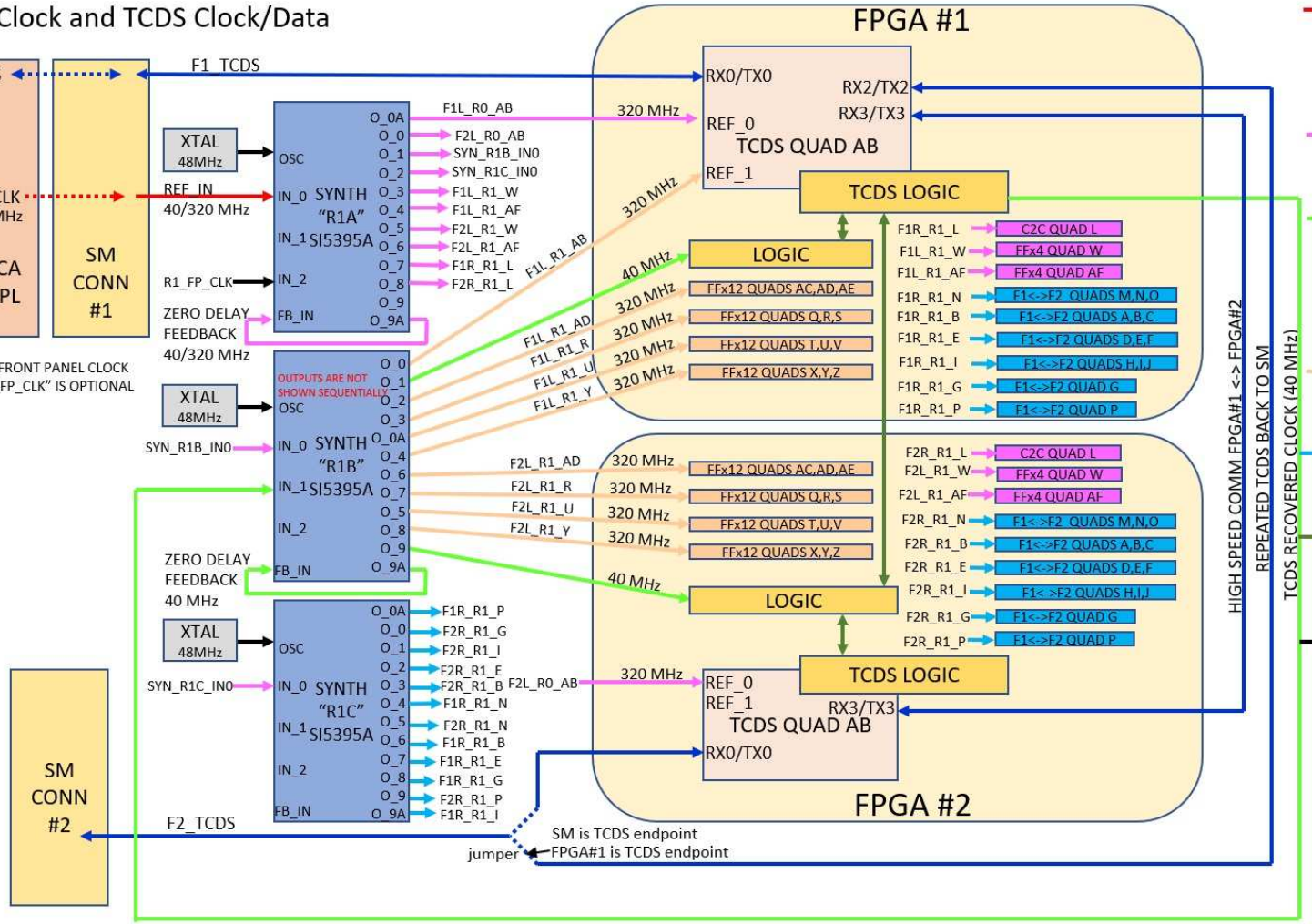
Apollo CMv3: External Clock Sources

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

LHC REFERENCE CLOCK

If the SM is not the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane. If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal. In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK

If the top synthesizer is using the clock on "IN_0", then these 320 MHz clocks all have zero phase offset relative to the incoming LHC REFERENCE CLOCK signal.

40 MHz TCDS RECOVERED CLOCK

This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK

These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

FPGA TO FPGA R1 CLOCK

These clocks drive the R1 reference for the FPGA quads that connect to the other FPGA. The frequency follows the 320 MHz REF CLOCK.

TTC/TTS DATA/CONTROL

These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

OTHER CLOCKS

These include the 40 MHz LHC clock and the outputs of various crystal oscillators. These can be used for testing or for adding flexibility to the synthesizer outputs.

GTY QUADS

FFx12 QUADS	12-lane FireFlys. For the IT-DTC, these will be detector facing.
FFx4 QUADS	4-lane FireFlys.
F1<->F2 QUADS	Connections between the two FPGAs.
TCDS QUAD	Dedicated for TCDS function.

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APOLLO CM v3		
Title: 1.06: R1 SYNTH CLOCKS		
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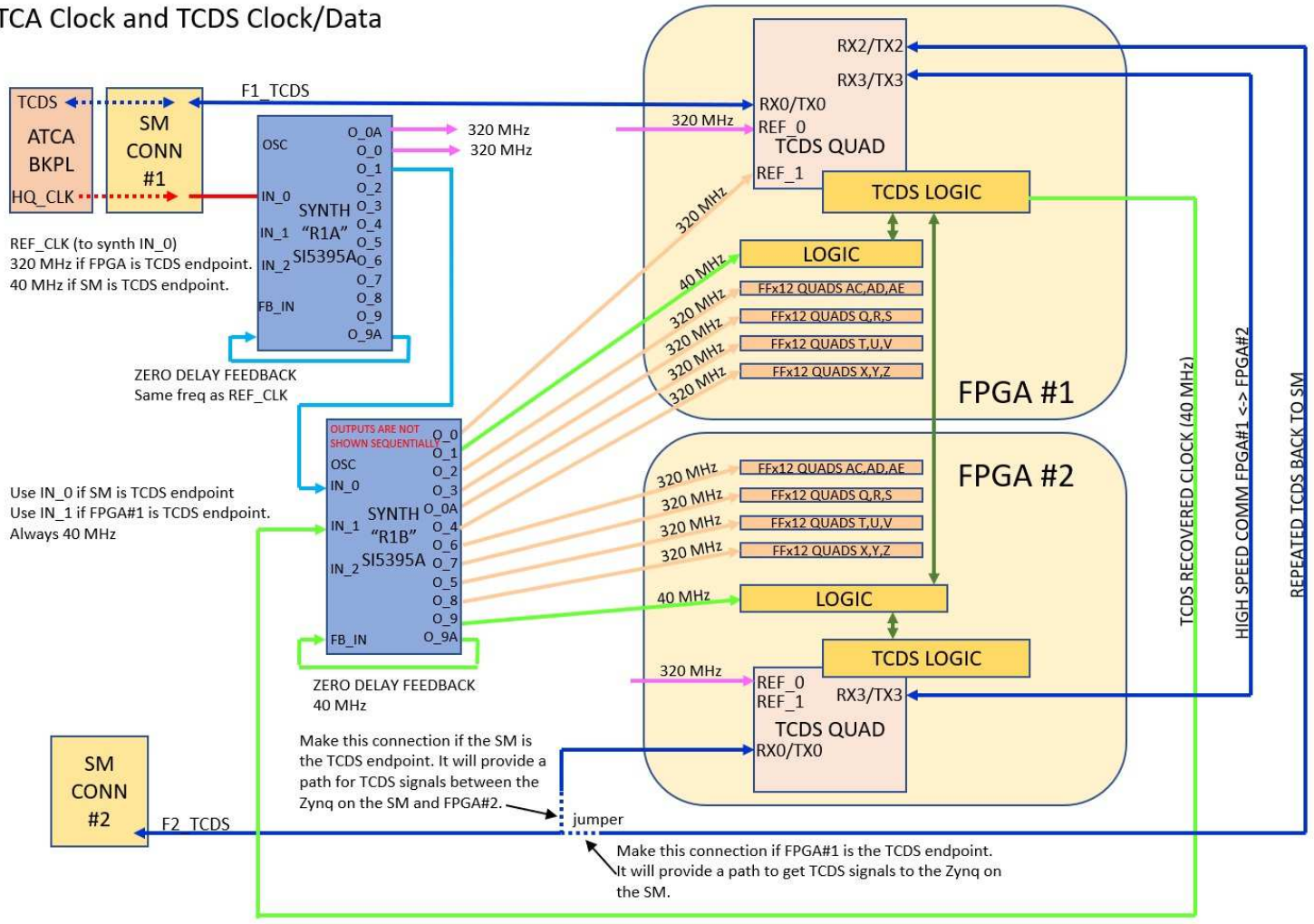
Apollo CMv3: TCDS Simplified

ATCA Clock and TCDS Clock/Data



GBIT CLOCK/DATA COMBINED

REFERENCE CLOCK
If FPGA#1 is the TCDS endpoint, then this is a 320 MHz clock passed directly from the ATCA backplane.
If the SM is the TCDS endpoint, then this is the 40 MHz clock recovered from the backplane TCDS signal.
In either case, the frequency of this clock changes when the LHC is ramping.

320 MHz REF CLOCK
These 320 MHz clocks all have zero phase offset relative to the incoming REFERENCE _CLOCK signal.

40 MHz TCDS RECOVERED CLOCK
This clock is recovered from the incoming TCDS signal. The TCDS LOGIC synchronizes this clock to the bunch crossing. It also adjusts the phase to compensate for distribution delay changes. It will always maintain a fixed phase relative to the bunch crossing. The frequency also varies during filling. This clock is made available to the logic in the FPGAs for synchronizing operations.

320 MHz TCDS RECOVERED CLOCK
These clocks drive the detector-facing FireFly devices, as well as the quad that sends the outgoing TCDS signal back to the SM. They track the TCDS RECOVERED CLOCK.

TTC/TTS DATA/CONTROL
These signals contain clocks/data/control extracted from the incoming TCDS signal (TTC) or destined for the outgoing TCDS signal (TTS). They are used within each FPGA, and can also pass from one FPGA to the other.

GTY QUADS

FFx12 QUADS — 12-lane FireFlys. For the IT-DTC, these will be detector facing.

TCDS QUAD — Dedicated for TCDS function.

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APOLLO CM v3		
Title: 1.07: TCDS SIMPLIFIED		
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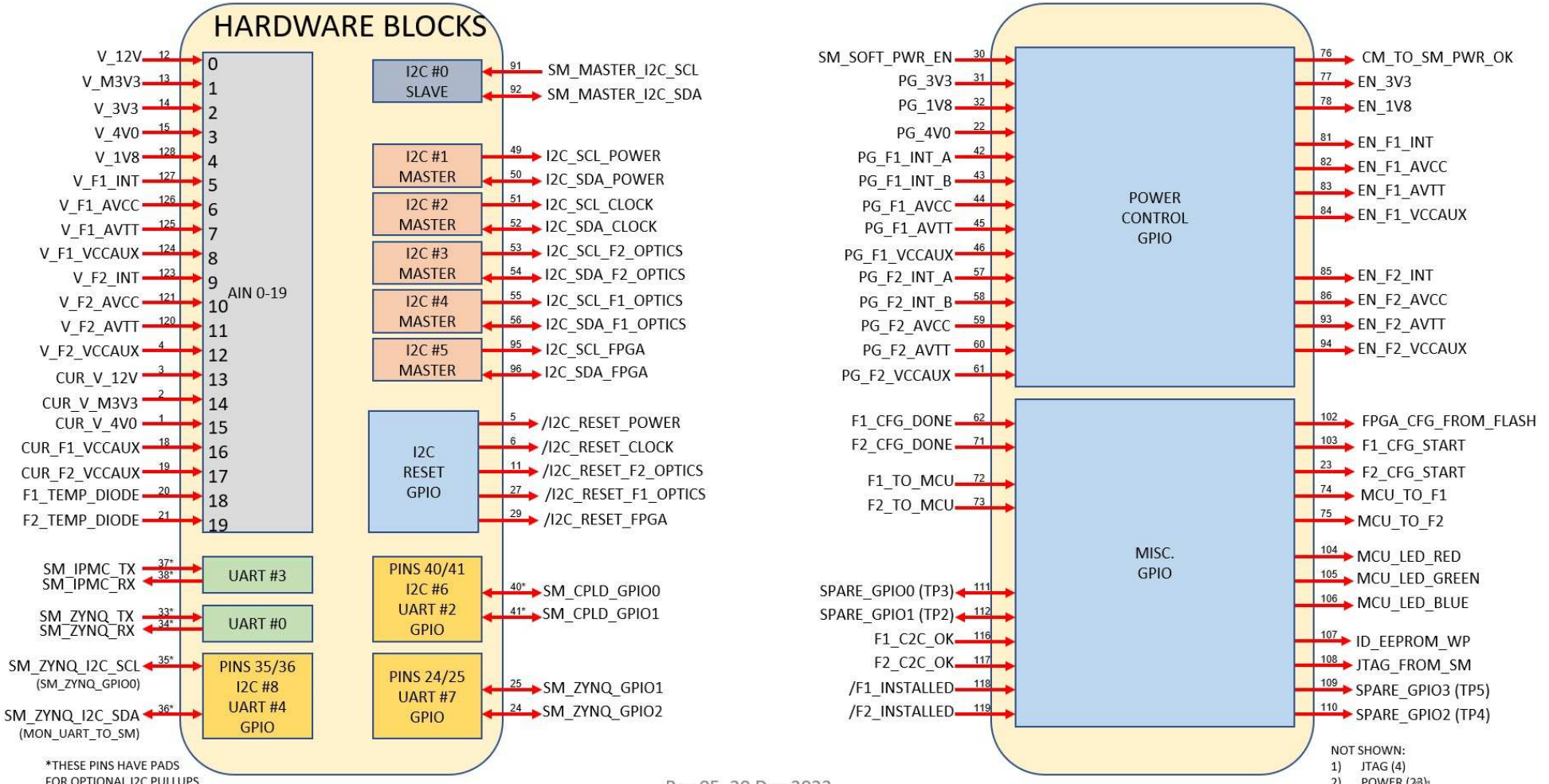
Apollo CMv3: MCU Connections and Internal Resources



Rev 05, 20 Dec 2023

APOLLO CM v3		
Title: 1.08: MCU I/O AND INTERNALS		
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2.01: SM POWER AND CONTROL CONNECTOR

THE "POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE MCU HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

POWER OK LED

THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 1 MILLIOHMS AND A CURRENT OF 30 AMPS WILL PRODUCE A VOLTAGE OF 30 MILLIVOLTS. THE SENSE AMPLIFIER HAS A GAIN OF 100, YIELDING 3.0 VOLTS AT 30 AMPS. THIS EQUALS 360 WATTS.

THIS DIVIDER FOLLOWING THE AMPLIFIER ALLOWS THE AMPLIFIER OUTPUT TO EXCEED THE 2.5 VOLT FULL-SCALE INPUT LIMIT OF THE MCU. WITH Rtop=2K AND Rbottom=10K, THE SCALE FACTOR NEEDED IN THE MCU IS 12.5 AMPS PER VOLT AND THE MAXIMUM CURRENT BEFORE SATURATION IS 30 AMPS (360 WATTS).

V_12V
R = 0.001 OHM
GAIN = 100 V/V
DIVIDER = 83%
SCALE = 12.5 AMPS PER VOLT

I2C0 IS A SLAVE INTERFACE. IT IS CONNECTED TO THE IPMC ON THE SM.

I2C8 CAN BE A MASTER OR A SLAVE. IT IS USED TO GET MONITORING DATA INTO THE ZYNQ. ON CMv1, THIS IS THE UART#4 PATH. IT IS CONNECTED TO THE ZYNQ ON THE SM.

I2C6 IS AVAILABLE FOR FUTURE USE. IT IS CONNECTED TO THE CPLD ON THE SM. PULLUPS ARE NOT INSTALLED.

THE I2C7 PINS ARE INITIALLY USED FOR UART#3 CONNECTIONS TO THE IPMC ON THE SM. PULLUPS ARE NOT INSTALLED.

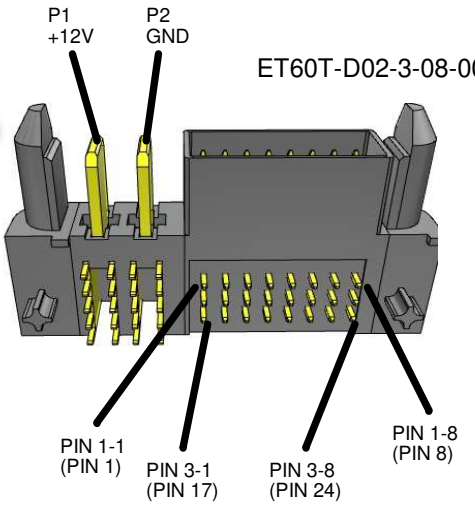
THE I2C9 PINS ARE INITIALLY USED FOR UART#0 CONNECTIONS TO THE ZYNQ ON THE SM.THIS PROVIDES A BOOTLOADER FUNCTION FOR THE MCU. PULLUPS ARE NOT INSTALLED.

IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH. IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

TM4C SLAVE I2C ADDR = 0X40

TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.

FOR STANDALONE USB-TO-UART CONNECTION, USE DIGIKEY 768-1015 (FTDI TTL-232R-3V3). CONNECT IT TO AN ADAPTER THAT PLUGS INTO CONNECTOR P1. USE PIN 5 (SM_ZYNQ_TX) AND PIN 21 (SM_ZYNG_RX).



ZERO-OHM RESISTORS ON PIN 4 AND PIN 20 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES.

THE SAME IS TRUE FOR THE RESISTORS ON PIN 5 AND PIN 21.

IN ROW 2, PINS 1, 4, 6, AND 8 ARE "GND" ON SMv1. A CMv3 BOARD MUST BE ABLE TO TOLERATE A HARD GND CONNECTION ON THESE PINS IN CASE IT IS CONNECTED TO AN SMv1.

IF THE MCU IS DRIVING AN OUTPUT HIGH, AND THE SIGNAL IS SHORTED TO GND, A 270 OHM RESISTOR WILL LIMIT THE CURRENT TO 12 MA. THE RESISTOR POWER WILL BE 0.04 WATTS.

APOLLO CM v3		
Title: 2.01: SM POWER AND CONTROL CONNECTOR		
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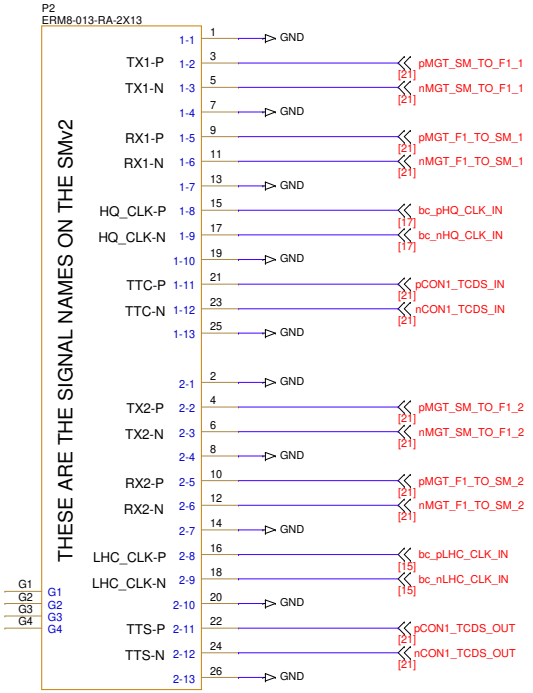
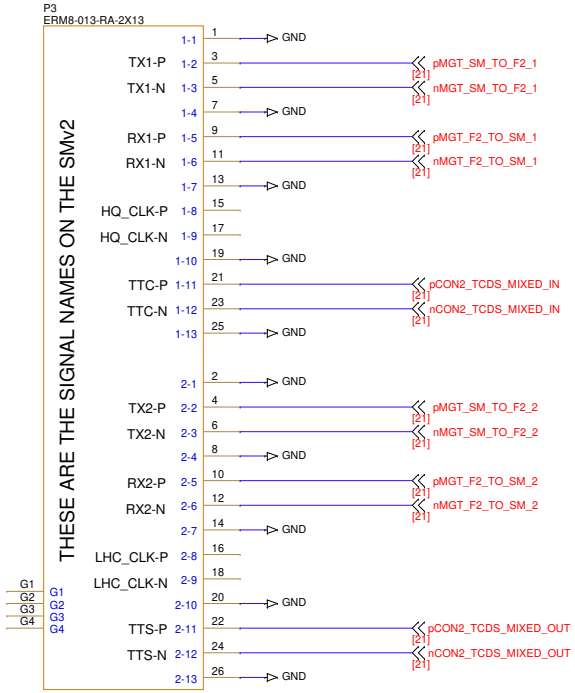
THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. AC COUPLING CAPACITORS ARE ASSUMED TO BE ON THE SM.

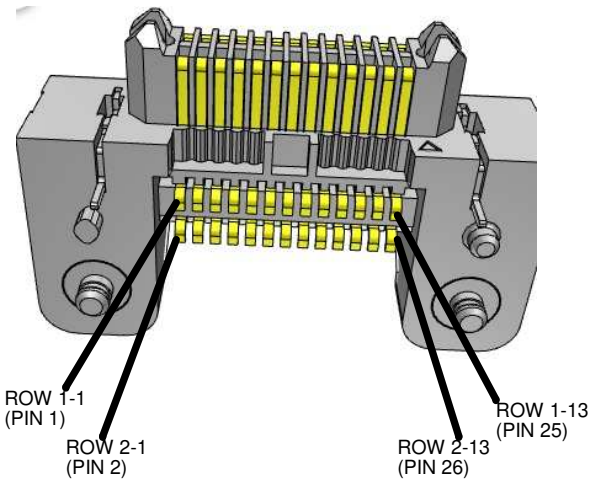
FPGA#1 AND BACKPLANE CLOCK SIGNALS



FPGA#2 SIGNALS



THE TCDS SIGNALS ON HIGH SPEED CONNECTOR #2 ARE LABELED "MIXED" BECAUSE THEY CAN EITHER BE REGULAR TCDS SIGNALS WHEN THE SM IS THE TCDS ENDPOINT, OR THEY CAN BE REPEATED TCDS SIGNALS WHEN FPGA#1 IS THE TCDS ENDPOINT.



ERM8-013-01-L-D-RA-DS

APOLLO CM v3		
Title: 2.02: SM HIGH SPEED CONNECTORS		
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2.03: MCU AND FPGA JTAG

THE FPGA JTAG REFERENCE IS 3.3 VOLTS.

J1 CON_2X7_RA

FP_JTAG_TMS
FP_JTAG_TCK
FP_JTAG_TDO
FP_JTAG_TDI

FRONT PANEL FPGA JTAG

SM_JTAG_TMS [9] — SM JTAG — R67 10K 0603 — V_M3V3

FP_JTAG_TMS — FP JTAG — R81 10K 0603 — V_M3V3

SM_JTAG_TCK [9] — SM JTAG — R91 10K 0603 — V_M3V3

FP_JTAG_TCK — FP JTAG — R99 10K 0603 — V_M3V3

SM_JTAG_TDI [9] — SM JTAG — R105 10K 0603 — V_M3V3

FP_JTAG_TDI — FP JTAG — R113 10K 0603 — V_M3V3

U60 74LVC1G126 — R69 33 0603 — F1_TMS
U51 74LVC1G126 — R66 33 0603 — F2_TMS
U62 74LVC1G125 — R83 33 0603
U61 74LVC1G125 — R79 33 0603
U65 74LVC1G126 — R94 33 0603 — F1_TCK
U64 74LVC1G126 — R89 33 0603 — F2_TCK
U71 74LVC1G125 — R101 33 0603
U69 74LVC1G125 — R97 33 0603
U74 74LVC1G126 — R107 33 0603
U76 74LVC1G125 — R114 33 0603 — F1_TDI

U79 74LVC1G125 — V_1V8 — GND

IF "JTAG_FROM_SM" IS ASSERTED, THE FPGA JTAG CHAIN WILL BE DRIVEN BY SIGNALS FROM THE SM. IF IT IS NEGATED, THE FPGA JTAG CHAIN WILL DE DRIVEN FROM THE FRONT PANEL CONNECTOR.

JTAG_FROM_SM

THE TEST POINT ON PIN 2 IS AVAILABLE FOR ADDING ANOTHER SIGNAL FROM THE SEGGER.

THE MCU HAS INTERNAL PULLUPS ENABLED ON ALL FOUR JTAG SIGNALS. REFER TO SECTION 4.3.1 OF THE TM4C1290NCPDT MANUAL.

THE MCU CONNECTOR ON THE FRONT PANEL IS A 10-PIN 50-MIL PITCH CONNECTOR. A SEGGER MODEL 8.06.28 "50-MIL 10-PIN PATCH ADAPTER" IS USED AT THE PROGRAMMER.

THE MCU JTAG REFERENCE IS 3.3 VOLTS.

J2 CON10A — TP1

FP_MCU_TMS
FP_MCU_TCK
FP_MCU_TDO
FP_MCU_TDI

U70-1 TM4C1290NCPDT_NEW

JTAG_TMS — PN1 — 108
JTAG_TCK — PN3 — 110 — SPARE_GPIO2 — TP4
JTAG_TDO — PN2 — 109 — SPARE_GPIO3 — TP5
JTAG_TDI — 98

THE TEST POINTS ON PINS 109 AND 110 ARE AVAILABLE FOR DEBUGGING OR MEETING NEW REQUIREMENTS.

FRONT PANEL MCU JTAG

THE MCU CAN BE RUN IN "JTAG" MODE OR "ARM SWD" MODE.

U80 74AUP1T34 — R123 33 0603 — FP_JTAG_TDO — FP JTAG
U81 74AUP1T34 — R124 33 0603 — SM_JTAG_TDO [9] — SM JTAG

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE SM OR THE EXTERNAL PROGRAMMER.

FPGA#2 JTAG BYPASS

BYPASS — R120 DNP 0603 — C897 0 0402 — IN CHAIN

IF THE FPGA IS INSTALLED AND PART OF THE JTAG CHAIN, INSTALL 0.0 OHM AT "IN CHAIN" SITE, AND OMIT 0.0 OHM AT "BYPASS" SITE.

IF THE FPGA IS NOT INSTALLED, INSTALL 0.0 OHM AT "BYPASS" SITE, AND OMIT 0.0 OHM AT "IN CHAIN" SITE.

U78-8 FPGA_VU13P_A2577 JTAG

F2_TDO AG14 — TDO_0
F2_TDI AH13 — TDI_0
F2_TMS AE14 — TMS_0
F2_TCK AF13 — TCK_0

FPGA#2

F2_TDI

FPGA#1 JTAG BYPASS

BYPASS — R117 DNP 0603 — C904 0 0402 — IN CHAIN

U77-8 FPGA_VU13P_A2577 JTAG

F1_TDO AG14 — TDO_0
F1_TDI AH13 — TDI_0
F1_TMS AE14 — TMS_0
F1_TCK AF13 — TCK_0

FPGA#1

V_1V8: C902 0.1 UF 0402, C914 0.1 UF 0402, C932 0.1 UF 0402, C944 0.1 UF 0402 — GND

V_1V8: C939 0.1 UF 0402, C956 0.1 UF 0402, C951 0.1 UF 0402, C969 0.1 UF 0402, C974 0.1 UF 0402, C986 0.1 UF 0402, C999 0.1 UF 0402 — GND

V_M3V3: C889 0.1 UF 0402, C884 0.1 UF 0402 — GND

APOLLO CM v3		
Title: 2.03: MCU AND FPGA JTAG		
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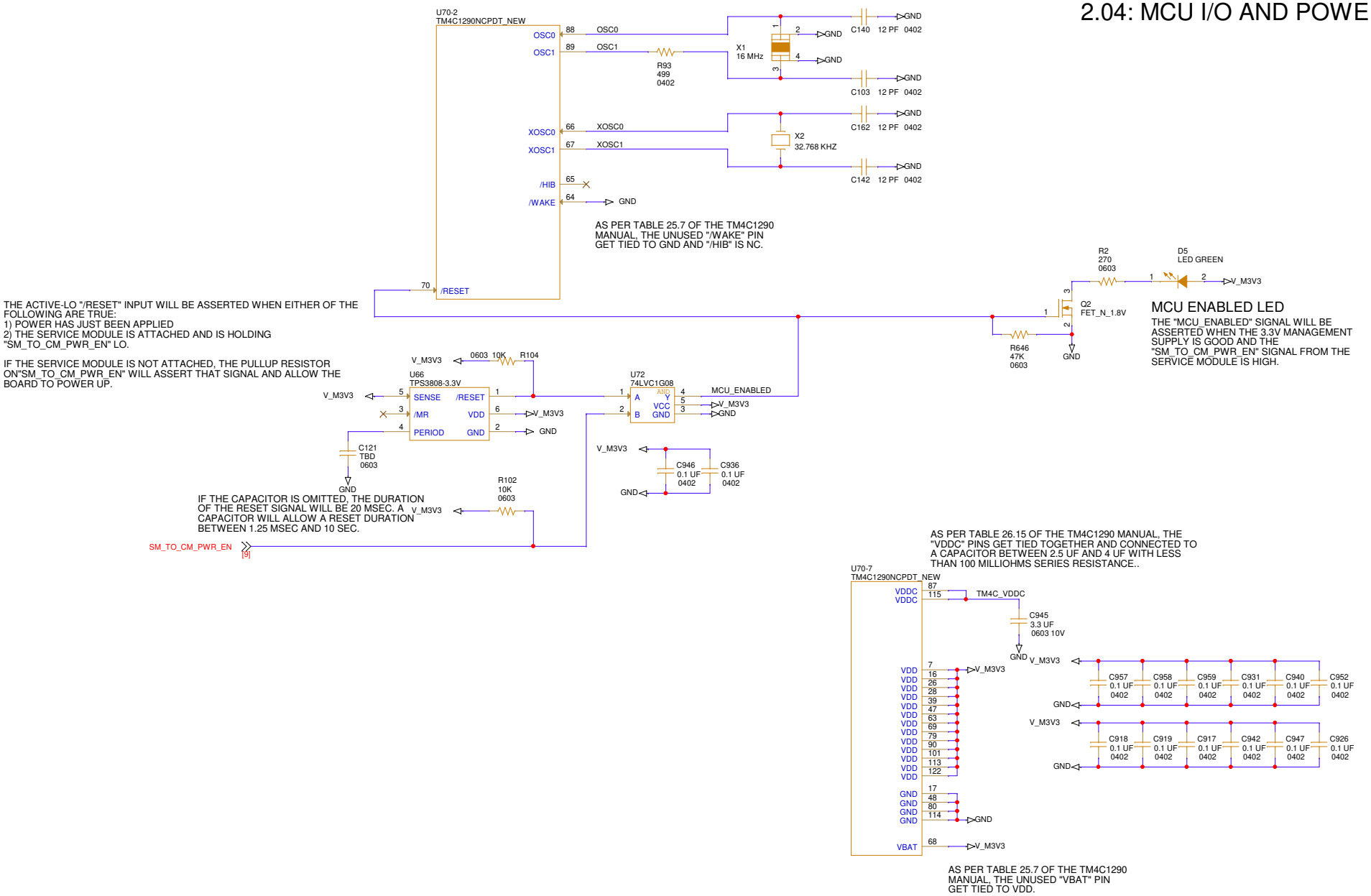
2.04: MCU I/O AND POWER



APOLLO CM v3		
Title: 2.04: MCU I/O AND POWER		
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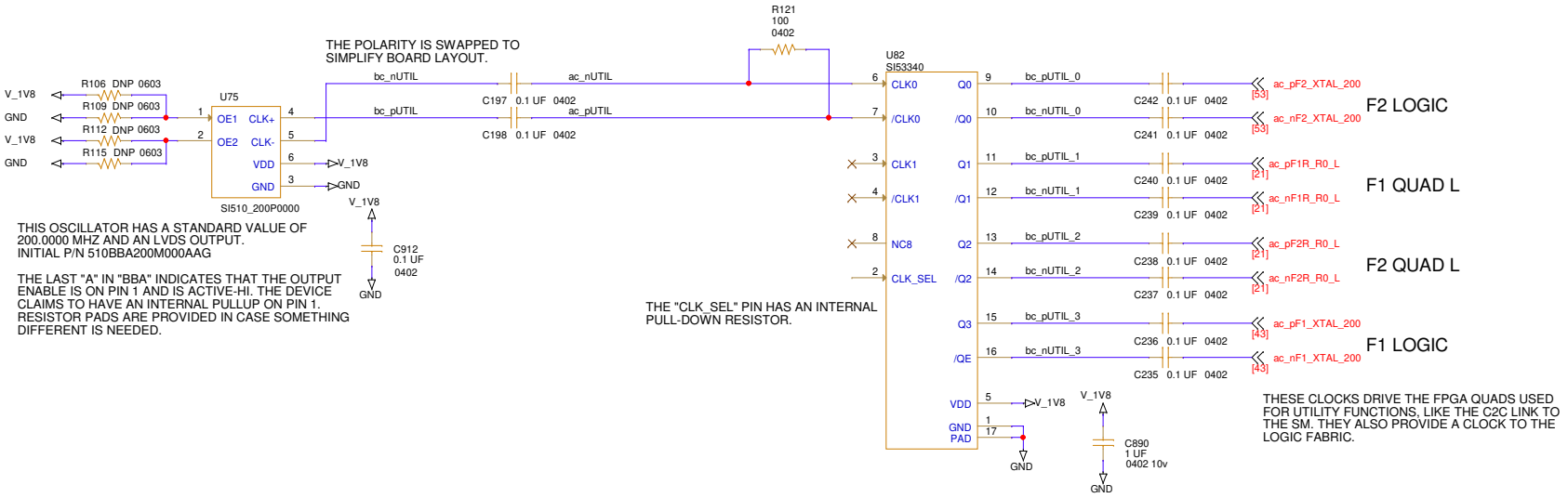
2.05: UTILITY CLOCK



THIS OSCILLATOR HAS A STANDARD VALUE OF 200.0000 MHZ AND AN LVDS OUTPUT. INITIAL P/N 510BBA200M000AAG

THE LAST "A" IN "BBA" INDICATES THAT THE OUTPUT ENABLE IS ON PIN 1 AND IS ACTIVE-HI. THE DEVICE CLAIMS TO HAVE AN INTERNAL PULLUP ON PIN 1. RESISTOR PADS ARE PROVIDED IN CASE SOMETHING DIFFERENT IS NEEDED.

THE "CLK_SEL" PIN HAS AN INTERNAL PULL-DOWN RESISTOR.

THESE CLOCKS DRIVE THE FPGA QUADS USED FOR UTILITY FUNCTIONS, LIKE THE C2C LINK TO THE SM. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

APOLLO CM v3		
Title: 2.05: UTILITY CLOCK		
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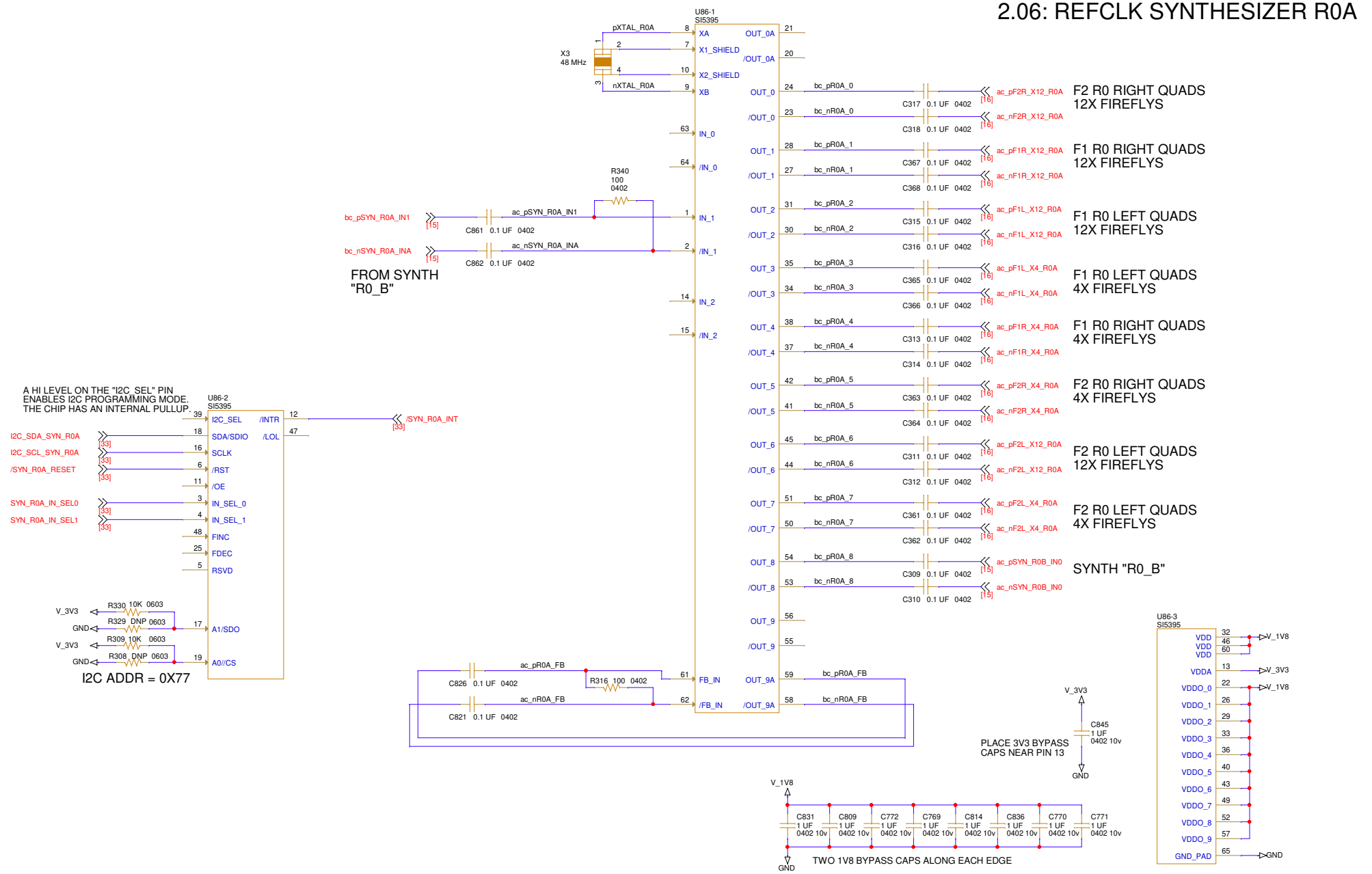
2.06: REFCLK SYNTHESIZER R0A



APOLLO CM v3		
Title: 2.06: REFCLK SYNTHESIZER R0A		
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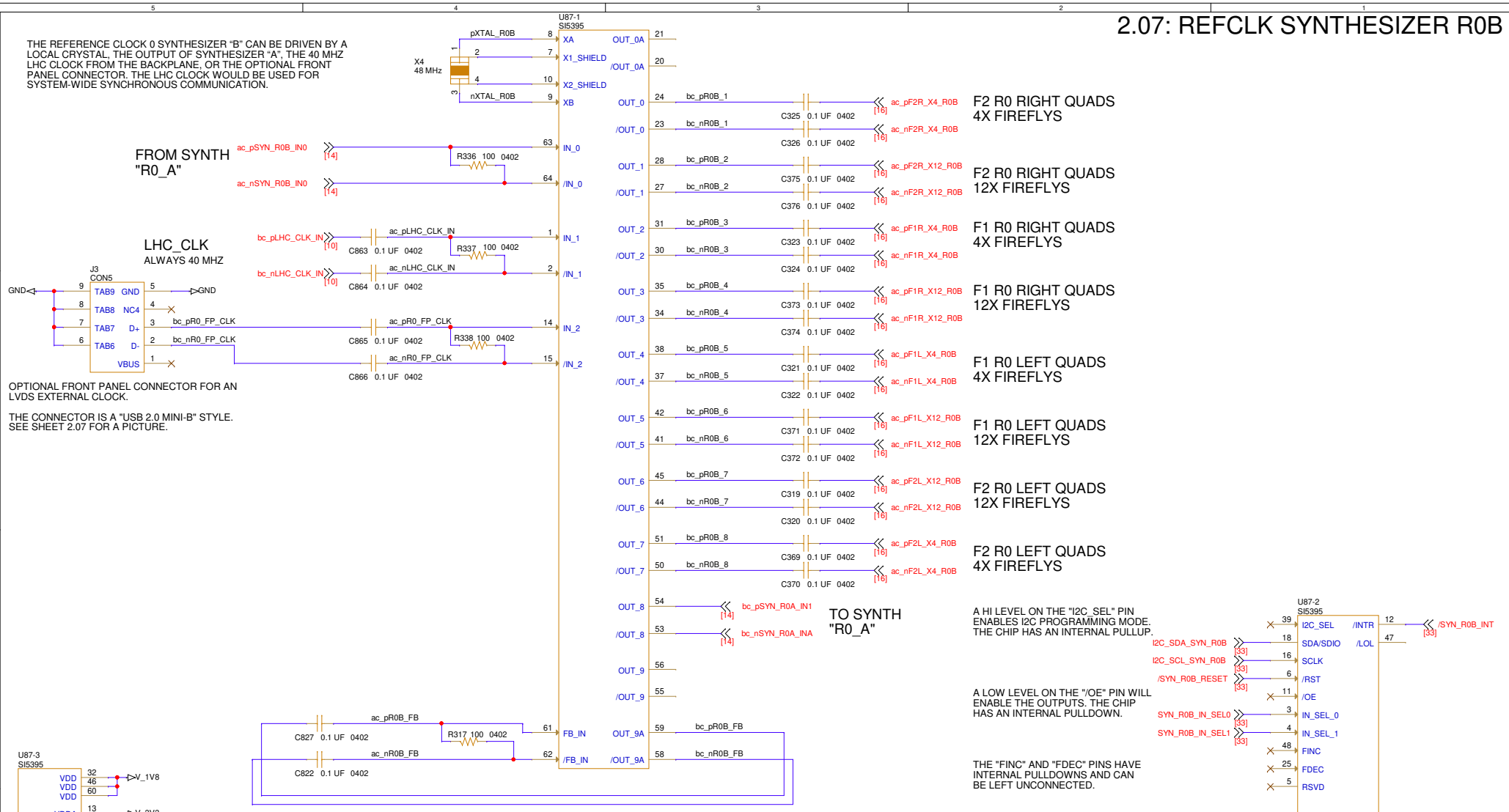
2.07: REFCLK SYNTHESIZER R0B

THE REFERENCE CLOCK 0 SYNTHESIZER "B" CAN BE DRIVEN BY A LOCAL CRYSTAL, THE OUTPUT OF SYNTHESIZER "A", THE 40 MHZ LHC CLOCK FROM THE BACKPLANE, OR THE OPTIONAL FRONT PANEL CONNECTOR. THE LHC CLOCK WOULD BE USED FOR SYSTEM-WIDE SYNCHRONOUS COMMUNICATION.



ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

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Title: 2.07: REFCLK SYNTHESIZER R0B		
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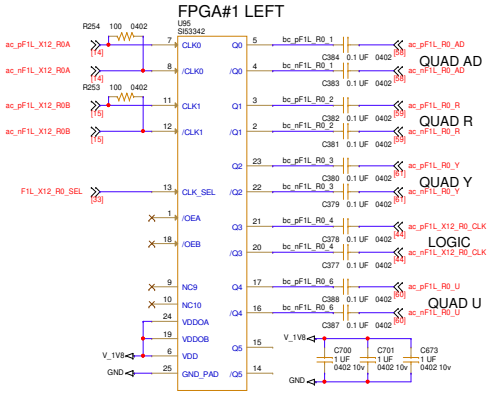
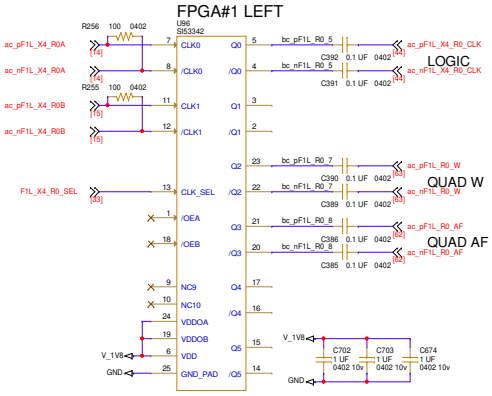
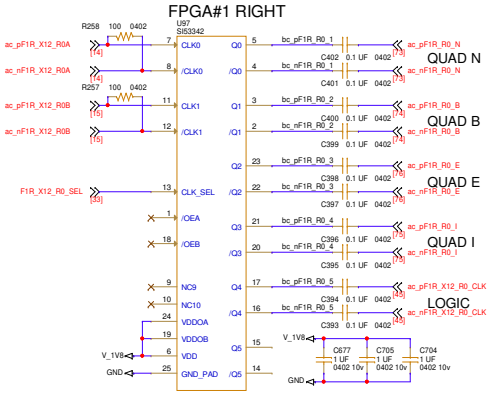
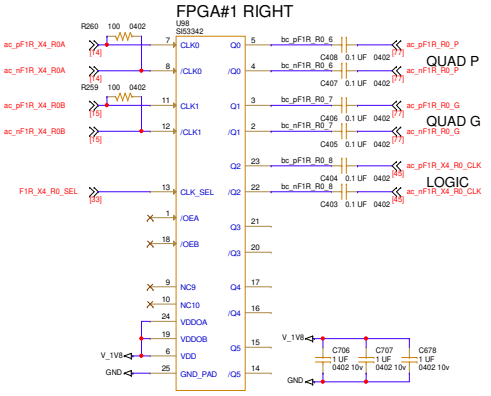
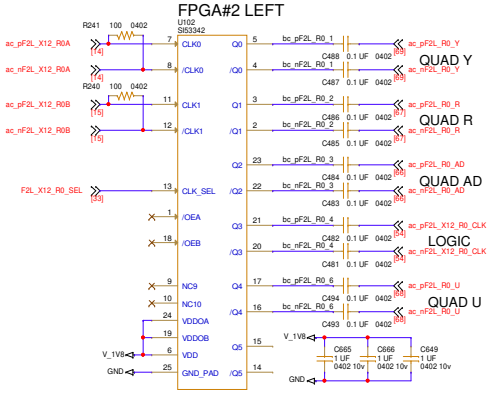
2.08: REFCLK R0 FANOUT

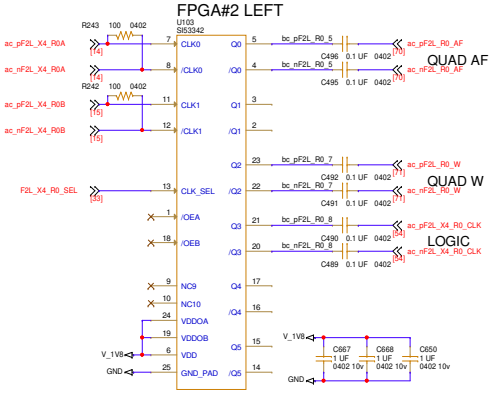


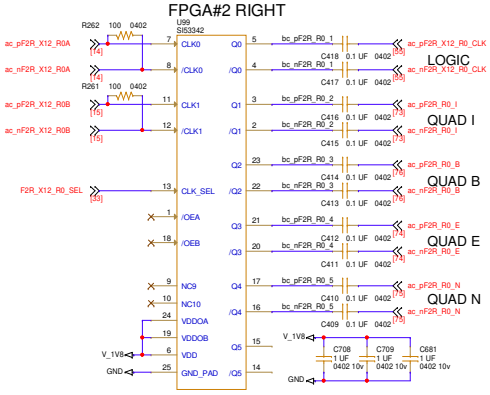


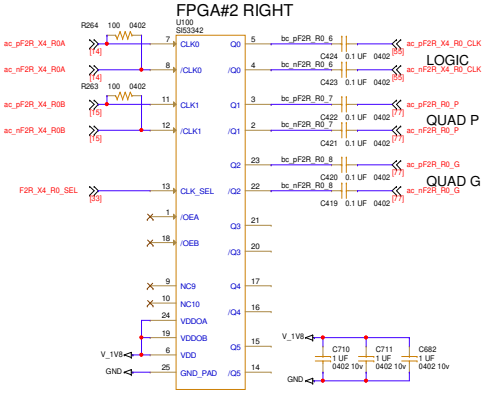












ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

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2.09: REFCLK SYNTHESIZER R1A

U91-1
SI5395

X7
48 MHz

IF THE HQ_CLK OR LHC_CLK IS AC-COUPLED ON THE SM, USE ZERO-OHM RESISTORS ON THESE CAPACITOR PADS.

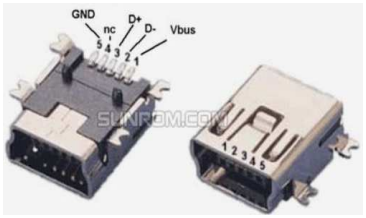
HQ_CLK

320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

J4
CON5

OPTIONAL FRONT PANEL CONNECTOR FOR AN LVDS EXTERNAL CLOCK.

THE CONNECTOR IS A "USB 2.0 MINI-B" STYLE.



F1 QUAD AB (TCDS QUAD)

F2 QUAD AB (TCDS QUAD)

SYN R1B IN0

SYN R1C IN0

F1 QUAD W

F1 QUAD AF

F2 QUAD W

F2 QUAD AF

F1 QUAD L (C2C/TCDS QUAD)

F2 QUAD L (C2C/TCDS QUAD)

ZERO-DELAY FEEDBACK
320 MHZ IF FPGA#1 IS TCDS ENDPOINT.
40 MHZ IF SM IS TCDS ENDPOINT

OUTPUTS 9 AND 9A MUST BE THE SAME FREQUENCY.

A HI LEVEL ON THE "I2C_SEL" PIN ENABLES I2C PROGRAMMING MODE. THE CHIP HAS AN INTERNAL PULLUP.

U91-2
SI5395

I2C ADDR = 0X77

U91-3
SI5395

V_3V3

V_1V8

ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM v3	
Title	2.09: REFCLK SYNTHESIZER R1A
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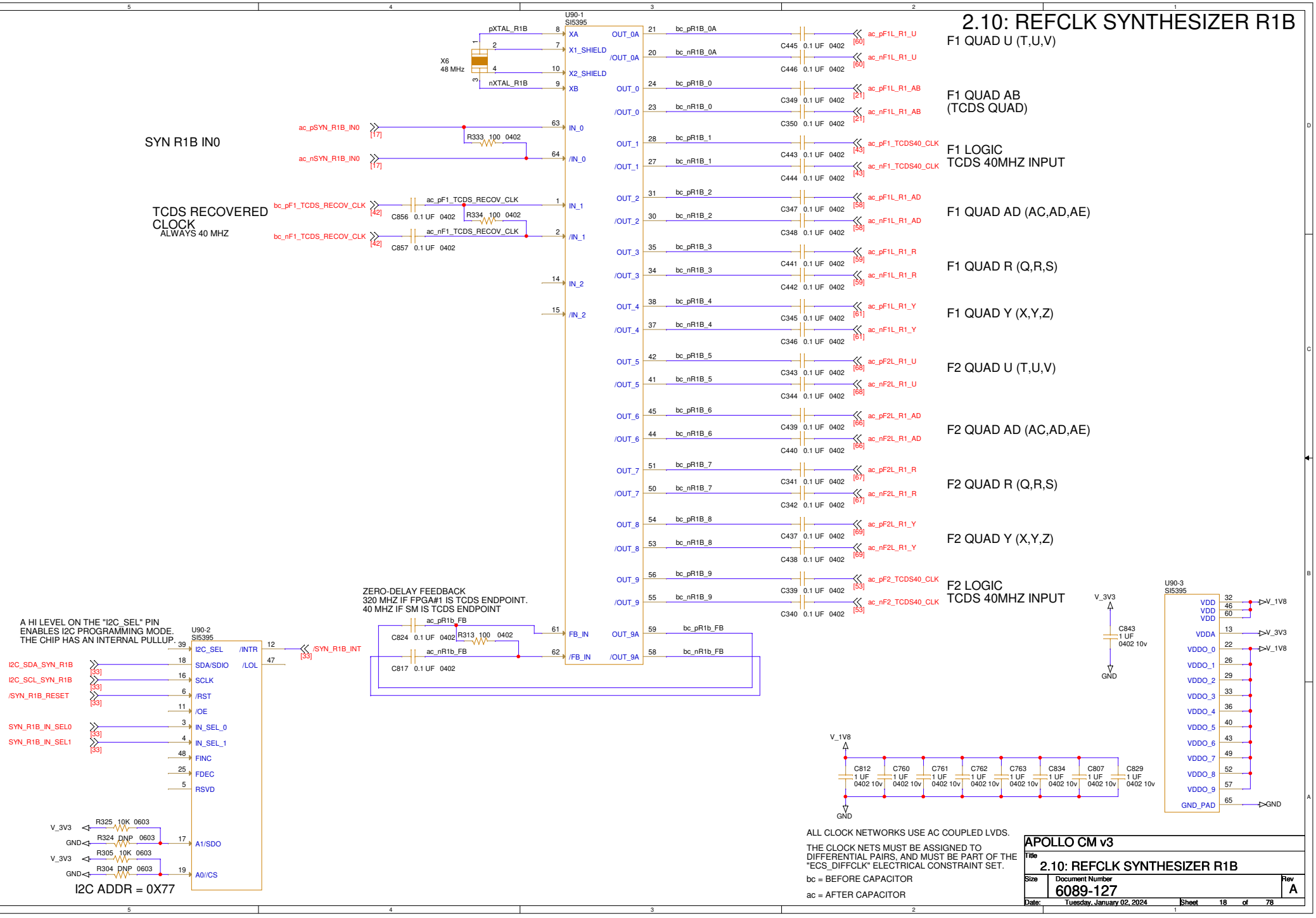
2.10: REFCLK SYNTHESIZER R1B



ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM v3			
Title: 2.10: REFCLK SYNTHESIZER R1B			
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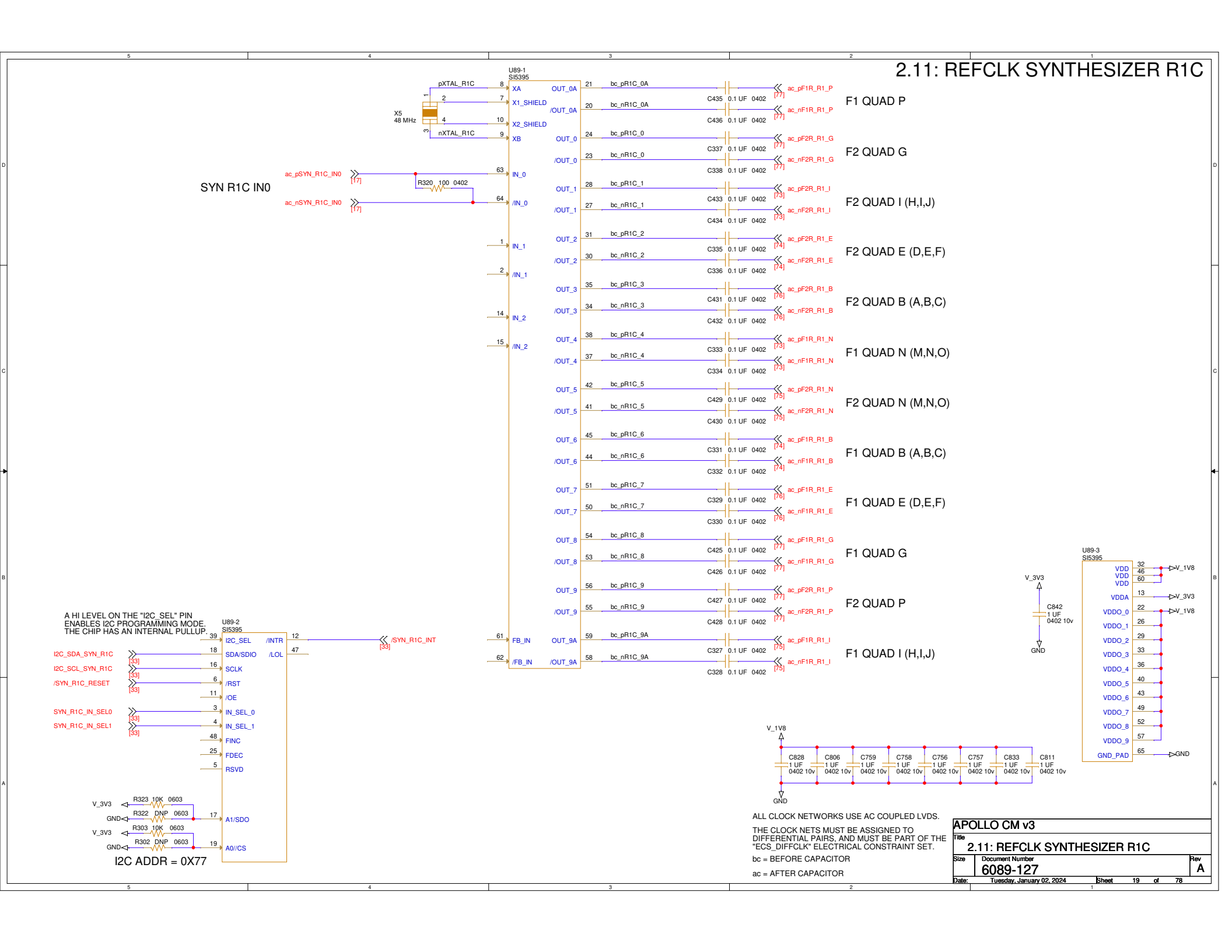
2.11: REFCLK SYNTHESIZER R1C



ALL CLOCK NETWORKS USE AC COUPLED LVDS.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

APOLLO CM v3	
Title	2.11: REFCLK SYNTHESIZER R1C
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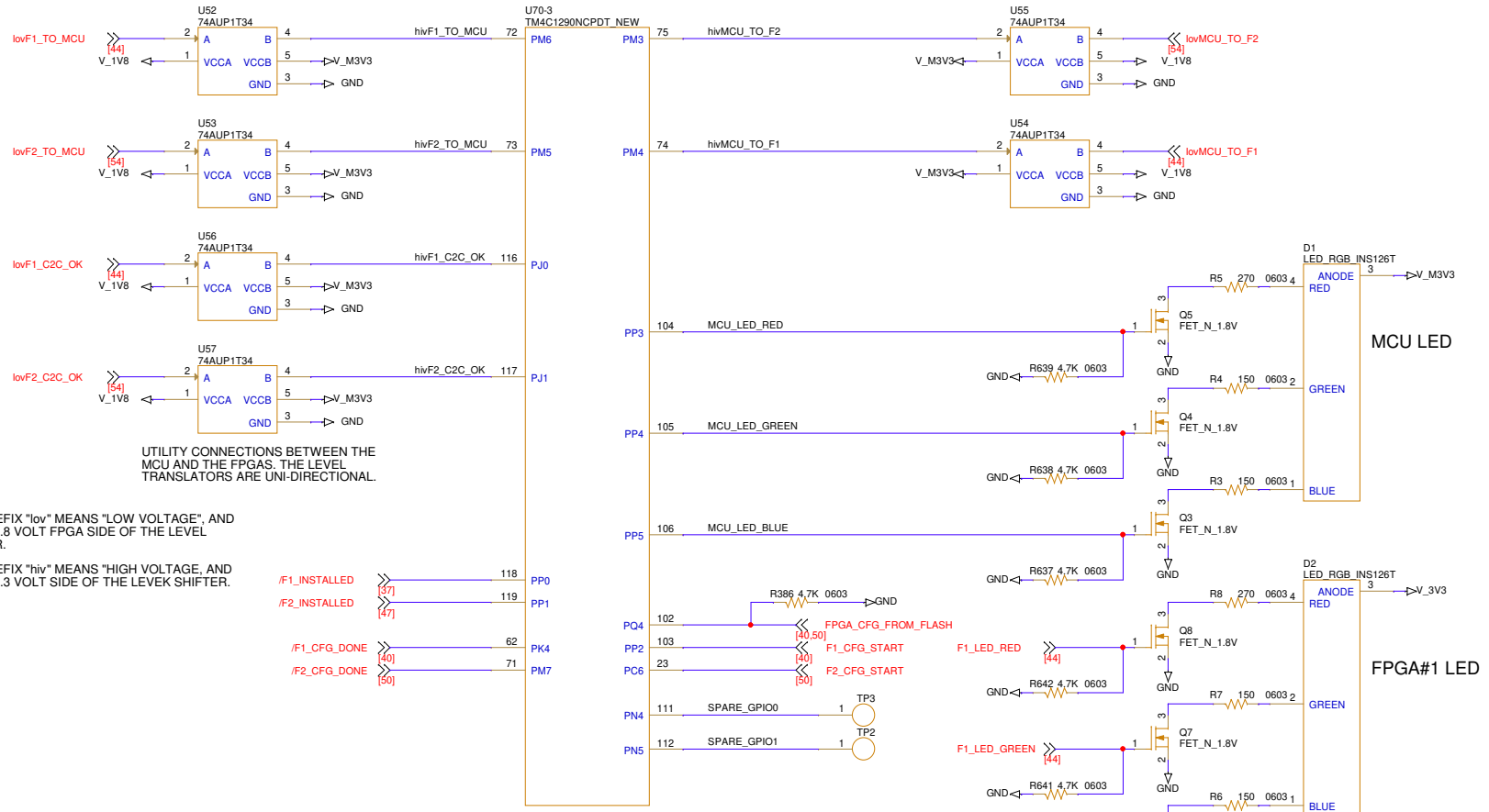
2.12: LEDS AND LEVEL SHIFTERS



APOLLO CM v3		
Title: 2.12: LEDS AND LEVEL SHIFTERS		
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2.13: C2C AND TCDS QUADS

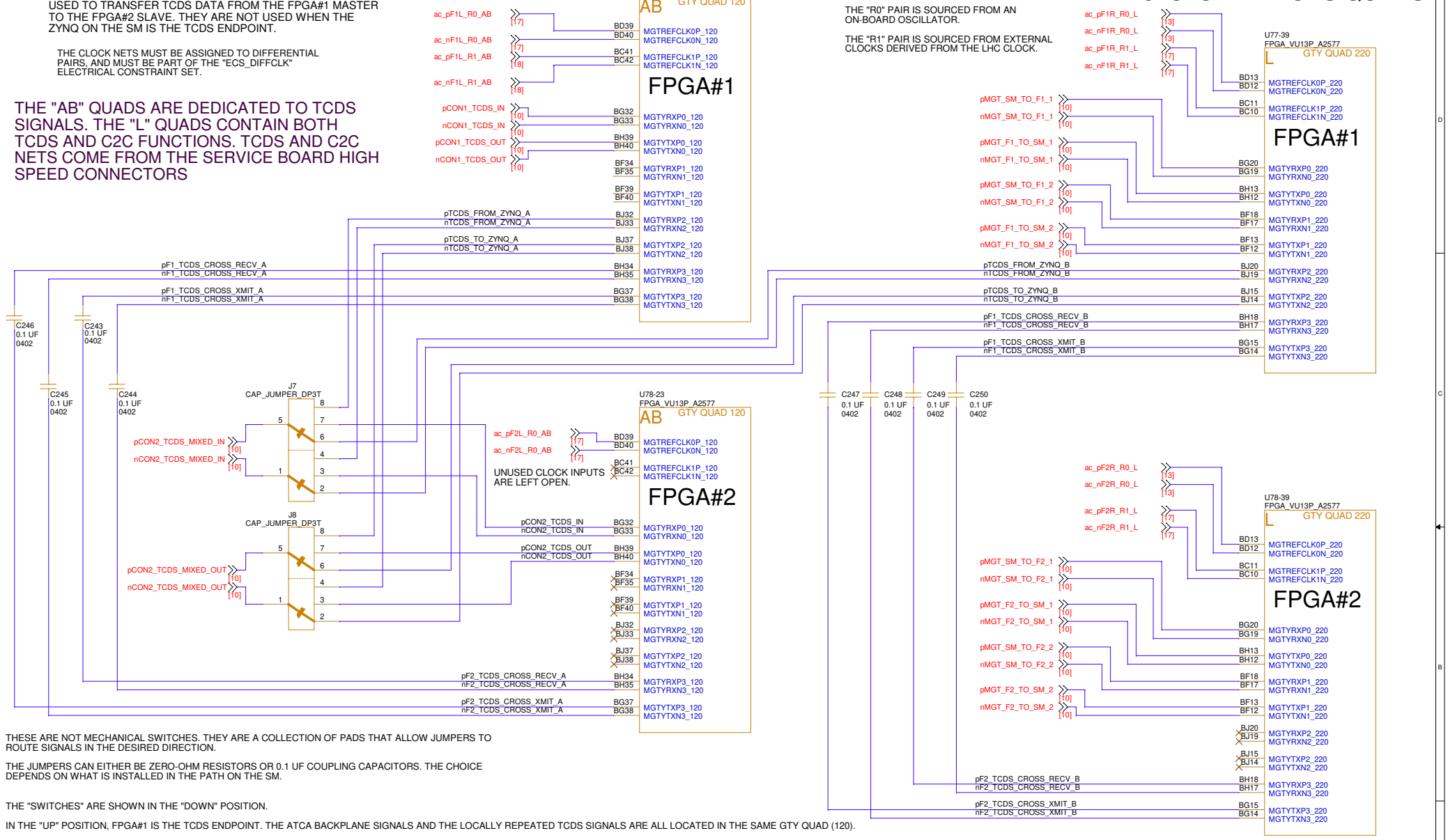
THE CROSS-CONNECT SIGNALS ON GTY CHANNEL 3 ARE USED TO TRANSFER TCDS DATA FROM THE FPGA#1 MASTER TO THE FPGA#2 SLAVE. THEY ARE NOT USED WHEN THE ZYNQ ON THE SM IS THE TCDS ENDPOINT.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE "AB" QUADS ARE DEDICATED TO TCDS SIGNALS. THE "L" QUADS CONTAIN BOTH TCDS AND C2C FUNCTIONS. TCDS AND C2C NETS COME FROM THE SERVICE BOARD HIGH SPEED CONNECTORS

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.



THESE ARE NOT MECHANICAL SWITCHES. THEY ARE A COLLECTION OF PADS THAT ALLOW JUMPERS TO ROUTE SIGNALS IN THE DESIRED DIRECTION.

THE JUMPERS CAN EITHER BE ZERO-OHM RESISTORS OR 0.1 UF COUPLING CAPACITORS. THE CHOICE DEPENDS ON WHAT IS INSTALLED IN THE PATH ON THE SM.

THE "SWITCHES" ARE SHOWN IN THE "DOWN" POSITION.

IN THE "UP" POSITION, FPGA#1 IS THE TCDS ENDPOINT. THE ATCA BACKPLANE SIGNALS AND THE LOCALLY REPEATED TCDS SIGNALS ARE ALL LOCATED IN THE SAME GTY QUAD (120).

"TTC" DATA IS RECEIVED BY FPGA#1 USING THE "CON1_TCDS_IN" CONNECTION ON CHANNEL 0. "TTC-TYPE" DATA IS SENT TO FPGA#2 USING THE "TCDS_CROSS_XMIT_A" CONNECTION ON CHANNEL 3. "TTC-TYPE" DATA IS SENT TO THE ZYNQ ON THE SM USING THE "TCDS_TO_ZYNQ_A" CONNECTION ON CHANNEL 2.

"TTS-TYPE" RESPONSE DATA FROM FPGA#2 IS RECEIVED ON THE "TCDS_CROSS_RECV_A" CONNECTION ON CHANNEL 3. "TTS-TYPE" RESPONSE DATA FROM THE SM COMES IN ON THE "TCDS_FROM_ZYNQ_A" CONNECTION ON CHANNEL 2. FPGA#1 MERGES THE "TTS" RESPONSE DATA FROM THE SM AND FPGA#2, AND SENDS IT TO THE ATCA BACKPLANE USING THE "CON1_TCDS_OUT" CONNECTION ON CHANNEL 0.

==========

IN THE "MIDDLE" POSITION, THE SM IS THE TCDS ENDPOINT. EACH FPGA HAS ITS OWN CONNECTION TO THE SM. NO CROSS CONNECTIONS BETWEEN THE TWO FPGAS ARE USED.

"TTC-TYPE" DATA IS RECEIVED BY FPGA#1 USING THE "CON1_TCDS_IN" CONNECTION ON CHANNEL 0.
"TTC-TYPE" DATA IS RECEIVED BY FPGA#2 USING THE "CON2_TCDS_MIXED_IN / CON2_TCDS_IN" CONNECTION ON CHANNEL 0.

"TTS-TYPE" RESPONSE DATA FROM FPGA#1 IS SENT TO THE SM USING THE "CON1_TCDS_OUT" CONNECTION ON CHANNEL 0. "TTS-TYPE" RESPONSE DATA FROM FPGA#2 IS SENT TO THE SM USING THE "CON2_TCDS_OUT / CONN2_TCDS_MIXED_OUT" CONNECTION ON CHANNEL 0. THE SM MERGES THE "TTS" RESPONSE DATA FROM THE TWO FPGAS.

==========

IN THE "DOWN" POSITION, FPGA#1 IS THE TCDS ENDPOINT. THE ATCA BACKPLANE SIGNALS ARE CONNECTED TO GTY QUAD 120. RELAYING THE "TTC-TYPE" DATA TO FPGA#2 AND THE SM IS DONE IN A DIFFERENT GTY QUAD, QUAD 220. THE "TTS-TYPE" RESPONSE DATA FROM FPGA#2 AND THE SM IS RECEIVED IN QUAD 220. IT IS COMBINED WITH "TTS-TYPE" DATA FROM FPGA#1 AND SENT TO THE ATCA BACKPLANE FROM QUAD 120.

"TTC" DATA IS RECEIVED BY FPGA#1 USING THE "CON1_TCDS_IN" CONNECTION ON CHANNEL 0.
"TTC-TYPE" DATA IS SENT TO FPGA#2 USING THE "TCDS_CROSS_XMIT_B" CONNECTION ON CHANNEL 3 OF QUAD 220.
"TTC-TYPE" DATA IS SENT TO THE ZYNQ ON THE SM USING THE "TCDS_TO_ZYNQ_B" CONNECTION ON CHANNEL 2 OF QUAD 220.

"TTS-TYPE" RESPONSE DATA FROM FPGA#2 IS RECEIVED ON THE "TCDS_CROSS_RECV_B" CONNECTION ON CHANNEL 3 OF QUAD 220. "TTS-TYPE" RESPONSE DATA FROM THE SM COMES IN ON THE "TCDS_FROM_ZYNQ_B" CONNECTION ON CHANNEL 2 OF QUAD 220. FPGA#1 MERGES THE "TTS" RESPONSE DATA FROM THE SM AND FPGA#2, AND SENDS IT TO THE ATCA BACKPLANE USING THE "CON1_TCDS_OUT" CONNECTION ON CHANNEL 0 OF QUAD 120.

APOLLO CM v3		
Title: 2.13: C2C_AND_TCDS_QUADS		
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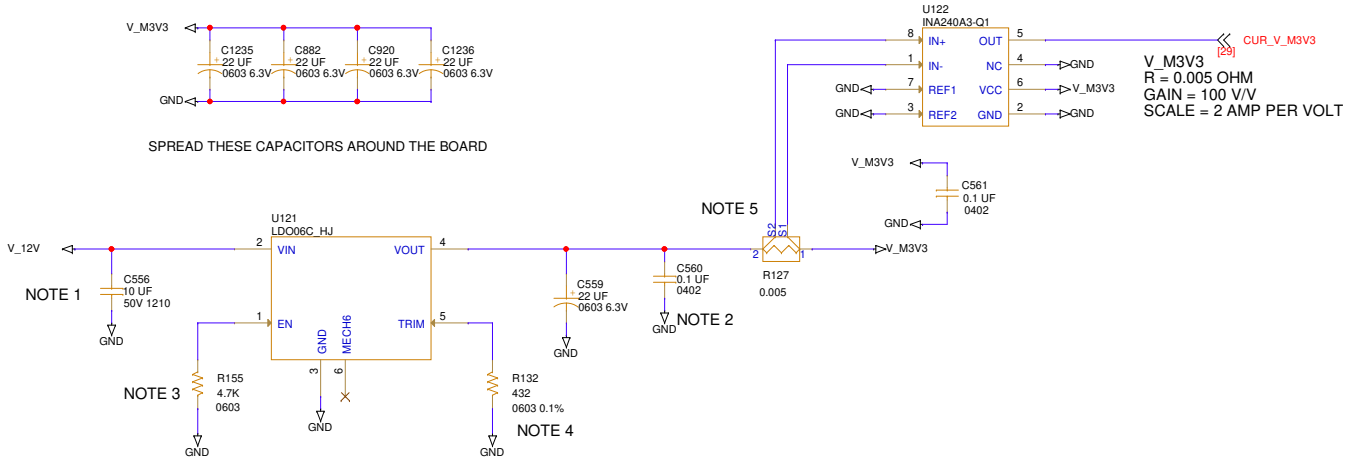
3.01: POWER MANAGEMENT M3V3



GENERAL NOTES:

V_M3V3 IS THE "MANAGEMENT" POWER. IT PROVIDES POWER TO THE POWER SEQUENCING CIRCUIT. IT IS ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

NOTES:

NOTE 1 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL INPUT CAPACITORS.

NOTE 2 THIS DEVICE DOES NOT REQUIRE ANY EXTERNAL OUTPUT CAPACITORS.

NOTE 3 UNDERVOLTAGE LOCKOUT RESISTOR
R = 14.81 * (6.81 / ((6.81*Ven) - 18.16))
A 4.7K RESISTOR GIVES 5.8 VOLTS MINIMUM TURNON VOLTAGE

NOTE 4 OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 3.3 VOLTS, R = 436 OHMS (IF R=432 THEN V=3.327)

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

APOLLO CM v3		
Title: 3.01: POWER MANAGEMENT M3V3		
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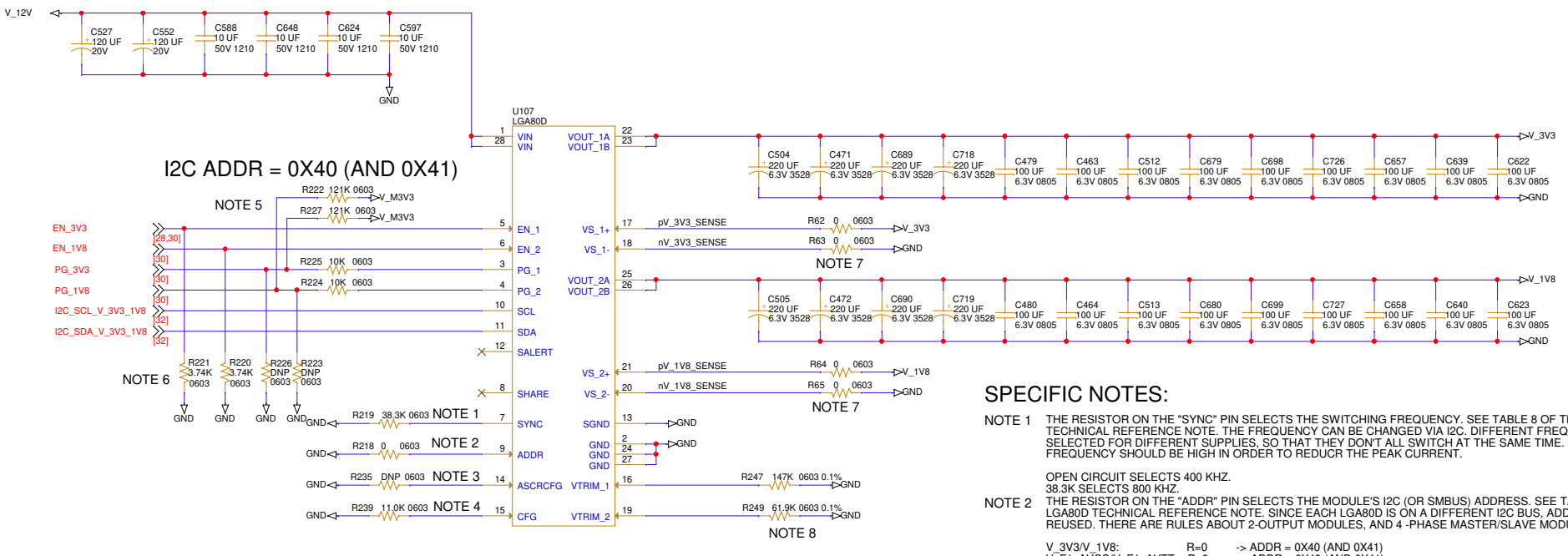
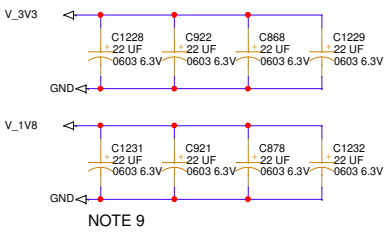
3.02: POWER GLOBAL 3.3V AND 1.8V





SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME. FOR 3.3V, THE FREQUENCY SHOULD BE HIGH IN ORDER TO REDUCR THE PEAK CURRENT.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=11K SELECTS 2-OUTPUT @ 35A(avg)/45A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 147K FOR 3.3V
RSET = 61.9K FOR 1.8V

NOTE 9 SPREAD THESE CAPACITORS AROUND THE BOARD

GENERAL NOTES:

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

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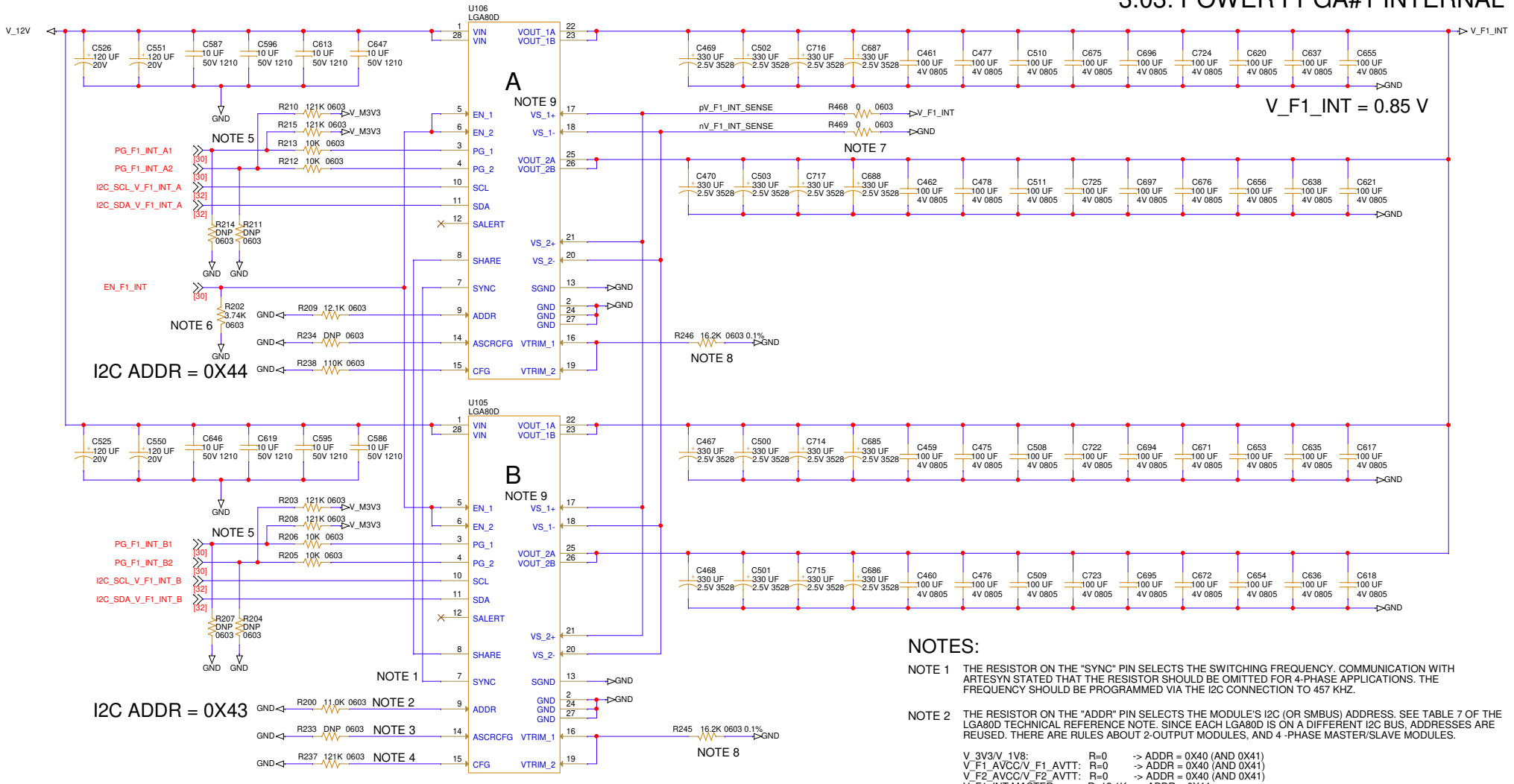
3.03: POWER FPGA#1 INTERNAL



NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

NOTE 10 PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

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Title: 3.03: POWER FPGA#1 INTERNAL			
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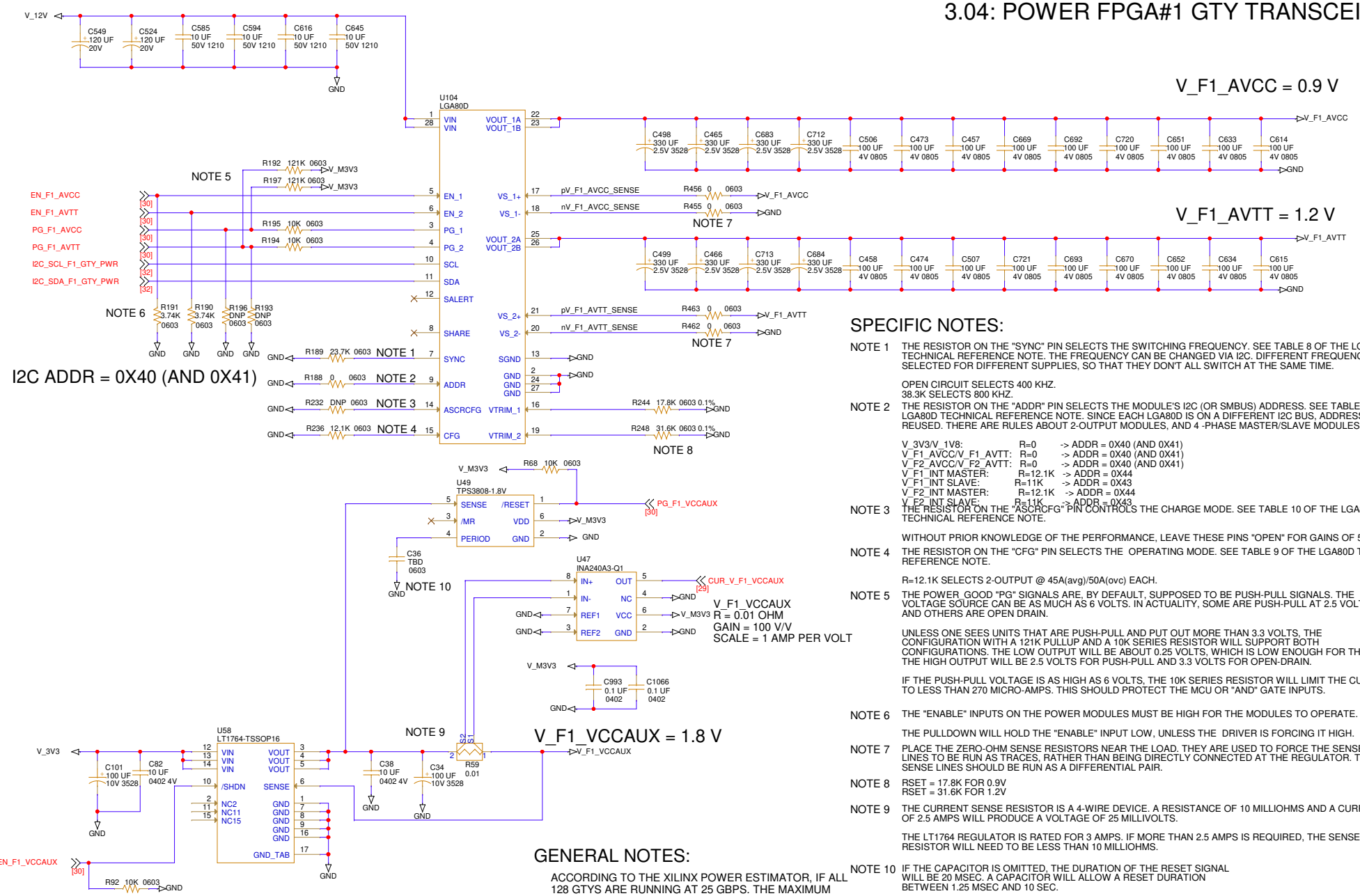
3.04: POWER FPGA#1 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
38.3K SELECTS 800 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM v3		
Title: 3.04: POWER FPGA#1 GTY TRANSCEIVER		
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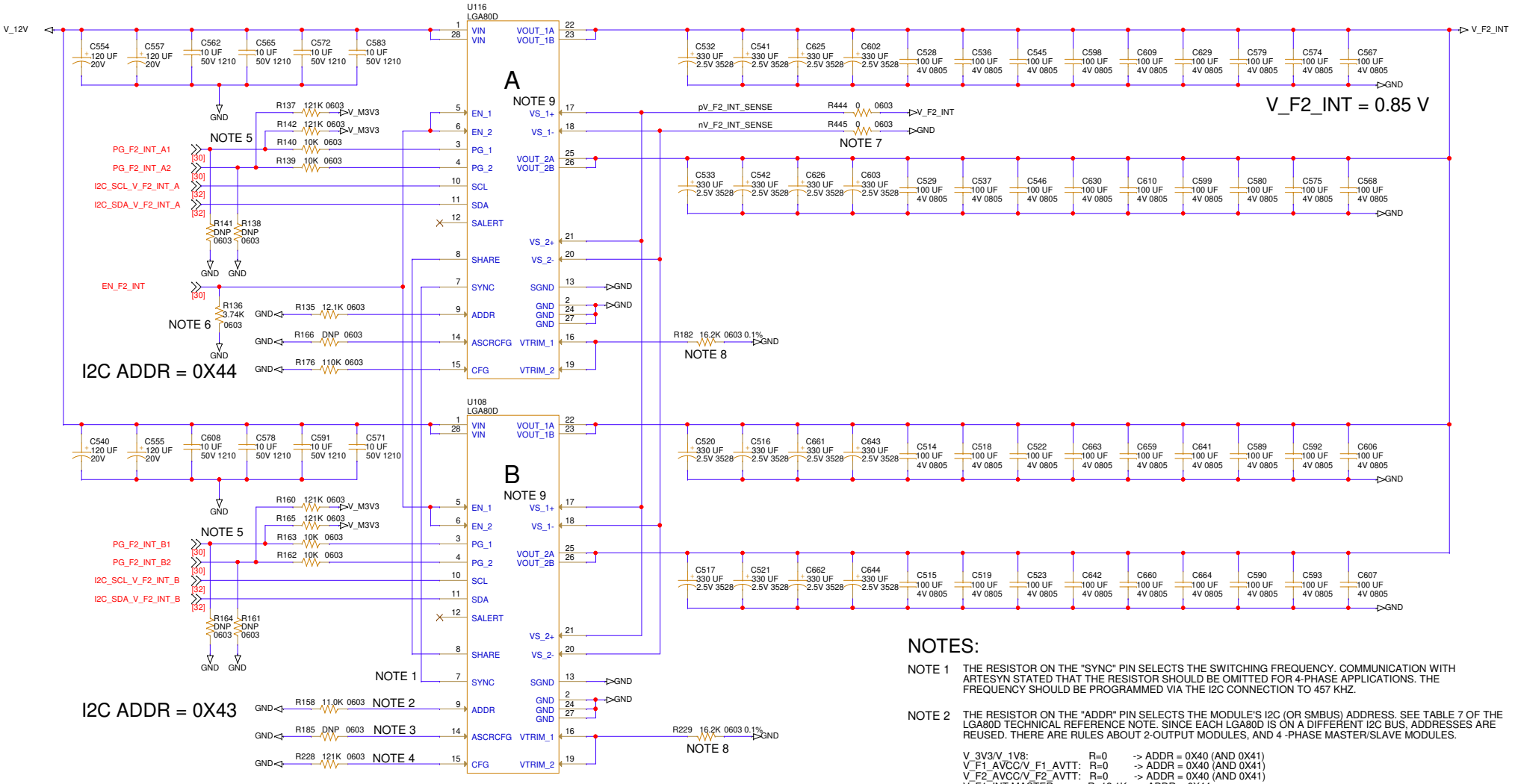
3.05: POWER FPGA#2 INTERNAL



NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. COMMUNICATION WITH ARTESYN STATED THAT THE RESISTOR SHOULD BE OMITTED FOR 4-PHASE APPLICATIONS. THE FREQUENCY SHOULD BE PROGRAMMED VIA THE I2C CONNECTION TO 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 10K.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

ARTESYN COMMUNICATION SPECIFIED 110K ON THE MASTER AND 121K ON THE SLAVE FOR 4-PHASE @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 16.2K FOR 0.85V

NOTE 9 THE MASTER IS LABELED "A".
THE SLAVE IS LABELED "B".

APOLLO CM v3			
Title: 3.05: POWER FPGA#2 INTERNAL			
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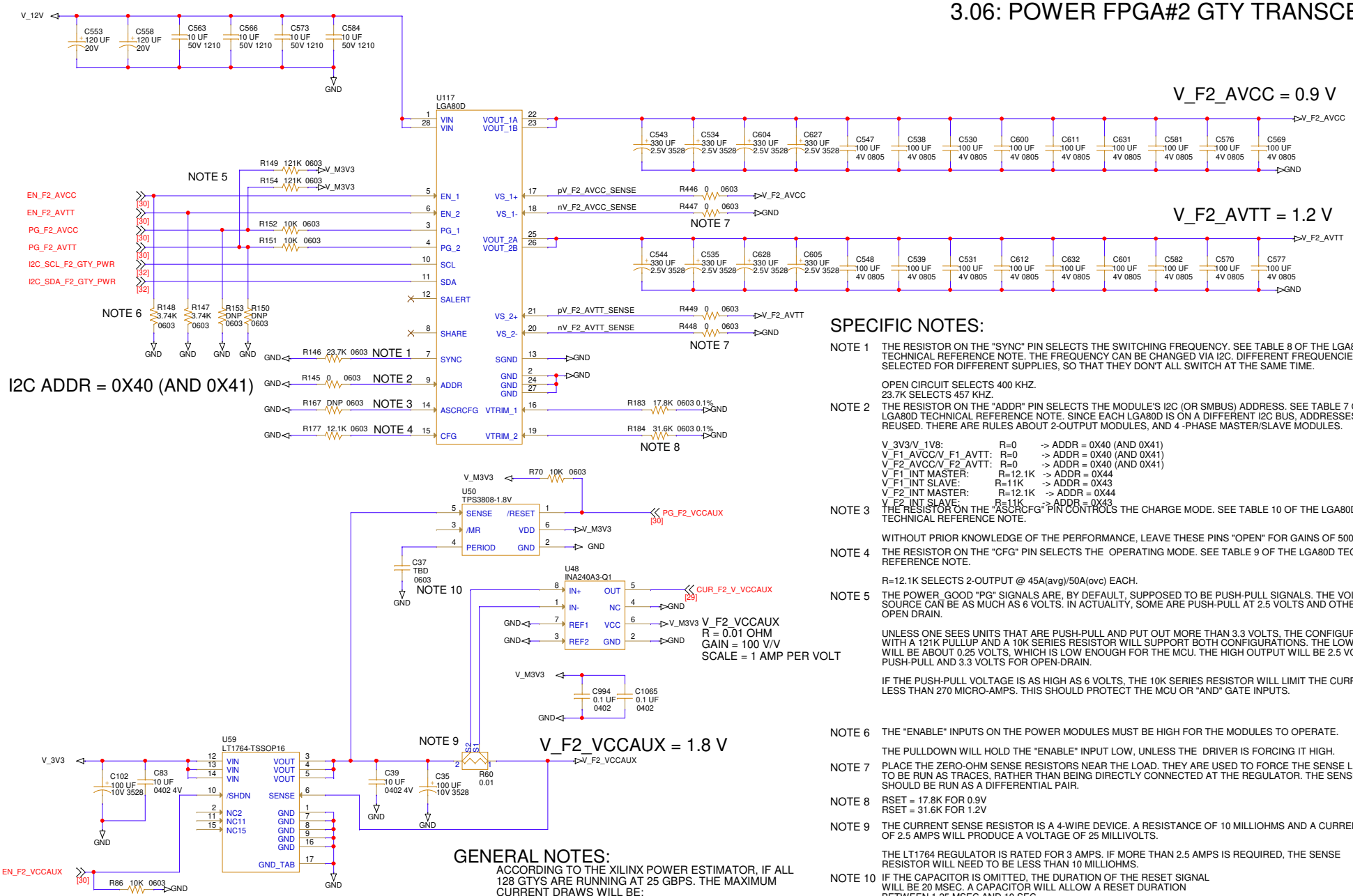
3.06: POWER FPGA#2 GTY TRANSCEIVER



SPECIFIC NOTES:

NOTE 1 THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.
23.7K SELECTS 457 KHZ.

NOTE 2 THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. SINCE EACH LGA80D IS ON A DIFFERENT I2C BUS, ADDRESSES ARE REUSED. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

V_3V3/V_1V8:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_AVCC/V_F1_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F2_AVCC/V_F2_AVTT:	R=0	-> ADDR = 0X40 (AND 0X41)
V_F1_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F1_INT SLAVE:	R=11K	-> ADDR = 0X43
V_F2_INT MASTER:	R=12.1K	-> ADDR = 0X44
V_F2_INT SLAVE:	R=11K	-> ADDR = 0X43

NOTE 3 THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

NOTE 4 THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=12.1K SELECTS 2-OUTPUT @ 45A(avg)/50A(ovc) EACH.

NOTE 5 THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, SUPPOSED TO BE PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS. IN ACTUALITY, SOME ARE PUSH-PULL AT 2.5 VOLTS AND OTHERS ARE OPEN DRAIN.

UNLESS ONE SEES UNITS THAT ARE PUSH-PULL AND PUT OUT MORE THAN 3.3 VOLTS, THE CONFIGURATION WITH A 121K PULLUP AND A 10K SERIES RESISTOR WILL SUPPORT BOTH CONFIGURATIONS. THE LOW OUTPUT WILL BE ABOUT 0.25 VOLTS, WHICH IS LOW ENOUGH FOR THE MCU. THE HIGH OUTPUT WILL BE 2.5 VOLTS FOR PUSH-PULL AND 3.3 VOLTS FOR OPEN-DRAIN.

IF THE PUSH-PULL VOLTAGE IS AS HIGH AS 6 VOLTS, THE 10K SERIES RESISTOR WILL LIMIT THE CURRENT TO LESS THAN 270 MICRO-AMPS. THIS SHOULD PROTECT THE MCU OR "AND" GATE INPUTS.

NOTE 6 THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

NOTE 7 PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

NOTE 8 RSET = 17.8K FOR 0.9V
RSET = 31.6K FOR 1.2V

NOTE 9 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 10 MILLIOHMS AND A CURRENT OF 2.5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LT1764 REGULATOR IS RATED FOR 3 AMPS. IF MORE THAN 2.5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 10 MILLIOHMS.

NOTE 10 IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

GENERAL NOTES:

ACCORDING TO THE XILINX POWER ESTIMATOR, IF ALL 128 GTYS ARE RUNNING AT 25 GBPS. THE MAXIMUM CURRENT DRAWS WILL BE:
GTY_AVCC = 11.5 AMPS
GTY_AVTT = 30 AMPS
GTY_VCCAUX = 2.5 AMPS

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM v3

Title: 3.06: POWER FPGA#2 GTY TRANSCEIVER

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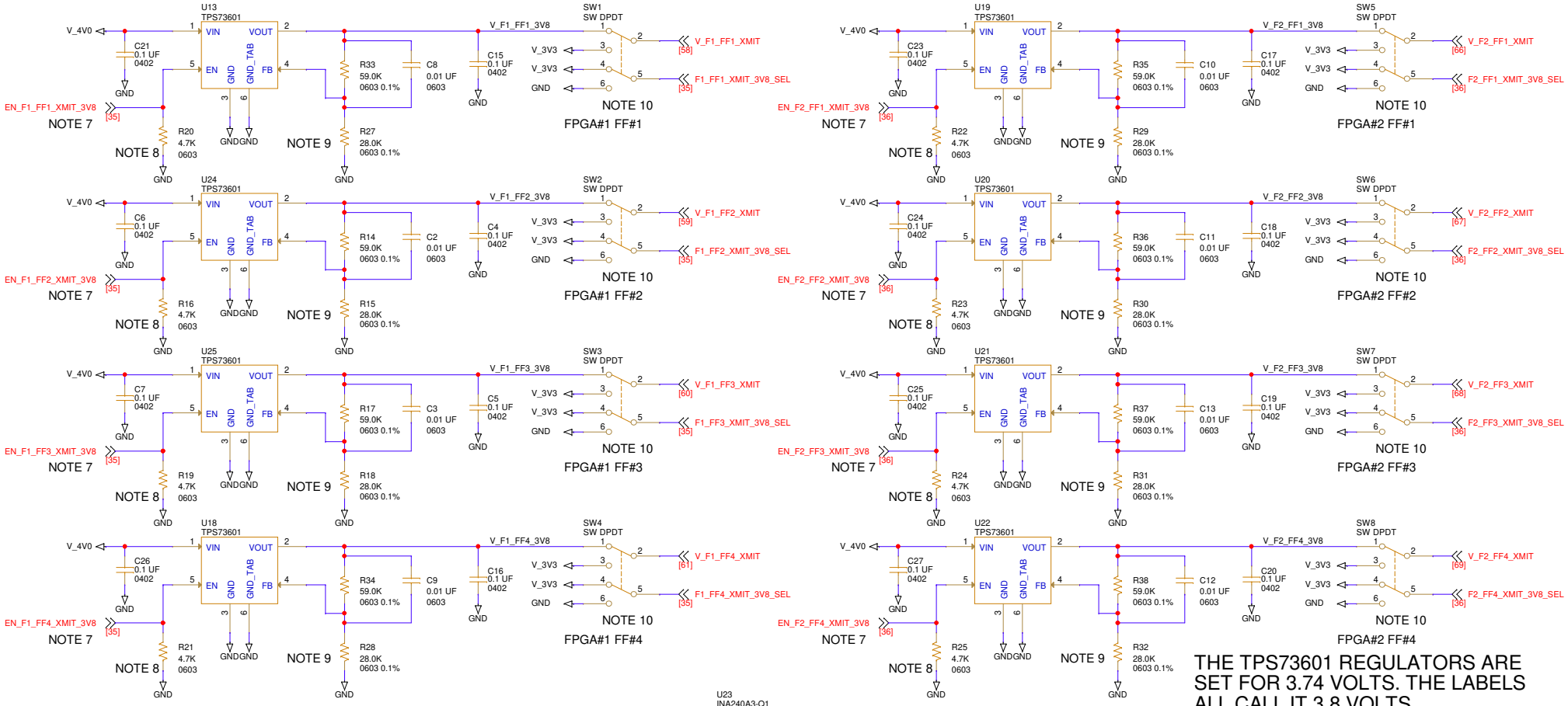
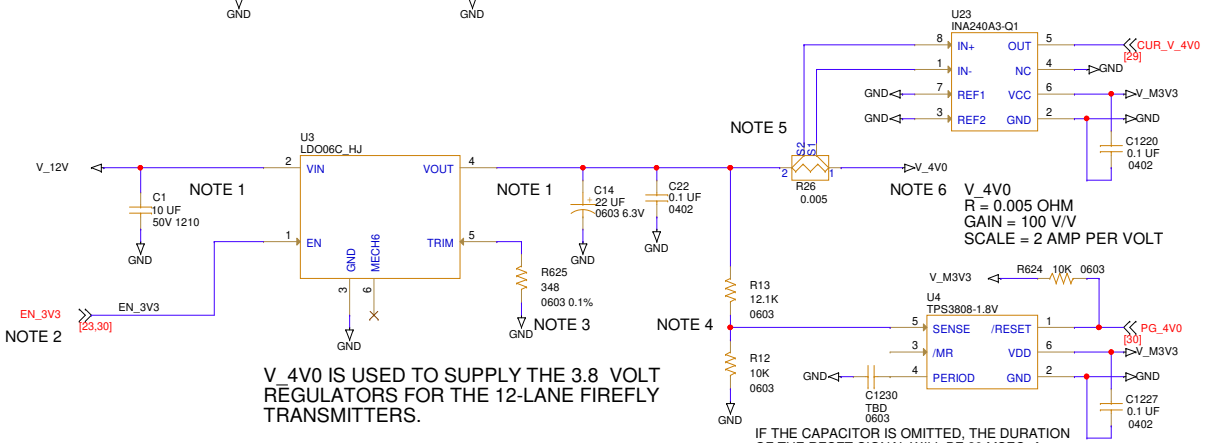
3.07: POWER FOR FF X12 XMIT



THE TPS73601 REGULATORS ARE SET FOR 3.74 VOLTS. THE LABELS ALL CALL IT 3.8 VOLTS.



V_4V0 IS USED TO SUPPLY THE 3.8 VOLT REGULATORS FOR THE 12-LANE FIREFLY TRANSMITTERS.

V_4V0
R = 0.005 OHM
GAIN = 100 V/V
SCALE = 2 AMP PER VOLT

IF THE CAPACITOR IS OMITTED, THE DURATION OF THE RESET SIGNAL WILL BE 20 MSEC. A CAPACITOR WILL ALLOW A RESET DURATION BETWEEN 1.25 MSEC AND 10 SEC.

NOTE 1 THE LDO06C DOES NOT REQUIRE ANY EXTERNAL INPUT OR OUTPUT CAPACITORS.

NOTE 2 THE LDO06C IS ENABLED AT THE SAME TIME AS THE BOARD-WIDE 3.3V SUPPLY.

NOTE 3 LDO06C OUTPUT SETPOINT RESISTOR
R = 1.182 / (VOUT - 0.591)
FOR 4.0 VOLTS, R=0.347 kOHMS

NOTE 4 THE MONITORING CHIP EXPECTS 1.8 VOLTS AT THE INPUT, SO THE 4.0 VOLTS IS DIVIDED.

NOTE 5 THE CURRENT SENSE RESISTOR IS A 4-WIRE DEVICE. A RESISTANCE OF 5 MILLIOHMS AND A CURRENT OF 5 AMPS WILL PRODUCE A VOLTAGE OF 25 MILLIVOLTS.

THE LDO06C REGULATOR IS RATED FOR 6 AMPS. IF MORE THAN 5 AMPS IS REQUIRED, THE SENSE RESISTOR WILL NEED TO BE LESS THAN 5 MILLIOHMS.

NOTE 6 V_4V0 IS ONLY CONNECTED ONTHIS PAGE, EXCEPT FOR MEASURING BY THE MCU ADC.

NOTE 7 THE TPS73601 REGULATOR SHOULD NOT BE ENABLED UNTIL THE FIREFLY TRANSMITTER TYPE HAS BEEN DETERMINED AND THE VOLTAGE SWITCH IS FOUND TO BE IN THE CORRECT POSITION.

NOTE 8 PULLDOWNS ARE NEEDED ON THE CONTROL INPUTS, SINCE THE I2C DRIVER DEVICES NEED TO BE CONFIGURED AS OUTPUTS BEFORE THEY CAN CONTOL THE LOGIC LEVEL. THE I2C DRIVERS HAVE A BUILT-IN 100K PULLUP.

NOTE 9 THE TPS73601 OUTPUT VOLTAGE IS CALCULATED BY:
VOUT = 1.204 * ((Rtop+Rbot)/Rbot)
IF Rtop = 59.0k AND Rbot=28K, THEN VOUT = 3.74 V

NOTE 10 THE SWITCH IS SHOWN IN THE POSITION TO PROVIDE 3.8 VOLTS TO THE FIREFLY TRANSMITTER. THE "*_3V8_SEL" SIGNAL WILL BE HIGH.

UNLESS NOTED, PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

APOLLO CM v3

Title: 3.07: POWER FOR FF X12 XMIT

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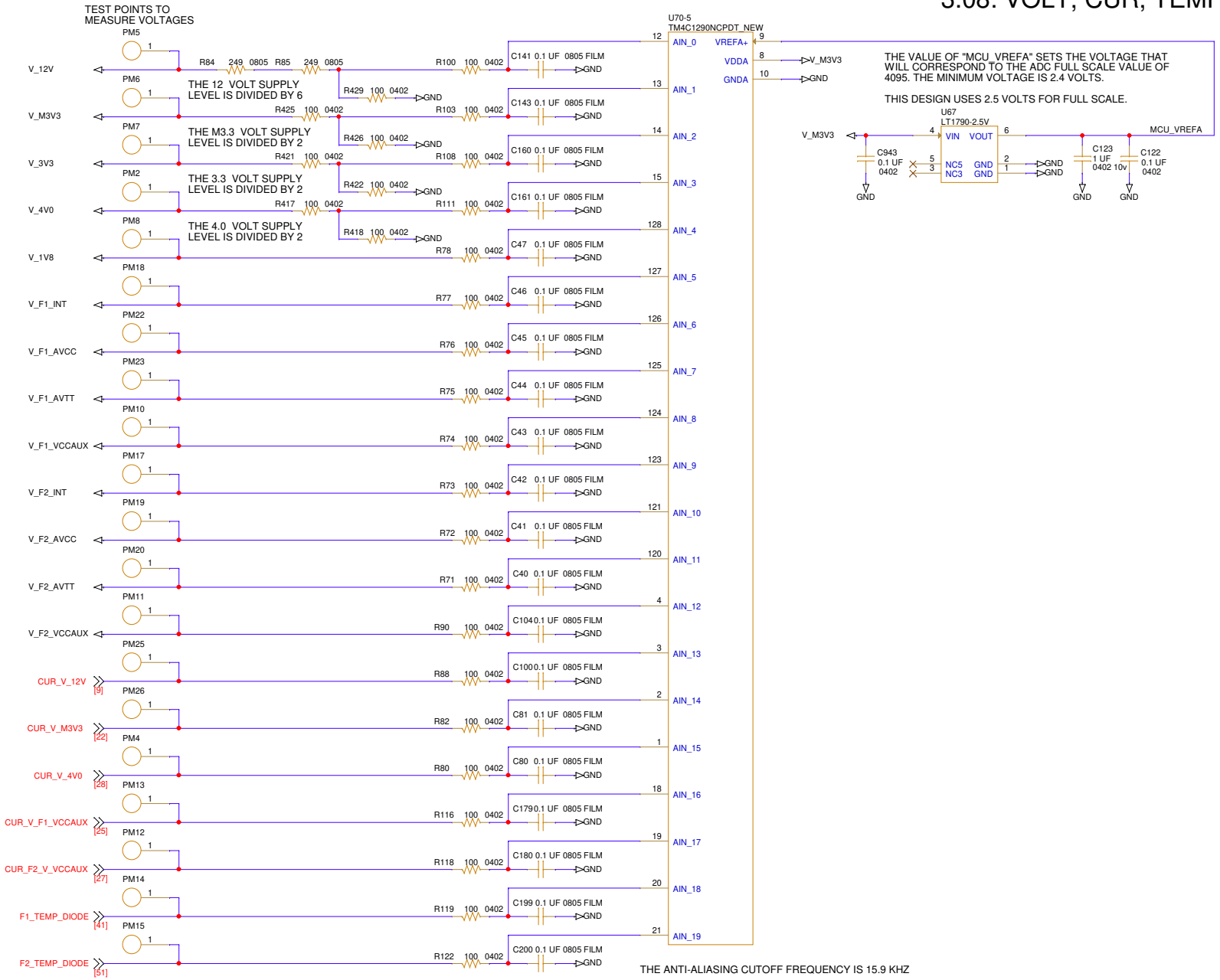
3.08: VOLT, CUR, TEMP MEASURE



Title	APOLLO CM v3
	3.08: VOLT, CUR, TEMP MEASURE
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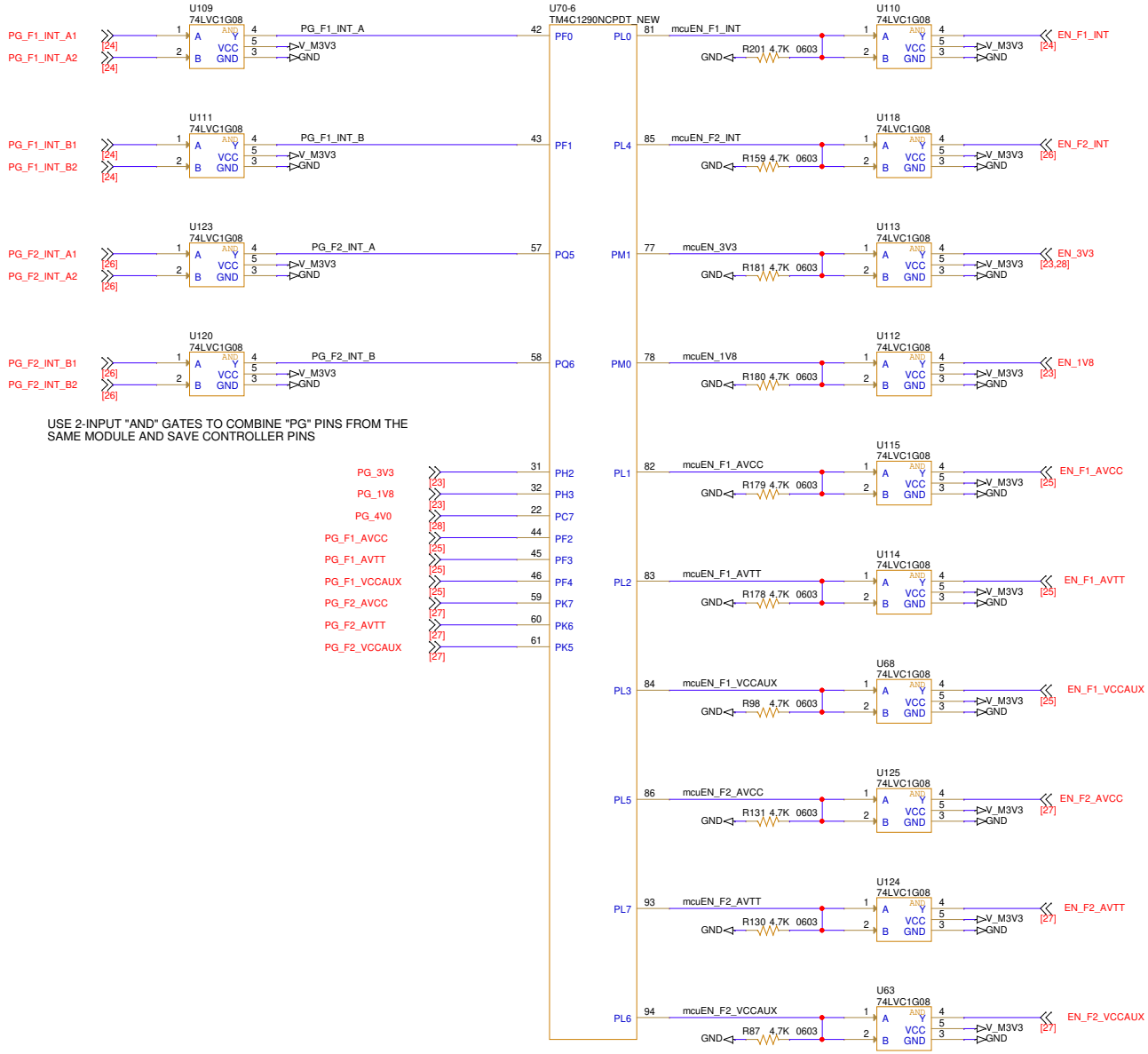
3.09: POWER CONTROL



USE 2-INPUT "AND" GATES TO COMBINE "PG" PINS FROM THE SAME MODULE AND SAVE CONTROLLER PINS

THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN V_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

APOLLO CM v3			
Title: 3.09: POWER CONTROL			
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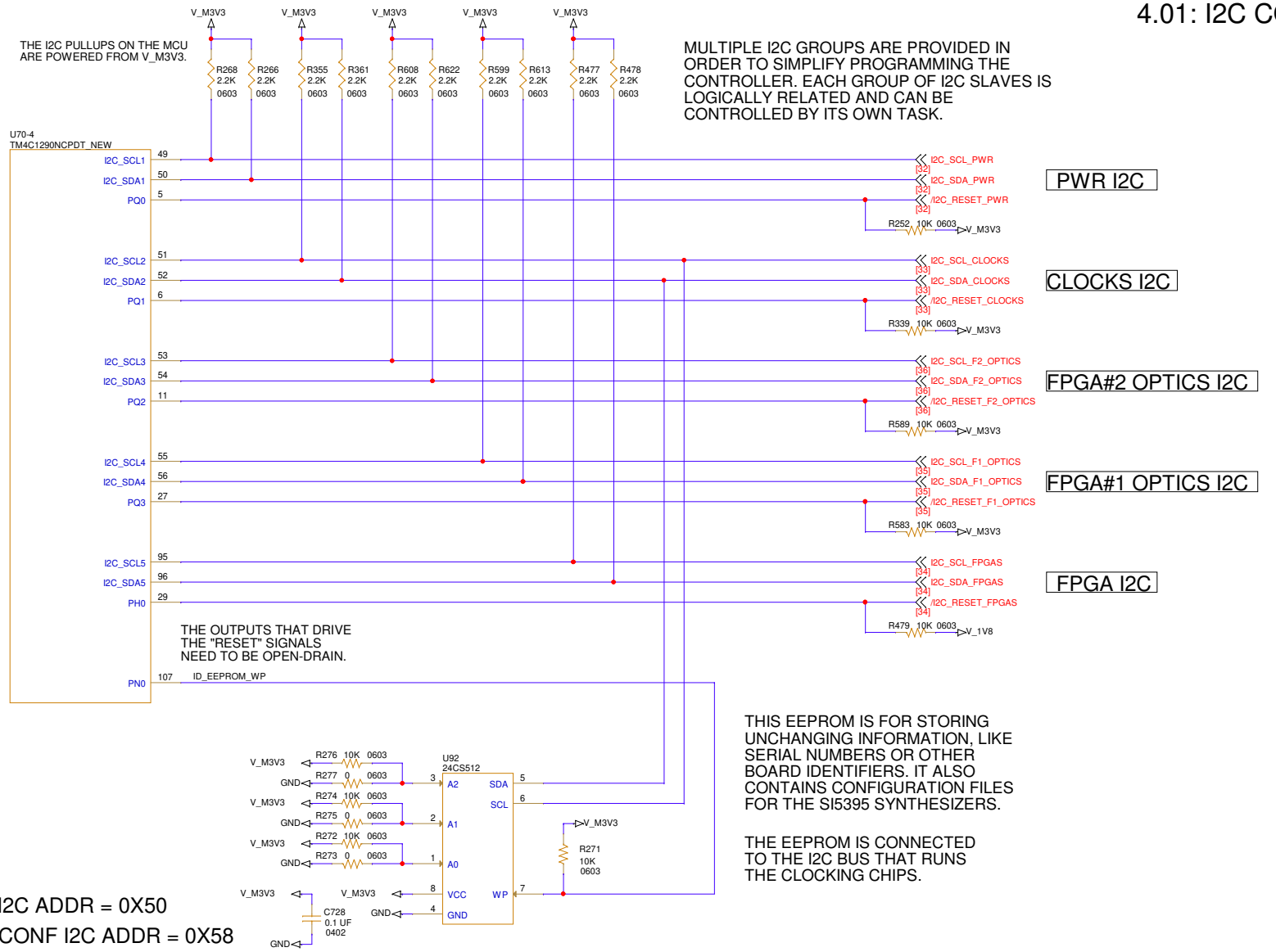
4.01: I2C CONTROLLER



R/W I2C ADDR = 0X50

SEC/CONF I2C ADDR = 0X58

24CS512 I2C ADDRESS:
EEPROM READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
SECURITY OR CONFIGURATION REGISTER
1 0 1 1 A2 A1 A0
RANGE 0X58 TO 0X5F

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

APOLLO CM v3		
Title: 4.01: I2C CONTROLLER		
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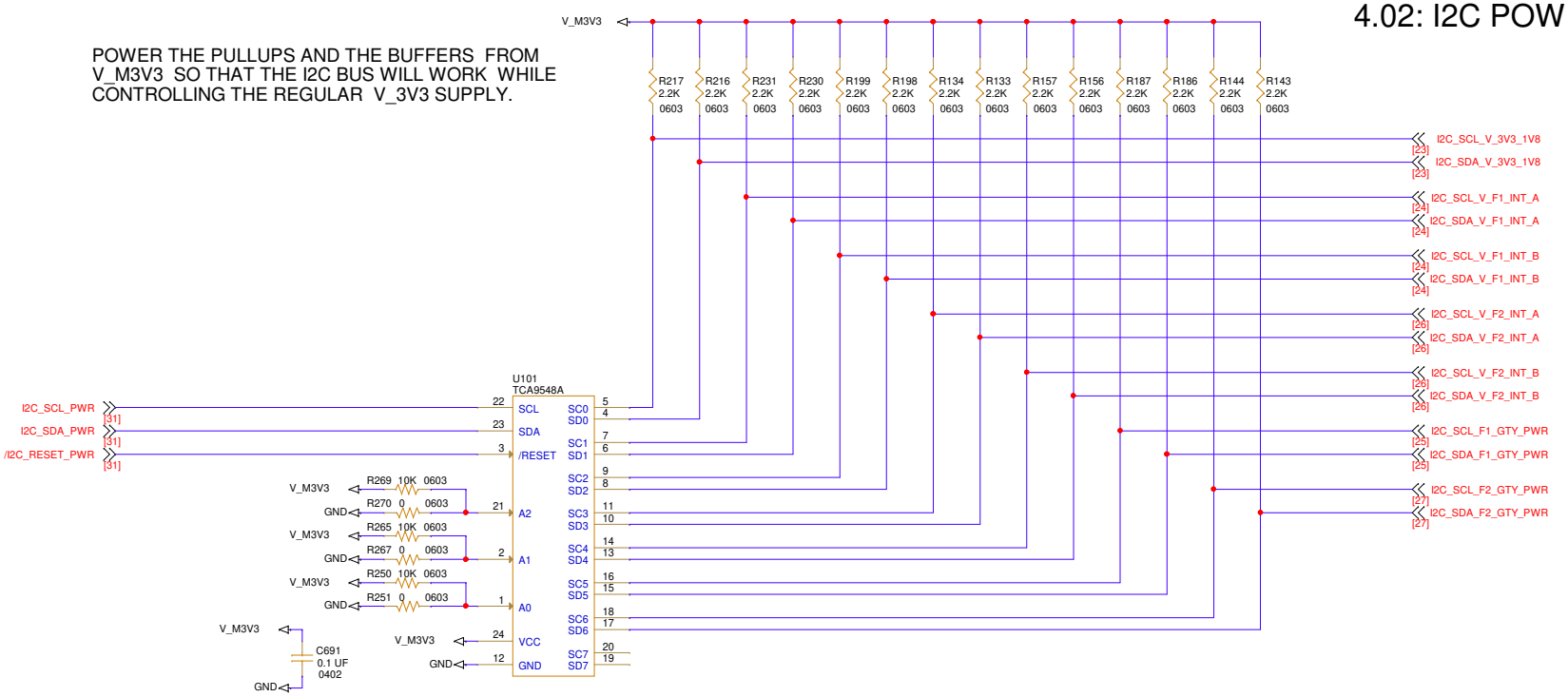
4.02: I2C POWER CONTROL

POWER THE PULLUPS AND THE BUFFERS FROM V_M3V3 SO THAT THE I2C BUS WILL WORK WHILE CONTROLLING THE REGULAR V_3V3 SUPPLY.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

APOLLO CM v3		
Title: 4.02: I2C POWER CONTROL		
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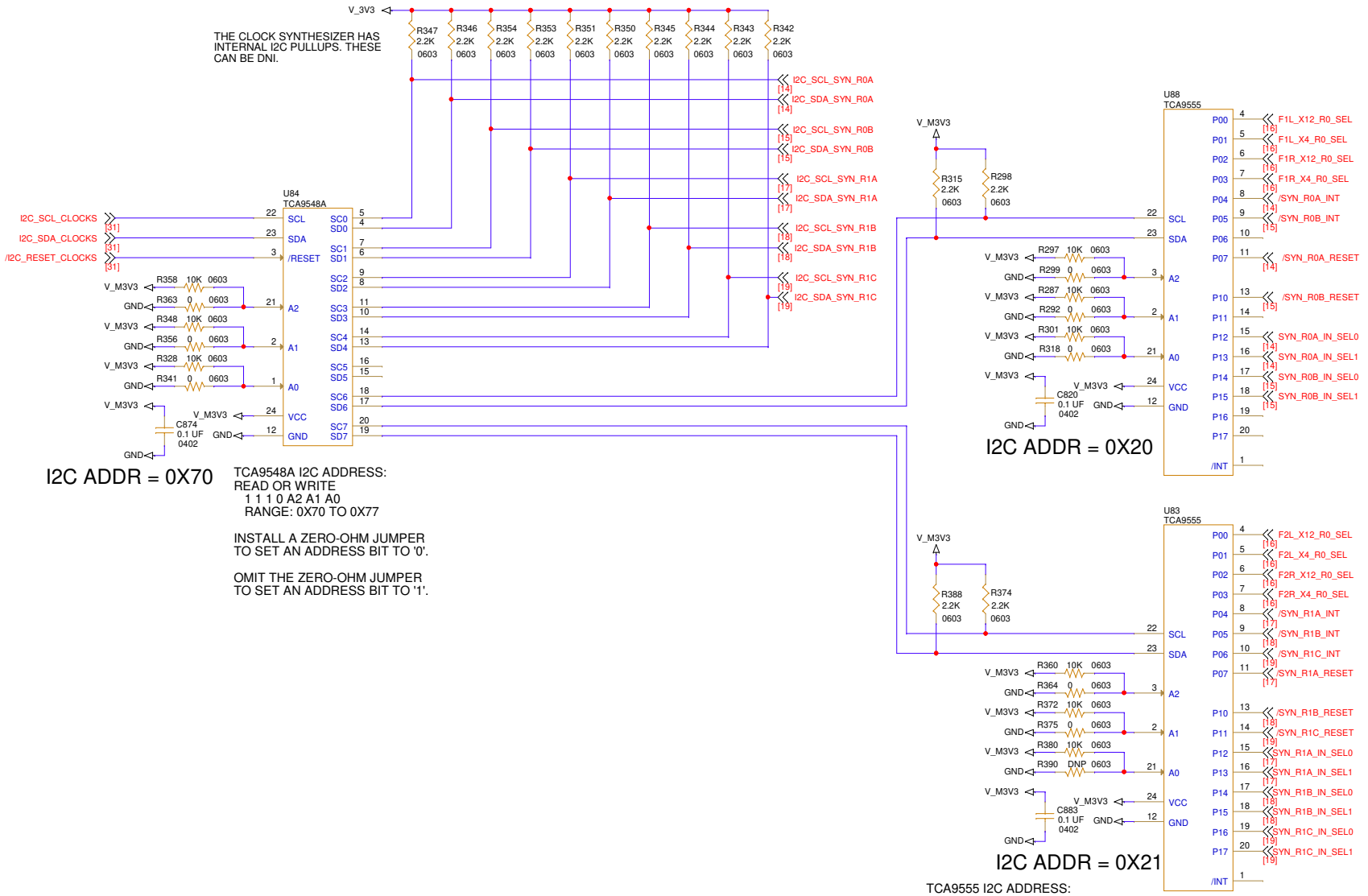
4.03: I2C CLOCK CONTROL



APOLLO CM v3		
Title: 4.03: I2C CLOCK CONTROL		
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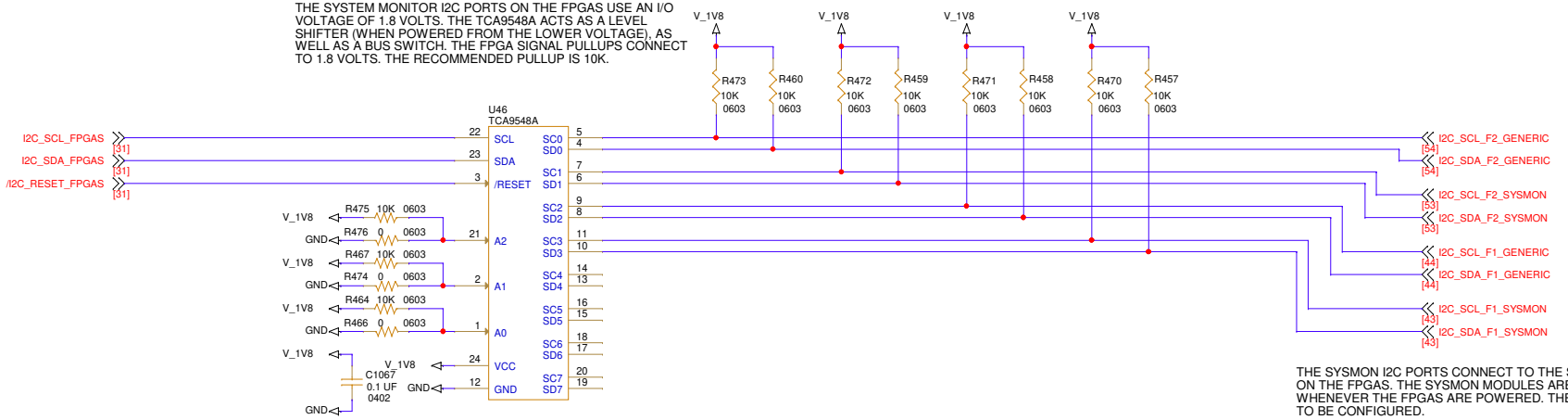
4.04: I2C FPGA INTERNALS

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER (WHEN POWERED FROM THE LOWER VOLTAGE), AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THE SYSMON I2C PORTS CONNECT TO THE SYSMON MODULE PINS ON THE FPGAS. THE SYSMON MODULES ARE AVAILABLE WHENEVER THE FPGAS ARE POWERED. THE FPGAS DO NOT HAVE TO BE CONFIGURED.

THE GENERIC I2C PORTS CONNECT TO I2C MODULES THAT ARE LOADED AS PART OF THE CONFIGURATION PROCESS. THEY ARE NOT AVAILABLE BEFORE THE FPGA HAS BEEN CONFIGURED.

THE GENERIC MODULES HAVE MORE CAPABILITY THAN THE SYSMON MODULES.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

APOLLO CM v3

Title: 4.04: I2C FPGA INTERNALS

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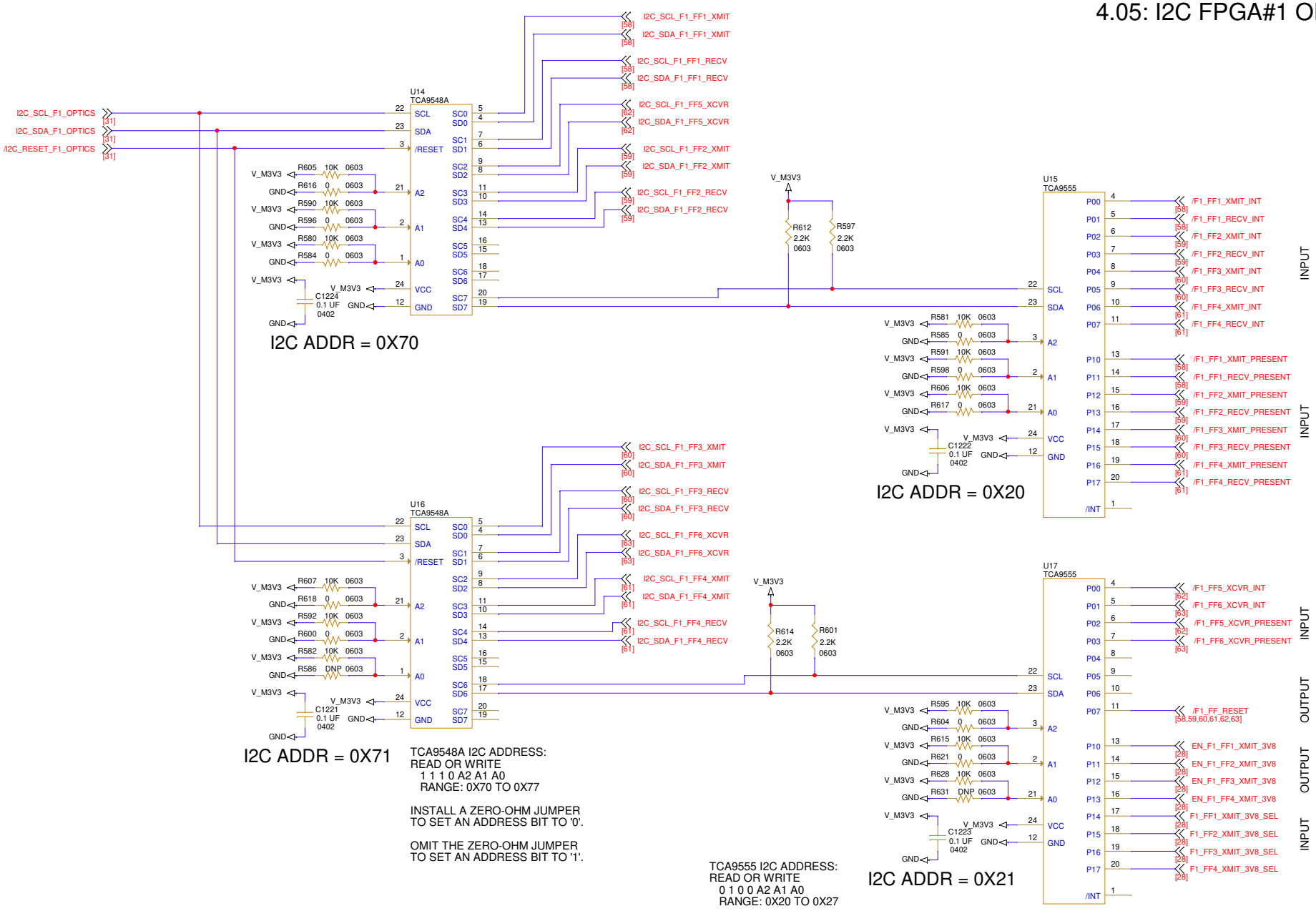
4.05: I2C FPGA#1 OPTICS



TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

I2C REGISTER PIN ASSIGNMENTS ARE SCRAMBLED COMPARED TO PREVIOUS CM VERSIONS

APOLLO CM v3		
Title: 4.05: I2C FPGA#1 OPTICS		
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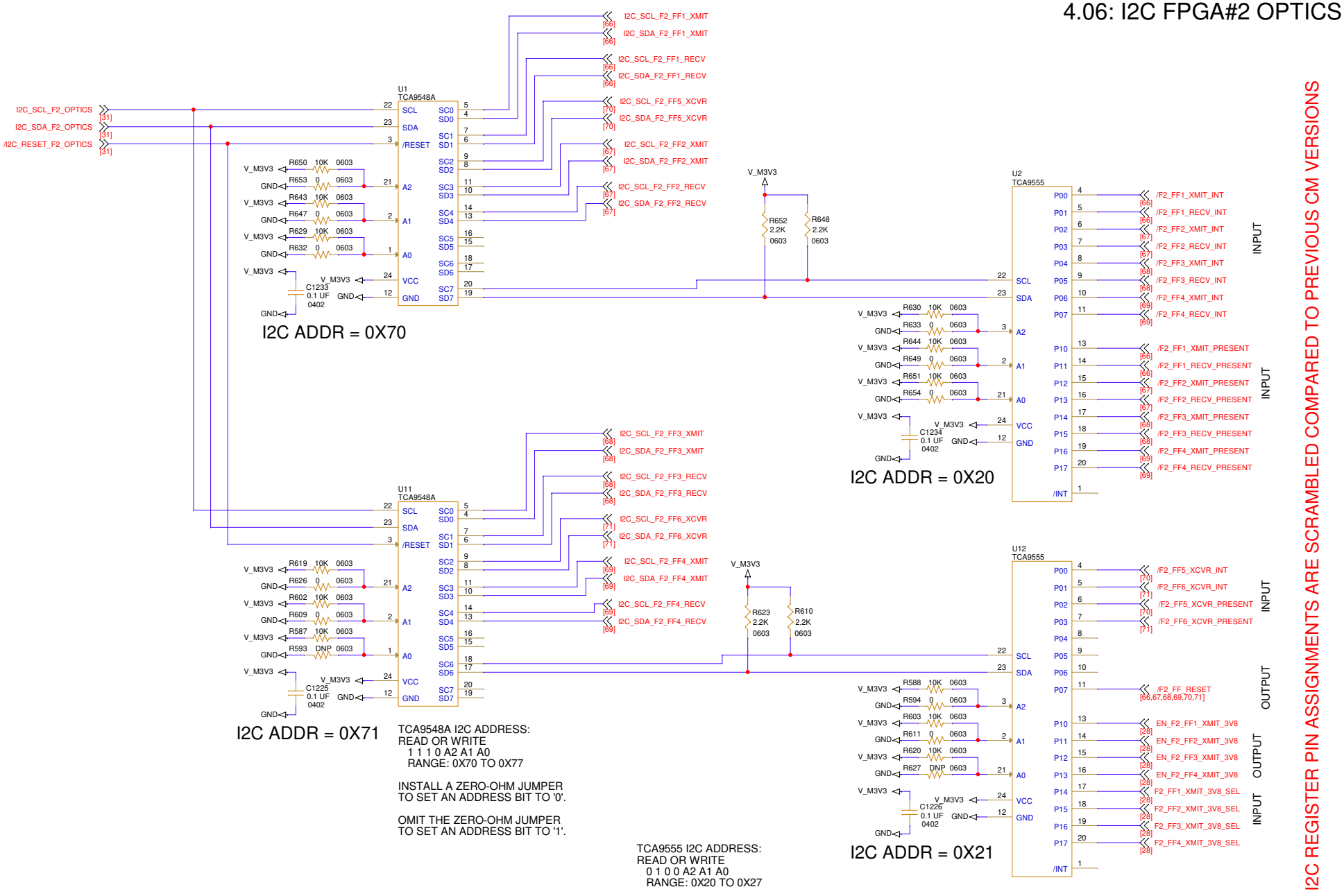
4.06: I2C FPGA#2 OPTICS



TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

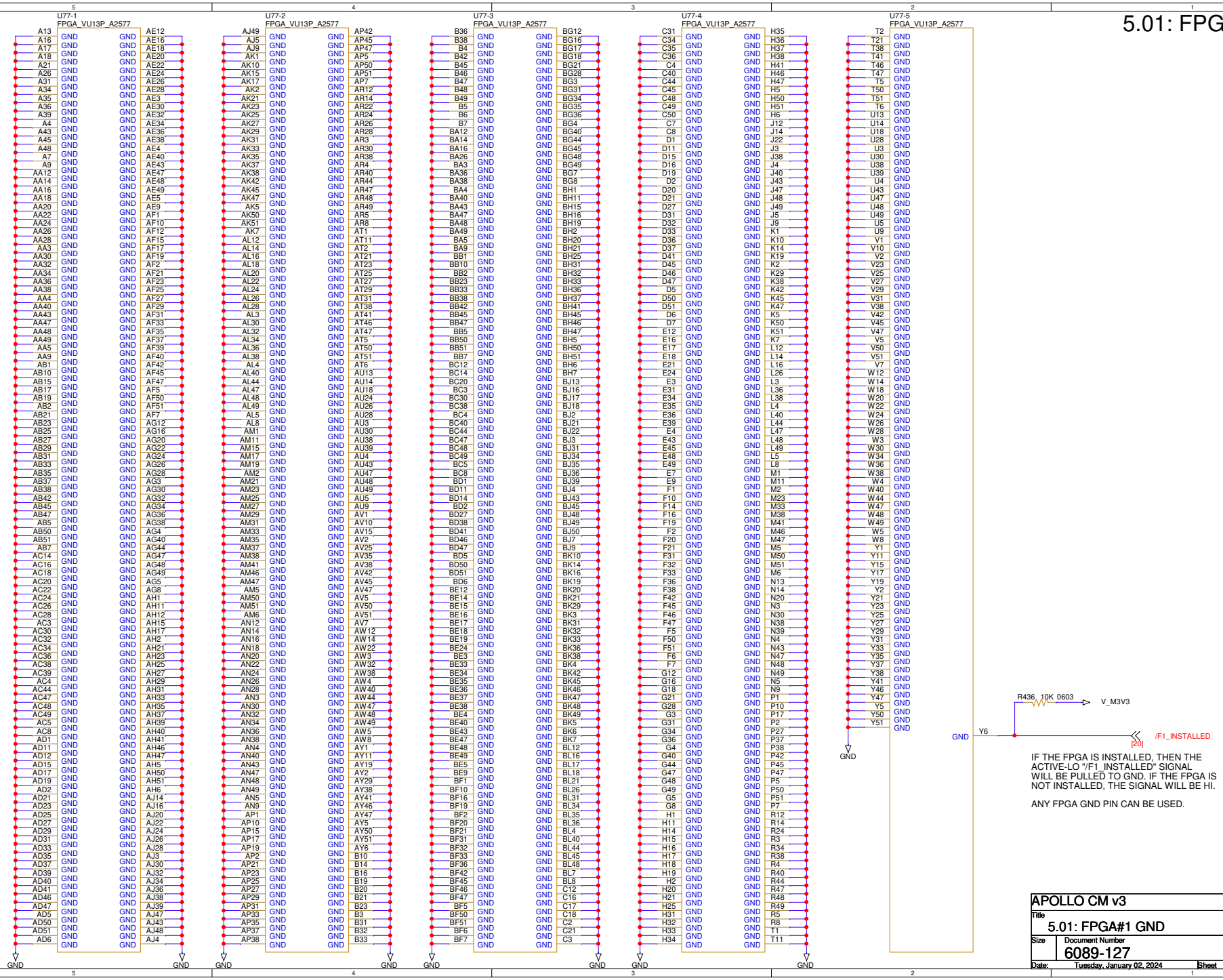
INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

I2C REGISTER PIN ASSIGNMENTS ARE SCRAMBLED COMPARED TO PREVIOUS CM VERSIONS

APOLLO CM v3		
Title: 4.06: I2C FPGA#2 OPTICS		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 36 of 78	

5.01: FPGA#1 GND



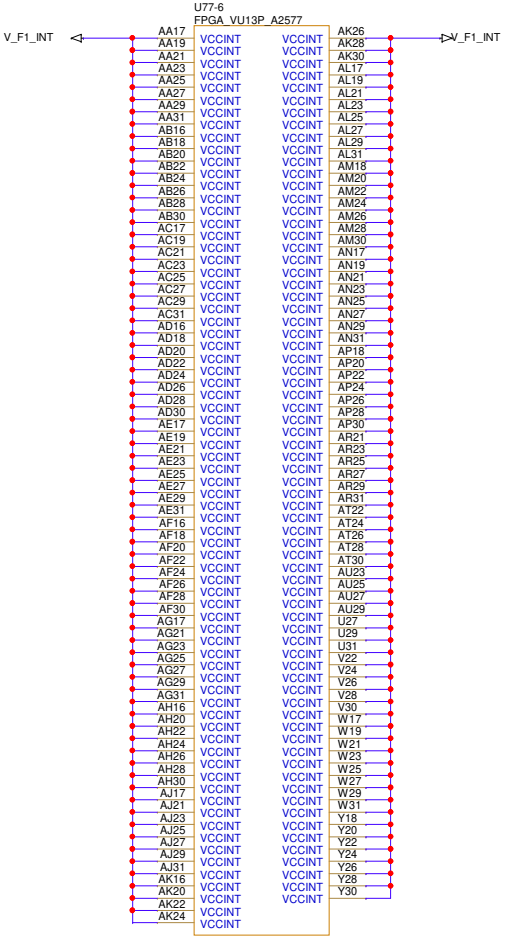
IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F1_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

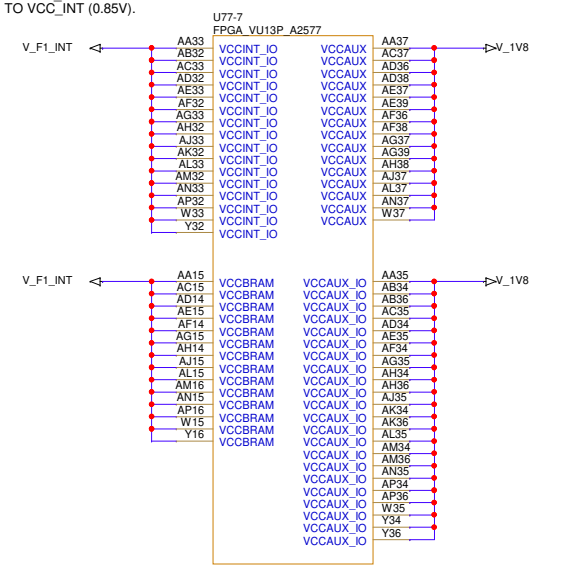
APOLLO CM v3		
Title: 5.01: FPGA#1 GND		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 37 of 78	

5.02: FPGA#1 POWER INTERNAL

VCCINT MUST BE 0.85V.

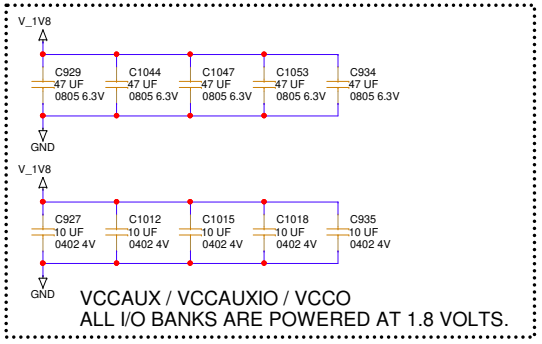


VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).

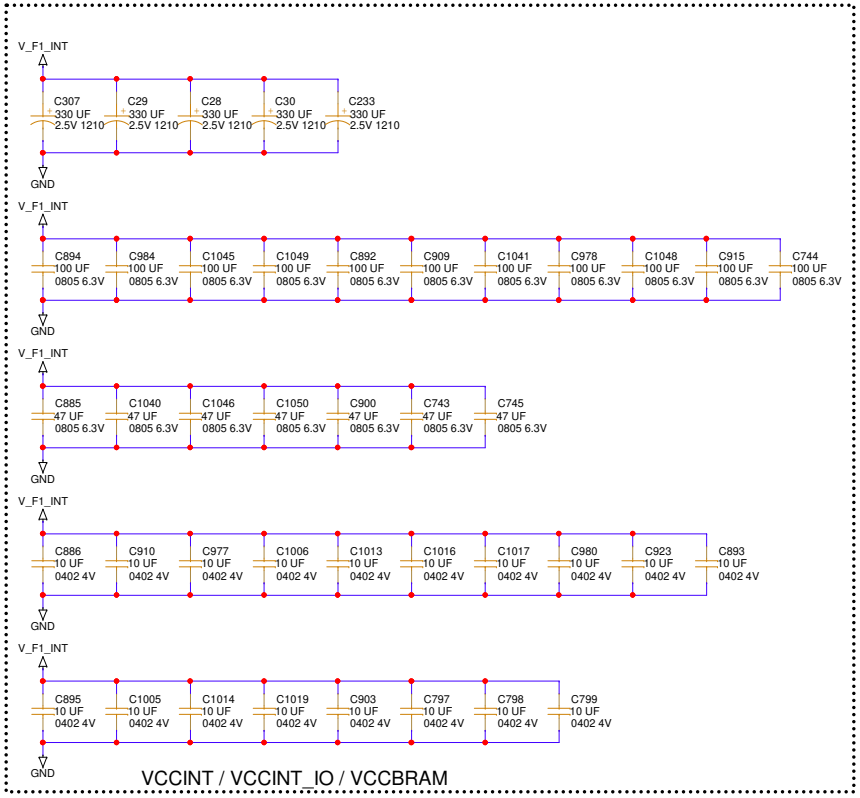


VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).



VCCAUX / VCCAUXIO / VCCO
ALL I/O BANKS ARE POWERED AT 1.8 VOLTS.

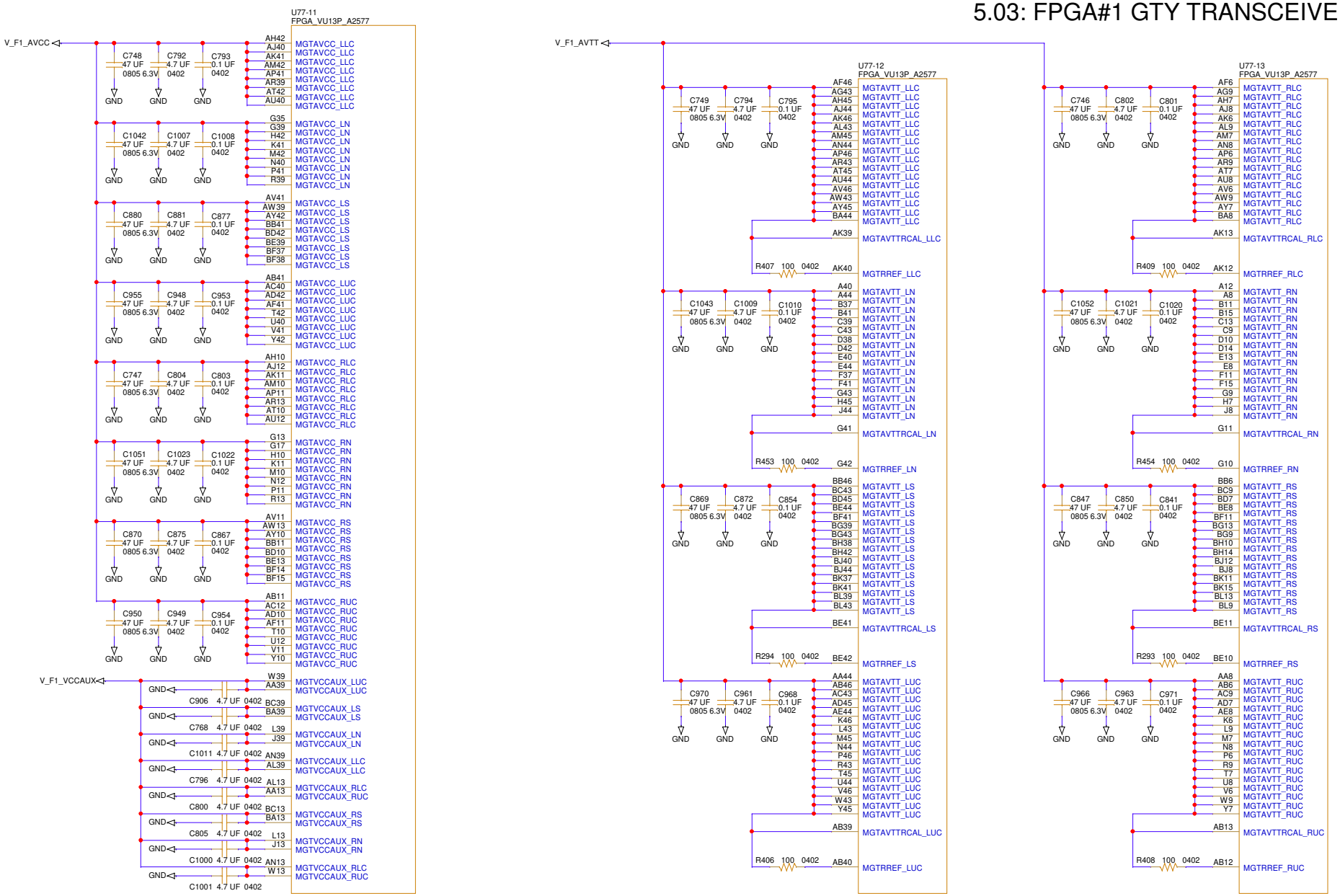


VCCINT / VCCINT_IO / VCCBRAM

BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"UG583 UltraScale Architecture PCB Design"

APOLLO CM v3		
Title: 5.02: FPGA#1 POWER INTERNAL		
Size	Document Number: 6089-127	Rev: A
Date: Friday, December 29, 2023	Sheet 38 of 78	

5.03: FPGA#1 GTY TRANSCEIVER POWER

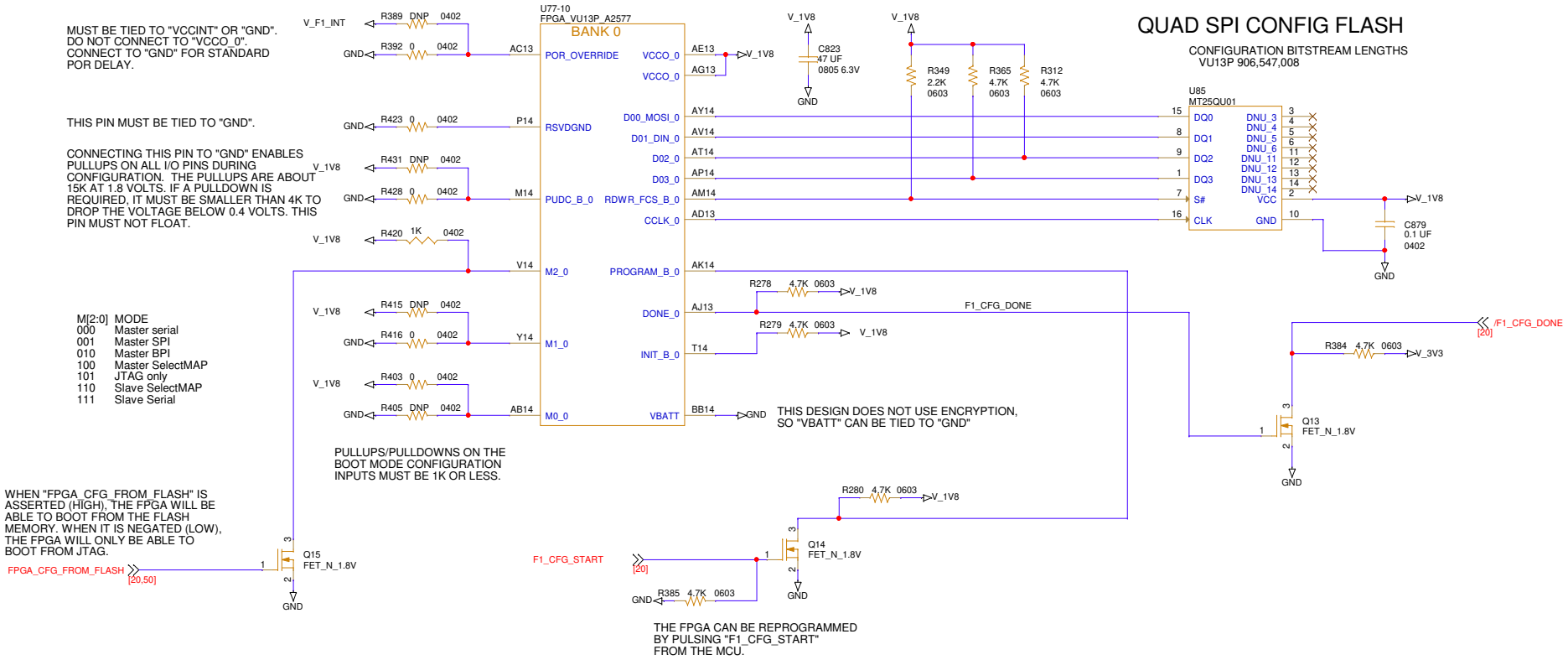


REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

APOLLO CM v3		
Title: 5.03: FPGA#1 GTY TRANSCEIVER POWER		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 39 of 78	

5.04: FPGA#1 CONFIGURATION



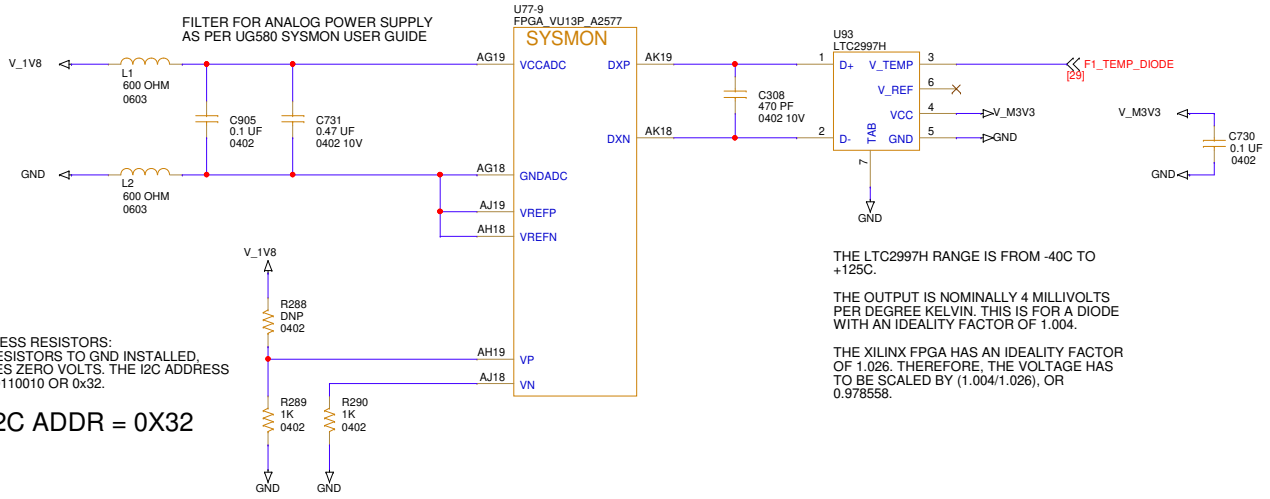
APOLLO CM v3		
Title: 5.04: FPGA#1 CONFIGURATION		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 40 of 78	

5.05: FPGA#1 SYSTEM MONITOR

FOR THE VU9P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0 AND SLR2.

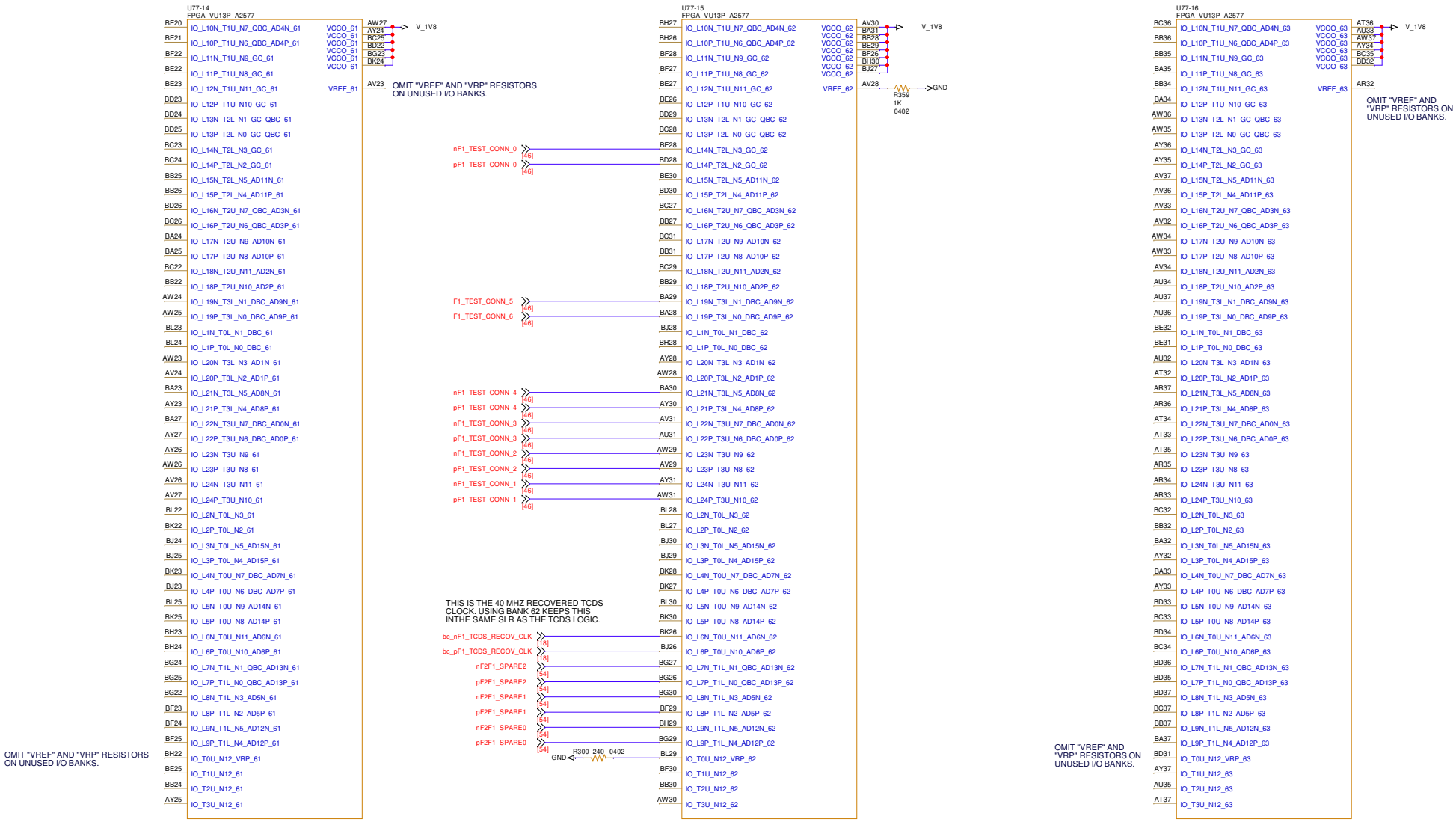
FOR THE VU13P, THE MASTER SLR INDEX IS SLR1, AND THE SLAVE SLR INDEX ARE SLR0, SLR2, AND SLR3.

ONLY THE MASTER SLR IS ACCESSABLE FROM THE I2C CONNECTIONS.



APOLLO CM v3		
Title: 5.05: FPGA#1 SYSTEM MONITOR		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 41 of 78	

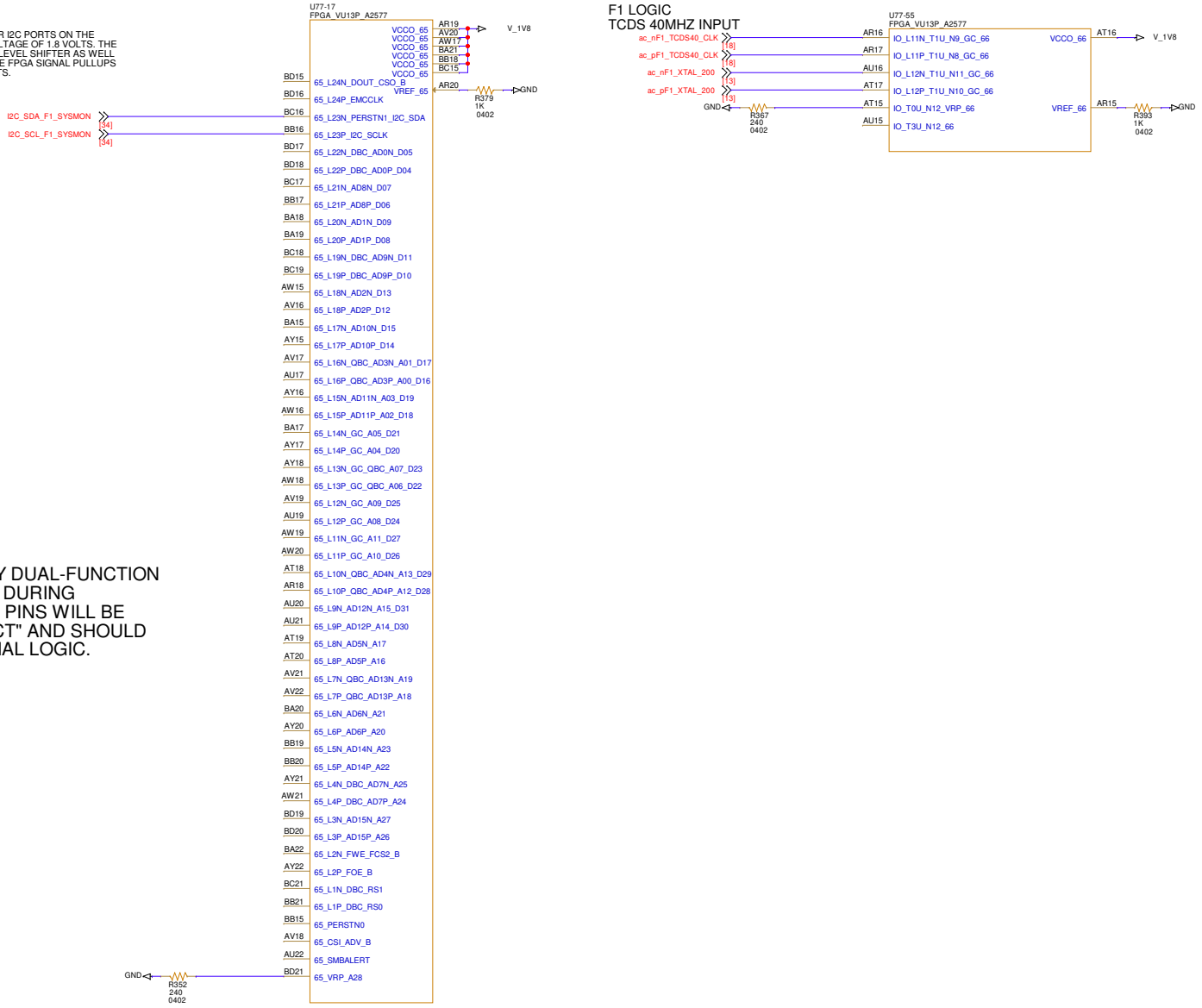
5.06 FPGA#1 I/O SLR0



APOLLO CM v3	
Title	5.06 FPGA#1 I/O SLR0
Size	Document Number 6089-127 Rev A
Date: Tuesday, January 02, 2024	Sheet 42 of 78

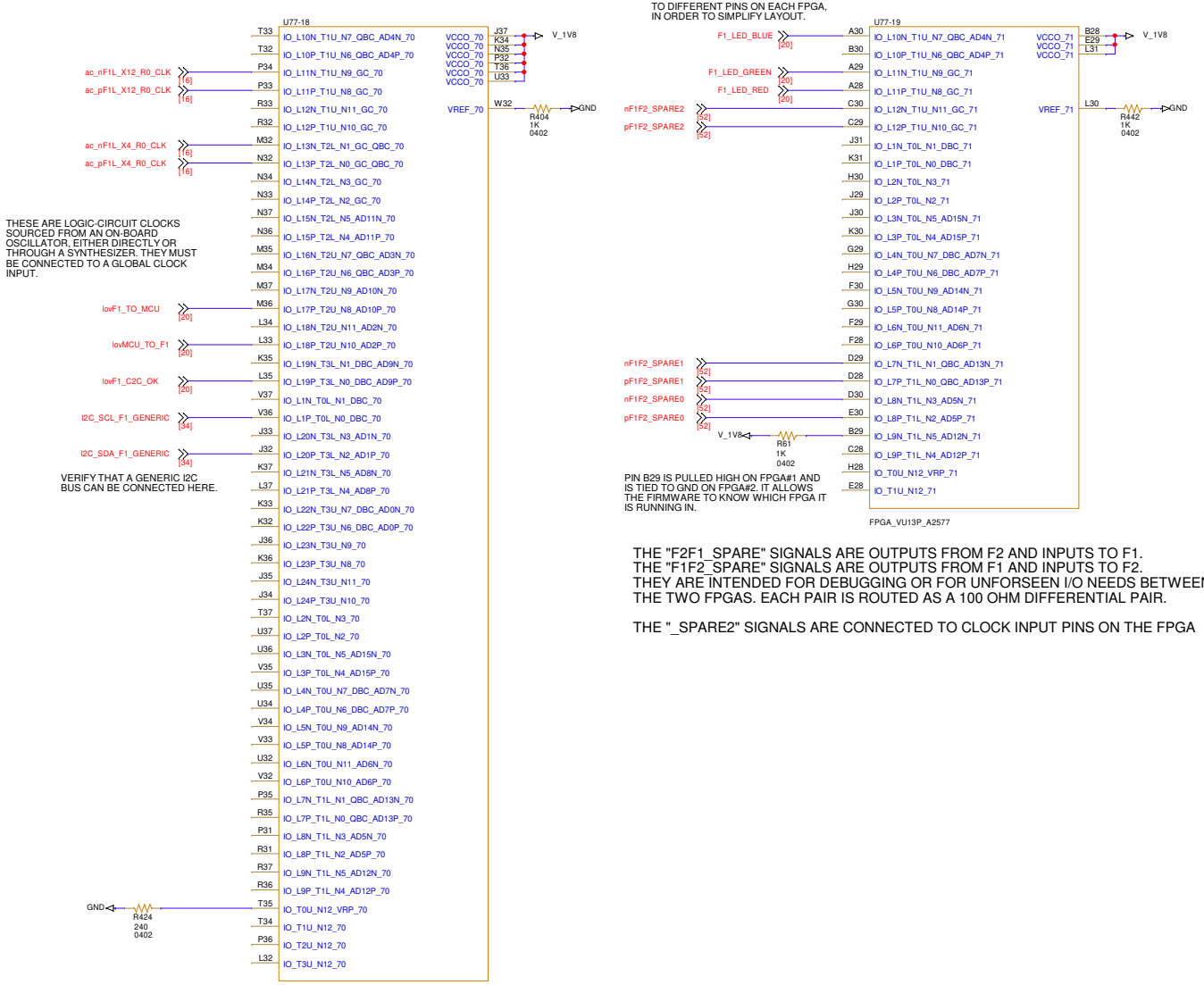
THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.



APOLLO CM v3		
Title: 5.07 FPGA#1 I/O SLR1		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 43 of 78	

5.08: FPGA#1 I/O SLR2



THE "F2F1_SPARE" SIGNALS ARE OUTPUTS FROM F2 AND INPUTS TO F1.
THE "F1F2_SPARE" SIGNALS ARE OUTPUTS FROM F1 AND INPUTS TO F2.
THEY ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE FPGA

APOLLO CM v3		
Title: 5.08: FPGA#1 I/O SLR2		
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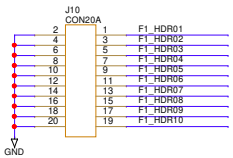
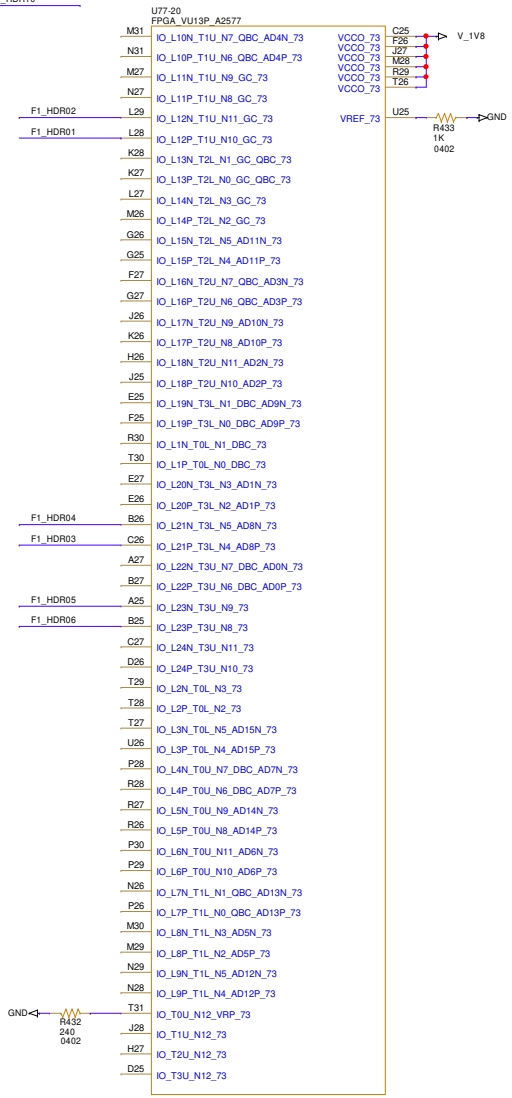
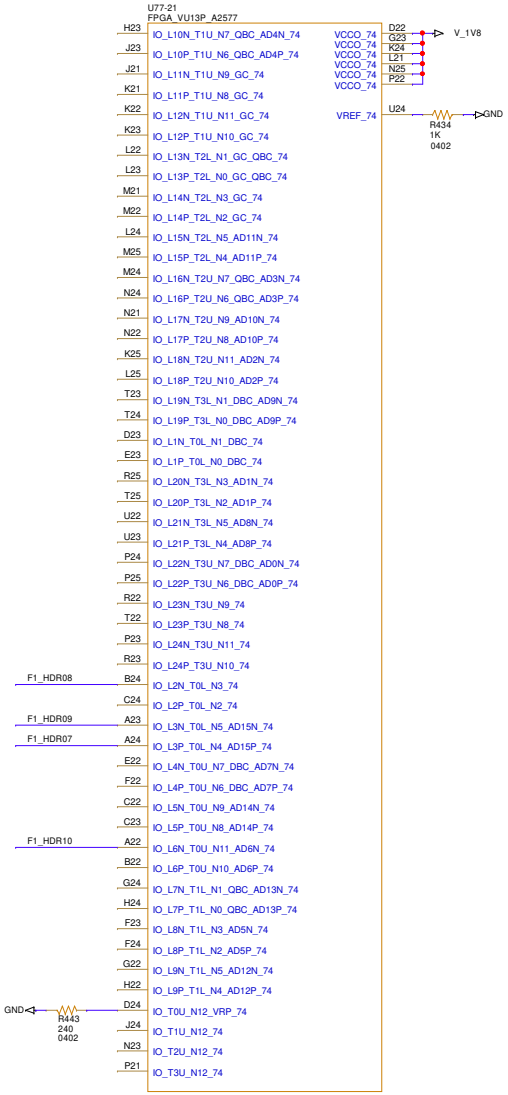
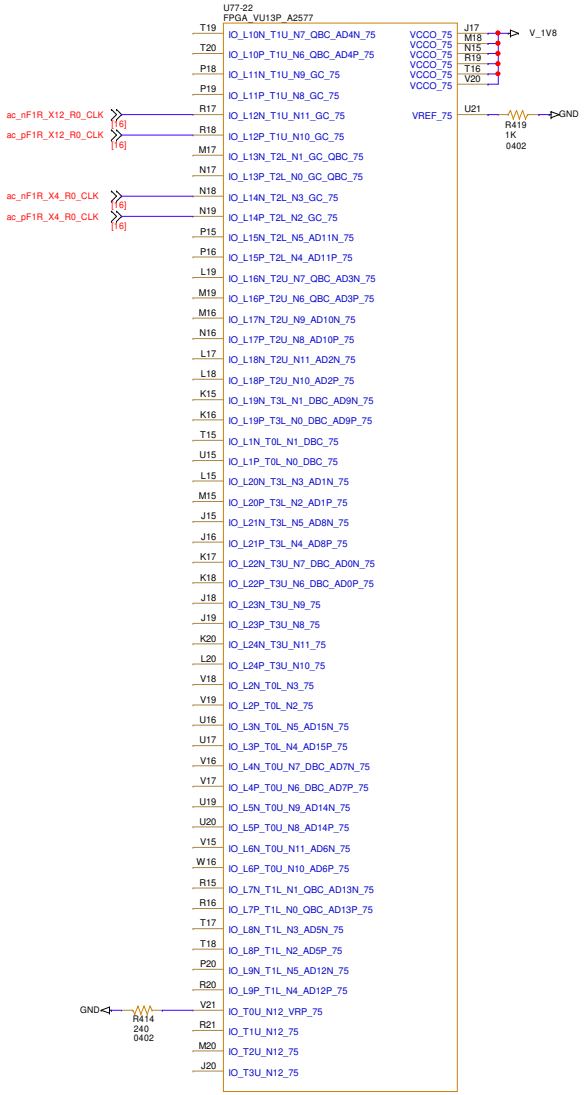
5.09: FPGA#1 I/O SLR3

THE "F1_HDRnn" SIGNALS ARE CONNECTED FROM THE FPGA TO PADS ON THE BOTTOM SIDE OF THE BOARD. A 20-PIN HEADER CAN BE ATTACHED. THESE SIGNALS ARE FOR DEBUGGING, OR FUTURE USE. HDR01 AND HDR02 ARE CONNECTED TO CLOCK-CAPABLE INPUTS.









APOLLO CM v3		
Title: 5.09: FPGA#1 I/O SLR3		
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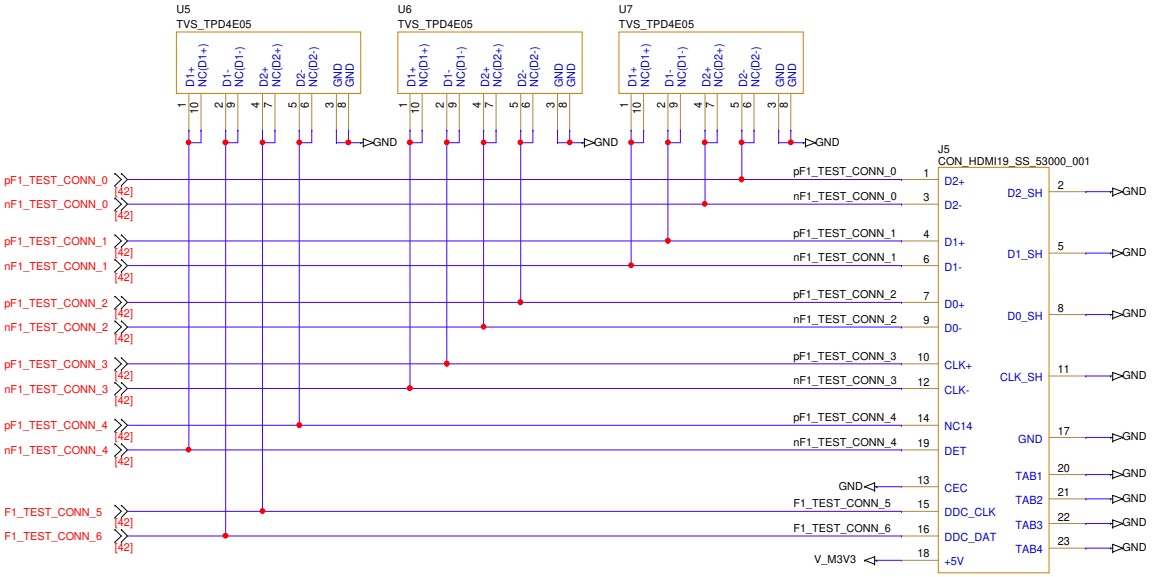
5.10: FPGA#1 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

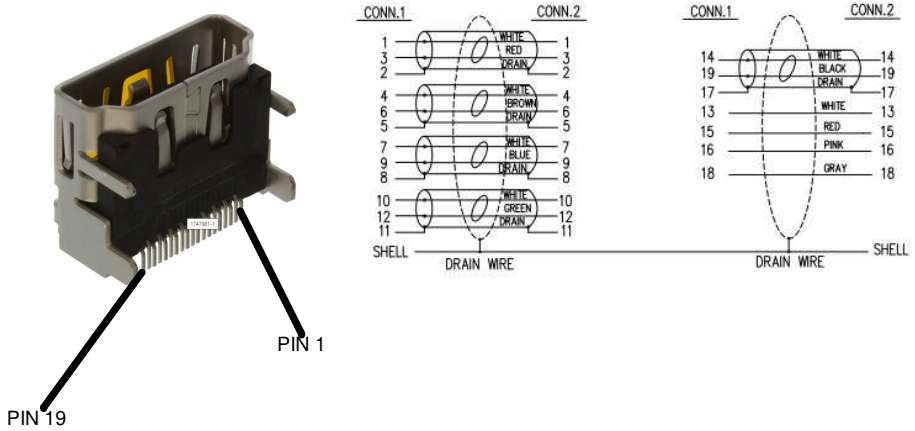
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F1_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.

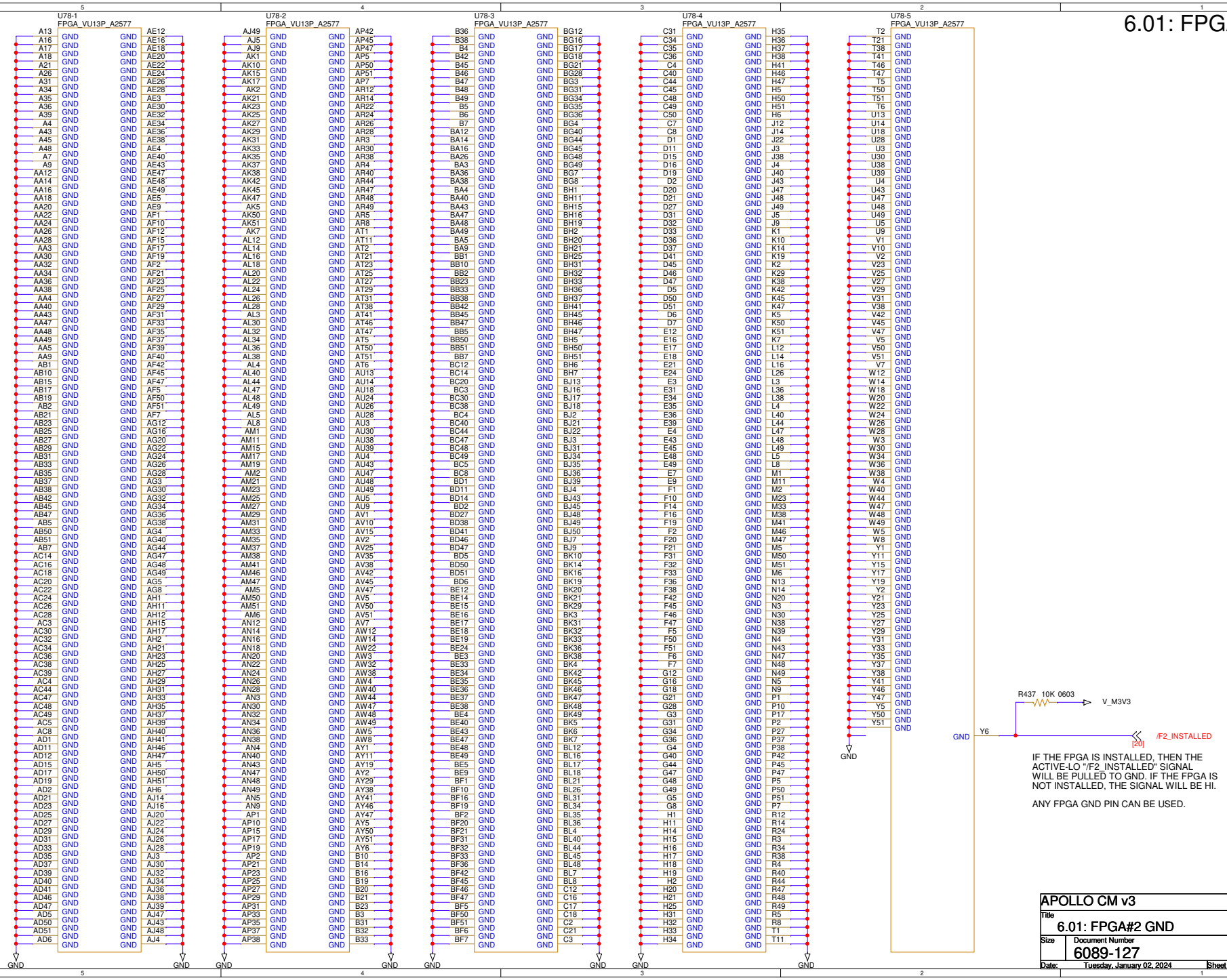


PIN ASSIGNMENT



APOLLO CM v3		
Title: 5.10: FPGA#1 TEST CONNECTOR		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 46 of 78	

6.01: FPGA#2 GND



IF THE FPGA IS INSTALLED, THEN THE ACTIVE-LO "/F2_INSTALLED" SIGNAL WILL BE PULLED TO GND. IF THE FPGA IS NOT INSTALLED, THE SIGNAL WILL BE HI.

ANY FPGA GND PIN CAN BE USED.

APOLLO CM v3		
Title: 6.01: FPGA#2 GND		
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6.02: FPGA#2 POWER INTERNAL

VCCINT MUST BE 0.85V.

U78-6
FPGA_VU13P_A2577

V_F2_INT → VCCINT → V_F2_INT

AA17	VCCINT	VCCINT	AK26
AA19	VCCINT	VCCINT	AK28
AA21	VCCINT	VCCINT	AK30
AA23	VCCINT	VCCINT	AL17
AA25	VCCINT	VCCINT	AL19
AA27	VCCINT	VCCINT	AL21
AA29	VCCINT	VCCINT	AL23
AA31	VCCINT	VCCINT	AL25
AB16	VCCINT	VCCINT	AL27
AB18	VCCINT	VCCINT	AL29
AB20	VCCINT	VCCINT	AL31
AB22	VCCINT	VCCINT	AM18
AB24	VCCINT	VCCINT	AM20
AB26	VCCINT	VCCINT	AM22
AB28	VCCINT	VCCINT	AM24
AB30	VCCINT	VCCINT	AM26
AC17	VCCINT	VCCINT	AM28
AC19	VCCINT	VCCINT	AM30
AC21	VCCINT	VCCINT	AN17
AC23	VCCINT	VCCINT	AN19
AC25	VCCINT	VCCINT	AN21
AC27	VCCINT	VCCINT	AN23
AC29	VCCINT	VCCINT	AN25
AC31	VCCINT	VCCINT	AN27
AD16	VCCINT	VCCINT	AN29
AD18	VCCINT	VCCINT	AN31
AD20	VCCINT	VCCINT	AP18
AD22	VCCINT	VCCINT	AP20
AD24	VCCINT	VCCINT	AP22
AD26	VCCINT	VCCINT	AP24
AD28	VCCINT	VCCINT	AP26
AD30	VCCINT	VCCINT	AP28
AE17	VCCINT	VCCINT	AP30
AE19	VCCINT	VCCINT	AR21
AE21	VCCINT	VCCINT	AR23
AE23	VCCINT	VCCINT	AR25
AE25	VCCINT	VCCINT	AR27
AE27	VCCINT	VCCINT	AR29
AE29	VCCINT	VCCINT	AR31
AE31	VCCINT	VCCINT	AT22
AF16	VCCINT	VCCINT	AT24
AF18	VCCINT	VCCINT	AT26
AF20	VCCINT	VCCINT	AT28
AF22	VCCINT	VCCINT	AT30
AF24	VCCINT	VCCINT	AU23
AF26	VCCINT	VCCINT	AU25
AF28	VCCINT	VCCINT	AU27
AF30	VCCINT	VCCINT	AU29
AG17	VCCINT	VCCINT	U27
AG21	VCCINT	VCCINT	U29
AG23	VCCINT	VCCINT	U31
AG25	VCCINT	VCCINT	V22
AG27	VCCINT	VCCINT	V24
AG29	VCCINT	VCCINT	V26
AG31	VCCINT	VCCINT	V28
AH16	VCCINT	VCCINT	V30
AH20	VCCINT	VCCINT	W17
AH22	VCCINT	VCCINT	W19
AH24	VCCINT	VCCINT	W21
AH26	VCCINT	VCCINT	W23
AH28	VCCINT	VCCINT	W25
AH30	VCCINT	VCCINT	W27
AJ17	VCCINT	VCCINT	W29
AJ21	VCCINT	VCCINT	W31
AJ23	VCCINT	VCCINT	Y18
AJ25	VCCINT	VCCINT	Y20
AJ27	VCCINT	VCCINT	Y22
AJ29	VCCINT	VCCINT	Y24
AJ31	VCCINT	VCCINT	Y26
AK16	VCCINT	VCCINT	Y28
AK20	VCCINT	VCCINT	Y30
AK22	VCCINT		
AK24	VCCINT		

VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).

U78-7
FPGA_VU13P_A2577

V_F2_INT → VCCINT_IO → VCCAUX → V_1V8

AA33	VCCINT_IO	VCCAUX	AA37
AB32	VCCINT_IO	VCCAUX	AC37
AC33	VCCINT_IO	VCCAUX	AD36
AD32	VCCINT_IO	VCCAUX	AD38
AE33	VCCINT_IO	VCCAUX	AE37
AF32	VCCINT_IO	VCCAUX	AE39
AG33	VCCINT_IO	VCCAUX	AF36
AH32	VCCINT_IO	VCCAUX	AF38
AJ33	VCCINT_IO	VCCAUX	AG37
AK32	VCCINT_IO	VCCAUX	AG39
AL33	VCCINT_IO	VCCAUX	AH38
AM32	VCCINT_IO	VCCAUX	AJ37
AN33	VCCINT_IO	VCCAUX	AL37
AP32	VCCINT_IO	VCCAUX	AN37
W33	VCCINT_IO	VCCAUX	W37
Y32	VCCINT_IO	VCCAUX	
	VCCINT_IO		

VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

V_F2_INT → VCCBRAM → VCCAUX_IO → V_1V8

AA15	VCCBRAM	VCCAUX_IO	AA35
AC15	VCCBRAM	VCCAUX_IO	AB34
AD14	VCCBRAM	VCCAUX_IO	AB36
AE15	VCCBRAM	VCCAUX_IO	AC35
AF14	VCCBRAM	VCCAUX_IO	AD34
AG15	VCCBRAM	VCCAUX_IO	AE35
AH14	VCCBRAM	VCCAUX_IO	AF34
AJ15	VCCBRAM	VCCAUX_IO	AG35
AL15	VCCBRAM	VCCAUX_IO	AH34
AM16	VCCBRAM	VCCAUX_IO	AH36
AN15	VCCBRAM	VCCAUX_IO	AJ35
AP16	VCCBRAM	VCCAUX_IO	AK34
W15	VCCBRAM	VCCAUX_IO	AK36
Y16	VCCBRAM	VCCAUX_IO	AL35
	VCCBRAM	VCCAUX_IO	AM34
		VCCAUX_IO	AM36
		VCCAUX_IO	AN35
		VCCAUX_IO	AP34
		VCCAUX_IO	AP36
		VCCAUX_IO	W35
		VCCAUX_IO	Y34
		VCCAUX_IO	Y36

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).

V_1V8

C1056	C1062	C737	C739	C887
47 UF	47 UF	47 UF	47 UF	47 UF
0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V

GND

V_1V8

C1028	C1003	C786	C781	C888
10 UF	10 UF	10 UF	10 UF	10 UF
0402 4V	0402 4V	0402 4V	0402 4V	0402 4V

GND

VCCAUX / VCCAUXIO / VCCO
ALL I/O BANKS ARE POWERED AT 1.8 VOLTS.

V_F2_INT

C33	C497	C32	C31	C234
330 UF	330 UF	330 UF	330 UF	330 UF
2.5V 1210	2.5V 1210	2.5V 1210	2.5V 1210	2.5V 1210

GND

V_F2_INT

C938	C928	C911	C896	C1061	C1060	C1059	C1058	C738	C1057	C740
100 UF	100 UF	100 UF	100 UF	100 UF	100 UF	100 UF	100 UF	100 UF	100 UF	100 UF
0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V

GND

V_F2_INT

C937	C924	C901	C891	C736	C735	C734
47 UF	47 UF	47 UF	47 UF	47 UF	47 UF	47 UF
0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V	0805 6.3V

GND

V_F2_INT

C941	C930	C913	C899	C933	C916	C908	C898	C1033	C1032
10 UF	10 UF	10 UF	10 UF	10 UF	10 UF	10 UF	10 UF	10 UF	10 UF
0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V

GND

V_F2_INT

C1031	C1002	C785	C753	C750	C782	C1037	C787
10 UF	10 UF	10 UF	10 UF	10 UF	10 UF	10 UF	10 UF
0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V	0402 4V

GND

VCCINT / VCCINT_IO / VCCBRAM

BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"UG583 UltraScale Architecture PCB Design"

APOLLO CM v3

Title: 6.02: FPGA#2 POWER INTERNAL

Size	Document Number	Rev
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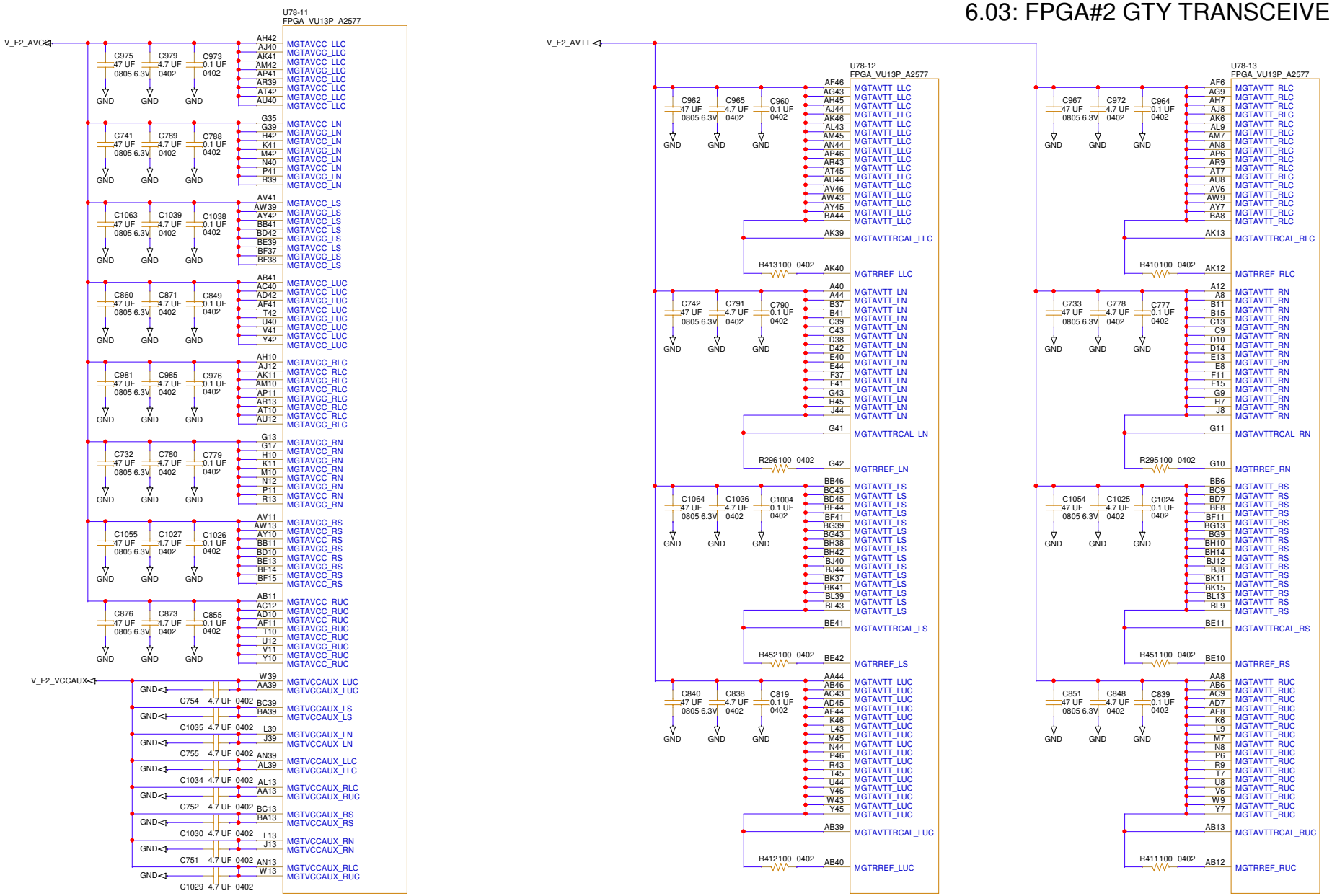
Date: Saturday, December 30, 2023 Sheet 48 of 78

6.03: FPGA#2 GTY TRANSCEIVER POWER

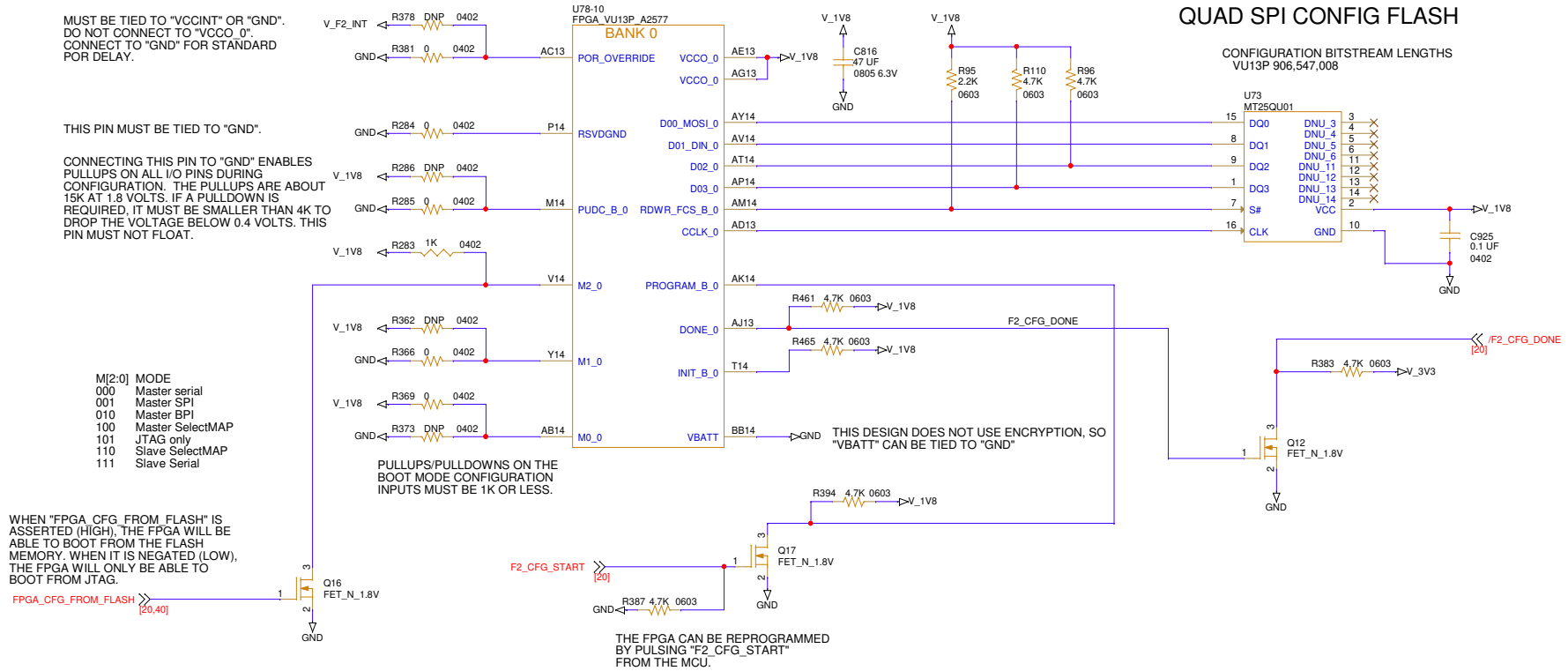


REFER TO THE GTY USER GUIDE FOR DETAILS ON TRACE ROUTING FOR THE MGTRREF RESISTOR.

PLACE CAPACITORS AND RESISTORS THAT ARE ON THIS SHEET NEAR THE BGA PINS.

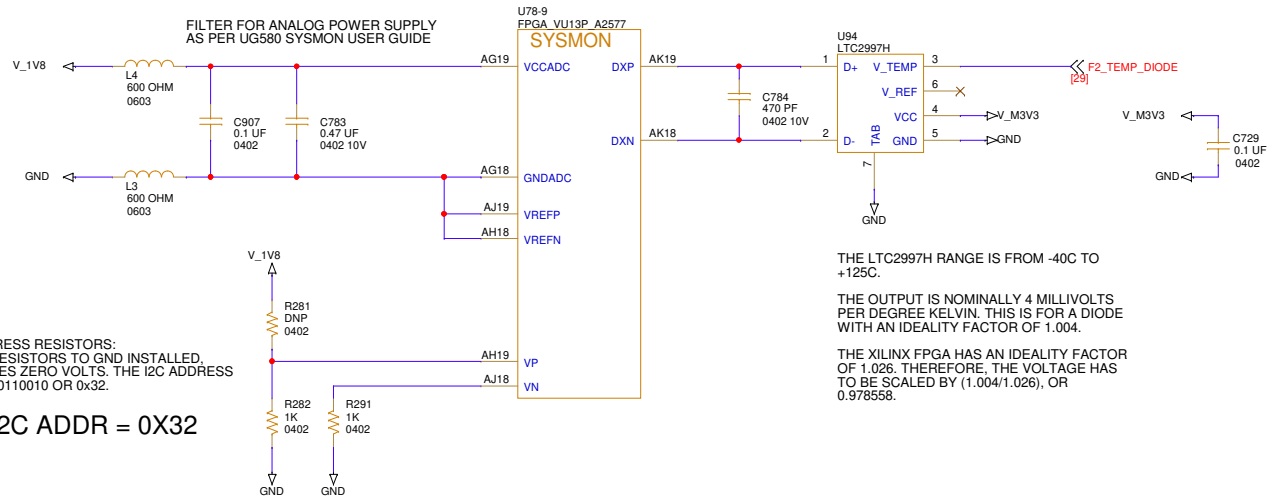
APOLLO CM v3		
Title: 6.03: FPGA#2 GTY TRANSCEIVER POWER		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 49 of 78	

6.04: FPGA#2 CONFIGURATION



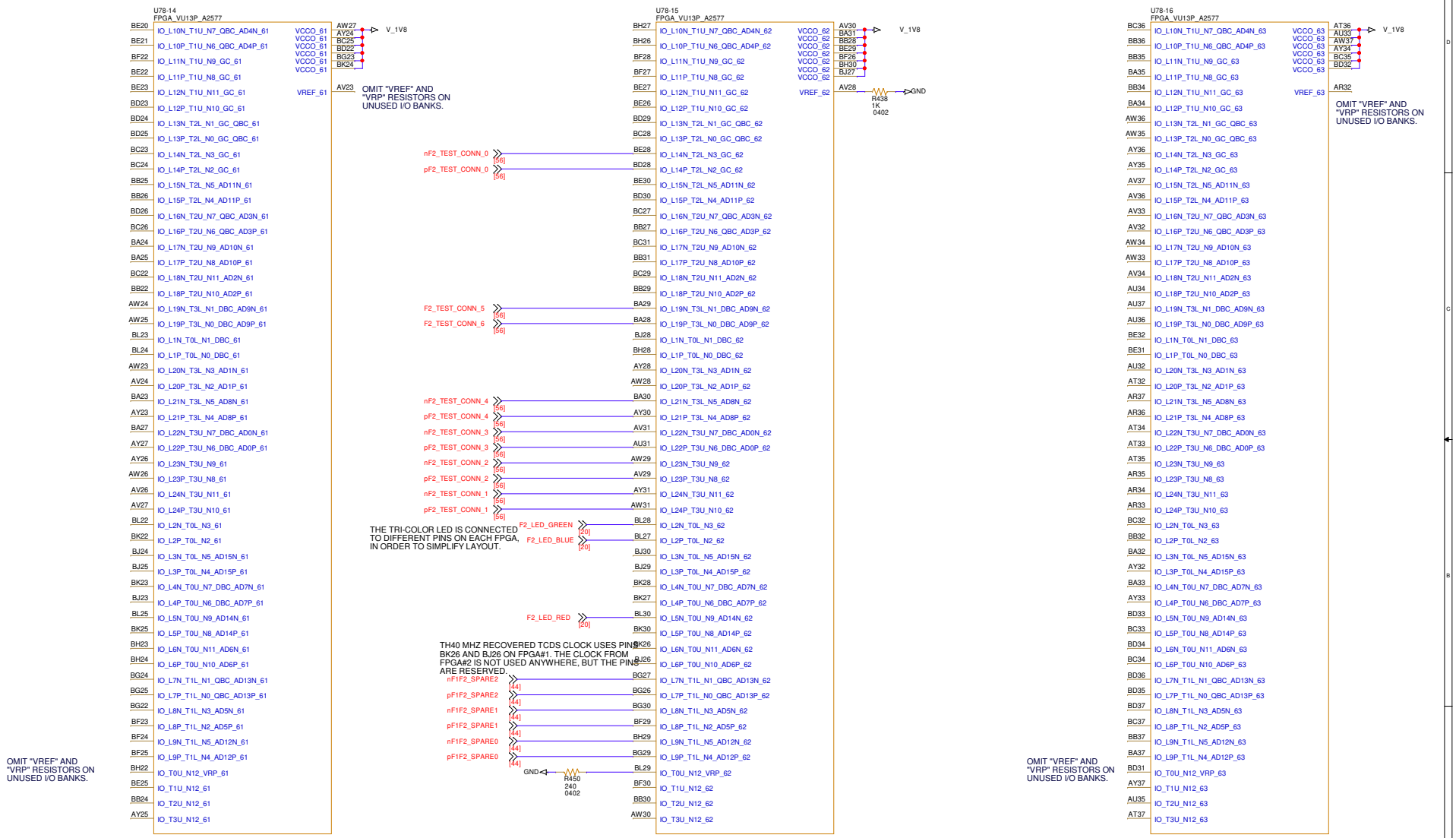
APOLLO CM v3	
Title	6.04: FPGA#2 CONFIGURATION
Size	Document Number 6089-127 Rev A
Date:	Tuesday, January 02, 2024 Sheet 50 of 78

6.05: FPGA#2 SYSTEM MONITOR



APOLLO CM v3		
Title: 6.05: FPGA#2 SYSTEM MONITOR		
Size	Document Number: 6089-127	Rev: A
Date: Tuesday, January 02, 2024	Sheet 51 of 78	

6.06 FPGA#2 I/O SLR0



APOLLO CM v3	
Title	6.06 FPGA#2 I/O SLR0
Size	Document Number 6089-127 Rev A
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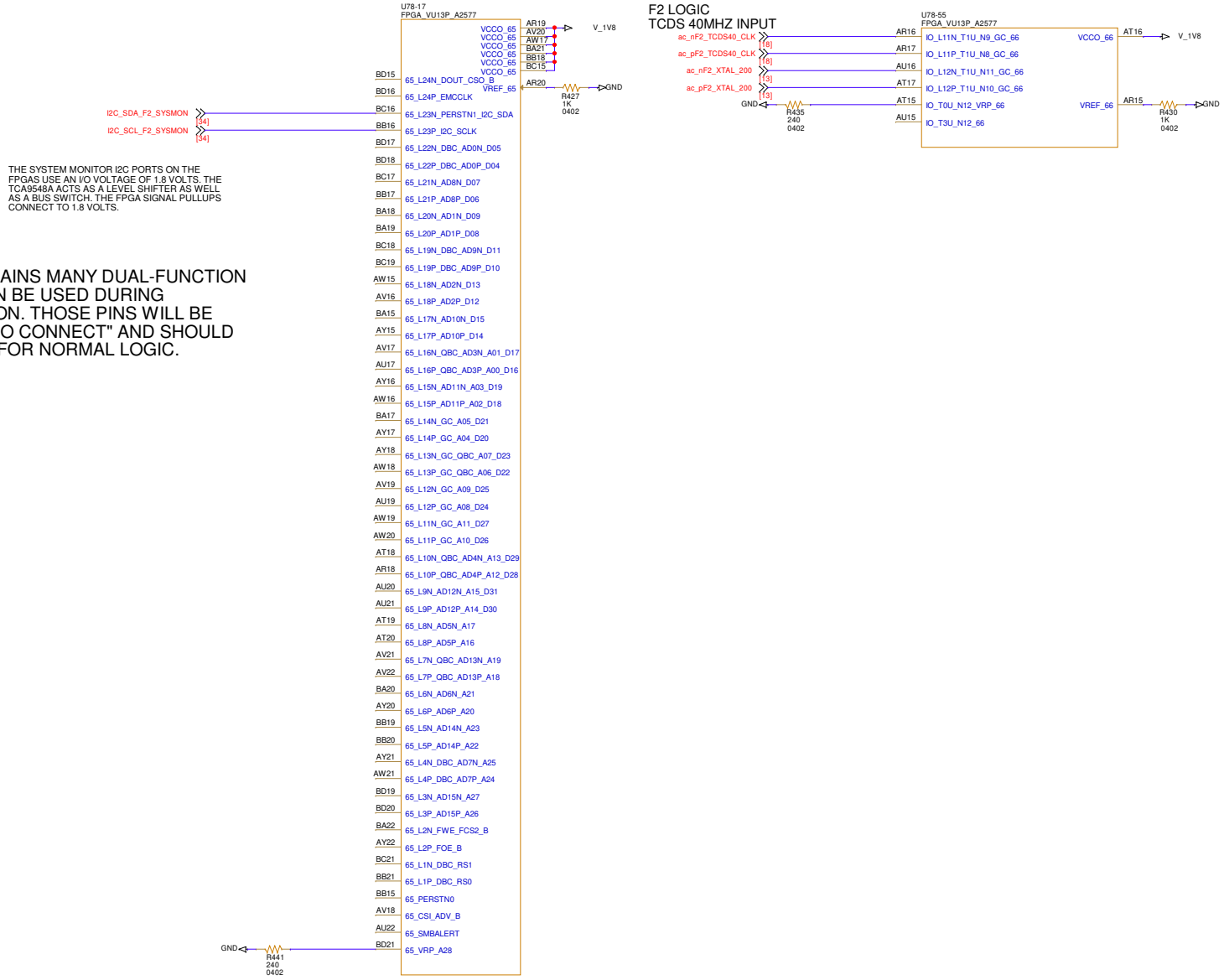
6.07 FPGA#2 I/O SLR1



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

APOLLO CM v3		
Title: 6.07 FPGA#2 I/O SLR1		
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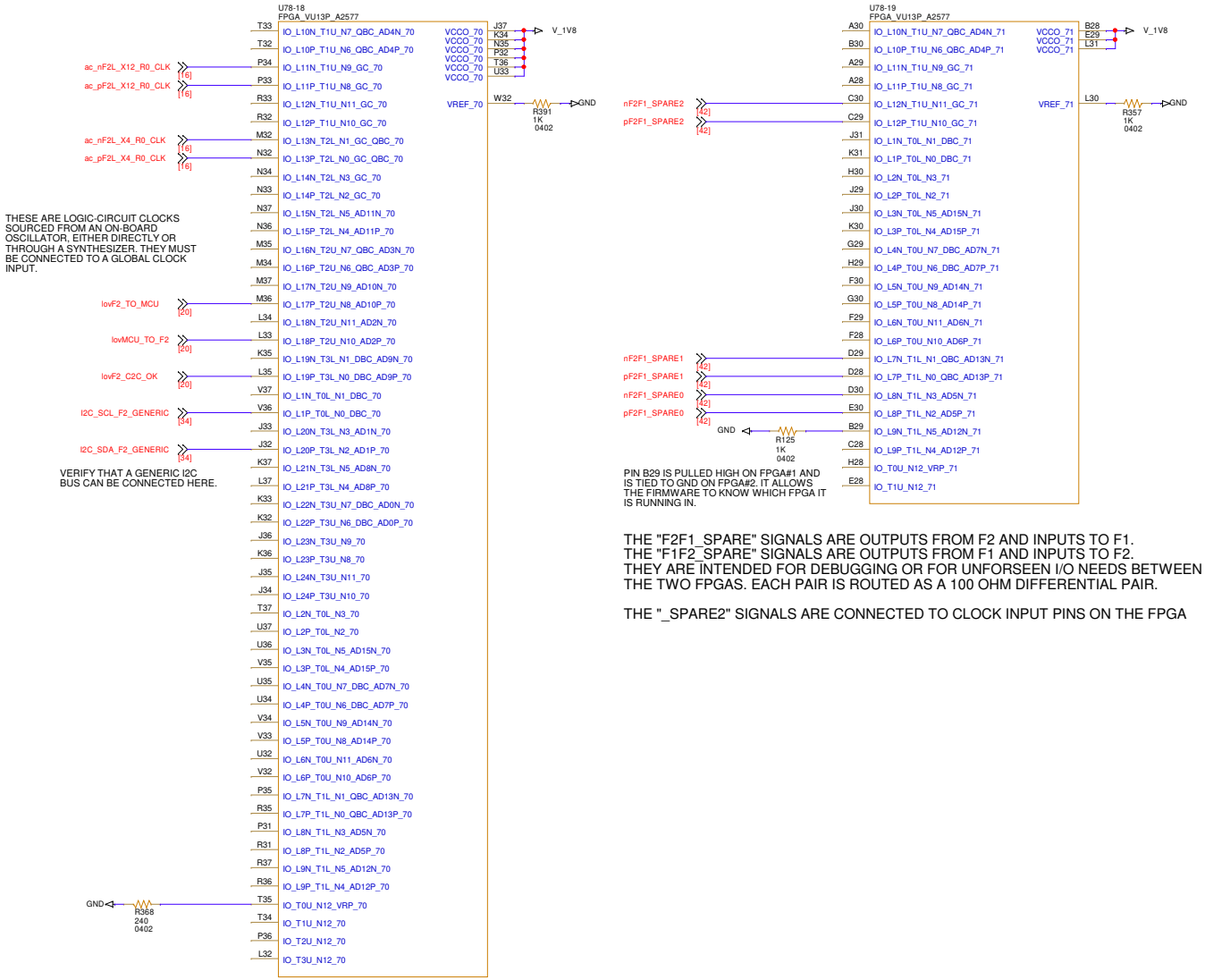
6.08: FPGA#2 I/O SLR2



APOLLO CM v3		
Title: 6.08: FPGA#2 I/O SLR2		
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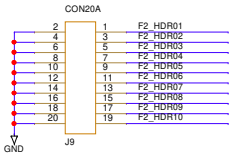
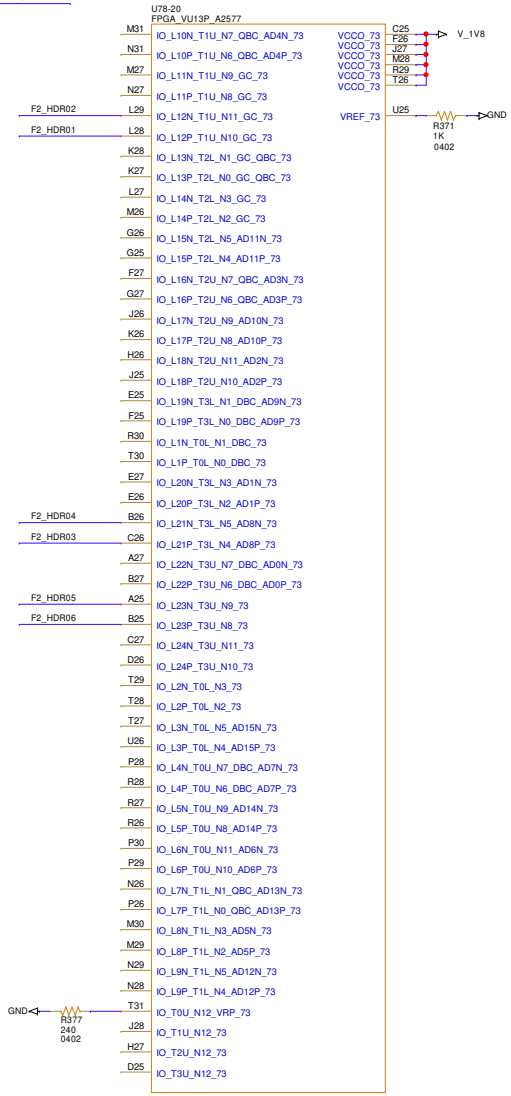
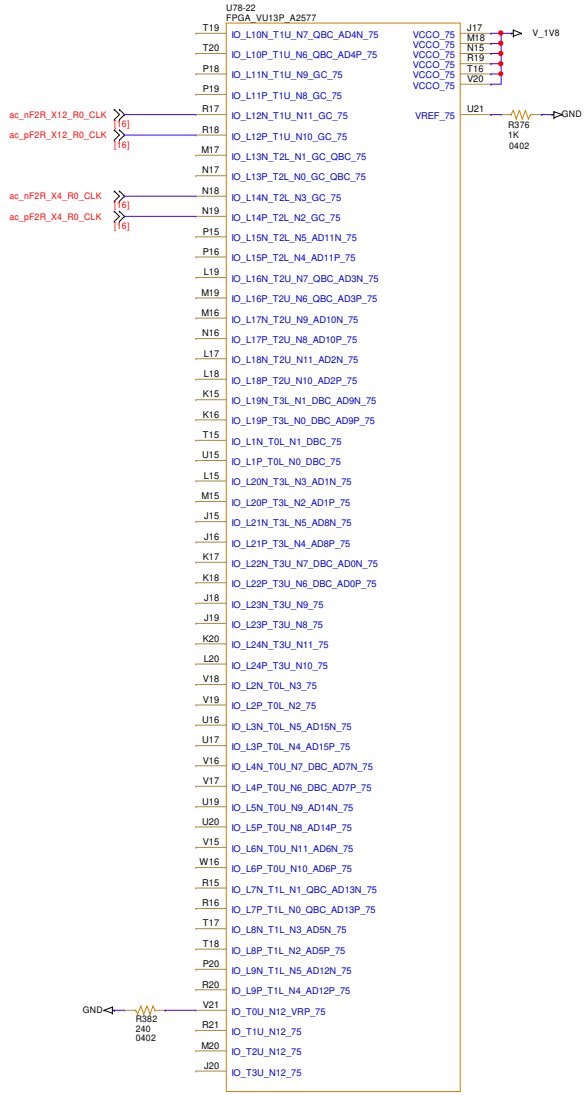
6.09: FPGA#2 I/O SLR3

THE "F2_HDRnn" SIGNALS ARE CONNECTED FROM THE FPGA TO PADS ON THE BOTTOM SIDE OF THE BOARD. A 20-PIN HEADER CAN BE ATTACHED. THESE SIGNALS ARE FOR DEBUGGING, OR FUTURE USE. HDR01 AND HDR02 ARE CONNECTED TO CLOCK-CAPABLE INPUTS.







APOLLO CM v3		
Title: 6.09: FPGA#2 I/O SLR3		
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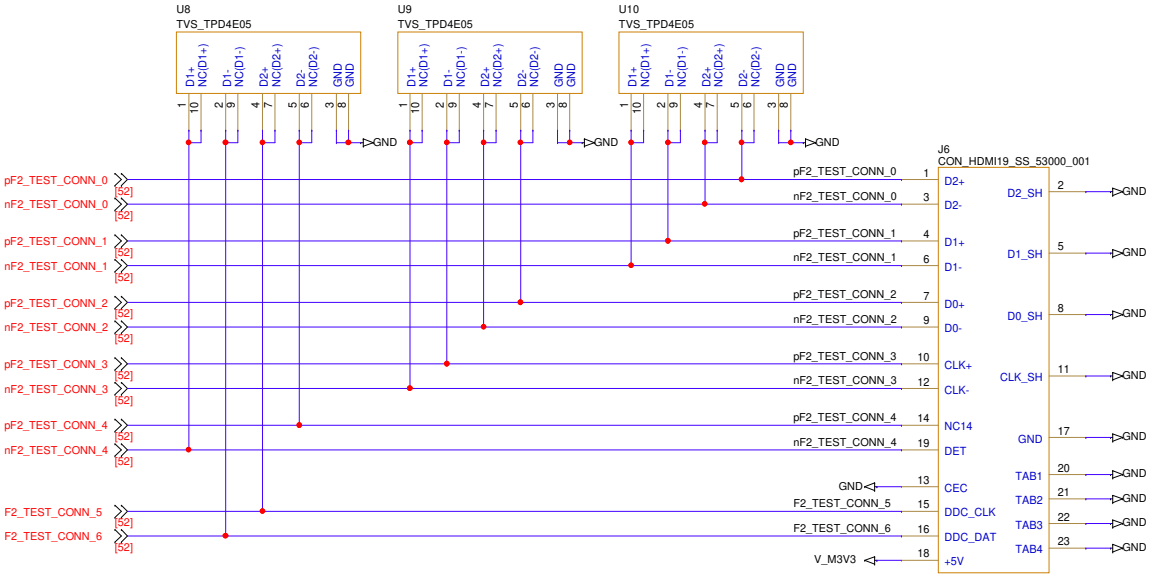
6.10 FPGA#2 TEST CONNECTOR

THIS CONNECTOR IS LOCATED ON THE FRONT PANEL. IT IS A RE-PURPOSED 19-PIN HDMI CONNECTOR. IT WAS CHOSEN BECAUSE THE PINS ARE RECESSED AND CANNOT BE TOUCHED, AND BECAUSE THE STANDARD CABLES OFFER 5 HIGH-SPEED SHIELDED PAIRS AND 4 UNCOMMITTED WIRES.

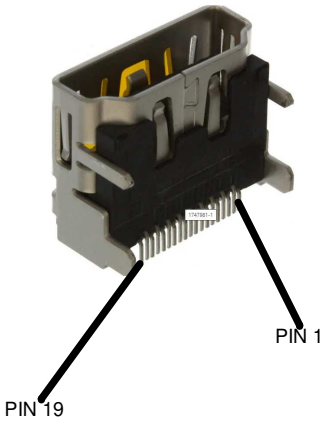
TWO UNCOMMITTED WIRES ARE USED FOR SINGLE-ENDED SIGNALS, ONE FOR 3.3 VOLTS, AND ONE FOR GND.

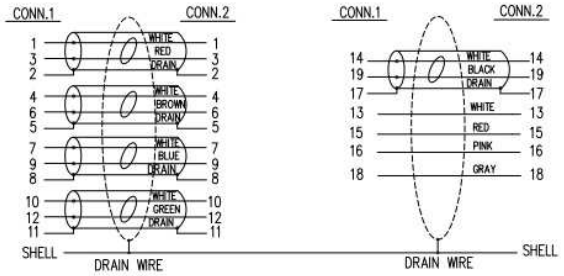
THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "F2_TEST_CONN_0" SIGNAL IS CONNECTED TO GLOBAL CLOCK CAPABLE INPUT PINS.



PIN ASSIGNMENT





APOLLO CM v3		
Title: 6.10 FPGA#2 TEST CONNECTOR		
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QUAD "L" WIRING FOR FPGA#1 CAN BE FOUND ON SHEET 2.13: C2C AND TCDS QUADS

APOLLO CM v3		
Title: 7.01: FPGA#1 SM C2C ON QUAD L		
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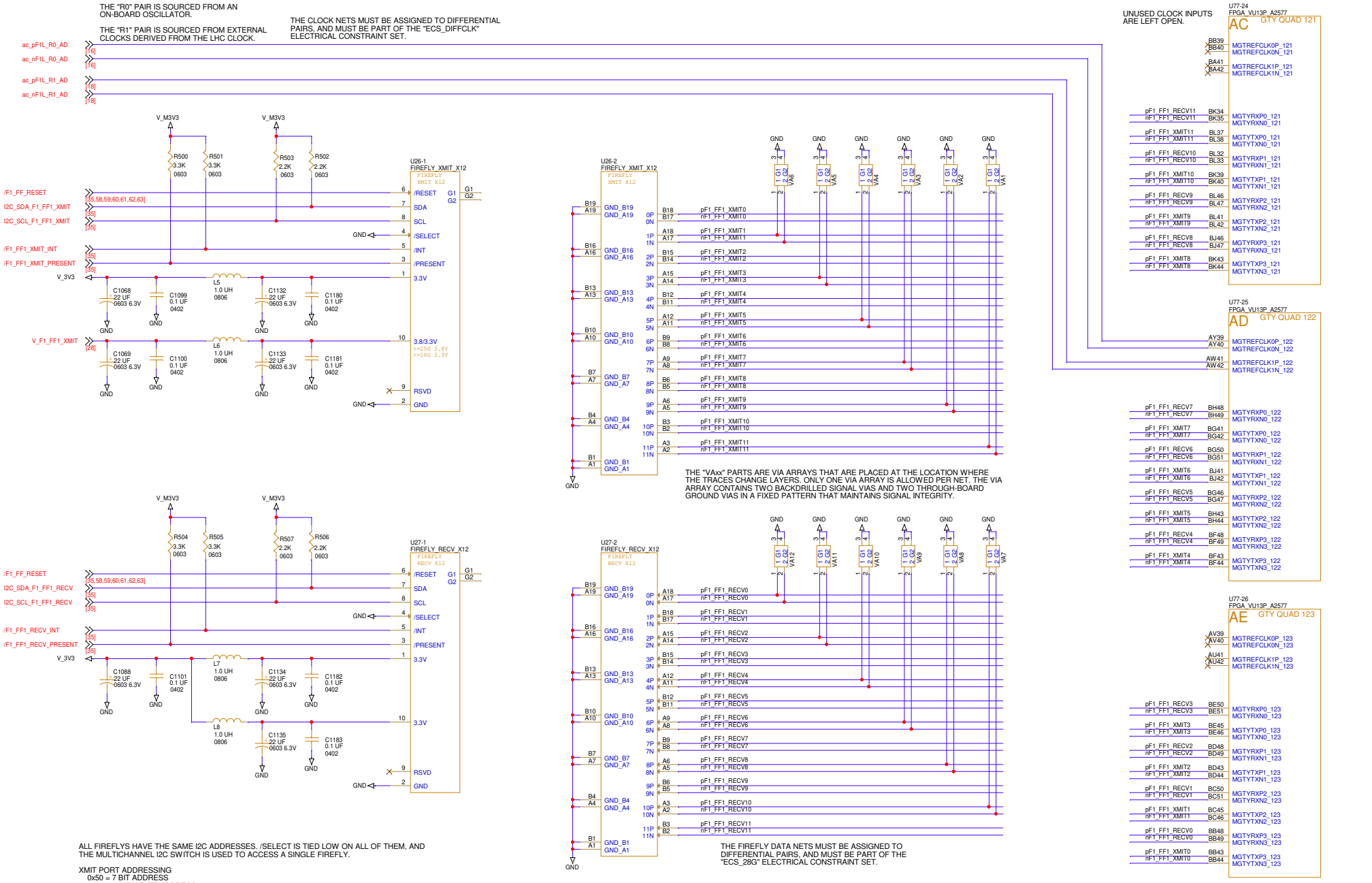
7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM v3	
Title	7.02: FPGA#1 FF#1 X12 ON QUADS AC AD AE
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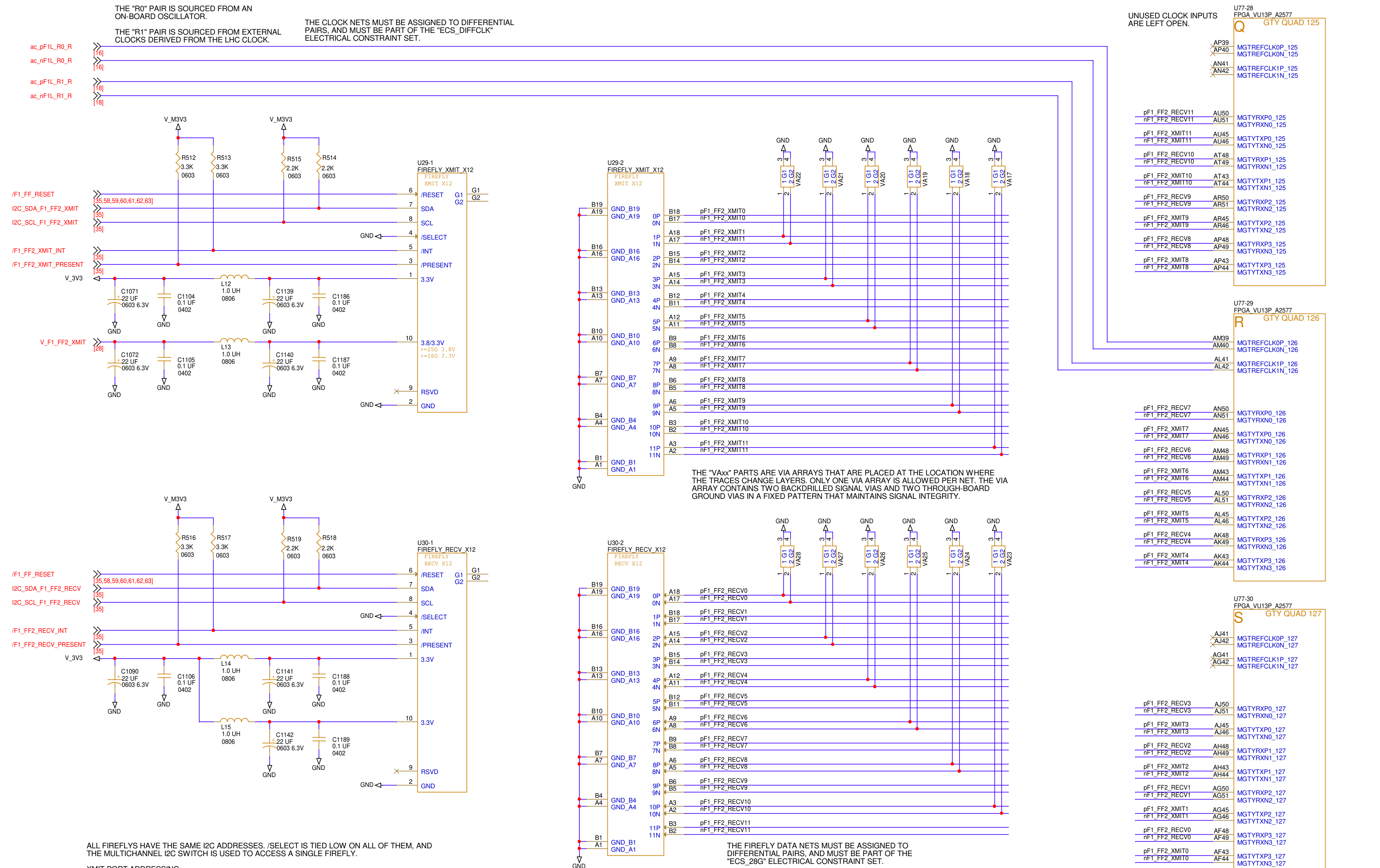
7.03: FPGA#1 FF#2 X12 ON QUADS Q R S



ac_pF1L_R0_R
ac_nF1L_R0_R
ac_pF1L_R1_R
ac_nF1L_R1_R
V_M3V3
R512 3.3K 0603
R513 3.3K 0603
R515 2.2K 0603
R514 2.2K 0603
U29-1 FIREFLY_XMIT_X12
/F1_FF_RESET
I2C_SDA_F1_FF2_XMIT
I2C_SCL_F1_FF2_XMIT
/F1_FF2_XMIT_INT
/F1_FF2_XMIT_PRESENT
V_3V3
V_F1_FF2_XMIT
/RESET
SDA
SCL
/SELECT
/INT
/PRESENT
3.3V
3.8/3.3V
RSVD
GND
L12 1.0 UH 0806
L13 1.0 UH 0806
C1071 22 UF 0603 6.3V
C1104 0.1 UF 0402
C1139 22 UF 0603 6.3V
C1186 0.1 UF 0402
C1072 22 UF 0603 6.3V
C1105 0.1 UF 0402
C1140 22 UF 0603 6.3V
C1187 0.1 UF 0402
U29-2 FIREFLY_XMIT_X12
U30-1 FIREFLY_RECV_X12
U30-2 FIREFLY_RECV_X12
/F1_FF2_RECV_INT
/F1_FF2_RECV_PRESENT
I2C_SDA_F1_FF2_RECV
I2C_SCL_F1_FF2_RECV
R516 3.3K 0603
R517 3.3K 0603
R519 2.2K 0603
R518 2.2K 0603
L14 1.0 UH 0806
L15 1.0 UH 0806
C1090 22 UF 0603 6.3V
C1106 0.1 UF 0402
C1141 22 UF 0603 6.3V
C1188 0.1 UF 0402
C1142 22 UF 0603 6.3V
C1189 0.1 UF 0402
pF1_FF2_XMIT0 … pF1_FF2_XMIT11
nF1_FF2_XMIT0 … nF1_FF2_XMIT11
pF1_FF2_RECV0 … pF1_FF2_RECV11
nF1_FF2_RECV0 … nF1_FF2_RECV11
VA17 VA18 VA19 VA20 VA21 VA22
VA23 VA24 VA25 VA26 VA27 VA28
U77-28 FPGA_VU13P_A2577 GTY QUAD 125
U77-29 FPGA_VU13P_A2577 GTY QUAD 126
U77-30 FPGA_VU13P_A2577 GTY QUAD 127
MGTREFCLK0P_125
MGTREFCLK0N_125
MGTREFCLK1P_125
MGTREFCLK1N_125
MGTREFCLK0P_126
MGTREFCLK0N_126
MGTREFCLK1P_126
MGTREFCLK1N_126
MGTREFCLK0P_127
MGTREFCLK0N_127
MGTREFCLK1P_127
MGTREFCLK1N_127
GND

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

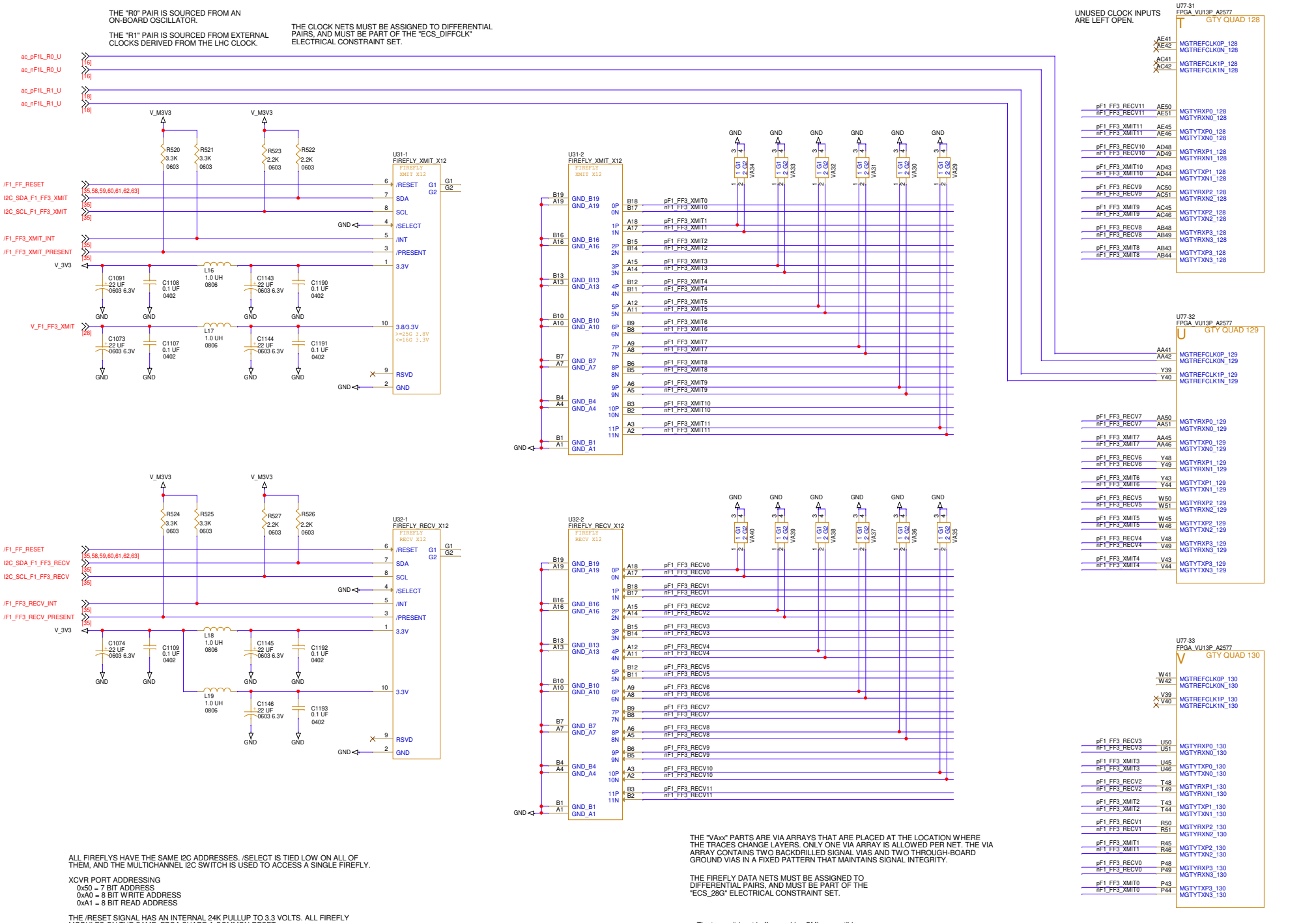
7.04: FPGA#1 FF#3 X12 ON QUADS T U V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM v3		
Title: 7.04: FPGA#1 FF#3 X12 ON QUADS T U V		
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7.05: FPGA#1 FF#4 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF1L_R0_Y [16]
ac_nF1L_R0_Y [16]
ac_pF1L_R1_Y [18]
ac_nF1L_R1_Y [18]

U77-35 FPGA_VU13P_A2577 — X — GTY QUAD 132
R41 MGTREFCLK0P_132
R42 MGTREFCLK0N_132
P39 MGTREFCLK1P_132
P40 MGTREFCLK1N_132

pF1_FF4_RECV11 J50 — MGTYRXP0_132
nF1_FF4_RECV11 J51 — MGTYRXN0_132
pF1_FF4_XMIT11 J45 — MGTYTXP0_132
nF1_FF4_XMIT11 J46 — MGTYTXN0_132
pF1_FF4_RECV10 H48 — MGTYRXP1_132
nF1_FF4_RECV10 H49 — MGTYRXN1_132
pF1_FF4_XMIT10 H43 — MGTYTXP1_132
nF1_FF4_XMIT10 H44 — MGTYTXN1_132
pF1_FF4_RECV9 G50 — MGTYRXP2_132
nF1_FF4_RECV9 G51 — MGTYRXN2_132
pF1_FF4_XMIT9 G45 — MGTYTXP2_132
nF1_FF4_XMIT9 G46 — MGTYTXN2_132
pF1_FF4_RECV8 F48 — MGTYRXP3_132
nF1_FF4_RECV8 F49 — MGTYRXN3_132
pF1_FF4_XMIT8 F43 — MGTYTXP3_132
nF1_FF4_XMIT8 F44 — MGTYTXN3_132

U77-36 FPGA_VU13P_A2577 — Y — GTY QUAD 133
N41 MGTREFCLK0P_133
N42 MGTREFCLK0N_133
M39 MGTREFCLK1P_133
M40 MGTREFCLK1N_133

pF1_FF4_RECV7 E50 — MGTYRXP0_133
nF1_FF4_RECV7 E51 — MGTYRXN0_133
pF1_FF4_XMIT7 D43 — MGTYTXP0_133
nF1_FF4_XMIT7 D44 — MGTYTXN0_133
pF1_FF4_RECV6 D48 — MGTYRXP1_133
nF1_FF4_RECV6 D49 — MGTYRXN1_133
pF1_FF4_XMIT6 B43 — MGTYTXP1_133
nF1_FF4_XMIT6 B44 — MGTYTXN1_133
pF1_FF4_RECV5 E46 — MGTYRXP2_133
nF1_FF4_RECV5 E47 — MGTYRXN2_133
pF1_FF4_XMIT5 C41 — MGTYTXP2_133
nF1_FF4_XMIT5 C42 — MGTYTXN2_133
pF1_FF4_RECV4 C46 — MGTYRXP3_133
nF1_FF4_RECV4 C47 — MGTYRXN3_133
pF1_FF4_XMIT4 E41 — MGTYTXP3_133
nF1_FF4_XMIT4 E42 — MGTYTXN3_133

U77-37 FPGA_VU13P_A2577 — Z — GTY QUAD 134
L41 MGTREFCLK0P_134
L42 MGTREFCLK0N_134
K39 MGTREFCLK1P_134
K40 MGTREFCLK1N_134

pF1_FF4_RECV3 A46 — MGTYRXP0_134
nF1_FF4_RECV3 A47 — MGTYRXN0_134
pF1_FF4_XMIT3 A41 — MGTYTXP0_134
nF1_FF4_XMIT3 A42 — MGTYTXN0_134
pF1_FF4_RECV2 A32 — MGTYRXP1_134
nF1_FF4_RECV2 A33 — MGTYRXN1_134
pF1_FF4_XMIT2 B39 — MGTYTXP1_134
nF1_FF4_XMIT2 B40 — MGTYTXN1_134
pF1_FF4_RECV1 B34 — MGTYRXP2_134
nF1_FF4_RECV1 B35 — MGTYRXN2_134
pF1_FF4_XMIT1 A37 — MGTYTXP2_134
nF1_FF4_XMIT1 A38 — MGTYTXN2_134
pF1_FF4_RECV0 C32 — MGTYRXP3_134
nF1_FF4_RECV0 C33 — MGTYRXN3_134
pF1_FF4_XMIT0 C37 — MGTYTXP3_134
nF1_FF4_XMIT0 C38 — MGTYTXN3_134

U34-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)
/F1_FF_RESET [35,58,59,60,61,62,63]
I2C_SDA_F1_FF4_XMIT [35]
I2C_SCL_F1_FF4_XMIT [35]
/F1_FF4_XMIT_INT [35]
/F1_FF4_XMIT_PRESENT [35]
V_3V3
V_F1_FF4_XMIT [28]
V_M3V3: R532 3.3K 0603, R533 3.3K 0603, R535 2.2K 0603, R534 2.2K 0603
C1076 22 UF 0603 6.3V, C1112 0.1 UF 0402, L23 1.0 UH 0806, C1150 22 UF 0603 6.3V, C1196 0.1 UF 0402
C1077 22 UF 0603 6.3V, C1113 0.1 UF 0402, L24 1.0 UH 0806, C1151 22 UF 0603 6.3V, C1197 0.1 UF 0402
/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.8/3.3V (>=25G 3.8V, <=16G 3.3V), RSVD, GND
<Implementation>

U34-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)
GND_B19 B19 A19, GND_B16 B16 A16, GND_B13 B13 A13, GND_B10 B10 A10, GND_B7 B7 A7, GND_B4 B4 A4, GND_B1 B1 A1
0P 0N, 1P 1N, 2P 2N, 3P 3N, 4P 4N, 5P 5N, 6P 6N, 7P 7N, 8P 8N, 9P 9N, 10P 10N, 11P 11N
pF1_FF4_XMIT0 nF1_FF4_XMIT0 … pF1_FF4_XMIT11 nF1_FF4_XMIT11
VA50, VA49, VA48, VA47, VA46, VA45

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U35-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)
/F1_FF_RESET [35,58,59,60,61,62,63]
I2C_SDA_F1_FF4_RECV [35]
I2C_SCL_F1_FF4_RECV [35]
/F1_FF4_RECV_INT [35]
/F1_FF4_RECV_PRESENT [35]
V_3V3
V_M3V3: R536 3.3K 0603, R537 3.3K 0603, R539 2.2K 0603, R538 2.2K 0603
C1093 22 UF 0603 6.3V, C1114 0.1 UF 0402, L25 1.0 UH 0806, C1152 22 UF 0603 6.3V, C1198 0.1 UF 0402
L26 1.0 UH 0806, C1153 22 UF 0603 6.3V, C1199 0.1 UF 0402
/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, RSVD, GND
<Implementation>

U35-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)
GND_B19 B19 A19, GND_B16 B16 A16, GND_B13 B13 A13, GND_B10 B10 A10, GND_B7 B7 A7, GND_B4 B4 A4, GND_B1 B1 A1
0P 0N, 1P 1N, 2P 2N, 3P 3N, 4P 4N, 5P 5N, 6P 6N, 7P 7N, 8P 8N, 9P 9N, 10P 10N, 11P 11N
pF1_FF4_RECV0 nF1_FF4_RECV0 … pF1_FF4_RECV11 nF1_FF4_RECV11
VA56, VA55, VA54, VA53, VA52, VA51

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3
Title: 7.05: FPGA#1 FF#4 X12 ON QUADS X Y Z
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7.06: FPGA#1 FF#5 X4 ON QUAD AF

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

U77-27
FPGA_VU13P_A2577
AF GTY QUAD 124

ac_pF1L_R0_AF [16]
ac_nF1L_R0_AF [16]
ac_pF1L_R1_AF [17]
ac_nF1L_R1_AF [17]

AT39 MGTREFCLK0P_124
AT40 MGTREFCLK0N_124
AR41 MGTREFCLK1P_124
AR42 MGTREFCLK1N_124

pF1_FF5_RECV0 BA50 MGTYRXP0_124
nF1_FF5_RECV0 BA51 MGTYRXN0_124
pF1_FF5_XMIT0 BA45 MGTYTXP0_124
nF1_FF5_XMIT0 BA46 MGTYTXN0_124
pF1_FF5_RECV1 AY48 MGTYRXP1_124
nF1_FF5_RECV1 AY49 MGTYRXN1_124
pF1_FF5_XMIT1 AY43 MGTYTXP1_124
nF1_FF5_XMIT1 AY44 MGTYTXN1_124
pF1_FF5_RECV2 AW50 MGTYRXP2_124
nF1_FF5_RECV2 AW51 MGTYRXN2_124
pF1_FF5_XMIT2 AW45 MGTYTXP2_124
nF1_FF5_XMIT2 AW46 MGTYTXN2_124
pF1_FF5_RECV3 AV48 MGTYRXP3_124
nF1_FF5_RECV3 AV49 MGTYRXN3_124
pF1_FF5_XMIT3 AV43 MGTYTXP3_124
nF1_FF5_XMIT3 AV44 MGTYTXN3_124

V_M3V3 R508 3.3K 0603 R509 3.3K 0603
V_M3V3 R511 2.2K 0603 R510 2.2K 0603

U28-1 FIREFLY_XCVR_X4

/F1_FF_RESET [35,58,59,60,61,63]
I2C_SDA_F1_FF5_XCVR [35]
I2C_SCL_F1_FF5_XCVR [35]
/F1_FF5_XCVR_INT [35]
/F1_FF5_XCVR_PRESENT [35]

6 /RESET G1 G2
7 SDA
8 SCL
GND 4 /SELECT
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 1.8V
GND 2 GND

V_3V3: C1089 22 UF 0603 6.3V, C1103 0.1 UF 0402, L9 1.0 UH 0806, C1136 22 UF 0603 6.3V, C1184 0.1 UF 0402
V_3V3: L11 1.0 UH 0806, C1138 22 UF 0603 6.3V, C1185 0.1 UF 0402
V_1V8: C1070 22 UF 0603 6.3V, C1102 0.1 UF 0402, L10 1.0 UH 0806, C1137 22 UF 0603 6.3V, C1176 0.1 UF 0402

U28-2 FIREFLY_XCVR_X4

B19 A19	GND_B19 GND_A19	RX1P RX1N	B17 B18	pF1_FF5_RECV0 nF1_FF5_RECV0
A17 A18		RX2P RX2N		pF1_FF5_RECV1 nF1_FF5_RECV1
B16 A16	GND_B16 GND_A16	RX3P RX3N	B14 B15	pF1_FF5_RECV2 nF1_FF5_RECV2
A14 A15		RX4P RX4N		pF1_FF5_RECV3 nF1_FF5_RECV3
B13 A13	GND_B13 GND_A13			
B7 A7	GND_B7 GND_A7	TX4P TX4N	B6 B5	pF1_FF5_XMIT3 nF1_FF5_XMIT3
A6 A5		TX3P TX3N		pF1_FF5_XMIT2 nF1_FF5_XMIT2
B4 A4	GND_B4 GND_A4	TX2P TX2N	B3 B2	pF1_FF5_XMIT1 nF1_FF5_XMIT1
A3 A2		TX1P TX1N		pF1_FF5_XMIT0 nF1_FF5_XMIT0
B1 A1	GND_B1 GND_A1			

GND VA16 VA15 VA14 VA13

R484 49p9 0402 B12 RESVD_B12
R483 49p9 0402 B11 RESVD_B11
R482 49p9 0402 B10 RESVD_B10
R481 49p9 0402 B9 RESVD_B9
R480 49p9 0402 B8 RESVD_B8
R43 49p9 0402 A12 RESVD_A12
R42 49p9 0402 A11 RESVD_A11
R41 49p9 0402 A10 RESVD_A10
R40 49p9 0402 A9 RESVD_A9
R39 49p9 0402 A8 RESVD_A8

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3		
Title: 7.06: FPGA#1 FF#5 X4 ON QUAD AF		
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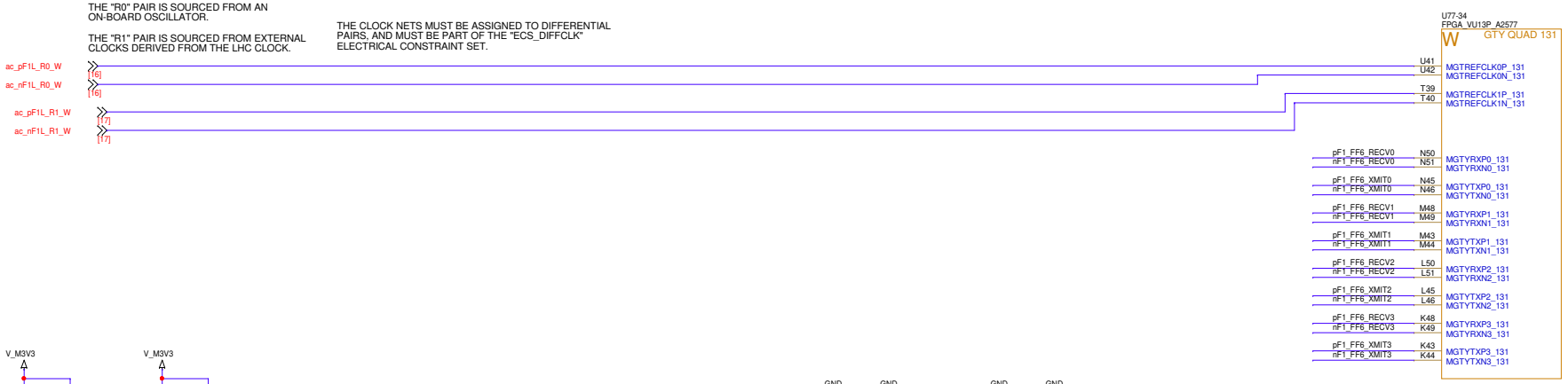
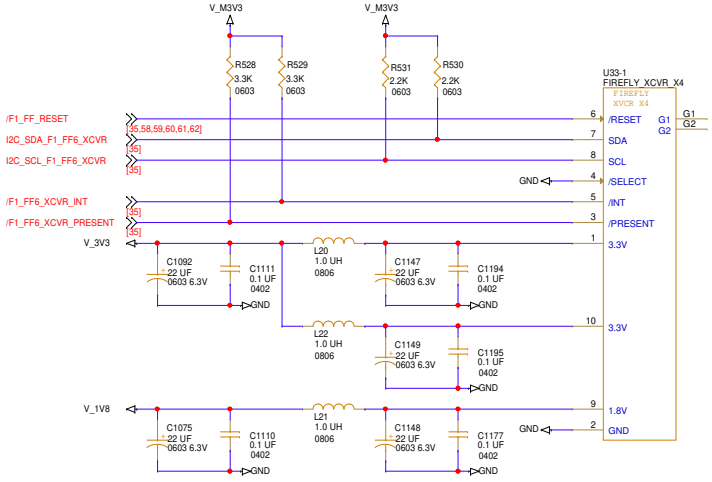
7.07: FPGA#1 FF#6 X4 ON QUAD W

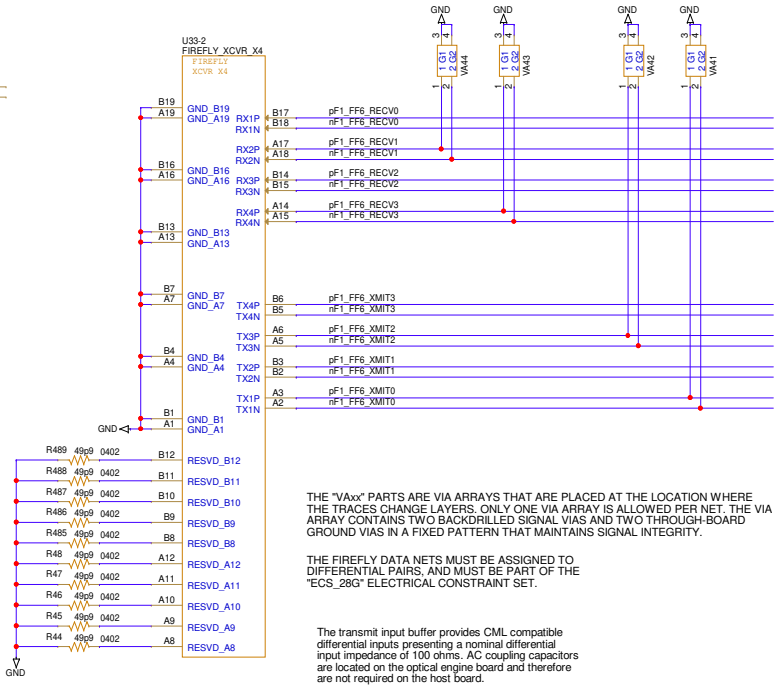
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM v3			
Title: 7.07: FPGA#1 FF#6 X4 ON QUAD W			
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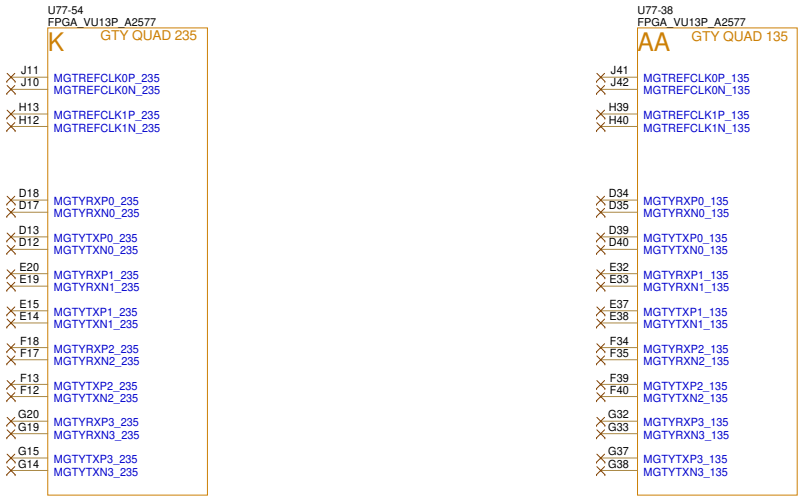
7.08: FPGA#1 UNUSED QUADS K, AA



APOLLO CM v3		
Title: 7.08: FPGA#1 UNUSED QUADS K, AA		
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QUAD "L" WIRING FOR FPGA#2 CAN BE FOUND ON SHEET 2.13: C2C AND TCDS QUADS

APOLLO CM v3		
Title: 8.01: FPGA#2 SM C2C ON QUAD L		
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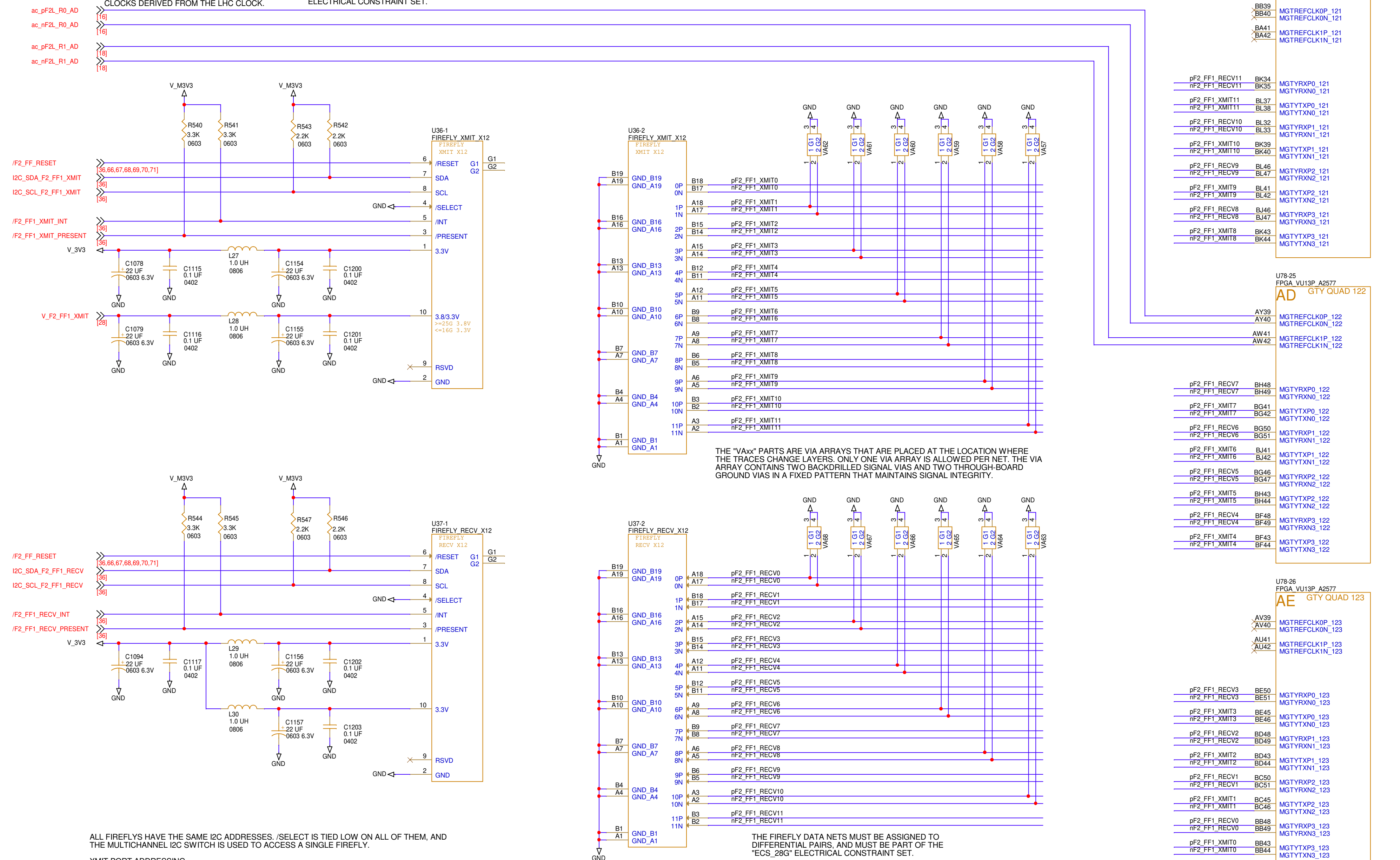
8.02: FPGA#2 FF#1 X12 ON QUADS AC AD AE

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

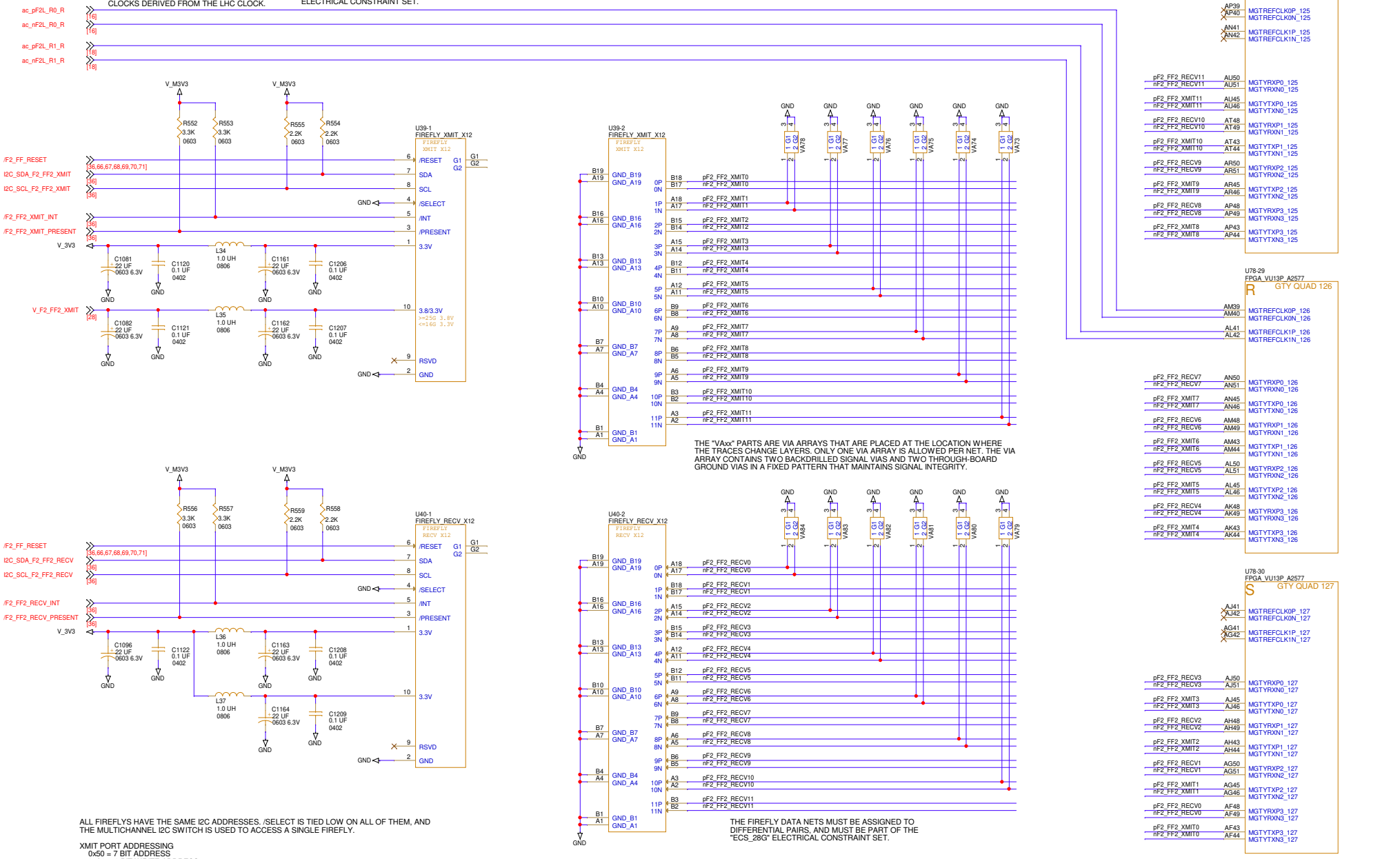
8.03: FPGA#2 FF#2 X12 ON QUADS Q R S

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3			
Title: 8.03: FPGA#2 FF#2 X12 ON QUADS Q R S			
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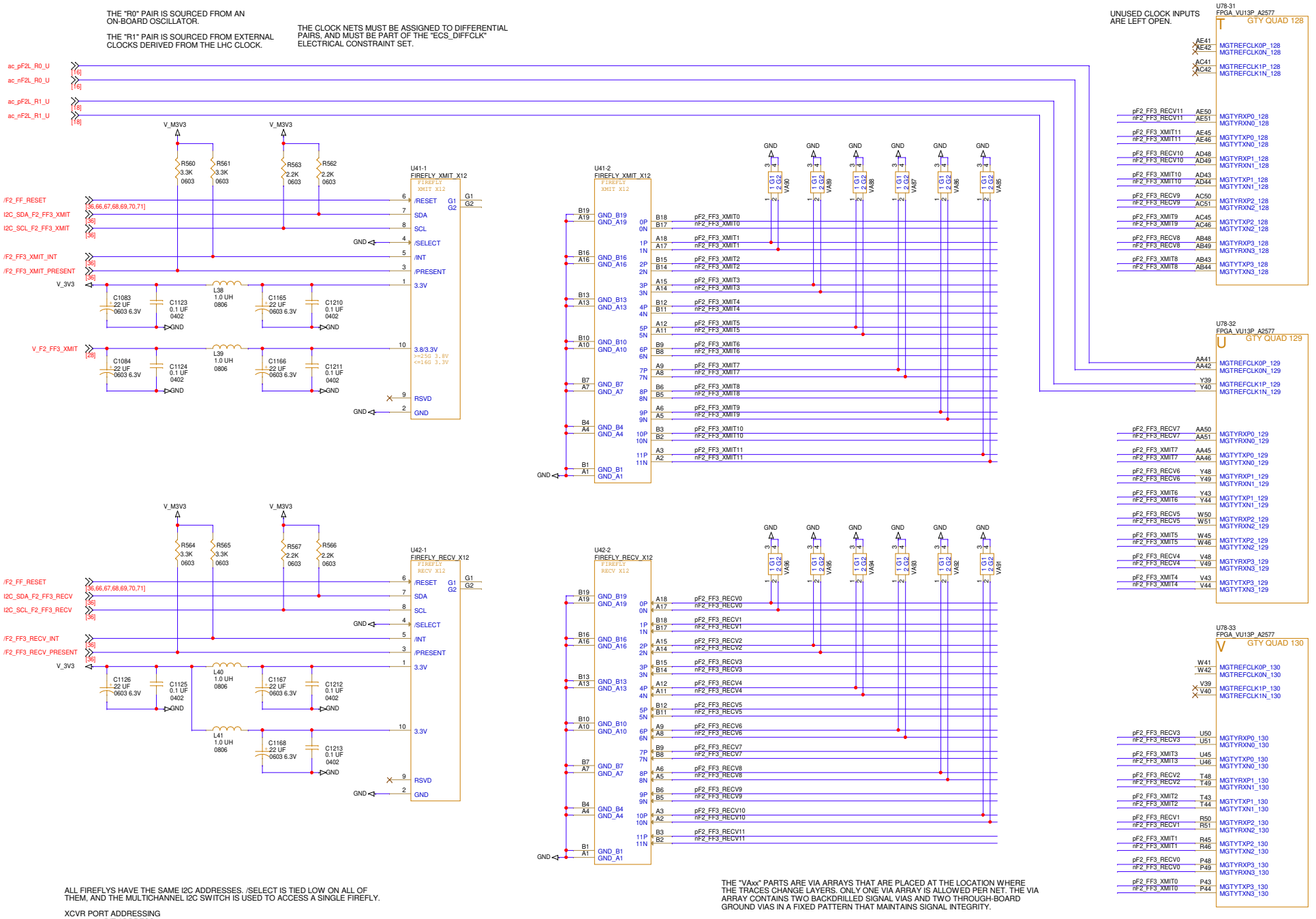
8.04: FPGA#2 FF#3 X12 ON QUADS T U V

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

APOLLO CM v3		
Title: 8.04: FPGA#2 FF#3 X12 ON QUADS T U V		
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8.05: FPGA#2 FF#4 X12 ON QUADS X Y Z

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pF2L_R0_Y [16]
ac_nF2L_R0_Y [16]
ac_pF2L_R1_Y [18]
ac_nF2L_R1_Y [18]

U78-35 FPGA_VU13P_A2577 — X — GTY QUAD 132
R41 MGTREFCLK0P_132
R42 MGTREFCLK0N_132
P39 MGTREFCLK1P_132
P40 MGTREFCLK1N_132

U78-36 FPGA_VU13P_A2577 — Y — GTY QUAD 133
N41 MGTREFCLK0P_133
N42 MGTREFCLK0N_133
M39 MGTREFCLK1P_133
M40 MGTREFCLK1N_133

U78-37 FPGA_VU13P_A2577 — Z — GTY QUAD 134
L41 MGTREFCLK0P_134
L42 MGTREFCLK0N_134
K39 MGTREFCLK1P_134
K40 MGTREFCLK1N_134

pF2_FF4_RECV11	J50	MGTYRXP0_132
nF2_FF4_RECV11	J51	MGTYRXN0_132
pF2_FF4_XMIT11	J45	MGTYTXP0_132
nF2_FF4_XMIT11	J46	MGTYTXN0_132
pF2_FF4_RECV10	H48	MGTYRXP1_132
nF2_FF4_RECV10	H49	MGTYRXN1_132
pF2_FF4_XMIT10	H43	MGTYTXP1_132
nF2_FF4_XMIT10	H44	MGTYTXN1_132
pF2_FF4_RECV9	G50	MGTYRXP2_132
nF2_FF4_RECV9	G51	MGTYRXN2_132
pF2_FF4_XMIT9	G45	MGTYTXP2_132
nF2_FF4_XMIT9	G46	MGTYTXN2_132
pF2_FF4_RECV8	F48	MGTYRXP3_132
nF2_FF4_RECV8	F49	MGTYRXN3_132
pF2_FF4_XMIT8	F43	MGTYTXP3_132
nF2_FF4_XMIT8	F44	MGTYTXN3_132

pF2_FF4_RECV7	E50	MGTYRXP0_133
nF2_FF4_RECV7	E51	MGTYRXN0_133
pF2_FF4_XMIT7	D43	MGTYTXP0_133
nF2_FF4_XMIT7	D44	MGTYTXN0_133
pF2_FF4_RECV6	D48	MGTYRXP1_133
nF2_FF4_RECV6	D49	MGTYRXN1_133
pF2_FF4_XMIT6	B43	MGTYTXP1_133
nF2_FF4_XMIT6	B44	MGTYTXN1_133
pF2_FF4_RECV5	E46	MGTYRXP2_133
nF2_FF4_RECV5	E47	MGTYRXN2_133
pF2_FF4_XMIT5	C41	MGTYTXP2_133
nF2_FF4_XMIT5	C42	MGTYTXN2_133
pF2_FF4_RECV4	C46	MGTYRXP3_133
nF2_FF4_RECV4	C47	MGTYRXN3_133
pF2_FF4_XMIT4	E41	MGTYTXP3_133
nF2_FF4_XMIT4	E42	MGTYTXN3_133

pF2_FF4_RECV3	A46	MGTYRXP0_134
nF2_FF4_RECV3	A47	MGTYRXN0_134
pF2_FF4_XMIT3	A41	MGTYTXP0_134
nF2_FF4_XMIT3	A42	MGTYTXN0_134
pF2_FF4_RECV2	A32	MGTYRXP1_134
nF2_FF4_RECV2	A33	MGTYRXN1_134
pF2_FF4_XMIT2	B39	MGTYTXP1_134
nF2_FF4_XMIT2	B40	MGTYTXN1_134
pF2_FF4_RECV1	B34	MGTYRXP2_134
nF2_FF4_RECV1	B35	MGTYRXN2_134
pF2_FF4_XMIT1	A37	MGTYTXP2_134
nF2_FF4_XMIT1	A38	MGTYTXN2_134
pF2_FF4_RECV0	C32	MGTYRXP3_134
nF2_FF4_RECV0	C33	MGTYRXN3_134
pF2_FF4_XMIT0	C37	MGTYTXP3_134
nF2_FF4_XMIT0	C38	MGTYTXN3_134

/F2_FF_RESET [16,66,67,68,69,70,71]
I2C_SDA_F2_FF4_XMIT [36]
I2C_SCL_F2_FF4_XMIT [36]
/F2_FF4_XMIT_INT [36]
/F2_FF4_XMIT_PRESENT [36]
V_3V3
V_F2_FF4_XMIT [28]

V_M3V3: R572 3.3K 0603, R573 3.3K 0603, R575 2.2K 0603, R574 2.2K 0603

U44-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)
/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.8/3.3V (>=25G 3.8V, <=16G 3.3V), RSVD, GND; G1, G2

C1086 22 UF 0603 6.3V, C1129 0.1 UF 0402, L45 1.0 UH 0806, C1172 22 UF 0603 6.3V, C1216 0.1 UF 0402
C1087 22 UF 0603 6.3V, C1130 0.1 UF 0402, L46 1.0 UH 0806, C1173 22 UF 0603 6.3V, C1217 0.1 UF 0402

U44-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)

B19	GND_B19	0P	pF2_FF4_XMIT0
A19	GND_A19	0N	nF2_FF4_XMIT0
B18	pF2_FF4_XMIT0	1P	pF2_FF4_XMIT1
B17	nF2_FF4_XMIT0	1N	nF2_FF4_XMIT1
A18	pF2_FF4_XMIT1	2P	pF2_FF4_XMIT2
A17	nF2_FF4_XMIT1	2N	nF2_FF4_XMIT2
B16	GND_B16	3P	pF2_FF4_XMIT3
A16	GND_A16	3N	nF2_FF4_XMIT3
B15	pF2_FF4_XMIT2	4P	pF2_FF4_XMIT4
B14	nF2_FF4_XMIT2	4N	nF2_FF4_XMIT4
A15	pF2_FF4_XMIT3	5P	pF2_FF4_XMIT5
A14	nF2_FF4_XMIT3	5N	nF2_FF4_XMIT5
B13	GND_B13	6P	pF2_FF4_XMIT6
A13	GND_A13	6N	nF2_FF4_XMIT6
B12	pF2_FF4_XMIT4	7P	pF2_FF4_XMIT7
B11	nF2_FF4_XMIT4	7N	nF2_FF4_XMIT7
A12	pF2_FF4_XMIT5	8P	pF2_FF4_XMIT8
A11	nF2_FF4_XMIT5	8N	nF2_FF4_XMIT8
B10	GND_B10	9P	pF2_FF4_XMIT9
A10	GND_A10	9N	nF2_FF4_XMIT9
B9	pF2_FF4_XMIT6	10P	pF2_FF4_XMIT10
B8	nF2_FF4_XMIT6	10N	nF2_FF4_XMIT10
B7	GND_B7	11P	pF2_FF4_XMIT11
A7	GND_A7	11N	nF2_FF4_XMIT11
B4	GND_B4		
A4	GND_A4		
B1	GND_B1		
A1	GND_A1		

GND; VA108, VA106, VA105, VA104, VA103, VA102, VA101

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

/F2_FF_RESET [16,66,67,68,69,70,71]
I2C_SDA_F2_FF4_RECV [36]
I2C_SCL_F2_FF4_RECV [36]
/F2_FF4_RECV_INT [36]
/F2_FF4_RECV_PRESENT [36]
V_3V3

V_M3V3: R576 3.3K 0603, R577 3.3K 0603, R579 2.2K 0603, R578 2.2K 0603

U45-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)
/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, RSVD, GND; G1, G2

C1098 22 UF 0603 6.3V, C1131 0.1 UF 0402, L47 1.0 UH 0806, C1174 22 UF 0603 6.3V, C1218 0.1 UF 0402
L48 1.0 UH 0806, C1175 22 UF 0603 6.3V, C1219 0.1 UF 0402

U45-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)

B19	GND_B19	0P	pF2_FF4_RECV0
A19	GND_A19	0N	nF2_FF4_RECV0
B18	pF2_FF4_RECV0	1P	pF2_FF4_RECV1
B17	nF2_FF4_RECV0	1N	nF2_FF4_RECV1
A18	pF2_FF4_RECV1	2P	pF2_FF4_RECV2
A17	nF2_FF4_RECV1	2N	nF2_FF4_RECV2
B16	GND_B16	3P	pF2_FF4_RECV3
A16	GND_A16	3N	nF2_FF4_RECV3
B15	pF2_FF4_RECV2	4P	pF2_FF4_RECV4
B14	nF2_FF4_RECV2	4N	nF2_FF4_RECV4
A15	pF2_FF4_RECV3	5P	pF2_FF4_RECV5
A14	nF2_FF4_RECV3	5N	nF2_FF4_RECV5
B13	GND_B13	6P	pF2_FF4_RECV6
A13	GND_A13	6N	nF2_FF4_RECV6
B12	pF2_FF4_RECV4	7P	pF2_FF4_RECV7
B11	nF2_FF4_RECV4	7N	nF2_FF4_RECV7
A12	pF2_FF4_RECV5	8P	pF2_FF4_RECV8
A11	nF2_FF4_RECV5	8N	nF2_FF4_RECV8
B10	GND_B10	9P	pF2_FF4_RECV9
A10	GND_A10	9N	nF2_FF4_RECV9
B9	pF2_FF4_RECV6	10P	pF2_FF4_RECV10
B8	nF2_FF4_RECV6	10N	nF2_FF4_RECV10
B7	GND_B7	11P	pF2_FF4_RECV11
A7	GND_A7	11N	nF2_FF4_RECV11
B4	GND_B4		
A4	GND_A4		
B1	GND_B1		
A1	GND_A1		

GND; VA112, VA111, VA110, VA109, VA108, VA107

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

APOLLO CM v3

Title: 8.05: FPGA#2 FF#4 X12 ON QUADS X Y Z

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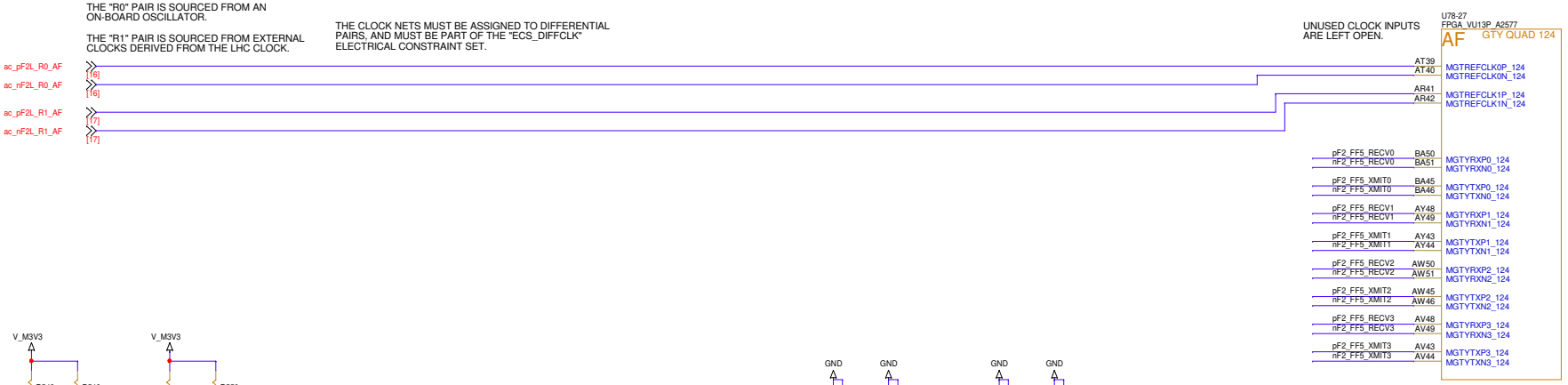
8.06: FPGA#2 FF#5 X4 ON QUAD AF

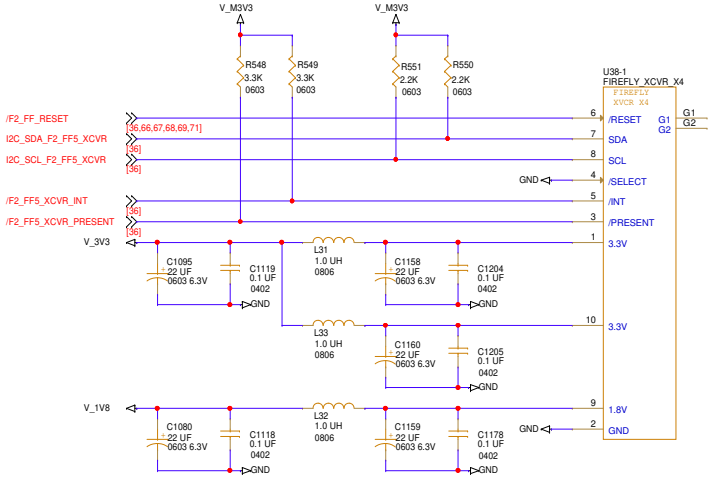
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

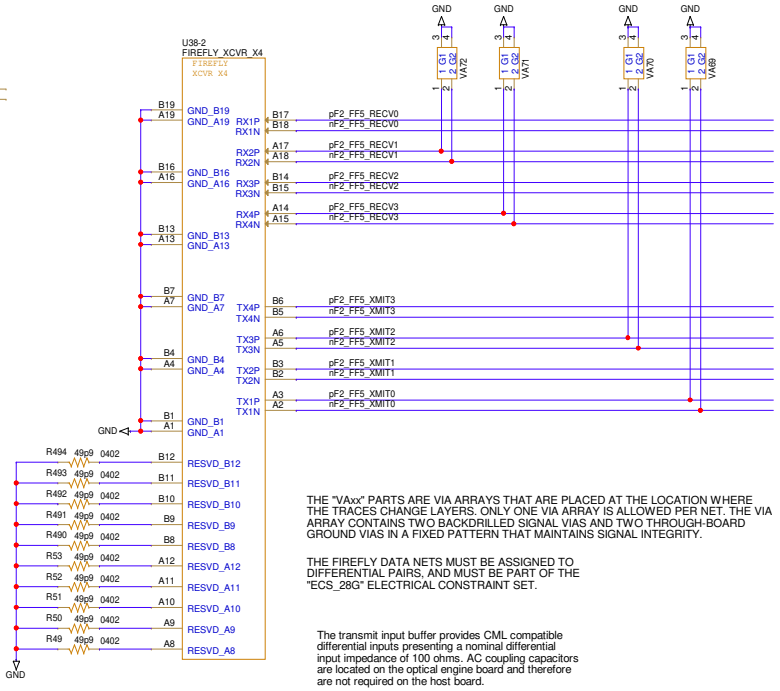
THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

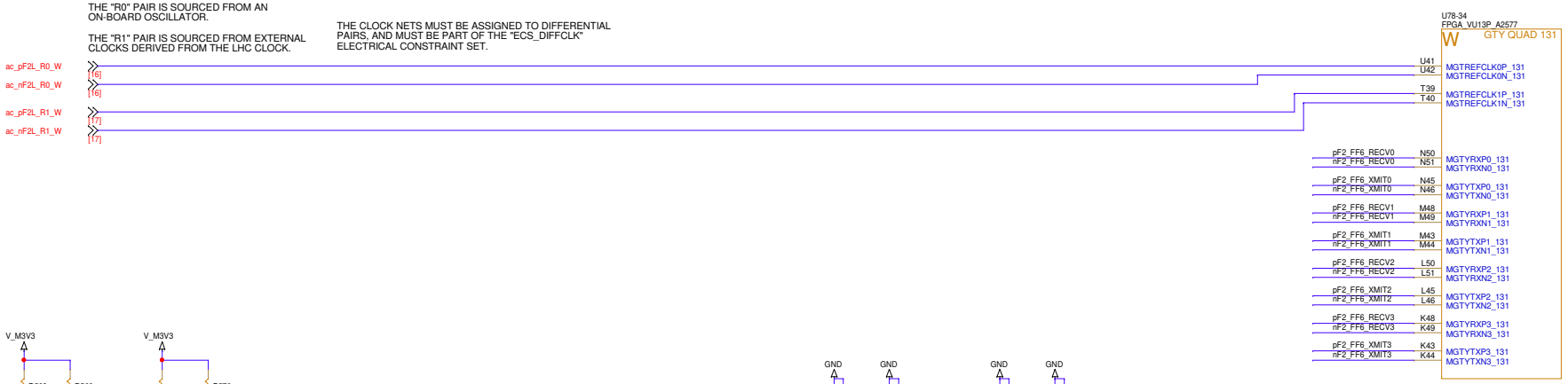
APOLLO CM v3			
Title: 8.06: FPGA#2 FF#5 X4 ON QUAD AF			
Size	Document Number: 6089-127		Rev: A
Date: Tuesday, January 02, 2024	Sheet 70 of 78		

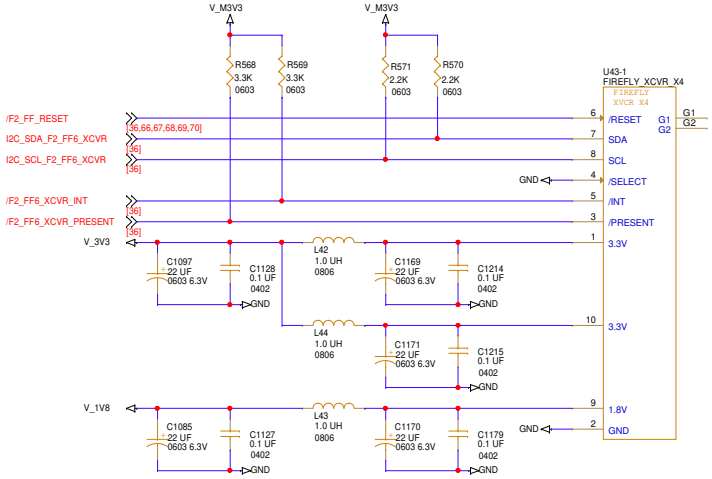
8.07: FPGA#2 FF#6 X4 ON QUAD W

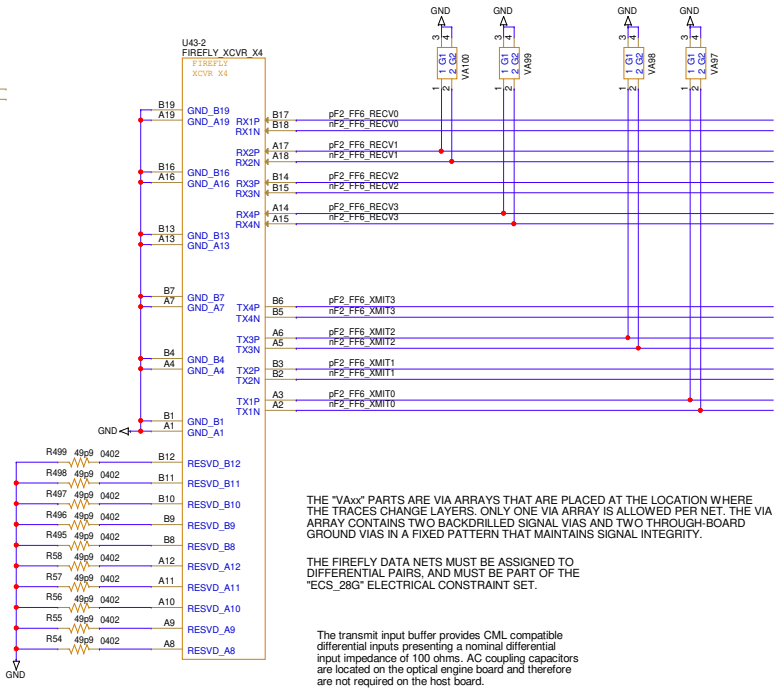
THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

APOLLO CM v3			
Title: 8.07: FPGA#2 FF#6 X4 ON QUAD W			
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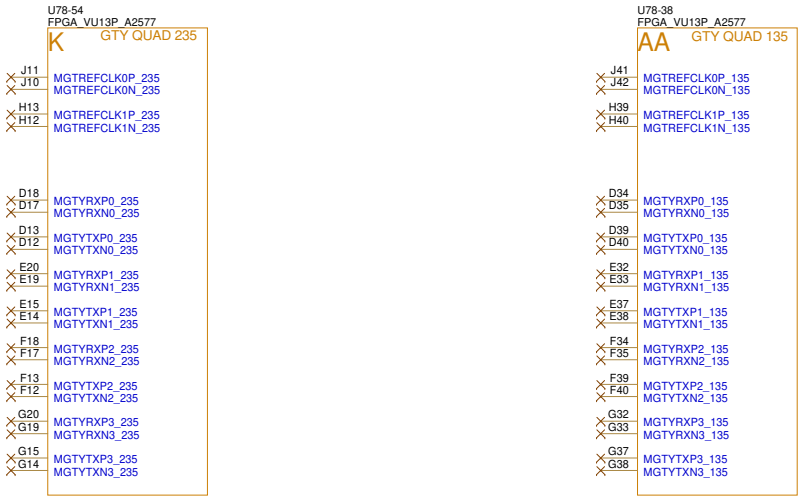
Date: Tuesday, January 02, 2024	Sheet 71 of 78		

8.08: FPGA#2 UNUSED QUADS K, AA



APOLLO CM v3		
Title: 8.08: FPGA#2 UNUSED QUADS K, AA		
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9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-40
FPGA_VU13P_A2577
GTY QUAD 221 M

MGTREFCLK0P_221 / MGTREFCLK0N_221 — BB13 / BB12
MGTREFCLK1P_221 / MGTREFCLK1N_221 — BA11 / BA10

MGTYRXP0_221 / MGTYRXN0_221	BK18 / BK17	pF1_M_RECV0 / nF1_M_RECV0	pF1_M_RECV0 / nF1_M_RECV0	C296 0.1 UF 0402	pF2_J_XMIT0 / nF2_J_XMIT0
MGTYTXP0_221 / MGTYTXN0_221	BL15 / BL14	pF1_M_XMIT0 / nF1_M_XMIT0		C295 0.1 UF 0402	
MGTYRXP1_221 / MGTYRXN1_221	BL20 / BL19	pF1_M_RECV1 / nF1_M_RECV1	pF1_M_RECV1 / nF1_M_RECV1	C298 0.1 UF 0402	pF2_J_XMIT1 / nF2_J_XMIT1
MGTYTXP1_221 / MGTYTXN1_221	BK13 / BK12	pF1_M_XMIT1 / nF1_M_XMIT1		C297 0.1 UF 0402	
MGTYRXP2_221 / MGTYRXN2_221	BL6 / BL5	pF1_M_RECV2 / nF1_M_RECV2	pF1_M_RECV2 / nF1_M_RECV2	C294 0.1 UF 0402	pF2_J_XMIT2 / nF2_J_XMIT2
MGTYTXP2_221 / MGTYTXN2_221	BL11 / BL10	pF1_M_XMIT2 / nF1_M_XMIT2		C293 0.1 UF 0402	
MGTYRXP3_221 / MGTYRXN3_221	BJ6 / BJ5	pF1_M_RECV3 / nF1_M_RECV3	pF1_M_RECV3 / nF1_M_RECV3	C292 0.1 UF 0402	pF2_J_XMIT3 / nF2_J_XMIT3
MGTYTXP3_221 / MGTYTXN3_221	BK9 / BK8	pF1_M_XMIT3 / nF1_M_XMIT3		C291 0.1 UF 0402	

		pF1_M_XMIT0 / nF1_M_XMIT0		C306 0.1 UF 0402	pF2_J_RECV0 / nF2_J_RECV0
				C305 0.1 UF 0402	
		pF1_M_XMIT1 / nF1_M_XMIT1		C304 0.1 UF 0402	pF2_J_RECV1 / nF2_J_RECV1
				C303 0.1 UF 0402	
		pF1_M_XMIT2 / nF1_M_XMIT2		C302 0.1 UF 0402	pF2_J_RECV2 / nF2_J_RECV2
				C301 0.1 UF 0402	
		pF1_M_XMIT3 / nF1_M_XMIT3		C300 0.1 UF 0402	pF2_J_RECV3 / nF2_J_RECV3
				C299 0.1 UF 0402	

U77-41
FPGA_VU13P_A2577
GTY QUAD 222 N

MGTREFCLK0P_222 / MGTREFCLK0N_222 — AY13 / AY12 — ac_pF1R_R0_N [16] / ac_nF1R_R0_N [16]
MGTREFCLK1P_222 / MGTREFCLK1N_222 — AW11 / AW10 — ac_pF1R_R1_N [19] / ac_nF1R_R1_N [19]

MGTYRXP0_222 / MGTYRXN0_222	BH4 / BH3	pF1_N_RECV0 / nF1_N_RECV0	pF1_N_RECV0 / nF1_N_RECV0	C282 0.1 UF 0402	pF2_I_XMIT0 / nF2_I_XMIT0
MGTYTXP0_222 / MGTYTXN0_222	BG11 / BG10	pF1_N_XMIT0 / nF1_N_XMIT0		C281 0.1 UF 0402	
MGTYRXP1_222 / MGTYRXN1_222	BG2 / BG1	pF1_N_RECV1 / nF1_N_RECV1	pF1_N_RECV1 / nF1_N_RECV1	C278 0.1 UF 0402	pF2_I_XMIT1 / nF2_I_XMIT1
MGTYTXP1_222 / MGTYTXN1_222	BJ11 / BJ10	pF1_N_XMIT1 / nF1_N_XMIT1		C277 0.1 UF 0402	
MGTYRXP2_222 / MGTYRXN2_222	BG5 / BG5	pF1_N_RECV2 / nF1_N_RECV2	pF1_N_RECV2 / nF1_N_RECV2	C280 0.1 UF 0402	pF2_I_XMIT2 / nF2_I_XMIT2
MGTYTXP2_222 / MGTYTXN2_222	BH9 / BH8	pF1_N_XMIT2 / nF1_N_XMIT2		C279 0.1 UF 0402	
MGTYRXP3_222 / MGTYRXN3_222	BF4 / BF3	pF1_N_RECV3 / nF1_N_RECV3	pF1_N_RECV3 / nF1_N_RECV3	C276 0.1 UF 0402	pF2_I_XMIT3 / nF2_I_XMIT3
MGTYTXP3_222 / MGTYTXN3_222	BF9 / BF8	pF1_N_XMIT3 / nF1_N_XMIT3		C275 0.1 UF 0402	

		pF1_N_XMIT0 / nF1_N_XMIT0		C286 0.1 UF 0402	pF2_I_RECV0 / nF2_I_RECV0
				C285 0.1 UF 0402	
		pF1_N_XMIT1 / nF1_N_XMIT1		C290 0.1 UF 0402	pF2_I_RECV1 / nF2_I_RECV1
				C289 0.1 UF 0402	
		pF1_N_XMIT2 / nF1_N_XMIT2		C288 0.1 UF 0402	pF2_I_RECV2 / nF2_I_RECV2
				C287 0.1 UF 0402	
		pF1_N_XMIT3 / nF1_N_XMIT3		C284 0.1 UF 0402	pF2_I_RECV3 / nF2_I_RECV3
				C283 0.1 UF 0402	

U77-42
FPGA_VU13P_A2577
GTY QUAD 223 O

MGTREFCLK0P_223 / MGTREFCLK0N_223 — AV13 / AV12
MGTREFCLK1P_223 / MGTREFCLK1N_223 — AU11 / AU10

MGTYRXP0_223 / MGTYRXN0_223	BE2 / BE1	pF1_O_RECV0 / nF1_O_RECV0	pF1_O_RECV0 / nF1_O_RECV0	C266 0.1 UF 0402	pF2_H_XMIT0 / nF2_H_XMIT0
MGTYTXP0_223 / MGTYTXN0_223	BE7 / BE6	pF1_O_XMIT0 / nF1_O_XMIT0		C265 0.1 UF 0402	
MGTYRXP1_223 / MGTYRXN1_223	BD4 / BD3	pF1_O_RECV1 / nF1_O_RECV1	pF1_O_RECV1 / nF1_O_RECV1	C264 0.1 UF 0402	pF2_H_XMIT1 / nF2_H_XMIT1
MGTYTXP1_223 / MGTYTXN1_223	BD9 / BD8	pF1_O_XMIT1 / nF1_O_XMIT1		C263 0.1 UF 0402	
MGTYRXP2_223 / MGTYRXN2_223	BC2 / BC1	pF1_O_RECV2 / nF1_O_RECV2	pF1_O_RECV2 / nF1_O_RECV2	C262 0.1 UF 0402	pF2_H_XMIT2 / nF2_H_XMIT2
MGTYTXP2_223 / MGTYTXN2_223	BC7 / BC6	pF1_O_XMIT2 / nF1_O_XMIT2		C261 0.1 UF 0402	
MGTYRXP3_223 / MGTYRXN3_223	BB4 / BB3	pF1_O_RECV3 / nF1_O_RECV3	pF1_O_RECV3 / nF1_O_RECV3	C260 0.1 UF 0402	pF2_H_XMIT3 / nF2_H_XMIT3
MGTYTXP3_223 / MGTYTXN3_223	BB9 / BB8	pF1_O_XMIT3 / nF1_O_XMIT3		C259 0.1 UF 0402	

		pF1_O_XMIT0 / nF1_O_XMIT0		C274 0.1 UF 0402	pF2_H_RECV0 / nF2_H_RECV0
				C273 0.1 UF 0402	
		pF1_O_XMIT1 / nF1_O_XMIT1		C272 0.1 UF 0402	pF2_H_RECV1 / nF2_H_RECV1
				C271 0.1 UF 0402	
		pF1_O_XMIT2 / nF1_O_XMIT2		C270 0.1 UF 0402	pF2_H_RECV2 / nF2_H_RECV2
				C269 0.1 UF 0402	
		pF1_O_XMIT3 / nF1_O_XMIT3		C268 0.1 UF 0402	pF2_H_RECV3 / nF2_H_RECV3
				C267 0.1 UF 0402	

FPGA#2

U78-53
FPGA_VU13P_A2577
GTY QUAD 234 J

MGTREFCLK0P_234 / MGTREFCLK0N_234 — L11 / L10
MGTREFCLK1P_234 / MGTREFCLK1N_234 — K13 / K12

MGTYRXP0_234 / MGTYRXN0_234	A6 / A5	pF2_J_RECV3 / nF2_J_RECV3			
MGTYTXP0_234 / MGTYTXN0_234	A11 / A10	pF2_J_XMIT3 / nF2_J_XMIT3			
MGTYRXP1_234 / MGTYRXN1_234	A20 / A19	pF2_J_RECV2 / nF2_J_RECV2			
MGTYTXP1_234 / MGTYTXN1_234	B13 / B12	pF2_J_XMIT2 / nF2_J_XMIT2			
MGTYRXP2_234 / MGTYRXN2_234	B18 / B17	pF2_J_RECV1 / nF2_J_RECV1			
MGTYTXP2_234 / MGTYTXN2_234	A15 / A14	pF2_J_XMIT1 / nF2_J_XMIT1			
MGTYRXP3_234 / MGTYRXN3_234	C20 / C19	pF2_J_RECV0 / nF2_J_RECV0			
MGTYTXP3_234 / MGTYTXN3_234	C15 / C14	pF2_J_XMIT0 / nF2_J_XMIT0			

U78-52
FPGA_VU13P_A2577
GTY QUAD 233 I

ac_pF2R_R0_I [16] / ac_nF2R_R0_I [16] — N11 / N10
ac_pF2R_R1_I [19] / ac_nF2R_R1_I [19] — M13 / M12
MGTREFCLK0P_233 / MGTREFCLK0N_233
MGTREFCLK1P_233 / MGTREFCLK1N_233

MGTYRXP0_233 / MGTYRXN0_233	E2 / E1	pF2_I_RECV3 / nF2_I_RECV3			
MGTYTXP0_233 / MGTYTXN0_233	D9 / D8	pF2_I_XMIT3 / nF2_I_XMIT3			
MGTYRXP1_233 / MGTYRXN1_233	D4 / D3	pF2_I_RECV2 / nF2_I_RECV2			
MGTYTXP1_233 / MGTYTXN1_233	B9 / B8	pF2_I_XMIT2 / nF2_I_XMIT2			
MGTYRXP2_233 / MGTYRXN2_233	E6 / E5	pF2_I_RECV1 / nF2_I_RECV1			
MGTYTXP2_233 / MGTYTXN2_233	C11 / C10	pF2_I_XMIT1 / nF2_I_XMIT1			
MGTYRXP3_233 / MGTYRXN3_233	C6 / C5	pF2_I_RECV0 / nF2_I_RECV0			
MGTYTXP3_233 / MGTYTXN3_233	E11 / E10	pF2_I_XMIT0 / nF2_I_XMIT0			

U78-51
FPGA_VU13P_A2577
GTY QUAD 232 H

MGTREFCLK0P_232 / MGTREFCLK0N_232 — R11 / R10
MGTREFCLK1P_232 / MGTREFCLK1N_232 — P13 / P12

MGTYRXP0_232 / MGTYRXN0_232	J2 / J1	pF2_H_RECV3 / nF2_H_RECV3			
MGTYTXP0_232 / MGTYTXN0_232	J7 / J6	pF2_H_XMIT3 / nF2_H_XMIT3			
MGTYRXP1_232 / MGTYRXN1_232	H4 / H3	pF2_H_RECV2 / nF2_H_RECV2			
MGTYTXP1_232 / MGTYTXN1_232	H9 / H8	pF2_H_XMIT2 / nF2_H_XMIT2			
MGTYRXP2_232 / MGTYRXN2_232	G2 / G1	pF2_H_RECV1 / nF2_H_RECV1			
MGTYTXP2_232 / MGTYTXN2_232	G7 / G6	pF2_H_XMIT1 / nF2_H_XMIT1			
MGTYRXP3_232 / MGTYRXN3_232	F4 / F3	pF2_H_RECV0 / nF2_H_RECV0			
MGTYTXP3_232 / MGTYTXN3_232	F9 / F8	pF2_H_XMIT0 / nF2_H_XMIT0			

APOLLO CM v3

Title: 9.01: F1 QUADS M, N, O TO F2 QUADS J, I, H

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9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-44
FPGA_VU13P_A2577
GTY QUAD 225 A

MGTREFCLK0P_225 / MGTREFCLK0N_225 — AP13 / AP12
MGTREFCLK1P_225 / MGTREFCLK1N_225 — AN11 / AN10

MGTYRXP0_225 / MGTYRXN0_225	AU2 / AU1	pF1_A_RECV0 / nF1_A_RECV0
MGTYTXP0_225 / MGTYTXN0_225	AU7 / AU6	pF1_A_XMIT0 / nF1_A_XMIT0
MGTYRXP1_225 / MGTYRXN1_225	AT4 / AT3	pF1_A_RECV1 / nF1_A_RECV1
MGTYTXP1_225 / MGTYTXN1_225	AT9 / AT8	pF1_A_XMIT1 / nF1_A_XMIT1
MGTYRXP2_225 / MGTYRXN2_225	AR2 / AR1	pF1_A_RECV2 / nF1_A_RECV2
MGTYTXP2_225 / MGTYTXN2_225	AR7 / AR6	pF1_A_XMIT2 / nF1_A_XMIT2
MGTYRXP3_225 / MGTYRXN3_225	AP4 / AP3	pF1_A_RECV3 / nF1_A_RECV3
MGTYTXP3_225 / MGTYTXN3_225	AP9 / AP8	pF1_A_XMIT3 / nF1_A_XMIT3

U77-45
FPGA_VU13P_A2577
GTY QUAD 226 B

MGTREFCLK0P_226 / MGTREFCLK0N_226 — AM13 / AM12 — ac_pF1R_R0_B [18] / ac_nF1R_R0_B [18]
MGTREFCLK1P_226 / MGTREFCLK1N_226 — AL11 / AL10 — ac_pF1R_R1_B [19] / ac_nF1R_R1_B [19]

MGTYRXP0_226 / MGTYRXN0_226	AN2 / AN1	pF1_B_RECV0 / nF1_B_RECV0
MGTYTXP0_226 / MGTYTXN0_226	AN7 / AN6	pF1_B_XMIT0 / nF1_B_XMIT0
MGTYRXP1_226 / MGTYRXN1_226	AM4 / AM3	pF1_B_RECV1 / nF1_B_RECV1
MGTYTXP1_226 / MGTYTXN1_226	AM9 / AM8	pF1_B_XMIT1 / nF1_B_XMIT1
MGTYRXP2_226 / MGTYRXN2_226	AL2 / AL1	pF1_B_RECV2 / nF1_B_RECV2
MGTYTXP2_226 / MGTYTXN2_226	AL7 / AL6	pF1_B_XMIT2 / nF1_B_XMIT2
MGTYRXP3_226 / MGTYRXN3_226	AK4 / AK3	pF1_B_RECV3 / nF1_B_RECV3
MGTYTXP3_226 / MGTYTXN3_226	AK9 / AK8	pF1_B_XMIT3 / nF1_B_XMIT3

U77-46
FPGA_VU13P_A2577
GTY QUAD 227 C

MGTREFCLK0P_227 / MGTREFCLK0N_227 — AJ11 / AJ10
MGTREFCLK1P_227 / MGTREFCLK1N_227 — AG11 / AG10

MGTYRXP0_227 / MGTYRXN0_227	AJ2 / AJ1	pF1_C_RECV0 / nF1_C_RECV0
MGTYTXP0_227 / MGTYTXN0_227	AJ7 / AJ6	pF1_C_XMIT0 / nF1_C_XMIT0
MGTYRXP1_227 / MGTYRXN1_227	AH4 / AH3	pF1_C_RECV1 / nF1_C_RECV1
MGTYTXP1_227 / MGTYTXN1_227	AH9 / AH8	pF1_C_XMIT1 / nF1_C_XMIT1
MGTYRXP2_227 / MGTYRXN2_227	AG2 / AG1	pF1_C_RECV2 / nF1_C_RECV2
MGTYTXP2_227 / MGTYTXN2_227	AG7 / AG6	pF1_C_XMIT2 / nF1_C_XMIT2
MGTYRXP3_227 / MGTYRXN3_227	AF4 / AF3	pF1_C_RECV3 / nF1_C_RECV3
MGTYTXP3_227 / MGTYTXN3_227	AF9 / AF8	pF1_C_XMIT3 / nF1_C_XMIT3

FPGA#2

U78-49
FPGA_VU13P_A2577
GTY QUAD 230 F

MGTREFCLK0P_230 / MGTREFCLK0N_230 — W11 / W10
MGTREFCLK1P_230 / MGTREFCLK1N_230 — V13 / V12

MGTYRXP0_230 / MGTYRXN0_230	U2 / U1	pF2_F_RECV3 / nF2_F_RECV3
MGTYTXP0_230 / MGTYTXN0_230	U7 / U6	pF2_F_XMIT3 / nF2_F_XMIT3
MGTYRXP1_230 / MGTYRXN1_230	T4 / T3	pF2_F_RECV2 / nF2_F_RECV2
MGTYTXP1_230 / MGTYTXN1_230	T9 / T8	pF2_F_XMIT2 / nF2_F_XMIT2
MGTYRXP2_230 / MGTYRXN2_230	R2 / R1	pF2_F_RECV1 / nF2_F_RECV1
MGTYTXP2_230 / MGTYTXN2_230	R7 / R6	pF2_F_XMIT1 / nF2_F_XMIT1
MGTYRXP3_230 / MGTYRXN3_230	P4 / P3	pF2_F_RECV0 / nF2_F_RECV0
MGTYTXP3_230 / MGTYTXN3_230	P9 / P8	pF2_F_XMIT0 / nF2_F_XMIT0

U78-48
FPGA_VU13P_A2577
GTY QUAD 229 E

MGTREFCLK0P_229 / MGTREFCLK0N_229 — AA11 / AA10 — ac_pF2R_R0_E [16] / ac_nF2R_R0_E [16]
MGTREFCLK1P_229 / MGTREFCLK1N_229 — Y13 / Y12 — ac_pF2R_R1_E [19] / ac_nF2R_R1_E [19]

MGTYRXP0_229 / MGTYRXN0_229	AA2 / AA1	pF2_E_RECV3 / nF2_E_RECV3
MGTYTXP0_229 / MGTYTXN0_229	AA7 / AA6	pF2_E_XMIT3 / nF2_E_XMIT3
MGTYRXP1_229 / MGTYRXN1_229	Y4 / Y3	pF2_E_RECV2 / nF2_E_RECV2
MGTYTXP1_229 / MGTYTXN1_229	Y9 / Y8	pF2_E_XMIT2 / nF2_E_XMIT2
MGTYRXP2_229 / MGTYRXN2_229	W2 / W1	pF2_E_RECV1 / nF2_E_RECV1
MGTYTXP2_229 / MGTYTXN2_229	W7 / W6	pF2_E_XMIT1 / nF2_E_XMIT1
MGTYRXP3_229 / MGTYRXN3_229	V4 / V3	pF2_E_RECV0 / nF2_E_RECV0
MGTYTXP3_229 / MGTYTXN3_229	V9 / V8	pF2_E_XMIT0 / nF2_E_XMIT0

U78-47
FPGA_VU13P_A2577
GTY QUAD 228 D

MGTREFCLK0P_228 / MGTREFCLK0N_228 — AE11 / AE10
MGTREFCLK1P_228 / MGTREFCLK1N_228 — AC11 / AC10

MGTYRXP0_228 / MGTYRXN0_228	AE2 / AE1	pF2_D_RECV3 / nF2_D_RECV3
MGTYTXP0_228 / MGTYTXN0_228	AE7 / AE6	pF2_D_XMIT3 / nF2_D_XMIT3
MGTYRXP1_228 / MGTYRXN1_228	AD4 / AD3	pF2_D_RECV2 / nF2_D_RECV2
MGTYTXP1_228 / MGTYTXN1_228	AD9 / AD8	pF2_D_XMIT2 / nF2_D_XMIT2
MGTYRXP2_228 / MGTYRXN2_228	AC2 / AC1	pF2_D_RECV1 / nF2_D_RECV1
MGTYTXP2_228 / MGTYTXN2_228	AC7 / AC6	pF2_D_XMIT1 / nF2_D_XMIT1
MGTYRXP3_228 / MGTYRXN3_228	AB4 / AB3	pF2_D_RECV0 / nF2_D_RECV0
MGTYTXP3_228 / MGTYTXN3_228	AB9 / AB8	pF2_D_XMIT0 / nF2_D_XMIT0

Cross-quad AC-coupling capacitors (0.1 uF 0402)

pF1_A_RECV0 / nF1_A_RECV0	C224	pF2_F_XMIT0 / nF2_F_XMIT0
pF1_A_RECV1 / nF1_A_RECV1	C223	pF2_F_XMIT1 / nF2_F_XMIT1
pF1_A_RECV2 / nF1_A_RECV2	C222	pF2_F_XMIT2 / nF2_F_XMIT2
pF1_A_RECV3 / nF1_A_RECV3	C221	pF2_F_XMIT3 / nF2_F_XMIT3
pF1_A_XMIT0 / nF1_A_XMIT0	C220	pF2_F_RECV0 / nF2_F_RECV0
pF1_A_XMIT1 / nF1_A_XMIT1	C219	pF2_F_RECV1 / nF2_F_RECV1
pF1_A_XMIT2 / nF1_A_XMIT2	C218	pF2_F_RECV2 / nF2_F_RECV2
pF1_A_XMIT3 / nF1_A_XMIT3	C217	pF2_F_RECV3 / nF2_F_RECV3
pF1_B_RECV0 / nF1_B_RECV0	C208	pF2_E_XMIT0 / nF2_E_XMIT0
pF1_B_RECV1 / nF1_B_RECV1	C207	pF2_E_XMIT1 / nF2_E_XMIT1
pF1_B_RECV2 / nF1_B_RECV2	C206	pF2_E_XMIT2 / nF2_E_XMIT2
pF1_B_RECV3 / nF1_B_RECV3	C205	pF2_E_XMIT3 / nF2_E_XMIT3
pF1_B_XMIT0 / nF1_B_XMIT0	C204	pF2_E_RECV0 / nF2_E_RECV0
pF1_B_XMIT1 / nF1_B_XMIT1	C203	pF2_E_RECV1 / nF2_E_RECV1
pF1_B_XMIT2 / nF1_B_XMIT2	C202	pF2_E_RECV2 / nF2_E_RECV2
pF1_B_XMIT3 / nF1_B_XMIT3	C201	pF2_E_RECV3 / nF2_E_RECV3
pF1_C_RECV0 / nF1_C_RECV0	C188	pF2_D_XMIT0 / nF2_D_XMIT0
pF1_C_RECV1 / nF1_C_RECV1	C187	pF2_D_XMIT1 / nF2_D_XMIT1
pF1_C_RECV2 / nF1_C_RECV2	C186	pF2_D_XMIT2 / nF2_D_XMIT2
pF1_C_RECV3 / nF1_C_RECV3	C185	pF2_D_XMIT3 / nF2_D_XMIT3
pF1_C_XMIT0 / nF1_C_XMIT0	C184	pF2_D_RECV0 / nF2_D_RECV0
pF1_C_XMIT1 / nF1_C_XMIT1	C183	pF2_D_RECV1 / nF2_D_RECV1
pF1_C_XMIT2 / nF1_C_XMIT2	C182	pF2_D_RECV2 / nF2_D_RECV2
pF1_C_XMIT3 / nF1_C_XMIT3	C181	pF2_D_RECV3 / nF2_D_RECV3

pF1_A_XMIT0 / nF1_A_XMIT0	C232	pF2_F_RECV0 / nF2_F_RECV0
pF1_A_XMIT1 / nF1_A_XMIT1	C231	pF2_F_RECV1 / nF2_F_RECV1
pF1_A_XMIT2 / nF1_A_XMIT2	C230	pF2_F_RECV2 / nF2_F_RECV2
pF1_A_XMIT3 / nF1_A_XMIT3	C229	pF2_F_RECV3 / nF2_F_RECV3
pF1_B_XMIT0 / nF1_B_XMIT0	C228	pF2_E_RECV0 / nF2_E_RECV0
pF1_B_XMIT1 / nF1_B_XMIT1	C227	pF2_E_RECV1 / nF2_E_RECV1
pF1_B_XMIT2 / nF1_B_XMIT2	C226	pF2_E_RECV2 / nF2_E_RECV2
pF1_B_XMIT3 / nF1_B_XMIT3	C225	pF2_E_RECV3 / nF2_E_RECV3
pF1_C_XMIT0 / nF1_C_XMIT0	C196	pF2_D_RECV0 / nF2_D_RECV0
pF1_C_XMIT1 / nF1_C_XMIT1	C195	pF2_D_RECV1 / nF2_D_RECV1
pF1_C_XMIT2 / nF1_C_XMIT2	C194	pF2_D_RECV2 / nF2_D_RECV2
pF1_C_XMIT3 / nF1_C_XMIT3	C193	pF2_D_RECV3 / nF2_D_RECV3
	C192	
	C191	
	C190	
	C189	

	C216	
	C215	
	C214	
	C213	
	C212	
	C211	
	C210	
	C209	

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Title	9.02: F1 QUADS A, B, C TO F2 QUADS F, E, D
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UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-51
FPGA_VU13P_A2577
GTY QUAD 232 H

MGTREFCLK0P_232 R11
MGTREFCLK0N_232 R10
MGTREFCLK1P_232 P13
MGTREFCLK1N_232 P12

MGTYRXP0_232 J2	pF1_H_RECV0	pF1_H_RECV0	pF2_O_XMIT0
MGTYRXN0_232 J1	nF1_H_RECV0	nF1_H_RECV0	nF2_O_XMIT0
MGTYTXP0_232 J7	pF1_H_XMIT0	pF1_H_XMIT0	pF2_O_RECV0
MGTYTXN0_232 J6	nF1_H_XMIT0	nF1_H_XMIT0	nF2_O_RECV0
MGTYRXP1_232 H4	pF1_H_RECV1	pF1_H_RECV1	pF2_O_XMIT1
MGTYRXN1_232 H3	nF1_H_RECV1	nF1_H_RECV1	nF2_O_XMIT1
MGTYTXP1_232 H9	pF1_H_XMIT1	pF1_H_XMIT1	pF2_O_RECV1
MGTYTXN1_232 H8	nF1_H_XMIT1	nF1_H_XMIT1	nF2_O_RECV1
MGTYRXP2_232 G2	pF1_H_RECV2	pF1_H_RECV2	pF2_O_XMIT2
MGTYRXN2_232 G1	nF1_H_RECV2	nF1_H_RECV2	nF2_O_XMIT2
MGTYTXP2_232 G7	pF1_H_XMIT2	pF1_H_XMIT2	pF2_O_RECV2
MGTYTXN2_232 G6	nF1_H_XMIT2	nF1_H_XMIT2	nF2_O_RECV2
MGTYRXP3_232 F4	pF1_H_RECV3	pF1_H_RECV3	pF2_O_XMIT3
MGTYRXN3_232 F3	nF1_H_RECV3	nF1_H_RECV3	nF2_O_XMIT3
MGTYTXP3_232 F9	pF1_H_XMIT3	pF1_H_XMIT3	pF2_O_RECV3
MGTYTXN3_232 F8	nF1_H_XMIT3	nF1_H_XMIT3	nF2_O_RECV3

C91 C90 C89 C88 C87 C86 C85 C84 C99 C98 C97 C96 C95 C94 C93 C92 — 0.1 UF 0402

U77-52
FPGA_VU13P_A2577
GTY QUAD 233 I

MGTREFCLK0P_233 N11
MGTREFCLK0N_233 N10
MGTREFCLK1P_233 M13
MGTREFCLK1N_233 M12

ac_pF1R_R0_I [18]
ac_nF1R_R0_I [18]
ac_pF1R_R1_I [19]
ac_nF1R_R1_I [19]

MGTYRXP0_233 E2	pF1_I_RECV0	pF1_I_RECV0	pF2_N_XMIT0
MGTYRXN0_233 E1	nF1_I_RECV0	nF1_I_RECV0	nF2_N_XMIT0
MGTYTXP0_233 D9	pF1_I_XMIT0	pF1_I_XMIT0	pF2_N_RECV0
MGTYTXN0_233 D8	nF1_I_XMIT0	nF1_I_XMIT0	nF2_N_RECV0
MGTYRXP1_233 D4	pF1_I_RECV1	pF1_I_RECV1	pF2_N_XMIT1
MGTYRXN1_233 D3	nF1_I_RECV1	nF1_I_RECV1	nF2_N_XMIT1
MGTYTXP1_233 B9	pF1_I_XMIT1	pF1_I_XMIT1	pF2_N_RECV1
MGTYTXN1_233 B8	nF1_I_XMIT1	nF1_I_XMIT1	nF2_N_RECV1
MGTYRXP2_233 E6	pF1_I_RECV2	pF1_I_RECV2	pF2_N_XMIT2
MGTYRXN2_233 E5	nF1_I_RECV2	nF1_I_RECV2	nF2_N_XMIT2
MGTYTXP2_233 C11	pF1_I_XMIT2	pF1_I_XMIT2	pF2_N_RECV2
MGTYTXN2_233 C10	nF1_I_XMIT2	nF1_I_XMIT2	nF2_N_RECV2
MGTYRXP3_233 C6	pF1_I_RECV3	pF1_I_RECV3	pF2_N_XMIT3
MGTYRXN3_233 C5	nF1_I_RECV3	nF1_I_RECV3	nF2_N_XMIT3
MGTYTXP3_233 E11	pF1_I_XMIT3	pF1_I_XMIT3	pF2_N_RECV3
MGTYTXN3_233 E10	nF1_I_XMIT3	nF1_I_XMIT3	nF2_N_RECV3

C71 C70 C69 C68 C64 C65 C66 C67 C79 C78 C77 C76 C74 C75 C72 C73 — 0.1 UF 0402

U77-53
FPGA_VU13P_A2577
GTY QUAD 234 J

MGTREFCLK0P_234 L11
MGTREFCLK0N_234 L10
MGTREFCLK1P_234 K13
MGTREFCLK1N_234 K12

MGTYRXP0_234 A6	pF1_J_RECV0	pF1_J_RECV0	pF2_M_XMIT0
MGTYRXN0_234 A5	nF1_J_RECV0	nF1_J_RECV0	nF2_M_XMIT0
MGTYTXP0_234 A11	pF1_J_XMIT0	pF1_J_XMIT0	pF2_M_RECV0
MGTYTXN0_234 A10	nF1_J_XMIT0	nF1_J_XMIT0	nF2_M_RECV0
MGTYRXP1_234 A20	pF1_J_RECV1	pF1_J_RECV1	pF2_M_XMIT1
MGTYRXN1_234 A19	nF1_J_RECV1	nF1_J_RECV1	nF2_M_XMIT1
MGTYTXP1_234 B13	pF1_J_XMIT1	pF1_J_XMIT1	pF2_M_RECV1
MGTYTXN1_234 B12	nF1_J_XMIT1	nF1_J_XMIT1	nF2_M_RECV1
MGTYRXP2_234 B18	pF1_J_RECV2	pF1_J_RECV2	pF2_M_XMIT2
MGTYRXN2_234 B17	nF1_J_RECV2	nF1_J_RECV2	nF2_M_XMIT2
MGTYTXP2_234 A15	pF1_J_XMIT2	pF1_J_XMIT2	pF2_M_RECV2
MGTYTXN2_234 A14	nF1_J_XMIT2	nF1_J_XMIT2	nF2_M_RECV2
MGTYRXP3_234 C20	pF1_J_RECV3	pF1_J_RECV3	pF2_M_XMIT3
MGTYRXN3_234 C19	nF1_J_RECV3	nF1_J_RECV3	nF2_M_XMIT3
MGTYTXP3_234 C15	pF1_J_XMIT3	pF1_J_XMIT3	pF2_M_RECV3
MGTYTXN3_234 C14	nF1_J_XMIT3	nF1_J_XMIT3	nF2_M_RECV3

C54 C55 C52 C53 C50 C51 C48 C49 C62 C63 C60 C61 C56 C57 C58 C59 — 0.1 UF 0402

FPGA#2

U78-42
FPGA_VU13P_A2577
GTY QUAD 223 O

AV13 AV12 MGTREFCLK0P_223 MGTREFCLK0N_223
AU11 AU10 MGTREFCLK1P_223 MGTREFCLK1N_223

pF2_O_RECV3 BE2	nF2_O_RECV3 BE1	MGTYRXP0_223	MGTYRXN0_223
pF2_O_XMIT3 BE7	nF2_O_XMIT3 BE6	MGTYTXP0_223	MGTYTXN0_223
pF2_O_RECV2 BD4	nF2_O_RECV2 BD3	MGTYRXP1_223	MGTYRXN1_223
pF2_O_XMIT2 BD9	nF2_O_XMIT2 BD8	MGTYTXP1_223	MGTYTXN1_223
pF2_O_RECV1 BC2	nF2_O_RECV1 BC1	MGTYRXP2_223	MGTYRXN2_223
pF2_O_XMIT1 BC7	nF2_O_XMIT1 BC6	MGTYTXP2_223	MGTYTXN2_223
pF2_O_RECV0 BB4	nF2_O_RECV0 BB3	MGTYRXP3_223	MGTYRXN3_223
pF2_O_XMIT0 BB9	nF2_O_XMIT0 BB8	MGTYTXP3_223	MGTYTXN3_223

U78-41
FPGA_VU13P_A2577
GTY QUAD 222 N

ac_pF2R_R0_N [16]
ac_nF2R_R0_N [16]
ac_pF2R_R1_N [19]
ac_nF2R_R1_N [19]

AY13 AY12 MGTREFCLK0P_222 MGTREFCLK0N_222
AW11 AW10 MGTREFCLK1P_222 MGTREFCLK1N_222

pF2_N_RECV3 BH4	nF2_N_RECV3 BH3	MGTYRXP0_222	MGTYRXN0_222
pF2_N_XMIT3 BG11	nF2_N_XMIT3 BG10	MGTYTXP0_222	MGTYTXN0_222
pF2_N_RECV2 BG2	nF2_N_RECV2 BG1	MGTYRXP1_222	MGTYRXN1_222
pF2_N_XMIT2 BJ11	nF2_N_XMIT2 BJ10	MGTYTXP1_222	MGTYTXN1_222
pF2_N_RECV1 BG6	nF2_N_RECV1 BG5	MGTYRXP2_222	MGTYRXN2_222
pF2_N_XMIT1 BH9	nF2_N_XMIT1 BH8	MGTYTXP2_222	MGTYTXN2_222
pF2_N_RECV0 BF4	nF2_N_RECV0 BF3	MGTYRXP3_222	MGTYRXN3_222
pF2_N_XMIT0 BF9	nF2_N_XMIT0 BF8	MGTYTXP3_222	MGTYTXN3_222

U78-40
FPGA_VU13P_A2577
GTY QUAD 221 M

BB13 BB12 MGTREFCLK0P_221 MGTREFCLK0N_221
BA11 BA10 MGTREFCLK1P_221 MGTREFCLK1N_221

pF2_M_RECV3 BK18	nF2_M_RECV3 BK17	MGTYRXP0_221	MGTYRXN0_221
pF2_M_XMIT3 BL15	nF2_M_XMIT3 BL14	MGTYTXP0_221	MGTYTXN0_221
pF2_M_RECV2 BL20	nF2_M_RECV2 BL19	MGTYRXP1_221	MGTYRXN1_221
pF2_M_XMIT2 BK13	nF2_M_XMIT2 BK12	MGTYTXP1_221	MGTYTXN1_221
pF2_M_RECV1 BL6	nF2_M_RECV1 BL5	MGTYRXP2_221	MGTYRXN2_221
pF2_M_XMIT1 BL11	nF2_M_XMIT1 BL10	MGTYTXP2_221	MGTYTXN2_221
pF2_M_RECV0 BJ6	nF2_M_RECV0 BJ5	MGTYRXP3_221	MGTYRXN3_221
pF2_M_XMIT0 BK9	nF2_M_XMIT0 BK8	MGTYTXP3_221	MGTYTXN3_221

APOLLO CM v3		
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FPGA#1

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#2

U77-47
FPGA_VU13P_A2577
GTY QUAD 228 D

U77-48
FPGA_VU13P_A2577
GTY QUAD 229 E

U77-49
FPGA_VU13P_A2577
GTY QUAD 230 F

U78-46
FPGA_VU13P_A2577
GTY QUAD 227 C

U78-45
FPGA_VU13P_A2577
GTY QUAD 226 B

U78-44
FPGA_VU13P_A2577
GTY QUAD 225 A

Title	
APOLLO CM v3	
9.04: F1 QUADS D, E, F TO F2 QUADS C, B, A	
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9.05: F1 QUAD G_P TO F2 QUAD P_G

UNUSED CLOCK INPUTS ARE LEFT OPEN.

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

THE DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

THE "R0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "R1" PAIR IS SOURCED FROM EXTERNAL CLOCKS DERIVED FROM THE LHC CLOCK.

FPGA#1

U77-50
FPGA_VU13P_A2577
GTY QUAD 231 G

MGTREFCLK0P_231 / MGTREFCLK0N_231 — U11 / U10
MGTREFCLK1P_231 / MGTREFCLK1N_231 — T13 / T12

ac_pF1R_R0_G [16]
ac_nF1R_R0_G [16]
ac_pF1R_R1_G [19]
ac_nF1R_R1_G [19]

MGTYRXP0_231 / MGTYRXN0_231	N2 / N1	pF1_G_RECV0 / nF1_G_RECV0
MGTYTXP0_231 / MGTYTXN0_231	N7 / N6	pF1_G_XMIT0 / nF1_G_XMIT0
MGTYRXP1_231 / MGTYRXN1_231	M4 / M3	pF1_G_RECV1 / nF1_G_RECV1
MGTYTXP1_231 / MGTYTXN1_231	M9 / M8	pF1_G_XMIT1 / nF1_G_XMIT1
MGTYRXP2_231 / MGTYRXN2_231	L2 / L1	pF1_G_RECV2 / nF1_G_RECV2
MGTYTXP2_231 / MGTYTXN2_231	L7 / L6	pF1_G_XMIT2 / nF1_G_XMIT2
MGTYRXP3_231 / MGTYRXN3_231	K4 / K3	pF1_G_RECV3 / nF1_G_RECV3
MGTYTXP3_231 / MGTYTXN3_231	K9 / K8	pF1_G_XMIT3 / nF1_G_XMIT3

pF1_G_RECV0 / nF1_G_RECV0	C112 0.1 UF 0402	C111 0.1 UF 0402	pF2_P_XMIT0 / nF2_P_XMIT0
pF1_G_RECV1 / nF1_G_RECV1	C110 0.1 UF 0402	C109 0.1 UF 0402	pF2_P_XMIT1 / nF2_P_XMIT1
pF1_G_RECV2 / nF1_G_RECV2	C108 0.1 UF 0402	C107 0.1 UF 0402	pF2_P_XMIT2 / nF2_P_XMIT2
pF1_G_RECV3 / nF1_G_RECV3	C106 0.1 UF 0402	C105 0.1 UF 0402	pF2_P_XMIT3 / nF2_P_XMIT3

pF1_G_XMIT0 / nF1_G_XMIT0	C120 0.1 UF 0402	C119 0.1 UF 0402	pF2_P_RECV0 / nF2_P_RECV0
pF1_G_XMIT1 / nF1_G_XMIT1	C118 0.1 UF 0402	C117 0.1 UF 0402	pF2_P_RECV1 / nF2_P_RECV1
pF1_G_XMIT2 / nF1_G_XMIT2	C116 0.1 UF 0402	C115 0.1 UF 0402	pF2_P_RECV2 / nF2_P_RECV2
pF1_G_XMIT3 / nF1_G_XMIT3	C114 0.1 UF 0402	C113 0.1 UF 0402	pF2_P_RECV3 / nF2_P_RECV3

FPGA#2

U78-43
FPGA_VU13P_A2577
GTY QUAD 224 P

ac_pF2R_R0_P [16]
ac_nF2R_R0_P [16]
ac_pF2R_R1_P [19]
ac_nF2R_R1_P [19]

MGTREFCLK0P_224 / MGTREFCLK0N_224 — AT13 / AT12
MGTREFCLK1P_224 / MGTREFCLK1N_224 — AR11 / AR10

MGTYRXP0_224 / MGTYRXN0_224	BA2 / BA1	pF2_P_RECV3 / nF2_P_RECV3
MGTYTXP0_224 / MGTYTXN0_224	BA7 / BA6	pF2_P_XMIT3 / nF2_P_XMIT3
MGTYRXP1_224 / MGTYRXN1_224	AY4 / AY3	pF2_P_RECV2 / nF2_P_RECV2
MGTYTXP1_224 / MGTYTXN1_224	AY9 / AY8	pF2_P_XMIT2 / nF2_P_XMIT2
MGTYRXP2_224 / MGTYRXN2_224	AW2 / AW1	pF2_P_RECV1 / nF2_P_RECV1
MGTYTXP2_224 / MGTYTXN2_224	AW7 / AW6	pF2_P_XMIT1 / nF2_P_XMIT1
MGTYRXP3_224 / MGTYRXN3_224	AV4 / AV3	pF2_P_RECV0 / nF2_P_RECV0
MGTYTXP3_224 / MGTYTXN3_224	AV9 / AV8	pF2_P_XMIT0 / nF2_P_XMIT0

U77-43
FPGA_VU13P_A2577
GTY QUAD 224 P

ac_pF1R_R0_P [16]
ac_nF1R_R0_P [16]
ac_pF1R_R1_P [19]
ac_nF1R_R1_P [19]

MGTREFCLK0P_224 / MGTREFCLK0N_224 — AT13 / AT12
MGTREFCLK1P_224 / MGTREFCLK1N_224 — AR11 / AR10

MGTYRXP0_224 / MGTYRXN0_224	BA2 / BA1	pF1_P_RECV0 / nF1_P_RECV0
MGTYTXP0_224 / MGTYTXN0_224	BA7 / BA6	pF1_P_XMIT0 / nF1_P_XMIT0
MGTYRXP1_224 / MGTYRXN1_224	AY4 / AY3	pF1_P_RECV1 / nF1_P_RECV1
MGTYTXP1_224 / MGTYTXN1_224	AY9 / AY8	pF1_P_XMIT1 / nF1_P_XMIT1
MGTYRXP2_224 / MGTYRXN2_224	AW2 / AW1	
MGTYTXP2_224 / MGTYTXN2_224	AW7 / AW6	
MGTYRXP3_224 / MGTYRXN3_224	AV4 / AV3	
MGTYTXP3_224 / MGTYTXN3_224	AV9 / AV8	

pF1_P_RECV0 / nF1_P_RECV0	C256 0.1 UF 0402	C255 0.1 UF 0402	pF2_G_XMIT0 / nF2_G_XMIT0
pF1_P_RECV1 / nF1_P_RECV1	C258 0.1 UF 0402	C257 0.1 UF 0402	pF2_G_XMIT1 / nF2_G_XMIT1

pF1_P_XMIT0 / nF1_P_XMIT0	C251 0.1 UF 0402	C252 0.1 UF 0402	pF2_G_RECV0 / nF2_G_RECV0
pF1_P_XMIT1 / nF1_P_XMIT1	C254 0.1 UF 0402	C253 0.1 UF 0402	pF2_G_RECV1 / nF2_G_RECV1

THERE IS ONLY SPACE ON THE PCB FOR 8 CAPACITORS. THIS SUPPORTS TWO OF THE FOUR TRANSMIT/RECEIVE PAIRS.

U78-50
FPGA_VU13P_A2577
GTY QUAD 231 G

ac_pF2R_R0_G [16]
ac_nF2R_R0_G [16]
ac_pF2R_R1_G [19]
ac_nF2R_R1_G [19]

MGTREFCLK0P_231 / MGTREFCLK0N_231 — U11 / U10
MGTREFCLK1P_231 / MGTREFCLK1N_231 — T13 / T12

MGTYRXP0_231 / MGTYRXN0_231	N2 / N1	
MGTYTXP0_231 / MGTYTXN0_231	N7 / N6	
MGTYRXP1_231 / MGTYRXN1_231	M4 / M3	
MGTYTXP1_231 / MGTYTXN1_231	M9 / M8	
MGTYRXP2_231 / MGTYRXN2_231	L2 / L1	pF2_G_RECV1 / nF2_G_RECV1
MGTYTXP2_231 / MGTYTXN2_231	L7 / L6	pF2_G_XMIT1 / nF2_G_XMIT1
MGTYRXP3_231 / MGTYRXN3_231	K4 / K3	pF2_G_RECV0 / nF2_G_RECV0
MGTYTXP3_231 / MGTYTXN3_231	K9 / K8	pF2_G_XMIT0 / nF2_G_XMIT0

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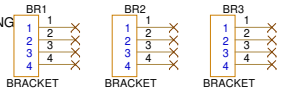
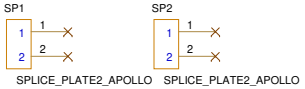
9.99: MECHANICAL PARTS

THESE SHAPES DEFINE MECHANICAL OBJECTS
THAT SHOULD BE IN THE BILL OF MATERIALS.

BRACKETS FOR SUPPORTING A SUB-FRONT PANEL



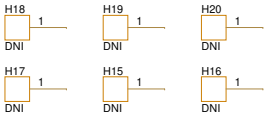
THESE SHAPES DEFINE HOLES AND KEEPOUT AREAS FOR THE SPLICE PLATES.



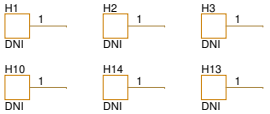
THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINK

THESE HOLES ARE FOR MOUNTING THE LGA80D HEATSINK

THESE STANDOFFS ARE FOR MOUNTING THE BOTTOM COVER. THE STANDOFF IS SOLDERED TO THE BOTTOM SIDE OF THE BOARD.



THESE STANDOFFS ARE FOR MOUNTING THE TOP COVER. THE STANDOFF IS SCREWED FROM THE BOTTOM SIDE OF THE BOARD.



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