

University Roll No. - T91 / ECE / 204058 Page No. - 01 Signature - Archana Kri.
University Roll No. - T91 / ECE / 204058
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Group-A (5 ques.)

- Q) a) At pure semiconductor behaves like an insulator at absolute 0K because at 0K no bond breakdown takes place and hence no ^{free} electron is available for conduction. ^{thermal} → The ~~free~~ electrons in VB don't have the enough energy to overcome the forbidden energy gap.
- b) Silicon is preferred over germanium because:-
 - i) Silicon is abundant on the earth's surface & hence it is cheaper than germanium.
 - ii) Silicon is thermally more stable (temperature stability) while, Germanium is more sensitive to temperature.
 - iii) Low reverse leakage current flows in silicon than in Germanium.
- c) Fermi level is a reference energy level at which the probability of finding an electron of n energy unit above it in CB is equal to the probability of finding a hole of n energy unit below the VB.

Q) Modulation index is the ratio of the amplitude of the modulating signal to the amplitude of the carrier signal. It is denoted by μ .

$$\Rightarrow \mu = \frac{A_m}{A_c} \quad \left\{ \begin{array}{l} \text{where, } A_m = \text{amplitude of modulating signal} \\ A_c = \text{Amplitude of carrier signal} \end{array} \right\}$$

Percentage of modulation: It is the modulation index expressed in percentage [by multiplying μ by 100].

$$\Rightarrow \% \text{ modulation} = \mu \times 100$$

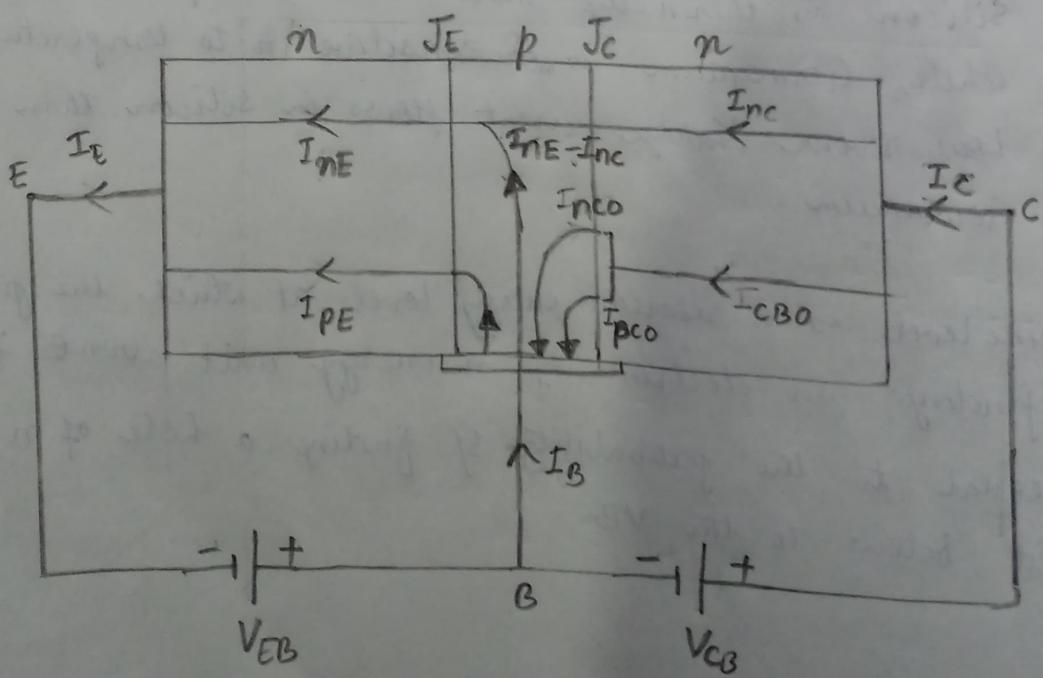
(h) De Morgan's theorem: It states that the complement of product of all terms is equal to the sum of complement of each term.

$$i) \overline{a+b} = \bar{a} \cdot \bar{b}$$

$$ii) \overline{a \cdot b} = \bar{a} + \bar{b}$$

Group-B (4 questions)

3) a)



The above circuit diagram shows the components of current flowing through the NPN transistor across the forward biased emitter junction & in reversed biased collector junction.

Here, n-emitter side is connected to -ve polarity of battery & base-p side is connected to the +, +, +, +.

Also, for collector, n-collected side is connected to +ve polarity & p-base side is connected to -ve polarity of battery.

At emitter side, electrons repels from the -ve polarity of battery & hence the current I_{nE} flows opposite to the base region.

The majority carriers ^{in p region} holes flows from the base to emitter, I_{pE} .
Thus, $I_E = I_{nE} + I_{pE}$. (emitter current).

The majority carrier in n-emitter region flows to ~~the~~ collector region through the base. While diffusion 1-3% of e^- will recombine with the majority carrier holes from base side. Remaining carrier e^- moves to the collector region & a current I_{nC} flows from collector to base.

Thus, the base current $I_B = I_{nE} - I_{nC}$

Now, the minority carrier in collector n side ^{holes} moves to base (repelled by battery) and hence, current, I_{pCO} flows from n to p side (collector) Now, the minority electrons in base, flow to base to collector & a current I_{nCO} flows in opposite direction.

Thus, overall, reverse saturation current, $I_{CBO} = I_{nCO} + I_{pCO}$ flows from collector to base region.

The overall collector current, $I_C = I_{nC} + I_{CBO}$

Here, $I_E = I_B + I_C$ [refer diagram].

(b) PNP :

current amplification factor, $\alpha = \frac{I_C}{I_E}$

Here, given, $\alpha = 0.988$

$$I_E = 1.2 \text{ mA}$$

$$\text{Thus, } I_C = \alpha \cdot I_E$$

$$\text{or, } I_C = 0.988 \times 1.2 \text{ mA}$$

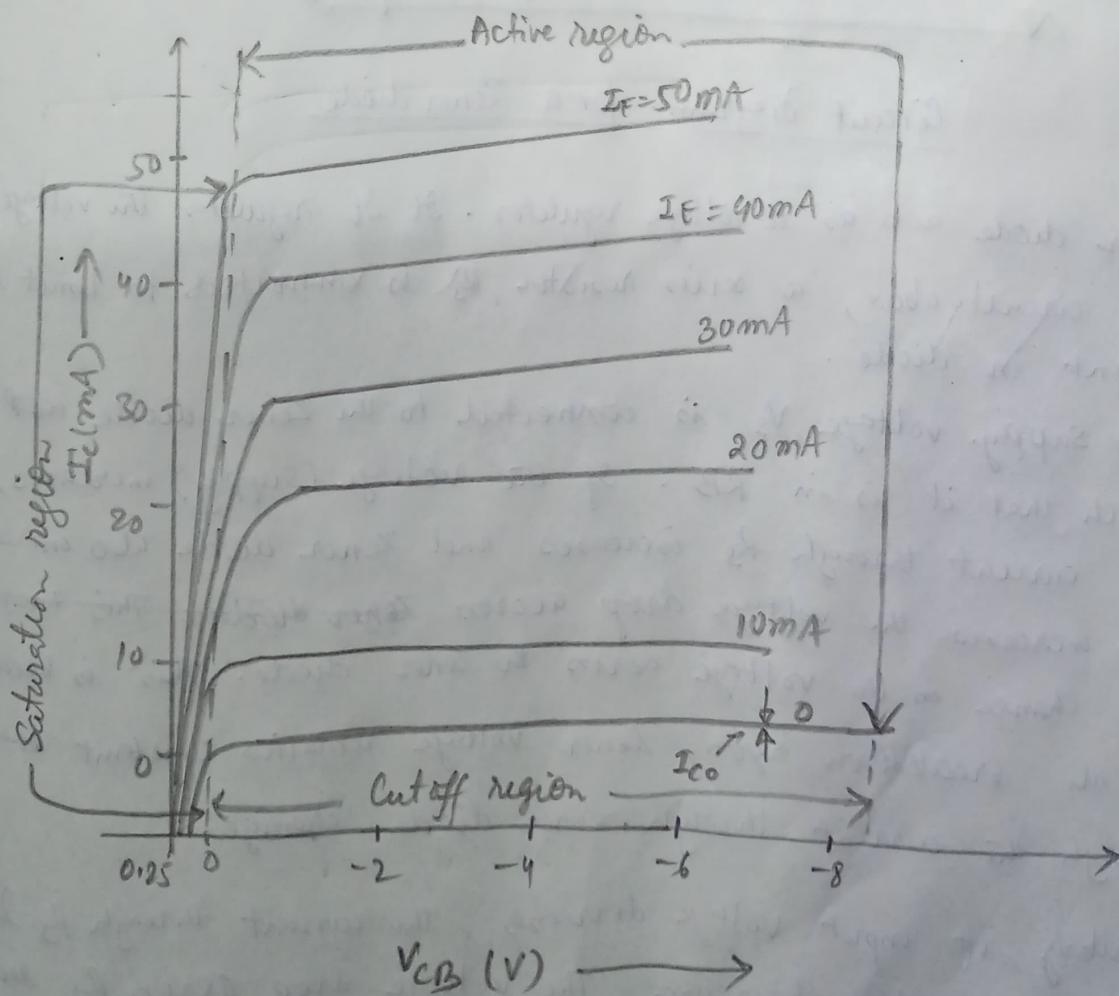
$$\text{or, } I_C = 1.1856 \text{ mA}$$

$$\text{Now, } I_E = I_B + I_C$$

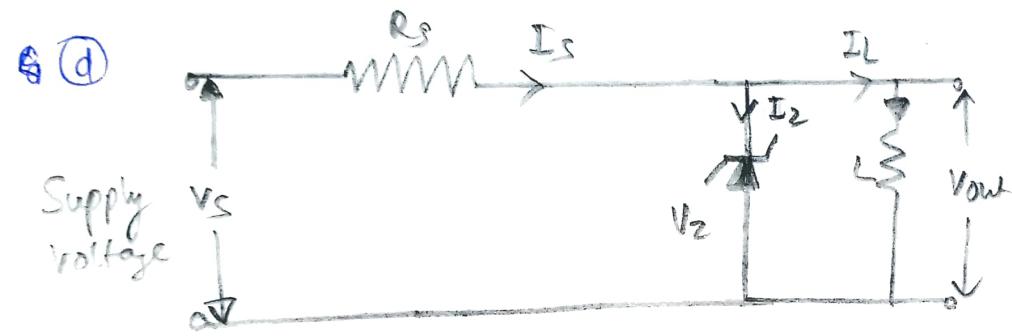
$$\text{Thus, } I_B = I_E - I_C$$

$$\text{or, } I_B = (1.2 - 1.1856) \text{ mA} = 0.0144 \text{ mA.}$$

(c) CE mode



- i) Active region: The region between ~~actn~~ cut off and saturation region where transistor will function normally with CB junction RB & EB junction FB.
- ii) Saturation region: The region in which current, I_E saturates to a constant value. At this ~~pt~~ \Rightarrow , the current is maximum.
- iii) Cut off ~~region~~: ~~At~~ The point where the base-emitter junction no longer remains in FB & normal transistor action is lost. The \ominus CE voltage is nearly equal to V_{cc} . [Refer above graph]



Circuit diagram for a Zener diode

Zener diode acts as a voltage regulator. It regulates the voltage level. In the circuit above, a series resistor, R_s is connected to limit the current in diode.

→ A supply voltage, V_s is connected to the Zener diode ~~so~~ such that it is in RB. If the voltage (supply) increases, the current through R_s increases and Zener diode also increases. This increases the voltage drop across R_s without ~~it~~ increases any change in the voltage across the Zener diode. This is because in the breakdown region, Zener voltage remains constant even though the current through Zener diode changes.

Similarly, if input voltage decreases, the current through R_s & Zener diode also decreases. The voltage drop across R_s decreases ~~but~~ without any change in voltage across Zener diode.

University Roll No.- T91/ECE/204058 Page No.- 6 Signature - Arshaneetkumar

Thus, increase / decrease ~~with~~ in input voltage results in increase / decrease of voltage across R_S without any change in voltage across Zener diode. Thus, Zener acts like a voltage regulator.

① LED is a Semiconductor device that emits light when an electric current is passed through it. It is a heavily doped p-n junction which under F-B emits spontaneous radiation. This diode is encapsulated with a transparent cover so that emitted light can come out.

Q. a) i) $(\bar{A} + B + \bar{C})(\bar{A} + B + D + E)(C + D)$

$$\Rightarrow (\bar{A} + (B + \bar{C})(B + D + E))(C + D)$$

$$\Rightarrow (\bar{A} + B + (\bar{C})(D + E))(C + D)$$

$$\Rightarrow (\bar{A} + B + \bar{C}D + \bar{C}E)(C + D)$$

$$\Rightarrow \bar{A}C + BC + C\bar{C}D + C\bar{C}E + \bar{A}D + BD + \bar{C}DD + \bar{C}ED$$

$$\Rightarrow \bar{A}C + BC + D + \Theta + \bar{A}D + BD + \bar{C}D + \bar{C}DE$$

$$\Rightarrow \bar{A}C + BC + \bar{A}D + BD + \bar{C}D + \cancel{\bar{C}DE}(1 + \bar{E})$$

$$\Rightarrow \bar{A}C + BC + \bar{A}D + BD + \bar{C}D$$

$$\Rightarrow (\cancel{\bar{A} + B})(C + D) + \bar{C}D$$

$$\Rightarrow \bar{A}C + BC + BD + \bar{C}D$$

$$\Rightarrow \bar{A}C + BC + \bar{C}D$$

$\left\{ \begin{array}{l} C\bar{C} = D \\ DD = D \end{array} \right\}$

$\left\{ \begin{array}{l} 1 + \bar{E} = 1 \\ \because 1 + \bar{E} = 1 \end{array} \right\}$

(consensus: $BC + BD + \bar{C}D = BC + \bar{C}D$)

Q.

ii) $\bar{A}\bar{B}C + BC + AC$

$$\Rightarrow (\bar{A}\bar{B} + B)C + AC$$

$$\Rightarrow (B + \bar{B})(B + \bar{A})C + AC$$

$$\Rightarrow (B + \bar{A})C + AC$$

$$\Rightarrow BC + (\bar{A} + A)C$$

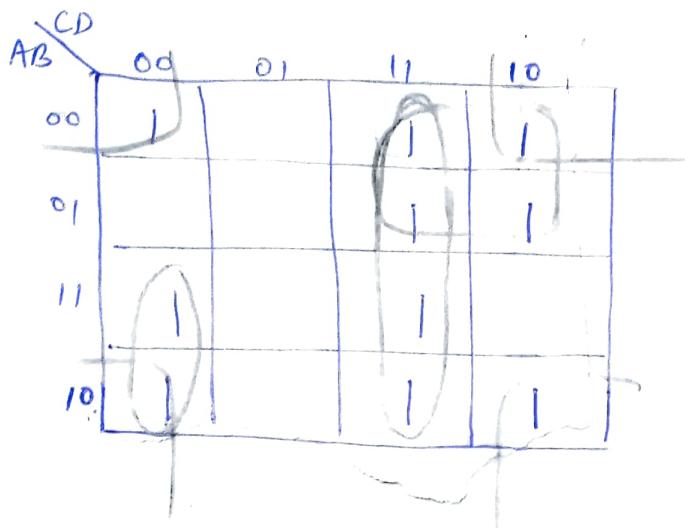
$$\Rightarrow BC + C$$

$$\Rightarrow C(1 + B)$$

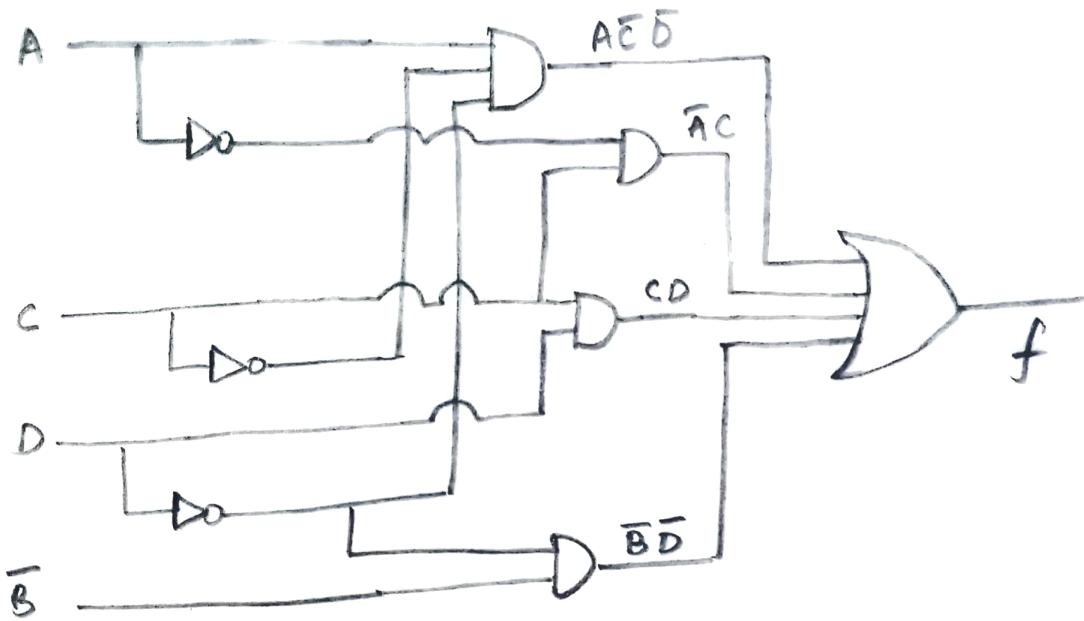
$$\Rightarrow C$$

$\left\{ \begin{array}{l} B + \bar{B} = 1 \\ A + \bar{A} = 1 \\ 1 + B = 1 \end{array} \right\}$

(b) $f(A, B, C, D) = \sum m (0, 2, 3, 6, 7, 8, 10, 11, 12, 15)$

~~Thus~~

Thus, $f(A, B, C, D) = \overline{BD} + \overline{AC} + CD + A\overline{CD}$



i) BCD 974 + 595

$$\begin{array}{r}
 \text{974} \\
 \Rightarrow + \quad 1001 \quad 0111 \quad 0100 \quad (974) \\
 + \quad 0101 \\
 \hline
 1111 \quad 1001 \quad 0101 \quad (595) \\
 + \quad 0110 \\
 \hline
 0110 \quad 0110 \quad 0000 \quad (\text{add 6 if not valid BCD}) \\
 + \quad 0101 \\
 \hline
 1010 \quad 0110 \quad 1001 \quad = 1569
 \end{array}$$

BCD sum :

Q) $(10001110)_2$ to hexadecimal.

$$\Rightarrow (\underline{1000} \ \underline{1110})_2$$

$$2) (8 \ F)_{16} \rightarrow (8F)_{16}$$

④ Full adder

I/P			O/P	
A	B	Cin	Sum	Cout
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

①

For carry (Cin)

A	B Cin			
	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$Cout = AB + A\bar{B}Cin + \bar{A}BCin$$

$$Cout = AB + (A \oplus B)Cin$$

②

For Sum

A	B Cin			
	00	01	11	10
0	0	1	0	1
1	0	1	1	0

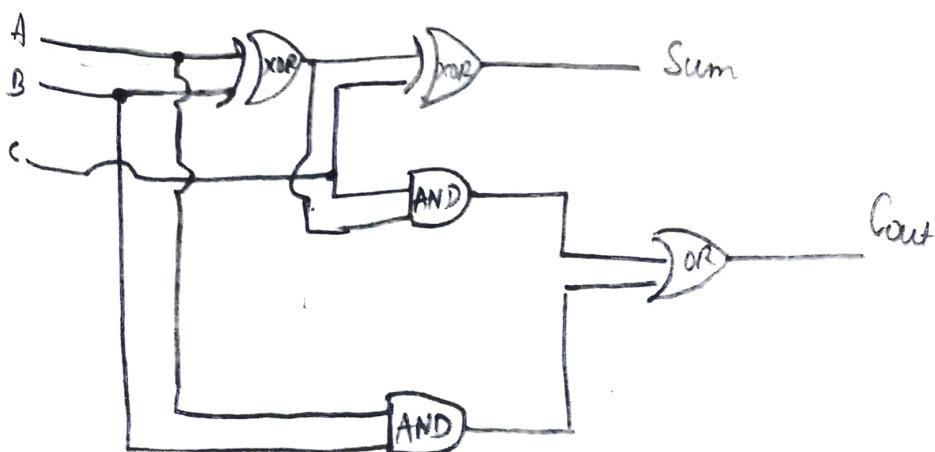
This is a checkboard configuration.

$$\text{Thus, } \text{Sum} = A \oplus B \oplus Cin$$

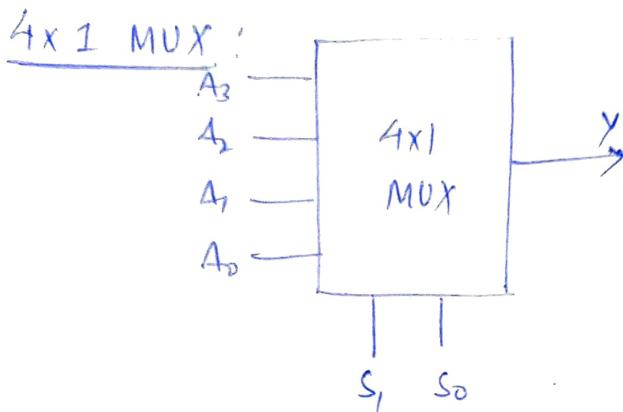
$$\text{Or } \text{Sum} = \bar{A}\bar{B}Cin + \bar{A}\bar{B}\bar{C}in + \bar{A}\bar{B}Cin + ABcin$$

$$\text{Thus, } Cout = AB + (A \oplus B)Cin = AB + (A \oplus B)Cin$$

$$\text{Sum} = \bar{A}\bar{B}Cin + \bar{A}\bar{B}\bar{C}in + \bar{A}\bar{B}Cin + ABcin$$



b) Multiplexers is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of lines is controlled by selection lines. If 2^n input lines then we have n selection lines.



In 4x1 MUX, there are total 4 IP lines ie, A_0, A_1, A_2, A_3 . & 2 selection lines ie, S_0, S_1 . and single OP, Y .

Truth Table

I/P		O/P
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

$$Y = \overline{S_1} \overline{S_0} A_0 + \overline{S_1} S_0 A_1 + S_1 \overline{S_0} A_2 + S_1 S_0 A_3$$

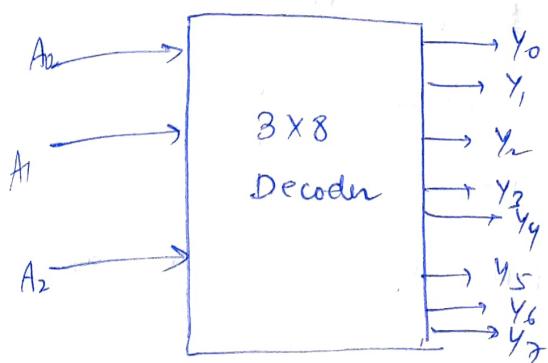
If $S_1 = S_2 = 0$ then, input line A_0 is selected as Y

If $S_1 = 0, S_2 = 1$ then, input line A_1 is selected as output, Y .

If $S_1 = 1, S_2 = 0$ " " " A_2 "

If $S_1 = 1, S_2 = 1$ " " " A_3 "

Thus, the selection lines controls the IP lines to be selected as OP.

① 3×8 Decoder

A decoder converts binary information from n I/P lines to a maximum of 2^n unique O/P lines.

Here, 3 input lines A_0, A_1, A_2 control the 8 O/Ps i.e., $Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6$ and Y_7 .

The circuit has enable input, E . ~~If~~ If $E=0$, the O/P = 0.

If $E=1$ then only the circuit operates.

Here, ~~If~~ If $E=1$: then,

If $A_0 = A_1 = A_2$ then, Y_0 is selected ($Y_0 = 1$)

If $A_0 = 1, A_1 = A_2 = 0$ then, $Y_1 = 1$.

If $A_0 = 1, A_1 = A_2 = 0$ then, $Y_2 = 1$

~~Then~~, If $A_1 = A_0 = 1, A_2 = 0$ then, $Y_3 = 1$

If $A_2 = 1, A_1 = A_0 = 0$ then, $Y_4 = 1$

If $A_2 = 1, A_1 = 0, A_0 = 1$ then, $Y_5 = 1$

If $A_2 = 1, A_1 = 1, A_0 = 0$ then, $Y_6 = 1$

If $A_2 = 1, A_1 = 1, A_0 = 1$ then, $Y_7 = 1$

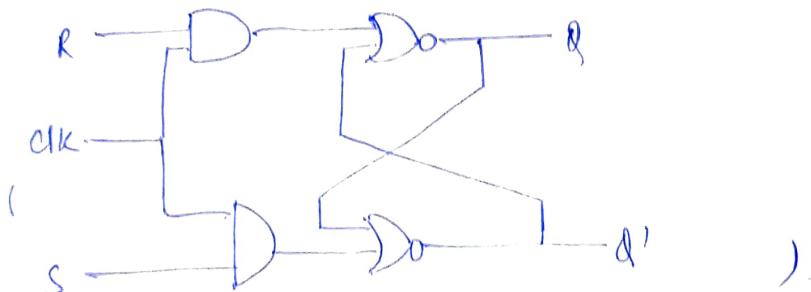
Thus, this acts like a binary to octal decoder. (3×8)

(Q) In sequential circuits, the output at any time depends on the present input values as well as the past output values.

→ It differs from combinational circuits, where, the output at any time depends only on the input values at that time.

→ Eg of sequential circuit are flip-flop, register, counter, clocks etc.

(8) a) SR flip-flop: SR flip flop is a sequential circuit which has 2 inputs that change its state: Reset & Set.
[It has 0 1-bit memory having 2 I/Ps : SET & RESET].

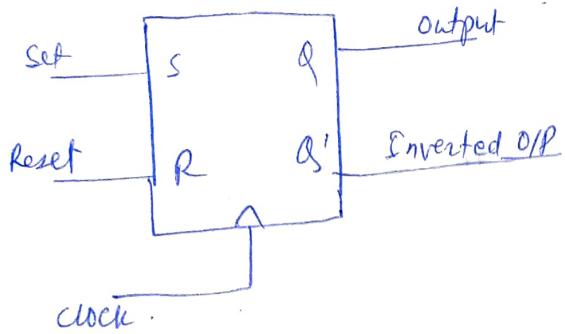


(AND-based SR flip flop.)

→ The single bit set-set reset of SR flip-flop is to a pair of cross coupled 2-input NAND gates (as shown fig 1) where the feedback from each O/P is given as an I/P to the other NAND gate.

S	R	Q	Q'	State
1	0	1	0	Q set to 1
1	1	1	0	No change
0	1	0	1	Q' set to 1
1	1	0	1	No change
0	0	1	1	Undefined / Invalid

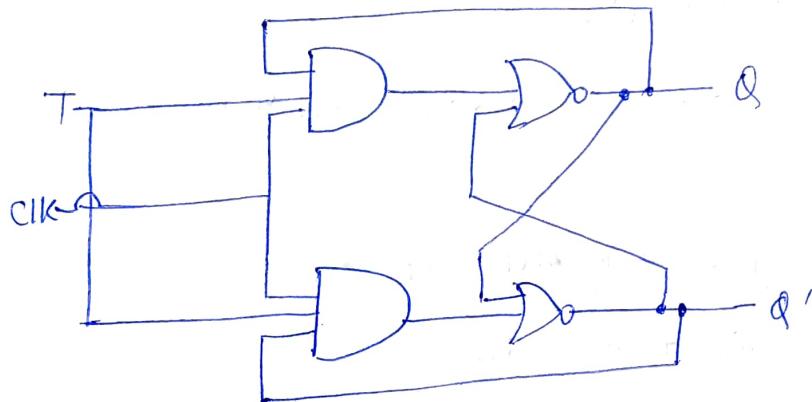
State Table



S	R	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	-

State table.

- b) T flip flop is derived from JK flip flop by connecting both inputs J & K together. This flip flop has only one I/P along with clock signal.
 → It has the ability to complement its state, (Toggle).



T	Q	$Q(t+1)$
0	0	0
1	0	1 ←
0	1	1
1	1	0 ←

Toggle with T.

- c) Modulation is a process of encoding information from a message information from a source in way that is suitable for transmission. By this, some characteristics of carrier signal is varied in accordance with instantaneous value of another signal called modulating signal.

- Types : (1) Amplitude Modulation (AM)
 (2) Frequency Modulation (FM)
 (3) Phase Modulation (PM)

d) Frequency Modulation :- It is a modulation in which the frequency of carrier wave is altered in accordance with the instantaneous amplitude of the modulating signal (keeping phase and amplitude constant).

$$\rightarrow \text{We know : } \phi = \omega_c t + \Phi_c$$

$$\text{On differentiating : } \frac{d\phi}{dt} = \omega_c$$

$$\Rightarrow \phi = \int \omega_c dt$$

$$\text{Instantaneous phase angle, } \phi_i = \int \omega_i dt \quad \text{--- (1)}$$

(where, ω_i is instantaneous frequency of the modulated wave).

$$\rightarrow \text{Expression for frequency : } s(t) = A_c \cos(\phi_i) = A_c \cos(\omega_i t + \Phi_c)$$

Putting ϕ_i from (1),

$$\phi_i = \int (\omega_c + k_f m(t)) dt$$

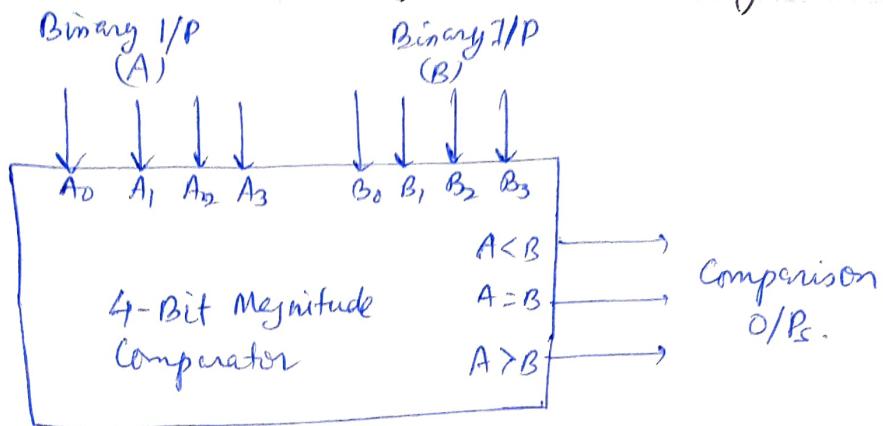
$$= \omega_c t + k_f \int m(t) dt$$

$$\therefore s(t) = A_c \cos [\omega_c t + k_f \int m(t) dt]$$

If phase angle of unmodulated carrier is taken at $t=0$,
exp for frequency modulated wave is :-

$$s(t) = A_c \cos [\omega_c t + k_f \int_0^t m(t) dt]$$

e)



4-Bit Magnitude Comparator, compares two 4-bit nos. A, B . and gives one of the following o/p :-

$$\textcircled{i} \quad A = B$$

$$\textcircled{ii} \quad A < B$$

$$\textcircled{iii} \quad A > B$$

Consider for : $A_3 A_2 A_1 A_0$ & $B_3 B_2 B_1 B_0$

If : $A_3 = 1, B_3 = 0$, Then, $A > B$.

If : $A_3 = A_3$, and if $A_2 = 1$, and $B_2 = 0$, $A > B$

If : $A_3 = B_3$ & $A_2 = B_2$ and if $A_1 = 1, B_1 = 0$ then, $A > B$.

If : $A_3 = B_3$ & $A_2 = B_2$ & $A_1 = B_1$, & ~~if~~ $A_0 = 1$ & $B_0 = 0$ then $A > B$

If $A_3 = B_3, A_2 = B_2, A_1 = B_1, A_0 = B_0$ then, $A = B$.

else $A < B$ (for all case not valid).