

Electronics Practical: To understand the function and use of logic gates.

Soham Chatterjee, ECE, 426

Aim:-

To understand the function and use of logic gates.

Theory:-

Analysis of Logic gates using 7400 (quad 2-input NAND gates), 7402 (quad 2-input NOR gates), 7404 (HEX inverter), 7408 (quad 2-input AND gates), 7432 (quad 2-input OR gates). Diagrams of each chip are shown below:

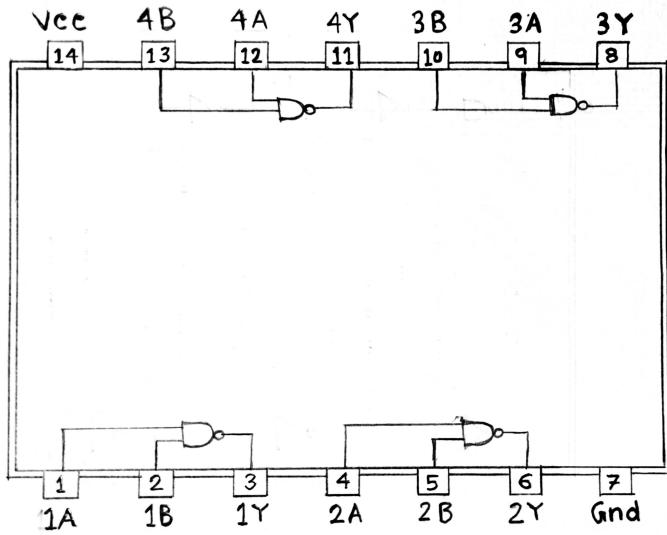


Figure 1: 7400 (quad 2-input NAND gates)

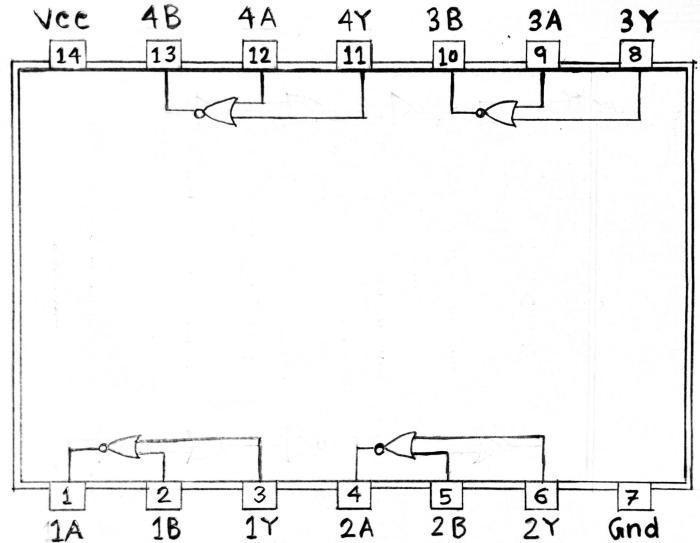


Figure 2: 7402 (quad 2-input NOR gates)

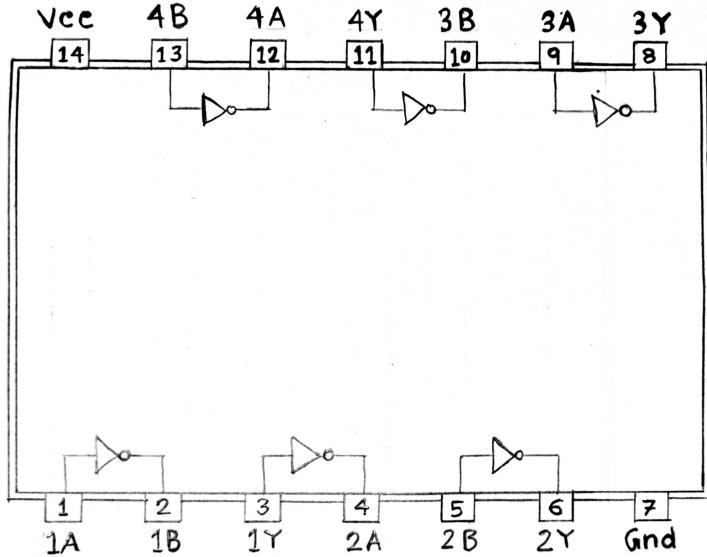


Figure 3: 7404 (HEX inverter)

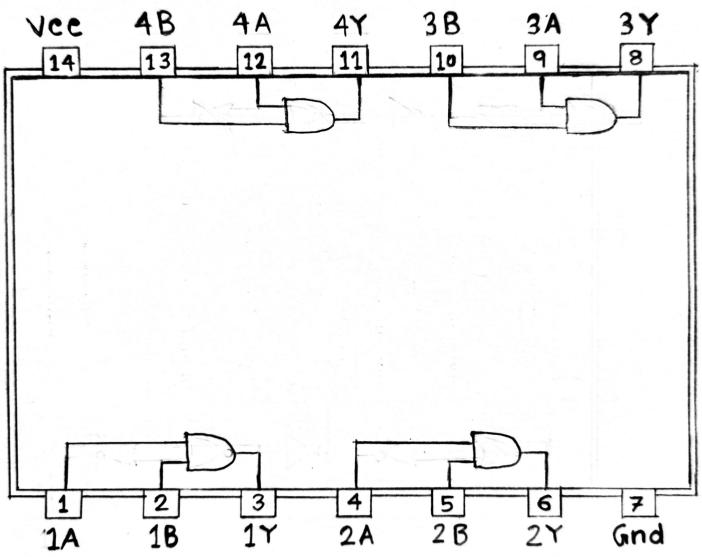


Figure 4: 7408 (quad 2-input AND gates)

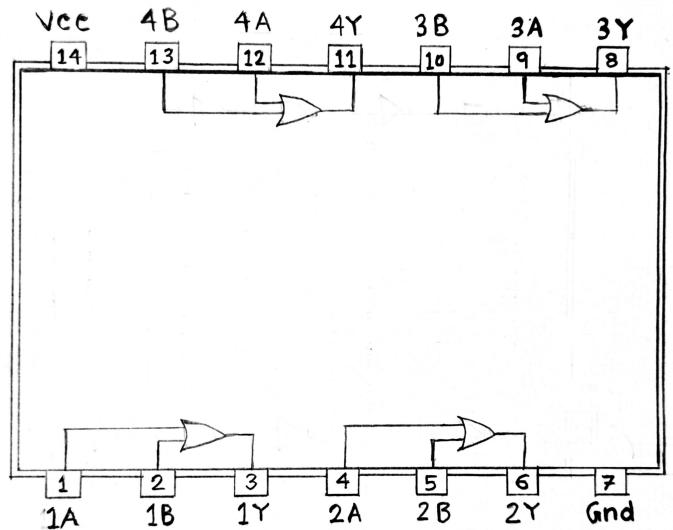


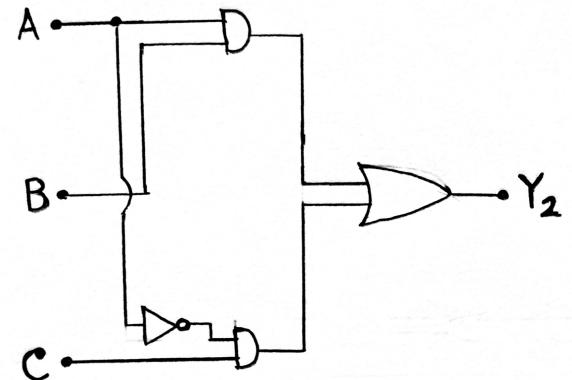
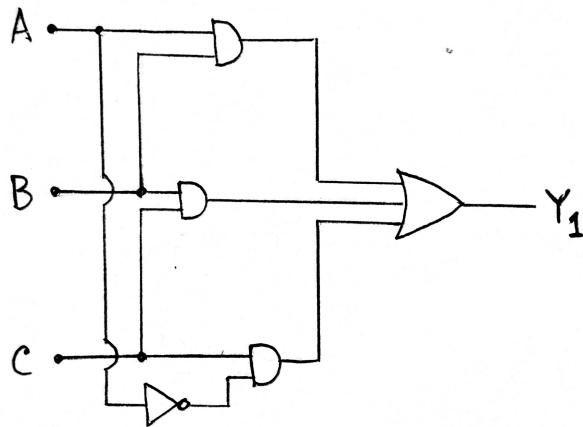
Figure 5: 7432 (quad 2-input OR gates)

Components:-

1. 7400 (Quad 2-Input NAND gates)
2. 7402 (Quad 2-Input NOR gates)
3. 7404 (HEX Inverter)
4. 7408 (Quad 2-Input AND gates)
5. 7432 (Quad 2-Input OR gates)
6. 10 Switches
7. 4 Cells
8. 2 LED's
9. 2 Resistors
10. Wires

Experiment Result:-

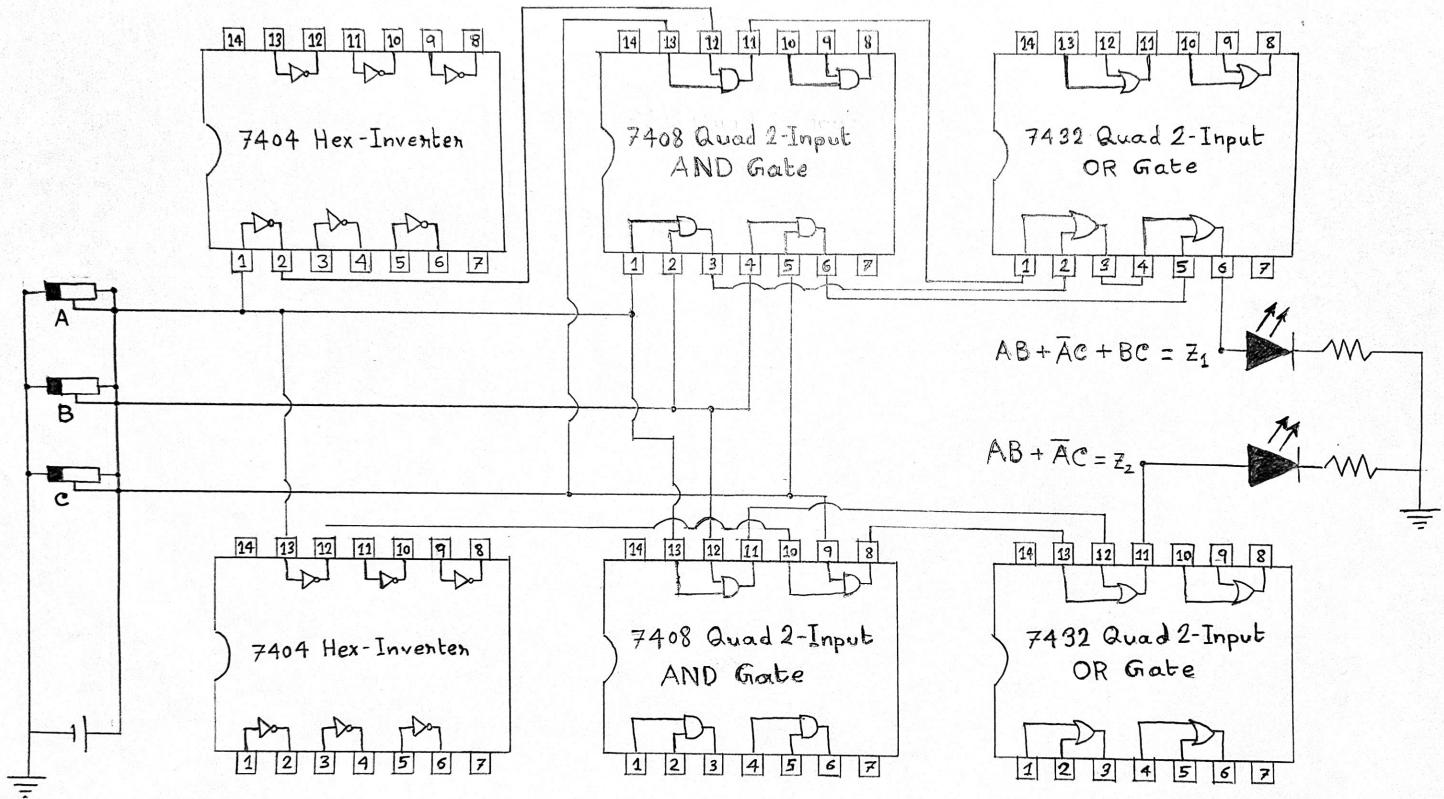
A) $AB + \overline{AC} + BC = AB + \overline{AC}$



Logic Circuit of $AB + \overline{AC} + BC = AB + \overline{AC}$

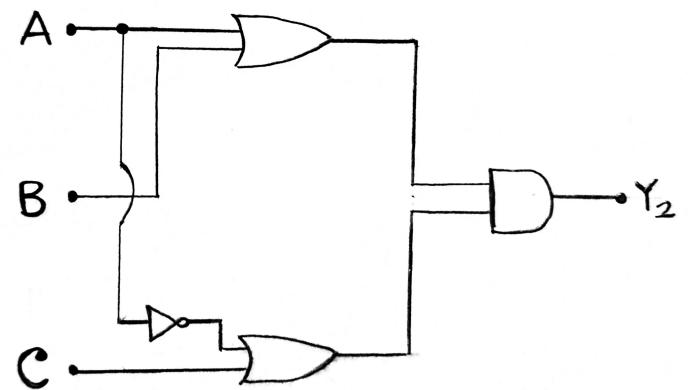
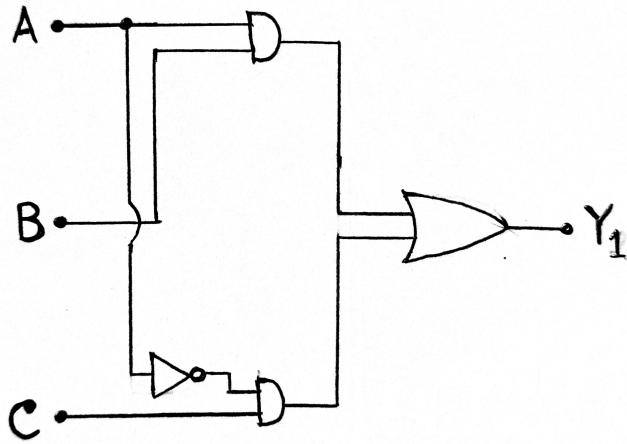
A	B	C	Y_1	Y_2
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	1

Table 1: Truth Table of $AB + \overline{AC} + BC = AB + \overline{AC}$



Circuit 1: Circuit Diagram of $AB + \overline{AC} + BC = AB + \overline{A}C$

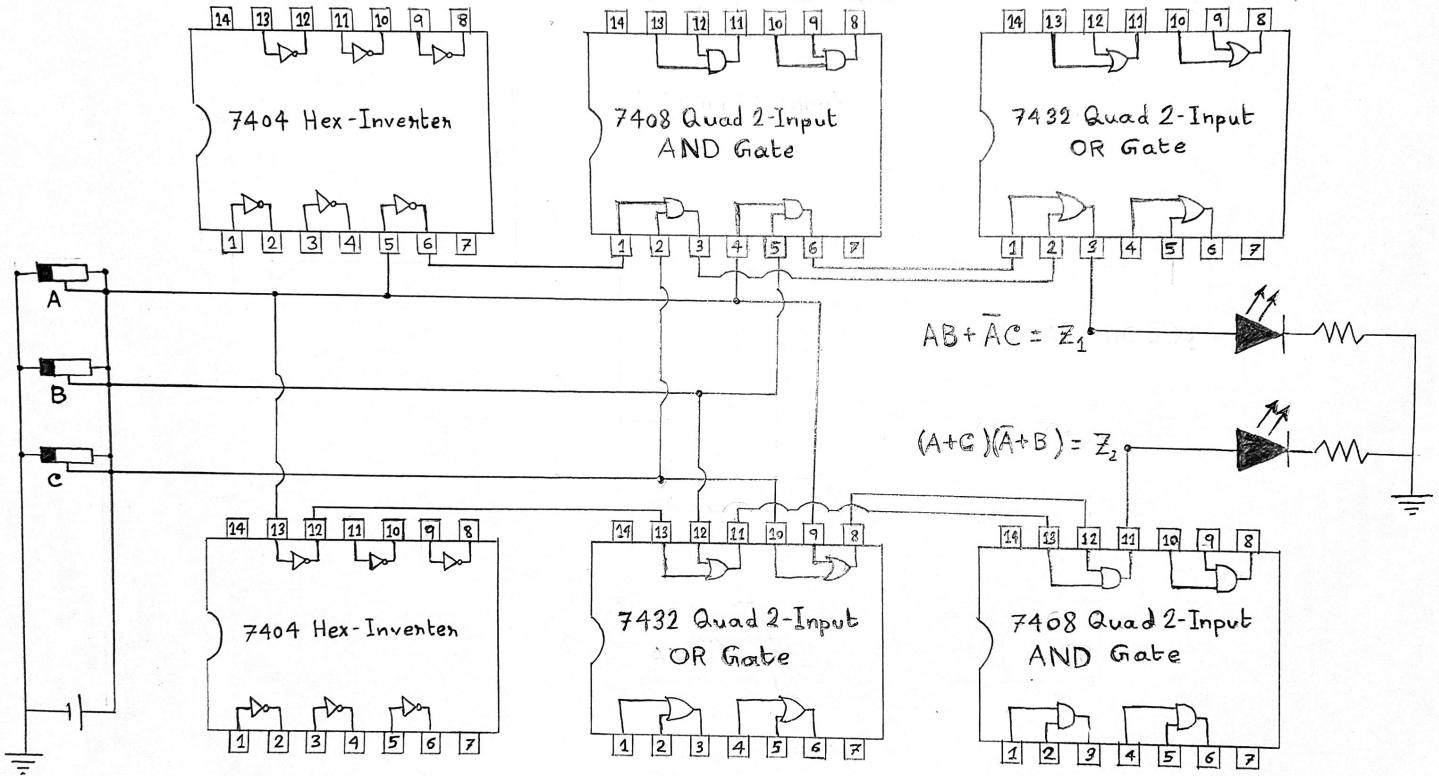
$$B) AB + \overline{A}C = (A+C)(\overline{A}+B)$$



Logic Circuit of $AB + \overline{A}C = (A+C)(\overline{A}+B)$

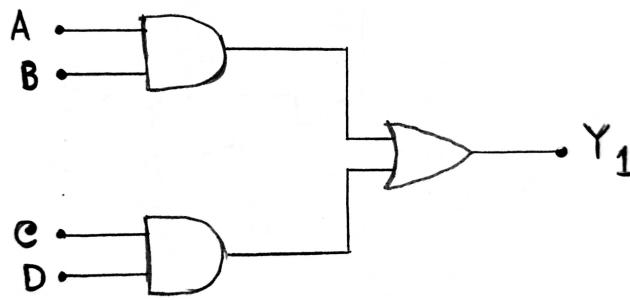
A	B	C	Y_1	Y_2
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	1

Table 2: Truth Table of $AB + \overline{A}C = (A+C)(\overline{A}+B)$

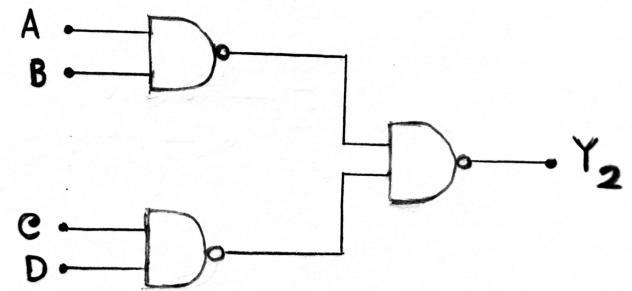


Circuit 2: Circuit Diagram of $AB + \overline{AC} = (A+C)(\overline{A}+\overline{C})$

C) Verify the equivalence of AND-OR and NAND-NAND Structure



L.H.S

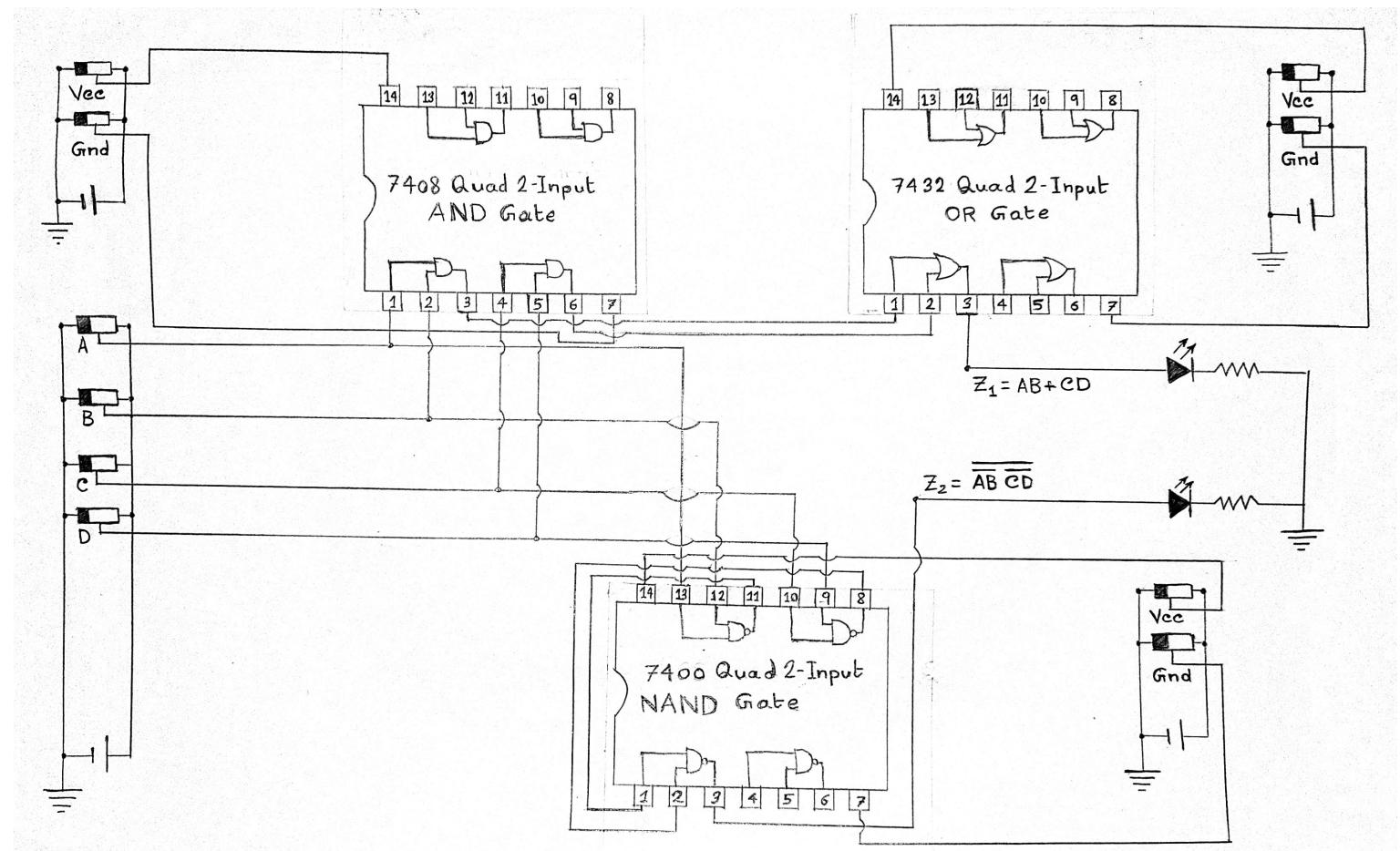


R.H.S

Logic Circuit of $AB+CD = \overline{AB} \overline{CD}$

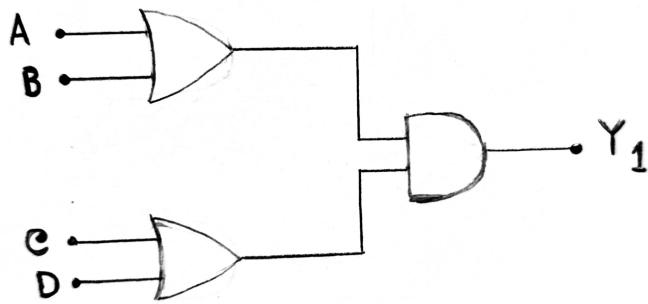
A	B	C	D	Y_1	Y_2
0	0	1	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1
1	1	1	1	1	1

Table 3: Truth Table of $AB+CD = \overline{AB} \overline{CD}$

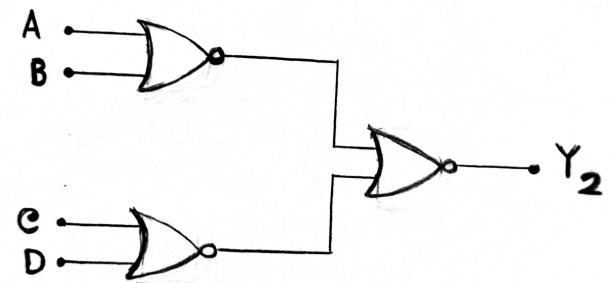


Circuit 3: Circuit Diagram of $AB + CD = \overline{AB} \overline{CD}$

D) Verify the equivalence of OR-AND and NOR-NOR Structure



L.H.S

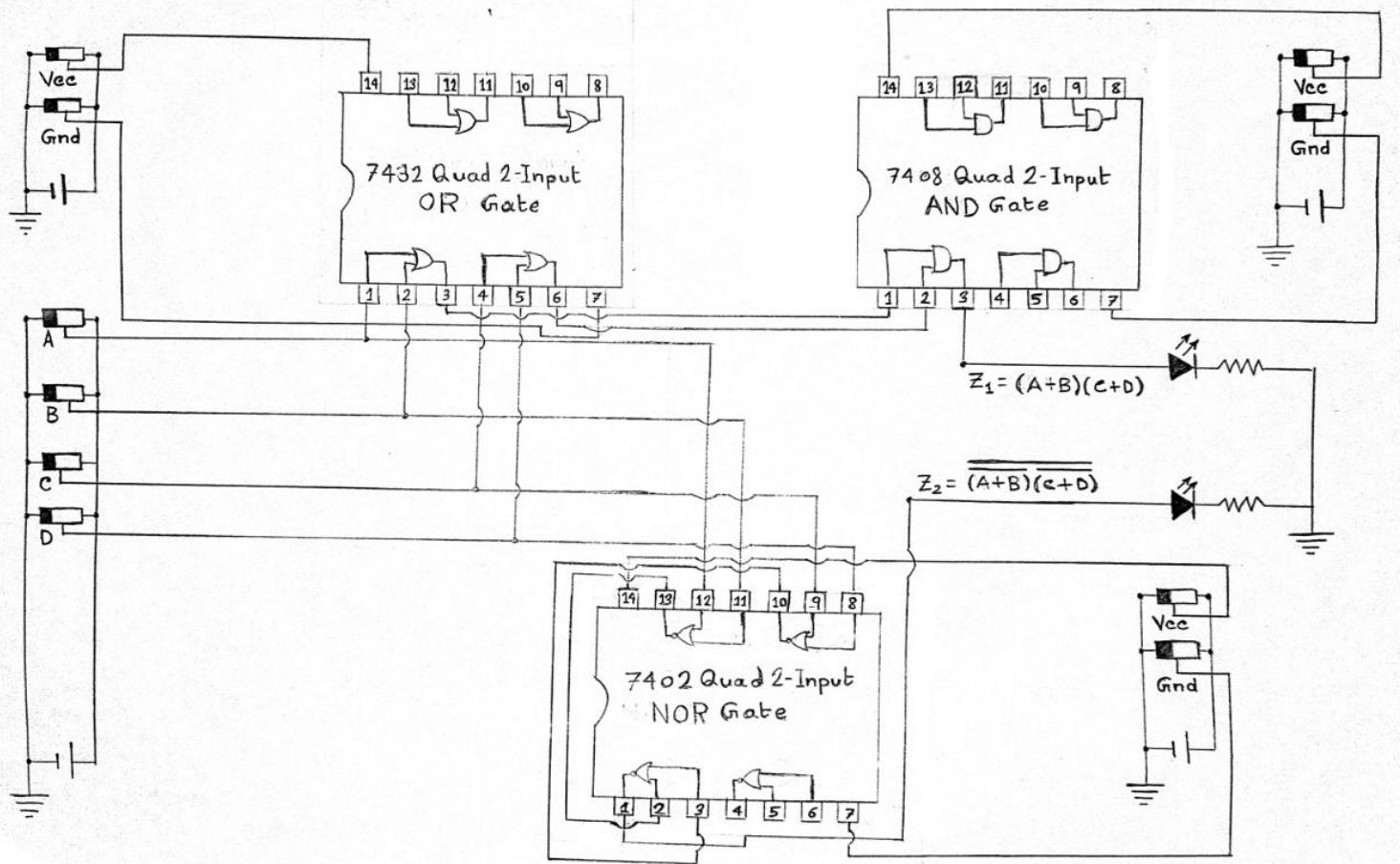


R.H.S

Logic Circuit of $(A+B)(C+D) = \overline{(A+B)} \overline{(C+D)}$

A	B	C	D	Y_1	Y_2
0	0	1	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	1	1	1
1	1	1	1	1	1

Table 4: Truth Table of $(A+B)(C+D) = \overline{(A+B)} \overline{(C+D)}$



Circuit 4: Circuit Diagram of $(A+B)(C+D) = \overline{(A+B)} \overline{(C+D)}$

Electronics Practical: Study on half wave and full wave rectifier and capacitive rectification – and determination of ripple factor without capacitive rectification.

Soham Chatterjee, ECE, 426

Aim:-

Study on half wave and full wave rectifier and capacitive rectification – and determination of ripple factor without capacitive rectification.

Theory:-

Half Wave Rectifier:-

A half wave rectifier is defined as a type of rectifier that only allows one half-cycle of an AC voltage waveform to pass, blocking the other half-cycle. On the positive cycle the diode is forward biased and on the negative cycle the diode is reverse biased. By using a diode we have converted an AC source into a pulsating DC source

The Ripple Factor in a half wave rectifier can be calculated with the following equations,

$$V_{rms} = \frac{V_m}{2}$$

$$V_{dc} = \frac{V_m}{\pi}$$

$$V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

$$\text{Ripple Factor} = \frac{V_{oc}}{V_{dc}}$$

Where,

V_{dc} = Output DC Voltage

V_m = Peak Voltage

Full Wave Rectifier:-

A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output and A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output.

To calculate the Ripple Factor,

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{dc} = \frac{2 \times V_m}{\pi}$$

$$\text{Since, } V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

$$\text{Ripple Factor} = \frac{V_{ac}}{V_{dc}}$$

Where,

V_{dc} = Output DC Voltage

V_m = Peak Voltage

Experimental Data:-

$$V_M = 1 V$$

$$\text{Frequency} = 1000 \text{ hz}$$

$$R_L = 100 \Omega$$

Half Wave Rectifier:-

Circuit Diagram (without capacitor filter):-

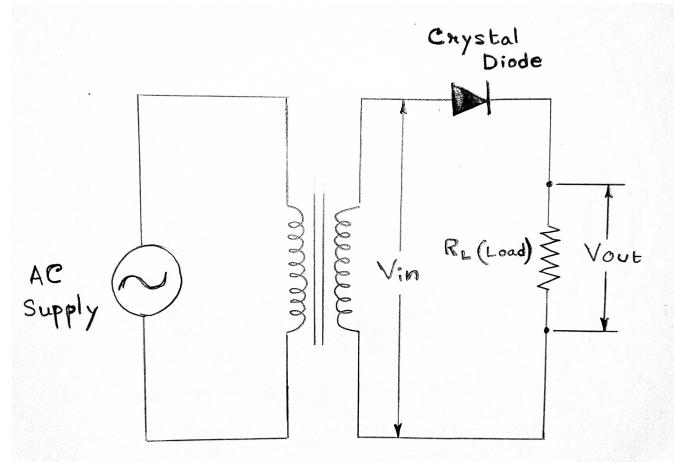


Figure 1: Half Wave Rectifier Circuit

Half Wave Rectifier

INSTRUCTION

OSCILLOSCOPE

Channel 1 Channel 2 Ground Dual

1000 Frequency(Hz)

1 Amplitude(Volt)

CALCULATION

$$V_{\text{rms}} = \frac{V_m}{2}, V_m \text{ is the peak voltage}$$
$$V_{\text{dc}} = \frac{V_m}{\pi}$$
$$\text{Ripple Factor} = \frac{V_m}{V_{\text{dc}}} \quad \text{Since, } V_{\text{ac}} = \sqrt{(V_{\text{rms}}^2 - V_{\text{dc}}^2)}$$

Peak Current: 2.999999892691407 mA

CIRCUIT

Off Check connection Delete all connections

100

Position-Y Position-Y Position-X Time(ms)/div

CONTROLS

1 100V/div 1 100V/div

Position-Y Position-Y Position-X Time(ms)/div

Virtual Oscilloscope Tutorial : [Virtual Oscilloscope Tutorial](#)

Circuit Diagram (with capacitor filter):-

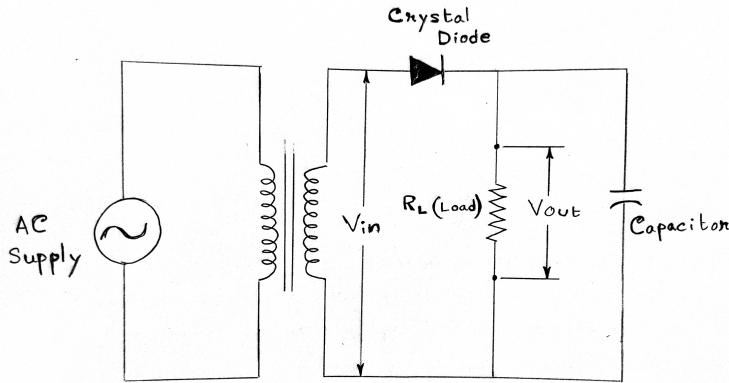


Figure 2: Half Wave Rectifier with Capacitive Rectification Circuit

Capacitative Rectification for Half Wave Rectifier

INSTRUCTION

GRAPH PLOT

Channel 1 Channel 2 Ground Dual

CIRCUIT

Half Wave Rectified Run Simulation Off

CALCULATION

Measure the V_{in}

$$V_{\text{rms}} = \frac{V_{\text{pk}}}{\sqrt{2}}$$

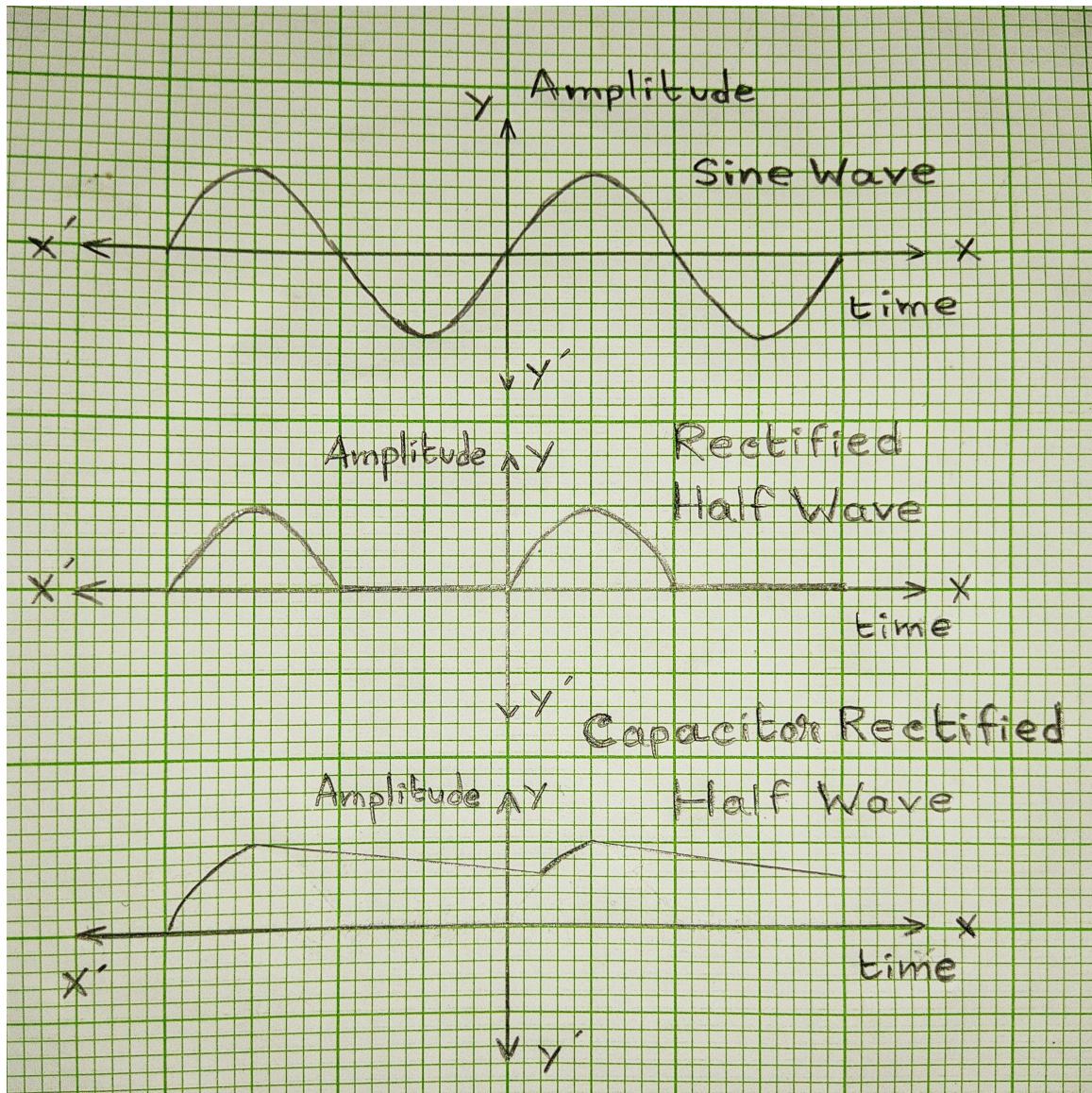
$$V_{\text{dc}} = \frac{V_{\text{pk}}}{\pi}$$

Ripple Factor: $\frac{V_{\text{pk}}}{V_{\text{dc}}} \quad \text{Since, } V_{\text{ac}} = \frac{\sqrt{2}(V_{\text{pk}} - V_{\text{dc}})}{V_{\text{dc}}}$

CONTROLS

V_{Peak} :	<input type="range"/>	<input type="text" value="1"/> V
Position Y-Axis:	<input type="range"/>	<input type="text" value="-1.29"/>
Phase:	<input type="range"/>	<input type="text" value="0"/> Deg
Frequency:	<input type="range"/>	<input type="text" value="1000"/> Hz
V_{Peak2} :	<input type="range"/>	<input type="text" value="1"/> V
Position Y-Axis:	<input type="range"/>	<input type="text" value="0"/>
Phase:	<input type="range"/>	<input type="text" value="0"/> Deg
Frequency:	<input type="range"/>	<input type="text" value="1000"/>

Waveform for Sine Wave, Half Wave Rectified, Half Wave and Capacitive Rectified:-



Calculation of Ripple factor:-

$$\begin{aligned}
 \text{Ripple Factor} &= \frac{V_{ac}}{V_{dc}} \\
 &= \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}} \\
 &= \frac{\sqrt{\left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2}}{\left(\frac{V_m}{\pi}\right)} \\
 &= \frac{\sqrt{\left(\frac{1}{2}\right)^2 - \left(\frac{1}{\pi}\right)^2}}{\left(\frac{1}{\pi}\right)} \\
 &= \sqrt{\left(\frac{\pi}{2}\right)^2 - (1)^2} \\
 &\approx 1.21
 \end{aligned}$$

Full Wave Rectifier:-

Circuit Diagram (without capacitor filter):-

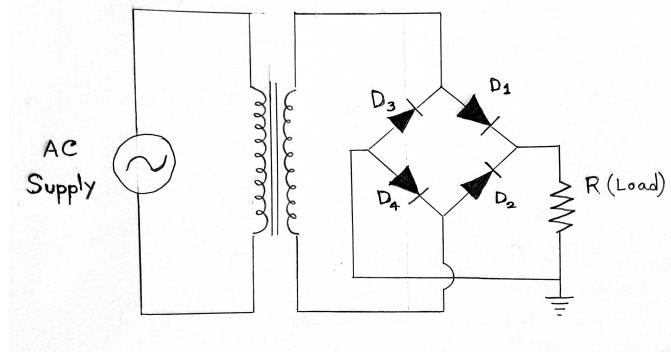
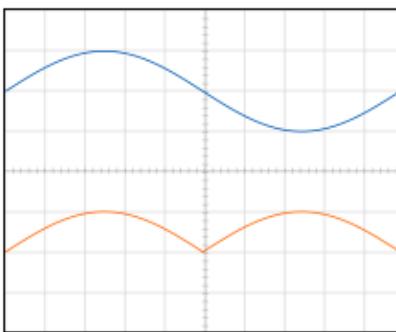


Figure 3: Half Wave Rectifier Circuit

Full Wave Rectifier

INSTRUCTION

OSCILLOSCOPE



Channel 1 Channel 2 Ground Dual

Frequency (Hz) 1000

Amplitude (V/div) 1

CALCULATION

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

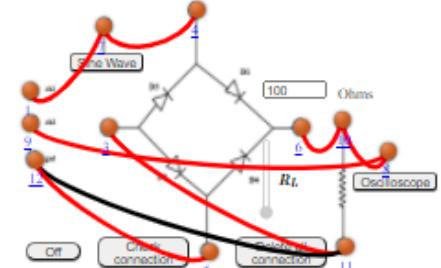
V_m is the peak voltage

$$V_{dc} = \frac{2 \times V_m}{\pi}$$

Ripple Factor = $\frac{V_{ac}}{V_{dc}}$ Since, $V_{dc} = \sqrt{(V_{max}^2 - V_{min}^2)}$

Peak Current: 2.9999999992691407 mA

CIRCUIT



Off Channel connection Ground connection 100 Ohms

CONTROLS

Position-Y Channel 1 Position-Y Channel 2

1 V/div 1 V/div

Position-X Time (ms)/div 0.1

Circuit Diagram (with capacitor filter):-

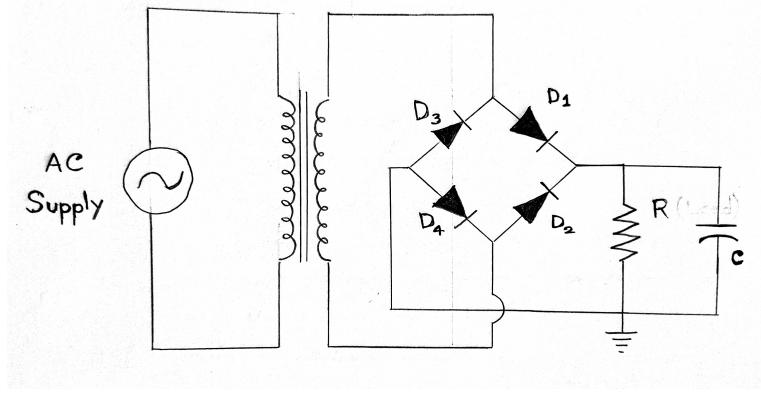


Figure 4: Half Wave Rectifier with Capacitive Rectification Circuit

Capacitative Rectification for Full Wave Rectifier

INSTRUCTION

GRAPH PLOT

Channel 1 Channel 2 Ground Dual

CIRCUIT

Full Wave Rectified Run Simulation Off

CALCULATION

Measure the V_{dc}

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

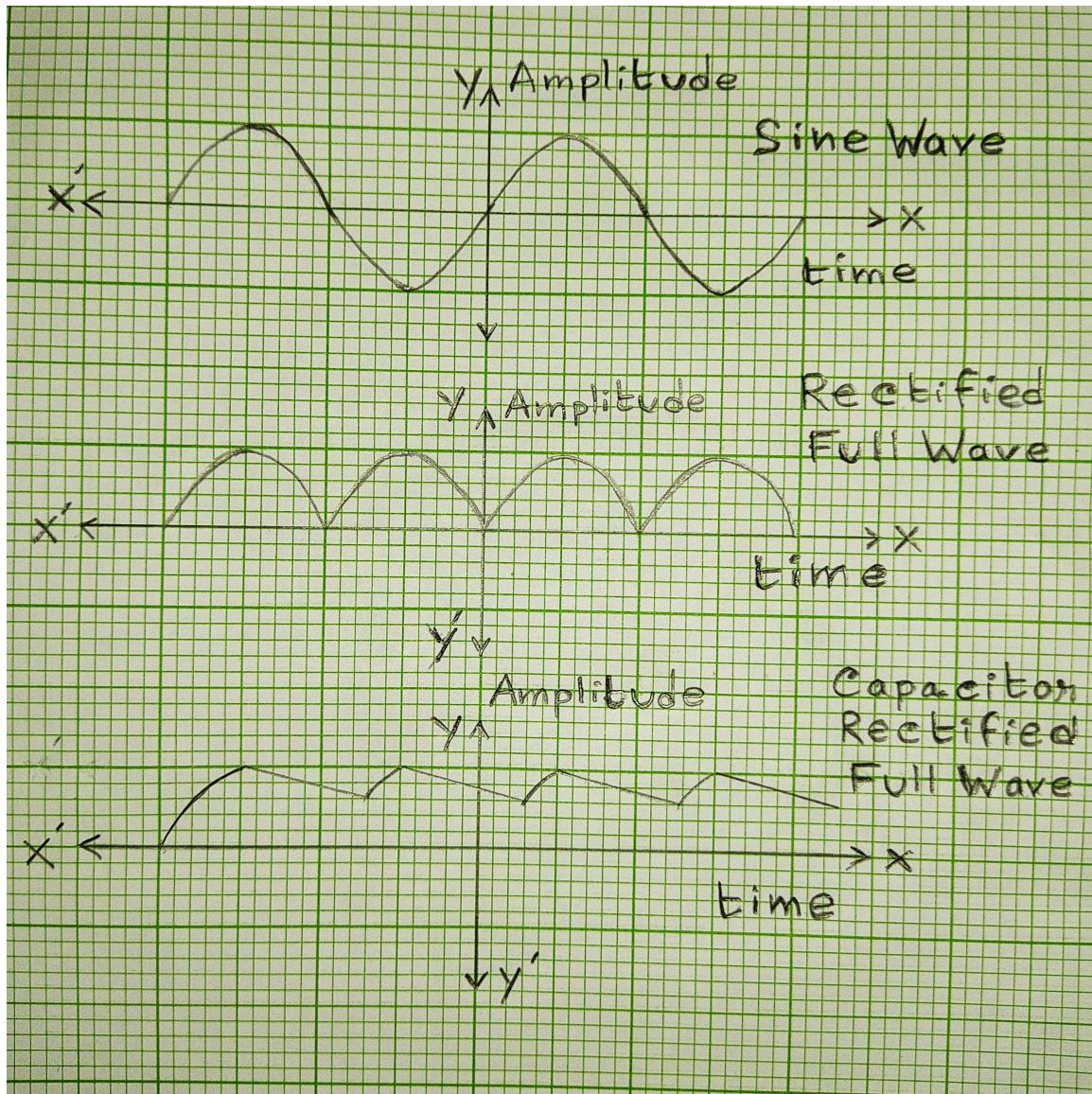
$$V_{dc} = \frac{V_m}{\pi}$$

Ripple Factor: $\frac{V_{dc}}{V_{dc}}$ Since, $V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$

CONTROLS

V _{Peak1} :	<input type="range"/>	1	V
Position Y-Axis:	<input type="range"/>	-1.71	
Phase:	<input type="range"/>	0	Deg
Frequency:	<input type="range"/>	1000	Hz
V _{Peak2} :	<input type="range"/>	1	V
Position Y-Axis:	<input type="range"/>	0	
Phase:	<input type="range"/>	0	Deg
Frequency:	<input type="range"/>	1000	

Waveform for Sine Wave, Half Wave Rectified, Half Wave and Capacitive Rectified:-



Calculation of Ripple factor:-

$$\begin{aligned}
 \text{Ripple Factor} &= \frac{V_{oc}}{V_{dc}} \\
 &= \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}} \\
 &= \frac{\sqrt{\left(\frac{V_m}{\sqrt{2}}\right)^2 - \left(\frac{2 \cdot V_m}{\pi}\right)^2}}{\left(\frac{2 \cdot V_m}{\pi}\right)} \\
 &= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - (1)^2} \\
 &\approx 0.48
 \end{aligned}$$

Conclusion:-

While the half-wave rectifier circuit converts only half the complete AC waveform to DC, the full-wave rectifier circuit converts the entire AC input waveform into DC. We also observe that adding a capacitor filter to the above circuits ‘dampens’ the waveform by a significant factor, especially towards the points where the output DC signal becomes zero, instead converting the above points to about midway of the peak voltage.

Electronics Practical: Study of V-I Characteristics of a P-N Diode
under forward bias and reverse bias.

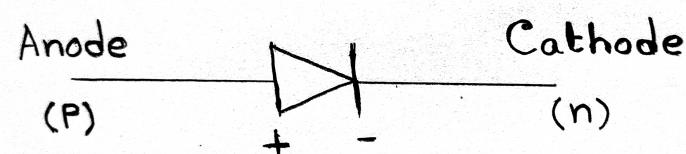
Soham Chatterjee, ECE, 426

Aim:-

Study of V-I Characteristics of a P-N Diode under forward bias and reverse bias.

Theory:-

The diode is a device formed from a junction of N-type and P-type semiconductor material. The lead connected to the P-type material is called the anode and the lead connected to the N-type material is the cathode



Function:-

In function Bias with increasing forward-bias voltage, the depletion zone eventually becomes thin enough that the zone's electric field cannot counteract charge carrier motion across the P-N junction, which as a consequence reduces electrical resistance. The electrons that cross the P-N junction into the P-type material (or holes that cross into the N-type material) will diffuse into the nearby neutral region. The amount of minority diffusion in the near-neutral zones determines the amount of current that may flow through the diode.

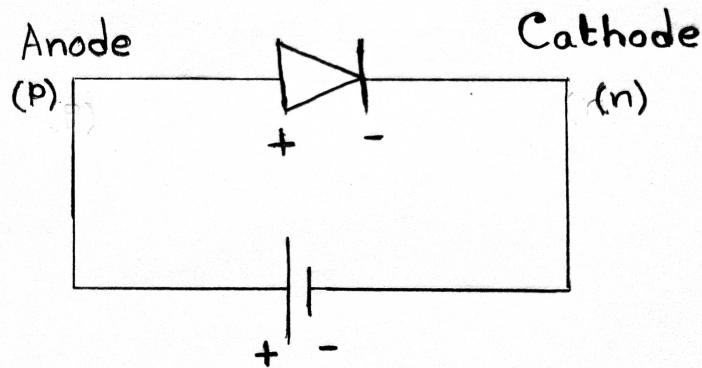


Figure 1: Forward biased P-N Junction Diode

While in Reverse Bias, the positive terminal of battery is connected to the N-side (cathode) and the negative terminal of battery is connected to the P-side (anode) of a diode. Therefore, very little current will flow until the diode breaks down.

Diode Equation:-

In the forward-biased and reversed-biased regions, the current (I_f), and the voltage (V_f), of a semiconductor diode are related by the diode equation.

$$I_f = I_s \times \left(e^{\frac{V_f}{n \times V_r}} - 1 \right)$$

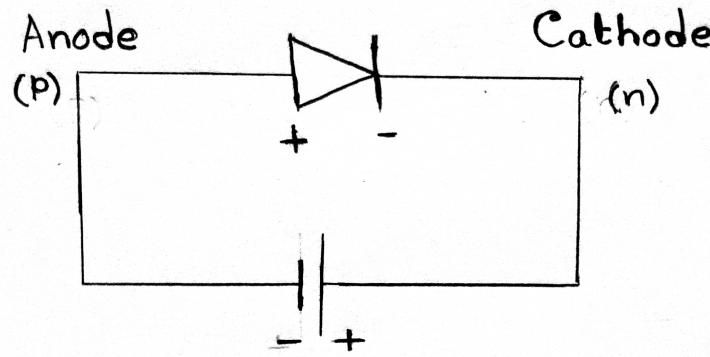


Figure 2: Reverse biased P-N Junction Diode

where,

I_s is reverse saturation current or leakage current.

I_f is current through the diode (forward current).

V_f is potential difference across the diode terminals (forward voltage).

V_T is thermal voltage, given by,

$$V_T = \frac{k \times T}{q}$$

Experimental Data:-

Forward Biased Characteristics:-

Diode: 1N4001

Knee Voltage: 0.6 V

Resistance: 100Ω

L.C. of Ammeter: 0.1 mA

L.C. of Voltmeter: 0.01 V

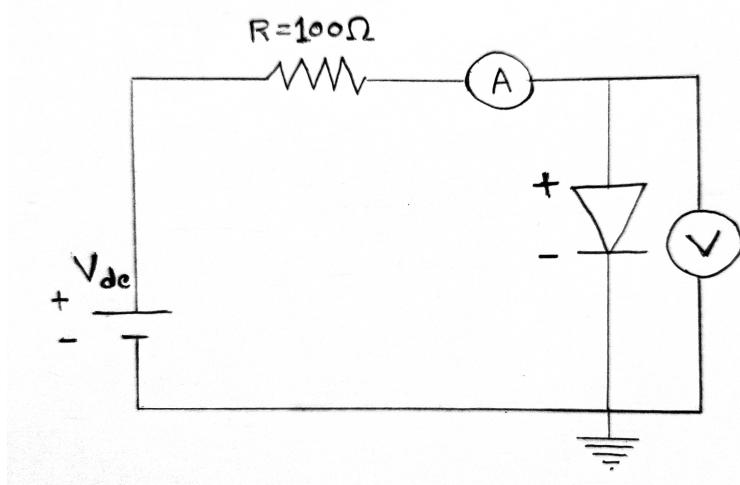


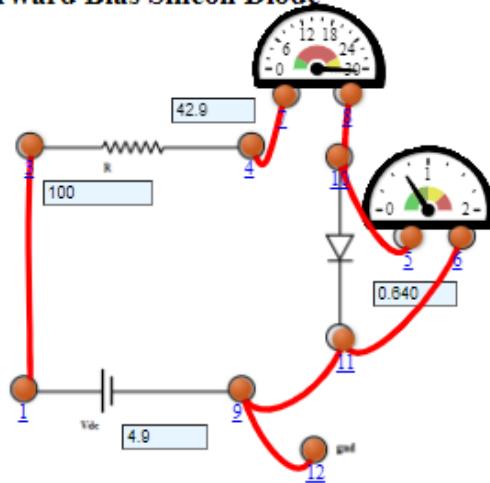
Figure 3: Circuit for Forward biased Silicon Diode

INSTRUCTION

EXPERIMENTAL TABLE

Serial No.	Forward Voltage(Volt)	Forward Current(mAmp)
1	0	0
2	0.589	0.997
3	0.601	4.99
4	0.611	9.97
5	0.620	16.9
6	0.630	26.9
7	0.640	42.9

Forward Bias Silicon Diode



CONTROLS

Select Diode: IN4001 V_F 0.6
 DC volt: Volt
 Resistance: ohms

Add to Table Plot Clear

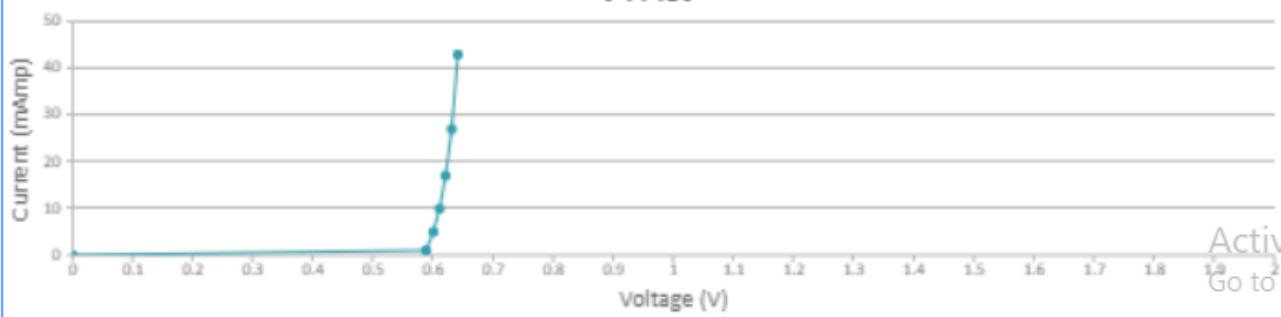
Check connection Delete all connection

Print It

Check for Reverse Bias

GRAPH PLOT

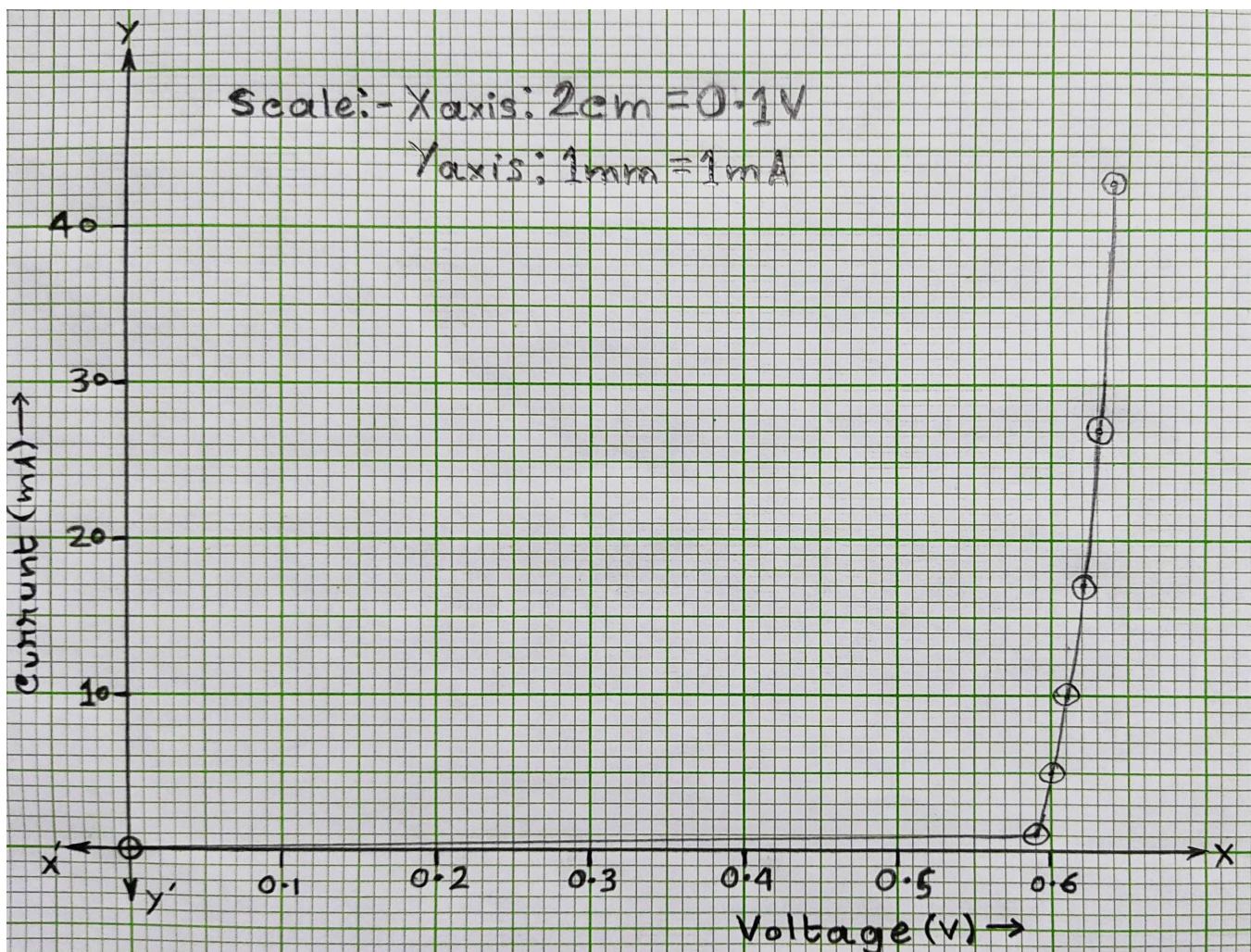
V-I Plot



Activate Windows
Go to Settings to activate !

SI	Resistance (in Ω)	Forward Voltage (in V)	Forward Current (in mA)
1	100	0	0
2	100	0.58	0.99
3	100	0.60	4.99
4	100	0.611	9.97
5	100	0.62	16.9
6	100	0.63	26.9
7	100	0.64	42.9

Table 1: Observation Table for Forward Biased Silicon Diode



Graph 1: Forward Biased Silicon Diode V-I Plot

Reverse Biased Characteristics:-

Diode: 1N4001

Knee Voltage: 0.6 V

Resistance: 100Ω

L.C. of Ammeter: $0.1\mu A$

L.C. of Voltmeter: 0.1 V

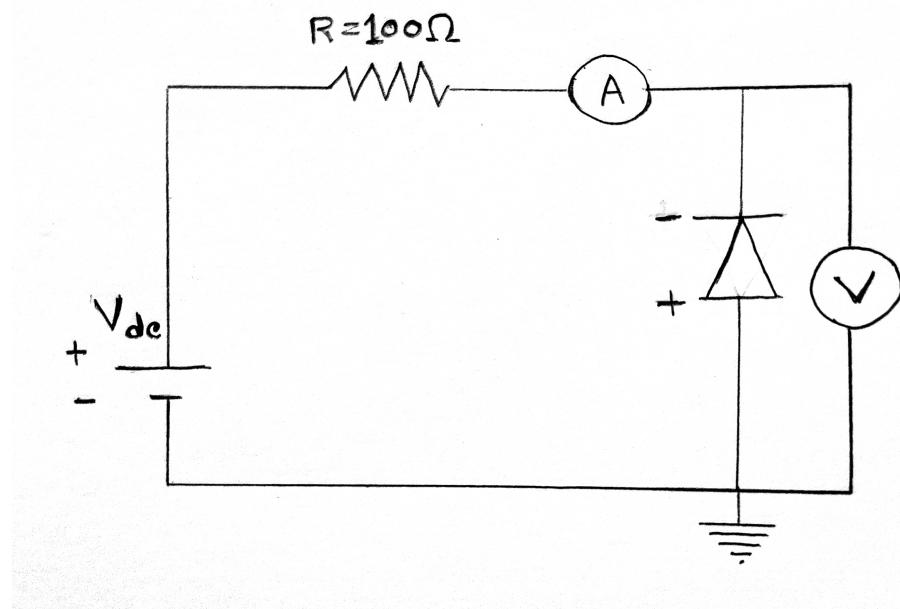


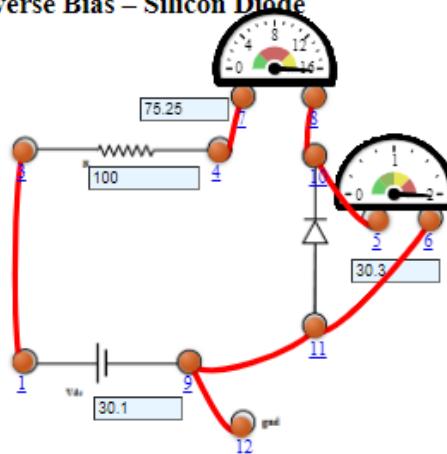
Figure 4: Circuit for Reverse biased Silicon Diode

INSTRUCTION

EXPERIMENTAL TABLE

Serial No.	Reverse Voltage(Volt)	Reverse Current(μ Amp)
1	0.170	0.100
2	5.04	0.100
3	10.0	0.100
4	15.0	0.100
5	20.0	0.100
6	25.0	0.100
7	30.3	75.25

Reverse Bias – Silicon Diode



CONTROLS

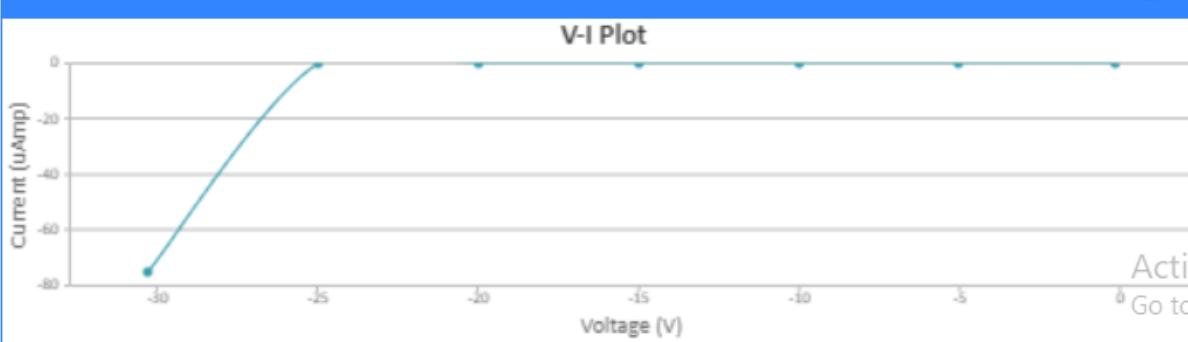
Select Diode: 1N4001 | V_R : 30
DC volt: Volt
Resistance: ohms

Add to Table Plot Clear

Check connection Delete all connection

Print It

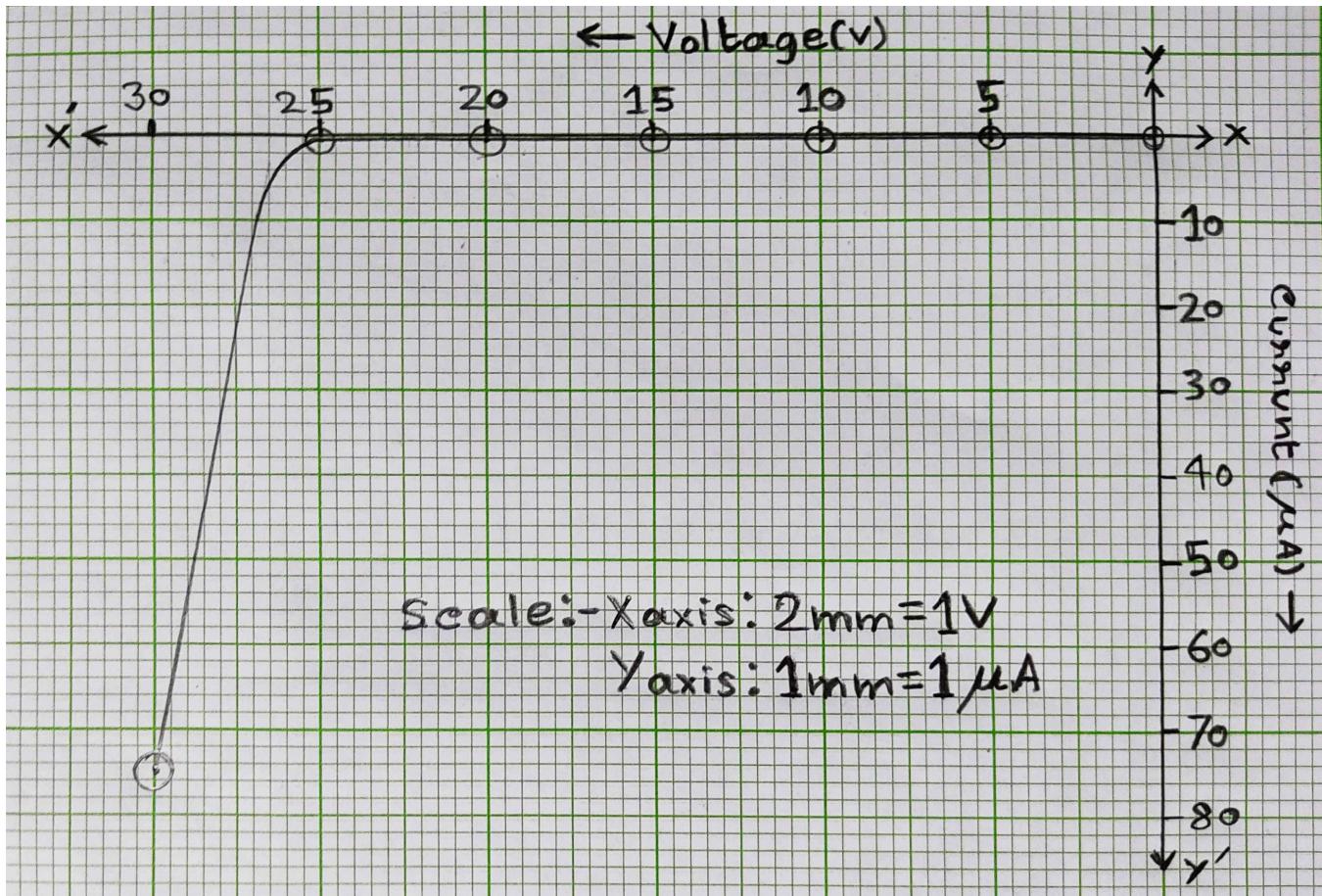
GRAPH PLOT



Activate Windows
Go to Settings to activate \

SI	Resistance (in Ω)	Reverse Voltage (in V)	Reverse Current (in μA)
1	100	0.17	0.1
2	100	5.04	0.1
3	100	10.0	0.1
4	100	15.0	0.1
5	100	20.0	0.1
6	100	25.0	0.1
7	100	30.3	75.25

Table 2: Observation Table for Reverse Biased Silicon Diode



Graph 2: Reverse Biased Silicon Diode V-I Plot

Conclusion:-

From the V-I characteristic graph of forward biased Si diode reveals that there is an almost flat, linear rise until the value of knee voltage of that particular diode is surpassed, and after that, there is a steep linear rise in the current flowing through the diode.

From the V-I characteristic graph of reverse biased Si diode reveals that the reverse voltage remains a flat line until the breakdown of the P-N junction (at breakdown voltage), after which, there is a steep linear rise in the current flowing through the diode.

Electronics Practical: Study the V-I Characteristics of Zener Diode under Reverse Bias and Forward Bias.

Soham Chatterjee, ECE, 426

Aim:-

Study the V-I Characteristics of Zener Diode under Reverse Bias and Forward Bias.

Theory:-

A Zener Diode is a special kind of diode which permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above the breakdown voltage or Zener voltage. Zener diodes are designed so that their breakdown voltage is much lower. In the reverse bias direction, there is practically no reverse current flow until the breakdown voltage is reached. When this occurs there is a sharp increase in reverse current. Varying amount of reverse current can pass through the diode without damaging it. The breakdown voltage or Zener voltage (V_Z) across the diode remains relatively constant.

A voltage regulator is an electronic circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations. A Zener diode of break down voltage V_Z is reverse connected to an input voltage source V_I across a load resistance R_L and a series resistor R_S . The voltage across the Zener will remain steady at its break down voltage V_Z for all the values of Zener current I_Z as long as the current remains in the break down region. Hence a regulated DC output voltage $V_o = V_Z$ is obtained across R_L whenever the input voltage remains within a minimum and maximum voltage.

There are two types of regulations:

1. **Line Regulation:** In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.

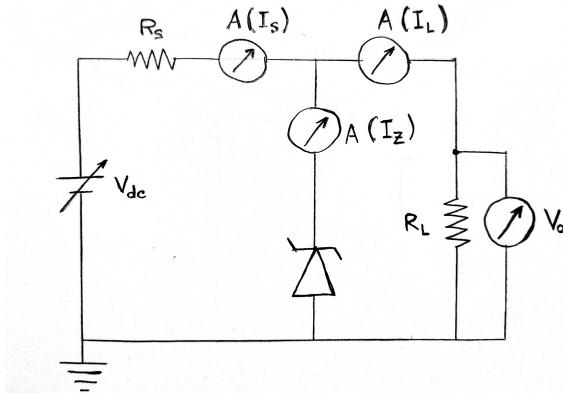


Figure 1: Circuit for Line Regulation of Voltage Regulator

2. **Load Regulation:** In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

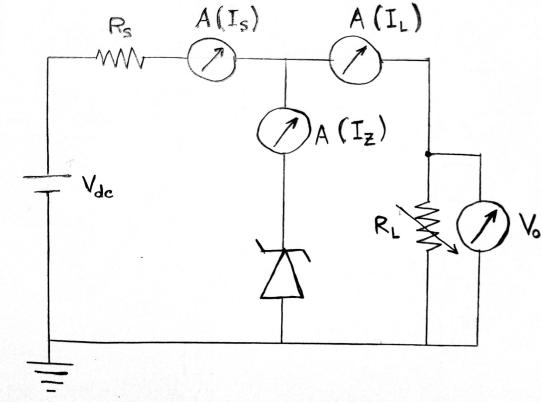
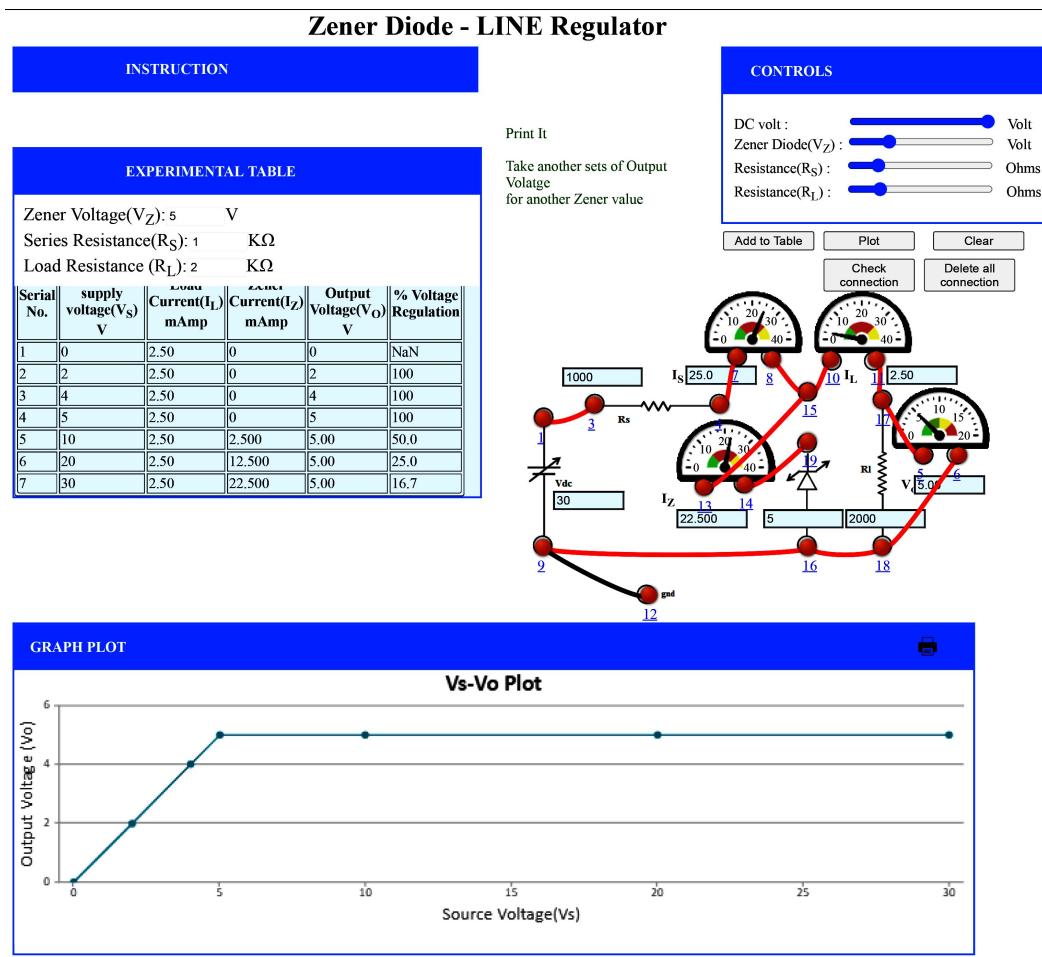


Figure 2: Circuit for Load Regulation of Voltage Regulator

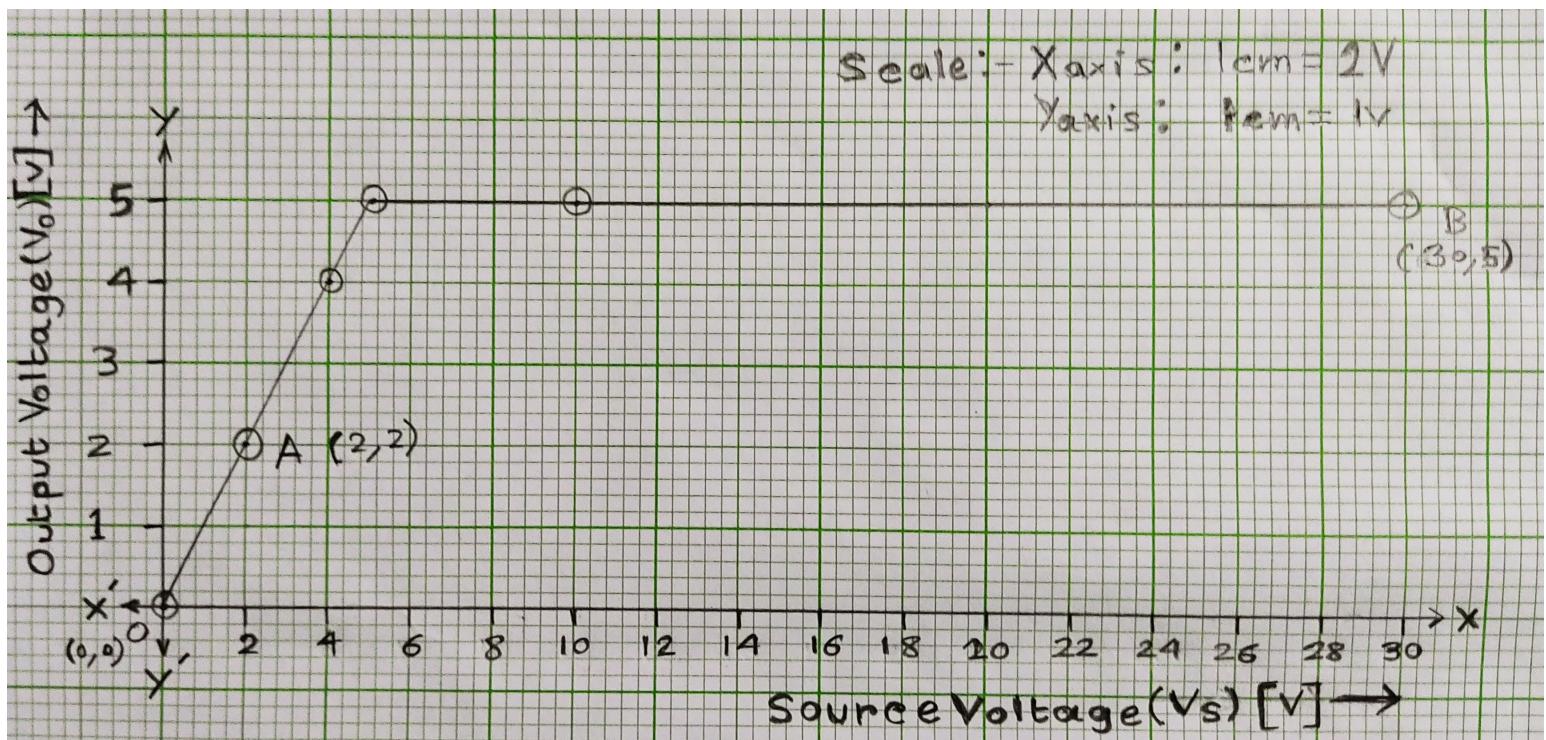
Experimental Data:-

Line Regulation:-



Serial No.	Unregulated supply voltage(V_S) (V)	Load Current (I_L) (mA)	Zener Current (I_L) (mA)	Regulated Output Voltage (V_O) (V)	% Voltage Regulation
1	2	2.50	0	0	NAN
2	4	2.50	0	2	100
3	5	2.50	0	4	100
4	10	2.50	0	5	100
5	10	2.50	2.5	5	50
6	20	2.50	12.5	5	25
7	30	2.50	22.5	5	16.7

Table 1: Line Regulator ($V_Z = 5 V$)



Graph 1: Line Regulation Graph

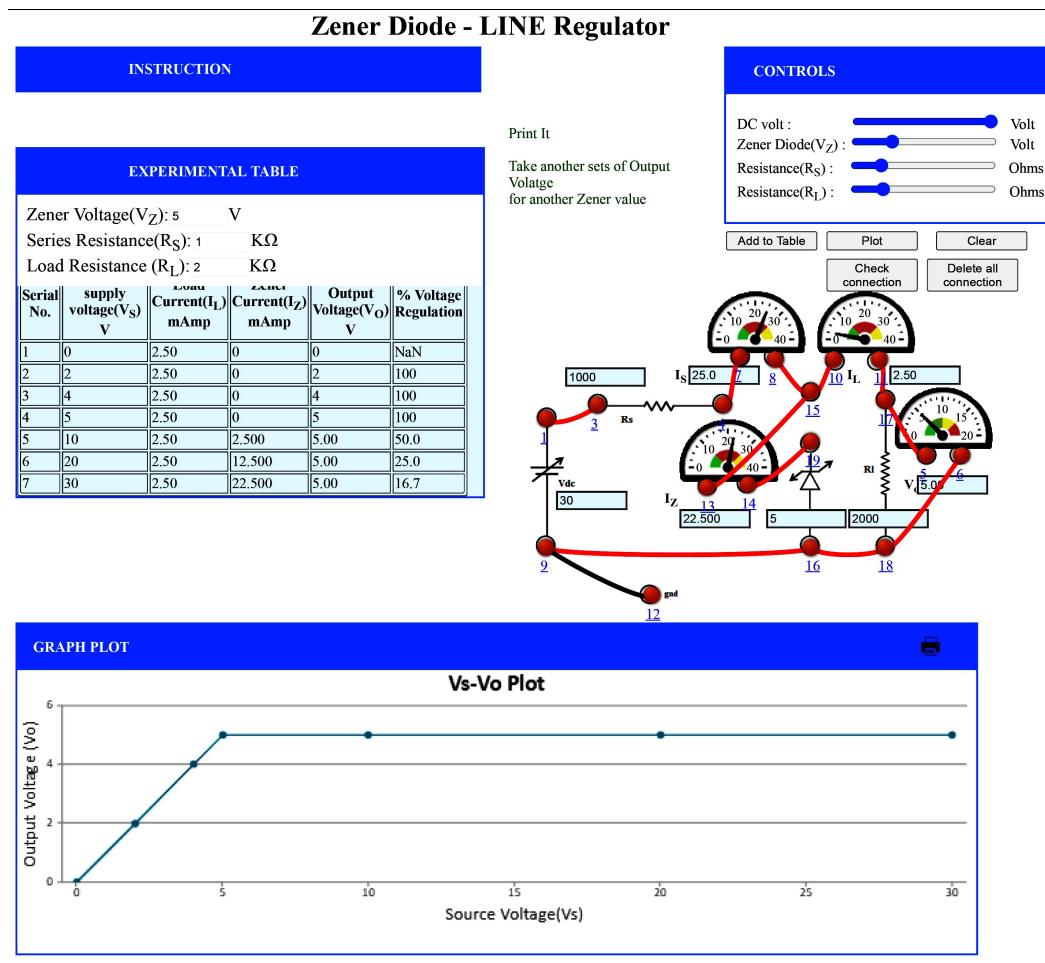
Calculation of Line Regulation:

From the Graph, $A = (2, 2)$ and $B = (30, 5)$

Thus,

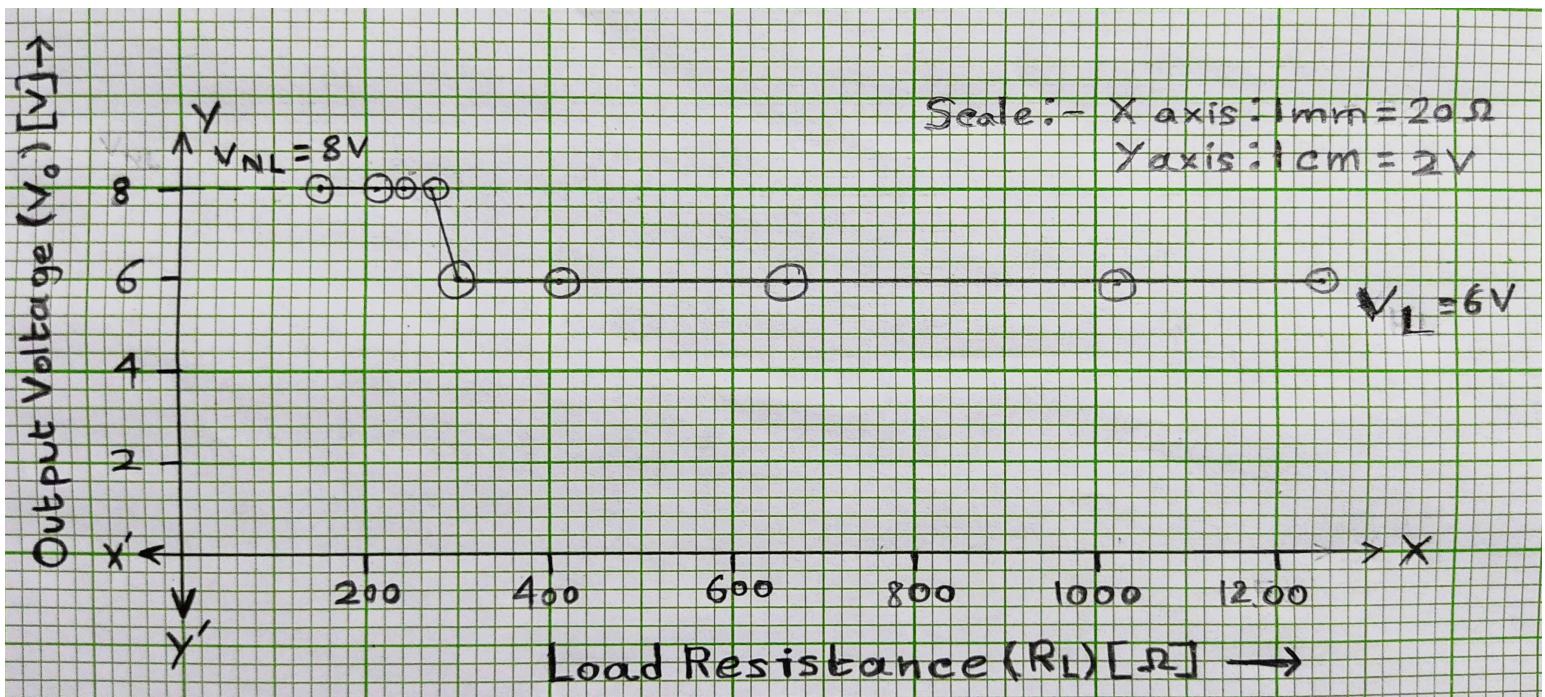
$$\begin{aligned} \text{Line Regulation } (S_i) &= \frac{\text{Change in Output Voltage } (V_{OB} - V_{OA})}{\text{Change in Supply Voltage } (V_{SB} - V_{SA})} \times 100\% \\ &= \frac{(5 - 2)}{(30 - 2)} \times 100\% \approx 10.71\% \end{aligned}$$

Load Regulation:-



Serial No.	Unregulated supply voltage(V_S) (V)	Load Current (I_L) (mA)	Zener Current (I_L) (mA)	Regulated Output Voltage (V_O) (V)	% Voltage Regulation
1	150	40.0	0	8	40.0
2	214	28.0	0	8	31.8
3	239	25.1	0	8	29.5
4	270	22.2	0	8	27.0
5	300	20.0	0	6	25.0
6	410	14.6	5.37	6	19.6
7	661	9.08	10.9	6	13.1
8	1027	5.84	14.2	6	8.87
9	1250	4.8	15.2	6	7.41

Table 2: Load Regulator ($V_{CE} = 6 \text{ V}$)



Graph 2: Load Regulation Graph

Calculation of Load Regulation:

From the Graph,

$$V_{NL} \text{ (No Load voltage)} = 8 \text{ V}$$

$$V_L \text{ (Full Load voltage)} = 6 \text{ V}$$

Thus,

$$\begin{aligned} \text{Load Regulation } (S_L) &= \frac{V_{NL} - V_L}{V_L} \times 100\% \\ &= \frac{8 - 6}{6} \approx 33.33\% \end{aligned}$$

Conclusion:-

The V-I Characteristics of Zener Diode under both line and load regulation shows that the unregulated input voltage is regulated to the Zener voltage after the input exceeds the Zener voltage value.

Electronics Practical: Study the Input and Output Characteristics Curve for Common Emitter (CE) mode.

Soham Chatterjee, ECE, 426

Aim:-

Study the Input and Output Characteristics Curve for Common Emitter (CE) mode.

Theory:-

A Common Emitter Bipolar Junction Transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions. BJTs can be made either as PNP or as NPN. They have three regions and three terminals, Emitter, Base, and Collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally.

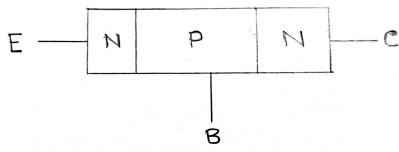
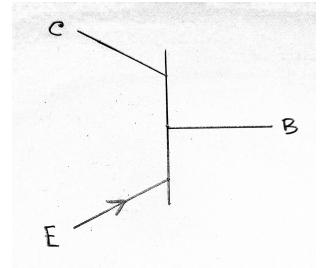
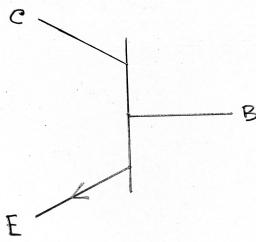


Figure 1: N-P-N

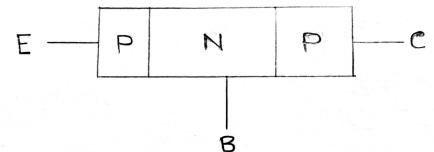


Figure 2: P-N-P

Emitter is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. Base is the middle very thin and lightly doped region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. Collector is the region with intermediate doping to the right end where charge carriers are collected. The area of this region is largest compared to emitter and base region.

Input Characteristics:-

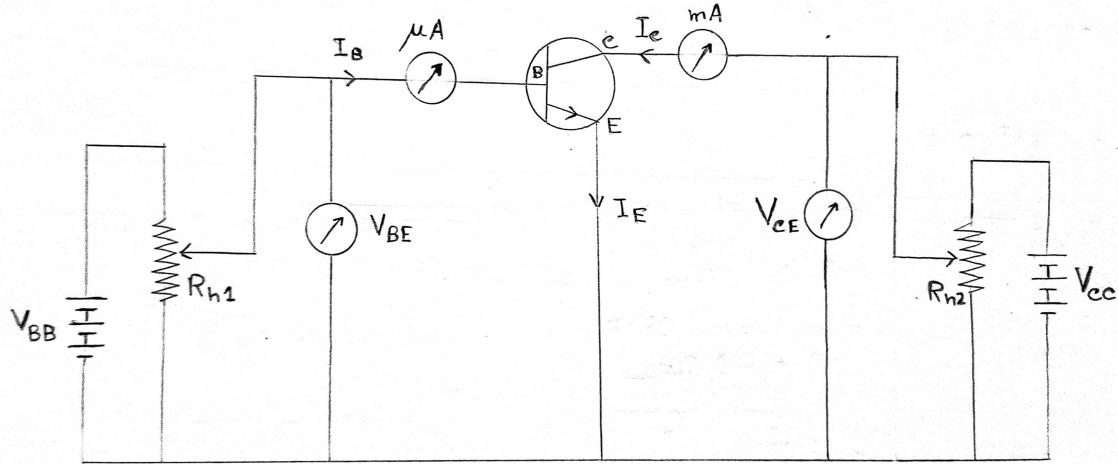
The most important characteristic of the BJT is the plot of the base current, I_B , versus the base-emitter voltage, V_{BE} , for various values of the collector-emitter voltage, V_{CE}

$$I_B = \phi(V_{BE}, V_{CE}) \text{ for constant } V_{CE}$$

Output Characteristics:-

The most important characteristic of the BJT is the plot of the collector current, I_C , versus the collector-emitter voltage, V_{CE} for various values of the base current, I_B as shown on the circuit on the right.

$$I_C = \phi(V_{CE}, I_B) \text{ for constant } I_B$$



Circuit: NPN CE BJT connected for study of input and output characteristics

Experimental Data:-

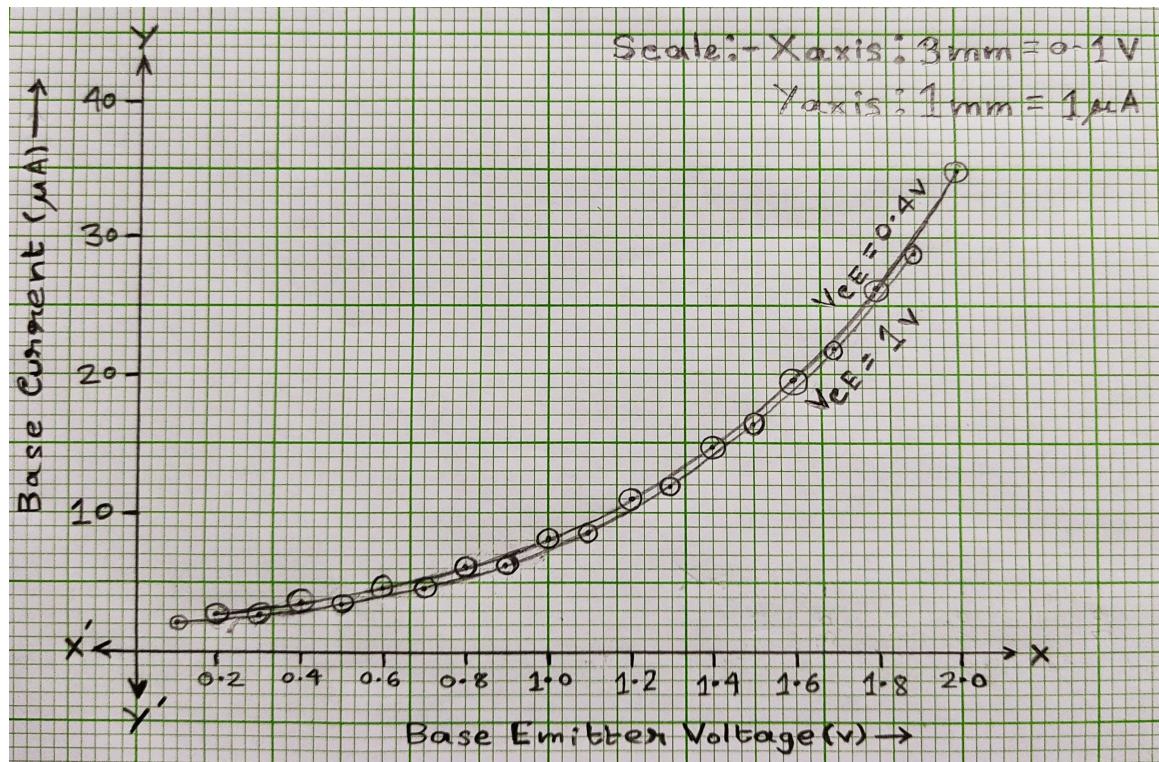
Input Characteristics:-

Sl. No.	Base Emitter Voltage (V_{BE}) (in V)	Base Current (I_B) (in μA)
1	0.2	2.661
2	0.4	3.542
3	0.6	4.713
4	0.8	6.271
5	1.0	8.345
6	1.2	11.11
7	1.4	14.68
8	1.6	19.67
9	1.8	26.17
10	2.0	34.82

Table 1: Set 1 DATA ($V_{CE} = 0.400$ V)

Sl. No.	Base Emitter Voltage (V_{BE}) (in V)	Base Current (I_B) (in μA)
1	0.1	2.307
2	0.3	3.07
3	0.5	4.085
4	0.7	5.437
5	0.9	7.235
6	1.1	9.627
7	1.3	12.81
8	1.5	17.05
9	1.7	22.69
10	1.9	30.19

Table 2: Set 2 DATA ($V_{CE} = 1.00$ V)



Graph 1: Input Characteristics Graph for CE N-P-N BJT

BJT- CE INPUT CHARACTERISTICS

INSTRUCTION

EXPERIMENTAL TABLE		
Serial No.	Collector-Emitter Voltage 0.4000 V	
	Base-Emitter Voltage V	Base Current(μ A)
1	0.2000	2.661
2	0.4000	3.542
3	0.6000	4.713
4	0.8000	6.271
5	1.000	8.345
6	1.200	11.11
7	1.400	14.78
8	1.600	19.67
9	1.800	26.17
10	2.000	34.82

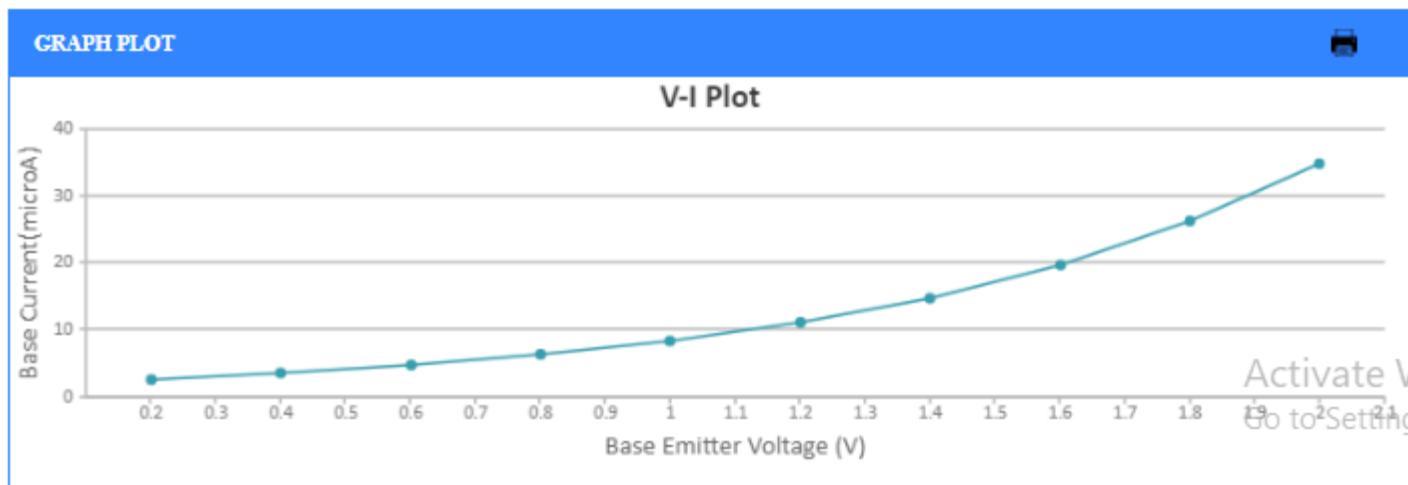
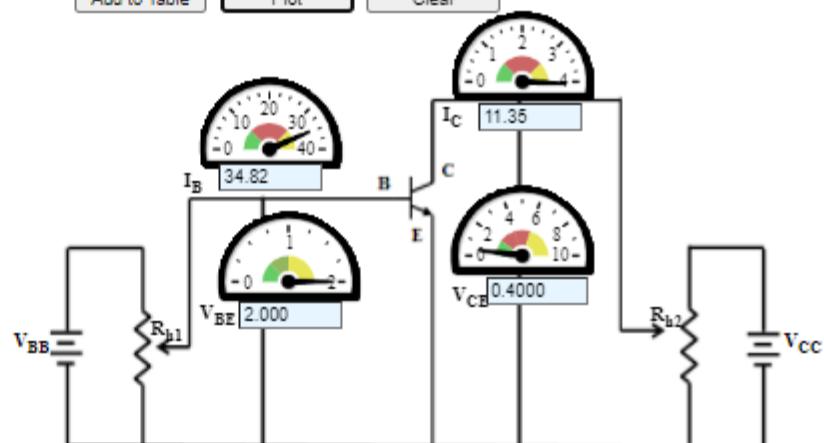
CONTROLS

R_{h1} Ohms 100
 R_{h2} Ohms 4

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Take another sets of Base-Emitter and Base Current readings for another Collector-Emitter value

[Add to Table](#) [Plot](#) [Clear](#)



Output Characteristics:-

Sl. No.	Collector Emitter Voltage (V_{CE}) (in V)	Collector Current (I_C) (in mA)
1	0.1	5.994
2	0.2	11.87
3	0.4	22.85
4	0.7	36.35
5	1.0	53.25
6	1.4	56.94
7	1.8	58.68
8	2.2	59.34
9	2.5	59.85
10	3.0	60.14
11	8.1	60.14

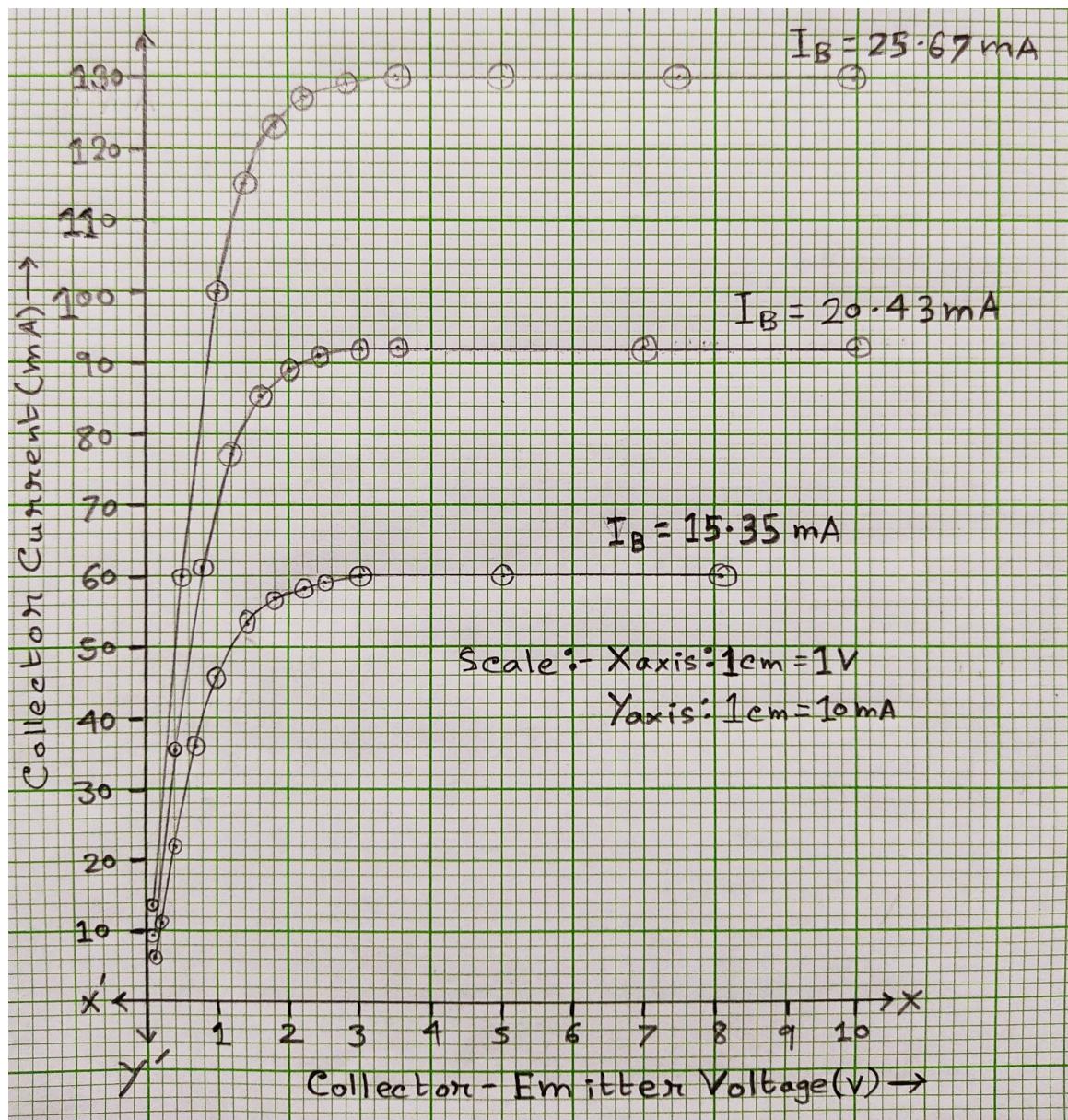
Table 1: Set 1 DATA ($I_B = 15.35 \mu A$)

Sl. No.	Collector Emitter Voltage (V_{CE}) (in V)	Collector Current (I_C) (in mA)
1	0.1	9.202
2	0.4	35.08
3	0.8	61.31
4	1.2	76.97
5	1.6	85.09
6	2.0	89.0
7	2.4	90.82
8	3.0	91.87
9	3.5	92.16
10	7.0	92.32
11	10.0	92.32

Table 2: Set 2 DATA ($I_B = 20.43 \mu A$)

Sl. No.	Collector Emitter Voltage (V_{CE}) (in V)	Collector Current (I_C) (in mA)
1	0.1	12.96
2	0.5	60.11
3	1.0	99.07
4	1.4	115.2
5	1.8	123.2
6	2.2	126.9
7	2.8	129.1
8	3.5	129.8
9	5.0	130.1
10	7.5	130.1
11	10.0	130.1

Table 3: Set 3 DATA ($I_B = 25.67 \mu A$)



Graph 2: Output Characteristics Graph for CE N-P-N BJT

BJT- CE OUTPUT CHARACTERISTICS

INSTRUCTION

EXPERIMENTAL TABLE

Serial No.	Base-Current 15.35 μ A	
	Collector-Emitter Voltage V	Collector Current mA
1	0.1000	5.994
2	0.2000	11.87
3	0.4000	22.85
4	0.7000	36.35
5	1.000	45.81
6	1.400	53.25
7	1.800	56.94
8	2.200	58.68
9	2.500	59.34
10	3.000	59.85
11	5.000	60.14
12	8.100	60.14

CONTROLS

R_{h1} Ohms 15 R_{h2} Ohms 81

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Take another sets of Collector-Emitter and Collector Current readings for another Base Current

GRAPH PLOT

V-I Plot

Collector-Emitter Voltage (V)	Collector Current (mA)
0.1	5
0.5	20
1.0	45
1.5	52
2.0	55
2.5	58
3.0	59
4.5	59
5.0	59
7.5	59
8.0	59

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Conclusion:-

The Input and Output Characteristics Curve for Common Base (CB) mode BJT were studied and the graphs were plotted

Electronics Practical: Study the Input and Output Characteristics
Curve for Common Base (CB) mode.

Soham Chatterjee, ECE, 426

Aim:-

Study the Input and Output Characteristics Curve for Common Base (CB) mode.

Theory:-

A Common Base Bipolar Junction Transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions. BJTs can be made either as PNP or as NPN. They have three regions and three terminals, Emitter, Base, and Collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally.

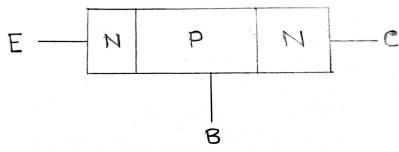
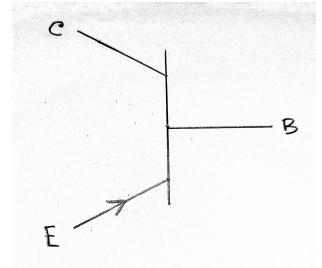
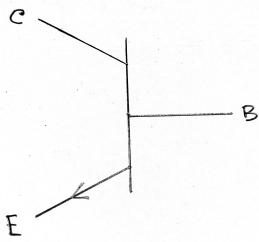


Figure 1: N-P-N

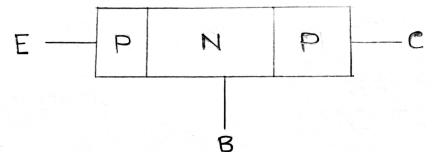


Figure 2: P-N-P

Emitter is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. Base is the middle very thin and lightly doped region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. Collector is the region with intermediate doping to the right end where charge carriers are collected. The area of this region is largest compared to emitter and base region.

Input Characteristics:-

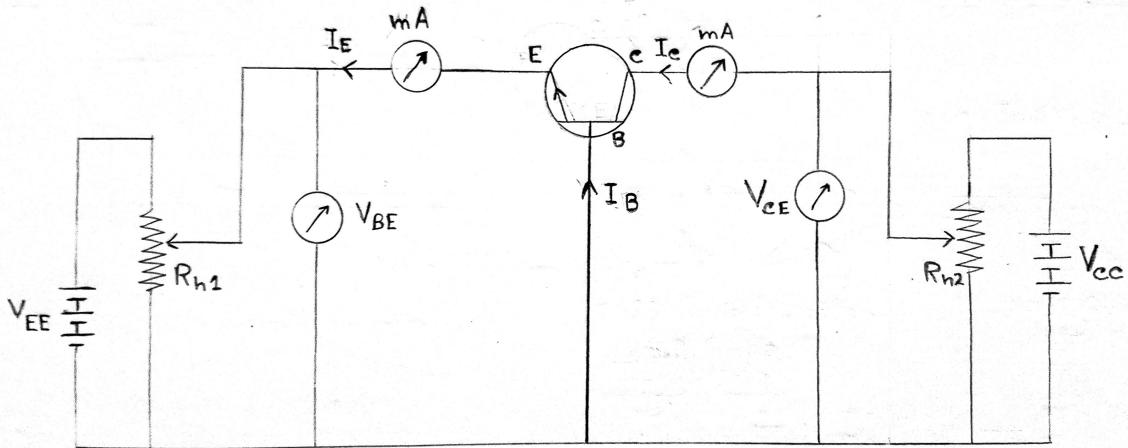
The most important characteristic of the BJT is the plot of the base current, I_E , versus the base-emitter voltage, V_{BE} , for various values of the base-collector voltage, V_{CE}

$$I_E = \phi(V_{BE}, V_{CB}) \text{ for constant } V_{CB}$$

Output Characteristics:-

The most important characteristic of the BJT is the plot of the collector current, I_C , versus the base-collector voltage, V_{CB} for various values of the emitter current, I_E as shown on the circuit on the right.

$$I_C = \phi(V_{CB}, I_E) \text{ for constant } I_E$$



Circuit: NPN CB BJT connected for study of input and output characteristics

Experimental Data:-

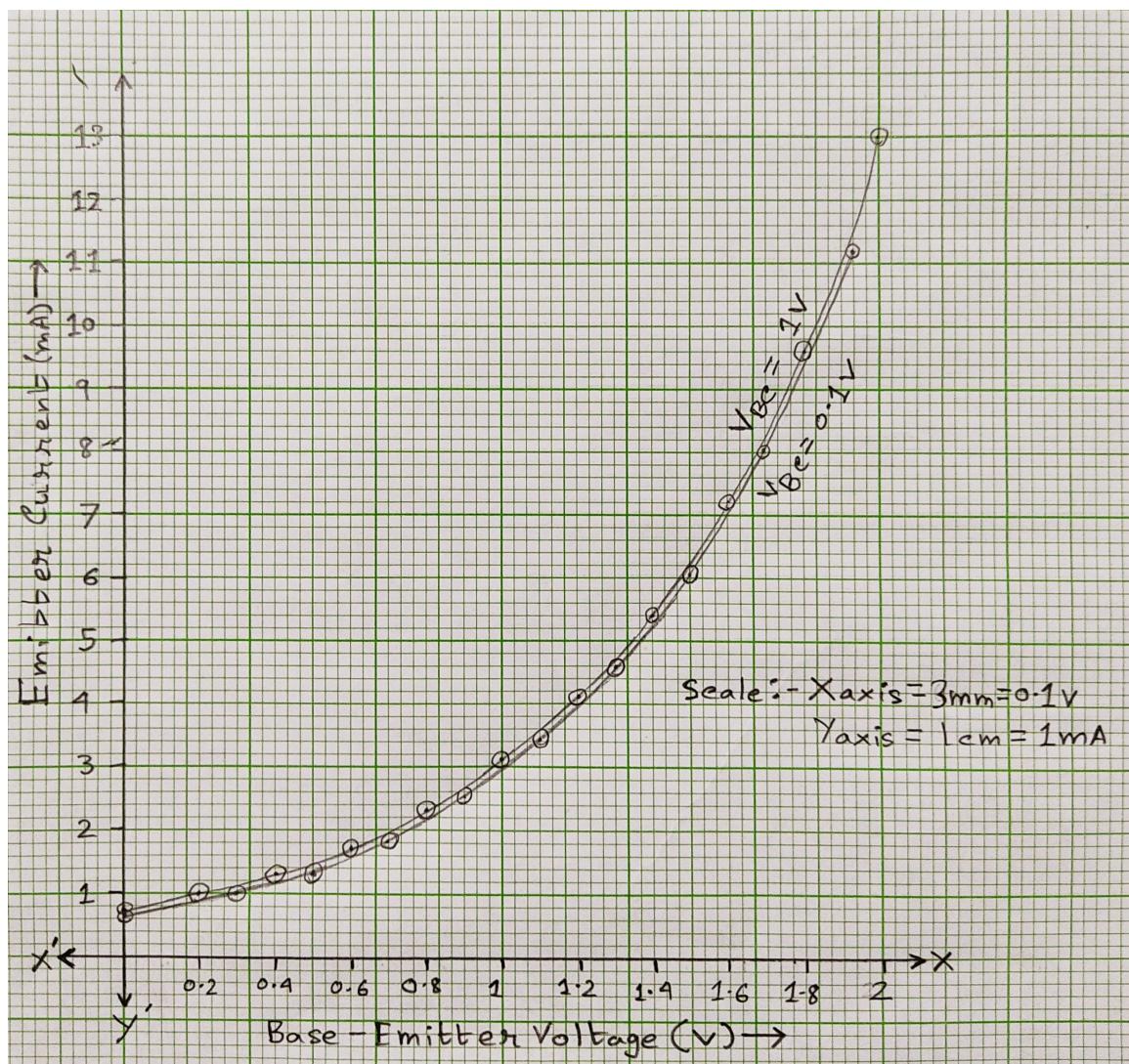
Input Characteristics:-

Sl. No.	Base Emitter Voltage (V_{BE}) (in V)	Emitter Current (I_E) (in mA)
1	0.02	0.76
2	0.2	0.95
3	0.4	1.3
4	0.6	1.7
5	0.8	2.3
6	1.0	3.1
7	1.2	4.1
8	1.4	5.4
9	1.6	7.2
10	1.8	9.6
11	2.0	13

Table 1: Set 1 DATA ($V_{CB} = 1.00$ V)

Sl. No.	Collector Emitter Voltage (V_{CE}) (in V)	Base Current (I_E) (in mA)
1	0.02	0.76
2	0.1	0.85
3	0.3	1.1
4	0.5	1.5
5	0.7	2.0
6	0.9	2.7
7	1.1	3.5
8	1.3	4.7
9	1.5	6.3
10	1.7	8.3
11	1.9	11

Table 2: Set 2 DATA ($V_{CB} = 0.10$ V)



Graph 1: Input Characteristics Graph for CB N-P-N BJT

BJT- CB INPUT CHARACTERISTICS

INSTRUCTION

EXPERIMENTAL TABLE

Serial No.	Base-Collector Voltage 1.000 V	
	Base-Emitter Voltage V	Emitter Current mA
1	0.02000	0.76
2	0.2000	0.98
3	0.4000	1.3
4	0.6000	1.7
5	0.8000	2.3
6	1.000	3.1
7	1.200	4.1
8	1.400	5.4
9	1.600	7.2
10	1.800	9.6
11	2.000	13

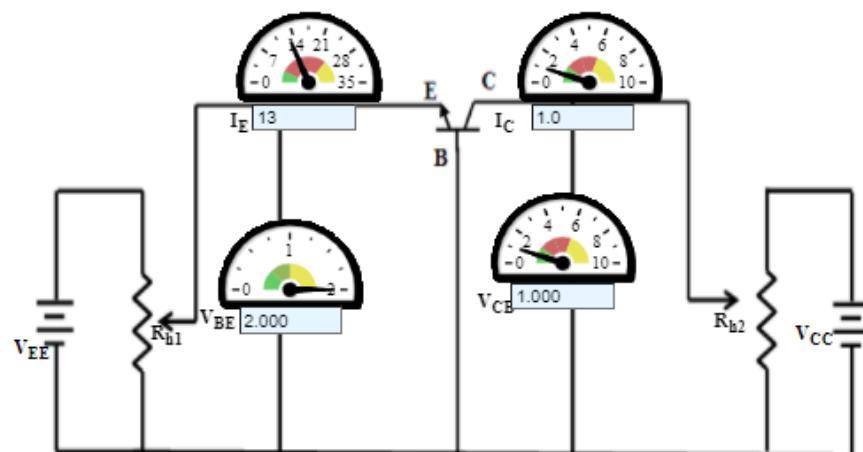
CONTROLS

Print It

R_{h1} Ohms 100
 R_{h2} Ohms 10

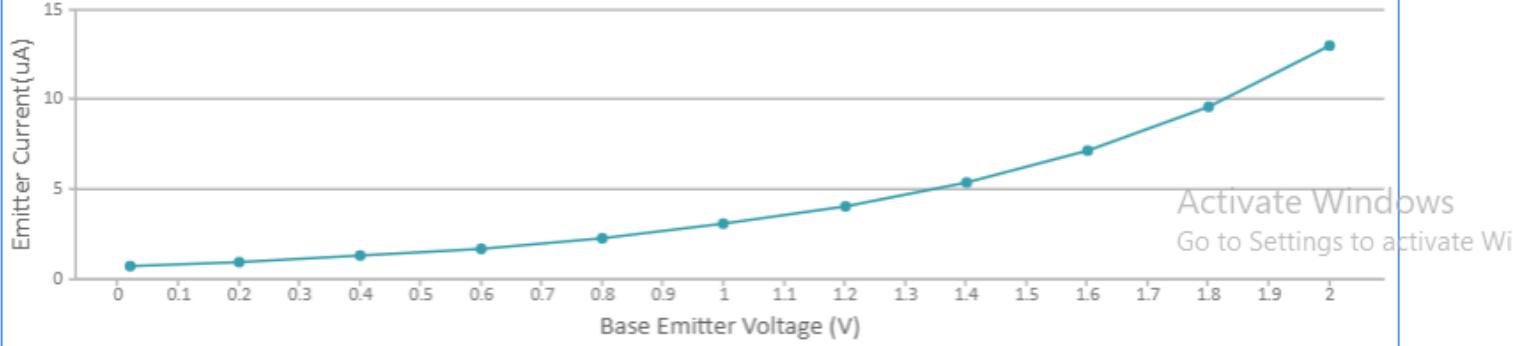
Take another sets of Base-Emitter Voltage and Emitter current readings for another Base-Collector value

Add to Table Plot Clear



GRAPH PLOT

V-I Plot



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Output Characteristics:-

Sl. No.	Base Collector Voltage (V_{CB}) (in V)	Collector Current (I_C) (in mA)
1	-0.14	-0.1442
2	0.16	0.1645
3	0.56	0.5266
4	0.96	0.7715
5	1.36	0.9085
6	1.76	0.977
7	2.16	1.009
8	2.76	1.028
9	4.76	1.036
10	6.76	1.037
11	9.76	1.037

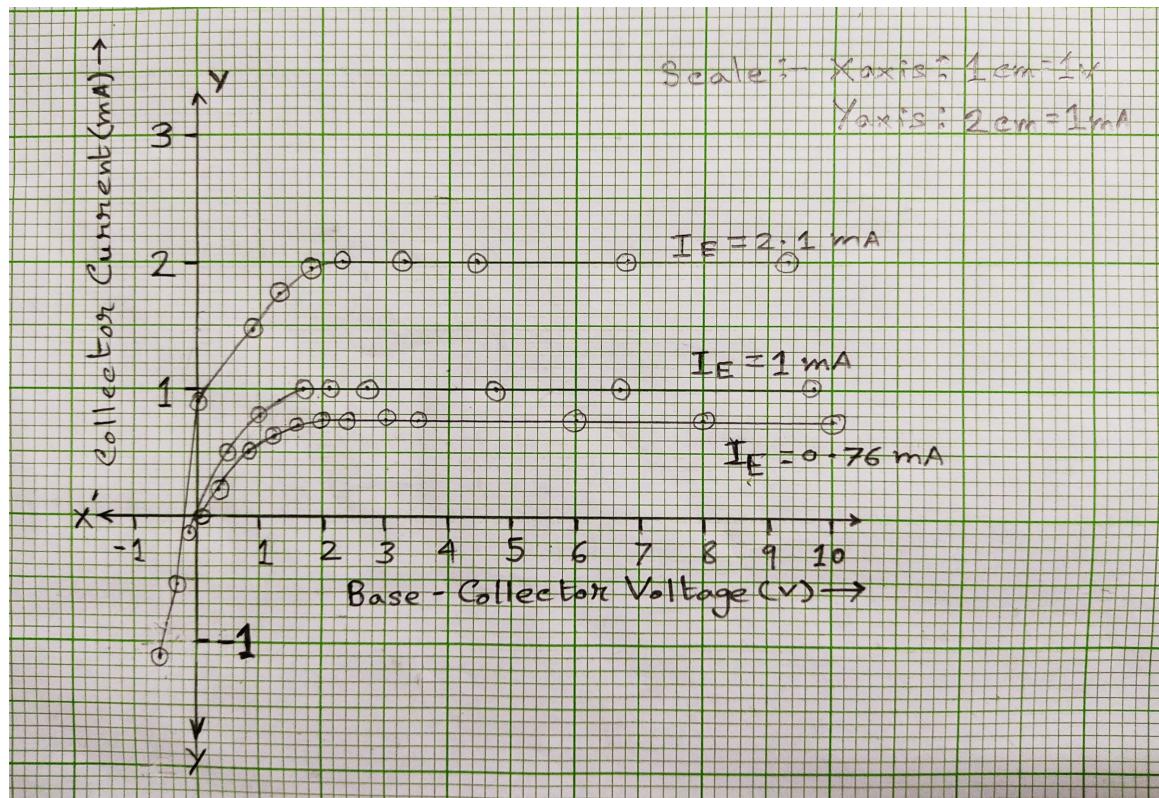
Table 1: Set 1 DATA ($I_E = 1 \text{ mA}$)

Sl. No.	Base Collector Voltage (V_{CB}) (in V)	Collector Current (I_C) (in mA)
1	-0.62	-1.134
2	-0.32	-0.637
3	0.08	0.1643
4	0.48	0.9184
5	0.88	1.454
6	1.28	1.763
7	1.78	1.944
8	2.28	2.015
9	3.28	2.052
10	4.38	2.057
11	6.78	2.058
12	9.78	2.058

Table 2: Set 2 DATA ($I_E = 2.1 \text{ mA}$)

Sl. No.	Base Collector Voltage (V_{CB}) (in V)	Collector Current (I_C) (in mA)
1	0.08	0.06043
2	0.38	0.2746
3	0.78	0.4941
4	1.18	0.6264
5	1.58	0.6954
6	1.98	0.7287
7	2.38	0.7441
8	2.98	0.7531
9	3.48	0.7556
10	5.98	0.757
11	7.98	0.757
12	9.98	0.757

Table 3: Set 3 DATA ($I_E = 0.76 \text{ mA}$)



Graph 2: Output Characteristics Graph for CB N-P-N BJT

BJT- CB -OUTPUT CHARACTERISTICS

INSTRUCTION

EXPERIMENTAL TABLE

Serial No.	Emitter Current	
	Base-Collector Voltage V	Collector Current mA
1	-0.1400	-0.1442
2	0.1600	0.1645
3	0.5600	0.5266
4	0.9600	0.7715
5	1.360	0.9085
6	1.760	0.9770
7	2.160	1.009
8	2.760	1.028
9	4.760	1.036
10	6.760	1.037
11	9.760	1.037

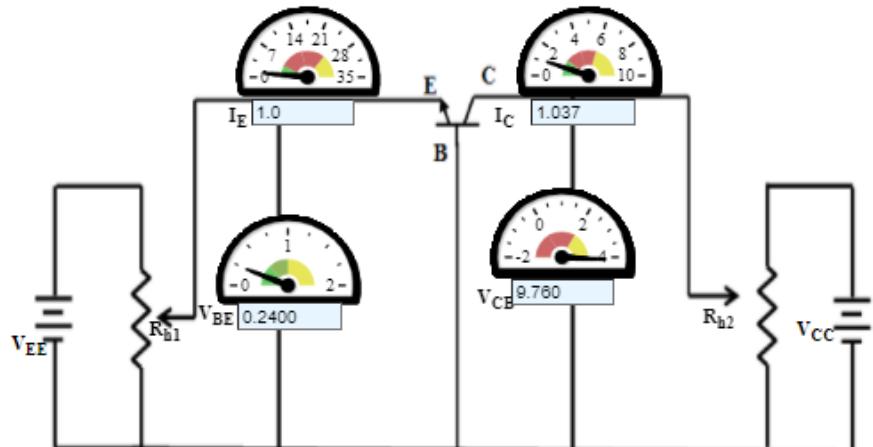
CONTROLS

R_{h1} Ohms
 R_{h2} Ohms

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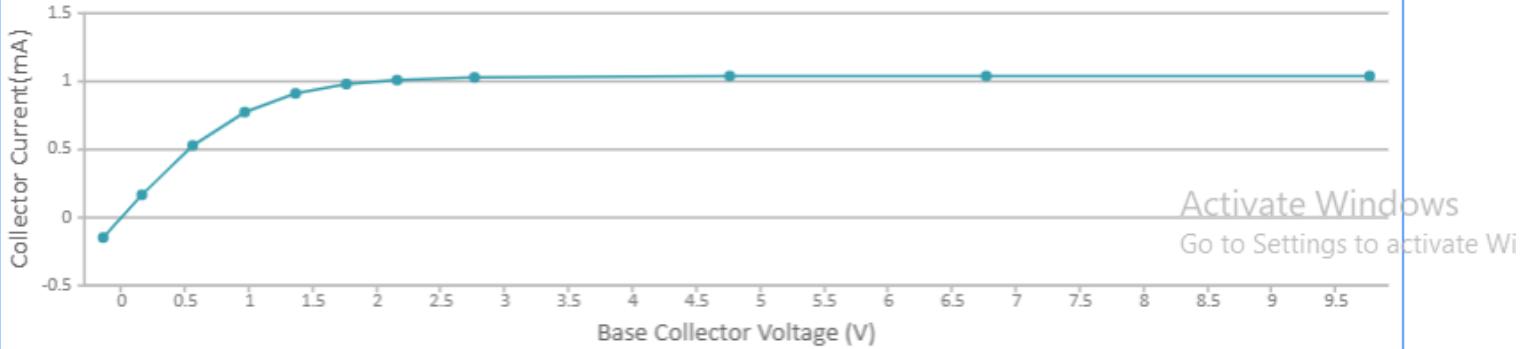
Take another sets of Base-Collector and Collector Current readings for another Emitter Current

[Add to Table](#) [Plot](#) [Clear](#)



GRAPH PLOT

V-I Plot



Conclusion:-

The Input and Output Characteristics Curve for Common Emitter (CE) mode were studied and the graphs were plotted.

Electronics Practical: Study of Op-Amp circuits: Inverting and Non-Inverting amplifiers.

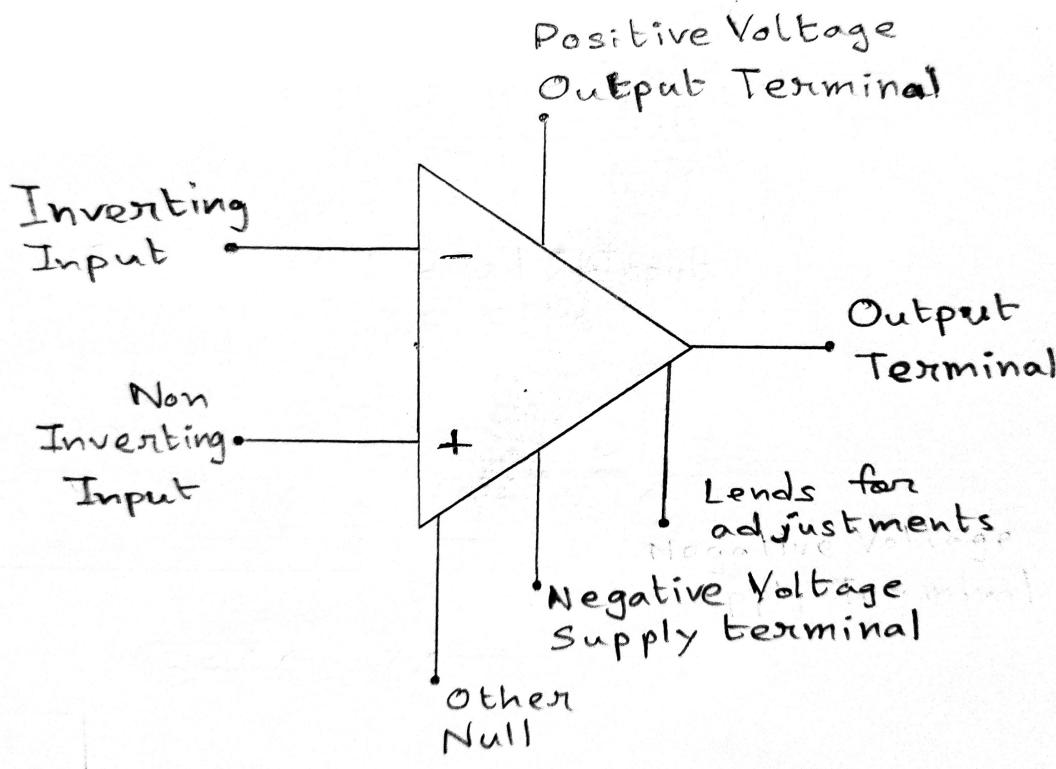
Soham Chatterjee, ECE, 426

Aim:-

Study of Op-Amp circuits: Inverting and Non-Inverting amplifiers.

Theory:-

Operational Amplifier commonly known as Op-Amp is a linear electronic device having three terminals, two high impedance input and one output terminal. Op-Amp can perform multiple function when attached to different feedback combinations like resistive, capacitive or both. Generally it is used as voltage amplifier and the output voltage of the Op-Amp is the difference between the voltages at its two input terminals. Op-Amp shows some properties that make it an ideal amplifier, its open loop gain and input impedance is infinite (i.e. practically very high), Output impedance and offset voltage is zero(i.e., practically very low) and bandwidth is infinite(i.e. practically limited to frequency where its gain become unity)



Invering Op-Amp:-

The open loop gain(A_O) of the Op-Amp is very high which makes it very unstable, so to make it stable with a controllable gain, a feedback is applied through some external resistor(R_F) from its output to inverting input terminal(i.e., also known as negative feedback) resulting in reduced gain(closed loop gain, A_V). So the voltage at inverting terminal is now the sum of the actual input and feedback voltages, and to separate both a input resistor (R_I) is introduced in the circuit. The non-Inverting terminal of the Op-Amp is grounded, and the inverting terminal behaves like a virtual ground as the junction of the input and feedback signal are at the same potential.

$$\text{The close loop } (A_{CL}) \text{ is given by: } A_d = \frac{V_{Out}}{V_{In}} = -\frac{R_F}{R_I}$$

$$\text{Output Voltage } (V_{Out}) \text{ is given by: } V_{Out} = -\frac{R_F}{R_I} \times V_{In}$$

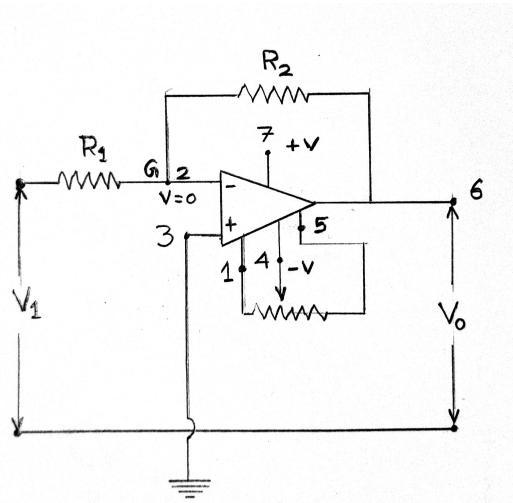


Figure 1: Inverting Amplifier

Non-Inverting Op-Amp:-

In this configuration of Op-amp the input signal is directly fed to the non-inverting terminal resulting in a positive gain and output voltage in phase with input as compared to inverting Op-amp where the gain is negative and output voltage is out of phase with input, and to stabilize the circuit a negative feedback is applied through a resistor (R_F) and the inverting terminal is grounded with an input resistor (R_2). This inverting Op-Amp like layout the at inverting terminal creates a virtual ground at the summing point make the R_F and R_2 a potential divider across inverting terminal, Hence determines the gain of the circuit.

$$\text{The close loop } (A_{CL}) \text{ is given by: } A_d = \frac{V_{Out}}{V_{In}} = -\frac{R_2 + R_F}{R_2} = 1 + \frac{R_F}{R_2}$$

$$\text{Output Voltage } (V_{Out}) \text{ is given by: } V_{Out} = \left[1 + \frac{R_F}{R_2} \right] V_{In}$$

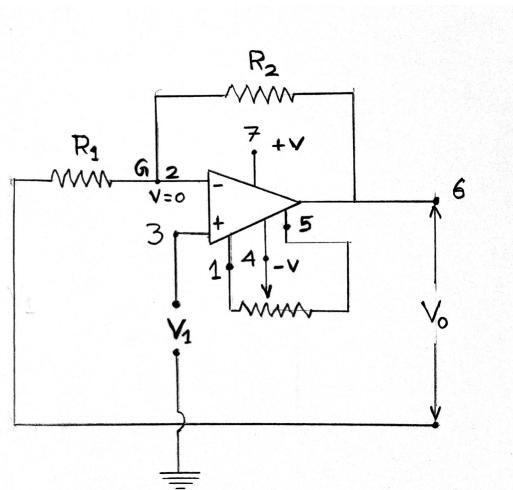


Figure 2: Inverting Amplifier

Experimental Data:-

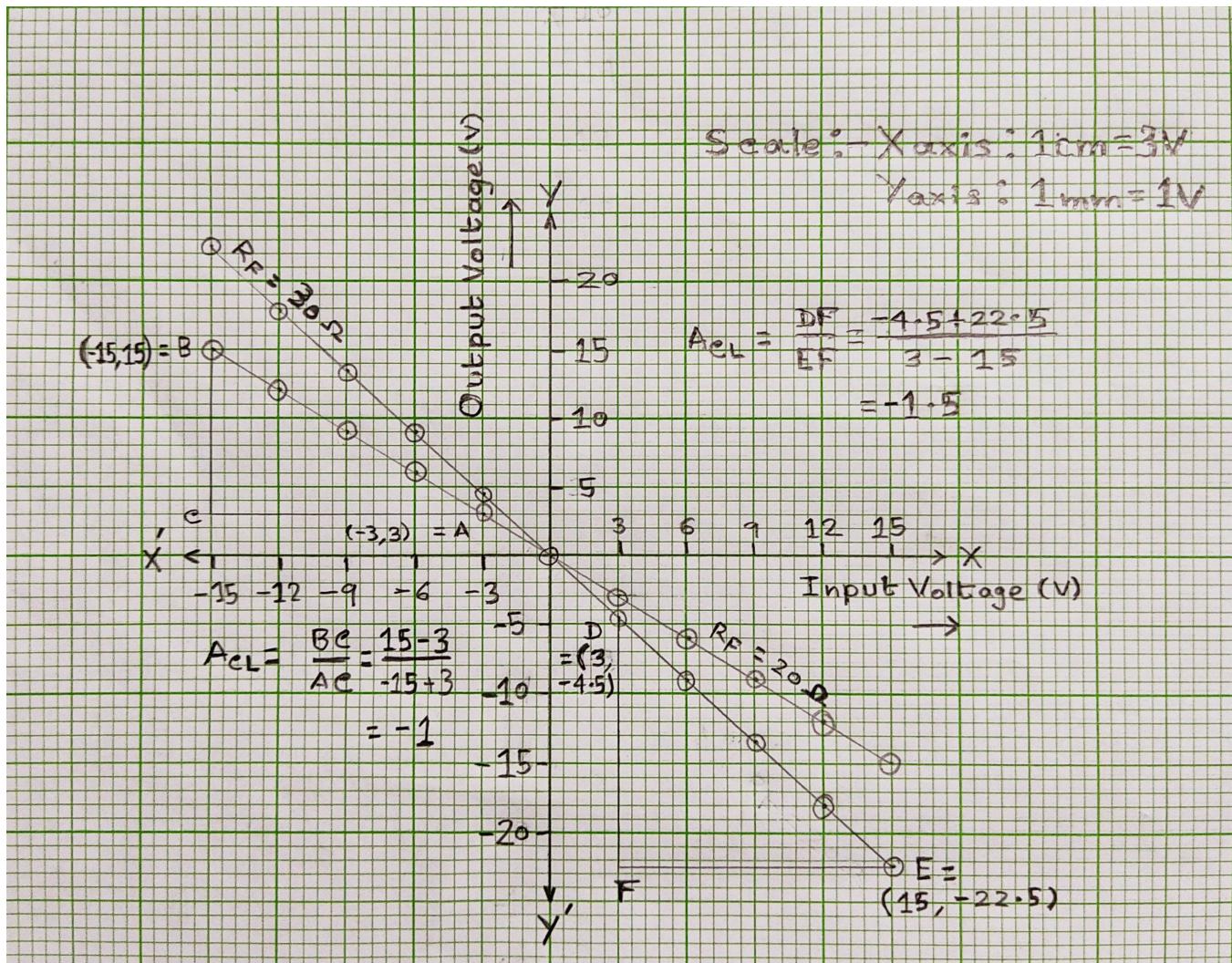
Invering Op-Amp:-

Sl. No.	Input Voltage(V)	Output Voltage (V)	Current (m A)
1	-15	15.0	-0.0149
2	-12	12.0	-0.0119
3	-9	9.00	-0.00891
4	-6	6.00	-0.00594
5	-3	3.00	-0.00297
6	0	0.00	0.00
7	3	-3.00	0.00297
8	6	-6.00	0.00594
9	9	-9.00	0.00891
10	12	-12.0	0.0119
11	15	-15.0	0.0149

Table 1: SET-1 Observation Table for the Inverting Op-Amp ($R_F = 20 \text{ K}\Omega$)

Sl. No.	Input Voltage(V)	Output Voltage (V)	Current (m A)
1	-15	22.5	-0.0185
2	-12	18.0	-0.0148
3	-6	9.00	-0.00739
4	-3	4.50	-0.00369
5	0	0.00	0.00
6	3	-4.50	0.00369
7	6	-9.00	0.00739
8	9	-13.5	0.0111
9	12	-18.0	0.0148
10	15	-22.5	0.0185

Table 2: SET-2 Observation Table for the Inverting Op-Amp ($R_F = 30 \text{ K}\Omega$)



Graph 1: Inverting Op-Amp Plot ($R_F = 20 \text{ K}\Omega, 40 \text{ K}\Omega$)

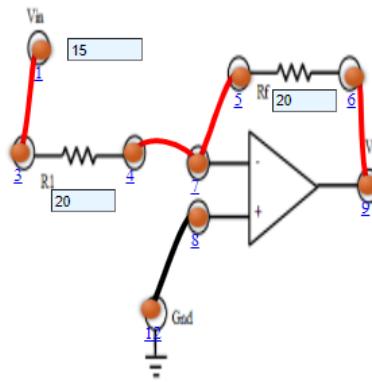
INSTRUCTION

EXPERIMENTAL TABLE

Resistance: 20 KΩ

Serial No.	Input Voltage V	Output Voltage V	Current mA
1	-15	15.0	-0.0149
2	-12	12.0	-0.0119
3	-9	9.00	-0.00891
4	-6	6.00	-0.00594
5	-3	3.00	-0.00297

Inverting Opamp



CONTROLS

Input volt : Volt
 Resistance (R₁) : Kohms
 Resistance (R_f) : Kohms

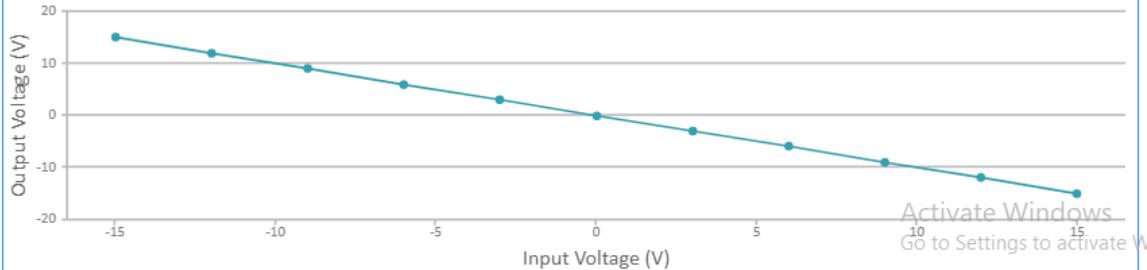
Add to Table Plot Clear
 Check connection Delete all connection
 -15.0
 0.0149
 -1

Print It

Take another sets of readings for different R₁ and R_f

GRAPH PLOT

Vo-Vi Plot



Calculation:-

Set 1:-

$$\begin{aligned}
 \text{Theoretical Close loop Gain } (A_{CL}) &= -\frac{R_F}{R_I} \\
 &= -\frac{20}{20} = -1
 \end{aligned}$$

$$\begin{aligned}
 \text{Practical Close loop Gain } (A_{CL}) &= \frac{BC}{AC} \\
 &= -\frac{15 - 3}{-15 + 3} = -1
 \end{aligned}$$

Set 2:-

$$\begin{aligned}
 \text{Theoretical Close loop Gain } (A_{CL}) &= -\frac{R_F}{R_I} \\
 &= -\frac{30}{20} = -1.5
 \end{aligned}$$

$$\begin{aligned}
 \text{Practical Close loop Gain } (A_{CL}) &= \frac{DF}{EF} \\
 &= -\frac{-4.5 + 22.5}{3 - 15} = -1.5
 \end{aligned}$$

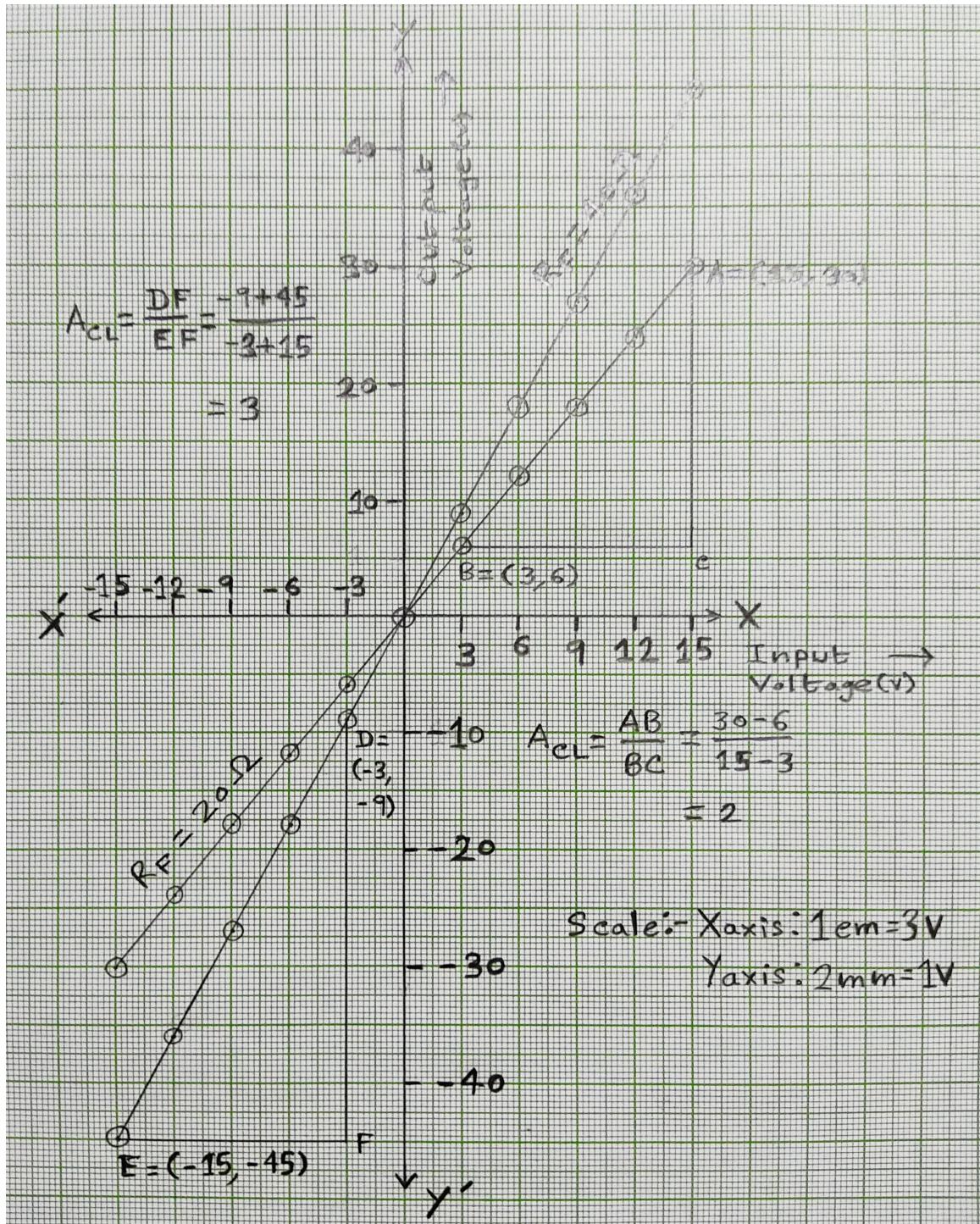
Non-Inverting Op-Amp:-

Sl. No.	Input Voltage(V)	Output Voltage (V)	Current ($m A$)
1	-15	-30.0	-0.0223
2	-12	-24.0	-0.0178
3	-9	-18.0	-0.0134
4	-6	-12.0	-0.00891
5	-3	-6.00	-0.00446
6	0	0.00	0.00
7	3	6.00	0.00446
8	6	12.0	0.00891
9	9	18.0	0.0134
10	12	24.0	0.0178
11	15	30.0	0.0223

Table 1: SET-1 Observation Table for the Inverting Op-Amp ($R_F = 20 \text{ K}\Omega$)

Sl. No.	Input Voltage(V)	Output Voltage (V)	Current ($m A$)
1	-15	-45.0	-0.0294
2	-12	-36.0	-0.0235
3	-9	-27.0	-0.0176
4	-6	-18.0	-0.0118
5	-3	-9.00	-0.00588
6	0	0.00	0.00
7	3	9.00	0.00588
8	6	18.0	0.0118
9	9	27.0	0.0176
10	12	36.0	0.0235
11	15	45.0	0.0294

Table 2: SET-2 Observation Table for the Inverting Op-Amp ($R_F = 40 \text{ K}\Omega$)

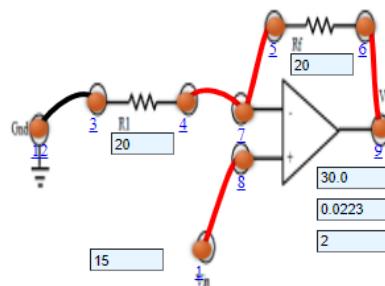


Graph 2: Non-Inverting Op-Amp Plot ($R_F = 20 \text{ K}\Omega, 40 \text{ K}\Omega$)

INSTRUCTION

Non Inverting Opamp

EXPERIMENTAL TABLE			
	Resistance: 20 KΩ		
Serial No.	Input Voltage V	Output Voltage V	Current mA
1	-15	-30.0	-0.0223
2	-12	-24.0	-0.0178
3	-9	-18.0	-0.0134
4	-6	-12.0	-0.00891
5	-3	-6.00	-0.00446



CONTROLS

Input volt : Volt
 Resistance (R_1) : Kohms
 Resistance (R_f) : Kohms

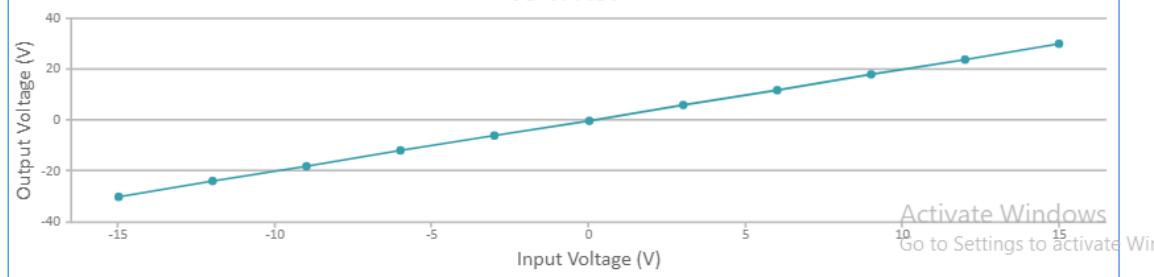
Add to Table Plot Clear
 Check connection Delete all connection

Print It

Take another sets of readings for different R1 and Rf

GRAPH PLOT

Vo-Vi Plot



Activate Windows

Go to Settings to activate Wi

Calculation:-

Set 1:-

$$\begin{aligned}\text{Theoretical Close loop Gain } (A_{CL}) &= 1 + \frac{R_F}{R_2} \\ &= 1 + \frac{20}{20} = 2\end{aligned}$$

$$\begin{aligned}\text{Practical Close loop Gain } (A_{CL}) &= \frac{AB}{BC} \\ &= -\frac{30 - 6}{15 - 3} = 2\end{aligned}$$

Set 2:-

$$\begin{aligned}\text{Theoretical Close loop Gain } (A_{CL}) &= 1 + \frac{R_F}{R_2} \\ &= 1 + \frac{40}{20} = 3\end{aligned}$$

$$\begin{aligned}\text{Practical Close loop Gain } (A_{CL}) &= \frac{DF}{EF} \\ &= -\frac{-9 + 45}{-3 + 15} = 3\end{aligned}$$

Conclusion:-

Thus the practical and theoretical gain values match and are equal for both the Inverting and Non-Inverting OP-Amp. The screenshots are attached below.

Electronics Practical: Study of Op-Amp circuits: Integrator and Differentiator using Op-Amp.

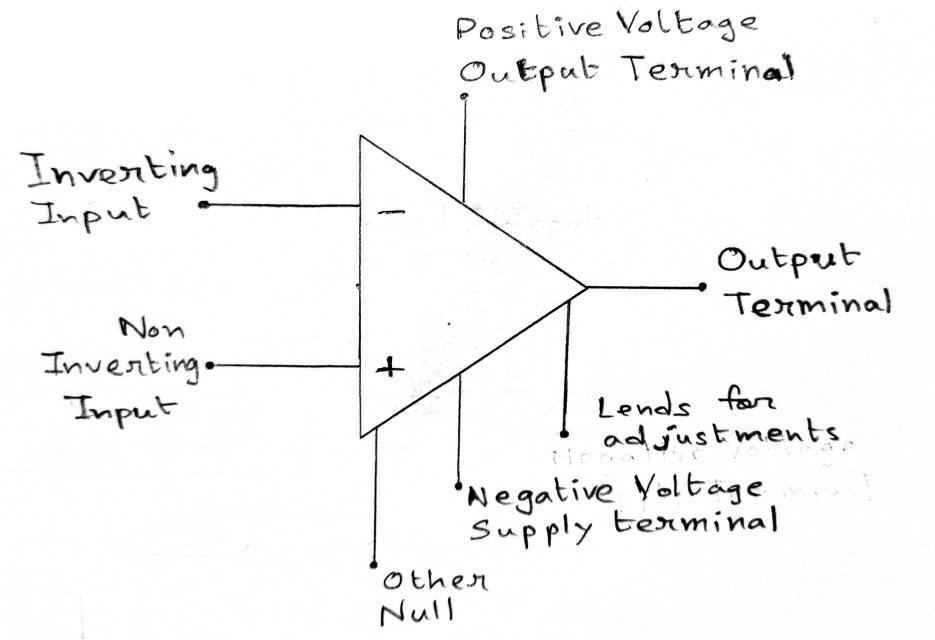
Soham Chatterjee, ECE, 426

Aim:-

Study of Op-Amp circuits: Integrator and Differentiator using Op-Amp.

Theory:-

Operational Amplifier commonly known as Op-Amp is a linear electronic device having three terminals, two high impedance input and one output terminal. Op-Amp can perform multiple function when attached to different feedback combinations like resistive, capacitive or both. Generally it is used as voltage amplifier and the output voltage of the Op-Amp is the difference between the voltages at its two input terminals. Op-Amp shows some properties that make it an ideal amplifier, its open loop gain and input impedance is infinite (i.e. practically very high), Output impedance and offset voltage is zero(i.e., practically very low) and bandwidth is infinite(i.e. practically limited to frequency where its gain become unity)



The Integrator:-

It is a circuit designed with Op-Amp in such a way that it performs the mathematical Integration operation, its output is proportional to the amplitude and time duration of the input applied. The integrator circuit layout is same as a inverting amplifier but the feedback resistor is replaced by a capacitor which make the circuit frequency dependent. In this case the circuit is derived by the time duration of input applied which results in the charging and discharging of the capacitor. Initially when the voltage is applied to integrator the uncharged capacitor allows maximum current to pass through it and no current flows through the Op-Amp due to the presence of virtual ground, the capacitor starts to charge at the rate of RC time constant and its impedance starts to increase with time and a potential difference is develops across the capacitor resulting in charging current to decrease. This results in the ratio of capacitor's impedance and input resistance increasing causing a linearly increasing ramp output voltage that continues to increase until the capacitor becomes fully charged.

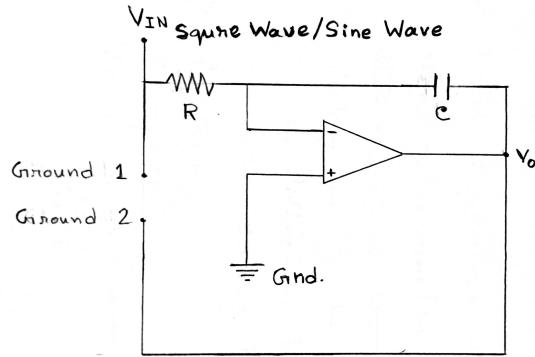


Figure 1: Integrator Circuit using Op-Amp

The Differentiator:-

In the differentiator circuit the input is connected to the inverting output of the Op-Amp through a capacitor (C) and a negative feedback is provided to the inverting input terminal through a resistor (R_F), which is same as an integrator circuit with feedback capacitor and input resistor being replaced with each other. Here the circuit performs a mathematical differentiation operation, and the output is the first derivative of the input signal, 180° out of phase and amplified with a factor $R_F \times C$. The capacitor on the input allows only the AC component and restrict the DC, at low frequency the reactance of capacitor is very high causing a low gain and high frequency vice versa but at high frequency the circuit becomes unstable.

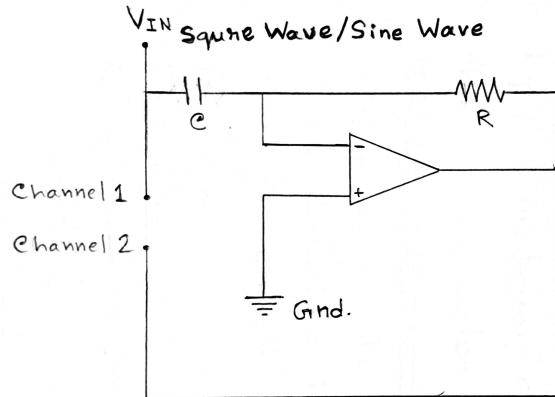


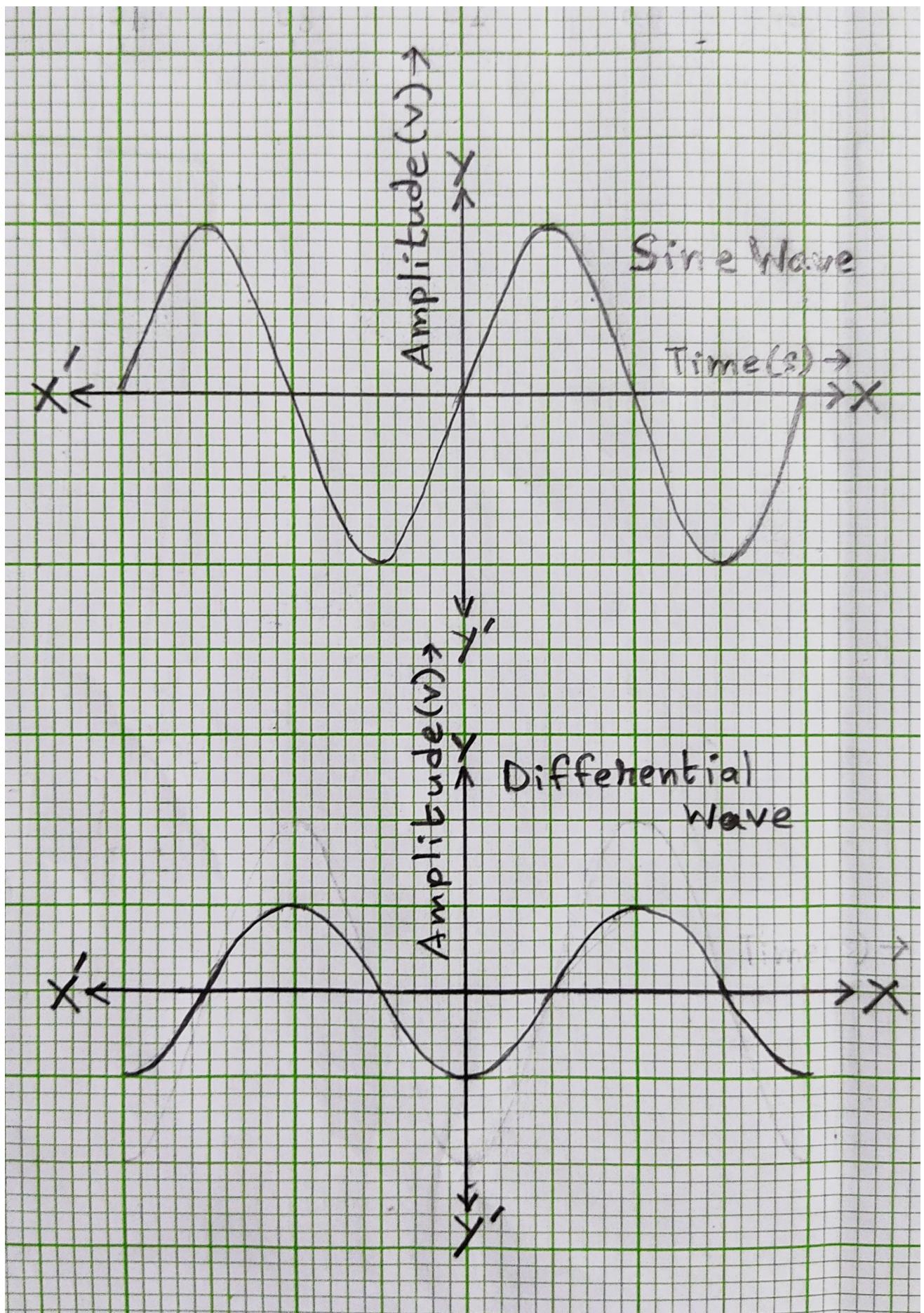
Figure 2: Differentiator Circuit using Op-Amp

Experimental Data:-

To analyse the output signals, the following graphs were plotted and for the following experiment the values of capacitor and resistor etc. used are:

Integrator using Op-Amp-

- Capacitor: $0.1 \mu F$
- Resistance: $3 K\Omega$
- Frequency: $2 KHz$
- Amplitude: $1 V$

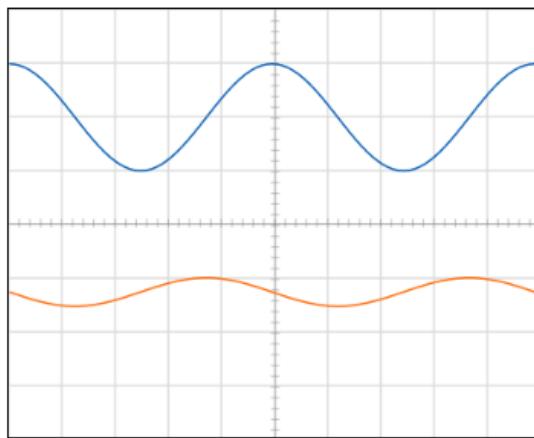


Graph 1: Integrator using Op-Amp Sine Wave Plot

Integrator using Opamp

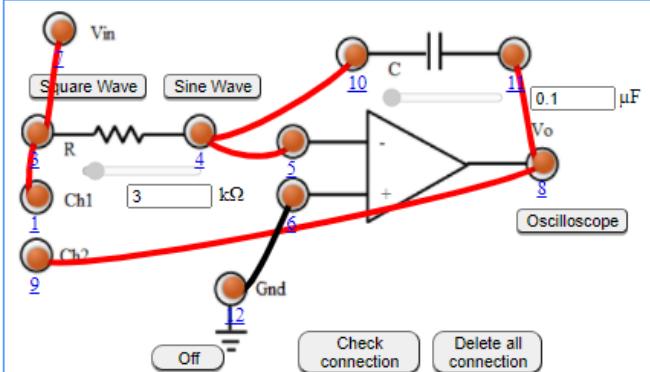
INSTRUCTION

OSCILLOSCOPE

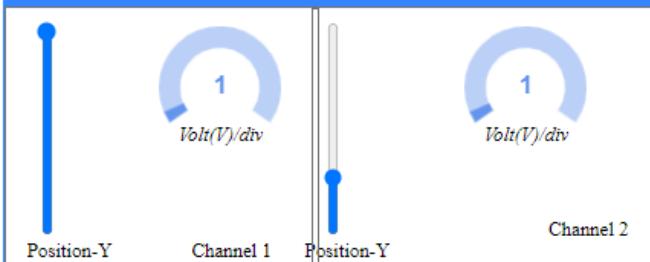


Virtual Oscilloscope Tutorial : [Virtual Oscilloscope Tutorial](#)

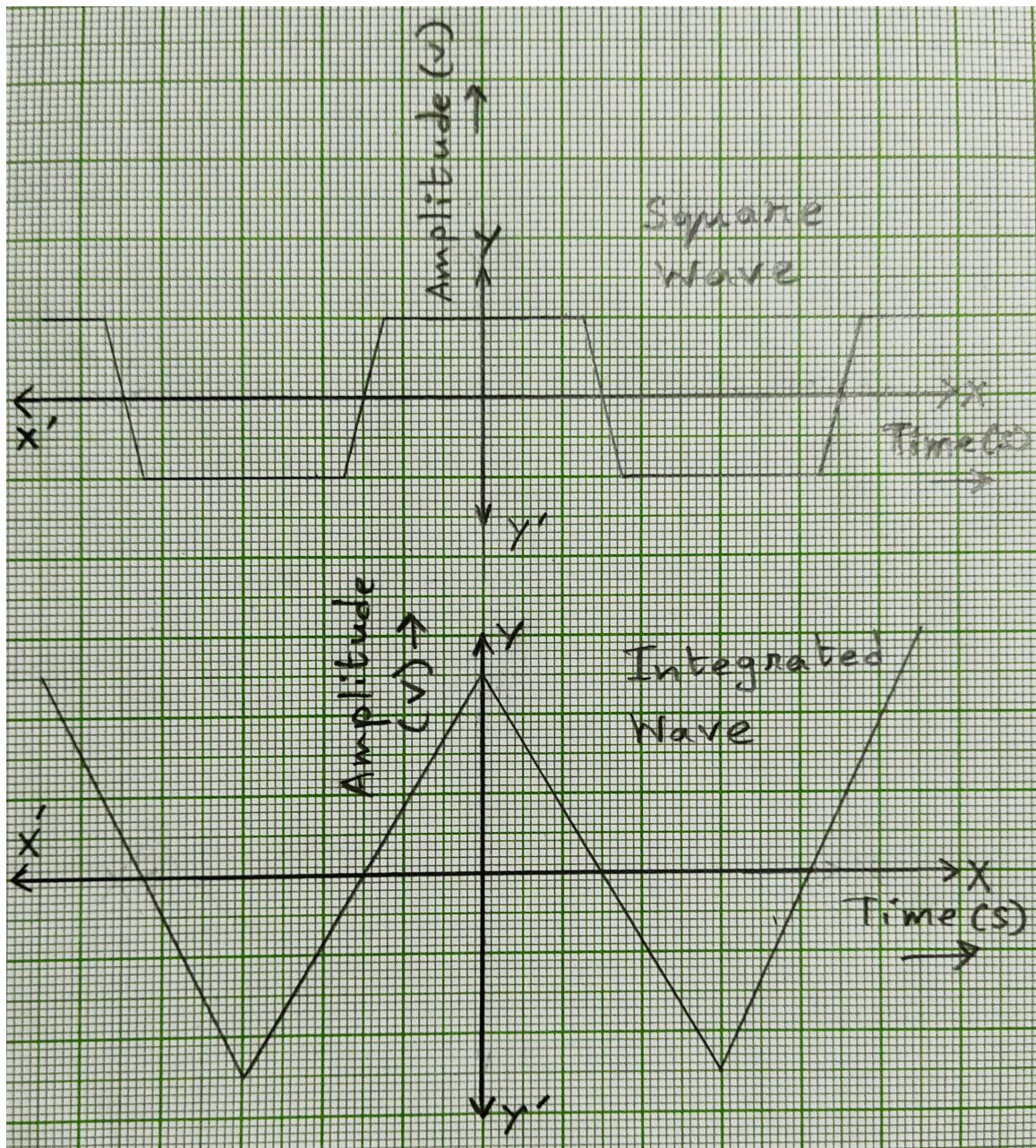
CIRCUIT



CONTROLS



Activate Windows
Go to Settings to activate Windows.

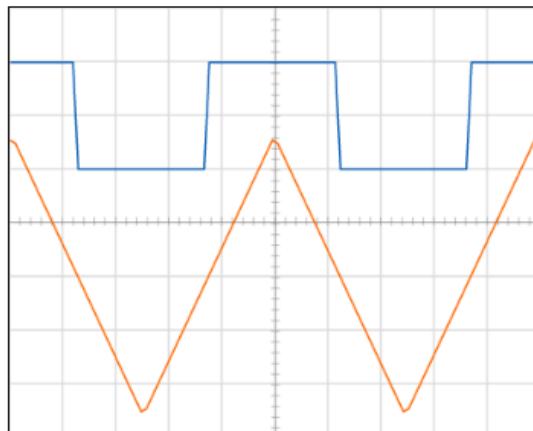


Graph 2: Integrator using Op-Amp Square Wave Plot

Integrator using Opamp

INSTRUCTION

OSCILLOSCOPE



Channel 1

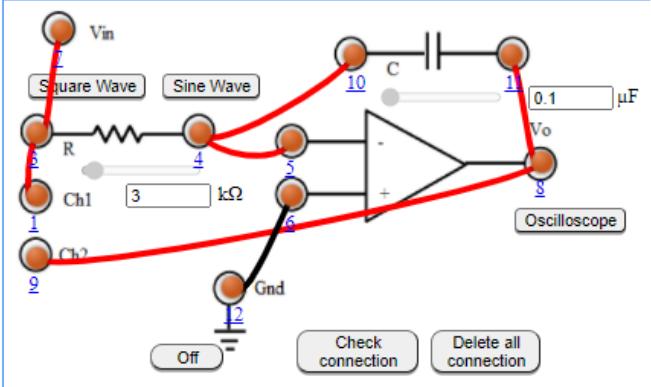
Channel 2

Ground

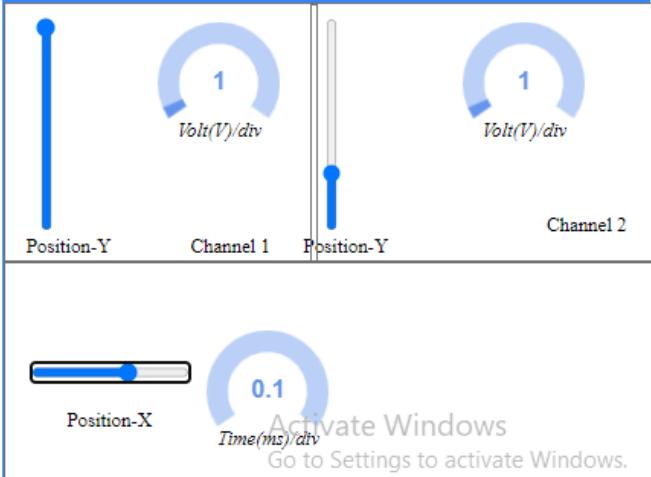
Dual



CIRCUIT



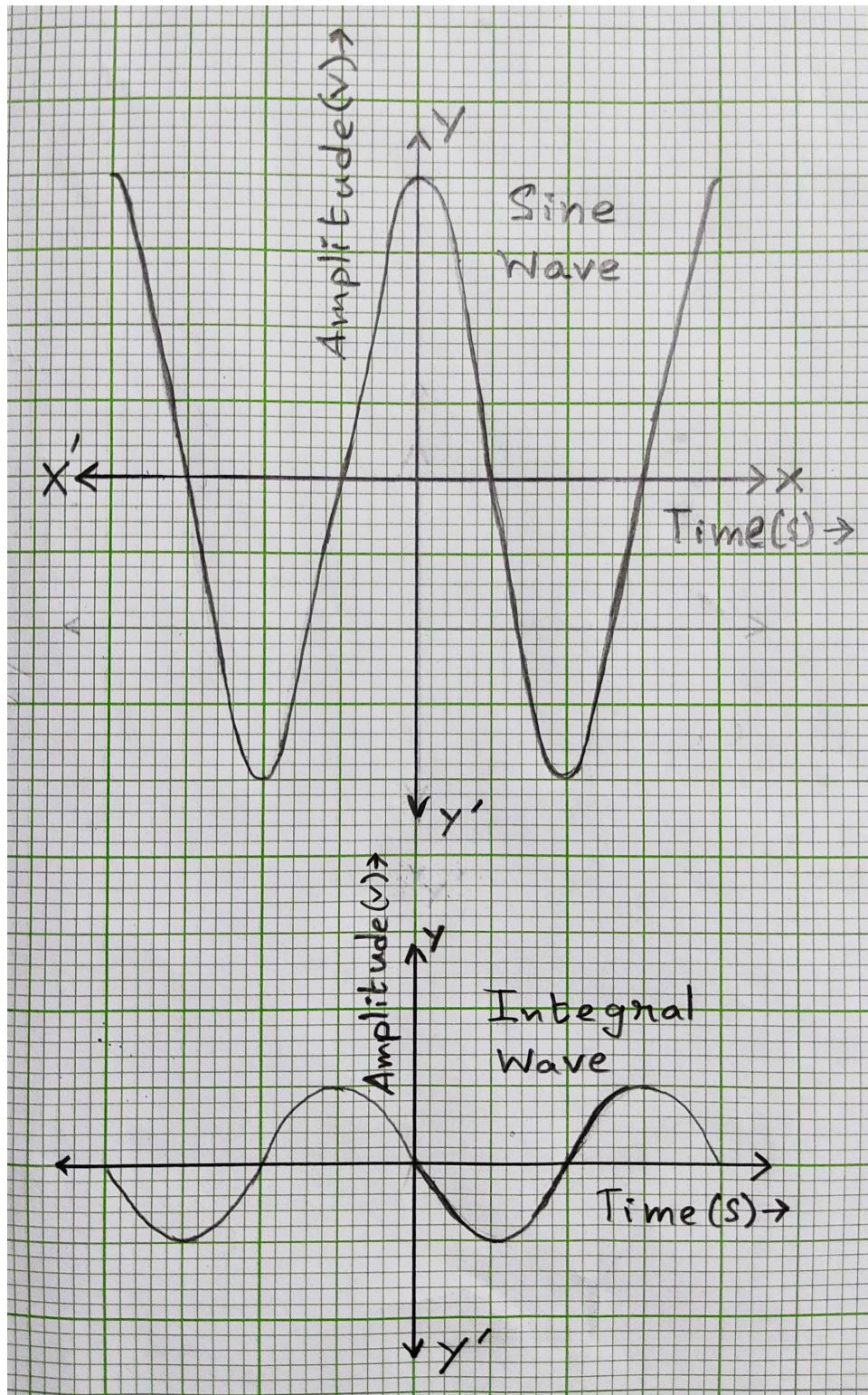
CONTROLS



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Differentiator using Op-Amp-

- Capacitor: $0.1 \mu F$
- Resistance: $1 K\Omega$
- Frequency: $2 KHz$
- Amplitude: $1 V$

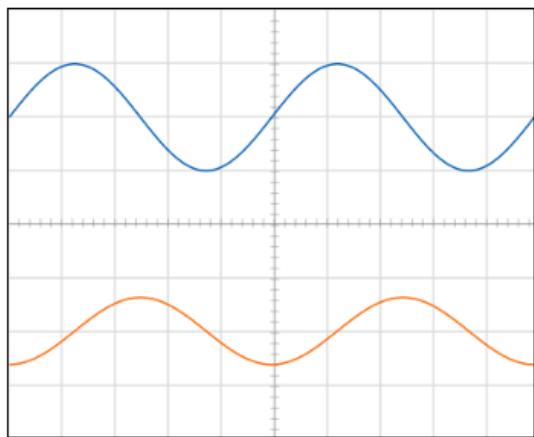


Graph 1: Differentiator using Op-Amp Sine Wave Plot

Differentiator using Opamp

INSTRUCTION

OSCILLOSCOPE



Channel 1

Channel 2

Ground

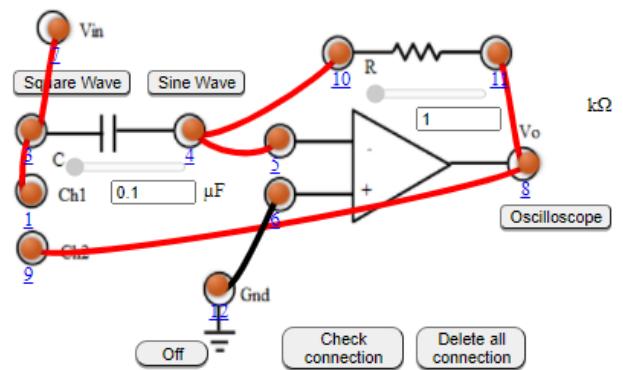
Dual

2000
Frequency(Hz)

1
Amplitude(Volt)

Virtual Oscilloscope Tutorial : [Virtual Oscilloscope Tutorial](#)

CIRCUIT

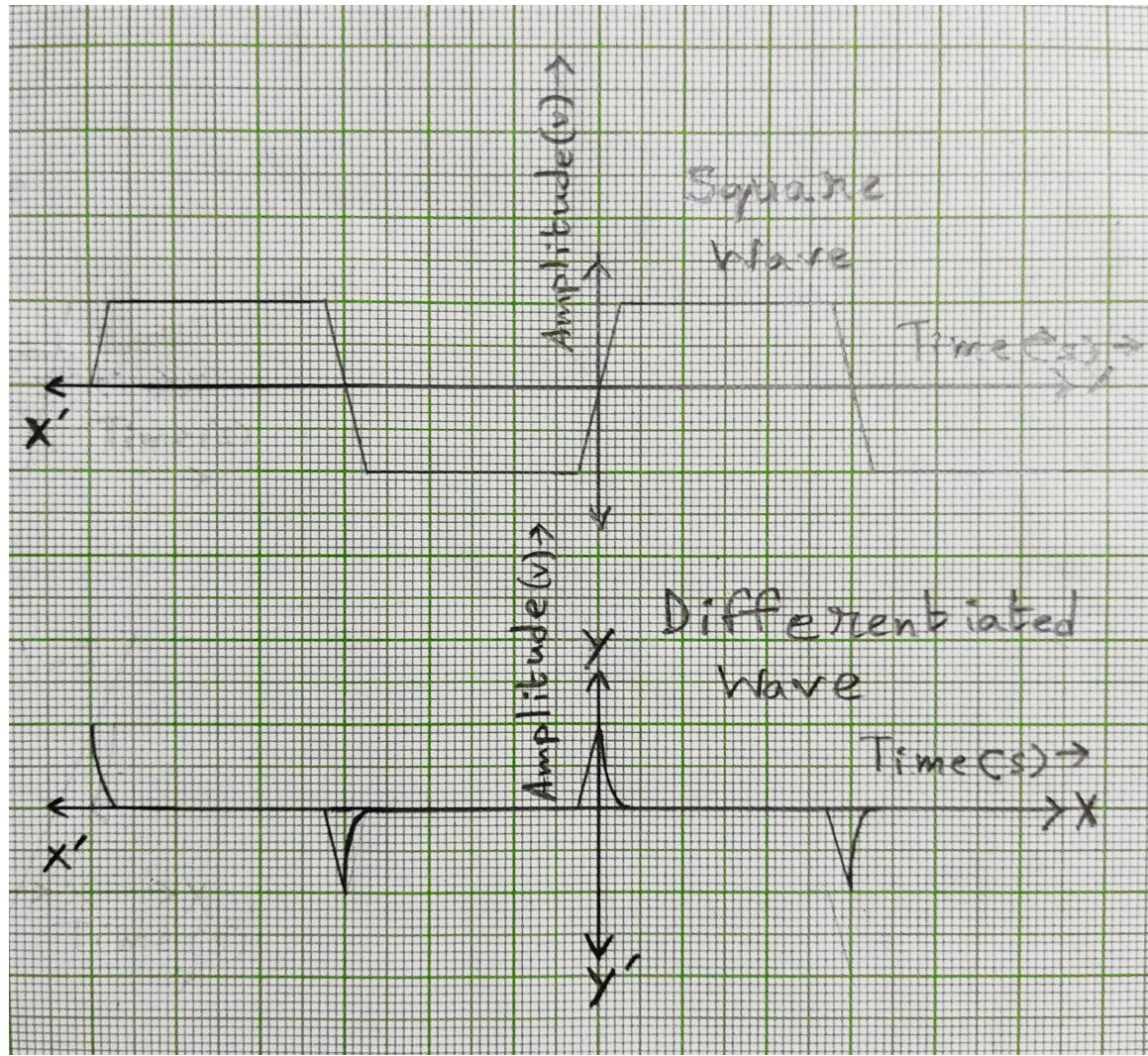


CONTROLS

 Position-Y Channel 1	 Position-Y Channel 2
 Position-X	 Position-Y Channel 2

Activate Windows
Go to Settings to activate Windows.

0.1
Time(ms/div)



Graph 2: Differentiator using Op-Amp Square Wave Plot

Differentiator using Opamp

INSTRUCTION

OSCILLOSCOPE

Channel 1 Channel 2 Ground Dual

Frequency(Hz) Amplitude(Volt)

CIRCUIT

Vin Square Wave Sine Wave
C Ch1 0.1 μ F Ch2
1 Gnd
10 R 11 Vo 1 8 Oscilloscope
Off Check connection Delete all connection

CONTROLS

Position-Y	1 Volt(V)/div	1 Volt(V)/div
Channel 1	Position-Y	Channel 2
Position-X	0.1 Time(ms)/div	Activate Windows Go to Settings to activate Windows.

Conclusion:-

Thus the practical and theoretical gain values match and are equal for both the Inverting and Non-Inverting OP-Amp. The screenshots are attached below.