

Electronics Practical

Name : Archana Kumari , Dept. : ECE

Univ. Roll No.: T91/ECE/204058 , Class Roll No.: 408

Analog Electronics Practical:

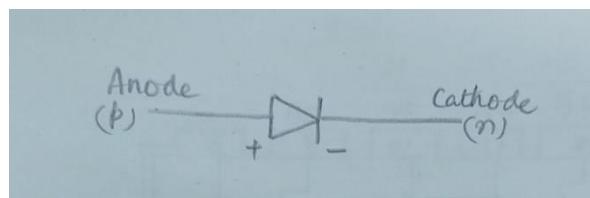
Exp - 1 :

Aim: Study of V-I characteristics of a P-N junction diode under Forward bias and reverse bias.

Theory:

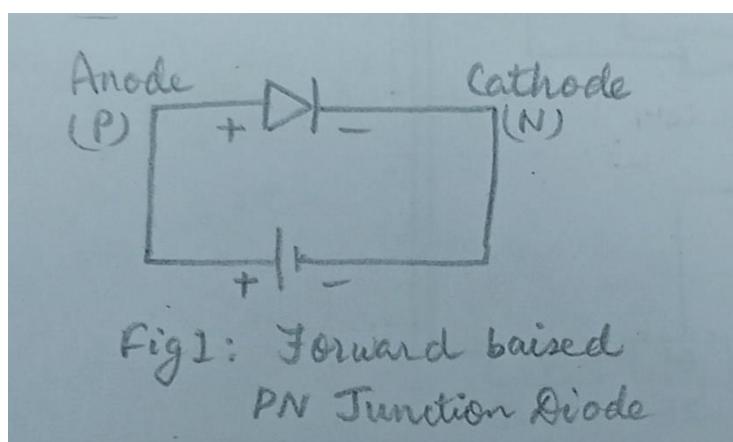
Structure ->

The diode is a device formed from a junction of n-type and p-type semiconductor material. The lead connected to the p-type material is called the anode and the lead connected to the n-type material is the cathode. In general, the cathode of a diode is marked by a solid line on the diode.



Function of a P-N junction diode in Forward Bias ->

The positive terminal of battery is connected to the P side(anode) and the negative terminal of battery is connected to the N side(cathode) of a diode, the holes in the p-type region and the electrons in the n-type region are pushed toward the junction and start to neutralize the depletion zone, reducing its width. The positive potential applied to the p-type material repels the holes, while the negative potential applied to the n-type material repels the electrons. The change in potential between the p side and the n side decreases or switches sign. With increasing forward-bias voltage, the depletion zone eventually becomes thin enough that the zone's electric field cannot counteract charge carrier motion across the p-n junction, which as a consequence reduces electrical resistance. The electrons that cross the p-n junction into the p-type material (or holes that cross into the n-type material) will diffuse into the nearby neutral region. The amount of minority diffusion in the near-neutral zones determines the amount of current that may flow through the diode.

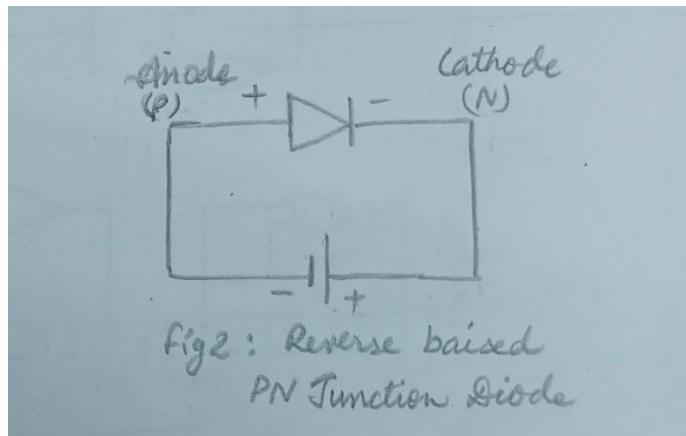


Function of a P-N junction diode in Reverse Bias -> The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode. Therefore, very little current will flow until the diode breaks down.

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Diode Equation ->

In the forward-biased and reversed-biased regions, the current (I_f), and the voltage (V_f), of a semiconductor diode are related by the diode equation.

$$I_f = I_s \times \left(\exp^{\frac{V_f}{n \times V_T}} - 1 \right)$$

where,

I_s is reverse saturation current or leakage current,

I_f is current through the diode (forward current),

V_f is potential difference across the diode terminals (forward voltage)

V_t is thermal voltage, given by

$$V_T = \frac{k \times T}{q}$$

Experimental Data:

Diode: 1N4001

Knee Voltage: 0.6 V

Resistance: 100 ohms

Forward Bias Characteristics:

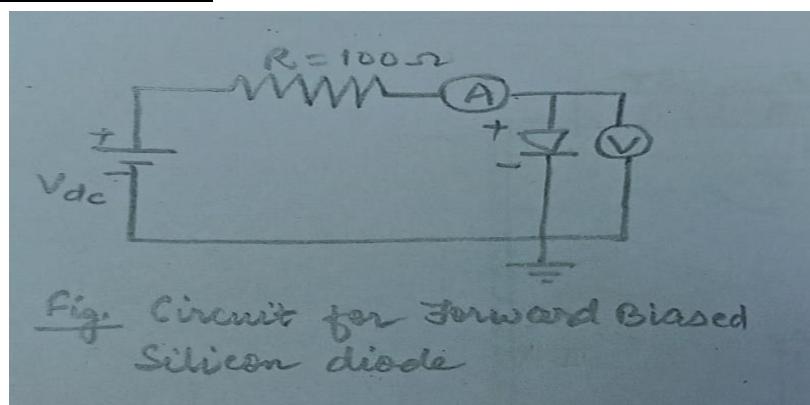
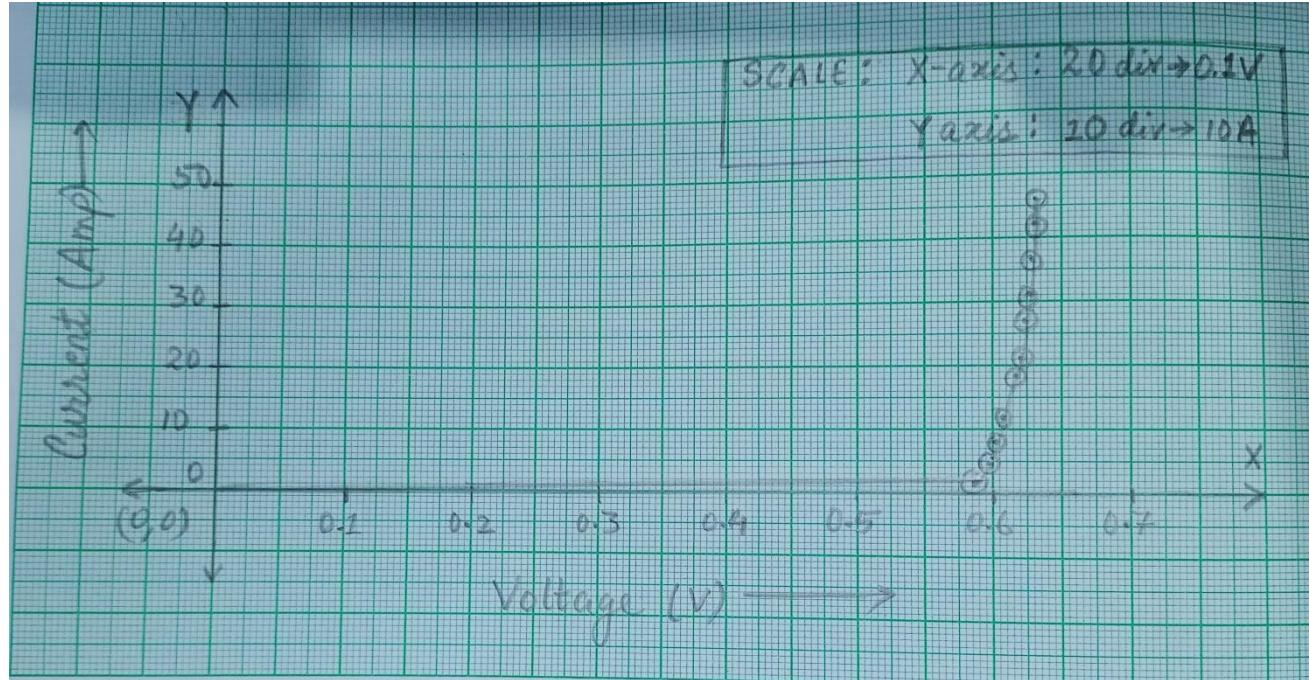


Table: Observation table for the Forward Biased Silicon diode:

Serial No.	Forward Voltage(Volt)	Forward Current(mAmp)
1	0	0
2	0.589	0.997
3	0.593	1.99
4	0.599	3.99
5	0.607	7.98
6	0.615	13.0
7	0.618	15.0
8	0.622	18.9
9	0.626	22.9
10	0.628	24.9
11	0.632	29.9
12	0.635	33.9
13	0.638	39.9
14	0.641	43.9

Graphs:



Screenshot Attached:

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Reverse Baised characteristics:

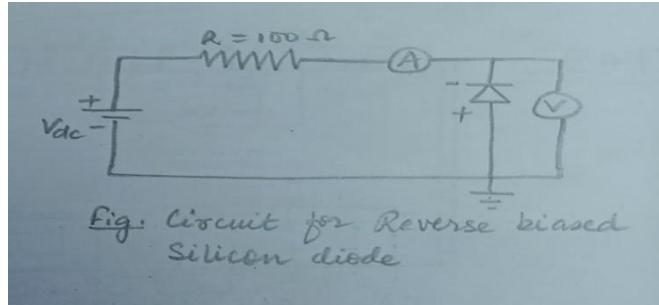
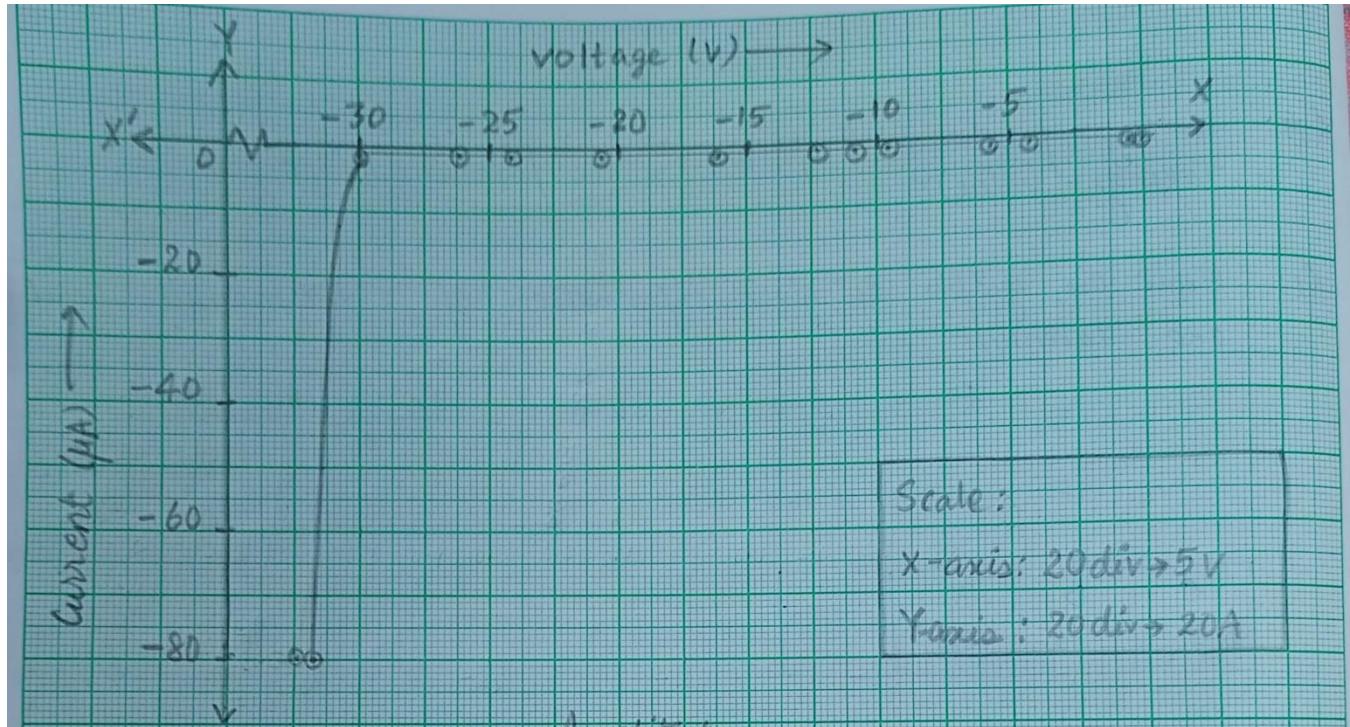


Table: Observation table for the Reverse Biased Silicon diode:

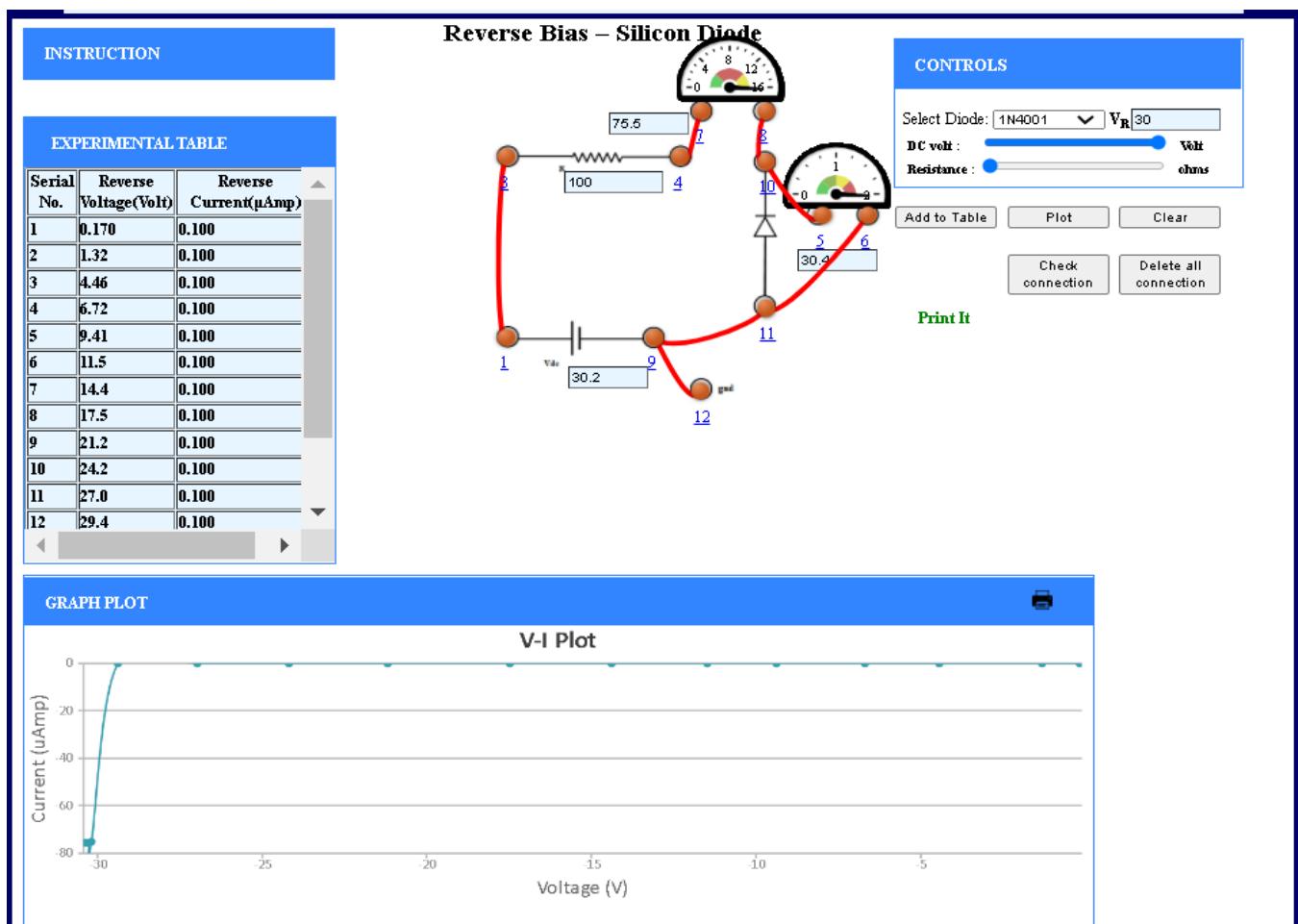
Serial No.	Reverse Voltage(Volt)	Reverse Current(μAmp)
1	0.170	0.100
2	1.32	0.100
3	4.46	0.100
4	6.72	0.100
5	9.41	0.100
6	11.5	0.100
7	14.4	0.100
8	17.5	0.100
9	21.2	0.100
10	24.2	0.100
11	27.0	0.100
12	29.4	0.100
13	30.2	75.125
14	30.3	75.37499999999999
15	30.4	75.5

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Graph:



Screenshot Attached:



Conclusion: We observed from the V-I characteristics graph of forward biased Si diode, that there the graph is almost flat, with small linear rise until the knee voltage is achieved and after that there is a steep rise in current flowing through the diode. From V-I characteristics of Reversed biased Si diode, we observed that there is almost no change in the voltage until the breakdown region of the diode is achieved and after that there is a sudden increase in the current flowing through the diode.



Experiment – 2, 3 & 4:

AIM:

Study on half wave and full wave rectifier & Capacitive Rectification. Determination of ripple factor.

THEORY:

Half Wave Rectifier-

A half wave rectifier is defined as a type of rectifier that only allows one half-cycle of an AC voltage waveform to pass, blocking the other half-cycle. On the positive cycle the diode is forward biased and on the negative cycle the diode is reverse biased. By using a diode we have converted an AC source into a pulsating DC source

The Ripple Factor in a half wave rectifier can be calculated with the following equations:

$$V_{rms} = \frac{V_m}{2}, \quad V_{dc} = \frac{V_m}{\pi}$$

$$V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

$$\text{Ripple Factor} = \frac{V_{ac}}{V_{dc}}$$

Where,

V_{dc} = Output DC Voltage

V_m = Peak Voltage

Full Wave Rectifier-

A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output and A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output.

To calculate the Ripple Factor:

$$V_{rms} = \frac{V_m}{\sqrt{2}}, \quad V_{dc} = \frac{2 \times V_m}{\pi}$$

$$\text{Since, } V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

$$\text{Ripple Factor} = \frac{V_{ac}}{V_{dc}}$$

Where,

V_{dc} = Output DC Voltage

V_m = Peak Voltage

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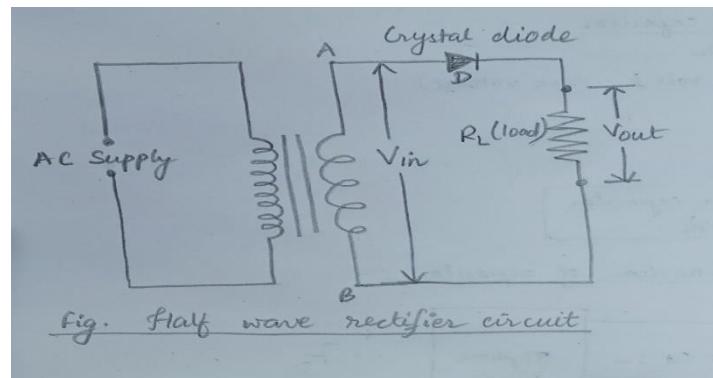
EXPERIMENTAL DATA:

Frequency = 1000 Hz

$R_L = 200 \Omega$

Half Wave Rectifier-

Circuit Diagram-



Calculation for Ripple factor-

Here, resistance, $R = 200 \Omega$
 Peak current, $I_0 = 1.499 \text{ mA}$
 $\approx 1.5 \text{ mA}$

$$\Rightarrow V_m = I_0 R \\ = 1.5 \times 10^{-3} \times 200 \text{ V} \\ = 0.3 \text{ V}$$

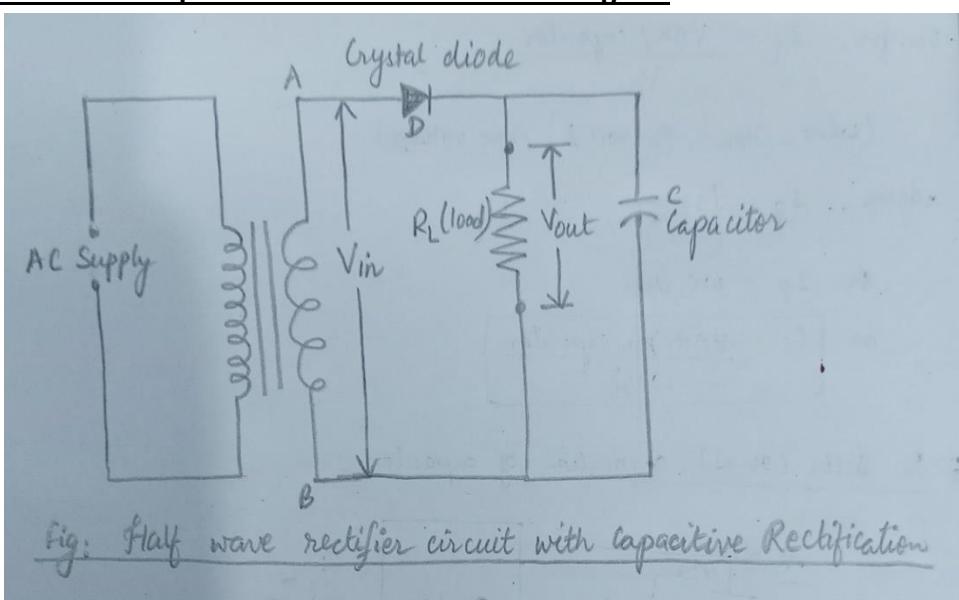
$$\Rightarrow V_{rms} = \frac{V_m}{\sqrt{2}} = 0.15 \text{ V}$$

$$\Rightarrow V_{dc} = \frac{V_m}{\pi} = \frac{0.3}{\pi} = 0.096 \text{ V}$$

$$\Rightarrow V_{ac} = \sqrt{(V_{rms})^2 - (V_{dc})^2} \\ = \sqrt{(0.15)^2 - (0.096)^2} \\ \approx 0.1162 \text{ V}$$

$$\Rightarrow \text{Ripple factor} = \frac{V_{ac}}{V_{dc}} = \frac{0.1162}{0.096} \\ \approx 1.210$$

Half Wave Rectifier with Capacitive Rectification Circuit Diagram-

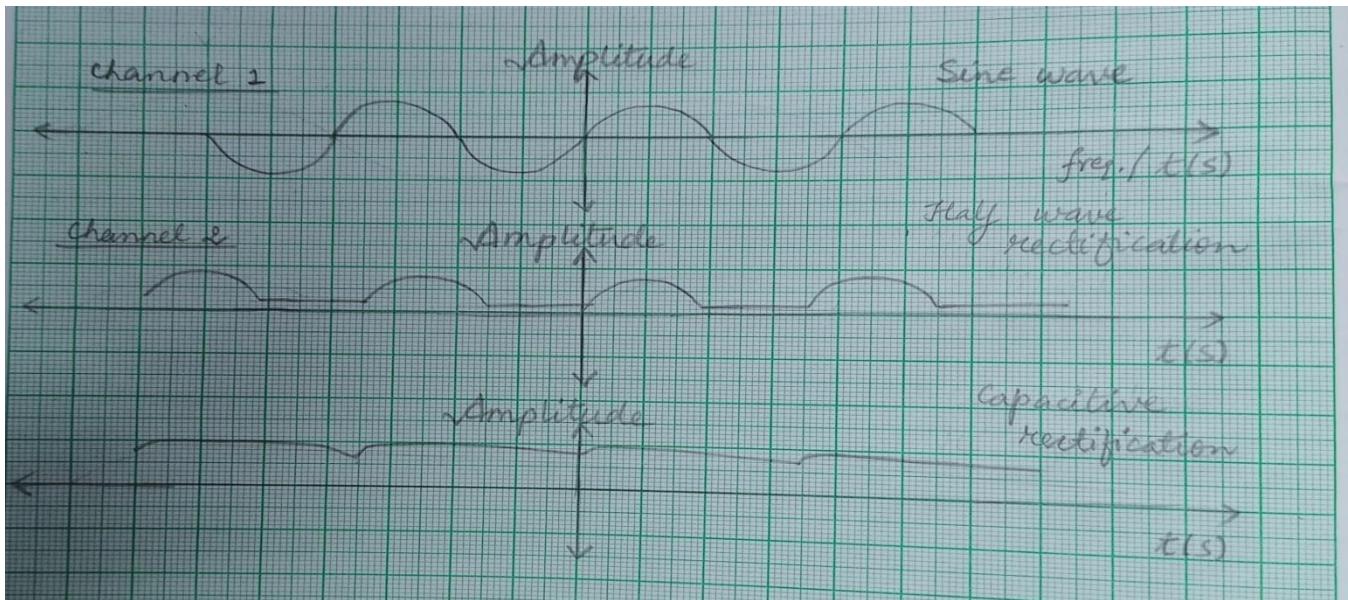


Waveform for Sine Wave, Half Wave Rectified, Half Wave and Capacitive Rectified

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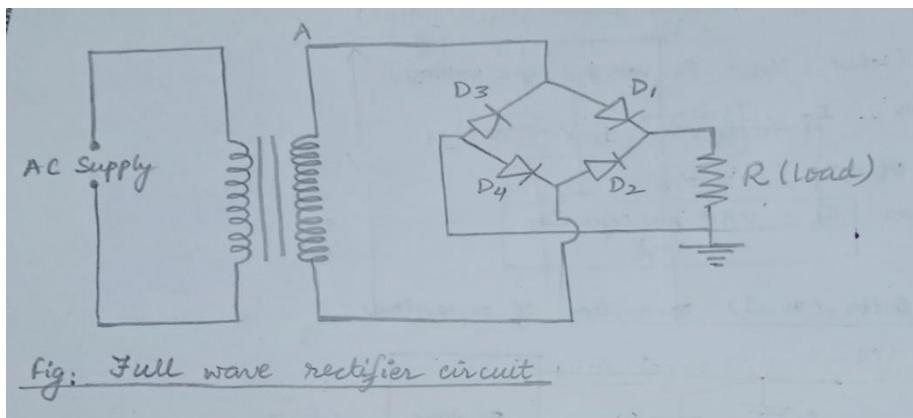
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Full Wave Rectifier-

Circuit Diagram-



Calculation:

$$\text{Here, resistance, } R = 100 \Omega$$

$$\text{Peak current, } I_0 = 2.99 \text{ mA}$$

$$\Rightarrow V_{m} = I_0 R \\ = 2.99 \times 10^{-3} \times 100 \text{ V} \\ = 0.299 \text{ V}$$

$$\Rightarrow V_{rms} = \frac{V_m}{\sqrt{2}} = 0.2114 \text{ A.V}$$

$$\Rightarrow V_{dc} = \frac{2 V_m}{\pi} = 0.1903 \text{ V}$$

$$\Rightarrow V_{ac} = \sqrt{(V_{rms})^2 - (V_{dc})^2} \\ = \sqrt{(0.2114)^2 - (0.1903)^2}$$

$$\Rightarrow V_{ac} = 0.09206 \text{ V}$$

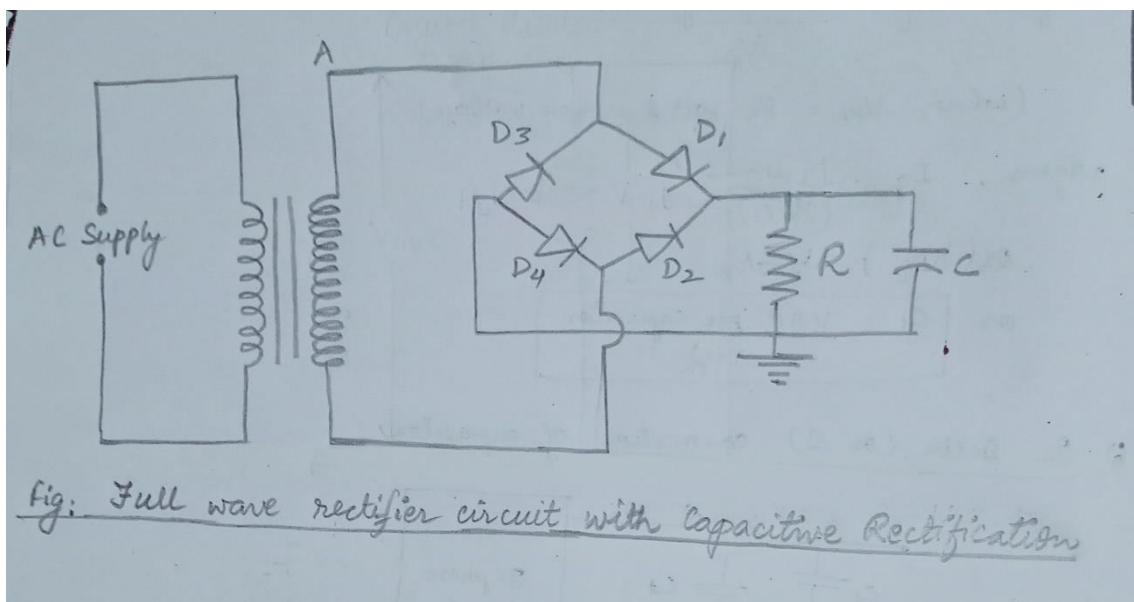
$$\Rightarrow \text{Ripple factor} = \frac{V_{ac}}{V_{dc}} = \frac{0.09206}{0.1903} = 0.483$$

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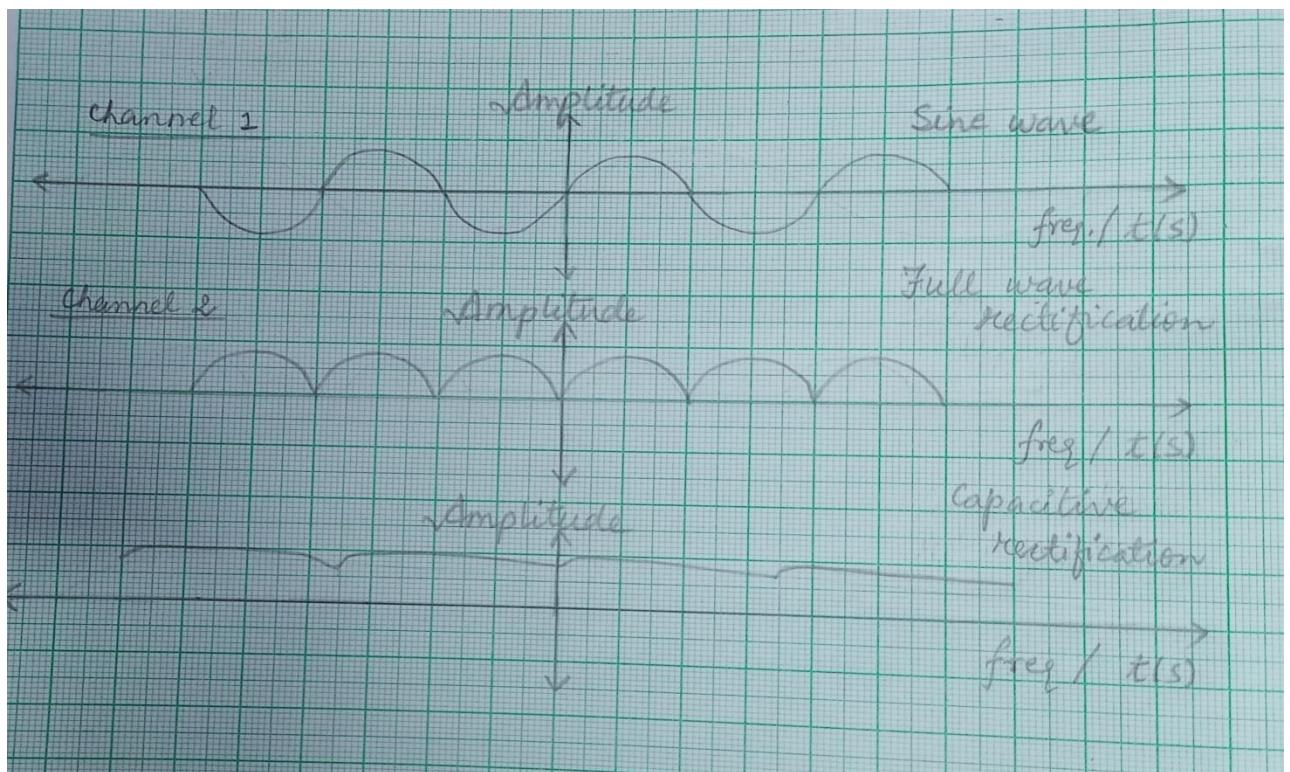
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Full Wave Rectifier with Capacitive Rectification Circuit Diagram-



Waveform for Sine Wave, Full Wave Rectified, Full Wave and Capacitive Rectified:



Screenshots Attached:

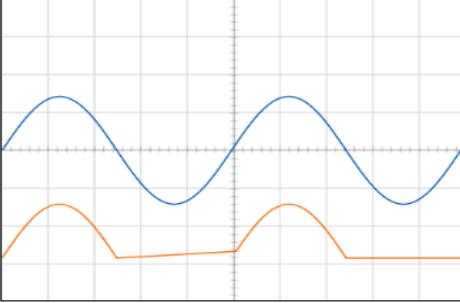
1. Half wave rectifier:

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Half Wave Rectifier

INSTRUCTION

OSCILLOSCOPE



Channel 1 Channel 2 Ground Dual

2000 Frequency(Hz) 1 Amplitude(Volt)

CALCULATION

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

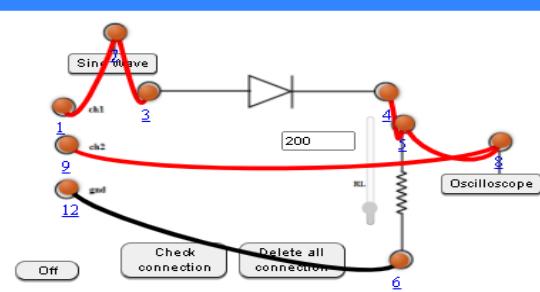
$$V_{dc} = \frac{V_m}{\pi}$$

$$\text{Ripple Factor} = \frac{V_r}{V_d}$$

Since, $V_{ar} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$

Peak Current: 1.499999946345703 mA

CIRCUIT



Off Check connection Delete all connection

CONTROLS

Position-Y Channel 1 Position-Y Channel 2

0.8 Volt(V)/div 0.70001 Volt(V)/div Ohms

Position-X

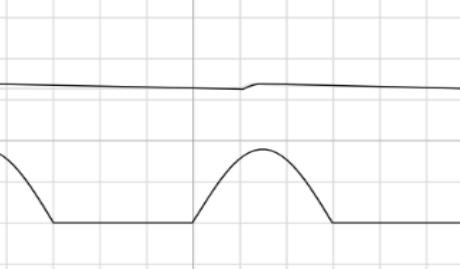
0.1 Time(ms)/div

Virtual Oscilloscope Tutorial : [Virtual Oscilloscope Tutorial](#)

Capacitative Rectification for Half Wave Rectifier

INSTRUCTION

GRAPH PLOT



Channel 1 Channel 2 Ground Dual

CALCULATION

Measure the V_m

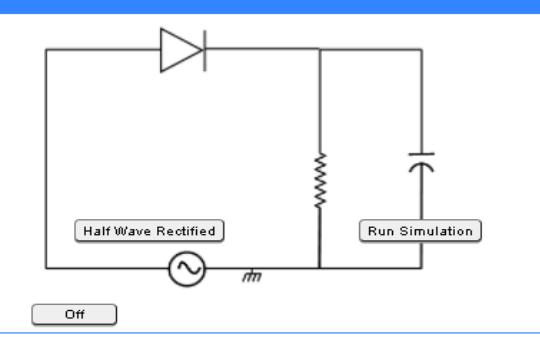
$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{dc} = \frac{V_m}{\pi}$$

$$\text{Ripple Factor} = \frac{V_r}{V_d}$$

Since, $V_{ar} = \frac{\sqrt{(V_{rms}^2 - V_{dc}^2)}}{V_{dc}}$

CIRCUIT



Off Run Simulation

CONTROLS

V_{PcM} : 0.9 V

Position Y-Axis: -1.79

Phase: 0 Deg

Frequency: 1000 Hz

V_{PcM} : 0.7 V

Position Y-Axis: 0.09

Phase: 0 Deg

Frequency: 1000

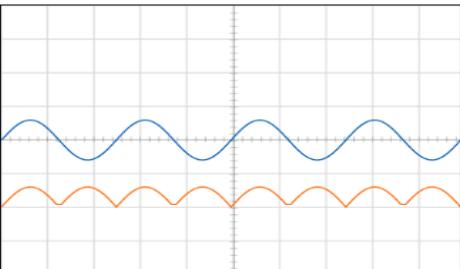
2. Full Wave Rectifier:

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Full Wave Rectifier

INSTRUCTION

OSCILLOSCOPE



Channel 1 Channel 2 Ground Dual

Frequency (Hz) : 4000 Amplitude (Volt) : 0.6

CALCULATION

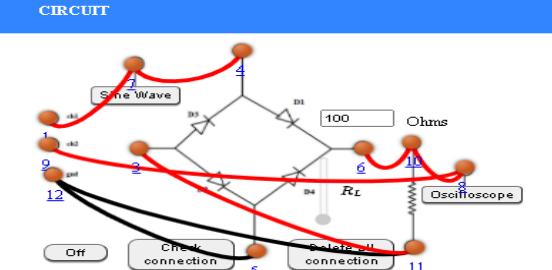
$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{dc} = \frac{2 \times V_m}{\pi}$$

$$\text{Ripple Factor} = \frac{V_r}{V_d} \quad \text{Since, } V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

Peak Current : 2.9999999992691407 mA

CIRCUIT



CONTROLS

Position-Y Channel 1 Position-Y Channel 2

Volt(V/div) Volt(V/div)

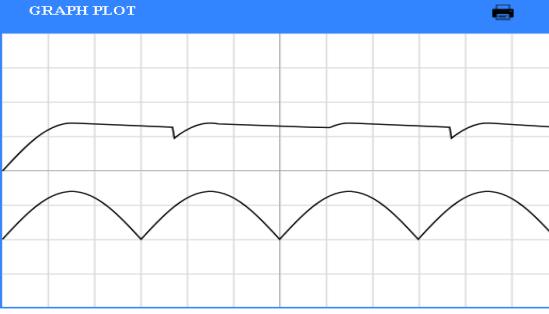
Position-X

Time(ms/div) : 0.1

Capacitative Rectification for Full Wave Rectifier

INSTRUCTION

GRAPH PLOT



Channel 1 Channel 2 Ground Dual

CALCULATION

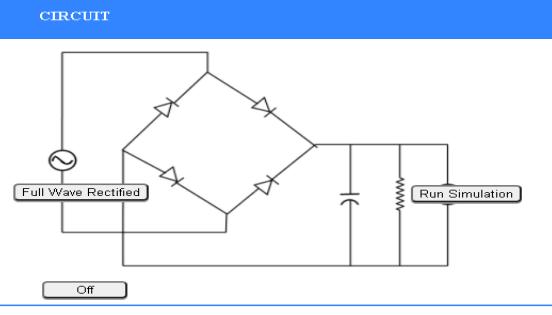
Measure the V_m

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{dc} = \frac{V_m}{\pi}$$

$$\text{Ripple Factor} = \frac{V_{ac}}{V_{dc}} \quad \text{Since, } V_{ac} = \frac{\sqrt{(V_{rms}^2 - V_{dc}^2)}}{V_{dc}}$$

CIRCUIT



CONTROLS

V_{Pch1} :	<input type="range"/>	-0.7	V
Position Y-Axis:	<input type="range"/>	-1.12	
Phase:	<input type="range"/>	0	Deg
Frequency:	<input type="range"/>	1000	Hz
V_{Pch2} :	<input type="range"/>	0.7	V
Position Y-Axis:	<input type="range"/>	0.14	
Phase:	<input type="range"/>	0	Deg
Frequency:	<input type="range"/>	1000	

CONCLUSION:

The Ripple factor for Full Wave Rectified circuit is found to be 0.48 & for the Half Wave Rectified circuit it is found to be 1.21. The waveforms obtained on an oscilloscope are drawn on the graph. This shows that capacitive rectification the A.C. is converted to D.C. with good results.

AIM:

Study the V-I Characteristics of Zener Diode under Reverse Bias and Forward Bias.

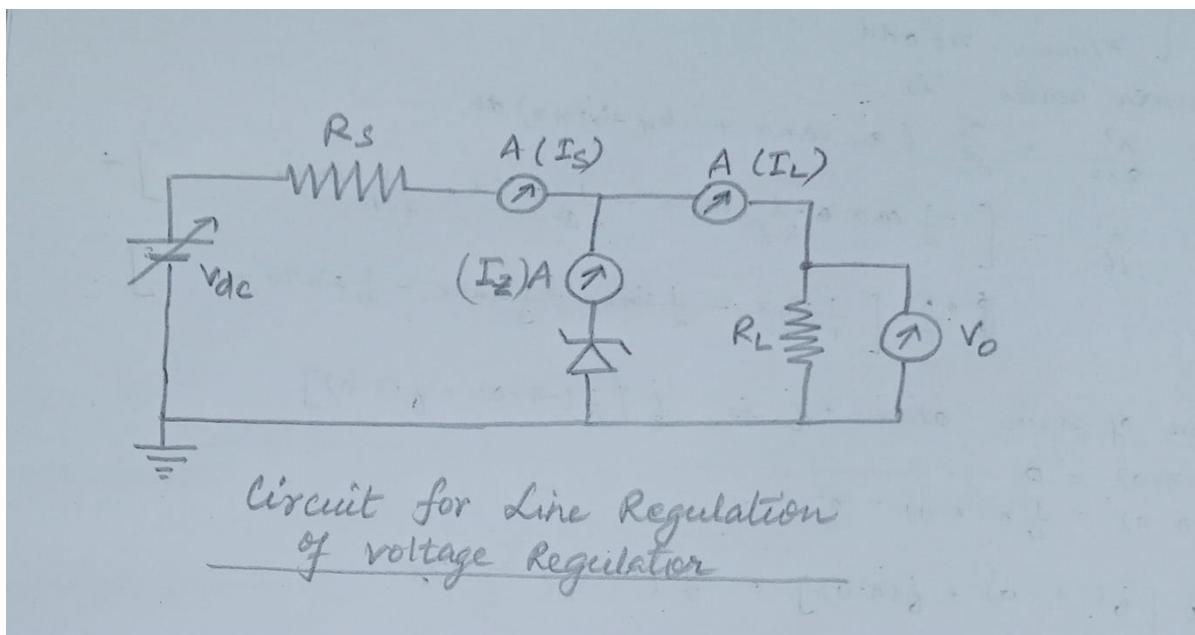
THEORY:

A Zener Diode is a special kind of diode which permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above the breakdown voltage or Zener voltage. Zener diodes are designed so that their breakdown voltage is much lower. In the reverse bias direction, there is practically no reverse current flow until the breakdown voltage is reached. When this occurs, there is a sharp increase in reverse current. Varying amount of reverse current can pass through the diode without damaging it. The breakdown voltage or zener voltage (V_Z) across the diode remains relatively constant.

A voltage regulator is an electronic circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations. A Zener diode of break down voltage V_Z is reverse connected to an input voltage source V_I across a load resistance R_L and a series resistor R_S . The voltage across the Zener will remain steady at its break down voltage V_Z for all the values of zener current I_Z as long as the current remains in the break down region. Hence a regulated DC output voltage $V_O=V_Z$ is obtained across R_L whenever the input voltage remains within a minimum and maximum voltage.

There are 2 types of regulations:

- Line Regulation:** In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.

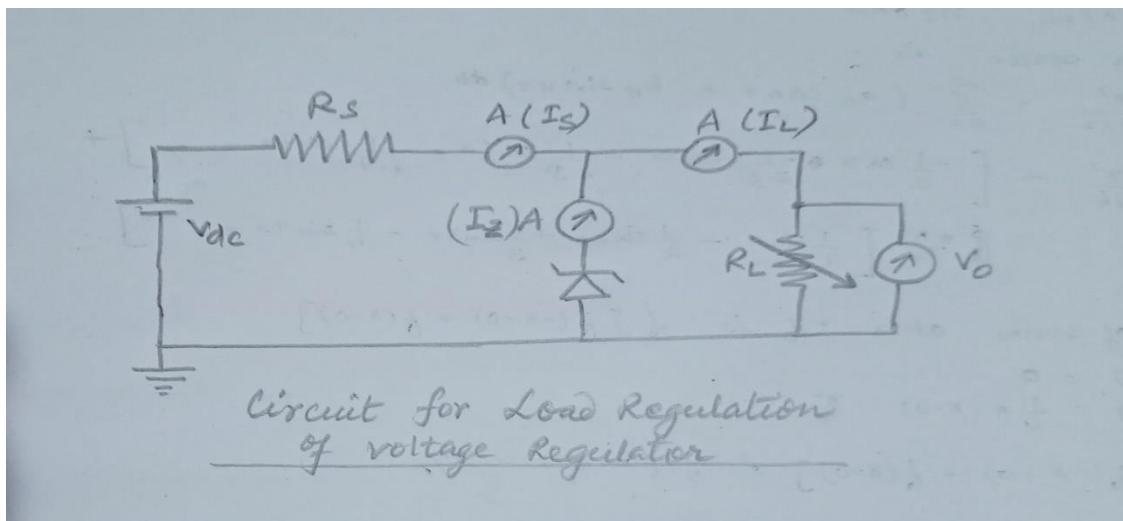


- Load Regulation:** In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

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Experimental Data:

Line Regulation –

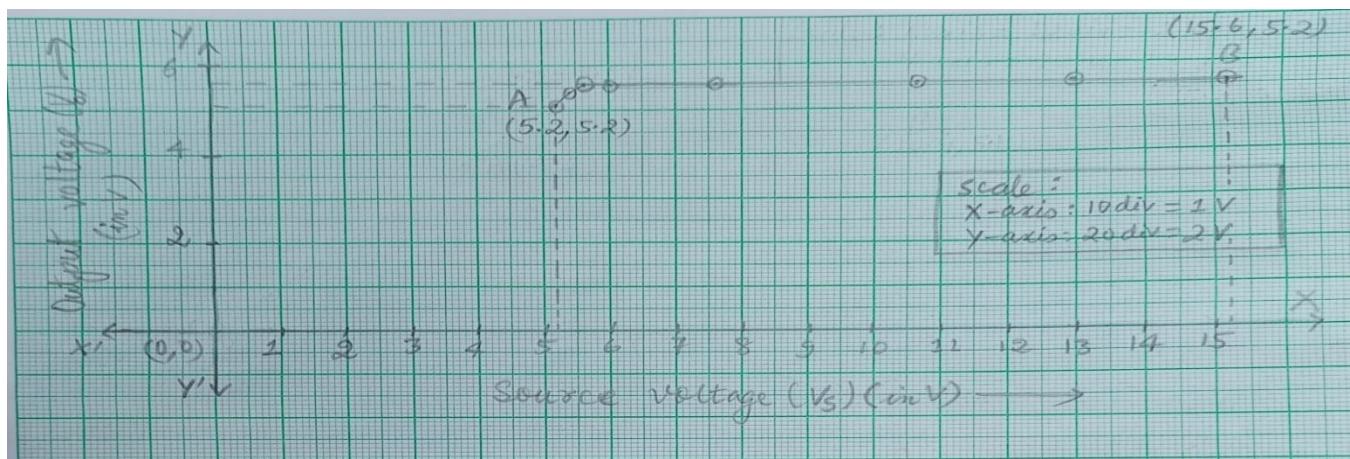
Zener Voltage(V_Z): 5.6 V

Series Resistance(R_S): 0.1 K Ω

Load Resistance (R_L): 1.1 K Ω

Serial No.	Unregulated supply voltage(V_s) V	Load Current(I_L) mAmp	Zener Current(I_Z) mAmp	Regulated Output Voltage(V_o) V	% Voltage Regulation
1	5.2	5.09	0	5.2	100
2	5.4	5.09	0	5.4	100
3	5.6	5.09	0	5.6	100
4	5.8	5.09	-3.091	5.60	100
5	7.6	5.09	14.909	5.60	71.4
6	10.4	5.09	42.909	5.60	50.0
7	13	5.09	68.909	5.60	38.5
8	15.2	5.09	90.909	5.60	33.3
9	19	5.09	128.909	5.60	26.3

Line Regulation Graph –



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CALCULATION OF LINE REGULATION:

From the graph, we obtain the values :

A (5.2, 5.2) & B (15.2, 5.6)

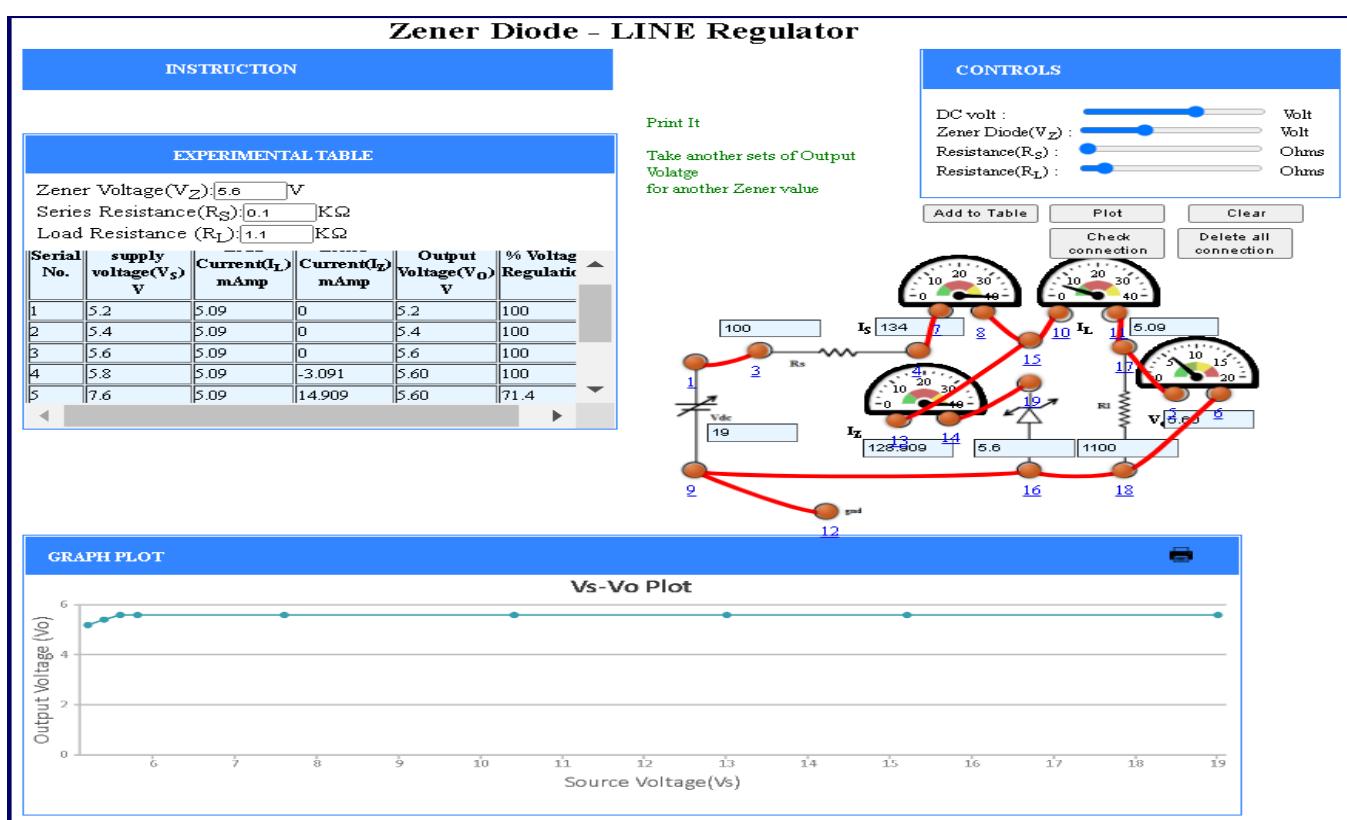
Thus, Line Regulation (S_L) = $\frac{\text{change in Output voltage}}{\text{change in Input voltage}}$

$$= \frac{V_{OB} - V_{OA}}{V_{IB} - V_{IA}}$$

$$= \frac{15.2 - 5.2}{5.6 - 5.2}$$

$$= \frac{10}{0.4} = \frac{100}{4} = 25\%$$

Screenshot attached:



Load Regulation:

DC Voltage (V_{DC}): V Zener Voltage (V_Z): V

Series Resistance (R_S): KΩ

Serial No.	Load Resistance(R _L) Ohm	Load Current(I _L) mAmp	Zener Current(I _Z) mAmp	Regulated Output Voltage(V _O) V	% Voltage Regulation
1	150	34.0	0	8	40.0
2	152	33.6	0	8	39.7
3	172	29.7	0	8	36.8

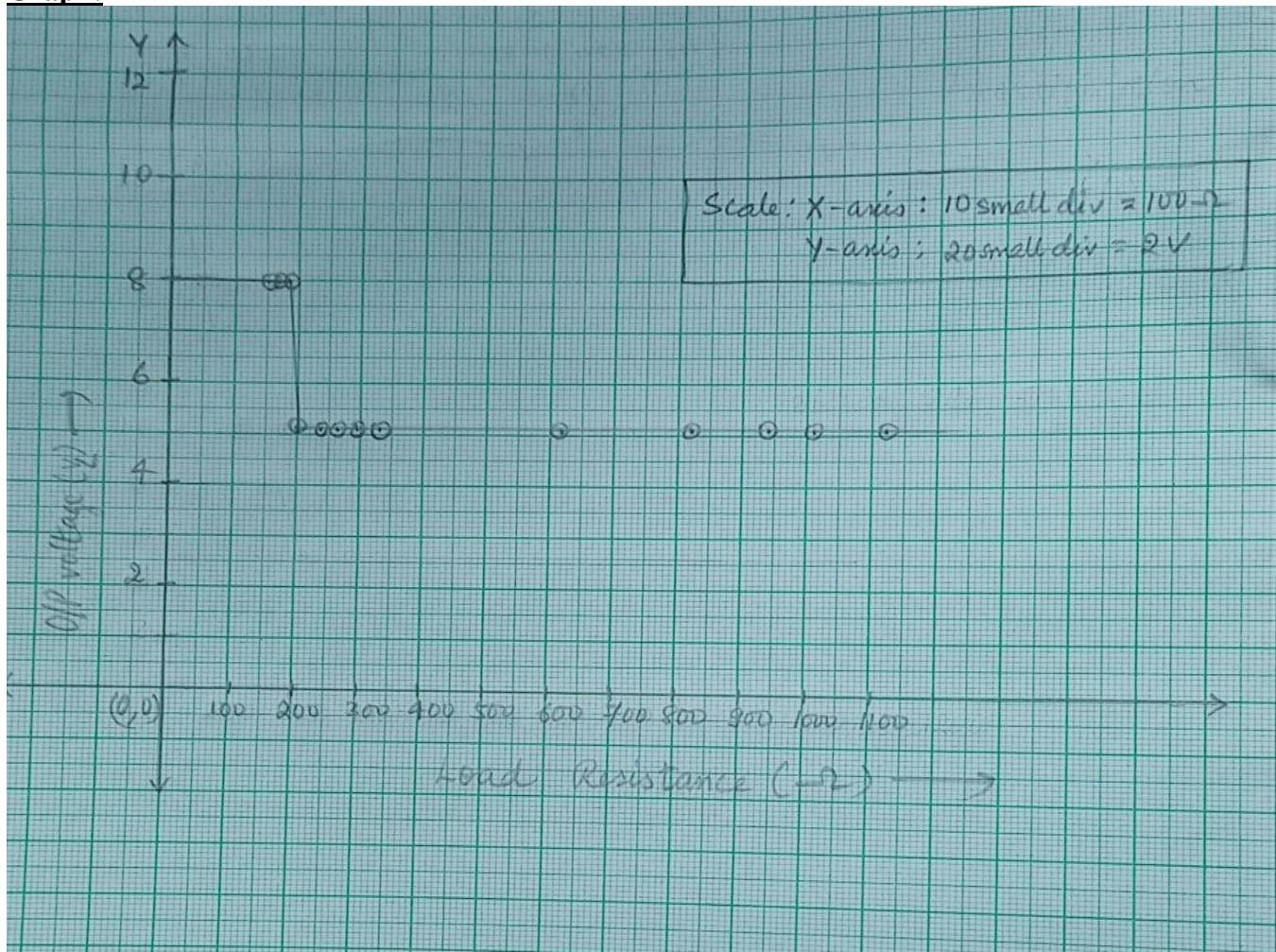
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4	197	25.9	3.11	5.10	33.7
5	223	22.9	6.13	5.10	31.0
6	254	20.1	8.92	5.10	28.2
7	280	18.2	10.8	5.10	26.3
8	324	15.7	13.3	5.10	23.6
9	624	8.17	20.8	5.10	13.8
10	827	6.17	22.8	5.10	10.8
11	948	5.38	23.6	5.10	9.54
12	1063	4.80	24.2	5.10	8.60
13	1235	4.13	24.9	5.10	7.49

Graph:

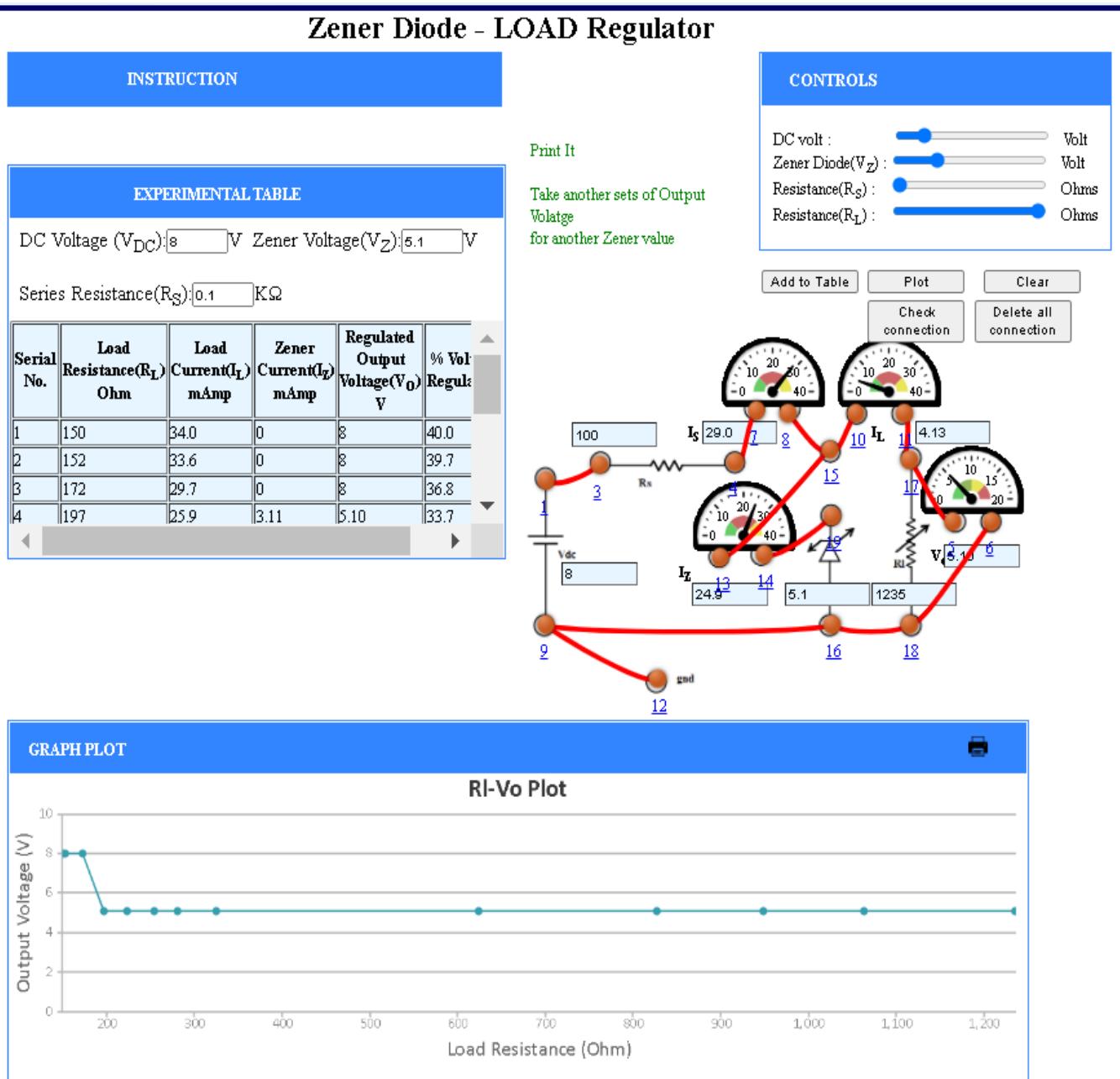


Calculation :

$$\begin{aligned}
 \text{Load Regulation (SL)} &= \frac{V_{NL} - V_L}{V_L} \times 100 && \left\{ \text{where, } V_{NL} \text{ is no load voltage &} \right. \\
 &= \frac{8 - 5.1}{5.1} \times 100 && \left. V_L \text{ is load voltage} \right\} \\
 &= \frac{2.9}{5.1} \times 100 \\
 &= 56.8 \%
 \end{aligned}$$

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Screenshots Attached:



Conclusion: We understood the Zener diode characteristics for Line Regulation & Load Regulation.

The V-I characteristics shows that the unregulated input voltage is regulated to the Zener voltage after the input exceeds the Zener voltage value.



Experiment – 6:

AIM: Study the Input and Output Characteristics Curve for BJT Common Base (CE) mode.

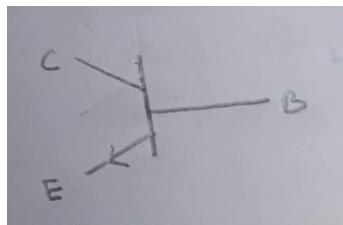
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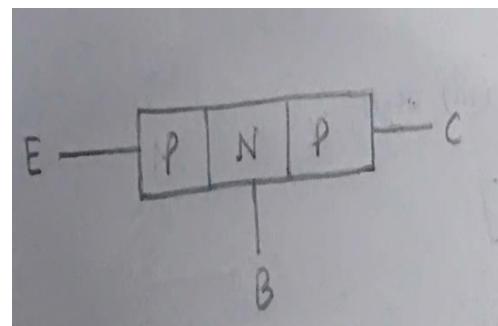
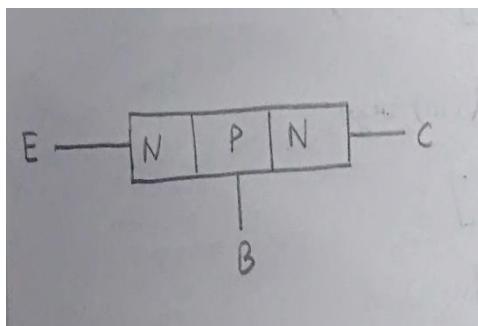
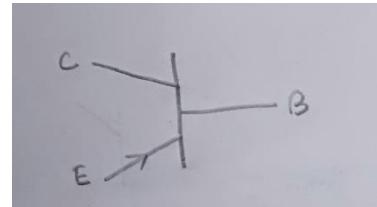
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THEORY: A Common Emitter Bipolar Junction Transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions. BJTs can be made either as PNP or as NPN. They have three regions and three terminals, Emitter, Base, and Collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally.

N-P-N



P-N-P



Emitter is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. Base is the middle very thin and lightly doped region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. Collector is the region with intermediate doping to the right end where charge carriers are collected. The area of this region is largest compared to emitter and base region.

Input Characteristics -

The most important characteristic of the BJT is the plot of the base current, I_B , versus the base-emitter voltage, V_{BE} , for various values of the collector-emitter voltage, V_{CE}

$$I_B = \phi(V_{BE}, V_{CE}) \quad \text{for constant } V_{CE}$$

Output Characteristics -

The most important characteristic of the BJT is the plot of the collector current, I_C , versus the collector-emitter voltage, V_{CE} for various values of the base current, I_B as shown on the circuit on the right.

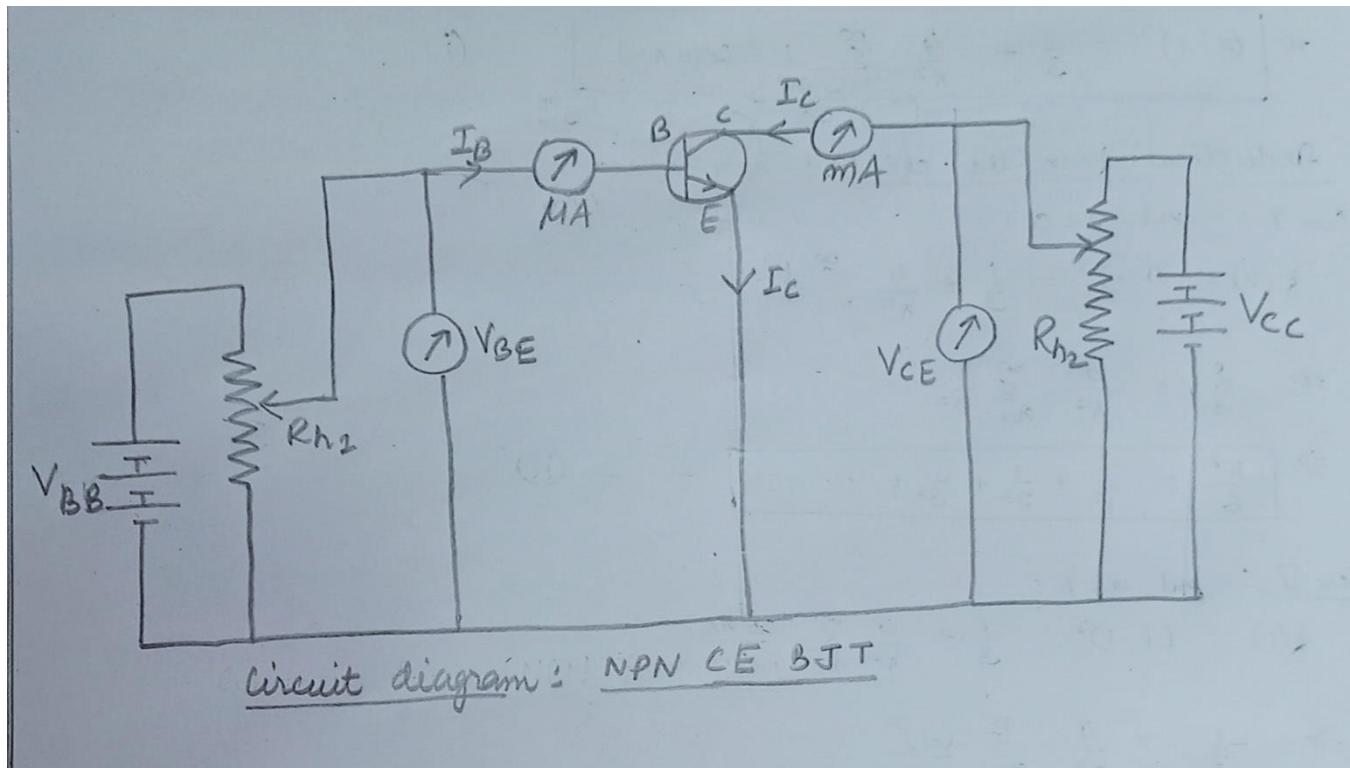
$$I_C = \phi(V_{CE}, I_B) \quad \text{for constant } I_B$$

Circuit Diagram: NPN CE BJT connected for study of input and output characteristics

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EXPERIMENTAL DATA:

Input Characteristics –

Table: SET 1 DATA ($V_{CE} = 1.500 \text{ V}$)

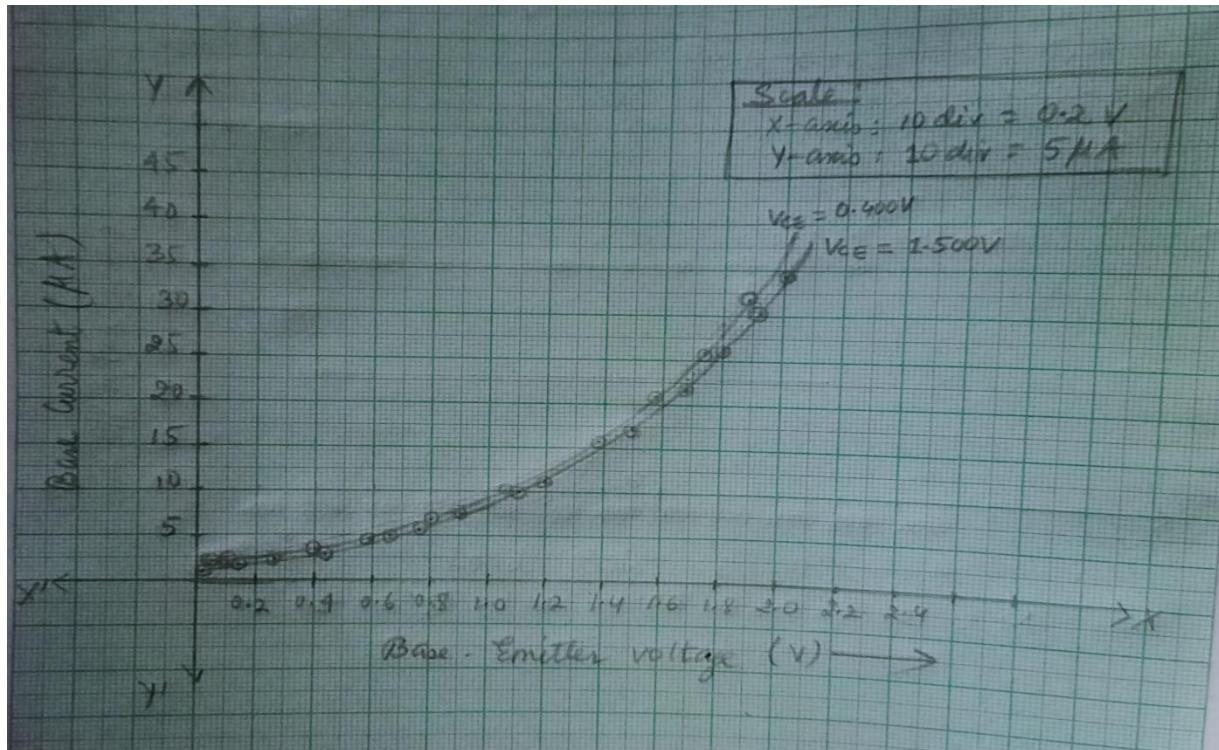
Serial No.	Collector-Emitter Voltage	
	1.50 V	Base Current(μA)
1	0.02000	2.058
2	0.1600	2.514
3	0.2600	2.900
4	0.4400	3.750
5	0.6600	5.135
6	0.7600	5.923
7	0.8800	7.031
8	1.120	9.906
9	1.320	13.18
10	1.520	17.54
11	1.760	24.72
12	1.920	31.06
13	2.000	34.82

Table: SET 2 DATA ($V_{CE} = 0.400 \text{ V}$)

Serial No.	Collector-Emitter Voltage	
	0.40 V	Base Current $I_B (\mu\text{A})$
1	0.04000	2.118
2	0.1000	2.307
3	0.1200	2.374
4	0.2400	2.818
5	0.4600	3.859
6	0.6000	4.713
7	0.8200	6.453
8	1.000	8.345
9	1.180	10.79
10	1.420	15.21
11	1.640	20.82
12	1.820	26.93

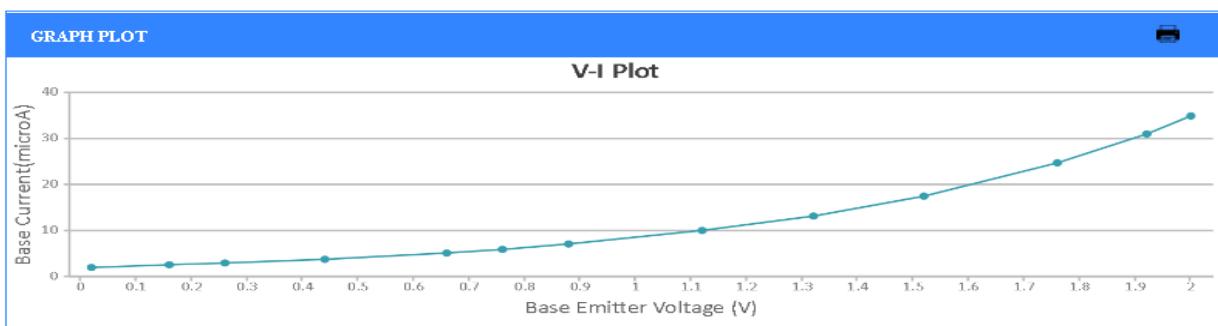
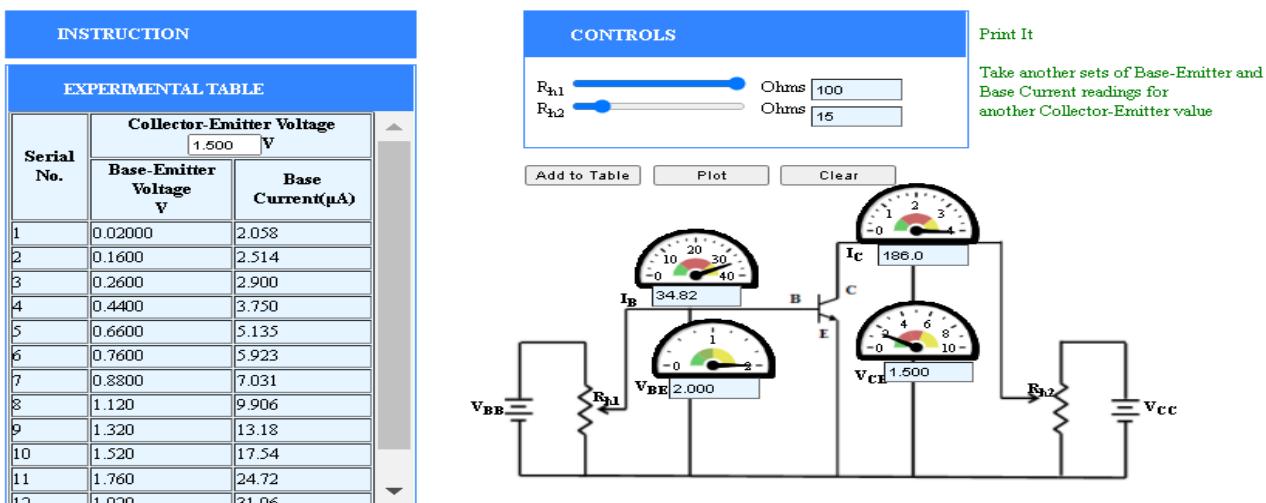
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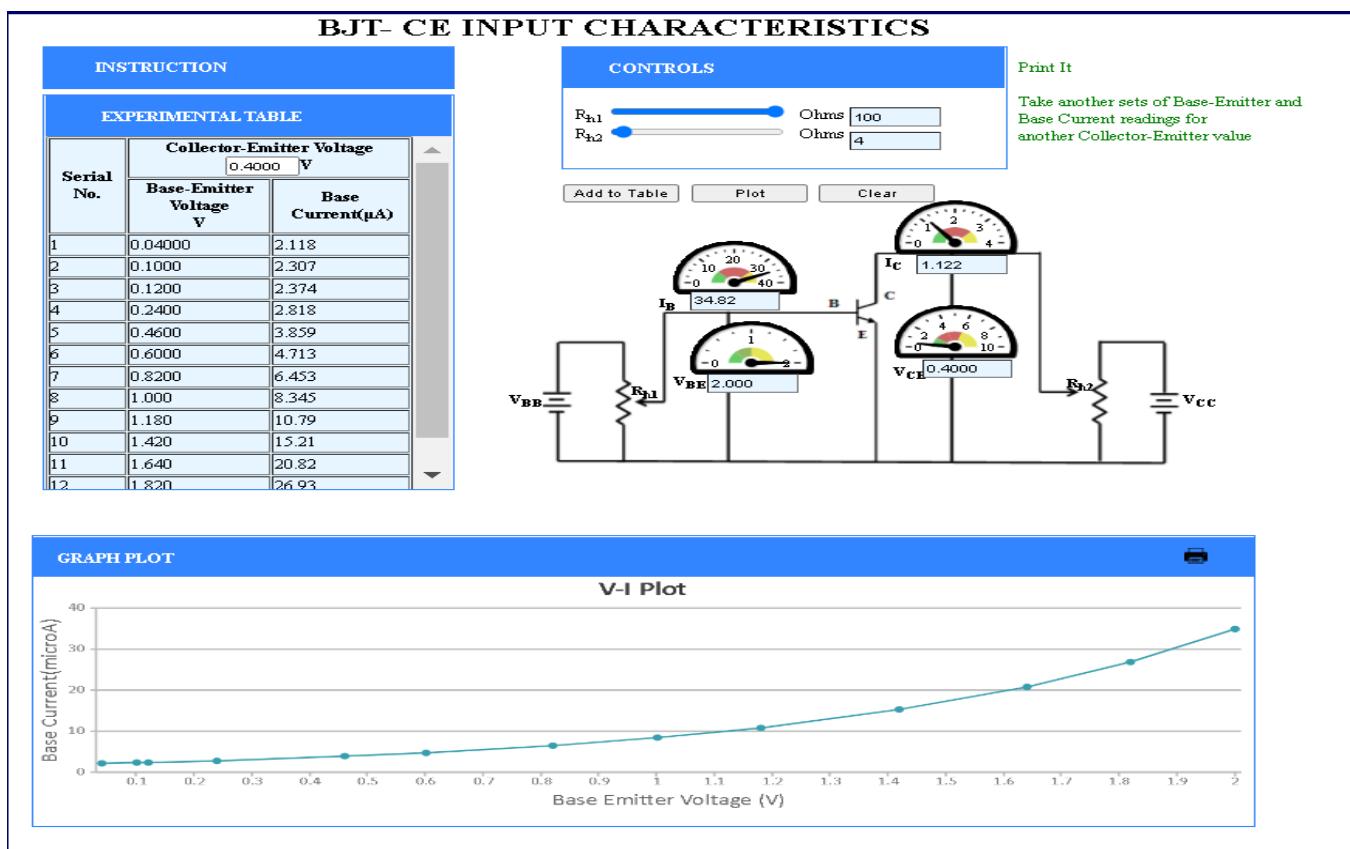
Input Characteristics Graph for CE N-P-N BJT -



Screenshots attached:

BJT- CE INPUT CHARACTERISTICS





Output Characteristics -

Table: SET 1 DATA (I_B = 12.57 μA)

Serial No.	Base-Current 12.57 μA	
	Collector-Emitter Voltage V	Collector Current mA
1	0.5000	20.59
2	0.9000	31.91
3	1.100	35.67
4	1.900	42.61
5	2.500	43.96
6	3.100	44.37
7	4.000	44.53
8	5.500	44.55
9	6.100	44.56
10	6.800	44.56
11	7.600	44.56
12	8.600	44.56
13	9.400	44.56
14	10.00	44.56

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Table: SET 2 DATA (I_B = 20.43 μA)

Serial No.	Base-Current 20.43 μA	
	Collector-Emitter Voltage V	Collector Current mA
1	0.3000	26.90
2	0.7000	55.80
3	1.000	70.31
4	1.400	81.74
5	2.000	89.00
6	3.200	92.02
7	3.900	92.25
8	6.000	92.32
9	7.000	92.32
10	8.100	92.32
11	9.100	92.32
12	10.00	92.32

Table: SET 3 DATA (I_B = 23.56 μA)

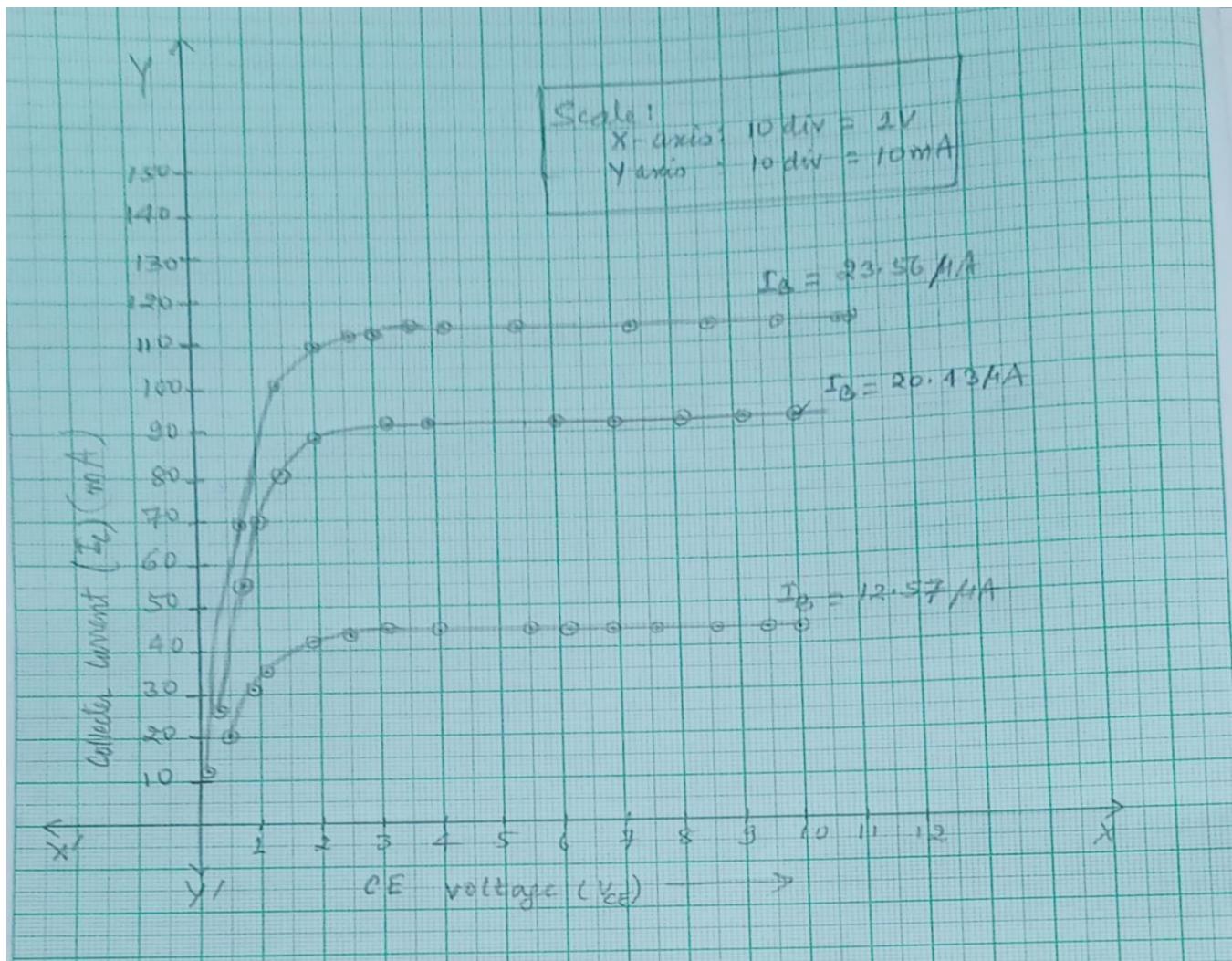
Serial No.	Base-Current 23.56 μA	
	Collector-Emitter Voltage V	Collector Current mA
1	0.1000	11.40
2	0.7000	69.13
3	1.400	101.3
4	2.000	110.3
5	2.600	113.1
6	3.000	113.8
7	3.600	114.2
8	4.200	114.3
9	5.400	114.4
10	6.300	114.4
11	7.600	114.4
12	8.700	114.4
13	9.700	114.4
14	10.00	114.4

Output Characteristics Graph for CE N-P-N BJT -

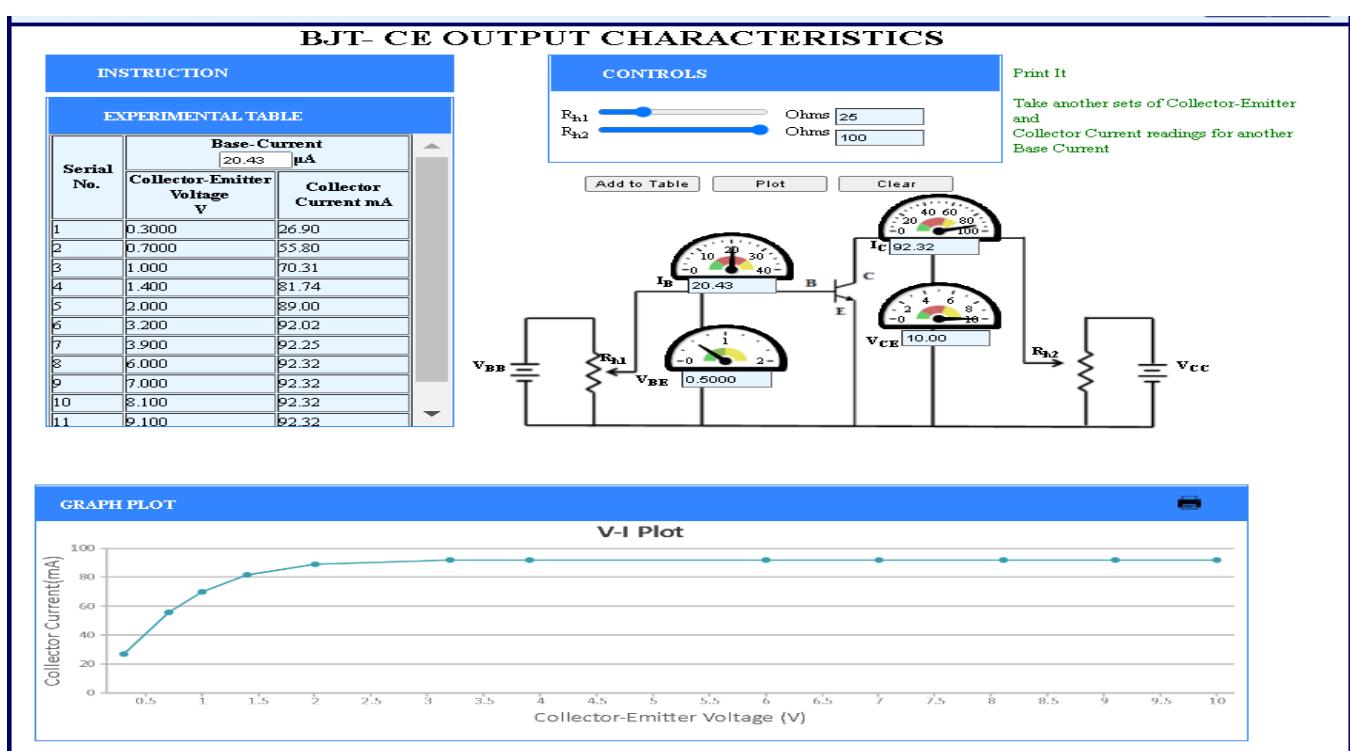
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Screenshot attached:



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CONCLUSION: The Input and Output Characteristics Curve for Common Emitter (CE) mode were studied and the graphs were plotted for different values.



Experiment – 8

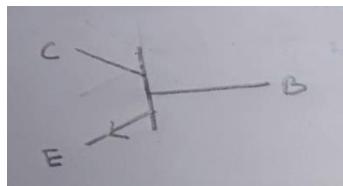
AIM:

Study the Input and Output Characteristics Curve for BJT Common Base (CB) mode.

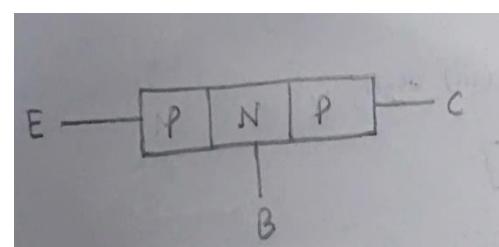
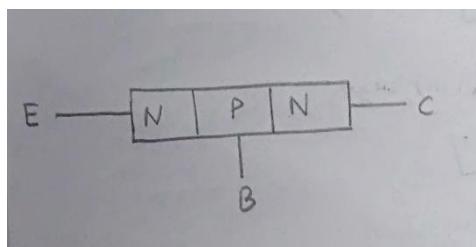
THEORY:

A Common Base Bipolar Junction Transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions. BJTs can be made either as PNP or as NPN. They have three regions and three terminals, Emitter, Base, and Collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally.

N-P-N



P-N-P



Emitter is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. Base is the middle very thin and lightly doped region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. Collector is the region with intermediate doping to the right end where charge carriers are collected. The area of this region is largest compared to emitter and base region.

Input Characteristics -

The most important characteristic of the BJT is the plot of the base current, I_B , versus the base-emitter voltage, V_{BE} , for various values of the collector-emitter voltage, V_{CE}

$$I_E = \phi(V_{BE}, V_{CB}) \quad \text{for constant } V_{CB}$$

Output Characteristics -

The most important characteristic of the BJT is the plot of the collector current, I_C , versus the collector-emitter voltage, V_{CE} for various values of the base current, I_B as shown on the circuit on the right.

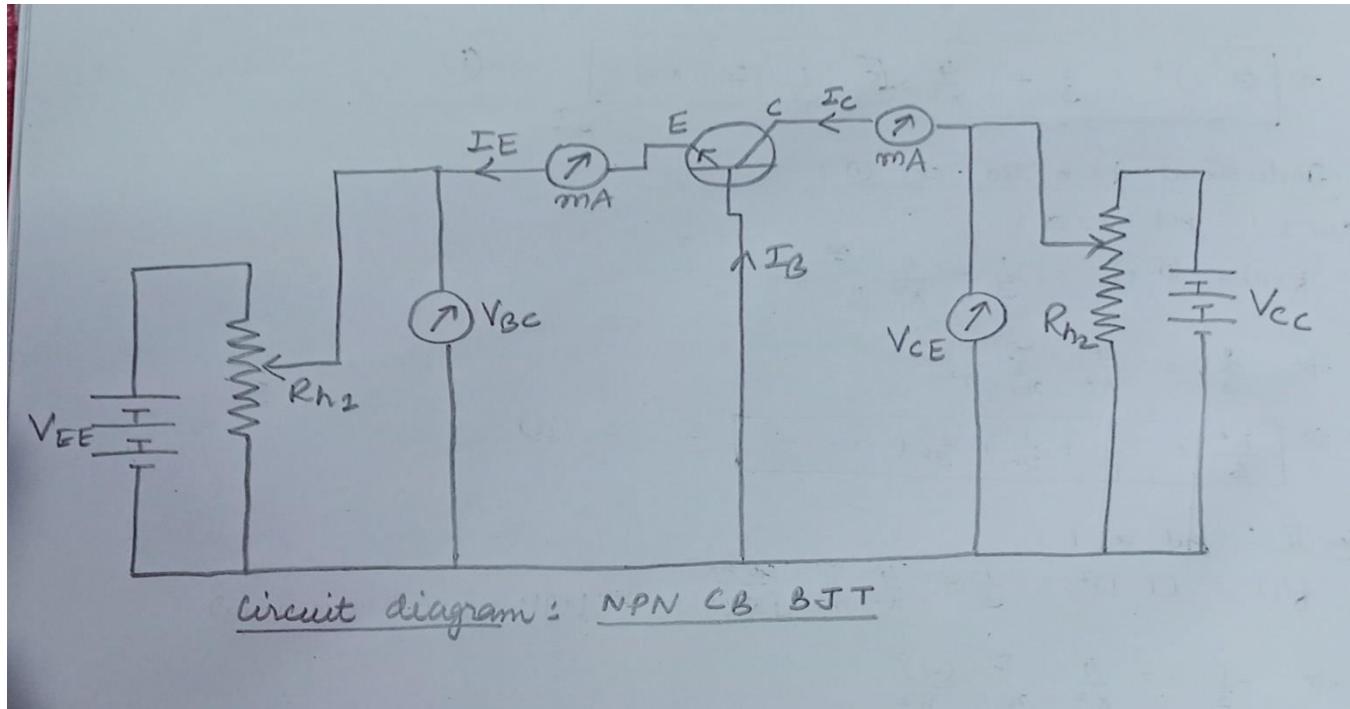
$$I_C = \phi(V_{CB}, I_E) \quad \text{for constant } I_E$$

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Circuit Diagram: NPN CB BJT connected for study of input and output characteristics



EXPERIMENTAL DATA:

Input Characteristics –

Table: SET 1 DATA ($V_{BC} = 1.00V$)

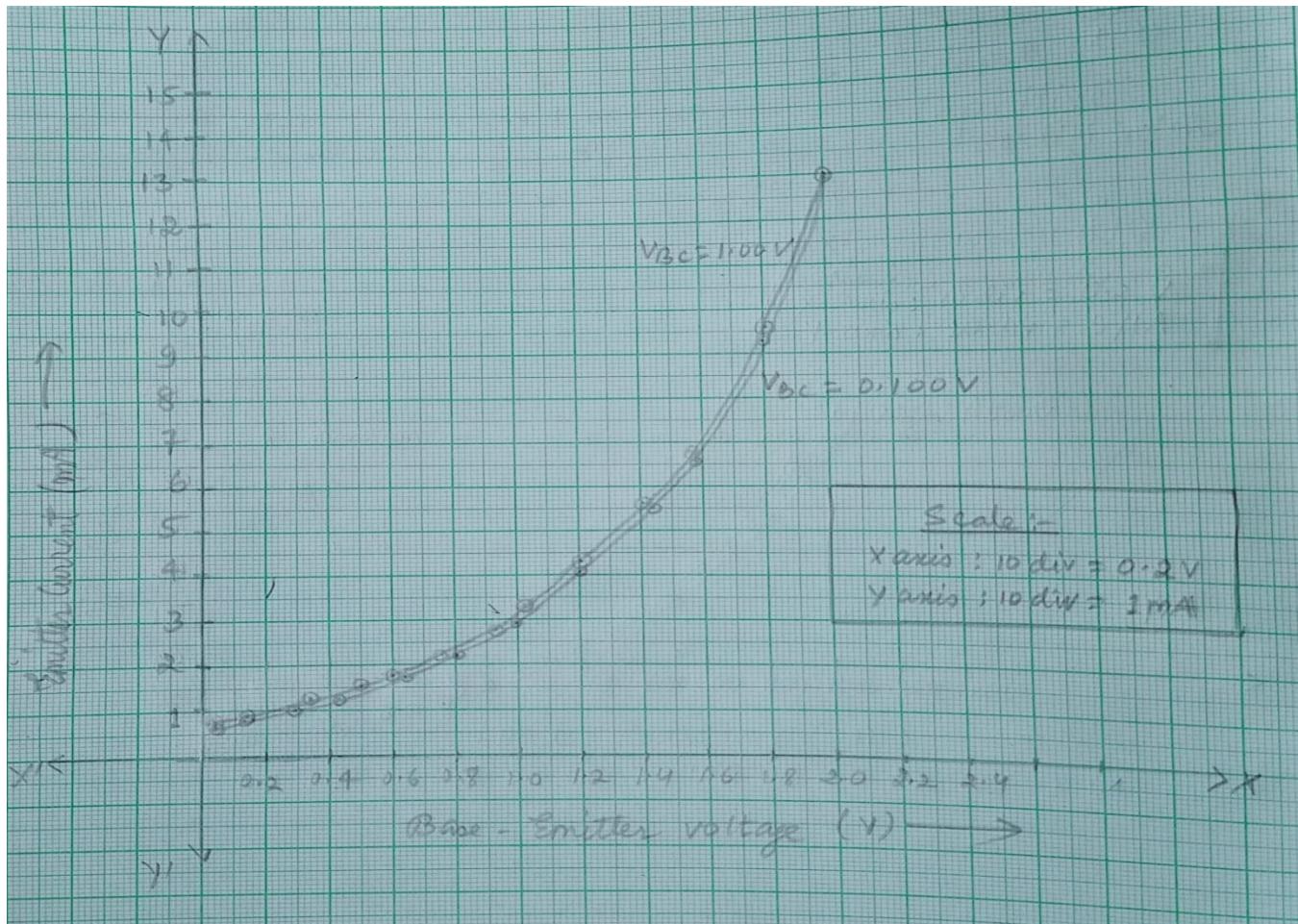
Serial No.	Base-Collector Voltage 1.00 V	
	Base-Emitter Voltage V	Emitter Current mA
1	0.02000	0.76
2	0.08000	0.82
3	0.2400	1.0
4	0.3600	1.2
5	0.5000	1.5
6	0.6000	1.7
7	0.7600	2.2
8	0.9200	2.7
9	1.080	3.4
10	1.240	4.3
11	1.420	5.6
12	1.560	6.8
13	1.800	9.6
14	2.000	13

Table: SET 2 DATA($V_{BC} = 0.100 V$)

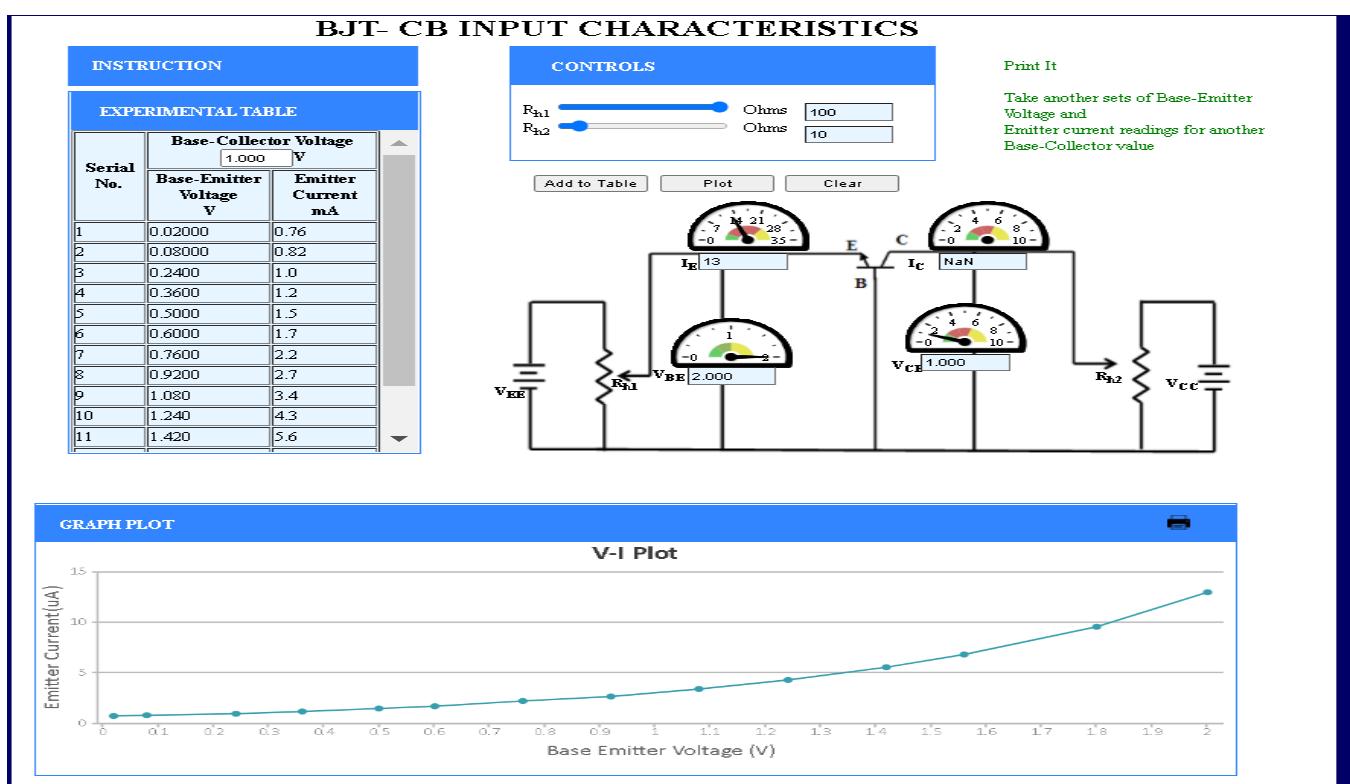
Serial No.	Base-Collector Voltage 0.10 V	
	Base-Emitter Voltage V	Emitter Current mA
1	0.02000	0.76
2	0.1200	0.87
3	0.2600	1.1
4	0.4200	1.3
5	0.6200	1.8
6	0.8000	2.3
7	0.9800	3.0
8	1.200	4.1
9	1.420	5.6
10	1.580	7.0
11	1.780	9.4
12	2.000	13

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Input Characteristics Graph for CB N-P-N BJT -



Screenshot attached:



Output Characteristics –

Table: SET 1 DATA ($I_E = 0.98 \text{ mA}$)

Serial No.	Emitter Current	
	Base-Collector Voltage V	Collector Current mA
1	-0.1000	-0.09757
2	0.1000	0.09757
3	0.4000	0.3720
4	1.000	0.7456
5	1.600	0.9023
6	2.100	0.9501
7	2.700	0.9702
8	3.300	0.9763
9	4.800	0.9789
10	5.700	0.9790
11	6.600	0.9790
12	7.500	0.9790
13	8.100	0.9790
14	9.000	0.9790
15	9.800	0.9790

Table: SET 2 DATA ($I_E = 1.5 \text{ mA}$)

Serial No.	Emitter Current	
	Base-Collector Voltage V	Collector Current mA
1	-0.4000	-0.5711
2	-0.1000	-0.1498
3	0.2000	0.2967
4	0.5000	0.6946
5	0.8000	0.9980
6	1.700	1.406
7	2.000	1.449
8	2.400	1.478
9	3.000	1.496
10	3.600	1.501
11	4.000	1.502
12	5.300	1.503
13	6.700	1.503
14	8.000	1.503
15	9.500	1.503

Table: SET 3 DATA ($I_E = 2.0 \text{ mA}$)

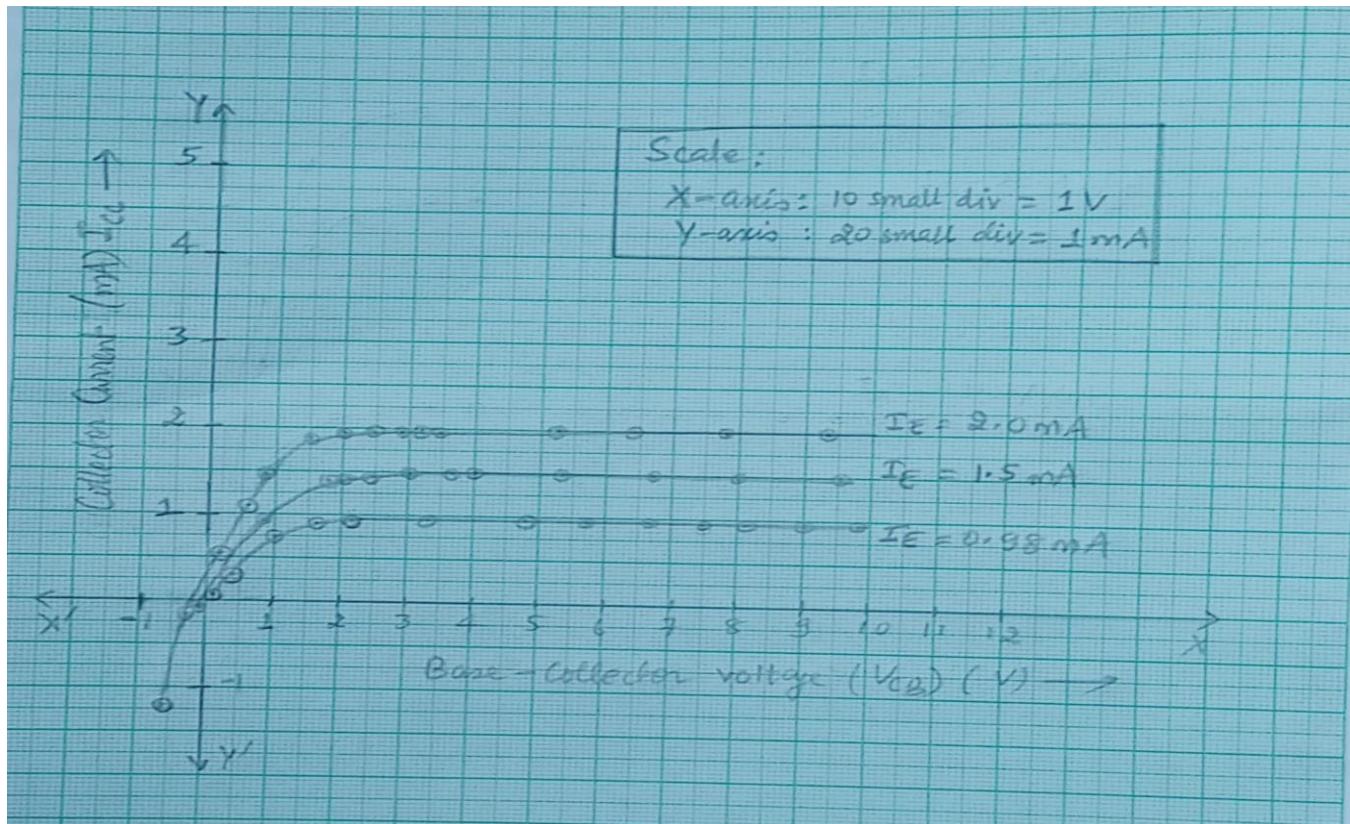
Serial No.	Emitter Current	
	Base-Collector Voltage V	Collector Current mA
1	-0.6000	-1.074
2	-0.1000	-0.1993
3	0.3000	0.5826
4	0.9000	1.433
5	1.500	1.810
6	2.000	1.928
7	2.400	1.967
8	2.600	1.978
9	2.800	1.985
10	3.200	1.993
11	3.400	1.996
12	5.300	2.000
13	6.400	2.000
14	7.700	2.000
15	9.300	2.000

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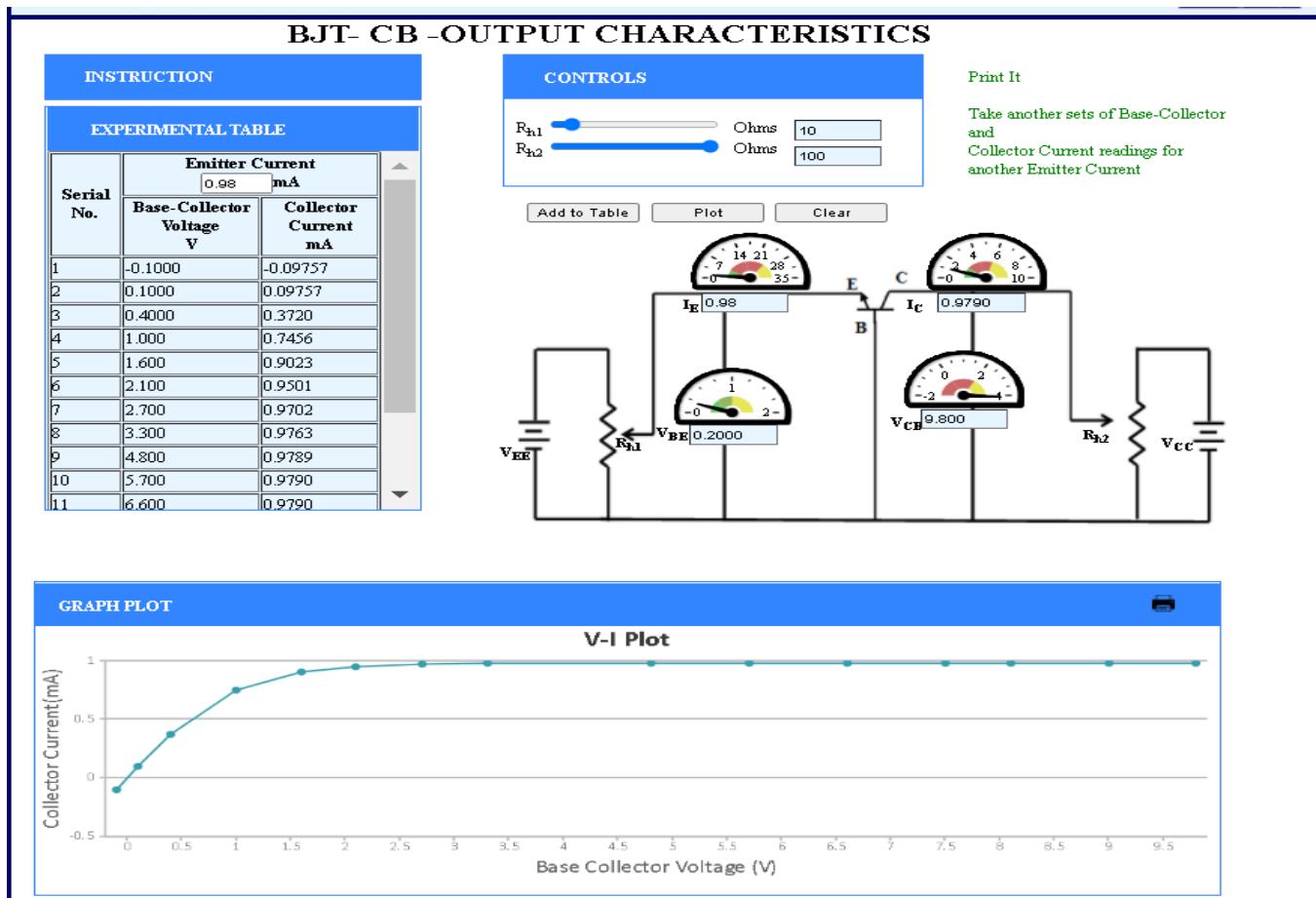
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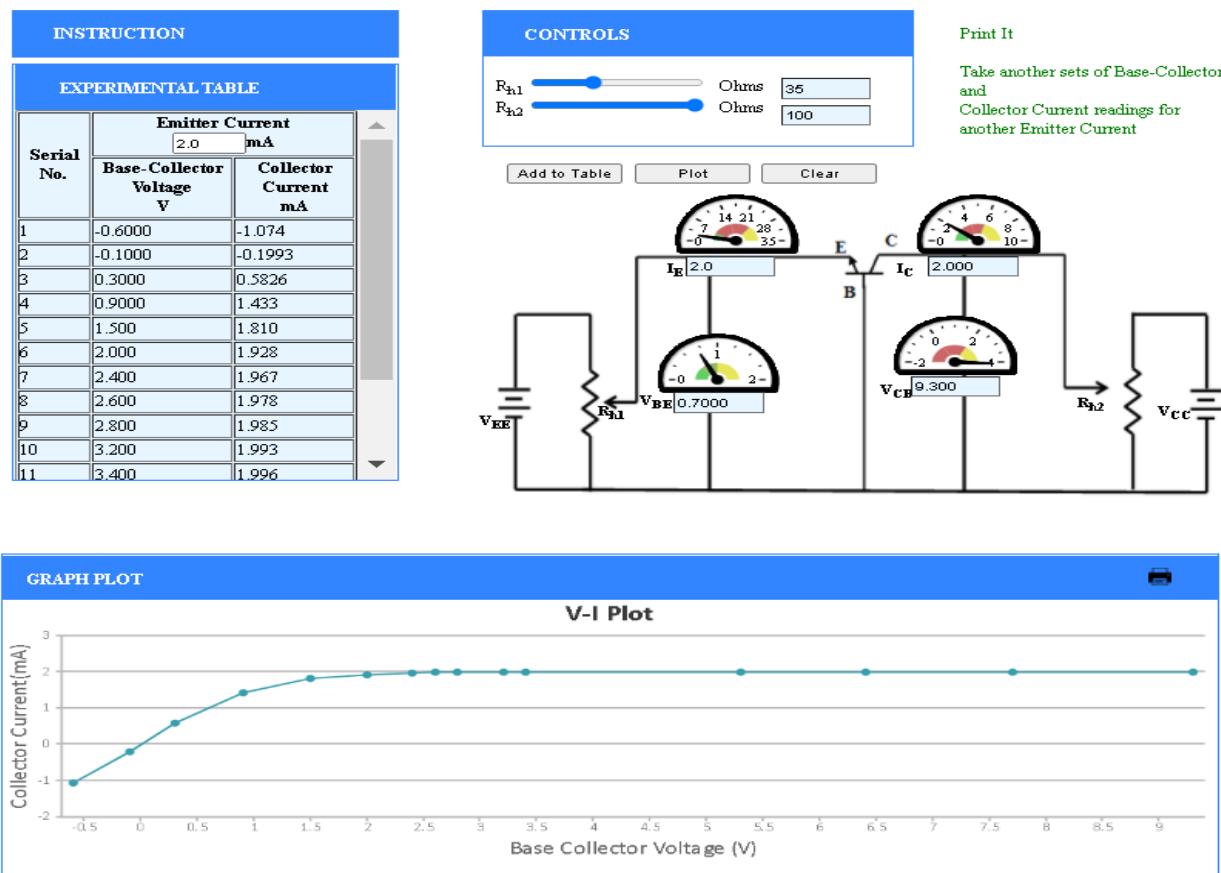
Output Characteristics Graph for CB N-P-N BJT –



Screenshot attached:



BJT- CB -OUTPUT CHARACTERISTICS



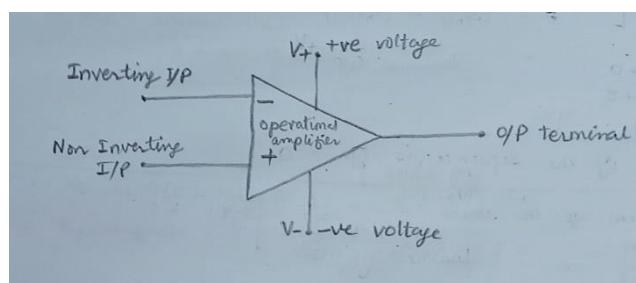
CONCLUSION: The Input and Output Characteristics Curve for Common Base (CB) mode BJT were studied and the graphs were plotted.



Experiment - 9:

Aim:- Study of Op-Amp circuits: Inverting and Non-Inverting amplifiers.

Theory:- Operational Amplifier commonly known as Op-Amp is a linear electronic device having three terminals, two high impedance input and one output terminal. Op-Amp can perform multiple function when attached to different feedback combinations like resistive, capacitive or both. Generally it is used as voltage amplifier and the output voltage of the Op-Amp is the difference between the voltages at its two input terminals. Op-Amp shows some properties that make it an ideal amplifier, its open loop gain and input impedance is infinite (i.e. practically very high), Output impedance and offset voltage is zero(i.e., practically very low) and bandwidth is infinite(i.e. practically limited to frequency where its gain become unity)



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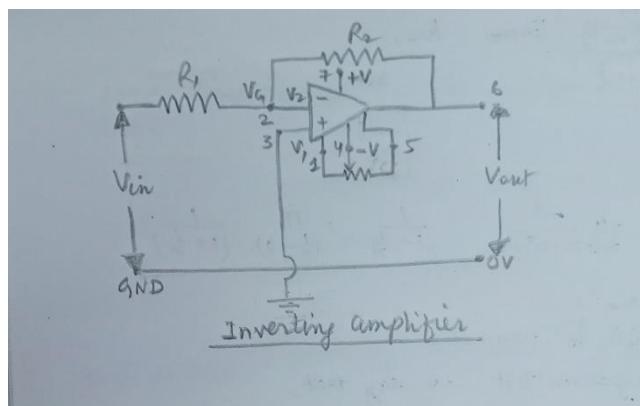
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Invering Op-Amp:-

The open loop gain(A_o) of the Op-Amp is very high which makes it very unstable, so to make it stable with a controllable gain, a feedback is applied through some external resistor(R_F) from its output to inverting input terminal(i.e., also known as negative feedback) resulting in reduced gain(closed loop gain, A_v). So the voltage at inverting terminal is now the sum of the actual input and feedback voltages, and to separate both a input resistor (R_I) is introduced in the circuit. The non-Inverting terminal of the Op-Amp is grounded, and the inverting terminal behaves like a virtual ground as the junction of the input and feedback signal are at the same potential.

$$\text{The close loop } (A_{CL}) \text{ is given by: } A_d = \frac{V_{Out}}{V_{In}} = -\frac{R_F}{R_I}$$

$$\text{Output Voltage } (V_{Out}) \text{ is given by: } V_{Out} = -\frac{R_F}{R_I} \times V_{In}$$

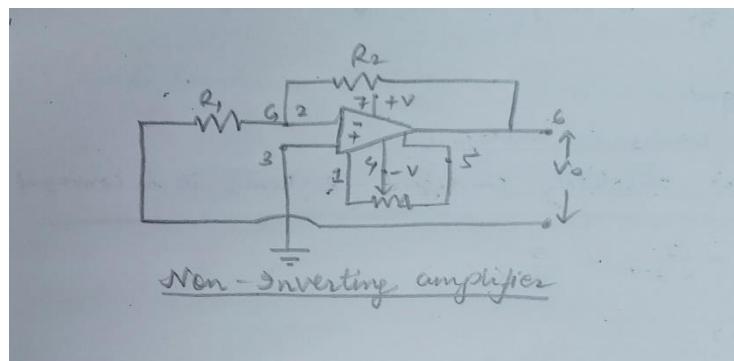


Non-Invering Op-Amp:-

In this configuration of Op-amp the input signal is directly fed to the non-inverting terminal resulting in a positive gain and output voltage in phase with input as compared to inverting Op-amp where the gain is negative and output voltage is out of phase with input, and to stabilize the circuit a negative feedback is applied through a resistor (R_F) and the inverting terminal is grounded with an input resistor (R_2). This inverting Op-Amp like layout the at inverting terminal creates a virtual ground at the summing point make the R_F and R_2 a potential divider across inverting terminal, hence determines the gain of the circuit.

$$\text{The close loop } (A_{CL}) \text{ is given by: } A_d = \frac{V_{Out}}{V_{In}} = -\frac{R_2 + R_F}{R_2} = 1 + \frac{R_F}{R_2}$$

$$\text{Output Voltage } (V_{Out}) \text{ is given by: } V_{Out} = \left[1 + \frac{R_F}{R_2} \right] V_{In}$$



Experimental Data:

Inverting op-amp:

Table 1:

Resistance: $\boxed{1}$ K Ω

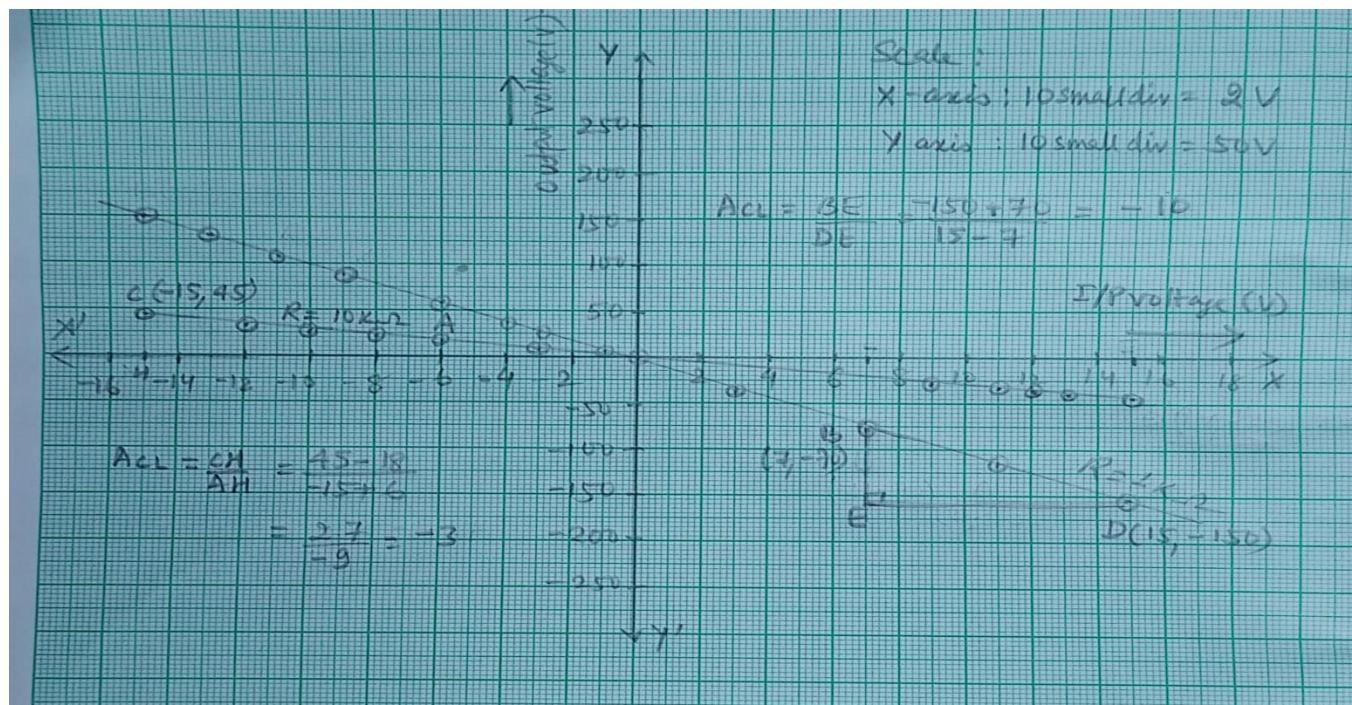
Serial No.	Input Voltage V	Output Voltage V	Current mA
1	-15	150	-1.50
2	-13	130	-1.30
3	-11	110	-1.10
4	-9	90.0	-0.900
5	-6	60.0	-0.600
6	-4	40.0	-0.400
7	-3	30.0	-0.300
8	-1	10.0	-0.100
9	2	-20.0	0.200
10	0	0.00	0.00
11	3	-30.0	0.300
12	7	-70.0	0.700
13	11	-110	1.10
14	15	-150	1.50

Table 2:

Resistance: $\boxed{10}$ K Ω

Serial No.	Input Voltage V	Output Voltage V	Current mA
1	-15	45.0	-0.0583
2	-13	39.0	-0.0505
3	-12	36.0	-0.0466
4	-10	30.0	-0.0388
5	-8	24.0	-0.0311
6	-6	18.0	-0.0233
7	-3	9.00	-0.0117
8	-1	3.00	-0.00388
9	1	-3.00	0.00388
10	3	-9.00	0.0117
11	4	-12.0	0.0155
12	7	-21.0	0.0272
13	9	-27.0	0.0350
14	11	-33.0	0.0427
15	15	-45.0	0.0583

Graphs for Inverting Opamp:



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Calculation:

Set 1: ($R = 1\text{ k}\Omega$)

Theoretical close loop gain (A_{CL}) = $-\frac{R_F}{R_1}$

$$= -\frac{10}{1}$$

$$= -10$$

Practical close loop gain (A_{CL}) = $\frac{-150 + 70}{15 - 7}$

$$= -10$$

Set 2: ($R = 10\text{ k}\Omega$)

Theoretical close loop gain (A_{CL}) = $-\frac{R_F}{R_1}$

$$= -\frac{30}{10}$$

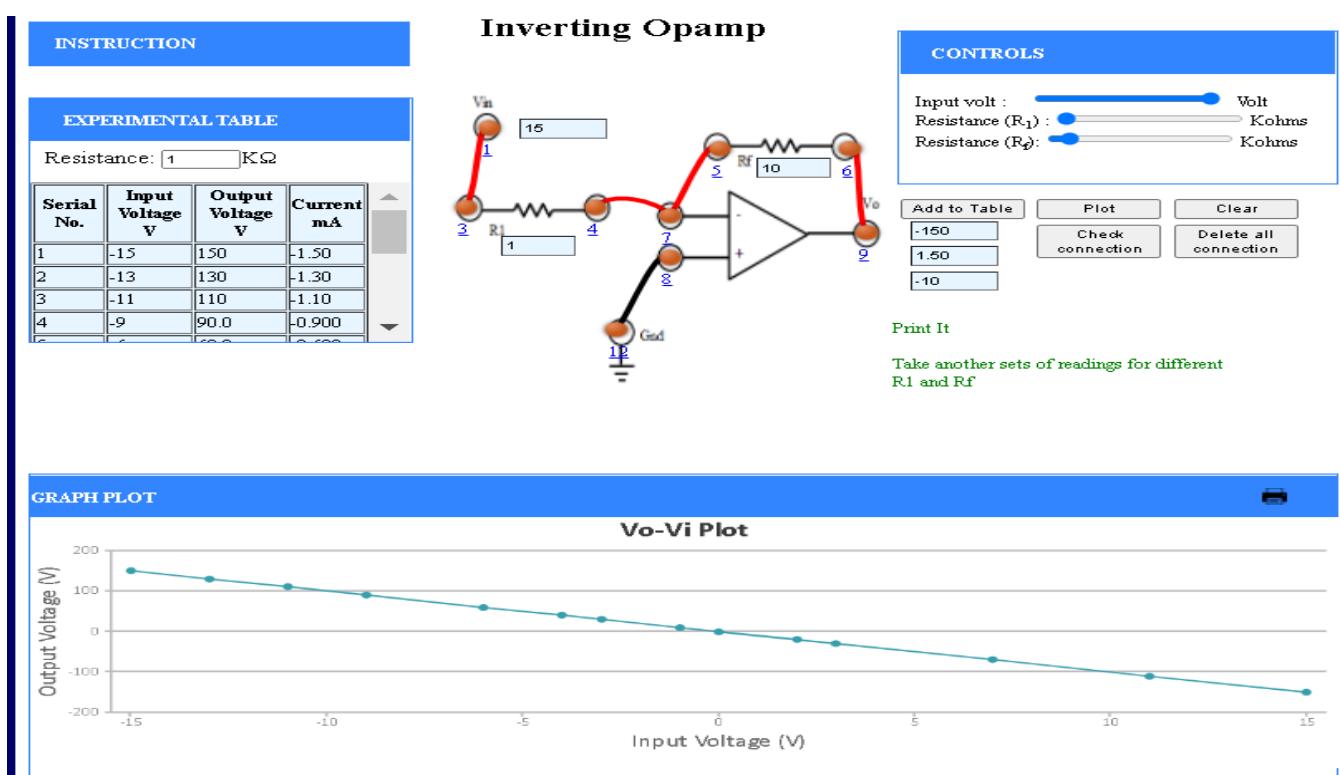
$$= -3$$

Practical close loop gain (A_{CL}) = $\frac{C_H}{A_H}$

$$= \frac{45 - 18}{-15 + 6}$$

$$= -3$$

Screenshots:



INSTRUCTION

EXPERIMENTAL TABLE

Resistance: K Ω

Serial No.	Input Voltage V	Output Voltage V	Current mA
1	-15	45.0	-0.0583
2	-13	39.0	-0.0505
3	-12	36.0	-0.0466
4	-10	30.0	-0.0388

Inverting Opamp

CONTROLS

Input volt : Volt
Resistance (R₁) : Kohms
Resistance (R_f) : Kohms

Add to Table Plot Clear

Print It
 Take another sets of readings for different R₁ and R_f

GRAPH PLOT

Vo-Vi Plot

Input Voltage (V)	Output Voltage (V)
-15	45.0
-13	39.0
-12	36.0
-10	30.0
-5	15.0
0	0.00
5	-15.0
10	-30.0
15	-45.0

Non-Inverting Op-Amp:

Table - 1:

Resistance: K Ω

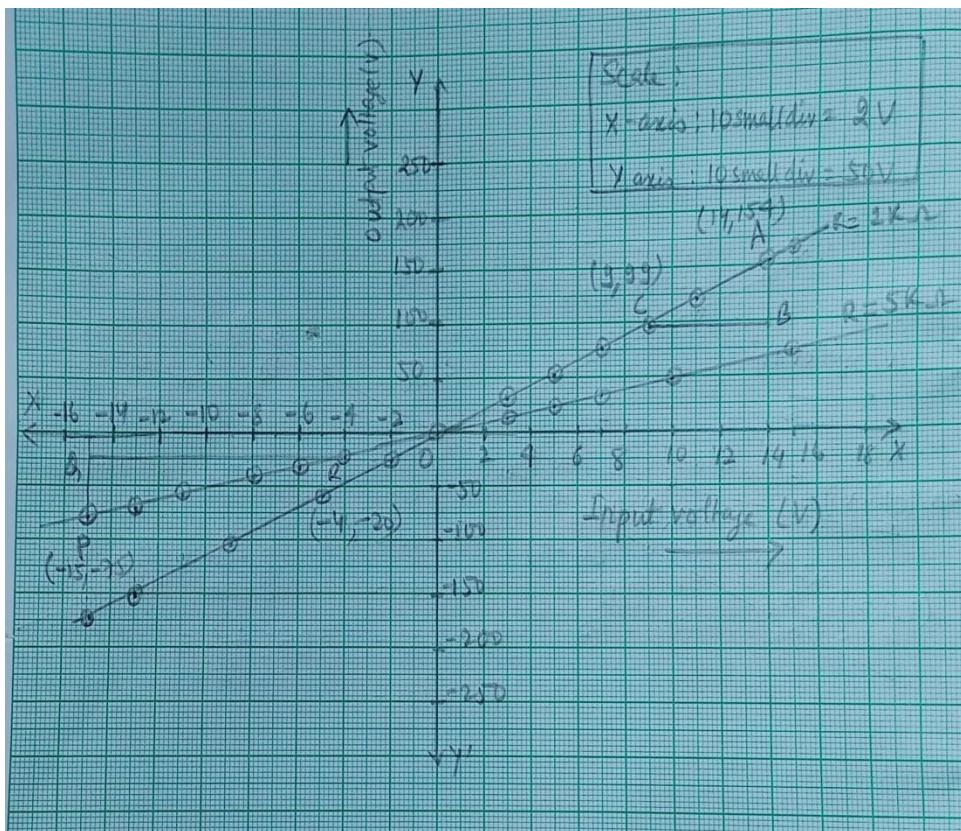
Serial No.	Input Voltage V	Output Voltage V	Current mA
1	-15	-165	-1.64
2	-13	-143	-1.42
3	-9	-99.0	-0.982
4	-5	-55.0	-0.545
5	-2	-22.0	-0.218
6	0	0.00	0.00
7	3	33.0	0.327
8	5	55.0	0.545
9	7	77.0	0.764
10	9	99.0	0.982
11	11	121	1.20
12	14	154	1.53
13	15	165	1.64

Table – 2:

Resistance: $\boxed{5}$ K Ω

Serial No.	Input Voltage V	Output Voltage V	Current mA
1	-15	-75.0	-0.173
2	-13	-65.0	-0.150
3	-11	-55.0	-0.127
4	-8	-40.0	-0.0923
5	-6	-30.0	-0.0692
6	-4	-20.0	-0.0462
7	0	0.00	0.00
8	3	15.0	0.0346
9	5	25.0	0.0577
10	7	35.0	0.0808
11	10	50.0	0.115
12	15	75.0	0.173

Graph:



Calculation:

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Set 1: $R = 1 \text{ k}\Omega$

Theoretical close loop gain (A_{CL}) = $1 + \frac{R_F}{R_1}$
 $= 1 + \frac{10}{1}$
 $= 11$

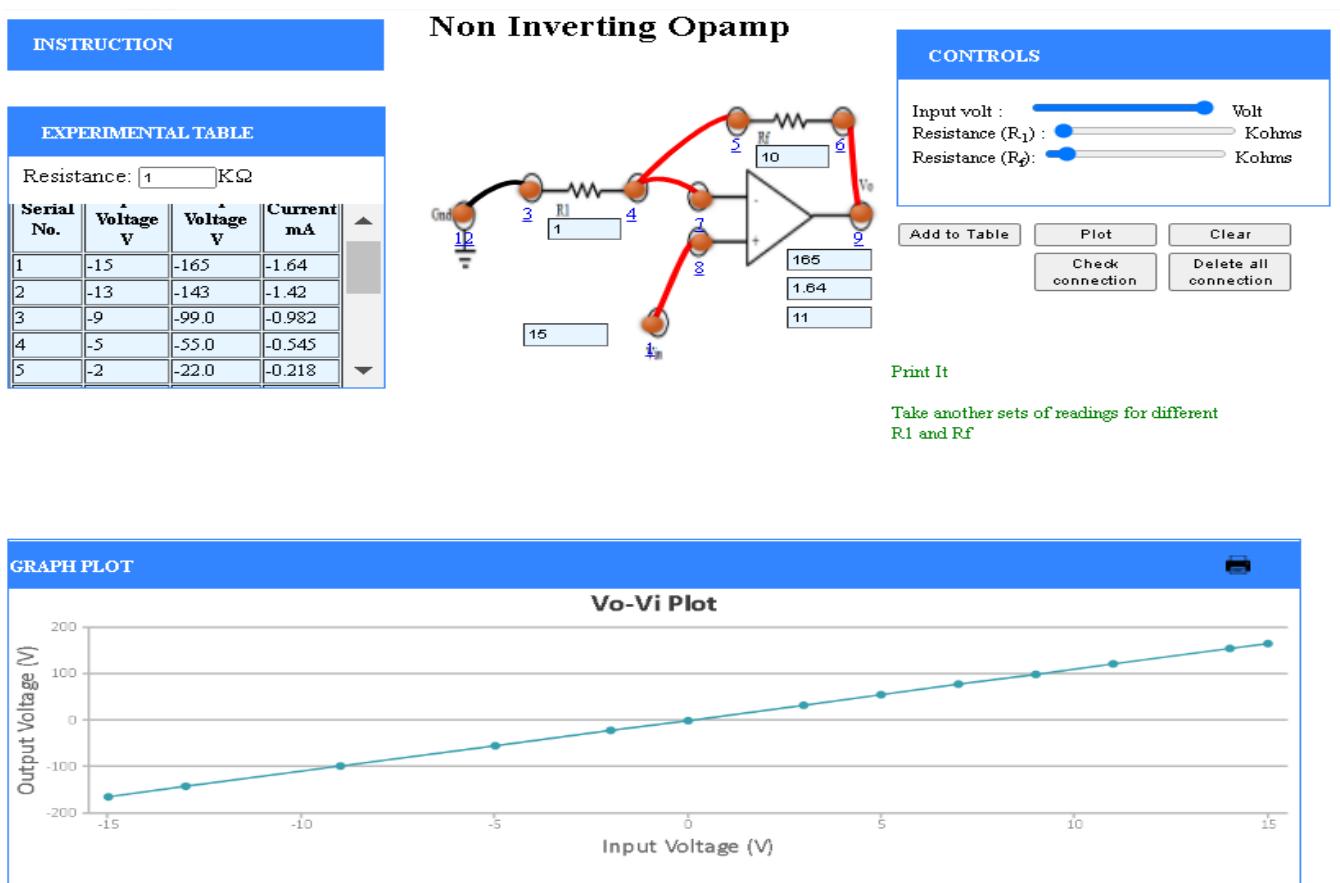
Practical close loop gain (A_{CL}) = $\frac{A_E}{B_C}$
 $= \frac{1.54 - 99}{14 - 9}$
 $= 11$

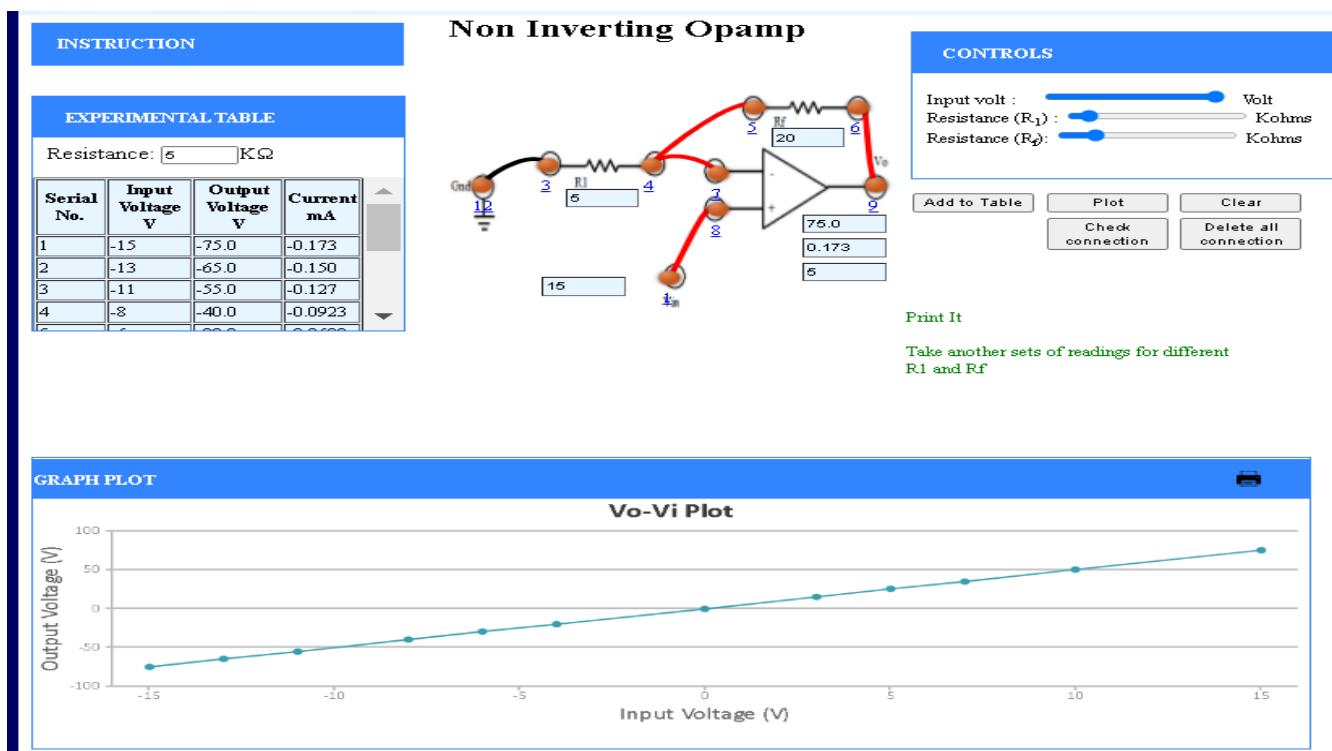
Set 2: $R = 5 \text{ k}\Omega$

Theoretical close loop gain (A_{CL}) = $1 + \frac{R_F}{R_1}$
 $= 1 + \frac{20}{5}$
 $= 5$

Practical close loop gain (A_{CL}) = $\frac{P_D}{R_D}$
 $= \frac{-75 + 20}{-15 + 4}$
 $= 5$

Screenshot attached:





Conclusion:- Thus the practical and theoretical gain values match and are equal for both the Inverting and Non-Inverting OP-Amp. The screenshots are attached below.



Experiment – 10:

Aim:-

Study of Op-Amp circuits: Integrator and Differentiator using Op-Amp.

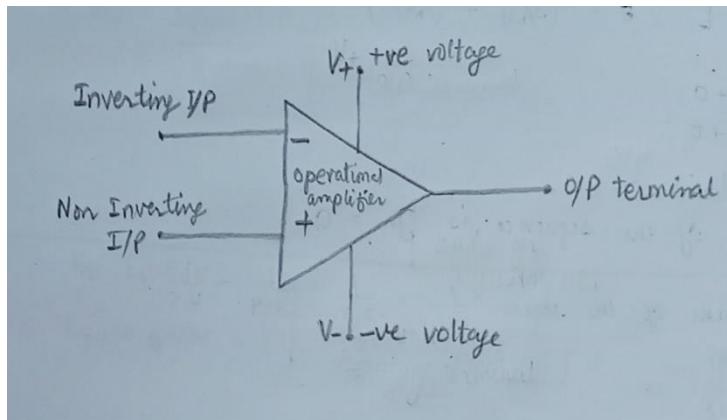
Theory:-

Operational Amplifier commonly known as Op-Amp is a linear electronic device having three terminals, two high impedance input and one output terminal. Op-Amp can perform multiple function when attached to different feedback combinations like resistive, capacitive or both. Generally it is used as voltage amplifier and the output voltage of the Op-Amp is the difference between the voltages at its two input terminals. Op-Amp shows some properties that make it an ideal amplifier, its open loop gain and input impedance is infinite (i.e. practically very high), Output impedance and offset voltage is zero(i.e., practically very low) and bandwidth is infinite(i.e. practically limited to frequency where its gain become unity)

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The Integrator:-

It is a circuit designed with Op-Amp in such a way that it performs the mathematical Integration operation, its output is proportional to the amplitude and time duration of the input applied. The integrator circuit layout is same as a inverting amplifier but the feedback resistor is replaced by a capacitor which make the circuit frequency dependent. In this case the circuit is derived by the time duration of input applied which results in the charging and discharging of the capacitor. Initially when the voltage is applied to integrator the uncharged capacitor allows maximum current to pass through it and no current flows through the Op-Amp due to the presence of virtual ground, the capacitor starts to charge at the rate of RC time constant and its impedance starts to increase with time and a potential difference is develops across the capacitor resulting in charging current to decrease. This results in the ratio of capacitor's impedance and input resistance increasing causing a linearly increasing ramp output voltage that continues to increase until the capacitor becomes fully charged.

The Differentiator:-

In the differentiator circuit the input is connected to the inverting output of the Op-Amp through a capacitor (C) and a negative feedback is provided to the inverting input terminal through a resistor (R_F), which is same as an integrator circuit with feedback capacitor and input resistor being replaced with each other. Here the circuit performs a mathematical differentiation operation, and the output is the first derivative of the input signal, 180° out of phase and amplified with a factor $R_F \times C$. The capacitor on the input allows only the AC component and restrict the DC, at low frequency the reactance of capacitor is very high causing a low gain and high frequency vice versa but at high frequency the circuit becomes unstable.

Experimental Data:-

To analyse the output signals, the following graphs were plotted and for the following experiment the values of capacitor and resistor etc. used are:

Integrator using Op-Amp:

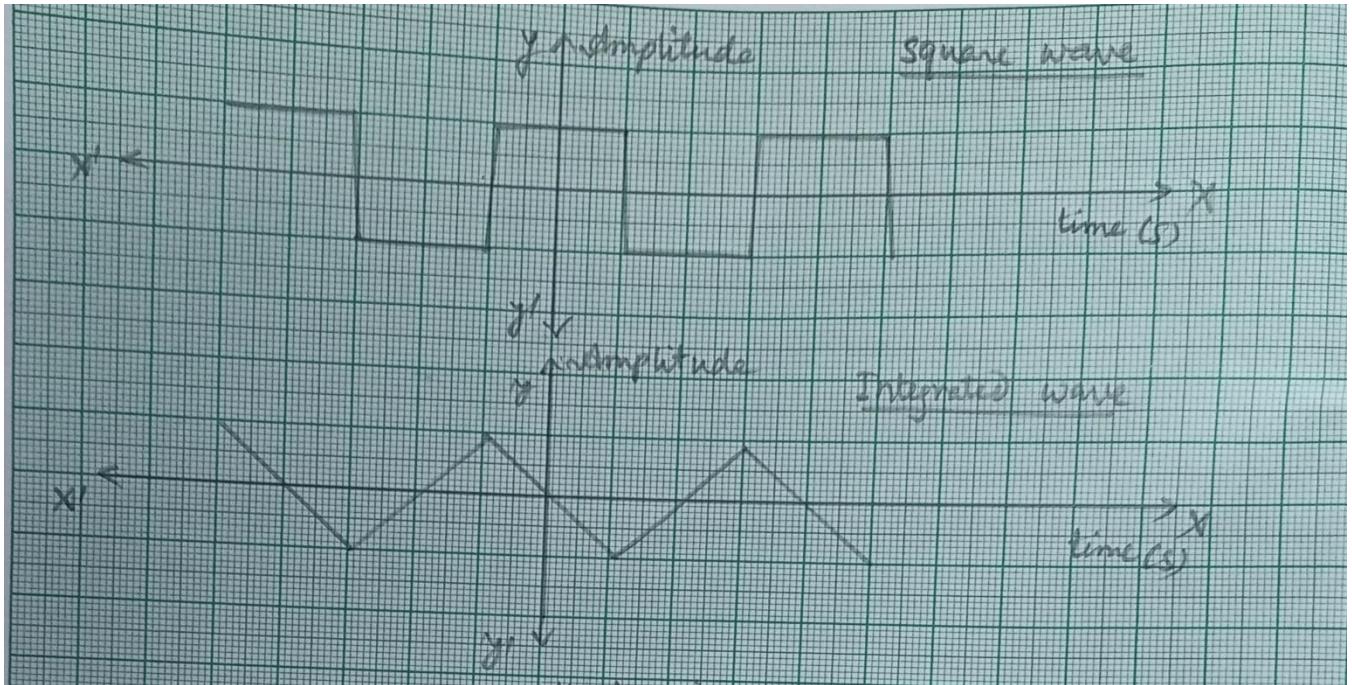
- • Capacitor: $0.1 \mu F$
- Resistance: $10 K\Omega$
- Frequency: 2.5 KHz

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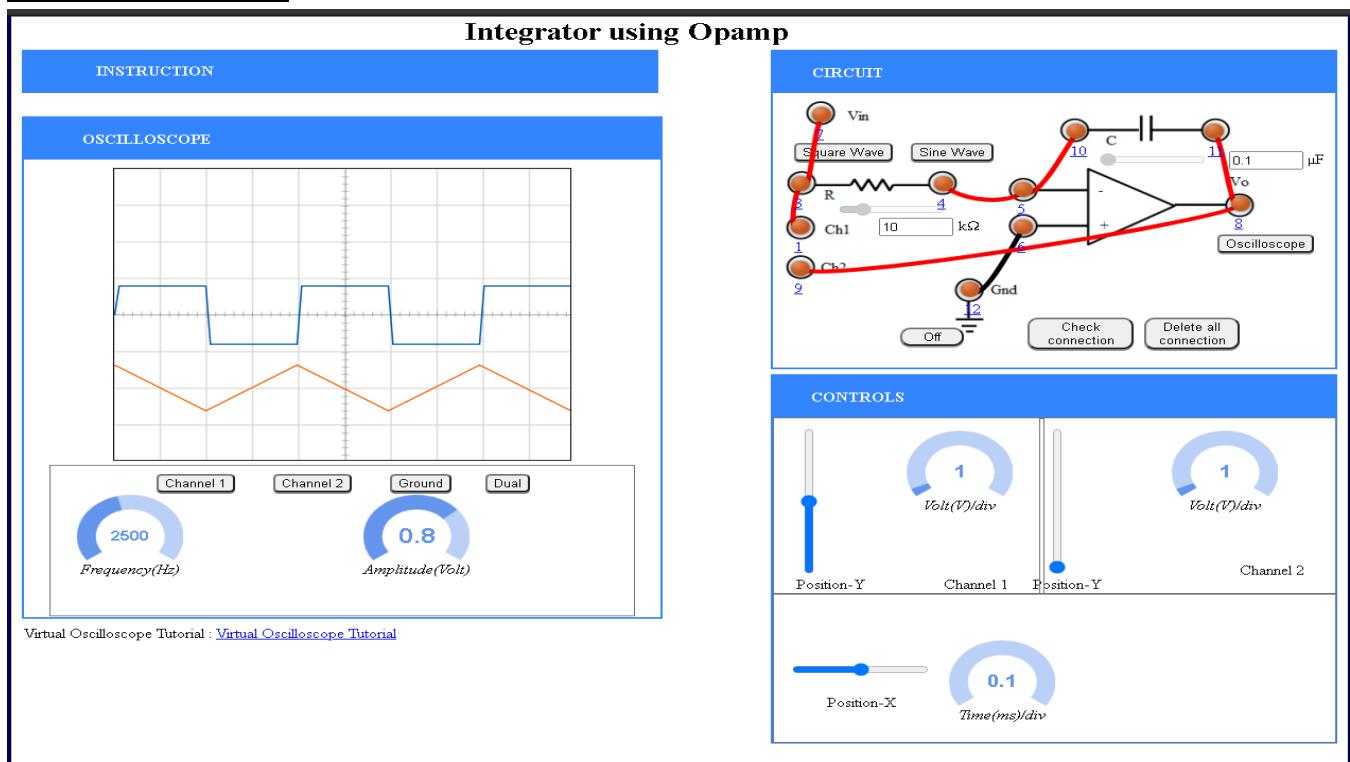
- Amplitude: 0.8V

Integrator using Op-Amp Square Wave Plot:

Graph:



Screenshot attached:



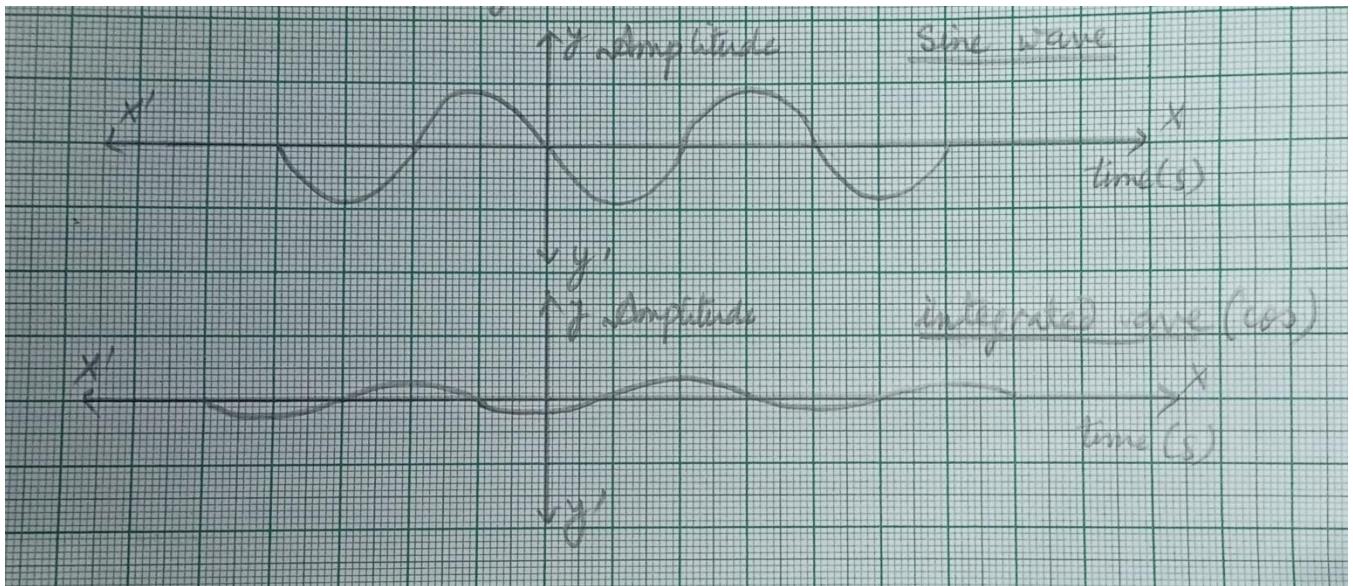
Integrator using Op-Amp Sine Wave Plot:

Graph:

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Screenshot attached:

Integrator using Opamp

The screenshot displays a virtual oscilloscope interface for simulating an integrator circuit using an operational amplifier (Opamp).

CIRCUIT: The circuit diagram shows an opamp configured as an integrator. The non-inverting input (pin 3) is connected to ground through a resistor (R). The inverting input (pin 5) is connected to the output (Vo) through a capacitor (C). The input voltage (Vin) is applied between pin 1 and pin 3. A feedback resistor (10 kΩ) is connected between pin 5 and ground. The output (Vo) is connected to an oscilloscope. The circuit includes a switch for selecting 'Square Wave' or 'Sine Wave' input, and a switch for selecting 'Ch1' or 'Ch2' output. There are also 'Check connection' and 'Delete all connection' buttons.

CONTROLS: The controls section includes:

- Frequency (Hz): 3000
- Amplitude (Volt): 1.5
- Channel 1: Position-Y (5.4 Volt/V/div)
- Channel 2: Position-Y (1.4 Volt/V/div)
- Position-X (0.1 Time(ms)/div)

OSCILLOSCOPE: The oscilloscope screen shows two traces. The top trace is a sine wave (blue), and the bottom trace is its integral (orange). The x-axis represents time, and the y-axis represents amplitude.

Virtual Oscilloscope Tutorial : [Virtual Oscilloscope Tutorial](#)

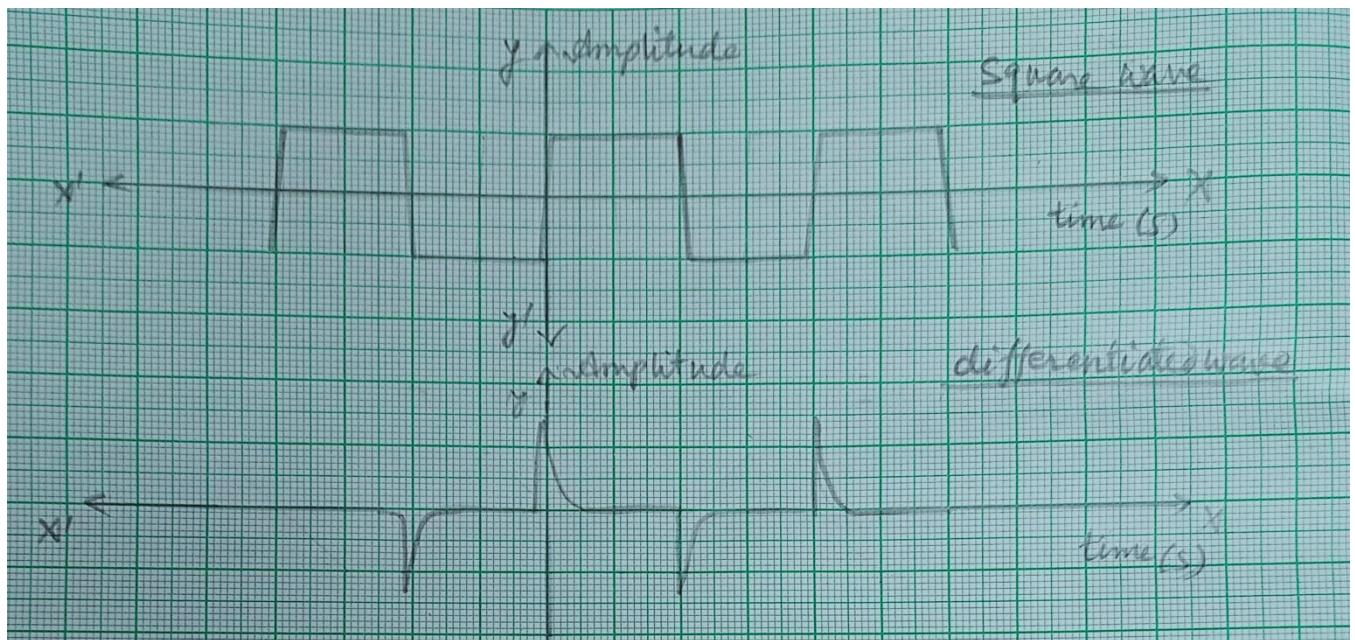
Differentiator using Op-Amp-

- Capacitor: $0.1 \mu\text{F}$
- Resistance: $1 \text{ K}\Omega$
- Frequency: 2 KHz
- Amplitude: 0.7V

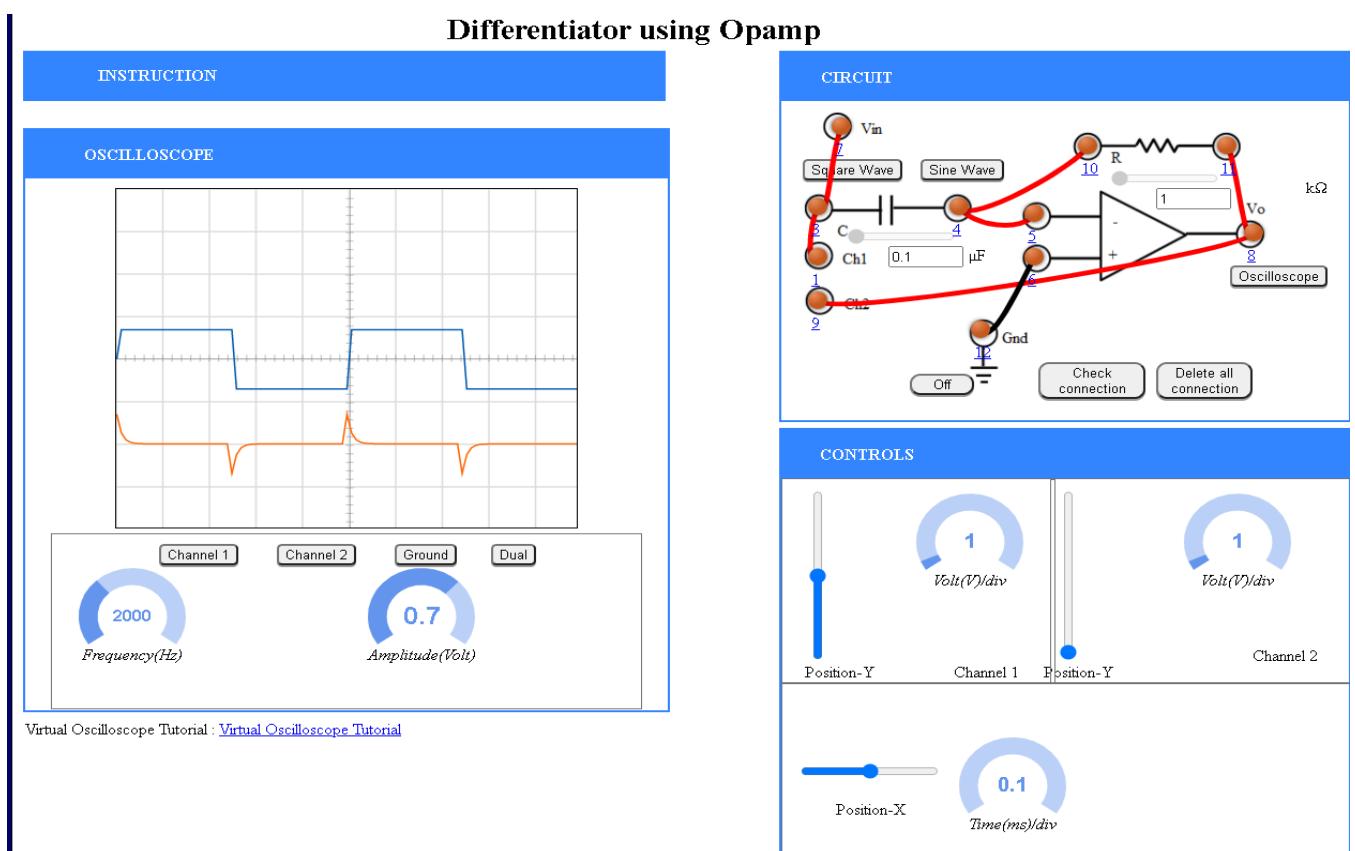
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Differentiator using Op-Amp Square Wave Plot:

Graph:



Screenshot attached:



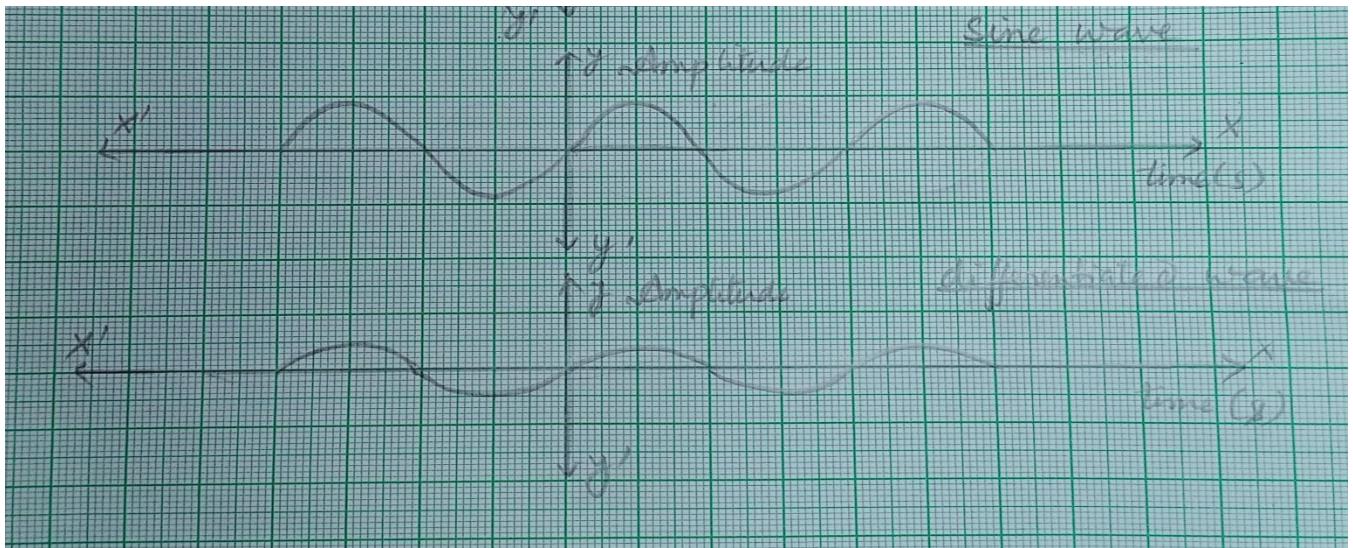
Differentiator using Op-Amp Sine Wave Plot:

Graph:

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Screenshot attached:

Differentiator using Opamp

INSTRUCTION

OSCILLOSCOPE

The oscilloscope screen displays two signals. Channel 1 shows a sine wave with a frequency of 2000 Hz and an amplitude of 0.7 Volts. Channel 2 shows the derivative of the sine wave, which is a square wave oscillating between -0.7 and 0.7 Volts.

Frequency(Hz) 2000
Amplitude(Volt) 0.7

Virtual Oscilloscope Tutorial : [Virtual Oscilloscope Tutorial](#)

CIRCUIT

The circuit diagram shows a non-inverting differentiator configuration using an operational amplifier (op-amp). The input signal V_{in} is connected to the non-inverting input ($+$) through a capacitor C (0.1 μ F). The inverting input ($-$) is grounded. The output V_o is connected to the inverting input through a resistor R (1 k Ω). A feedback resistor $10k\Omega$ is connected from the output V_o back to the non-inverting input. The op-amp is connected with a gain of 1. There are buttons for 'Square Wave' and 'Sine Wave' at the input, and 'Check connection' and 'Delete all connection' at the bottom.

Off Check connection Delete all connection

CONTROLS

Position-Y Channel 1 Position-Y Channel 2

1 Volt(V)/div 1 Volt(V)/div

Position-X 0.1 Time(ms)/div

Conclusion:- Thus, we learnt the differentiator & integrator using operational amplifiers..

Digital Electronics Practical:

Aim of the Experiment:

The principal objective of this experiment is to fully understand the function and use of logic gates such as 7400(quad 2-input NAND gates), 7402(quad 2-input NOR gates), 7404(Hex inverter), 7408(quad 2-input AND gates) and 7432(quad 2-input OR gates) and also to learn-

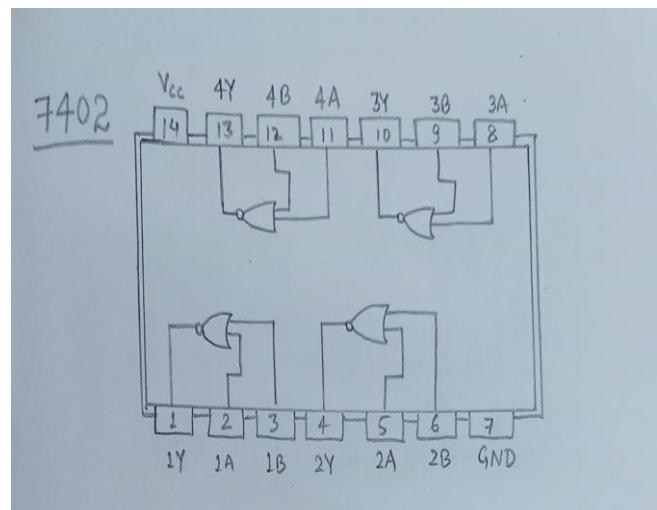
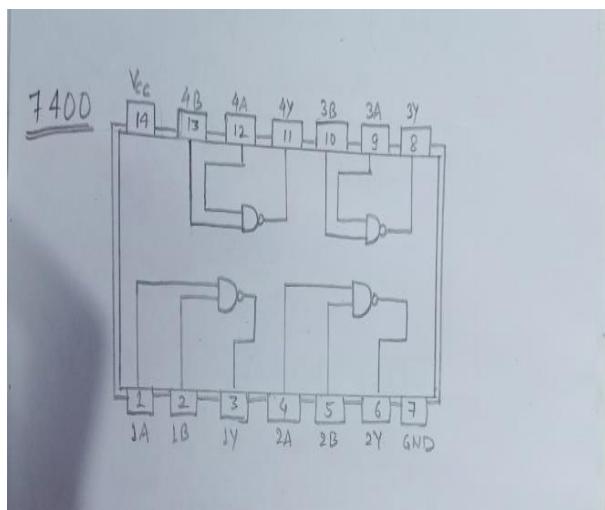
1. To analyse logic gates
2. To express Boolean expression using logic gates
3. To check equivalence of two Boolean expressions using logic gates
4. To check equivalence of two logic circuits consisting of multiple gates

THEORY:

Analysis of Logic gates using 7400(quad 2-input NAND gates), 7402(quad 2-input NOR gates), 7404(HEX inverter), 7408(quad 2-input AND gates), 7432(quad 2-input OR gates).

NOTE - We consider output as 0 for 0 V – 0.6 V & 1 for 4.2 V – 5.0 V

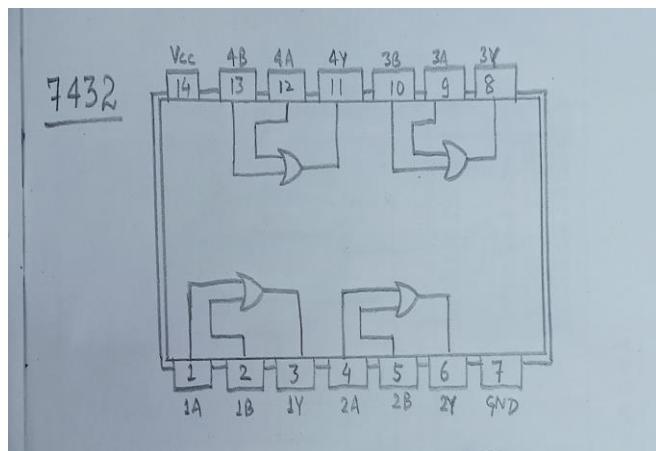
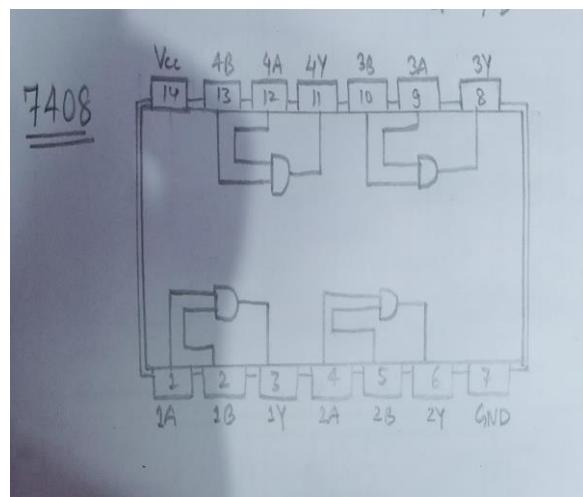
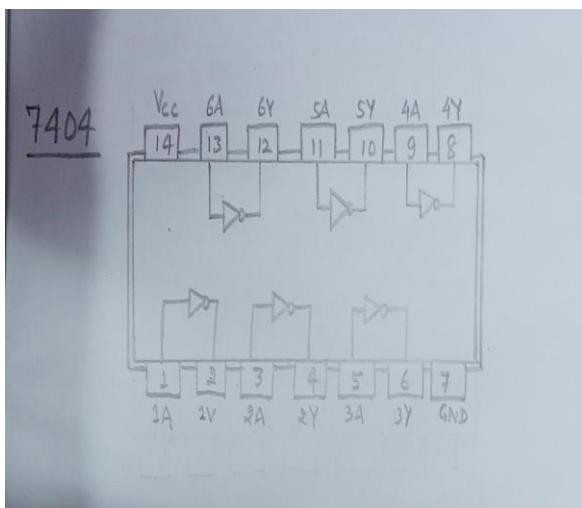
Diagrams of each chip are shown below:



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Components:

1. 7400(quad 2-input NAND gates)
2. 7402(quad 2-input NOR gates)
3. 7404(HEX inverter)
4. 7408(quad 2-input AND gates)
5. 7432(quad 2-input OR gates)
6. LED's
7. Switches
8. Cells
9. Resistors
10. Connecting Wires

Experimental Data:

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Experiment – 1:

TRURTH TABLE FOR $AB + A'C + BC = AB + A'C$

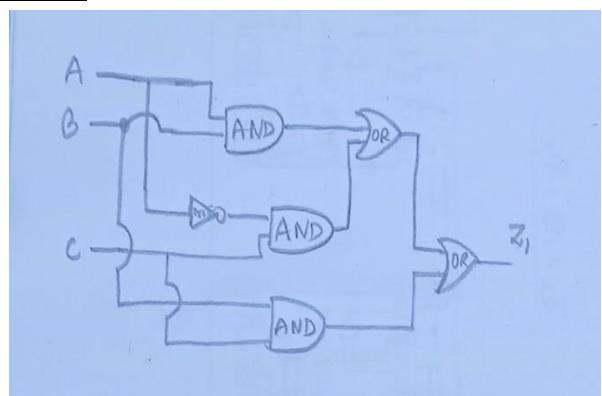
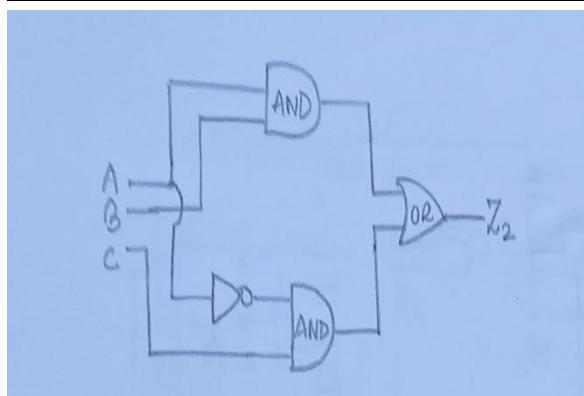
A	B	C	$AB + A'C + BC$	ON / OFF	$AB + A'C$	ON / OFF
0	0	0	0	OFF	0	OFF
0	0	1	1	ON	1	ON
0	1	0	0	OFF	0	OFF
0	1	1	1	ON	1	ON
1	0	0	0	OFF	0	OFF
1	0	1	0	OFF	0	OFF
1	1	0	1	ON	1	ON
1	1	1	1	ON	1	ON

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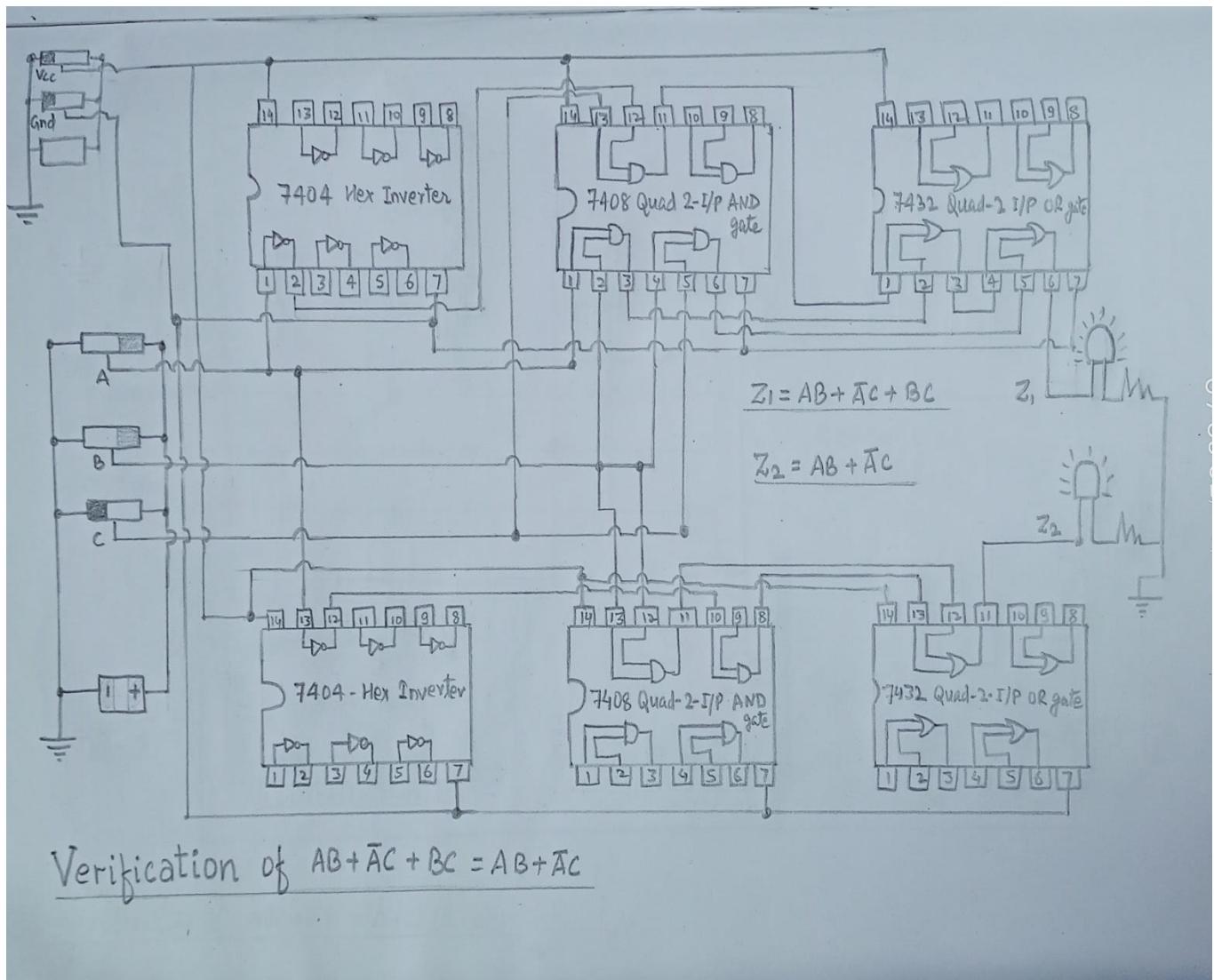
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LOGIC CIRCUIT OF THE ABOVE EXPRESSION -



Circuit Diagram –



Experiment – 2:

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TRUTH TABLE FOR AB + A'C = (A +B)(A' + C)

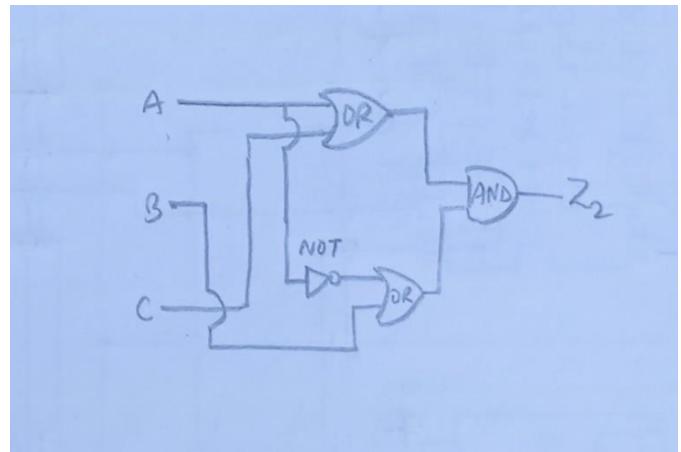
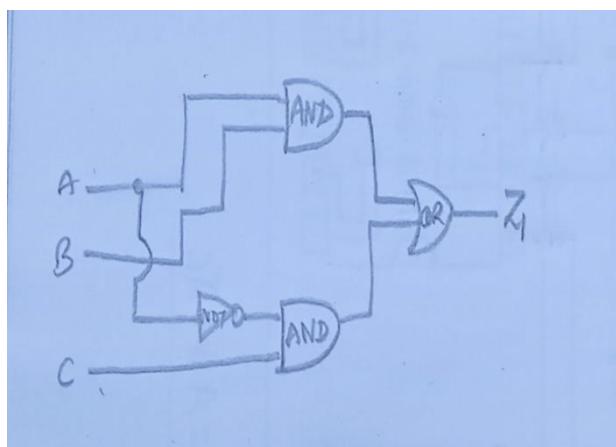
A	B	C	AB + A'C	ON / OFF	(A + B)(A' + C)	ON / OFF
0	0	0	0	OFF	0	OFF
0	0	1	1	ON	1	ON
0	1	0	0	OFF	0	OFF
0	1	1	1	ON	1	ON
1	0	0	0	OFF	0	OFF
1	0	1	0	OFF	0	OFF
1	1	0	1	ON	1	ON
1	1	1	1	ON	1	ON

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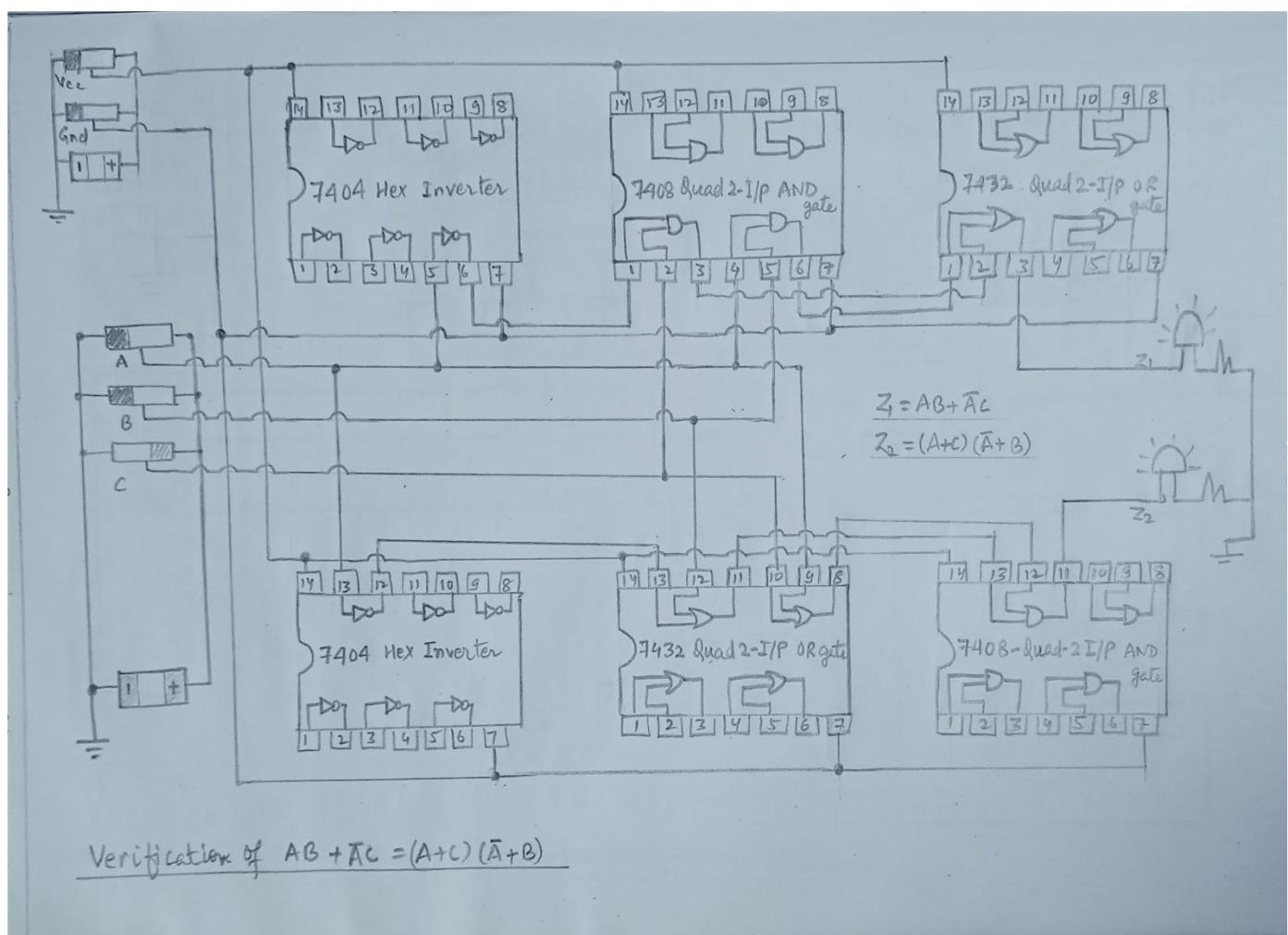
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LOGIC CIRCUIT OF THE ABOVE EXPRESSION –



CIRCUIT DIAGRAM –



Experiment – 3:

Verify the equivalence of AND-OR and NAND-NAND Structure:

TRUTH TABLE FOR AB + CD = (A'B' + C'D')'

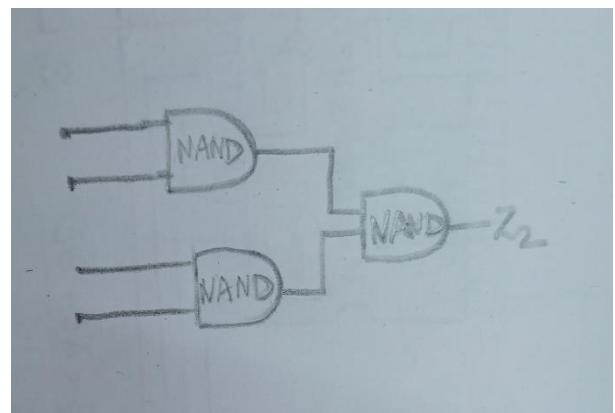
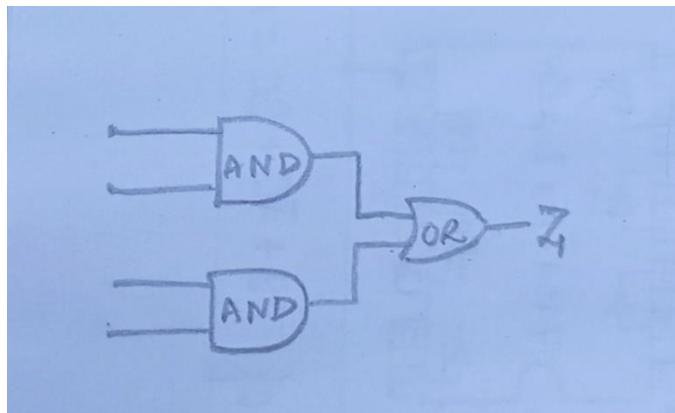
	B	C	D	AB + CD	ON/OFF	(A'B' + C'D')'	ON/OFF
0	0	0	0	0	OFF	0	OFF
0	0	0	1	0	OFF	0	OFF
0	0	1	0	0	OFF	0	OFF
0	0	1	1	1	ON	1	ON
0	1	0	0	0	OFF	0	OFF
0	1	0	1	0	OFF	0	OFF
0	1	1	0	0	OFF	0	OFF
0	1	1	1	1	ON	1	ON
1	0	0	0	0	OFF	0	OFF
1	0	0	1	0	OFF	0	OFF
1	0	1	0	0	OFF	0	OFF
1	0	1	1	1	ON	1	ON
1	1	0	0	1	ON	1	ON
1	1	0	1	1	ON	1	ON
1	1	1	0	1	ON	1	ON
1	1	1	1	1	ON	1	ON

LOGIC CIRCUIT OF THE ABOVE EXPRESSION –

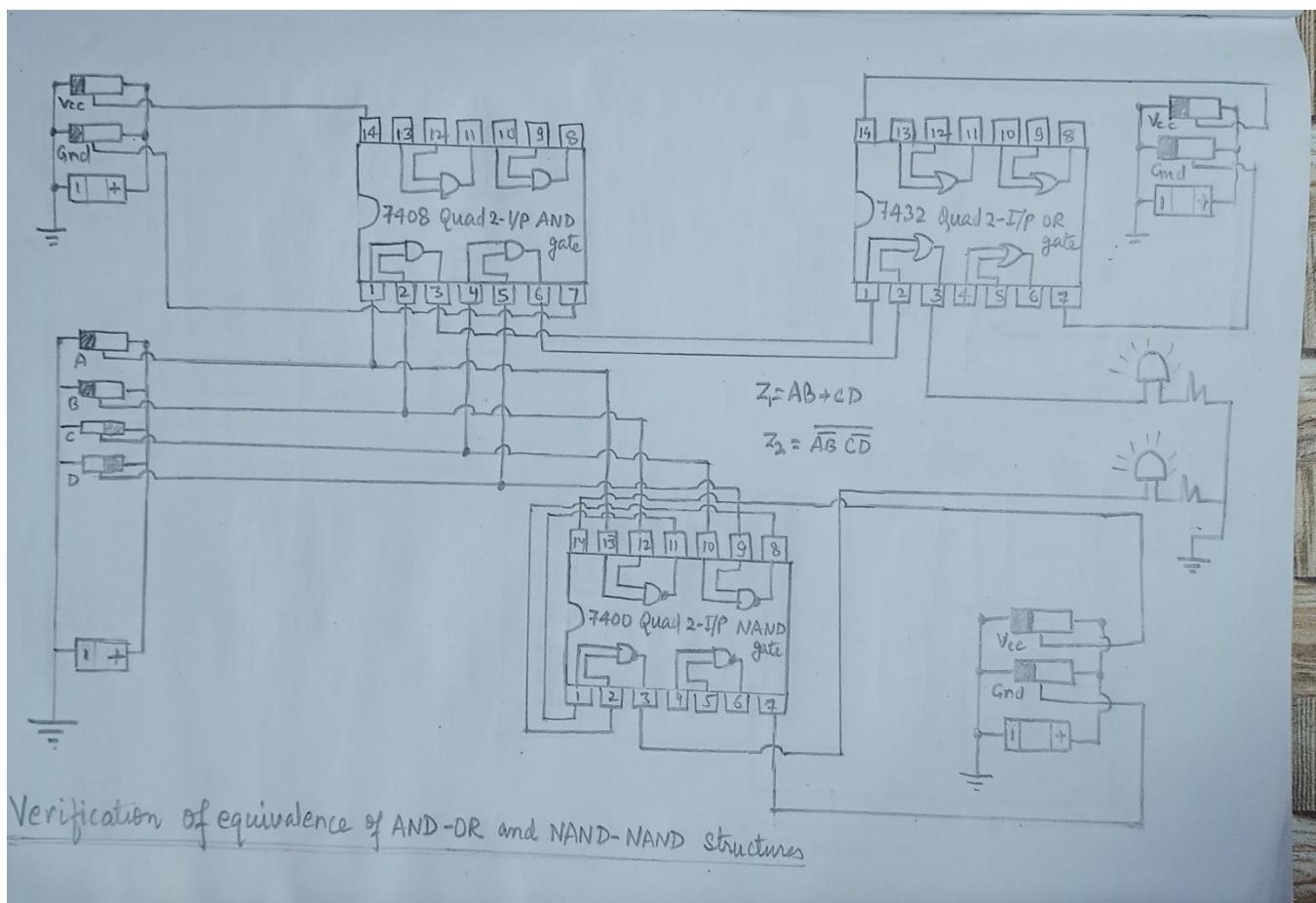
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CIRCUIT DIAGRAM –



Experiment – 4:

Verify the equivalence of AND-OR and NAND-NAND Structure:

TRUTH TABLE FOR $(A + B)(C + D) = ((A' + B')(C' + D'))'$

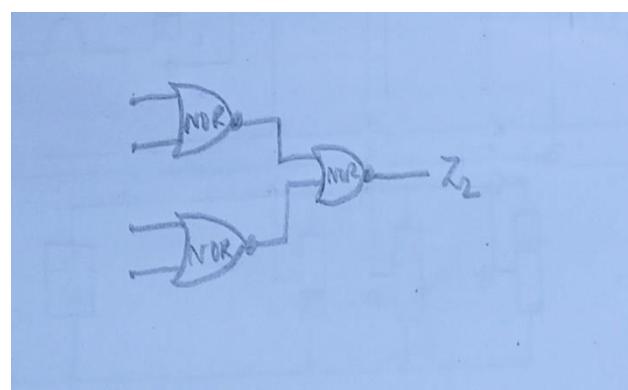
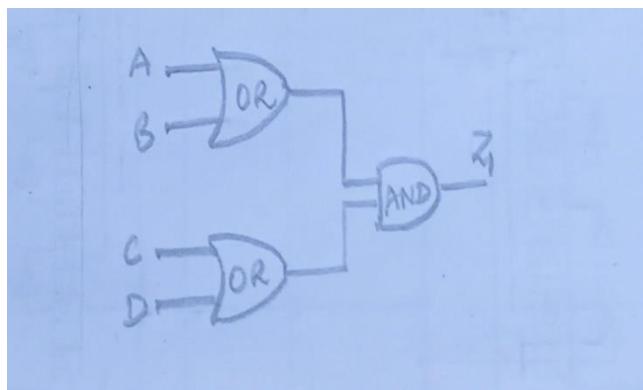
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A	B	C	D	$(A+B)(C+D)$	ON/OFF	$((A'+B')(C'+D'))'$	ON/OFF
0	0	0	0	0	OFF	0	OFF
0	0	0	1	0	OFF	0	OFF
0	0	1	0	0	OFF	0	OFF
0	0	1	1	0	OFF	0	OFF
0	1	0	0	0	OFF	0	OFF
0	1	0	1	1	ON	1	ON
0	1	1	0	1	ON	1	ON
0	1	1	1	1	ON	1	ON
1	0	0	0	0	OFF	0	OFF
1	0	0	1	1	ON	1	ON
1	0	1	0	1	ON	1	ON
1	0	1	1	1	ON	1	ON
1	1	0	0	0	OFF	0	OFF
1	1	0	1	1	ON	1	ON
1	1	1	0	1	ON	1	ON
1	1	1	1	1	ON	1	ON

LOGIC CIRCUIT OF THE ABOVE EXPRESSION –

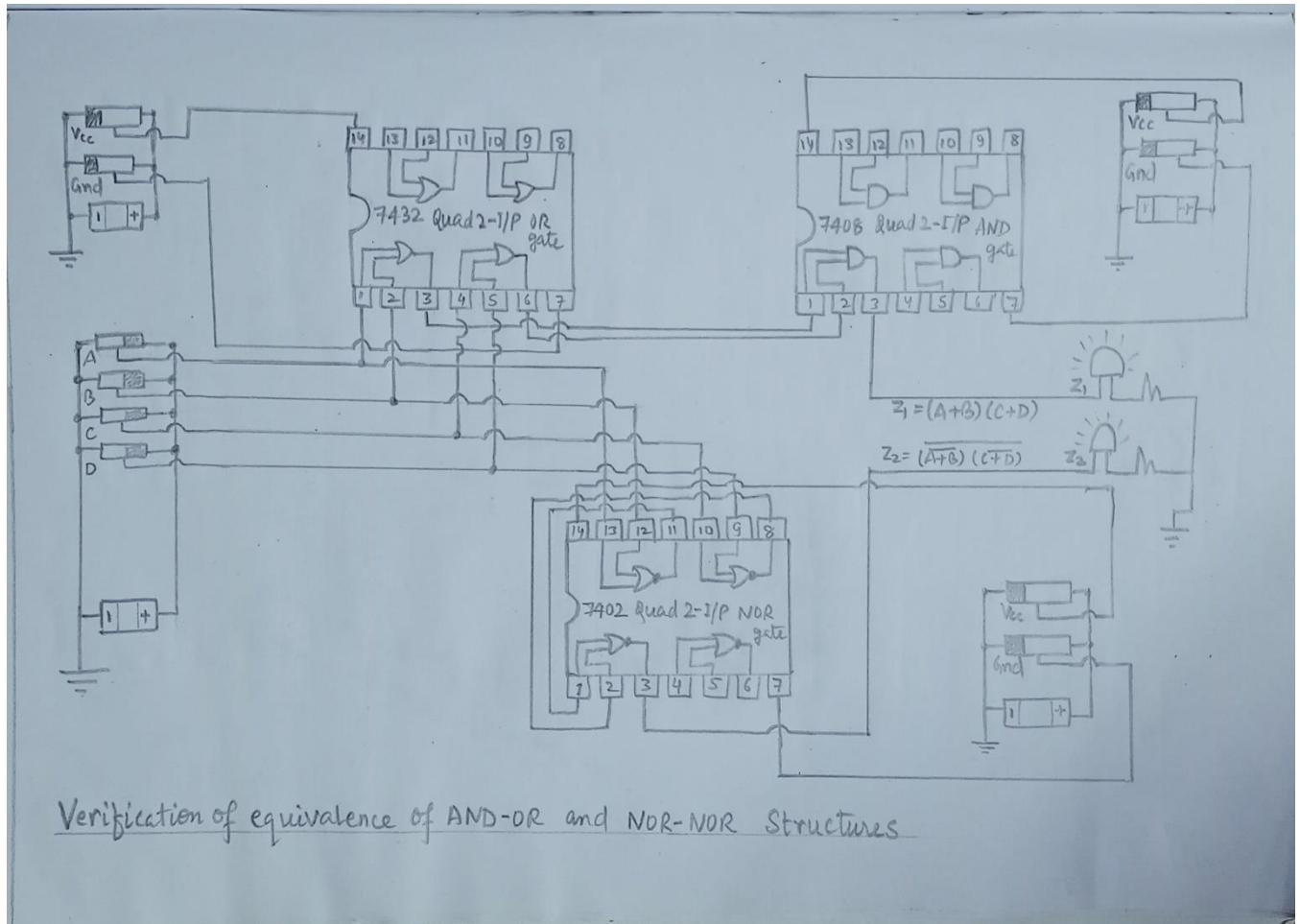


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CIRCUIT DIAGRAM –



CONCLUSION: We understood the principal objective of this experiment with the use of logic gates 7400(quad 2-input NAND gates), 7402(quad 2-input NOR gates), 7404(Hex inverter), 7408(quad 2-input AND gates) and 7432(quad 2-input OR gates). Also, we analysed logic gates and expressed their Boolean expressions using them by checking equivalence of the Boolean expressions, also two logic circuits consisting of multiple gates.