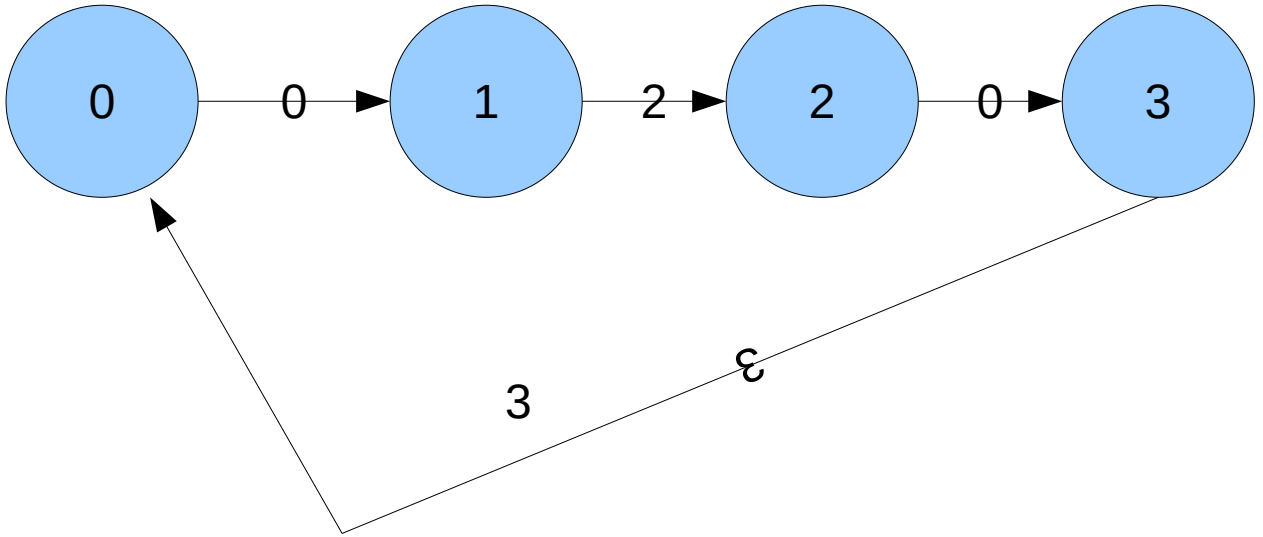
Preparação Teste

- Flip flop
- Registrador
- Contador
- **Maquina com contador em memória**
- **Maquina com porta**
- **Maquina em memória para controle (elevador)**
- **Maquina para memória cache**

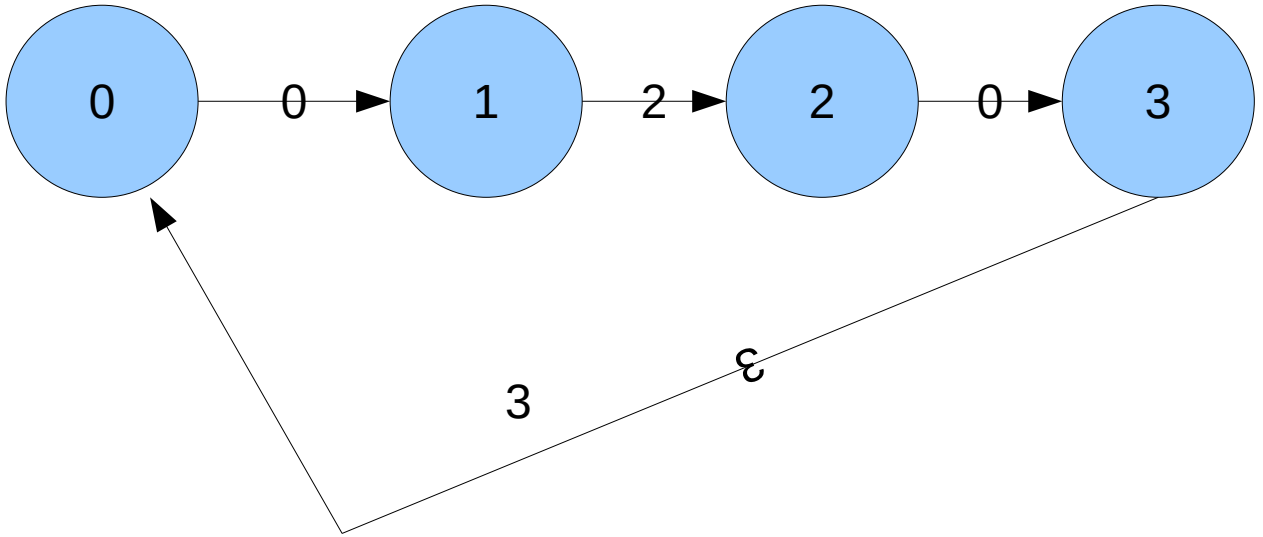
Máquina com Contador

Contador para sequencia 0,2,0,3,0,2,0,3...
solução 4 estados



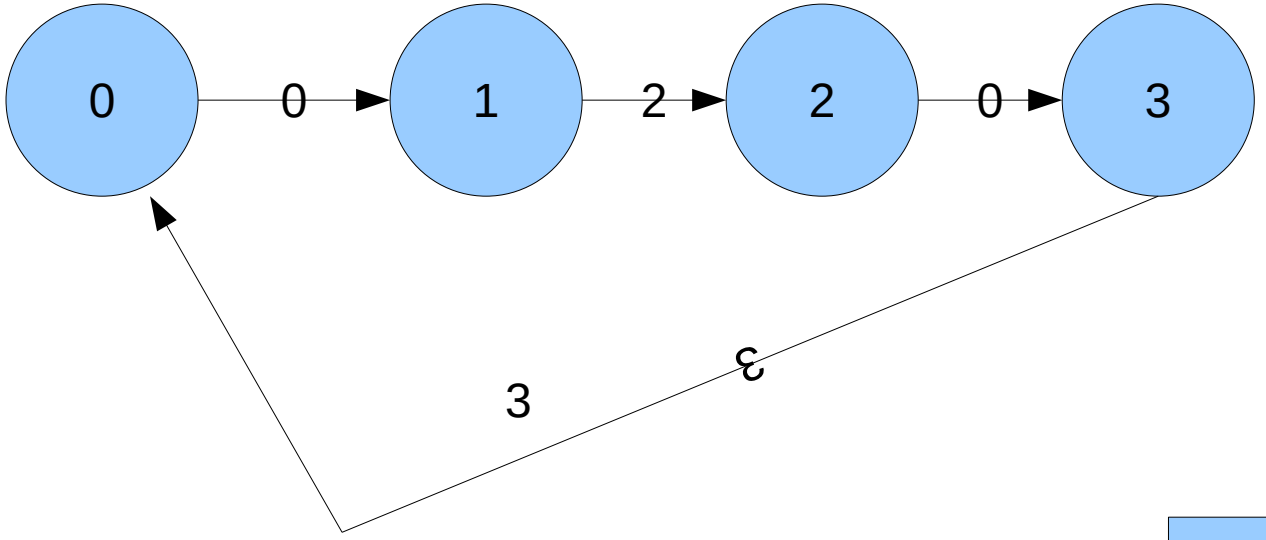
Máquina com Contador

Contador para sequencia 0,2,0,3,0,2,0,3...
solução 4 estados



0 = 00 tudo desligado
2 = 10 liga motor sobe
0 = 00 desliga
3 = 11 liga motor e desce

Máquina com Contador



Estado	Proximo	Saida
0	1	0
1	2	2
2	3	0
3	0	3

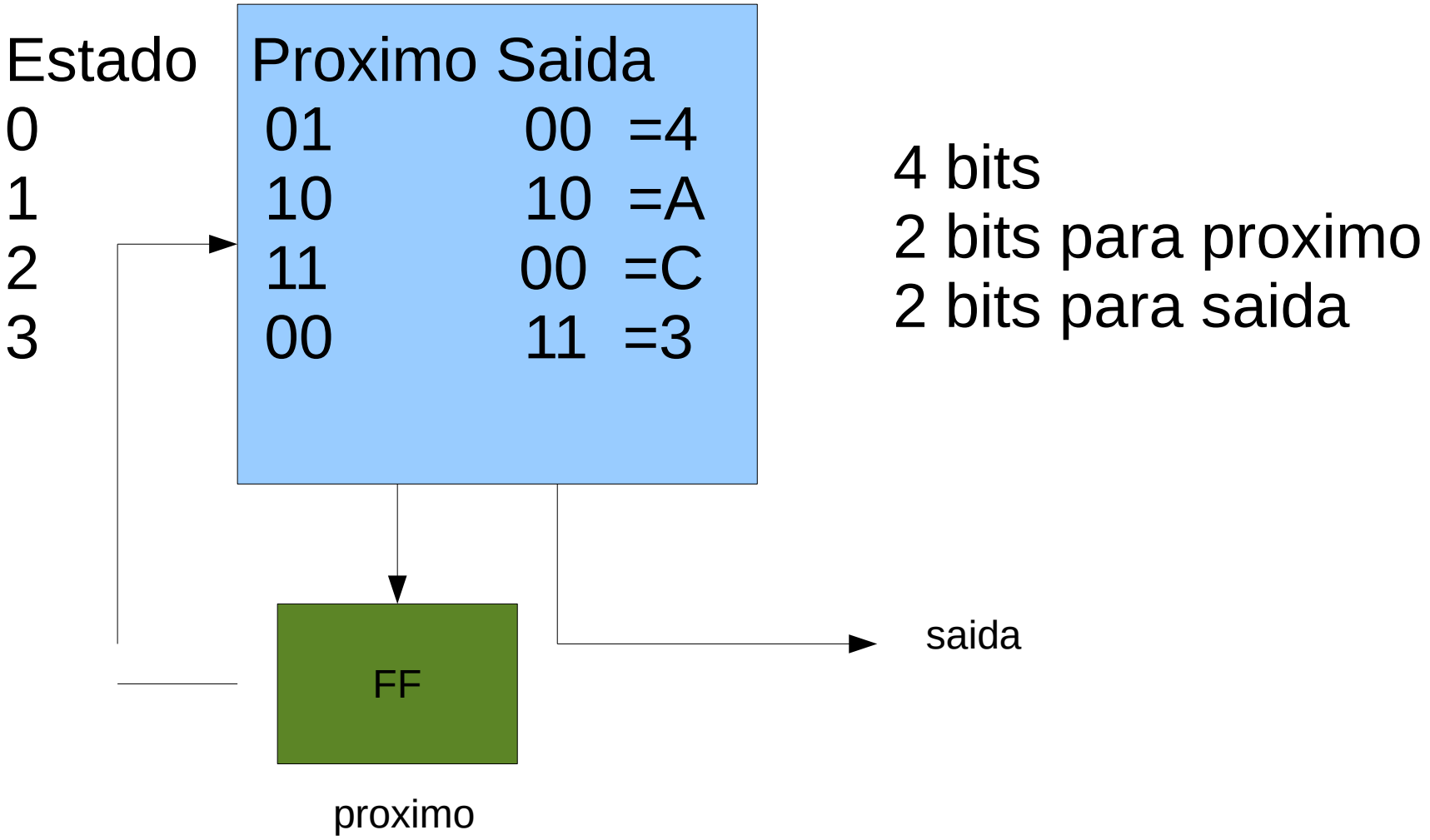
Máquina com Contador

Estado	Proximo	Saida
0	1=01	0=00
1	2=10	2=10
2	3=11	0=00
3	0=00	3=11

Estado	Proximo	Saida
0	01	00 =4
1	10	10 =A
2	11	00 =C
3	00	11 =3

4 bits
2 bits para proximo
2 bits para saida

Máquina com Contador

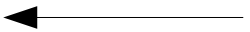


ROM em VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.Numeric_Std.all;

entity rom_contador1 is
  port (address : in std_logic_vector (1 downto 0);
        data : out std_logic_vector (3 downto 0));
end entity rom_contador1;

architecture fsmrom of rom_contador1 is
  type rom_array is array (0 to 3) of std_logic_vector(3 downto 0);
  constant rom : rom_array := ("0100",
                               "1010",
                               "1100",
                               "0011"
                              );
begin
  data <= rom(to_integer(unsigned(address)));
end architecture fsmrom;
```

Usando a ROM com FSM

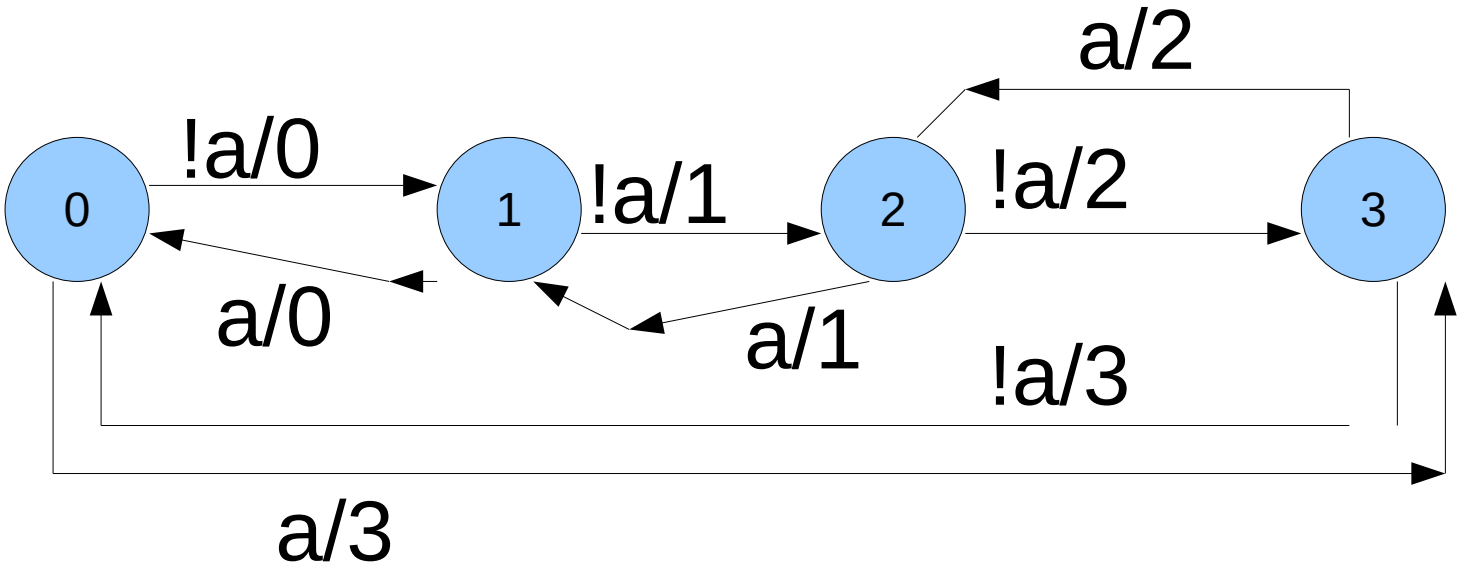
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library work;
use work.ALL;
use IEEE.Numeric_Std.all;

entity fsm_contador1 is
port ( clk : in std_logic;
              count : out std_logic_vector(1 downto 0));
end fsm_contador1;

architecture Behavioral of fsm_contador1 is
signal address : std_logic_vector(1 downto 0);
signal data : std_logic_vector(3 downto 0);
begin
rom : entity work.rom_contador1 port map(address,data);

fsmMemory :  process(clk)
  begin
      if (clk = '1' and clk'event) then
            address <= data(3 downto 2);
            count <= data(1 downto 0);
      end if;
  end process;

end Behavioral;
```



Síncrono para a Maquina
De estados funcionar....

Com Sinais de Entrada

- Contador com uma entrada A
- Se A=0, contar 0,1,2,3,0,1,2,3,.....
- Se A=1, contar 3,2,1,0,3,2,1,0,....



Com Sinais de Entrada

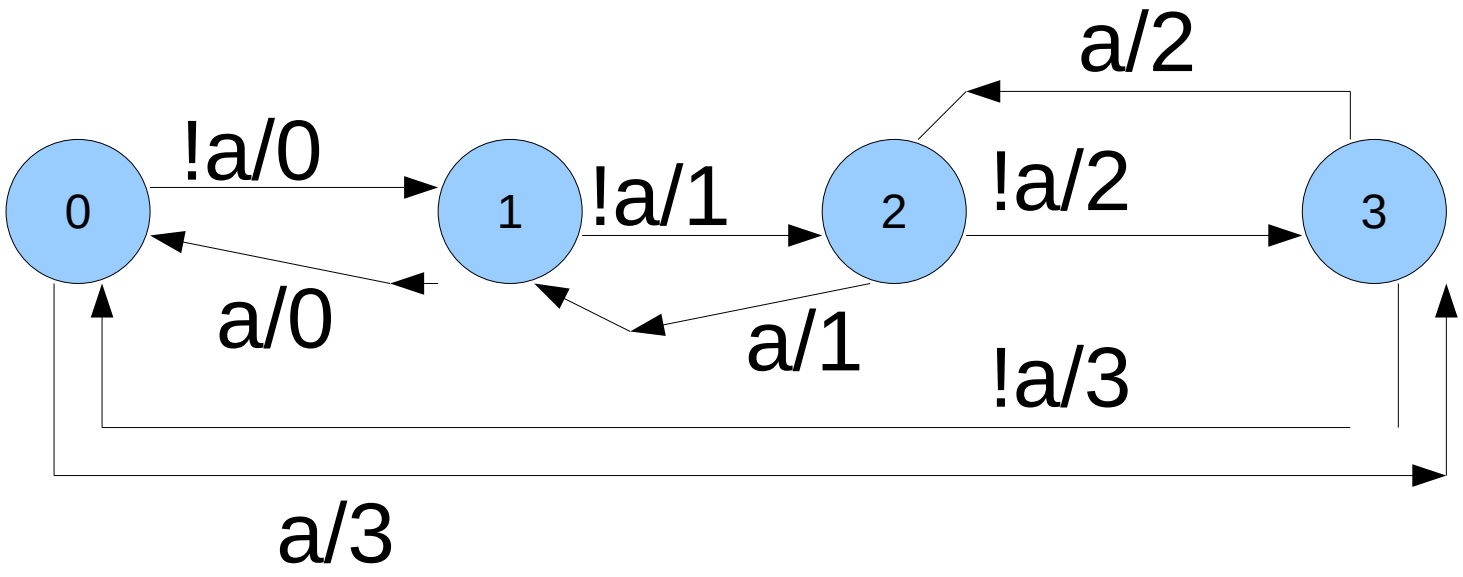
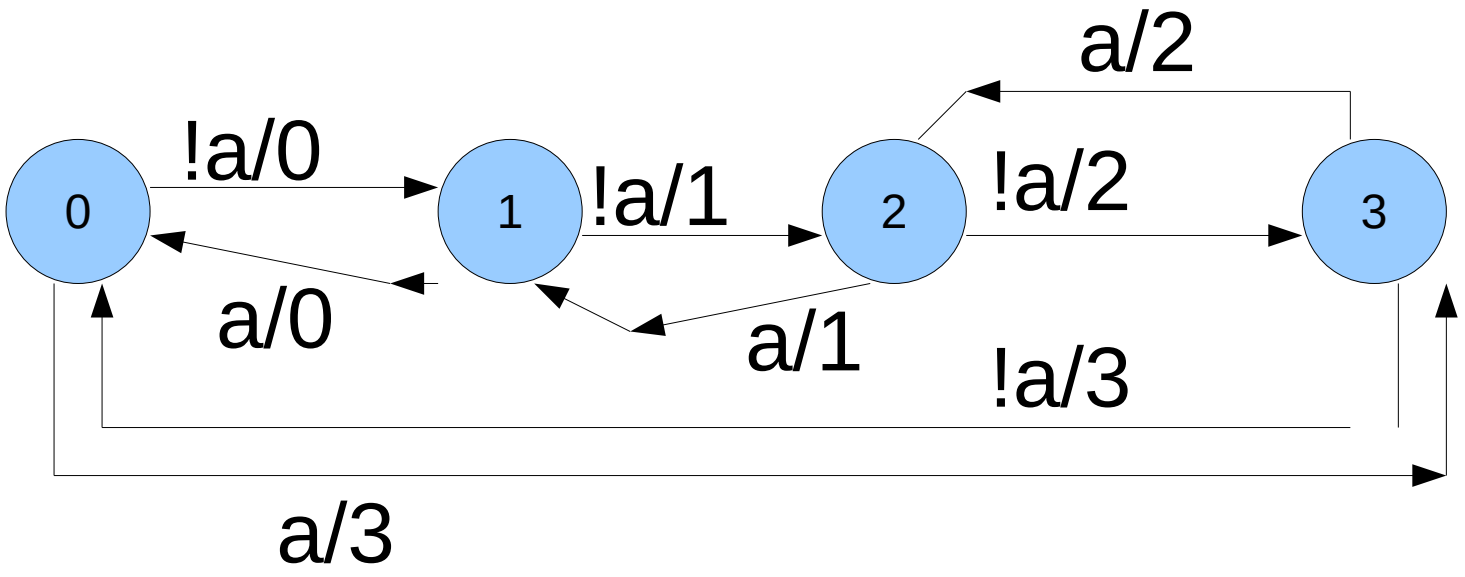


Tabela ???

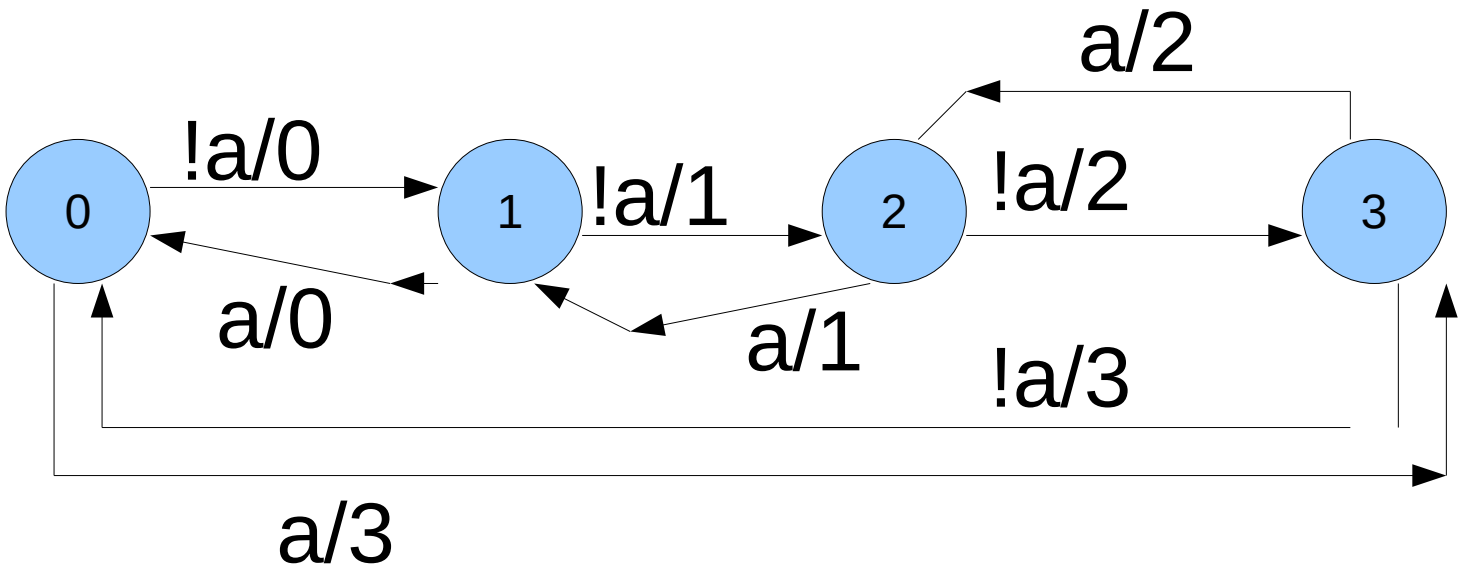
4 estados, 1 entrada, 2 bits de saida

Com Sinais de Entrada



A	Estado	Proximo	Saida
0	00	01	0
0	01	10	1
0	10	11	2
0	11	00	3
1	00	11	3
.....			

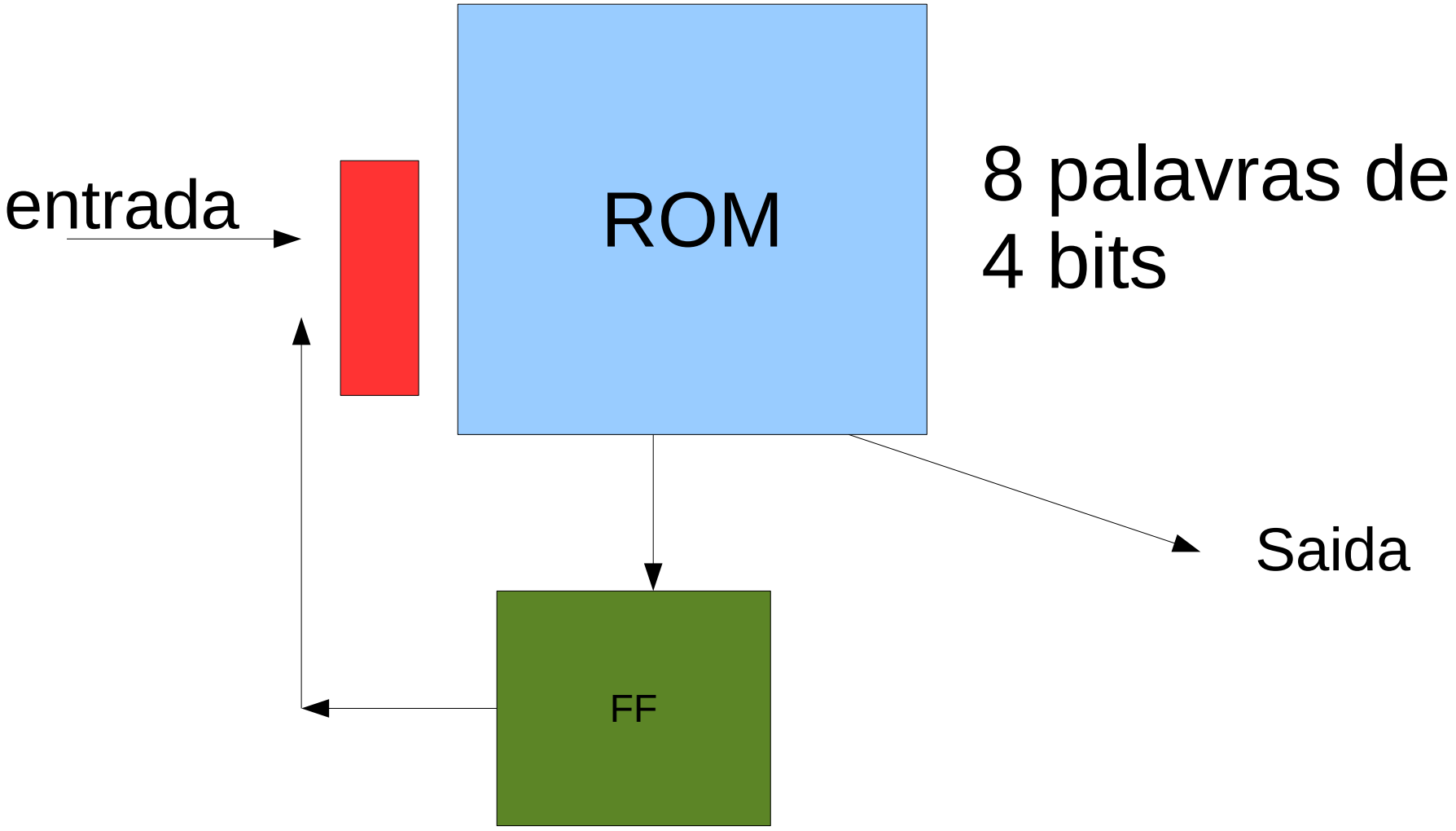
Com Sinais de Entrada



Estado	A
00	0
00	1
01	0
01	1
10	
.....	

Proximo	Saida
01	0
11	3
10	1
00	0

Circuito com entrada

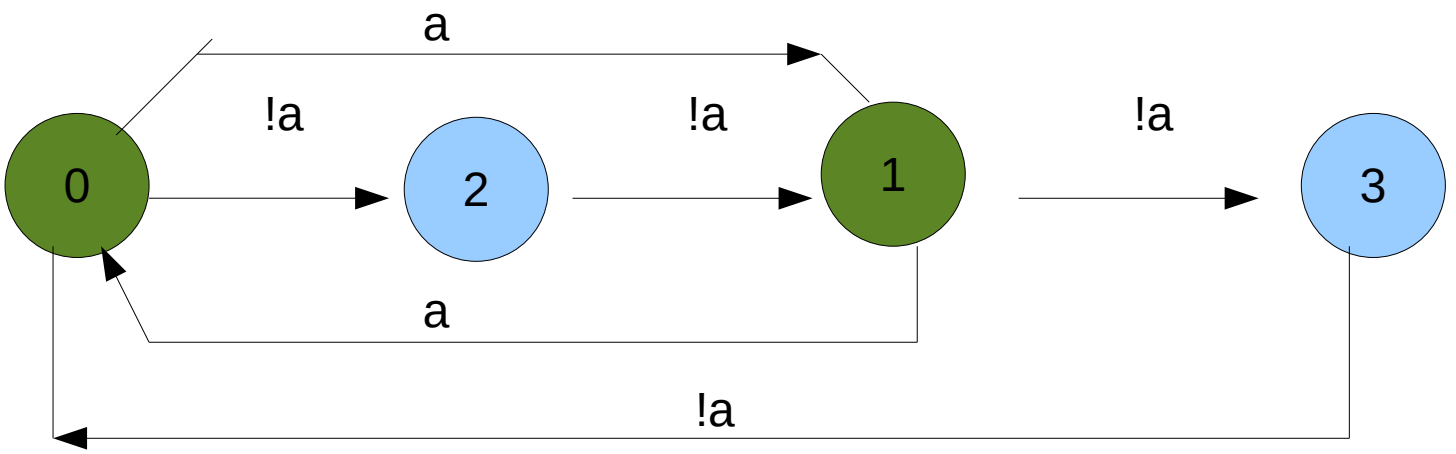


Ex4 teste 2011

A com 1 bit
A=0 fazer 0,2,1,3,0,2,1,3

A=1 fazer 0,1,0,1,.....

Ex4 teste 2011



A com 1 bit
A=0 fazer 0,2,1,3,0,2,1,3

A=1 fazer 0,1,0,1,.....