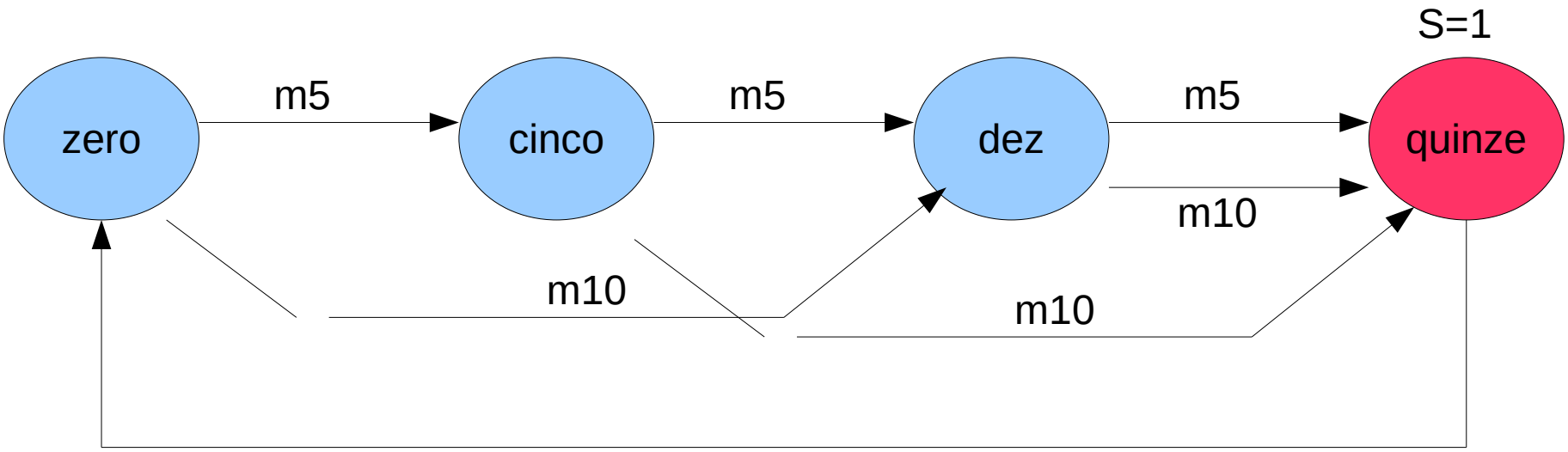
Departamento de Informática UFV

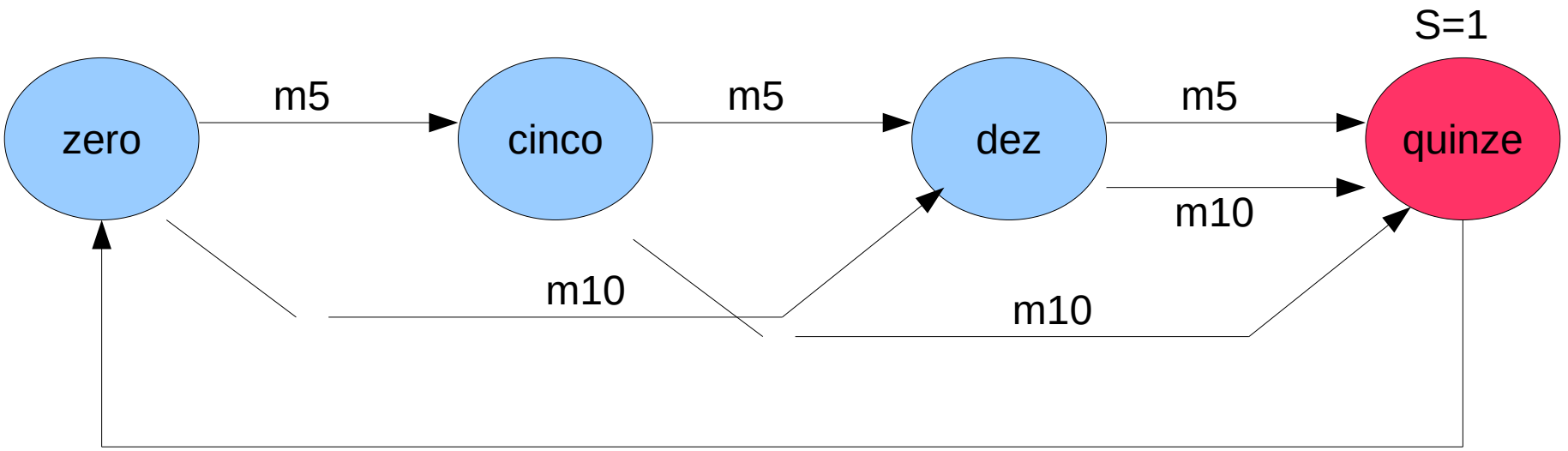
Maquina de Vendas

Especificação

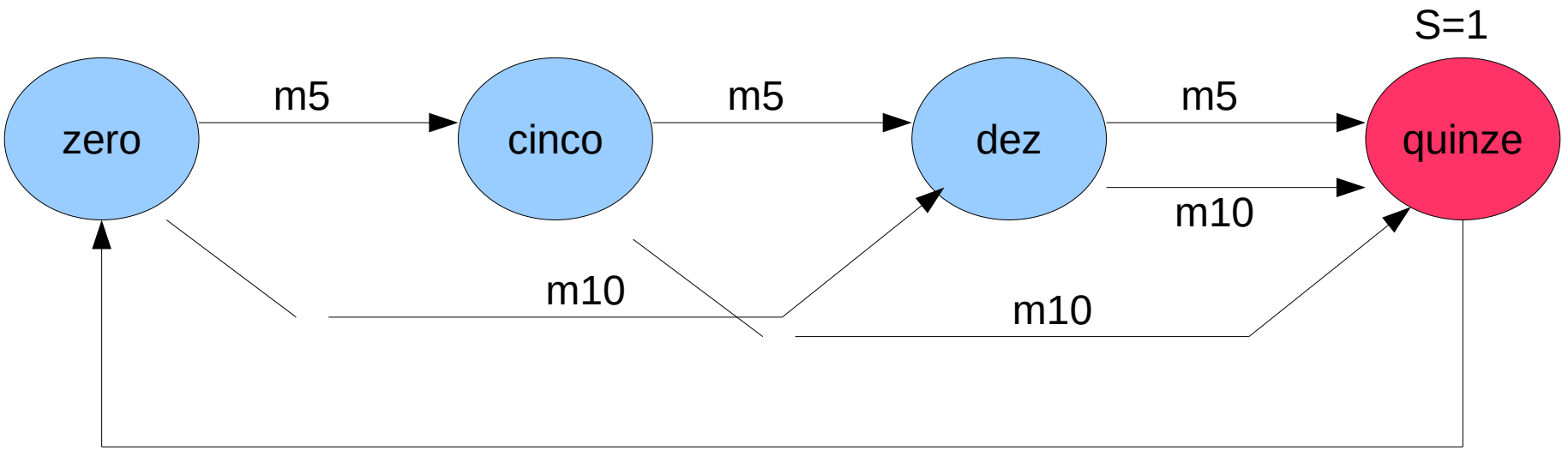
- Entradas Moedas de 5 e 10
- Saída S para vender o produto
- Preço do produto é 15
- Primeira versão sem troco....

Primeira Versão



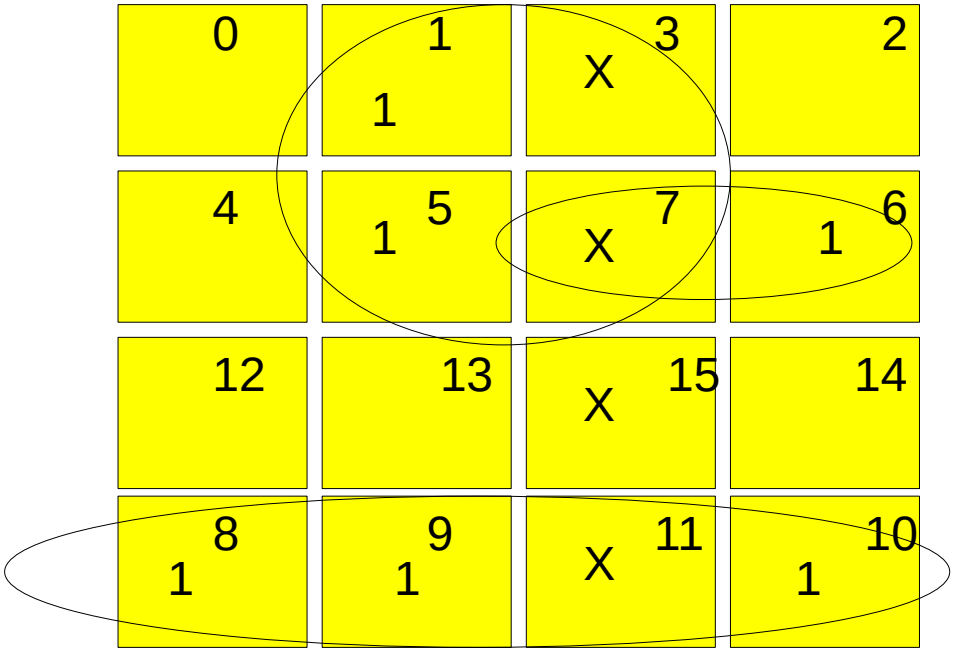


Estrado	M5	M10	Proximo		S
Zero 00	0	0	zero	0 0	0
Zero	0	1	dez	1 0	0
Zero	1	0	cinco	0 1	0
Zero	1	1		X X	X



Estrado	M5	M10	Proximo	S
Zero 00	0	0	zero 0 0	0
Zero	0	1	dez 1 0	0
Zero	1	0	cinco 0 1	0
Zero	1	1	X X	X
Cinco	0	0	cinco 0 1	0
Cinco	0	1	quinze 1 1	0
Cinco	1	0	dez 1 0	0
Cinco	1	1	X X	X

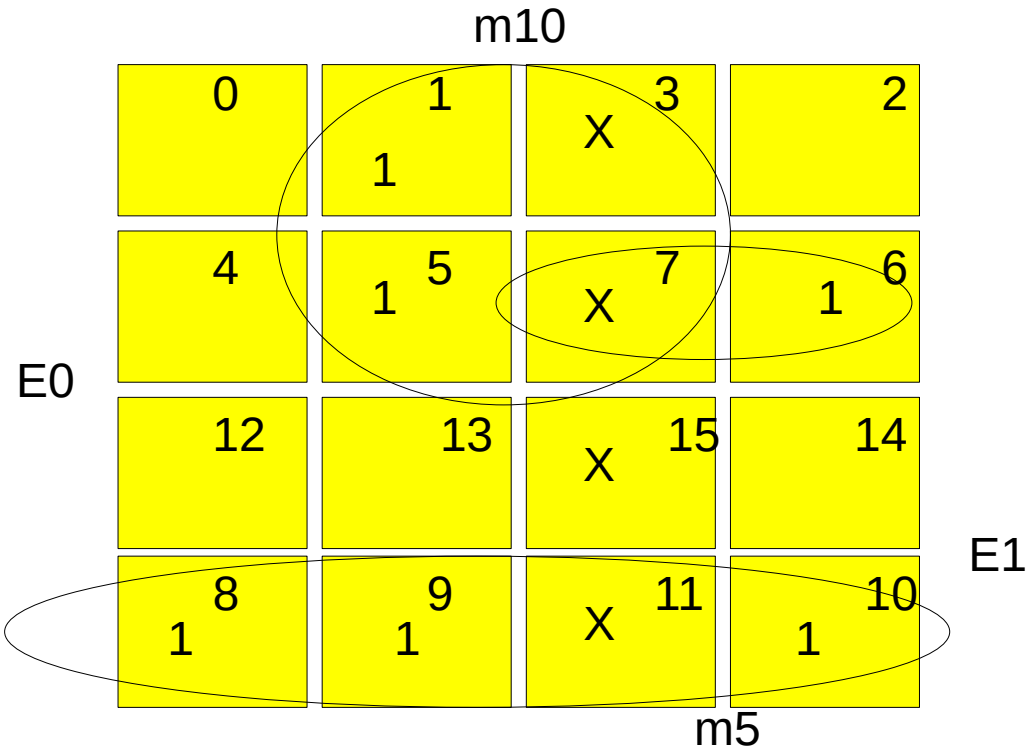
Estrado	M5	M10	Proximo	S
dez 00	0	0	dez 1 0	0
dez	0	1	quinze 1 1	0
dez	1	0	quinze 1 1	0
dez	1	1	X X	X
quinze	0	0	zero 0 0	1
quinze	0	1	zero 0 0	1
quinze	1	0	zero 0 0	1
quinze	1	1	X X	X



P1 = S(1,5,6,8,9,10)

Estrado	M5	M10	Proximo	S
Zero 00	0	0	zero 0 0	0
Zero	0	1	dez 1 0	0
Zero	1	0	cinco 0 1	0
Zero	1	1	X X	X
Cinco	0	0	cinco 0 1	0
Cinco	0	1	quinze 1 1	0
Cinco	1	0	dez 1 0	0
Cinco	1	1	X X	X

Estrado	M5	M10	Proximo	S
dez 00	0	0	dez 1 0	0
dez	0	1	quinze 1 1	0
dez	1	0	quinze 1 1	0
dez	1	1	X X	X
quinze	0	0	zero 0 0	1
quinze	0	1	zero 0 0	1
quinze	1	0	zero 0 0	1
quinze	1	1	X X	X

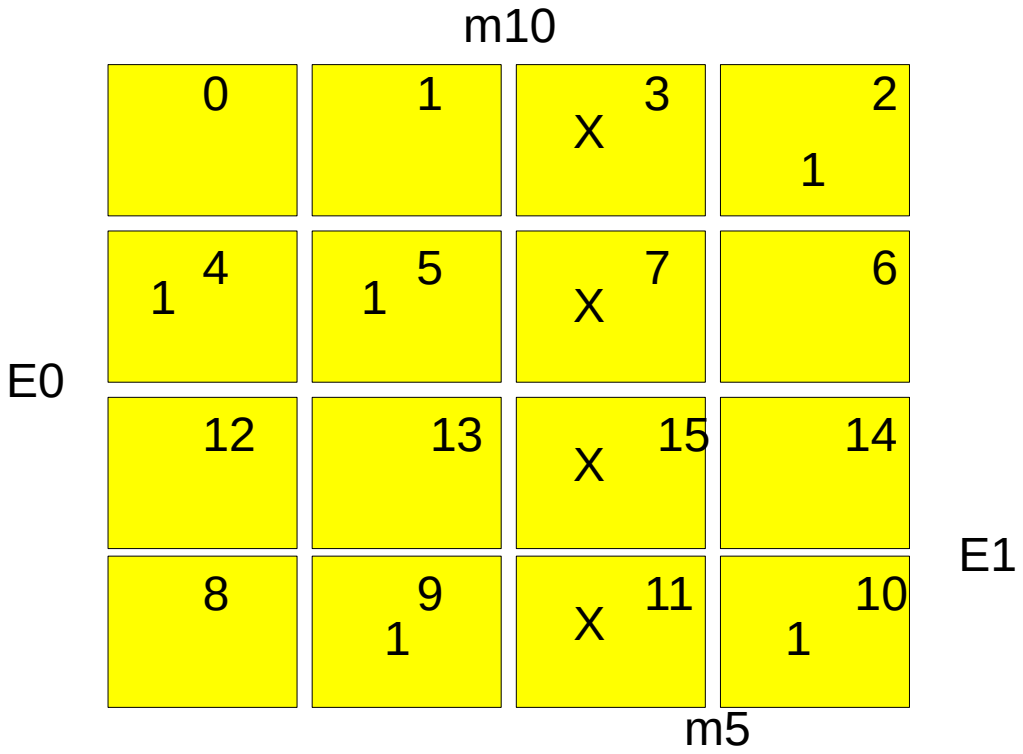


P1 = S(1,5,6,8,9,10)

P1 = E1!E0 + m10 !E1 + m5 E0 !E1

Estrado	M5	M10	Proximo	S
Zero 00	0	0	zero 0 0	0
Zero	0	1	dez 1 0	0
Zero	1	0	cinco 0 1	0
Zero	1	1	X X	X
Cinco	0	0	cinco 0 1	0
Cinco	0	1	quinze 1 1	0
Cinco	1	0	dez 1 0	0
Cinco	1	1	X X	X

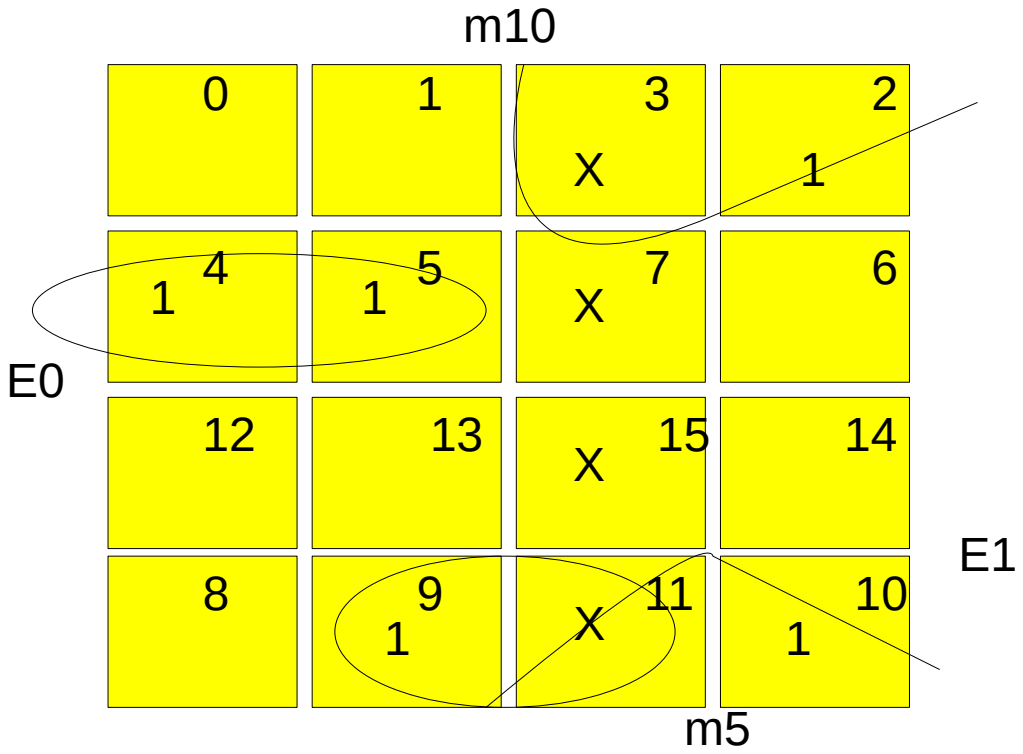
Estrado	M5	M10	Proximo	S
dez 00	0	0	dez 1 0	0
dez	0	1	quinze 1 1	0
dez	1	0	quinze 1 1	0
dez	1	1	X X	X
quinze	0	0	zero 0 0	1
quinze	0	1	zero 0 0	1
quinze	1	0	zero 0 0	1
quinze	1	1	X X	X



P0 = S(2,4,5,,9,10)

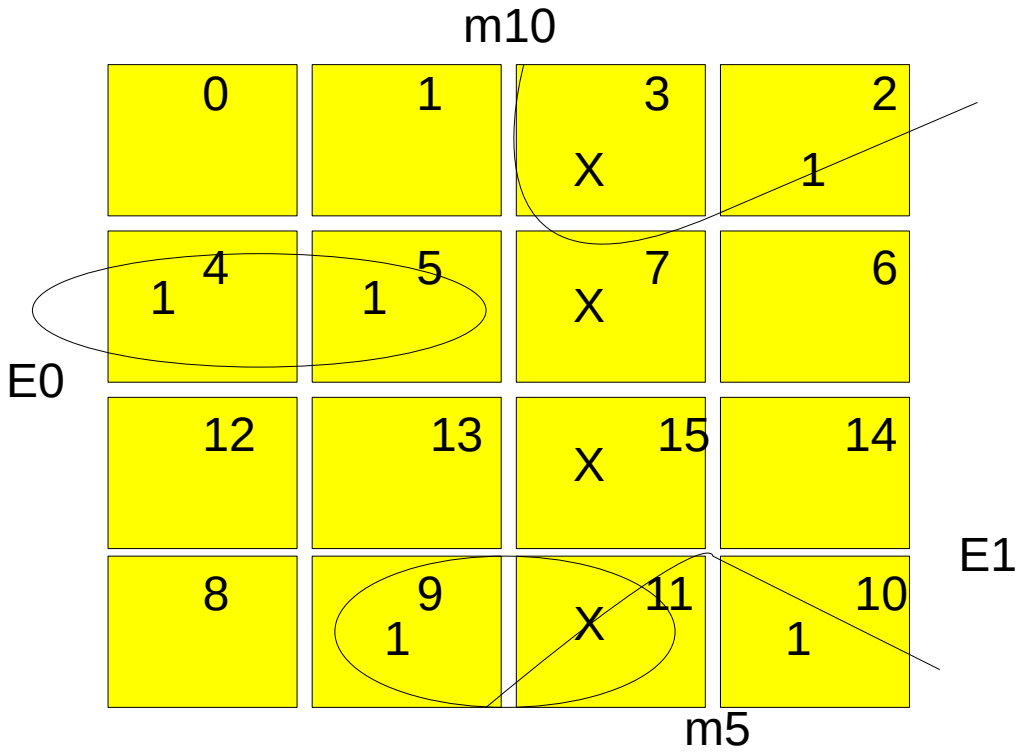
Estrado	M5	M10	Proximo		S
Zero 00	0	0	zero	0 0	0
Zero	0	1	dez	1 0	0
Zero	1	0	cinco	0 1	0
Zero	1	1		X X	X
Cinco	0	0	cinco	0 1	0
Cinco	0	1	quinze	1 1	0
Cinco	1	0	dez	1 0	0
Cinco	1	1		X X	X

Estrado	M5	M10	Proximo		S
dez 00	0	0	dez	1 0	0
dez	0	1	quinze	1 1	0
dez	1	0	quinze	1 1	0
dez	1	1		X X	X
quinze	0	0	zero	0 0	1
quinze	0	1	zero	0 0	1
quinze	1	0	zero	0 0	1
quinze	1	1		X X	X



Estrado	M5	M10	Proximo		S
Zero 00	0	0	zero	0 0	0
Zero	0	1	dez	1 0	0
Zero	1	0	cinco	0 1	0
Zero	1	1		X X	X
Cinco	0	0	cinco	0 1	0
Cinco	0	1	quinze	1 1	0
Cinco	1	0	dez	1 0	0
Cinco	1	1		X X	X

Estrado	M5	M10	Proximo		S
dez 00	0	0	dez	1 0	0
dez	0	1	quinze	1 1	0
dez	1	0	quinze	1 1	0
dez	1	1		X X	X
quinze	0	0	zero	0 0	1
quinze	0	1	zero	0 0	1
quinze	1	0	zero	0 0	1
quinze	1	1		X X	X



P0 = S(2,4,5,,9,10)

P0 = ! E0 m5 + !m5 E0 !E1 + m10 E1 !E0

Estrado	M5	M10	Proximo		S
Zero 00	0	0	zero	0	0
Zero	0	1	dez	1	0
Zero	1	0	cinco	0	0
Zero	1	1		X	X
Cinco	0	0	cinco	0	0
Cinco	0	1	quinze	1	0
Cinco	1	0	dez	1	0
Cinco	1	1		X	X

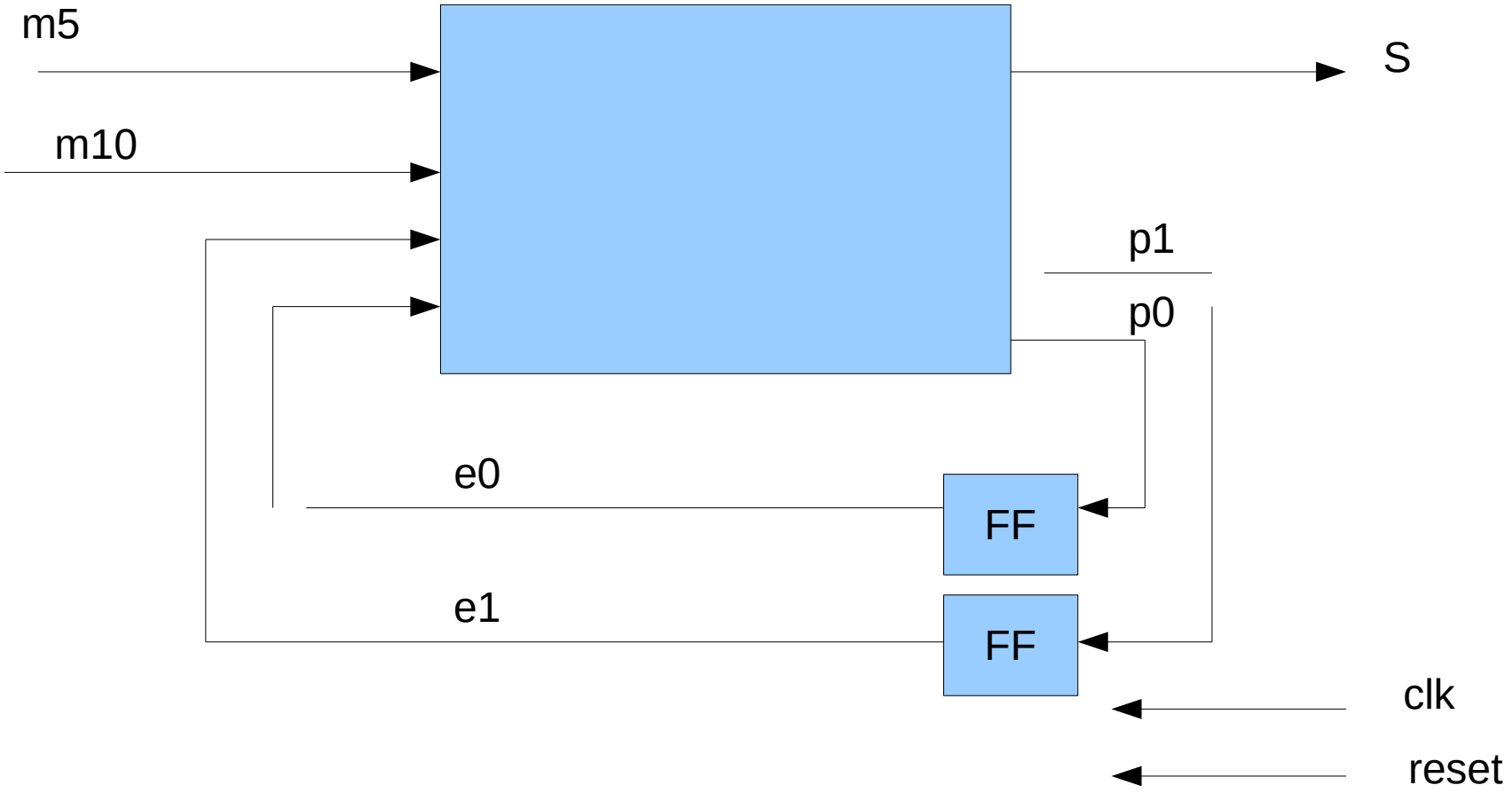
Estrado	M5	M10	Proximo		S
dez 00	0	0	dez	1	0
dez	0	1	quinze	1	0
dez	1	0	quinze	1	0
dez	1	1		X	X
quinze	0	0	zero	0	1
quinze	0	1	zero	0	1
quinze	1	0	zero	0	1
quinze	1	1		X	X

S = E1 E0 - estado quinze

Estrado	M5	M10	Proximo	S
Zero 00	0	0	zero 0 0	0
Zero	0	1	dez 1 0	0
Zero	1	0	cinco 0 1	0
Zero	1	1	X X	X
Cinco	0	0	cinco 0 1	0
Cinco	0	1	quinze 1 1	0
Cinco	1	0	dez 1 0	0
Cinco	1	1	X X	X

Estrado	M5	M10	Proximo	S
dez 00	0	0	dez 1 0	0
dez	0	1	quinze 1 1	0
dez	1	0	quinze 1 1	0
dez	1	1	X X	X
quinze	0	0	zero 0 0	1
quinze	0	1	zero 0 0	1
quinze	1	0	zero 0 0	1
quinze	1	1	X X	X

Estrutural em VHDL



código

```
entity dff is
port( d: in std_logic;       clk, reset: in std_logic;
            q: out std_logic
);
end dff;
architecture Behavioral of dff is
begin
      process(reset, clk)
            begin
      -- clock rising edge
            if ( reset = '1' ) then q <='0';
            elsif (clk='1' and clk'event) then
                  q <= d;
            end if;
end process;
end Behavioral;
```

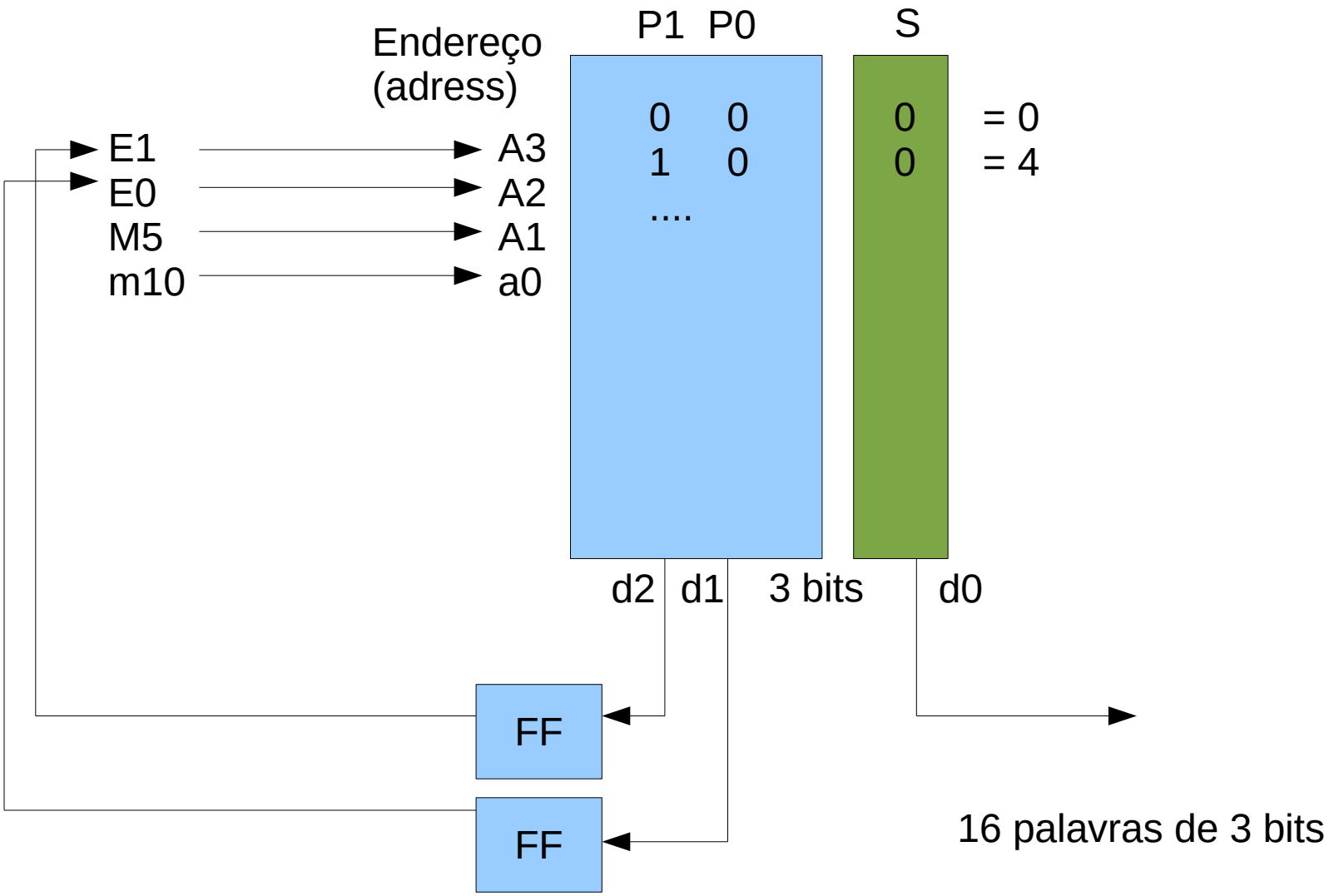
código

```
entity maq_vendas is
port (   m5,m10 : in std_logic;
                              clk, reset : in std_logic;
                  s : out std_logic );
end maq_vendas;

architecture Behavioral of maq_vendas is
signal p1,p0,e1,e0 : std_logic;
begin
p1 <= ( e1 and (not e0)) or (m10 and (not e1))
                  or (m5 and e0 and (not e1));
p0 <= ( (not e0) and m5) or ((not m5) and e0 and (not e1))
                  or (m10 and e1 and (not e0));
s <= e1 and e0;
ff0 : entity work.dff port map ( p0, clk, reset, e0);
ff1 : entity work.dff port map ( p1, clk, reset, e1);

end Behavioral;
```

Modelo com Memoria



VHDL

```
Begin
        if(reset = '1') then
                Moore_state <= ZERO;
        elsif (clk = '1' and clk'event) then
                case Moore_state is
        when zero =>
        if M10 = '1' then Moore_state <= ten;
        elsif M5 = '1' then Moore_state <= five;
        Else Moore_state <= zero;
end if;
when five=>
......
end case;
end if;
End process;
s <= '1' when Moore_state = three else '0';
```