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Technical Reference Manual

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CoreSight Design Kit
Technical Reference Manual

Release Information

Change history

Date	Issue	Confidentiality	Change
29 September 2004	A	Non-confidential	First release for r0p0.
24 March 2005	B	Non-confidential	Updated for r0p1. Programmer's model revised.
28 February 2006	C1b	Confidential	Updated for r1p0 (Alpha). Serial Wire information added to Chapter 3. Chapter 11 (SWV), Chapter 12 (SWO), Chapter 13 (ITM), and Appendix C (SWD and JTAG Trace Connector) added.
20 March 2006	C2	Non-Confidential	This is an extract from an unreleased version of the CoreSight Design Kit Technical Reference Manual, and will be superseded on release of the full document.
10 April 2006	C3	Non-Confidential	Values changed in SWD and JTAG select mecahnism.

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The information in this document is for a Beta product, that is a product under development.

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Chapter 1
Debug Access Port

This is an extract of the chapter that describes the *Debug Access Port* (DAP). It contains the following section:

1.1 SWJ-DP

SWJ-DP is a combined JTAG-DP and SW-DP that enables either a *Serial Wire Debug* (SWD) or JTAG probe to be connected to a target. It is the standard CoreSight debug port, and enables access either the JTAG-DP or SW-DP blocks. To make efficient use of package pins, serial wire shares, or overlays, the JTAG pins, using an autodetect mechanism that switches between JTAG-DP and SW-DP, depending on which probe is connected. A special sequence on the **TMS** pin is used to switch between JTAG-DP and SW-DP. The SWJ-DP behaves like a pure JTAG target if normal JTAG sequences are sent to it.

Figure 1-1 shows the external connections to the SWJ-DP.

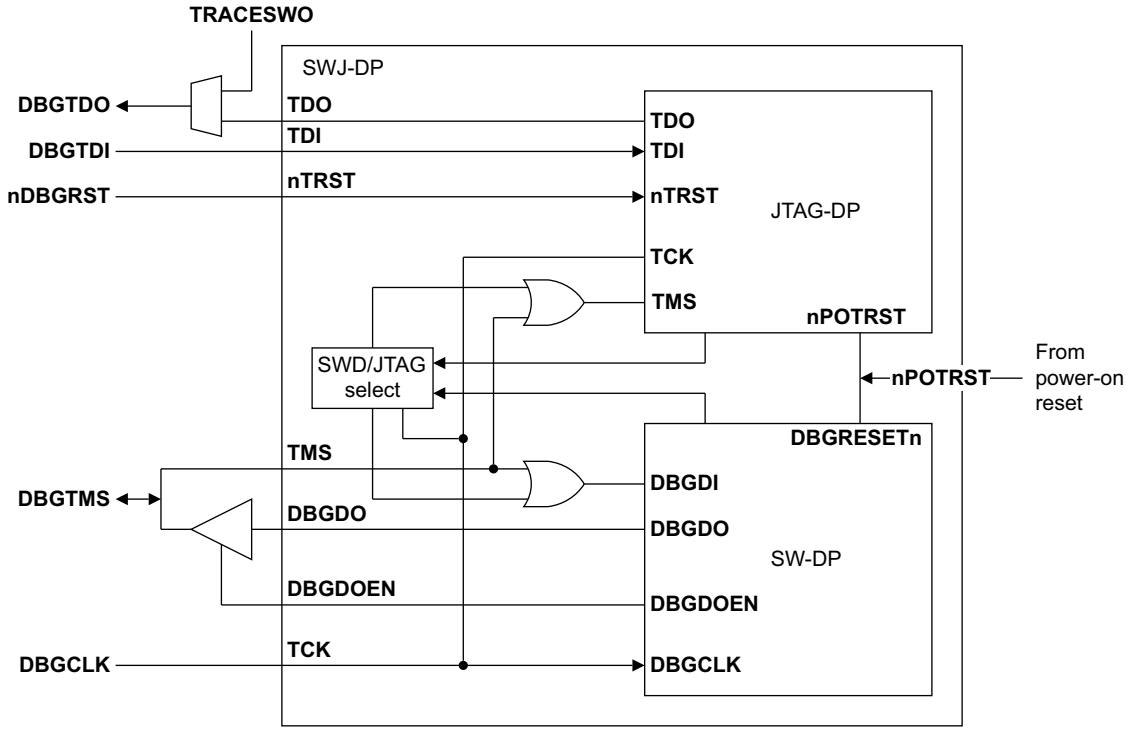

Figure 1-1 SWJ-DP external connections

The SWJ-DP is described in more detail in:

- *Structure* on page 1-3
- *Operation* on page 1-3
- *JTAG and SWD interface* on page 1-4
- *Clock and reset control interface* on page 1-4
- *SWD and JTAG select mechanism* on page 1-4.

1.1.1 Structure

The SWJ-DP consists of a wrapper around the JTAG-DP and SW-DP. Its function is to select JTAG or SWD as the connection mechanism and enable either JTAG-DP or SW-DP as the interface to the DAP.

1.1.2 Operation

SWJ-DP enables an *Application Specific Integrated Circuit* (ASIC) to be designed which can be used in systems that require either a JTAG interface or a SWD interface. There is a trade-off between the number of pins used and compatibility with existing hardware and test equipment. There are several scenarios where the use of a JTAG debug interface must be maintained:

- to enable inclusion in an existing scan chain, generally on-chip TAPs used for test or other purposes.
- to enable the device to be cascaded with legacy devices which use JTAG for debug
- to enable use of existing debug hardware with the corresponding test TAPs, for example, in *Automatic Test Equipment* (ATE).

An ASIC fitted with SWJ-DP support can be connected to legacy JTAG equipment without any requirement to make changes. If a SWD tool is available, only two pins are required, instead of the usual four used for JTAG. Two pins are therefore released for alternative use.

These two pins can only be used when there is no conflict with their use in JTAG mode. In addition, to support use of SWJ-DP in a scan chain with other JTAG devices, the default state after reset must be to use these pins for their JTAG function. If the direction of the alternative function is compatible with being driven by a JTAG debug device, the transition to a shift state can be used to transition from the alternative function to JTAG mode.

The alternate function cannot be used while the ASIC is being used in JTAG debug mode.

The switching scheme is arranged so that, provided there is no conflict on the **TDI** and **TDO** pins, a JTAG debugger is able to connect by sending a specific sequence.

The connection sequence used for SWD is safe when applied to the JTAG interface, even if hot-plugged, enabling the debugger to continually retry its access sequence. A sequence with `TMS=1` ensures that JTAG-DP, SW-DP, and the watcher circuit are in a known reset state. The pattern used to select SWD has no effect on JTAG targets.

SWJ-DP is compatible with a free-running **TCK**, or a gated clock which is supplied by the external tools.

1.1.3 JTAG and SWD interface

The external JTAG interface has four mandatory pins, **TCK**, **TMS**, **TDI**, and **TDO**, and an optional reset, **nTRST**. JTAG-DP and SW-DP also require a separate power-on reset, **nPOTRST**.

The external SWD interface requires two pins:

- a bidirectional **SWDIO** signal
- a clock, which can be input or output from the device.

The block level interface has two pins for data plus an output enable, which must be used to drive a bidirectional pad for the external interface, and clock and reset signals.

To enable sharing of the connector for either JTAG or SWD, connections must be made external to the SWJ-DP block, as shown in Figure 1-1 on page 1-2. In particular, **TMS** must be a bidirectional pin to support the bidirectional **SWDIO** pin in SWD mode.

When SWD mode is being used, the **TDO** pin is expected to be re-used for *Serial Wire Output* (SWO). The **TDI** pin is available for use as an alternative input function.

Note

If SWO functionality is required in JTAG mode, a dedicated pin is required.

1.1.4 Clock and reset control interface

In the **DBGCLK** clock domain, there are registers to enable power control for the on-chip debug infrastructure. This enables the majority of the debug logic, such as ETM and ETB, to be powered down by default, and only the serial engine has to be clocked. A debug session then starts by powering up the remainder of the debug components. In SWJ-DP, either JTAG-DP or SW-DP can make power-up or reset requests but only if they are the selected device. Even in a system which does not provide a clock and reset control interface to the DAP, it is necessary to connect these signals so it appears that a clock and reset controller is present. This permits correct handshaking of the request and acknowledge signals to be performed.

1.1.5 SWD and JTAG select mechanism

SWJ-DP enables either a SWD or JTAG protocol to be used on the debug port. To do this, it implements a watcher circuit that detects a specific 16-bit select sequence on the DBGTMS pin:

- one 16-bit sequence is used to switch from JTAG to SWD operation
- a different 16-bit sequence is used to switch from SWD to JTAG.

The switcher defaults to JTAG operation on power-on reset and therefore the JTAG protocol can be used from reset without sending a select sequence.

Switching from one protocol to the other can only occur when the selected interface is in its reset state: JTAG must be in its *Test-Logic-Reset* (TLR) state and SWD must be in line-reset.

The watcher block puts itself to sleep when it has finished tracking a specific sequence and only wakes up again when it detects the next reset condition. Figure 1-2 is a simplified state diagram that shows how the watcher transitions between sleeping, detecting, and selection states.

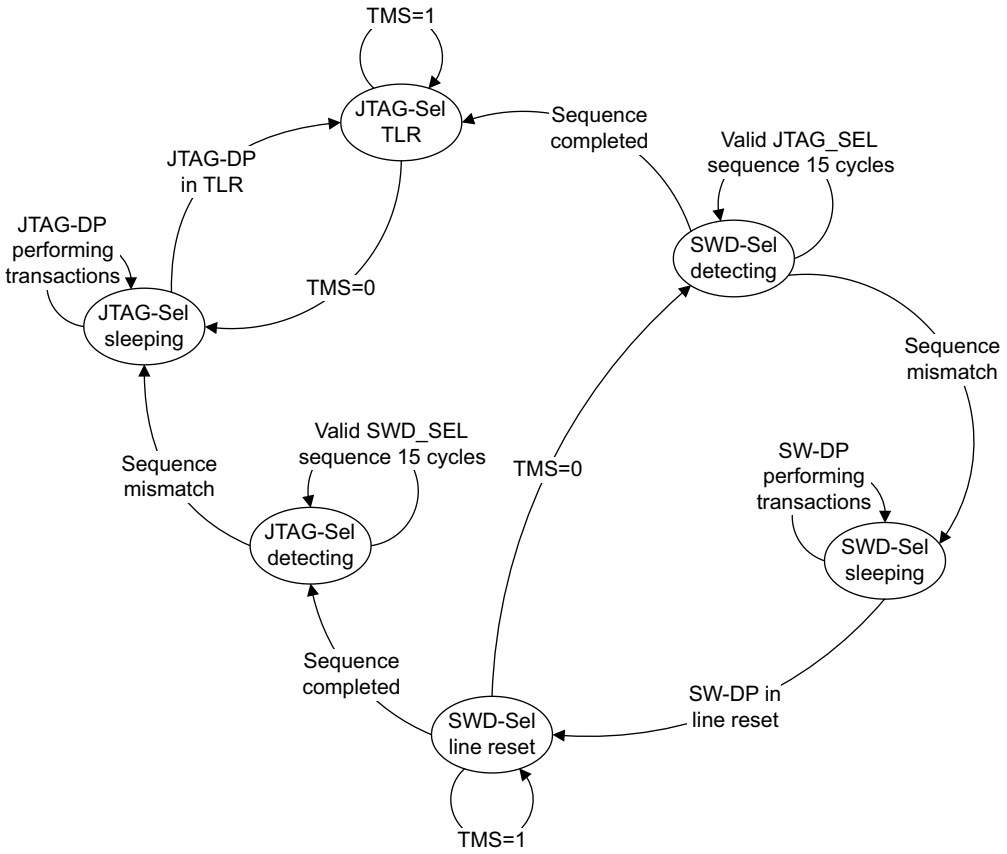

Figure 1-2 SWD and JTAG select state diagram

3.4.5.1 SWJ-DP programmer's model

The SWJ-DP programmer's model is described in:

- *JTAG to SWD switching*
- *SWD to JTAG switching*.

JTAG to SWD switching

To switch SWJ-DP from JTAG to SWD operation:

- Send more than 50 **DBGCLK** cycles with DBGTMS=1. This ensures that both SWD and JTAG are in their reset states.
- Send the 16-bit JTAG-to-SWD select sequence on **DBGTMS**.
- Send more than 50 **DBGCLK** cycles with DBGTMS=1. This ensures that if SWJ-DP was already in SWD mode, before sending the select sequence, the SWD goes to line reset.
- Perform a READID to validate that SWJ-DP has switched to SWD operation.

The 16-bit JTAG-to-SWD select sequence is defined to be 0111100111100111, MSB first. This can be represented as 16'h79E7 transmitted MSB first or 16'hE79E when transmitted LSB first.

This sequence has been chosen to ensure that the SWJ-DP switches to using SWD whether it was previously expecting JTAG or SWD. As long as the 50 DBGTMS=1 sequence is sent first, the JTAG-to-SWD select sequence is benign to SW-DP, and is also benign to SWD and JTAG protocols used in the SWJ-DP, and any other TAP controllers that might be connected to **DBGTMS**.

Note

An earlier version of SWJ-DP uses a different switching sequence which is now deprecated. See Appendix D *Deprecated SWJ-DP Switching Sequences* for details of this switching sequence.

SWD to JTAG switching

To switch SWJ-DP from SWD to JTAG operation:

- Send more than 50 **DBGCLK** cycles with DBGTMS=1. This ensures that both SWD and JTAG are in their reset states.
- Send the 16-bit SWD-to-JTAG select sequence on **DBGTMS**.

- Send at least 5 **DBGCLK** cycles with DBGTMS=1. This ensures that if SWJ-DP was already in JTAG mode, before sending the select sequence, that JTAG goes into the TLR state.
- Set the JTAG-DP IR to READID and shift out the DR to read the ID.

The 16-bit JTAG-to-SWD select sequence is defined to be 0011110011100111, MSB first. This can be represented as 16'h3CE7 transmitted MSB first or 16'hE73C when transmitted LSB first.

This sequence has been chosen to ensure that the SWJ-DP switches to using JTAG whether it was previously expecting JTAG or SWD. If the DBGTMS=1 sequence is sent first, the SWD-to-JTAG select sequence is benign to SW-DP, and is also benign to SWD and JTAG protocols used in the SWJ-DP, and any other TAP controllers that might be connected to **DBGTMS**.

Note

An earlier version of SWJ-DP uses a different switching sequence which is now deprecated. See Appendix D *Deprecated SWJ-DP Switching Sequences* for details of this switching sequence.

3.4.5.2 Restriction on switching

It is recommended that when a system is powered up, a debug connection is made, and the mode is selected, either SWD or JTAG, the system remains in this mode throughout the debug session. Switching between modes should not be attempted while any component of the DAP is active.

Attempting to switch between modes while any component of the DAP is active can have unpredictable results. A power-on reset cycle might be required to reset the DAP before switching can be retried.

Appendix A
Serial Wire Debug and JTAG Trace Connector

This appendix describes the SWD and JTAG trace connector. It contains the following sections:

- *About the SWD and JTAG trace connector* on page A-2.
- *Pinout details* on page A-3.

A.1 About the SWD and JTAG trace connector

The SWD and JTAG trace connector is used for debug targets requiring JTAG, SWD, SWO, and low bandwidth trace connectivity.

This appendix describes 10-way and 20-way connectors that are mounted on debug target boards. These are specified as 0.050 inch pitch two-row pin headers, Samtec FTSH or equivalent. See `www.samtec.com`.

The connectors are grouped into compatible sets according to the functions supported. Some targets support communication by both SWD and JTAG using the SWJ-DP block to switch between protocols.

A.2 Pinout details

The connector pin layouts are described in:

- *Combined pin names*
- *10-way connector pinouts* on page A-4
- *20-way connector pinouts including trace* on page A-6
- *20-way connector pinouts for legacy JTAG connections* on page A-12.

Note

The equivalent pin numbers on a CoreSight-compatible Mictor connector pinout are shown in the tables. This enables you to build a target where the debug communication signals are brought in parallel to both connectors so that the target can be debugged using either physical connector.

A.2.1 Combined pin names

Table A-1 shows a summary of the pin names.

Table A-1 Summary of pin names

Pin number	Combined pin names
1	Vref+Cap
2	**TMS/SWDIO**
3	GND
4	**TCK/SWCLK**
5	GND
6	**TDO/SWO/EXTa/TraceCtl**
7	(key)
8	**TDI/EXTb/TraceCtl**
9	GND(1)
10	**TraceCtl/nRESET**
11	Gnd/TgtPwr+Cap
12	**TraceClk/RTCK**
13	Gnd/TgtPwr+Cap

Table A-1 Summary of pin names (continued)

Pin number	Combined pin names
14	**TraceD0/SWO**
15	GND
16	**TraceD1/nTRST**
17	GND
18	**TraceD2/TrigIn**
19	GND
20	**TraceD3/TrigOut**

A.2.2 10-way connector pinouts

There are two types of the pinout for a 10-pin connector, one supporting communication using SWD, and one using JTAG, and these are arranged to facilitate dynamic switching between the protocols.

SWD is the preferred protocol for debugging because it provides more data bandwidth over fewer pins, therefore freeing some for use by application functions. JTAG can be used where the target is communicating with a tool chain that does not support SWD, or with test tools performing board-level boundary scan testing, where it might be acceptable to sacrifice the functional pins multiplexed with JTAG.

Table A-2 shows the 10-way header for targets using SWD for debug communication, and includes an optional *Serial Wire Output* (SWO) signal for conveying application and instrumentation trace. This layout is typically used in a CoreSight system that uses a SWJ-DP operating in SWD mode.

Table A-2 10-way connector for SWD

Pin name	10-way pin number	Mictor pin number
Vref+Cap	1	12
SWDIO	2	17
GND	3	-
SWCLK	4	15
GND	5	-

Table A-2 10-way connector for SWD (continued)

Pin name	10-way pin number	Mictor pin number
SWO	6	11
(key)	7	-
NC/EXTb	8	19
GND(1)	9	-
nRESET	10	9

Table A-3 shows the 10-way header for targets using JTAG for debug communication. This layout is typically used in a CoreSight system including a JTAG-DP, or one with a SWJ-DP operating JTAG mode, possibly because it is cascaded with other JTAG TAPs. A target board can use this connector for performing board-level boundary scan but then switch its SWJ-DP into SWD mode for debugging according to the layout shown in Table A-2 on page A-4. This frees up pins 6 and 8 for either application functions or SWO.

Table A-3 10-way connector for JTAG

Pin name	10-way pin number	Mictor pin number
Vref+Cap	1	12
TMS	2	17
GND	3	-
TCK	4	15
GND	5	-
TDO	6	11
(key)	7	-
TDI	8	19
GND(1)	9	-
nRESET	10	9

A.2.3 20-way connector pinouts including trace

20-way connectors include support for a narrow trace port, up to four data bits, operating at moderate speed, up to 100 MSamples/sec. They are described in:

- *Connector pinouts for trace systems using TraceCtl*
- *Connector pinouts for future systems* on page A-10.

Connector pinouts for trace systems using TraceCtl

Most existing trace systems operate their CoreSight TPIU in normal mode or bypass mode, or use a dedicated trace port that is equivalent to bypass mode. All of these require a **TraceCtl** signal for identifying trigger events and idle trace samples.

There are several possible pin locations for the **TraceCtl** signal according to which other signals a particular target requires. Trace collection equipment can be configured to accept any of these.

Table A-4 shows the 20-way header for targets using SWD for debug communication, which also require both **nRESET**, pin 10, and a **SWO** signal for conveying application and instrumentation trace. This layout is typically used in a CoreSight system that uses a SWJ-DP operating in SWD mode, where it is necessary to operate that trace port in normal or bypass mode.

Table A-4 20-way connector for SWD

Pin name	20-way pin number	Mictor pin number
Vref+Cap	1	12
SWDIO	2	17
GND	3	-
SWCLK	4	15
GND	5	-
SWO/EXTa	6	(11)
(key)	7	-
TraceCtl	8	36
GND(1)	9	-
nRESET	10	9

Table A-4 20-way connector for SWD (continued)

Pin name	20-way pin number	Mictor pin number
Gnd/TgtPwr+Cap	11	-
TraceClk	12	6
Gnd/TgtPwr+Cap	13	-
TraceD0	14	38
GND	15	-
TraceD1	16	28
GND	17	-
TraceD2	18	26
GND	19	-
TraceD3	20	24

Table A-5 shows the 20-way header for targets using SWD for debug communication and includes an optional **SWO** signal for conveying application and instrumentation trace. This layout is typically used in a CoreSight system that uses a SWJ-DP operating in SWD mode, where it is necessary to operate that trace port in normal or bypass mode, but also necessary to communicate with the same target using JTAG.

Table A-5 10-way connector for SWD and JTAG

Pin name	20-way pin number	Mictor pin number
Vref+Cap	1	12
SWDIO	2	17
GND	3	-
SWCLK	4	15
GND	5	-
SWO/EXTa	6	11
(key)	7	-
NC/EXTb	8	19

Table A-5 10-way connector for SWD and JTAG (continued)

Pin name	20-way pin number	Mictor pin number
GND(1)	9	-
TraceCtl	10	36
Gnd/TgtPwr+Cap	11	-
TraceClk	12	6
Gnd/TgtPwr+Cap	13	-
TraceD0	14	38
GND	15	-
TraceD1	16	28
GND	17	-
TraceD2	18	26
GND	19	-
TraceD3	20	24

Table A-6 shows the 20-way header for targets using JTAG for debug communication, that do not require an **nRESET** signal. This layout is typically used in a CoreSight system including a JTAG-DP, where it is necessary to operate that trace port in normal or bypass mode, or a system with a SWJ-DP operating in JTAG mode, possibly because it is cascaded with other JTAG TAPs.

A target board might use this layout for performing board-level boundary scan, but then switch its SWJ-DP into SWD mode for debugging according to the layout shown in Table A-5 on page A-7. This frees up pins 6 and 8 for either application functions or SWO.

Table A-6 10-way connector for JTAG

Pin name	20-way pin number	Mictor pin number
Vref+Cap	1	12
TMS	2	17
GND	3	-

Table A-6 10-way connector for JTAG (continued)

Pin name	20-way pin number	Mictor pin number
TCK	4	15
GND	5	-
TDO	6	11
(key)	7	-
TDI	8	19
GND(1)	9	-
TraceCtl	10	36
Gnd/TgtPwr+Cap	11	-
TraceClk	12	6
Gnd/TgtPwr+Cap	13	-
TraceD0	14	38
GND	15	-
TraceD1	16	28
GND	17	-
TraceD2	18	26
GND	19	-
TraceD3	20	24

Connector pinouts for future systems

Table A-7 shows the 20-way header for targets using SWD for debug communication, and includes an optional **SWO** signal for conveying application/instrumentation trace. Alternatively, a target trace port operating in CoreSight normal or bypass modes might convey the TraceCtl signal on pin 6.

Both pin 6 and pin 8 are shown with alternative extra signals, **EXTa** and **EXTb**. This enables flexibility to communicate other signals on these pins. For example, future target systems and trace equipment might convey two further trace data signals on these pins. This layout is typically used in a CoreSight system that uses a SWJ-DP operating in SWD mode.

Table A-7 20-way connector for future SWD systems

Pin name	20-way pin number	Mictor pin number
Vref+Cap	1	12
SWDIO	2	17
GND	3	-
SWCLK	4	15
GND	5	-
SWO/EXTa/TraceCtl	6	11
(key)	7	-
NC/EXTb	8	(19)
GND(1)	9	-
nRESET	10	9
Gnd/TgtPwr+Cap	11	-
TraceClk	12	6
Gnd/TgtPwr+Cap	13	-
TraceD0	14	38
GND	15	-
TraceD1	16	28
GND	17	-

Table A-7 20-way connector for future SWD systems (continued)

Pin name	20-way pin number	Mictor pin number
TraceD2	18	26
GND	19	-
TraceD3	20	24

Table A-8 shows the 20-way header for targets using JTAG for debug communication. This layout is typically used in a CoreSight system including a JTAG-DP, or one with a SWJ-DP operating JTAG mode, possibly because it is cascaded with other JTAG TAPs.

A target board might use this layout for performing board-level boundary scan but then switch its SWJ-DP into SWD mode for debugging according to the layout shown in Table A-7 on page A-10. This frees up pins 6 and 8 for either application functions or SWO.

Table A-8 20-way connector for future JTAG systems

Pin name	20-way pin number	Mictor pin number
Vref+Cap	1	12
TMS	2	17
GND	3	-
TCK	4	15
GND	5	-
TDO	6	11
(key)	7	-
TDI	8	19
GND(1)	9	-
nRESET	10	9
Gnd/TgtPwr+Cap	11	-
TraceClk	12	6
Gnd/TgtPwr+Cap	13	-

Table A-8 20-way connector for future JTAG systems (continued)

Pin name	20-way pin number	Mictor pin number
TraceD0	14	38
GND	15	-
TraceD1	16	28
GND	17	-
TraceD2	18	26
GND	19	-
TraceD3	20	24

Note

The pin layout shown in Table A-8 on page A-11 is the recommended debug connection for a processor built with support for instruction trace, that is, including an ETM.

A.2.4 20-way connector pinouts for legacy JTAG connections

Table A-9 shows the 20-way header for targets using legacy JTAG for debug communication. It includes support for adaptive clocking where the communication rate is throttled by the debug equipment waiting for each **TCK** change to be reflected from the target on **RTCK**. It includes an optional **SWO** signal for conveying application and instrumentation trace.

Table A-9 20-way connector for legacy JTAG connections

Pin name	20-way pin number	Mictor pin number
Vref+Cap	1	12
TMS	2	17
GND	3	-
TCK	4	15
GND	5	-
TDO	6	11

Table A-9 20-way connector for legacy JTAG connections (continued)

Pin name	20-way pin number	Mictor pin number
(key)	7	-
TDI	8	19
GND(1)	9	-
nRESET	10	9
Gnd/TgtPwr+Cap	11	-
RTCK	12	13
Gnd/TgtPwr+Cap	13	-
SWO	14	(38)
GND	15	-
nTRST	16	21
GND	17	-
DBGRQ/TrigIn	18	7
GND	19	-
DBGACK/TrigOut	20	8

Appendix B
Deprecated SWJ-DP Switching Sequences

This appendix describes the switching sequences used in earlier versions of the *Serial Wire JTAG Debug Port* (SWJ-DP). It contains the following section:

- *About the deprecated SWJ-DP switching sequences* on page B-2.

B.1 About the deprecated SWJ-DP switching sequences

An earlier version of the SWJ-DP uses different select sequences for switching between JTAG and SWD, and between SWD and JTAG.

The earlier version can be identified as follows:

- the Version field in the DeviceID code of JTAG-DP is `0x1`
- the Version field in the DeviceID code of SW-DP being `0x0`.

Table B-1 shows the deprecated switching sequences.

Table B-1 Deprecated switching sequences

Deprecated switching sequence	MSB first	LSB first
JTAG to SWD	0110110110110111 or 16'h6DB7	16'hEDB6
SWD to JTAG	0111010101110101 or 16'h7575	16'hAEAE