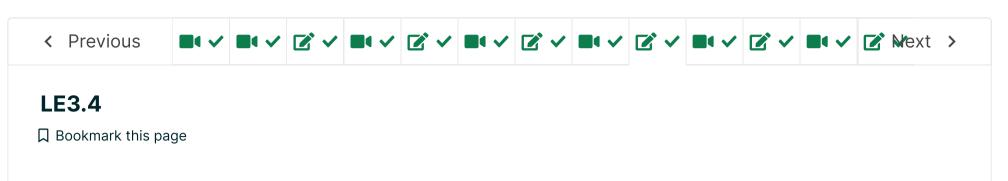
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★ Course / 3. CMOS / Lecture Videos (44:58)

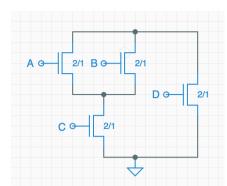




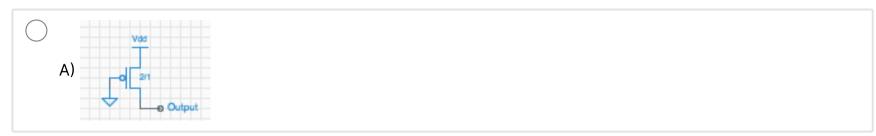
LE3.4.1: Complementary circuits

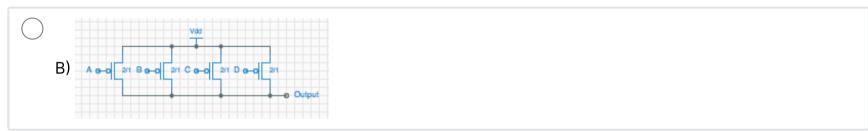
1/1 point (ungraded)

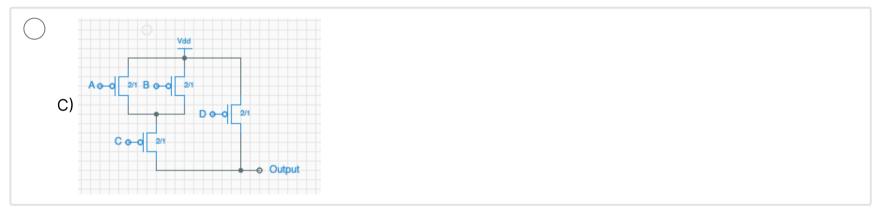
The following diagram shows a schematic for the pulldown circuitry for a particular CMOS logic gate.

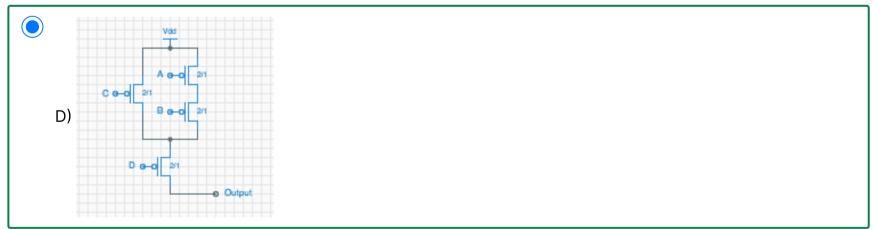


Which of the following would be the most likely schematic for the pullup circuitry?









E) None of the above



Submit

LE3.4.2: CMOS Recipe

1/1 point (ungraded)

A single 3-input CMOS logic gate computes F(A,B,C). Its circuit has the property that every mosfet's gate is connected to one of A, B, or C. Which logic function might it compute?

 \bigcirc A) $oldsymbol{A} \cdot oldsymbol{B} \cdot oldsymbol{C}$

 \bigcirc B) $A+B\cdot C$

⊞ Calculator

● E) <i>AE</i>	\overline{SC}		
F) Nor	ne or several of the abov	ve (or can't tell)	
~			
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