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## ★ Course / 15. Pipelining the Beta / Tutorial Problems

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Pipelined Beta: 1

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■ Calculator

For all Beta related questions, you should make use of the <u>Beta documentation</u>, the <u>Beta Instruction Summary</u>, the <u>Unpipelined Beta Diagram</u> and the <u>Pipelined Beta Diagram</u>.

## Pipelined Beta: 1

0.0/1.0 point (ungraded)

Assume a 5-stage Beta with full bypass paths, as presented in lecture. Remember that, in the pipelined Beta, the data read by loads becomes available in the writeback stage. Fill in the pipelining diagram below using the command names (e.g., LD, ST) that live in each stage. If no operation happens in a particular slot, enter the word EMPTY. In steady state, how many cycles does this code consume in the pipelined Beta?

	LD(R0,0,R2)			
	LD(R1,0,R3) ST(R2,0,R1)			
	ST(R3,0,R0)			
	0	1	2	3
			_	
IF				
••				
RF				
•				
EXE				
MEM				
WB				
If this	code was executed repeatedl	y, how many cycles would it ta	ike in steady state?	
Numbe	er of Cycles in Steady State:			
		WAP(Ra, literal, Rc), was added	d to the Beta. SWAP swaps a r	egister value and
a mem	ory location The behavior of	this instruction is as follows:		

```
tmp <-- Mem[Reg[Ra] + SEXT(literal)]
Mem[Reg[Ra] + SEXT(literal)] <-- Reg[Rc]
Reg[Rc] <-- tmp</pre>
```

Using this new instruction, the code sequence above can be rewritten as:

```
LD(R0,0,R2)
SWAP(R1,0,R2)
ST(R2,0,R0)
```

Assume that the SWAP instruction is implementable in the fully bypassed 5-stage Beta, and also returns data in the writeback stage. Fill in the pipelined timing diagram as above. Remember that SWAP(Ra,literal,Rc) reads and writes Rc (in the register file and writeback stages, respectively).

IF					
RF					
EXE					
MEM					
WB					
If this code	was executed repeate	edly, how many cycle	s would it take in steady	/ state?	
Number of	Cycles in Steady State	:			
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Submit					
Submit					
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