



< Previous



Next >

WE5.2

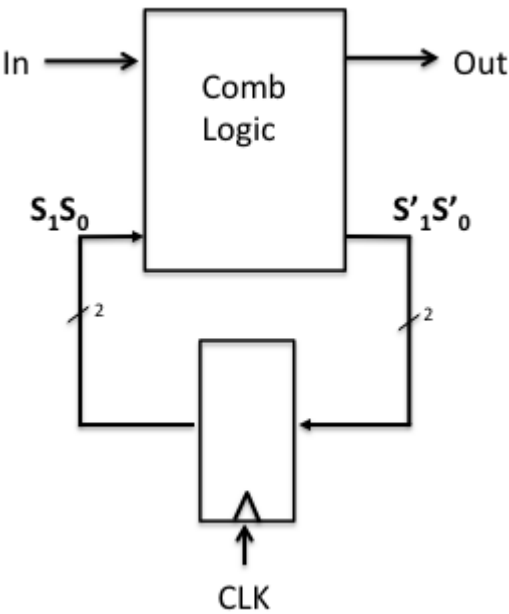
🔖 Bookmark this page

Sequential Logic Timing

4/4 points (ungraded)

OpenFSM.org, an organization dedicated to public disclosure of the transition diagrams of all commercially interesting FSMs, has hired you as an (unpaid) consultant. They’ve asked you to help reverse-engineer the BSM, an FSM embedded in the hot-selling consumer product, BlingSox.

You’ve been given the schematic diagram for the BSM below, and immediately recognize the diagram as an FSM having two state bits held in a single register.



OpenFSM has somehow been able to determine certain component timing specifications, listed below, but has been unable to come up with specifications for the BSM device as a whole. Moreover, they could not determine the hold time spec for the register.

Combinational Logic		Register	
t _{PD}	11ns	t _{PD}	1ns
t _{CD}	0.1ns	t _{CD}	0.1ns
		t _{SETUP}	6ns
		t _{HOLD}	???

Nick O’Tyme, OpenFSM’s performance expert, has asked you to find boundary values for timing specs that just guarantee reliable operation of the BSM.

What is the largest value for the register’s hold time that allows the necessary timing specifications to be met?

Largest valid value for t_{HOLD} (ns): ✓

What is the smallest value for the period of CLK that will meet the timing specifications?

Smallest value for t_{CLK} (ns): ✓

Give the smallest setup and hold time specifications on IN with respect to the active edge of CLK that ensures the necessary timing specifications are met. **Assume that the t_{HOLD} spec for the register is 0.1ns.**

Setup time (ns): ✓

Hold time (ns): ✓

Submit

Sequential Logic Timing

Combinational Logic	
t _{pD}	3ns
t _{CD}	0.2ns

Register	
t _{pD}	5ns
t _{CD}	0.1ns
t _{SETUP}	2ns
t _{HOLD}	???

$$t_{\text{HOLD}} \leq t_{\text{CD,register}} + t_{\text{CD,logic}}$$
$$t_{\text{HOLD}} \leq 0.1 + 0.2 = 0.3\text{ns}$$

(Caption will be displayed when you start playing the video.)

▶ 0:00 / 0:00

▶ 1.0x

🔊

🔍

📺

🗣️

Video

[Download video file](#)

Transcripts

[Download SubRip \(.srt\) file](#)

[Download Text \(.txt\) file](#)

Discussion

Topic: 5. Sequential Logic / WE5.2

Hide Discussion

Add a Post

Show all posts

by recent activity

?

[Can,t tsetup\(input\) be reduced by tcd,L?](#)

Can,t tsetup(input) be reduced by tcd,L? I understand that it takes 11ns so that signal of the logic will be valid and the signal has to s...

3

✓

[tHOLD,register](#)

Why is tHOLD,register <= tCD,register + tCD,logic?

6

💬

[\[STAFF\] Does hold time can actually be negative?](#)

Sorry for discussing answers (well, this is WE...), but is that really possible? Of course, it's mathematically true, but is it physically tru...

4

< Previous

Next >

© All Rights Reserved

Calculator

https://learning.edx.org/course/course-v1:MITx+6.004.1x_3+3T2016/block-v1:MITx+6.004.1x_3+3T2016+type@sequential+block@c9s2/block-v1:MITx+6.004.1x_3+3T2016+type@vertical+block@c9s2v2

3/4

edX

- [About](#)
- [Affiliates](#)
- [edX for Business](#)
- [Open edX](#)
- [Careers](#)
- [News](#)

Legal

- [Terms of Service & Honor Code](#)
- [Privacy Policy](#)
- [Accessibility Policy](#)
- [Trademark Policy](#)
- [Sitemap](#)

Connect

- [Blog](#)
- [Contact Us](#)
- [Help Center](#)
- [Media Kit](#)
- [Donate](#)



© 2021 edX Inc. All rights reserved.
深圳市恒宇博科技有限公司 [粤ICP备17044299号-2](#)