LE5.2

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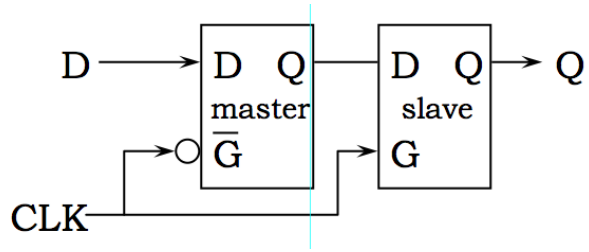
LE5.2.1 D-register Timing

5/5 points (ungraded)

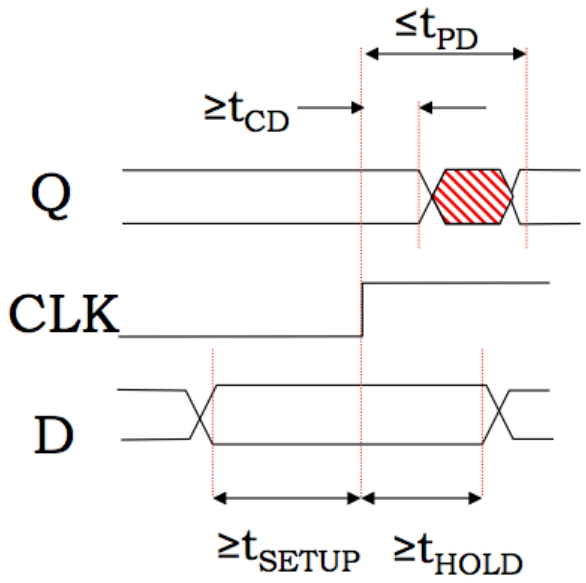
A D-register is constructed from two D-latches according to the schematic shown below.



The timing specifications for the master and slave latches are shown below.

	Master	Slave
t_{PD}	0.90 ns	1.30 ns
t_{CD}	0.17 ns	0.20 ns
t_{SETUP}	0.91 ns	0.82 ns
t_{HOLD}	0.20 ns	0.13 ns

Please determine the appropriate timing specifications for the register, selecting values for $t_{CD}, t_{PD}, t_{SETUP}, t_{HOLD}$, shown in the following figure.



Register contamination delay t_{CD} (ns): 0.2 ✔

Register propagation delay t_{PD} (ns): 1.3 ✔

Register setup time t_{SETUP} (ns): 0.91 ✔

Register hold time t_{HOLD} (ns): 0.2 ✔

Suppose we're able to choose a faster time for the contamination delay t_{CD} for the master latch. What would be the smallest possible time we could choose and still have the register work correctly?

Smallest possible t_{CD} for master latch (ns): 0.13 ✔

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☑	Last question Why should the contamination delay of the master latch be greater than or equal to the hold time of the slave latch?	5
☑	D Latch Time specifications in LE5.2.1 I'm confused about the specification chart provided for this question. As we've seen, in a latch, Tsetup is equal to two times Tpd and ...	8
?	Propagation Delay Propagation delay is defined as the delay from valid input to a valid output. When we consider a d register the input propagates thro...	2
💬	Tsetup and Thold ? Hello , In the Question above we have considered the set up and hold times of the circuit equivalent to that of master latch ..is it bec...	3
💬	slave register's tsetup I dont get something. In the rising edge of the clock the contamination delay of the máster latch must satisfy the thold of the slave. ...	4

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