LE16.2

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LE 16.2.1: Page faults galore!

0.0/1.0 point (ungraded)

1. A particular Beta implementation has 32-bit virtual addresses, 32-bit physical addresses and a page size of $\mathbf{2^{12}}$ bytes. A test program has been running on this Beta and has been halted *just before* execution of the following instruction at location 0×1FFC:

```
LD(R31,0x34C8,R1) | PC = 0x1FFC
ST(R1,0x6004,R31) | PC = 0x2000
```

The first 8 locations of the page table at the time execution was halted are shown below; the least recently used page ("LRU") and next least recently used page ("next LRU") are as indicated. Assume that all the pages in physical memory are in use. Execution resumes and the LD and ST instructions are executed.

VPN	D	R	PPN
0	1	1	0×1
1	0	1	0×0
LRU→2	1	1	0×6
3	--	0	--
Next LRU→4	0	1	0×4
5	0	1	0×2
6	0	1	0×7
7	0	1	0×3

Please **fill in the contents of the page table** after the ST instruction has completed execution. For resident pages set R = 1 and indicate whether the dirty (D) bit is a 0 or a 1. For the PPN enter the physical page number in hex. **If a virtual page is removed from memory, indicate that by setting R = 0 and setting the dirty bit and the PPN to "--"**.

VPN	D	R	PPN
0	Select an option	Select an option	0x:
1	Select an option	Select an option	0x:
2	Select an option	Select an option	0x:
3	Select an option	Select an option	0x:
4	Select an option	Select an option	0x:
5	Select an option	Select an option	0x:
6	Select an option	Select an option	0x:
7	Select an option	Select an option	0x:

2. Which physical pages, if any, needed to be written to disk during the execution of the LD and ST instructions?
Physical page numbers written to disk or NONE:

- [ ] 0×0
- [ ] 0×1
- [ ] 0×2

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- [ ] 0×3
- [ ] 0×4
- [ ] 0×5
- [ ] 0×6
- [ ] 0×7
- [ ] NONE

3. Please give the 32-bit physical memory addresses used for the four memory accesses associated with the execution of the LD and ST instruction.

32-bit physical memory address of LD instruction: 0x

32-bit physical memory address of data read by LD: 0x

32-bit physical memory address of ST instruction: 0x

32-bit physical memory address of data written by ST: 0x

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