

<u>Help</u>

selfpoised ~

<u>Course Progress Dates Course Notes Discussion</u>



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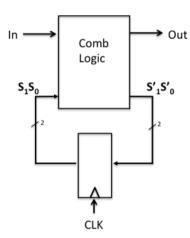
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FSM

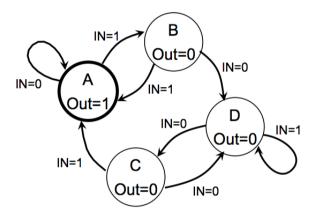
6/6 points (ungraded)

OpenFSM.org, an organization dedicated to public disclosure of the transition diagrams of all commercially interesting FSMs, has hired you as an (unpaid) consultant. They've asked you to help reverse-engineer the BSM, an FSM embedded in the hot-selling consumer product, BlingSox.

You've been given the schematic diagram for the BSM, as shown below, and immediately recognize the S1S0 diagram as an FSM having two state bits held in a single register.



Through a series of tedious experiments, you deduce the state transition diagram for the BSM as shown below.



You have verified that the BSM has four states, that it is a Moore machine (the output is a function only of the current state), and have determined the value of the output for each of the four states. You have also determined that the current state is encoded as two state variables S1S0 stored in the two-bit register shown in the circuit diagram above, and that A is the initial state.

Further reverse engineering on your part yields the partially-completed truth table for the BSM's combinational logic shown below. Unfortunately, you left five blank entries in the table. At the time you made the table, their values seemed too obvious to bother writing down; a week later, however, they didn't seem quite so obvious.

(A) Fill in the missing five entries in the table below.

S1	SO	IN	S1'	SO'		оит
0	0	0	0	0		1
0	0	1	0	1		1
0	1	0	1	0		0
0	1	1	0	0	~	0
1	0	0	1	1		0
1	0	1	1	0	~	0
1	1	0	1	0		0
1	1	1	0	0	~	0

After you show your progress to your OpenFSM buddies, they ask if you can tell from that diagram whether it might be possible to find a 3-state machine that is equivalent to the 4-state BSM.

⊞ Calculator

Worked Examples | 6. Finite State Machines | Computation Structures 1: Digital Circuits | edX equivalent states that may be merged to yield the simpler FSM; otherwise, mark NO. NO Α **✓** B ✓ C D Submit **FSM Implementation FSM Implementation** S0 IN S1' S0' OUT 0 0 В 0 0 Out=0 IN=0 0 0 0 0 A Out=1 D 0 0 0 IN=0 IN=1 Out=0 0 0 0 IN=1 C Out=0 0 IN=0 (Caption will be displayed when you start playing the video.) 0 0 0:00 / 0:00 ▶ 1.0x X CC Video **Transcripts** Download SubRip (.srt) file Download video file Download Text (.txt) file Discussion **Hide Discussion** Topic: 6. Finite State Machines / WE6.2 **Add a Post** Show all posts by recent activity ~ <u>▼ Benefit of merging states?</u> 2 Hello, We see from the lecture that we get two states merged as one leaving behind a total of 3 states instead of 4 But for both 3,4 ... **⊞** Calculator Shouldn't the answer to the second column be 0?

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