LE6.4

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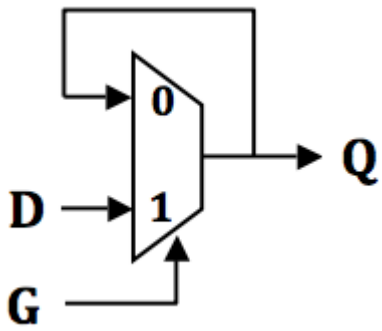
LE6.4.1 Metastability in latches

6/6 points (ungraded)



Assume that we have made a transparent latch using a lenient 2-input MUX as shown above. The lenient MUX has a propagation delay of t_{PD} and a contamination delay of t_{CD}.

A certain sequence of inputs -- violating the dynamic discipline -- has caused the Q output to assume an invalid voltage. You have observed the voltage at Q at this value for an interval many times larger than t_{PD}, despite valid stable inputs at D and G during this interval.

For each of the following statements, please indicate either TRUE or FALSE, assuming you are observing an invalid Q output after this relatively long interval of valid D and G inputs.

(A) The G input must be 0.

- (●) True
- ( ) False

✔

(B) The D input must be 1.

- ( ) True
- (●) False

✔

(C) Setting and holding G=1 (while D remains valid and stable) will assure a stable value at Q after a delay of t_{PD}.

- (●) True
- ( ) False

✔

(D) Setting and holding G=1 for t_{PD} and returning it to 0 for another t_{PD} (while D remains valid and stable) will assure that the value at D appears at Q.

- ( ) True
- (●) False

✔

(E) If the inputs remain unchanged (stable and valid) for an interval of T seconds, the probability of a valid Q output at the end of this interval increases exponentially with T.

- (●) True
- ( ) False

Calculator

False

✔

(F) Assuming the valid stable inputs remain at D and G, once Q leaves the metastable state and reaches a valid logic level it is guaranteed to have the same value as D.

- True
- False

✔

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- Increasing exponentially — 3
- Why D false? — 3
  Hello, Can you explain why we need G=1 for 2*t_pd and not single t_PD to guarantee propagation of D to Q? **" If G had been 1 for 2...

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