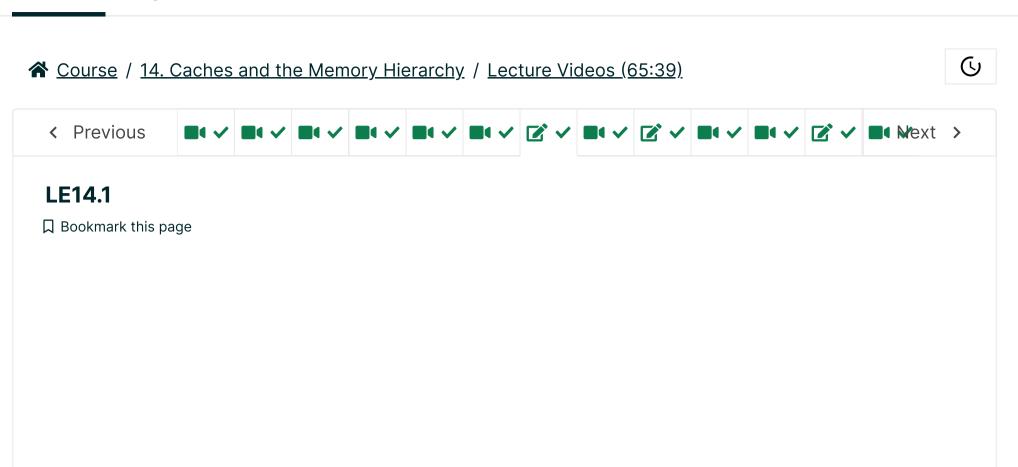


<u>Help</u>

selfpoised >

<u>Course</u> <u>Progress</u> <u>Dates</u> <u>Discussion</u>



LE14.1.1 Average Memory Access Time

1.0/1.0 point (ungraded)

A particular cache design responds in 1 cycle on a cache hit, but takes an *additional* 20 clock cycles if there's a cache miss. If we want an average memory access time of 2 cycles or better, what is the minimal acceptable cache hit ratio?

