



< Previous

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

Next >

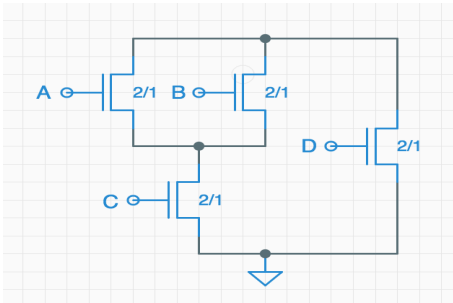
LE3.6

🔖 Bookmark this page

LE3.6.1: Leniency

1/1 point (ungraded)

The following diagram shows a schematic for the pulldown circuitry for a particular CMOS logic gate.



Assuming the pullup circuitry is designed correctly, is the CMOS gate above lenient?

☒ Yes

☐ No

☐ Not enough information to tell



Submit

Discussion

Hide Discussion

Topic: 3. CMOS / LE3.6

Add a Post

Show all posts ▾

by recent activity ▾

- ?

Where is the output located?

I have come across a few diagrams like this one which has only inputs and GROUND displayed without the output point. And I find thi...

3
- 💬

lenient

I know the definition of the lenient, but I still not understand why "a glitch-free output using a minimal number of required inputs" is I...

5

< Previous

Next >



edX

- [About](#)
- [Affiliates](#)
- [edX for Business](#)
- [Open edX](#)
- [Careers](#)
- [News](#)

Legal

- [Terms of Service & Honor Code](#)
- [Privacy Policy](#)
- [Accessibility Policy](#)
- [Trademark Policy](#)
- [Sitemap](#)

Connect

- [Blog](#)
- [Contact Us](#)
- [Help Center](#)
- [Media Kit](#)
- [Donate](#)



© 2021 edX Inc. All rights reserved.
深圳市恒宇博科技有限公司 [粤ICP备17044299号-2](#)