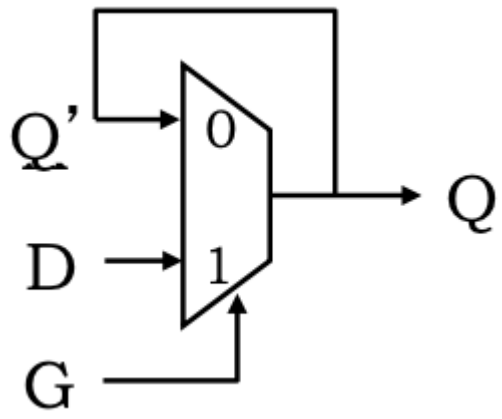
LE5.1

Bookmark this page

LE5.1.1 D-latch Timing

4/4 points (ungraded)

A D-latch is constructed from a lenient MUX according to the schematic shown below.



The MUX has a propagation delay of 1.6ns and a contamination delay of 0.2ns. Please determine the appropriate timing specifications for the latch.

Latch contamination delay (ns): 0.2

Latch propagation delay (ns): 1.6

Latch setup time (ns): 3.2

Latch hold time (ns): 1.6

Submit

Discussion

Topic: 5. Sequential Logic / LE5.1

Hide Discussion

Add a Post

Show all posts by recent activity

Does latch hold and setup time depends only on Tpd ? 4

As according to the question, we wait for 2Tpd for setup and Tpd for hold time . (We are only thinking for when d input is valid and st...

edX

About
Affiliates
edX for Business
Open edX
Careers
News

Legal

Terms of Service & Honor Code
Privacy Policy
Accessibility Policy
Trademark Policy
Sitemap

Connect

Blog
Contact Us
Help Center
Media Kit
Donate

Calculator