



< Previous

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

 ✓

Next >

## LE14.2

🔖 Bookmark this page

### LE14.2.1 Cache Addresses

1.0/1.0 point (ungraded)

The contents of a small 4-line Direct Mapped cache is shown to the right. Note that some of the leading 0's in the Tag field value are not shown. The cache is part of the Beta's memory system. What is the main memory (byte) address for each of the 32-bit data words held in the cache? Please express the value in hex or write "CAN'T TELL" if the value cannot be determined.

Line #	Tag	Data
3	0×07	0×739F0083
2	0×07	0×73FF012C
1	0×02	0×73FF029E
0	0×10	0×627F0060

Byte address of data word in cache line 0: 0x

✓

Byte address of data word in cache line 1: 0x

✓

Byte address of data word in cache line 2: 0x

✓

Byte address of data word in cache line 3: 0x

✓

Submit

## Discussion


Hide Discussion

**Topic:** 14. Caches and the Memory Hierarchy / LE14.2

Add a Post

Show all posts ▾

by recent activity ▾

-  [Some questions](#) 8
1. What is the meaning of 4-line Directed Mapped Cache? 2. Shouldn't offset be given for the problem?

< Previous

Next >

 Calculator



# edX

- [About](#)
- [Affiliates](#)
- [edX for Business](#)
- [Open edX](#)
- [Careers](#)
- [News](#)

# Legal

- [Terms of Service & Honor Code](#)
- [Privacy Policy](#)
- [Accessibility Policy](#)
- [Trademark Policy](#)
- [Sitemap](#)

# Connect

- [Blog](#)
- [Contact Us](#)
- [Help Center](#)
- [Media Kit](#)
- [Donate](#)



© 2021 edX Inc. All rights reserved.  
深圳市恒宇博科技有限公司 [粤ICP备17044299号-2](#)