LE5.3

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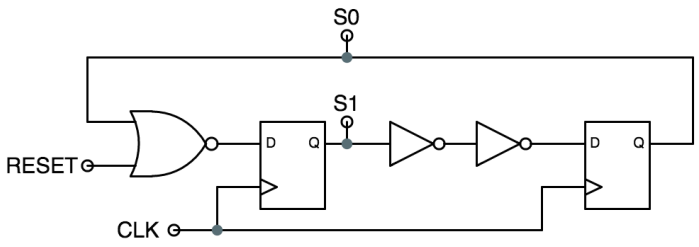
LE5.3.1 Sequential Logic Timing

3/3 points (ungraded)

You are given the sequential circuit and component specs shown below.



Inverter	
t_{pd}	1.7ns
t_{cd}	0.2ns

NOR-2	
t_{pd}	1.9ns
t_{cd}	0.3ns

Register	
t_{pd}	3.5ns
t_{cd}	0.5ns
t_s	1.6ns
t_h	0.4ns

Minimum clock period (ns): 8.5 ✔

Setup time for RESET relative to CLK rising edge (ns): 3.5 ✔

Hold time for RESET relative to CLK rising edge (ns): 0.10000000000000003 ✔

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- Floating point issues — 5
- tH,INPUT — 3
  I still don't understand why tH,INPUT = tH,R - tCD,L.

edX

Calculator