WE5.1

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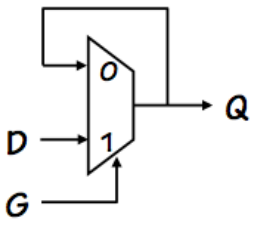
Latch Implementation

3/3 points (ungraded)

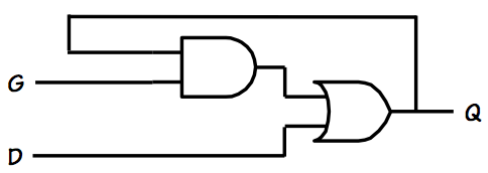
Untel, Inc is a startup exploring a new gate technology that has hired you as a consultant. They have learned how to make reliable, lenient AND gates, OR gates, and inverters, but don't yet have a cell library offering devices like multiplexors. Their current crisis, for which they need your help, is the design of a reliable latch.

The Untel engineers vaguely remember a 6.004 lecture showing how to make a latch using a lenient multiplexor (as shown below), and reason that they can make a latch at least as good starting from AND/OR/inverter logic.

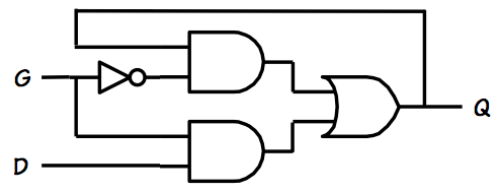


There are three different proposals being considered:

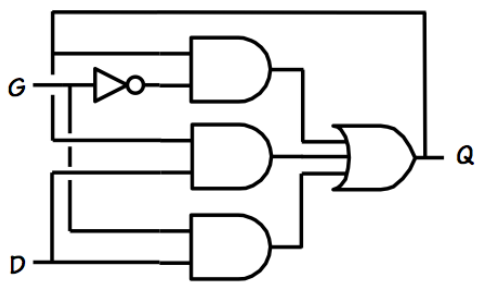
Proposal A



Proposal B



Proposal C



The Untel CTO shows you the diagrams, and asks you characterize each as

- BAD, meaning it doesn't work reliably;
- GOOD, meaning that it works reliably (given appropriate dynamic discipline rules); or
- OBESE, meaning that it works but uses more gates than necessary

Characterize each of the above proposals.

Proposal A

- (●) BAD
- ( ) GOOD
- ( ) OBESE

✔

Proposal B

- (●) BAD
- ( ) GOOD

Calculator

OBESE

Proposal C

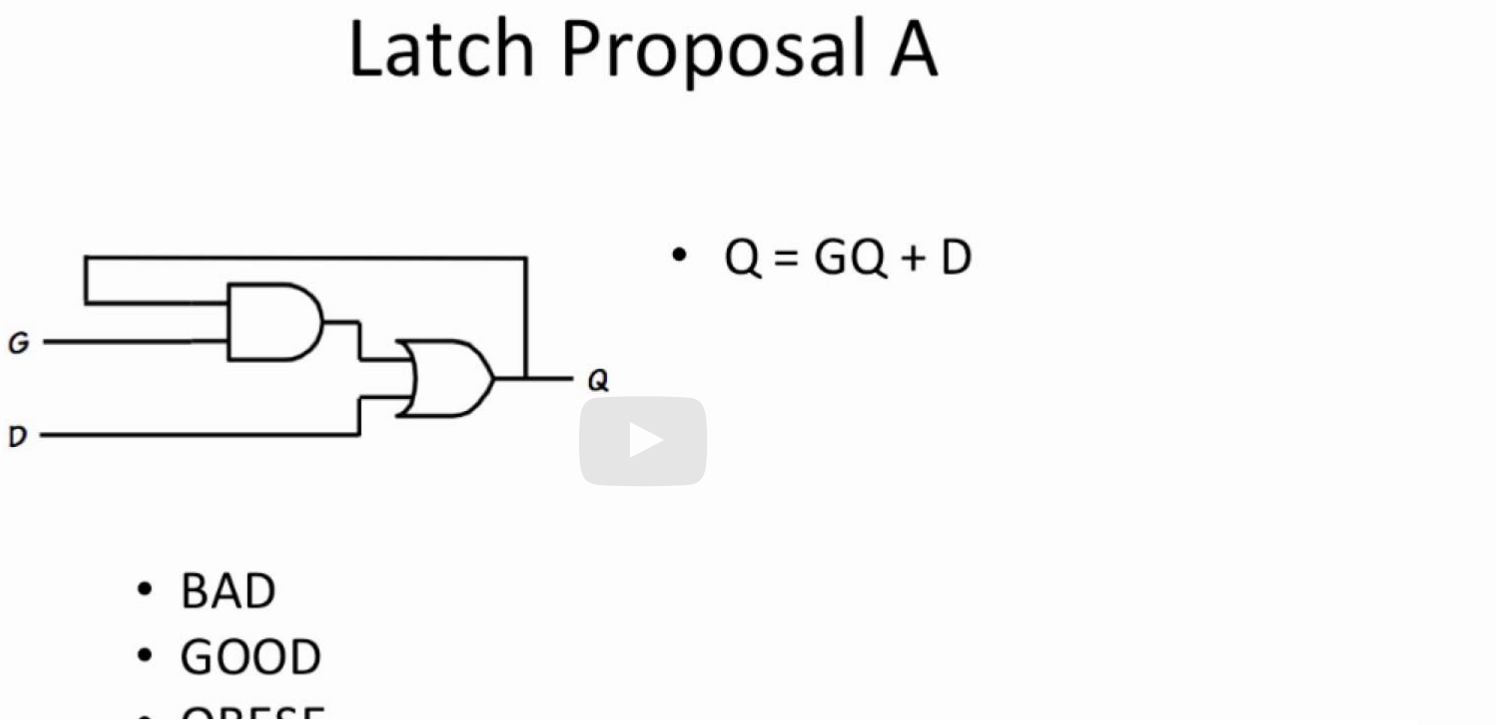
BAD

GOOD

OBESE

Submit

Latch Implementation



(Caption will be displayed when you start playing the video.)

0:00 / 0:00 1.0x

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method to come up with lenient circuit? 3
Unfortunately, the video does not explain why proposal B is not lenient, but simply states so. My understanding was that the minimal...

Calculator

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