WE7.2

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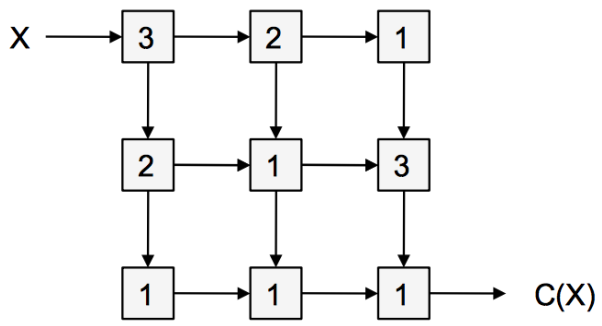
Video explanation of solution is provided below the problem.

Pipelining

7/7 points (ungraded)

The RIAA has come up with a new media encryption engine called the Piper, consisting of nine combinational modules connected as shown to the right.



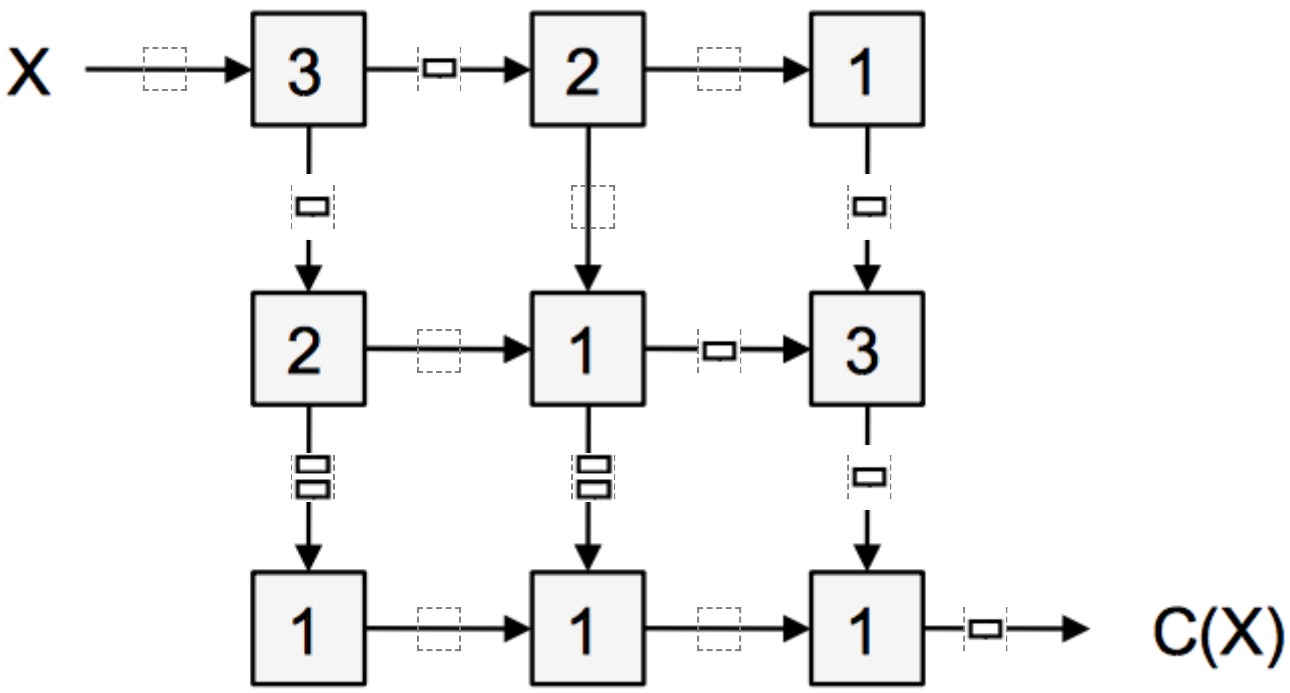
The device takes a music sample X and computes an encrypted version C(X). In the diagram to the right each combinational component is marked with its propagation delay in microseconds; contamination delays are zero for each component. Unfortunately, it is too slow.

(A) What are the latency and throughput of the Piper device?

Latency (microseconds): 10 ✔

Throughput (1/microseconds): 1/10 ✔

(B) Show the RIAA how to pipeline the Piper by adding registers to maximize throughput, but achieve the smallest latency that meets the maximum throughput constraint. Using the diagram below indicate the locations for ideal (zero-delay) registers to create a pipelined implementation that meets these goals. Remember that your answer should have a register on the output signal.



✔

(C) What is the latency and throughput of your pipelined implementation?

Latency (microseconds): 12 ✔

Throughput (provide your answer in the form 1/X) (1/microseconds): 1/3 ✔

(D) Suppose you found pipelined replacements for the components marked 3 and 2 that had 3 and 2 stages, respectively, and could be clocked at a 1 microsecond period. Using these replacements and pipelining for maximum throughput, what is the best achievable performance?

Latency (microseconds): 10 ✔

Throughput (provide your answer in the form 1/X) (1/microseconds): 1 ✔

Calculator

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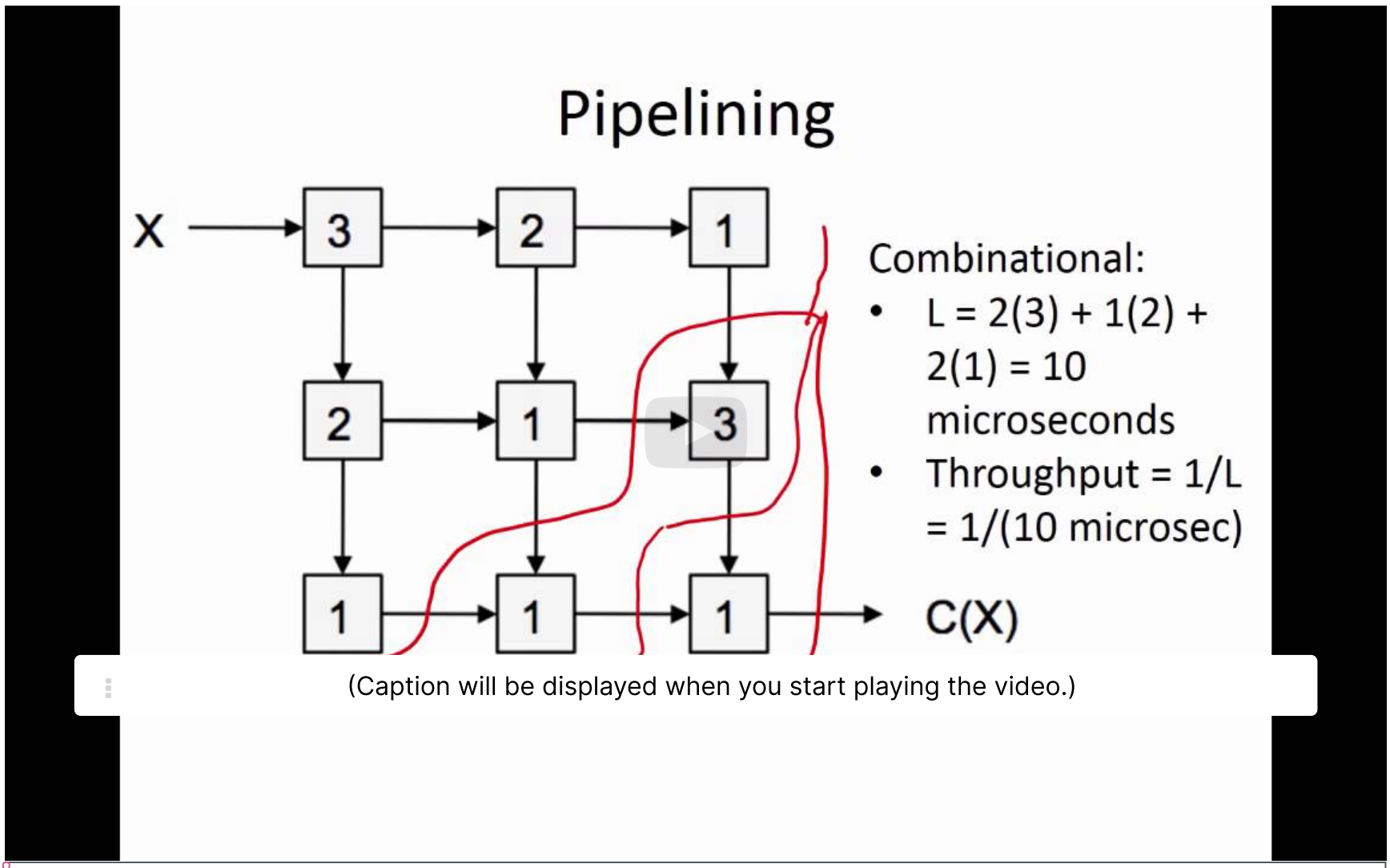
Pipelining 2



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Why isn't the solution below for the pipeline stages correct? 3

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