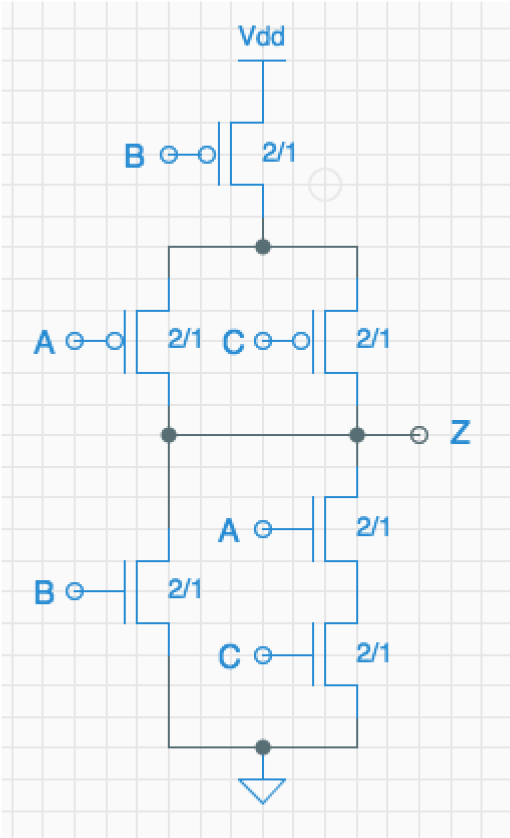
Tutorial : CMOS Continued

CMOS

1/1 point (ungraded)

Given the following cmos gate, determine the function computed by this gate.



- A) $Z = B \cdot (A + C)$
- B) $Z = B + A \cdot C$
- C) $Z = \overline{B} \cdot (\overline{A} + \overline{C})$
- D) $Z = \overline{B} + \overline{A} \cdot \overline{C}$
- E) None of the above

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CMOS

1/1 point (ungraded)

What is the minimum number of NFETs required to build a CMOS circuit (perhaps involving more than one CMOS gate) that has the following truth table?

A	B	C	G
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Calculator

- ( ) A) 3
- ( ) B) 4
- (•) C) 5
- ( ) D) 6
- ( ) E) None of the above

✔

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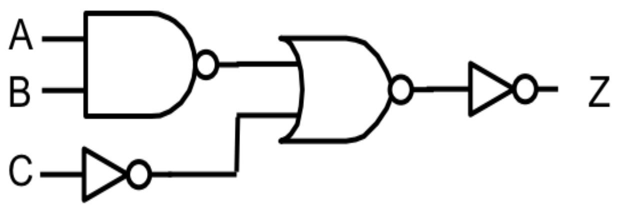
CMOS

2/2 points (ungraded)

Consider the following circuit that implements the 3-input function Z(A,B,C):



Which of the proposals below is the best way to shorten the rise time of the signal at Z?

P1: Add two additional series-connected inverters to the output.
P2: Double the width of the NFET in the output inverter.
P3: Double the width of the PFET in the output inverter.
P4: Halve the width of the NFET in the output inverter.
P5: Halve the width of the PFET in the output inverter.

Best proposal: P3 ✔

Can the function Z(A, B, C) be implemented as a single 3-input CMOS gate having complementary pullup/pulldown circuits?

Implement as a single CMOS gate? YES ✔

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? Why more current causes faster rise time?
I'm not surprised though, but why exactly is that? I don't remember learning it in the course. 2

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