LE13.1

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LE13.1.1 New Load/Store Instructions

1.0/1.0 point (ungraded)

For each of the following potential additions to the Beta instruction set, fill in the table with the control signal settings needed to execute these instructions on an unpipelined Beta. Assume the datapath and control signals as shown at the end of the previous video. Please choose "do not care" if the value of control signal doesn't matter when executing the instruction.

(A) **Swap register contents with memory location**

```
Usage:     MSWP (Ra, literal, Rc)
Operation: PC ← PC + 4
           EA ← Reg[Ra] + SEXT(literal)
           tmp ← Mem[EA]
           Mem[EA] ← Reg[Rc]
           Reg[Rc] ← tmp
```

ALUFN: adder unit: A + B ✔

BSEL: 1 ✔

MOE: 1 ✔

MWR: 1 ✔

RA2SEL: 1 ✔

WDSEL: 2 ✔

WERF: 1 ✔

(B) **Load indexed**

```
Usage:     LDX (Ra, Rb, Rc)
Operation: PC ← PC + 4
           Reg[Rc] ← Mem[Reg[Ra] + Reg[Rb]]
```

ALUFN: adder unit: A + B ✔

BSEL: 0 ✔

MOE: 1 ✔

MWR: 0 ✔

RA2SEL: 0 ✔

WDSEL: 2 ✔

WERF: 1 ✔

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Calculator

☑	Confusion over MSWP 1. How is $temp$ implemented? Another register or data stored in memory? 2. How many clock cycles does $MSWP$ need to finish ex...	4
☑	[STAFF]Assertion of control signals My understanding is that the all the control signals are not asserted at the same time. For eg in questionA MSWP instruction, the LD ...	3

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