WE16.1

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Video explanation of solution is provided below the problem.

Virtual Memory

10 points possible (ungraded)

Apple's iWatch is rumored to include an embedded Beta processor, referred to as the "micro Beta". The micro Beta design includes an MMU (Memory Management Unit) that supports 256 (2^8) bytes per page but only implements a 16-bit virtual address, i.e., the MMU ignores address bits [31:16] coming from the CPU. The MMU and the page fault handler implement an LRU replacement strategy. The design also includes 1M (2^{20}) bytes of physical memory and a large Flash memory that serves as a "disk."

1. Apple's engineers are thinking about implementing the page map using a separate SRAM memory with L entries, where each entry has B bits. If the page map includes the standard dirty and resident bits, what are the appropriate values for the parameters L and B? You can provide your answer in the form "2^N" to express a power of 2.

   Appropriate value for the parameter L:

   Appropriate value for the parameter B:

2. If the engineers decide to increase the page size to 512 (2^9) bytes but keep the same size virtual and physical addresses, what affect will the change have on the following architectural parameters?

   Size of page map entry in bits:

   - ◯ doubled
   - ◯ increased by 1
   - ◯ stays the same
   - ◯ decreased by 1
   - ◯ halved

   Number of entries in the page map:

   - ◯ doubled
   - ◯ increased by 1
   - ◯ stays the same
   - ◯ decreased by 1
   - ◯ halved

   Number of accesses to page map to translate a single virtual address:

   - ◯ doubled
   - ◯ increased by 1
   - ◯ stays the same
   - ◯ decreased by 1
   - ◯ halved

Calculator

Back to the micro Beta with 256-byte pages: A test program is run on the micro Beta and halted just before the execution of the two instructions shown below. The first 8 locations of the page table at the time execution was halted are shown in the page map below the code; the least recently used page ("LRU") and next least recently used page ("next LRU") are as indicated. Execution resumes and the following two instructions at locations 0×1FC and 0×200 are executed:

```
        LD(R31, 0x34C, R1)     | PC = 0x1FC
        ST(R1, 0x604, R31)     | PC = 0x200
```

VPN	D	R	PPN
0×0	0	1	0×123
0×1	1	1	0×007
LRU ⟶ 0×2	0	1	0×602
0×3	--	0	--
0×4	1	1	0xACE
next LRU ⟶ 0×5	1	1	0×097
0×6	1	1	0×790
0×7	--	0	--

3. Assume that all the code and data for handling page faults is located on physical page 0. When the micro Beta executes the two instructions above it will access five different physical pages. Please list the five physical page numbers below **in hex**, in the order they are first accessed. Hint: all the page map information you need is shown in the page table.

Addr 1: 0x

Addr 2: 0x

Addr 3: 0x

Addr 4: 0x

Addr 5: 0x

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(Caption will be displayed when you start playing the video.)

Calculator

(Caption will be displayed when you start playing the video.)

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