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LE15.1

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For all Beta related questions, you should make use of the [Beta documentation](#), the [Beta Instruction Summary](#), the [Unpipelined Beta Diagram](#) and the [Pipelined Beta Diagram](#).

LE15.1.1: Data Hazards

0.0/1.0 point (ungraded)
This problem concerns the 5-stage Beta pipeline with full bypass logic.

Consider the execution of the following sequence on the 5-stage pipelined Beta:

```
ADDC(R31, 44, R0)
SUBC(R0, 0, R1)
MULC(R0, 23, R4)
LD(R0, 0, R2)
XORC(R2, 1, R3)
```

For the following questions, we recommend first drawing out the pipeline diagram associated with this problem. Identify all the cycles where the situation described occurs, then check off all the instructions that appear in the RF stage of these cycles. If the situation never occurs, then select "NONE".

1. Are there points in the execution of the sequence when data is bypassed from the **ALU** stage back to the **RF** stage?

☐ ADDC

☐ SUBC

☐ MULC

☐ LD

☐ XORC

☐ NONE

2. Are there points in the execution of the sequence when data is bypassed from the **WB** stage back to the **RF** stage?

☐ ADDC

☐ SUBC

☐ MULC

☐ LD


☐ XORC

☐ NONE

3. Are there points during the execution of the sequence when the pipeline is stalled?

☐ ADDC

☐ SUBC

 Calculator

☐ MULC

☐ LD

☐ XORC

☐ NONE

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💬	[STAFF] please re-phrase questions A and B	4	▼
	Hi staff, These questions A and B were a bit confusing to me. You bypass data from an instruction to another instruction. It wasn't cle...		
✓	Why does the XORC instruction need to stall while It can take data from WB state?	2	▼
	As title. I think the answer of question B which is just I D instruction.		

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