Tutorial : Sequential Logic Timing

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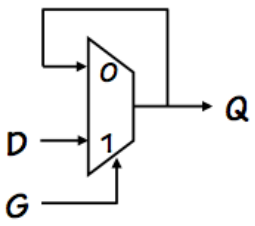
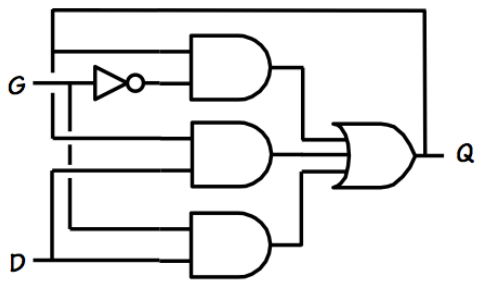
Sequential Logic Timing

2/2 points (ungraded)

In lecture, we saw that one way to impelement a latch is using a lenient multiplexor as shown below.



An alternative way to build a latch is using the following AND/OR/inverter logic which results in a lenient latch implementation.



Determine the minimal setup and hold times for the latch that guarantee its proper operation. While the analysis in lecture derived these specifications from the propagation delay of the multiplexor used there to build the latch, here you must use the propagation delays of the AND/OR/invert gates, each of which is 1 nanosecond. Assume the contamination delay of the gates is zero.

Give appropriate setup and hold time specifications for a latch built using AND/OR/invert components. [HINT: This requires careful analysis!]

Setup Time (ns): 4 ✔

Hold Time (ns): 3 ✔

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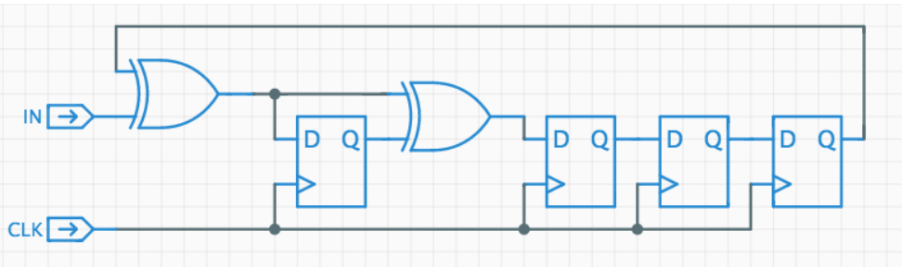
Sequential Logic Timing

4/4 points (ungraded)

A cyclical redundancy check (CRC) is a common technique for detecting errors in a data packet. The sequential circuit below implements a 4-bit CRC:



A) Using the timing specifications shown below for the XOR and DREG components, determine the shortest clock period, t_{CLK}, that will allow the circuit to operate correctly or write NONE if no choice for t_{CLK} will allow the circuit to operate correctly.

$Component$	t_{CD}	t_{PD}	t_{SETUP}	t_{HOLD}
$XOR2$	$0.4ns$	$2.1ns$	–	–
$DREG$	$0.2ns$	$1.8ns$	$0.8ns$	$0.15ns$

Minimum value for t_{CLK} (ns) or NONE if none exists:

6.8 ✔

B) Using the same timing specifications as in (A), determine the setup and hold times for IN with respect to t

Calculator

rising edge of CLK.

t_{SETUP} for IN with respect to CLK↑ (ns): 5 ✔

t_{HOLD} for IN respect to CLK↑ (ns): -0.25 ✔

C) To allow the circuit to run faster, i.e., to achieve a smaller t_{CLK}, the designers are considering replacing the original DREG component with the faster DREG2 which has half the t_{CD} and t_{PD} (see timing specification below). Determine the new shortest clock period, t_{CLK}, that will allow the circuit to operate correctly or write NONE if no choice for t_{CLK} will allow the circuit to operate correctly.

$Component$	t_{CD}	t_{PD}	t_{SETUP}	t_{HOLD}
$DREG2$	$0.1ns$	$0.9ns$	$0.8ns$	$0.15ns$

Minimum value for t_{CLK} (ns) or NONE if none exists:

None ✔

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- T setup for IN — 3
  Why do we not include Tpd reg when calculating T hold for input? The first dreg is clearly not a part of the longest combinational par...
- Propagation delay of 4-bit CRC Circuit — 5
  The propagation delay of the 4-bit CRC circuit is equal to 2*tpd,xor + 4*tpd,dreg or it is need to sum t_setup of each D register too?
- Why can't hold time be 2ns? — 7
  if we take hold time as 2ns i.e. 2ns after G transitions from 1 to 0 i change the value of D then my Q will still be same by the timing an...
- This was unexpected — 3
- Sequential Logic Timing (A) — 4
  i can't understand how can i choose the longest path to calculate propagation delay along any combinational logic path between regi...
- Sequential Logic Timing — 2
  Did not understand why the NOT gate doesn't come into picture while calculating 'setup time'? Please explain
- calculate the timings in sequential device — 3

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