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LE17.1

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LE17.1.1: Interrupts

0.0/1.0 point (ungraded)

1. A busy Beta system spends about half of its CPU cycles servicing interrupts in the OS kernel. For what fraction of these interrupts would you expect the high-order bit of the XP register to be a 1 on entry to the interrupt handler?

☐ 0%

☐ 50%

☐ 100%

2. A JMP instruction is executed on the Beta in Kernel mode. What are the possible values of the high-order PC bit immediately following the JMP?

Select best choice:

☐ only 1

☐ only 0

☐ 1 or 0

3. An interrupt is taken while a Beta is executing application code in a user-mode program. What, if any, register contents of the interrupted application might be changed as a result of this device interrupt?

Select all that apply, or NONE if none apply:

☐ R0

☐ LP

☐ BP

☐ XP

☐ NONE

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