WE15.1

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Video explanation of solution is provided below the problem.

Pipelined Beta

8 points possible (ungraded)

A 5-stage pipelined Beta with full bypassing and annulment of branch delay slots has been running the program below for a while. A snapshot of the execution starting at cycle 1001 is shown in the pipeline diagram.

```
      ...
      CMOVE(0, R1)
LOOP: LD(R1, array, R0)
      ADDC(R1, 4, R1)
      CMPEQ(R0, R1, R2)
      BNE(R2, LOOP, R31)
      ST(R1, index, R31)
      ...
```

Cycle #	1001	1002	1003	1004	1005	1006	1007
IF	LD	ADDC	CMPEQ	BNE	BNE	ST	LD
RF	NOP	LD	ADDC	CMPEQ	CMPEQ	BNE	NOP
ALU	BNE	NOP	LD	ADDC	NOP	CMPEQ	BNE
MEM	CMPEQ	BNE	NOP	LD	ADDC	NOP	CMPEQ
WB	NOP	CMPEQ	BNE	NOP	LD	ADDC	NOP

1. The program reads from registers R0, R1 and R2. In a pipelined processor, sometimes the register contents come from the register file and sometimes from a bypass path. Select all registers whose contents came from the register file at least once during cycles 1001 through 1007.

   Select all registers whose contents are read from register file at least once:

   - [ ] R0
   - [ ] R1
   - [ ] R2

2. Referring to the cycle numbers at the top of the pipeline diagram, please indicate the cycle numbers for which the specified signal had the specified value. Select NONE if the signal did not have that value during any of cycles 1001 through 1007.

   Cycle(s) when STALL was 1:

   - [ ] 1001
   - [ ] 1002
   - [ ] 1003
   - [ ] 1004
   - [ ] 1005
   - [ ] 1006
   - [ ] 1007

Calculator

- [ ] NONE

Cycle(s) when $IRSrc^{IF}$ was not 0:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

Cycle(s) when $IRSrc^{RF}$ was not 0:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

Cycle(s) when $IRSrc^{ALU}$ was not 0:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005
- [ ] 1006

Calculator

- [ ] 1007
- [ ] NONE

Cycle(s) when either bypass was from ALU stage:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

Cycle(s) when either bypass was from MEM stage:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005
- [ ] 1006
- [ ] 1007
- [ ] NONE

Cycle(s) when either bypass was from WB stage:

- [ ] 1001
- [ ] 1002
- [ ] 1003
- [ ] 1004
- [ ] 1005

Calculator

- [ ] 1006
- [ ] 1007
- [ ] NONE

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Pipelined Beta

(Caption will be displayed when you start playing the video.)

0:00 / 0:00 1.0x

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