WE14.2

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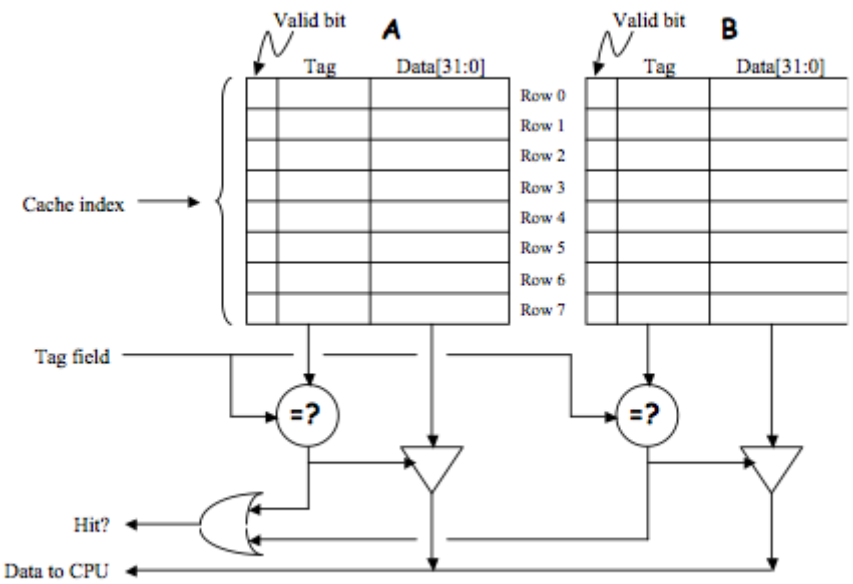
Video explanation of solution is provided below the problem.

Caches

10/10 points (ungraded)

Consider the diagram below for a 2-way set associative cache to be used with our Beta design. Each cache line holds a single 32-bit word of data along with its associated tag and valid bit (0 when the cache line is invalid, 1 when the cache line is valid).



1. The Beta produces 32-bit byte addresses, A[31:0]. To ensure the best cache performance, which address bits should be used for the cache index? For the tag field?

   Address bits used for cache index: A[4 ✔ **:** 2 ✔ **]**

   Address bits used for tag field: A[31 ✔ **:** 5 ✔ **]**

2. Suppose the Beta does a read of location 0×5678. Identify which cache location(s) would be checked to see if that location is in the cache. Select **all** locations that would be checked where 3A, for example, refers to row 3, section A. If there is a cache hit on this access what would be the contents of the tag data for the cache line that holds the data for this location?

   - [ ] 1A
   - [ ] 2A
   - [ ] 3A
   - [ ] 4A
   - [ ] 5A
   - [x] 6A
   - [ ] 7A
   - [ ] 1B
   - [ ] 2B
   - [ ] 3B
   - [ ] 4B
   - [ ] 5B

Calculator

- [x] 6B
- [ ] 7B

✔

Cache tag data on hit for location 0×5678 (hex): 0x 2B3 ✔

3. Assume that checking the cache on each read takes 1 cycle and that refilling the cache on a miss takes an additional 8 cycles. If we wanted the average access time over many reads to be 1.1 cycles, what is the minimum hit ratio the cache must achieve during that period of time? (Enter your response as a fraction X/Y).

   Minimum hit ratio for 1.1 cycle average access time: 7.9/8 ✔

4. Estimate the approximate cache hit ratio for the following program. Assume the cache is empty before execution begins (all the valid bits are 0) and that an LRU replacement strategy is used. Remember the cache is used for both instruction and data (LD) accesses.

```
        . = 0
        CMOVE(source,R0)
        CMOVE(0,R1)
        CMOVE(0x1000,R2)
  loop: LD(R0,0,R3)
        ADDC(R0,4,R0)
        ADD(R3,R1,R1)
        SUBC(R2,1,R2)
        BNE(R2,loop)
        ST(R1,source)
        HALT()

        . = 0x100
source:
        . = . + 0x4000 // Set source to 0x100, reserve 0x1000 words
```

   Approximate hit ratio (Enter your response as a fraction X/Y): 5/6 ✔

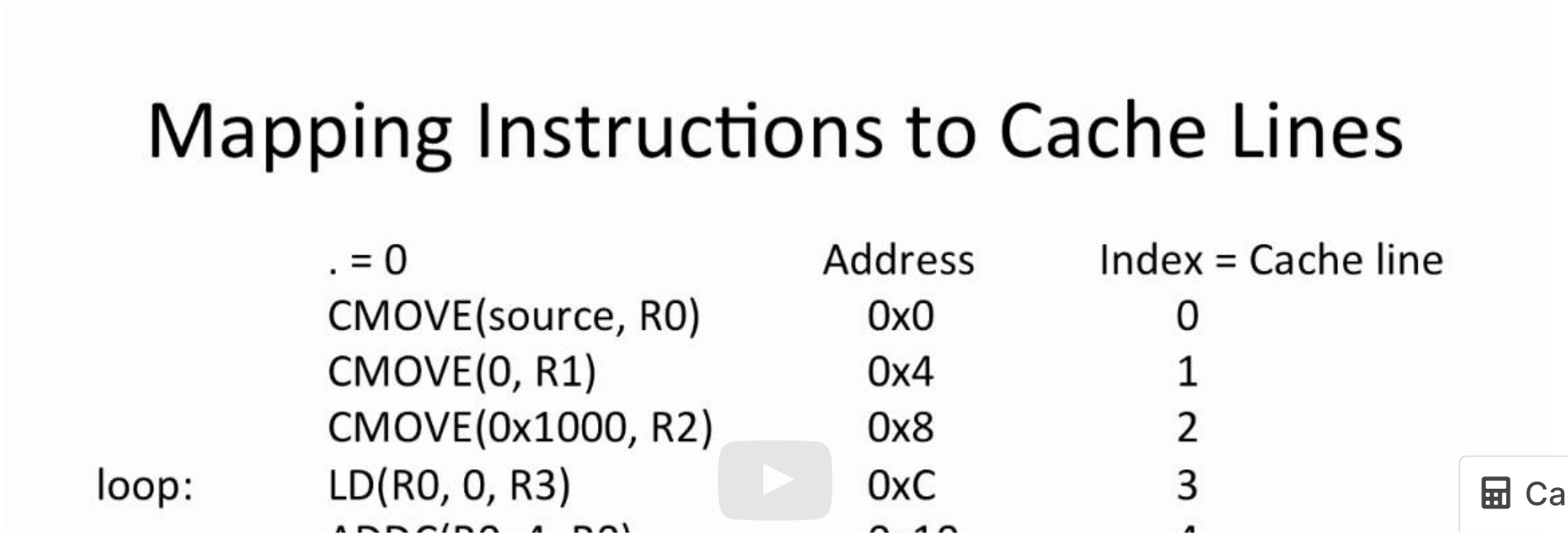
5. After the program of part (D) has finished execution what information is stored in row 4 of the cache? Give the addresses for the instruction word and the data word that are cached (one in each of the sections).

   Address of instruction that is cached in “Row 4”: 0x 10 ✔

   Address of data that is cached in “Row 4”: 0x 40f0 ✔

Submit

Caches



Calculator

ADDC(R0, 4, R0)	0x10	4
ADD(R3, R1, R1)	0x14	5
SUBC(R2, 1, R2)	0x18	6
BNE(R2, loop)	0x1C	7
HALT()	0x24	1

(Caption will be displayed when you start playing the video.)

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In D the hit ratio must be expressed as x/y 3
In D the hit ratio must be expressed as x/y

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