LE7.2

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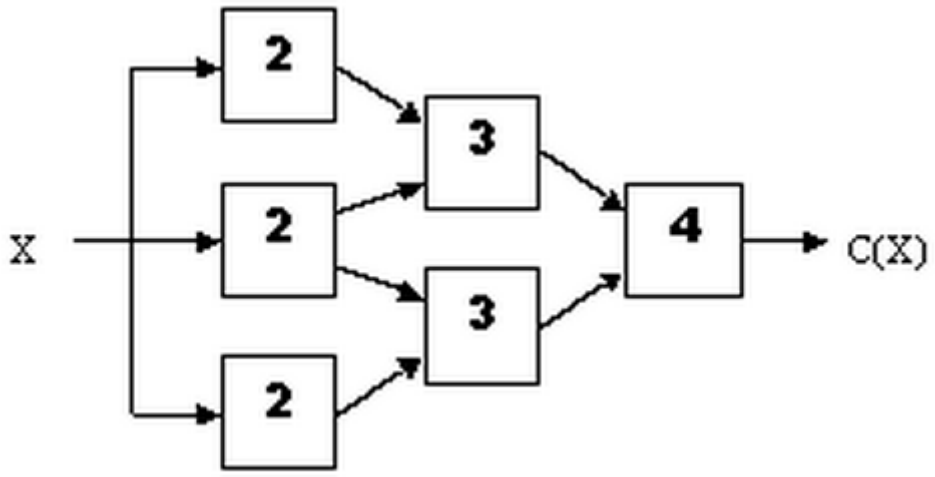
LE7.2.1 Pipeline Design

5/5 points (ungraded)

Consider the following combinational encryption device constructed from six modules:



The device takes an integer value, X, and computes an encrypted version C(X). In the diagram above, each combinational component is marked with its propagation delay in ns; contamination delays are zero for each component.

In answering the following questions assume that registers added to the circuit introduce no additional delays (i.e., the registers have a contamination and propagation delay of zero, as well as zero setup and hold times). Any modifications must result in a circuit that obeys our rules for a well-formed pipeline and that computes the same results as the combinational circuit above. Remember that our pipeline convention requires that every pipeline stage has a register on its output.

(A) What is the latency of the combinational encryption device?

Latency of device (ns): 9 ✔

(B) If we want to increase the throughput of the encryption device, what is the minimum number of registers we need to add?

Minimum number of registers: 3 ✔

(C) If we are required to add exactly 5 registers, what is the best throughput we can achieve?

Maximum throughput (1/ns): 1/5 ✔

(D) If we can add as many registers as we like, what is the upper bound on the throughput we can achieve?

Maximum throughput (1/ns): 1/4 ✔

(E) If we can add as many registers as we like, what is the lower bound on the latency we can achieve?

Minimum latency (ns): 9 ✔

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LE7.2.2 Pipelining Combinational Logic

2/2 points (ungraded)

A combinational circuit C, built entirely from 2-input NAND gates having a propagation delay of 2 ns, has a propagation delay of 20 ns. You pipeline C for maximum throuput using the minimum number of registers necessary; the registers have 1ns setup time and 1ns propagation delay. What would you expect for the late the resulting pipeline?

Calculator

Latency of pipelined version (ns): 40 ✔

Throughput of pipelined version (1/ns): 1/4 ✔

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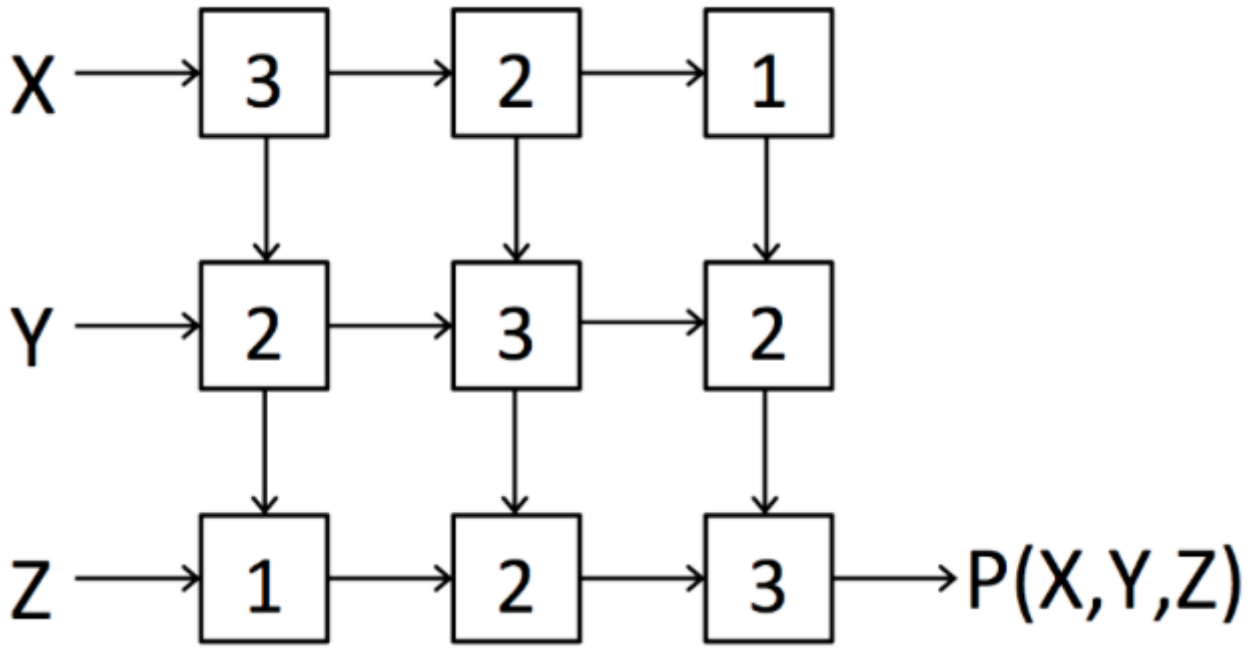
LE7.2.3 Building a Pipeline

5/5 points (ungraded)

The top-secret diagram of the NSA's phone call tracking circuitry is shown below. We don't know what the boxes do, but we do know their t_{PD} (annotated inside each component) and how they are connected.

You've been hired to do a design study looking into pipelining the circuit above. Assume that the pipeline registers have $t_{CD} = 0, t_{PD} = 0, t_{SETUP} = 1, t_{HOLD} = 0$. Recall that using our pipelining convention, each pipelined circuit must have at least 1 register on the P(X,Y,Z) signal.

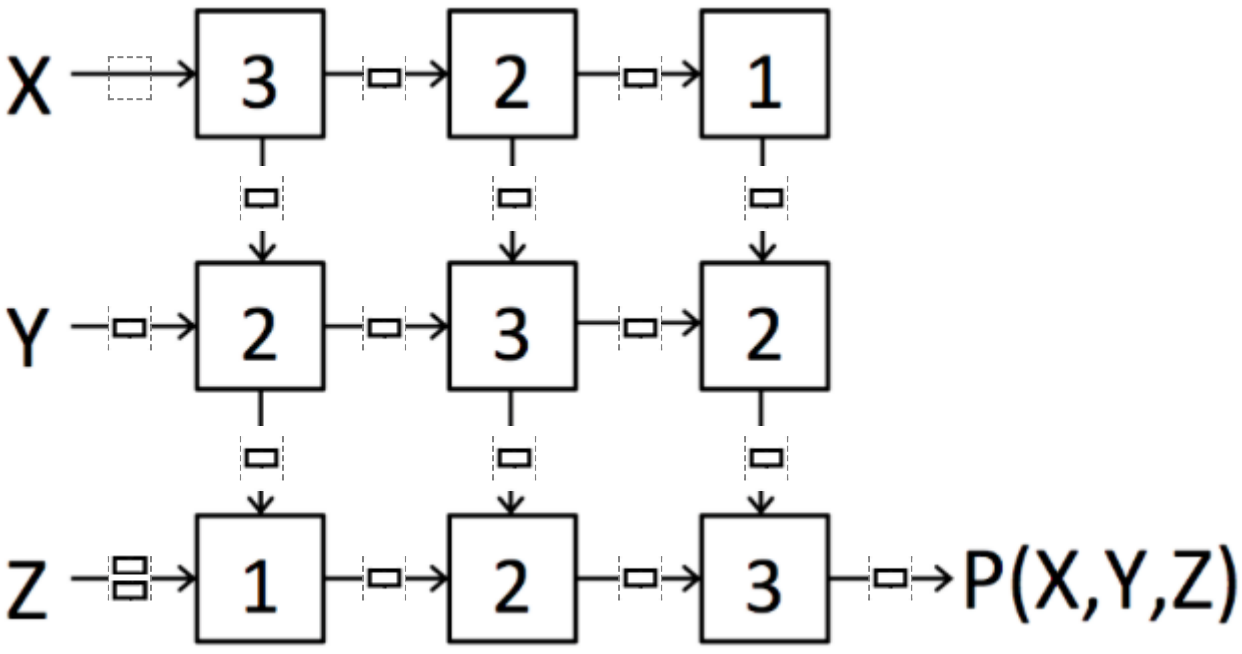


What are the latency and throughput of a 1-pipeline implementation?

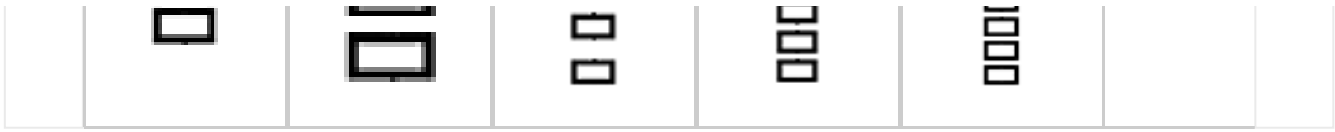
Latency: 14 ✔

Throughput: 1/14 ✔

Add pipeline boundaries to the circuit, choosing the boundaries to achieve maximum throughput. Use the minimum number of registers necessary to achieve this throughput. Provide your answer by dragging the correct number of pipeline registers onto each of the dashed square boxes.



Calculator



What are the latency and throughput of your pipelined circuit?

Latency: 20

Throughput: 1/4

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- If you need help — 2
  Watch this lecture if you need some help regarding methodology of pipelining https://nptel.ac.in/courses/117106114/
- registers on the input of NSA's whatever.. — 2
  I got the question right but this contrary to what we have already learned, i.e we learned not to put registers on the inputs so when ...
- Why is it required to use a register in the final stage output of a pipeline? — 4
  I know it is required to use a register to remember the output in the pipeline middle stage, but why a register is needed in the final ou...
- Note that from every input to output path there must be exactly the same number of pipeline registers for your solution to be valid? — 2
  Why "Note that from every input to output path there must be exactly the same number of pipeline registers for your solution to be v...
- [STAFF] How to calculate tclk and Tpd at various stages of pipelining ? — 2
  I am absolutely confused on how to calculate Tclk and Tpd at various pipelining stages..None of my answers seem to be correct :/ Pl...
- 7.2.1 c and d — 2
- [[STAFF]] No. of reg. in pipelining — 5
  [[STAFF]] I can't figure out how we obtained number of registers during pipeline implementation .... If you can provide me with a mor...
- count — 10
  he best throughput we can achieve with 5 registers is 1/5: place 3 (!) registers on the output and two registers on the arcs leading to ...
- LE7.2.3 Pipelining — 5
- TIS-100 — 2
  The whole thing starts to look a lot like TIS-100 :) I find pipelines to be fairly easy to understand after it.

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Calculator

Calculator