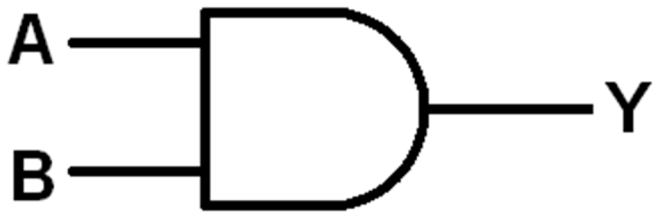
EXPT NO. : 1

To simulate the operation of AND, OR and NAND

AND gate:

This logic gate consists of two input terminal and one output terminal. The working of these gate is such that at output terminal we will get binary 1 if and only if both the input is binary 1. In the case if any of the input has binary zero then the output we got will be binary 0.

The symbol and truth table of AND gate is given below:



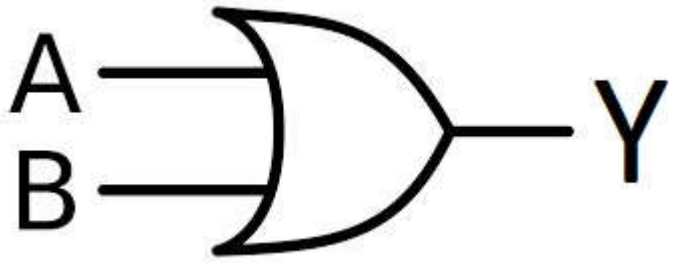
Input		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

The i/o ports needed to be declared for the formation of AND gate is given below:

Port Name	input/output	Bus
A	In	No
B	In	No
Y	Out	No

OR gate:

Likewise, AND gate, OR gate is one of the other fundamental logic gate which has two input terminal and one output terminal. If any of the input is at the low stage i.e. at binary 0 then the output got will be high i.e. binary 1. In case of only both the input is at binary low stage output will be binary low. The symbol and truth table of OR gate is given below:



Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

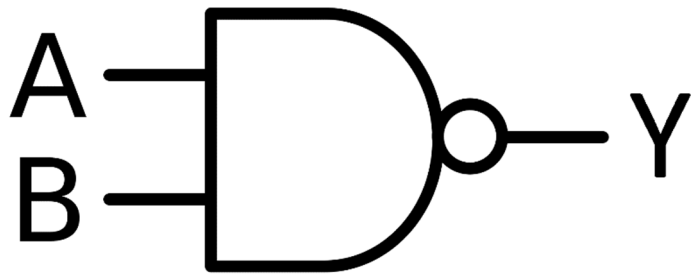
The i/o ports needed to be declared for the formation of OR gate is given below:

Port Name	Input/output	Bus
A	In	No
B	In	No
Y	Out	No

NAND gate:

The NAND gate is just a combination of the expression NOT gate as well as AND gate. Hence the NAND gate is made up of AND gate which is followed by an inverter. The working of these gate is like that we get binary 1 at the output of the gate if and only is both the input is at the binary low state i.e. at 0. While if any of the input terminal is at the binary high i.e. at 1 then the output we got will be binary low state i.e. at 0.

The symbol and truth table of NAND gate is given below:



Input		Output
A	B	Y= $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

The i/o ports needed to be declared for the formation of NAND gate is given below:

Port Name	Input/output	Bus
A	In	No
B	In	No
Y	Out	No

Implementation of NAND gate can be done by two methods:

1. Using the build in **NAND** logical operator.
2. Using a temporary variable. Temporary variable can be declared as given below

   signal temp: STD_LOGIC: = '0';

   Where **signal** is the data type, **temp** is the variable name and the variable has been initialized with value '**0**'.

   The above declaration is made in the **'Behavioral block'** before **'begin'** as shown in the picture below: