EXPT NO. : 5

To simulate the operation of a half-subtractor using basic gates

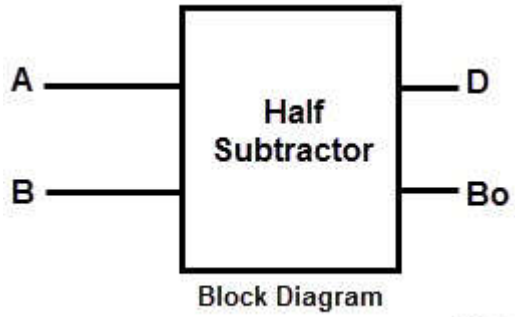
Theory:

A half subtractor is a multiple output combinational logic network that does the subtraction of two bits of binary data. It has input variables and two output variables. Two inputs are corresponding to two input bits and two output variables corresponds to the difference bit and borrow bit.

The binary subtraction is also performed by the Ex-OR gate with additional circuitry to perform the borrow operation. Thus, a half subtractor is designed by an Ex-OR gate including AND gate with the A input complemented before feeding into the gate.

$$D = A \oplus B, B_0 = A' \cdot B$$

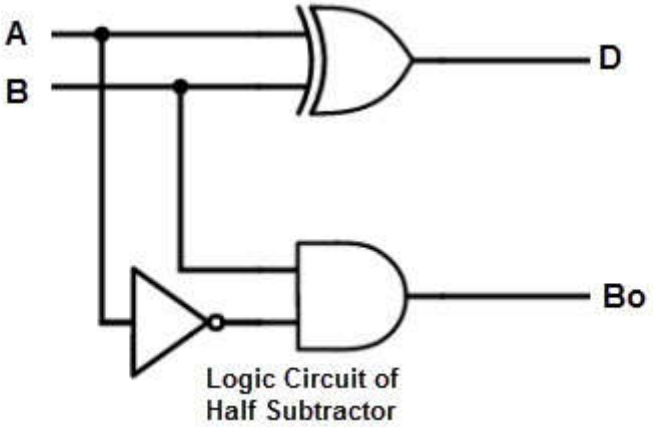
The block diagram, circuit diagram and the truth table for half adder is given below:



Block Diagram

A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table



Logic Circuit of
Half Subtractor

The i/o ports needed to be declared for the formation of half adder is given below:

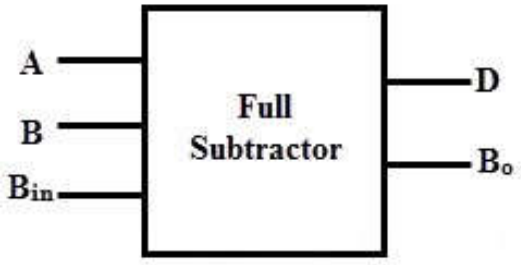
Port Name	input/output	Bus
A	In	No
B	In	No
D	Out	No
Bout	Out	No

NB: Use temporary variable where ever necessary.

To simulate the operation of a full subtractor using half subtractor as component

A combinational logic circuit performs a subtraction between the two binary bits by considering borrow of the lower significant stage is called as the full subtractor. In this, subtraction of the two digits is performed by taking into consideration whether a 1 has already borrowed by the previous adjacent lower minuend bit or not.

It has three input terminals in which two terminals corresponds to the two bits to be subtracted (minuend A and subtrahend B), and a borrow bit Bi corresponds to the borrow operation. There are two outputs, one corresponds to the difference D output and other borrow output Bo as shown in figure along with truth table.

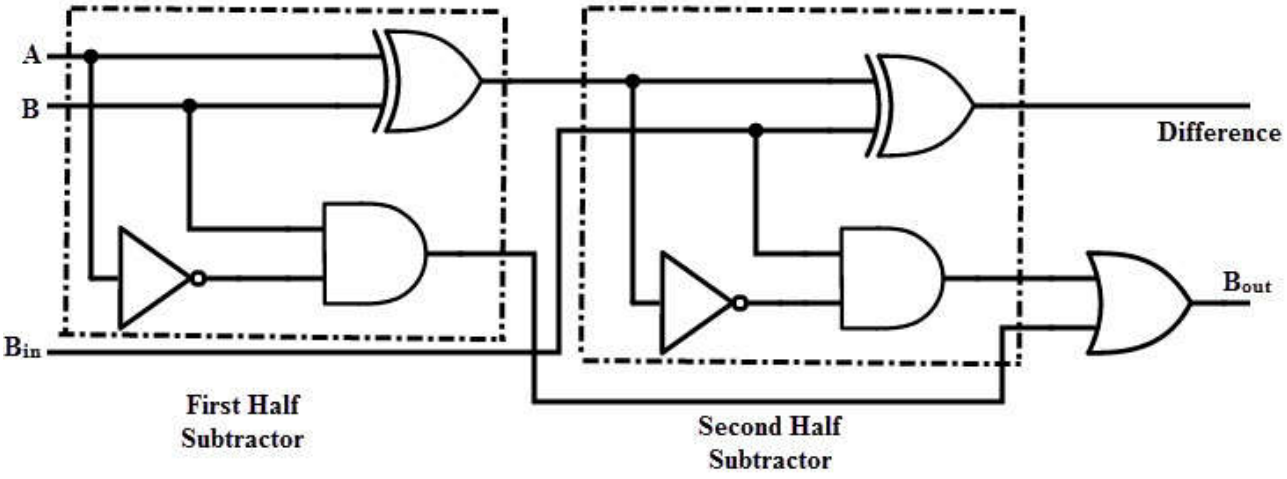


Block Diagram of
Full Subtractor

A	B	B_{in}	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Truth Table

The circuit diagram of a full subtractor is given below:



The I/O ports needed to be declared for the formation of full subtractor is given below:

Port Name	Input/output	Bus
A	In	No
B	In	No
Bin	In	No
Diff	Out	No
Bout	Out	No

NB: Use temporary variables where ever necessary.