NAME OF THE PROGRAM: *CSE*	**DEGREE:** *B.Tech*
COURSE NAME: *Computer Architecture*	**SEMESTER:** *4th*
COURSE CODE: *PCC-CS 492*	**COURSE CREDIT:** *2*
COURSE TYPE: *LAB*	**CONTACT HOURS:** *4P*

Exp. No.	List of Experiments	Date
1.	Illustration of basic Gates: AND, OR & NAND Verify the results using a test bench	**Week 1**
2.	Design of Half Adder(Using Basic Gate) , Full Adder(Using Basic Gate) and Full adder using 2 half adder. Verify the results using a test bench	**Week 2**
3.	Design of 8-bit Adder using Full Adder as component Verify the results using a test bench	**Week 3**
4.	Create a 4 bit adder_subtractor composite circuit using 1 bit adder and XOR gate as components Verify the results using a test bench	**Week 4**
5.	Create a Half Subtractor, Full Subtractor, Full Subtractor using 2 half Subtractor, 8-bit Subtractor using Full Subtractor Verify the results using a test bench	**Week 5**
6.	Create a 4 bit comparator. Use buses for each of the input signal lines Verify the results using a test bench	**Week 6**
7.	Create 8:1 Multiplexer with select line. Use buses for each of the input signal lines Create 8:1 DeMultiplexer with select line. Use buses for each of the input signal lines Verify the results using a test bench	**Week 7**
8.	Design a behavioral simulation of JK flip flop and D flip flop. Consider clock period = 1 ps Design a behavioral simulation of T flip flop. Verify the results using a test bench	**Week 8**
9.	Design a 4-bit serial in and parallel out shift register Design a 4-bit parallel in and serial out shift register Verify the results using a test bench	**Week 9**
10.	Design 4 bit up down counter. Verify the results using a test bench	**Week 10**
11.	Design 4-bit simple ALU Verify the results using a test bench	**Week 11**
12.	Design memory modules for a RAM Verify the results using a test bench	**Week 12**