SoC Chapter 8: Fabrication

Modern SoC Design on Arm
End-of-Chapter Exercises

Q1 Chip Fabrication

List and describe the main layers of a modern silicon chip.

Q2 Place-and-Route

What problems can be found during net routing that would suggest a better placement is needed? How can these be anticipated during placement? Would a constructive placer take these considerations into account?

Q3 FPGA vs ASIC

Why is an FPGA larger and slower than the equivalent ASIC?

Q4 FPGA Multiplication

How many FPGA DSP blocks are needed for a 32×32 multiplier? What is its latency? What difference does it make if only 32 bits of the result are needed?

Q5 Production Test

Design a logic structure that will be very difficult to assess in a production test, but which does not include redundant logic. What is the problem? Could such a structure be needed in a real application?

Q6 Floorplanning (also Clock and Power Domains)

What principal data needs to be held in a floor plan? Can a good floor plan reduce the number of domain crossing and isolation components needed?

Q7 Slew Rate Limiting

Choose one of the reasons listed in the book for limiting the transition times in a design and expand upon the reasoning with examples, simulations or mathematical modelling. Why is the transition time especially important for clock signals?

Q8 Conductor Delay Scaling

Why does the net delay become a larger proportion of the path delay as process geometries shrink?

Q9 Statistical Delay Modelling

Why would it be helpful to model the statistical variation of net delays instead of assuming all interconnect segments are at one BEOL corner?

Q10 Static Timing Analysis

-o- Create a list of the sources of timing uncertainty considered during STA. Are there any that were not discussed?

-o- On-chip Parameter Variation: Give an example of OCV that is dependent on location and one that is dependent on time. Is there an example that depends on both location and time?

-o- Negative Slack Amelioration 1: What kind of optimisations might be done to fix STA minimum timing violations with negative slack?

-o- Negative Slack Amelioration 2: What kind of optimisation might be done to fix timing violations with negative slack in maximum timing analysis?

-o- Exploiting Positive Slack Time: What kind of optimisations might be done to lower the power by reclaiming positive slack in a maximum timing analysis?

-o- Hold Time Violations: Why can minimum timing violations not be fixed by decreasing the clock frequency?

-o- Why is it important that inputs to STA, like Liberty abstract timing models and SPEF netlists, conform to an IEEE standard?

Q11 Yield Improvement Through Redundancy

Describe how the die yield can be improved if a structure is replicated hundreds of times over a chip? Should the end user be involved in this process? Consult a recent DRAM chip data sheet and discuss the mechanisms likely to be used during a production test and at boot time.