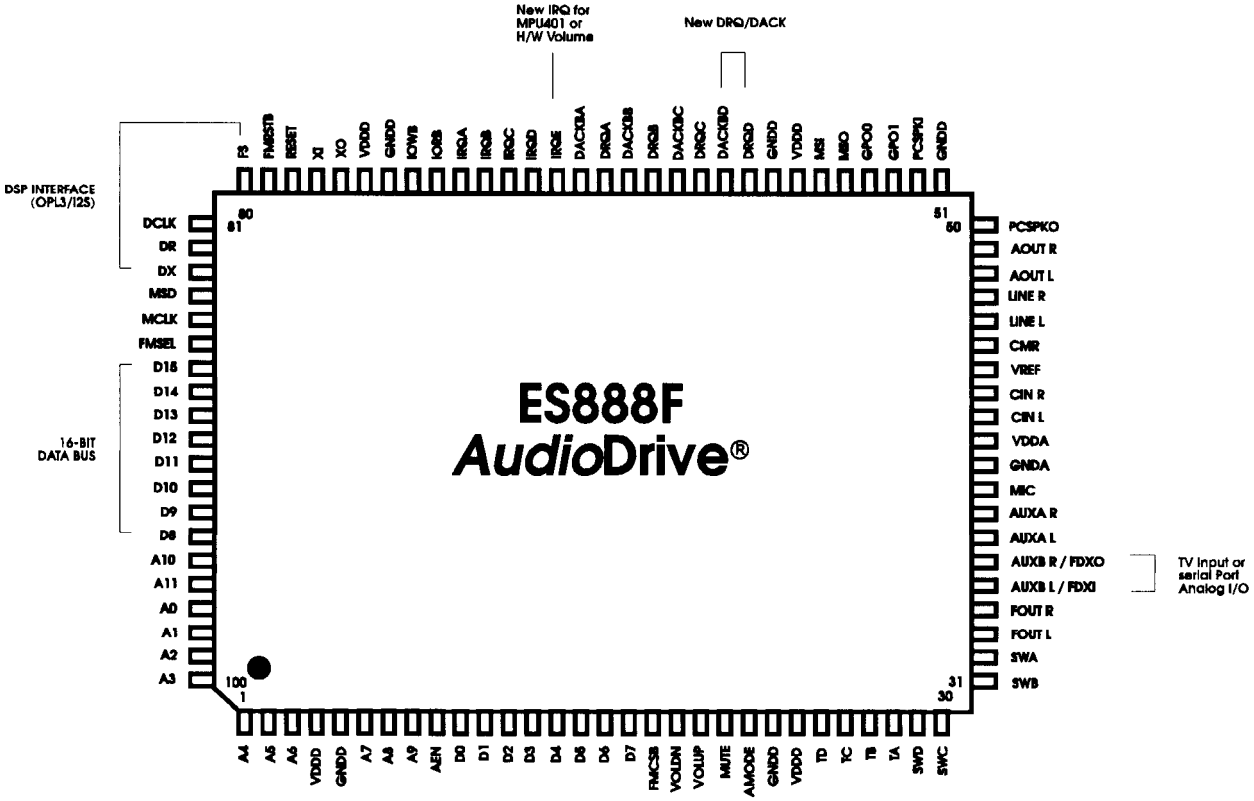
ES888 Preliminary Product Description
1 1/14/96

Features:

- o Simple interface to external FM synthesizer
- o Integrated Music DAC -- serial interface to external FM Synthesizer or ES689/ES690 Wavetable Synthesizer or IIS audio source.
- o Easy upgrade to ES1 888 integrated-FM solution

Pin Diagram



Interface to External FM Synthesizer

FMCSB (pin 18) of the ES888 is an active low address decode output to an external FM synthesizer. It is connected to the /CS input of the FM synthesizer as well as the enable input of a 74LS245 buffer, if required.

FMRSTB (pin 79) of the ES888 is an active low reset to the external FM synthesizer. This pin is controlled by the ISA hardware reset signal as well as a programmable register bit within the ES888.

There are two general methods of bringing FM audio into the ES888: digital serial interface or analog interface. The ES888 has an internal stereo D/A converter called the Music DAC. Two separate serial interfaces can access the Music DAC: the ES689 Wave Table serial interface, or, the new FM serial interface.

FM/IIS Serial Interface to Music DAC

The new FM serial interface reuses pins of the DSP serial interface. When the FM serial interface is enabled, the DSP interface is disabled, and vice-versa. Input FMSEL, when high, enables the FM serial interface and disables the DSP serial interface. Three formats are supported by the FM serial interface. The following table shows how the DSP interface pins are reused for the FM serial interface:

ES888 Pin	0PL3 Pin	OPL3-L Pin	IIS Signal
DCLK	ΦSY	BCO	Bit Clock
FS	SMPBD/SMPR	WCO	Vcc (tie high)
DR	DOAB/MO	DO	Data
DX	SMPAC/SMPL	LRO	-Left/Right

(Note: Pads FS and DX do not have pulldown devices in the ES888).

The ES888 will automatically detect which serial format is being used based on the behaviour of the FS pin.

Analog Interface to FM Synthesizer

If the external FM synthesizer has its own D/A converter, the analog outputs of that converter can be A.C. coupled to ES888 analog inputs AUXBL / R. System software should set bit 0 of externded mode register BB high: this maps the AUXB L/R mixer inputs to be controlled by the music volume registers.

When the AUXB L/R inputs are used for music (either FM or FM mixed with wavetable), the DSP serial port pins can be used as a DSP interface or as an IIS interface. The Music DAC can be used by the IIS or ES689 serial interfaces.

ES689 Serial Interface

The ES689 serial interface pins are supported in the ES888. If these pins are active and enabled, then they will override the FM or IIS use of the Music DAC. The Music DAC volume will always be controlled by mixer registers 36H for playback and 6BH for record when the ES689 serial interface is both active and enabled. As in previous AudioDrive chips, bit 4 of mixer register 48H enables the ES689 serial interface.

Music/AUXB Mixer Controls

Bits 0 and 1 of extended mode register BB can change the how the Music DAC and AUXB audio sources get their volume control information. The normal, reset default is as follows:

Music DAC	Playback = 36H	Record = 6BH
AUXB	Playback = 3AH	Record = 6CH

Bit 0 of extended mode register BB, if high, forces AUXB to be controlled by mixer registers 36 for playback, 6B for record. This is useful when the AUXB inputs are from external music devices.

Bit 1, if high (and if the ES689 serial interface is inactive or disabled), forces the Music DAC volume to be controlled by mixer register 3A for playback, 6C for record. This allows the IIS audio source, which uses the Music DAC, to have an independent mixer control.

Both bits are cleared by hardware reset.

Record Mixer

The record mixer has two new inputs. The first is from the Music DAC. The second is from the Second DMA Channel DAC.

68H Microphone
69H Second DMA Channel
6AH AUXA/CD
6BH Music DAC (unless the Music DAC is mapped to 6C by extended register BB bit 1)
6CH AUXB (unless the AUXB inputs are mapped to 6B by extended register BB bit 0)
6EH Line

Upgrade Path to ES1888

It is easy to produce a design that works with either the ES888 or ES1888.

Pin	ES888	ES1 888
FMCSB	Connects to FM synthesizer and 74LS245 Enable	Becomes ENB245: no connect
FMRSTB	Connects to FM synthesizer	Becomes FSR input: connect to FSX
FMSEL	Tied high or low.	Becomes SE input: no connect
FS/DCLK/ DR/DX	DSP or FM serial interface	DSP serial interface or no connect

Software Issues

Extended mode register BB is not supported by the ES1888 and should not be programmed to any value other than zero for the ES1 888. System software should detect the ES888 vs. ES1888 before writing to extended mode register BB.

The ES1888 does not support mixer registers 69 and 6B. In the ES1888 these registers are aliases of 68 and 6A respectively. Future versions of the ES1 888 may well support these registers. If so, extended mode register BB will also be supported, so the presence of theses registers is a good way to decide if register BB can be programmed, and, whether these registers are supported in the record mixer application.

Driver software should try to detect the presence of the ESFM synthesizer with a separate test routine in order to decide which FM driver to install.

Extended Mode Register BBH

7	6	5	4	3	2	1	0
Reserved: write 0				1:enable rec mix special mute	1:enable play mix special mute	1:serial D/A volume map	1: AUXB volume map

Bits 3 and 2 enable a new feature called special mute that changes the way the mixer handles inputs that are muted so that noise is reduced.

Bit 1, if high, causes the new serial interface stereo D/A to be controlled by mixer registers 3AH for playback and 6CH for record rather than the default music volume registers.

Bit 0, if high, causes the AUXB L/R inputs to be controlled by mixer registers 3AH for playback and 6CH for record rather than the default music volume registers.

This register is reset to zero by hardware reset.

ES1887 Enhanced Features

Hardware Volume Control

Mixer Extension Register 64H Master Volume Control

7	6	5	4	3	2	1	0
Mode		1:Count by 3	Read Only HWV Int request	0	1:Enable HWV Int. using IRQE	1:Enable HWV Int. share w/ audio int	1:Disable SB PRO Master Vol Emulation

Bit 7-6 Selects operation mode:

- 0 0 Normal 3-wire mode (hardware reset default)
- 01 2-wire mode: both UP and DOWN inputs being low together act as a MUTE input low.
- 10 2-wire enabled, debounce disabled, auto-increment/decrement disabled.
- 11 Hardware volume control disabled.

Bit 5 1: Count up and down by 3 for each push of UP or DOWN buttons.
0: Count up and down by 1 for each push of UP or DOWN buttons.

Bit 4 Read only interrupt request from hardware volume event.

Bit 3 Reserved -- write 0.

Bit 2 When high, enables IRQE as an output for the hardware volume control interrupt. This bit is cleared by hardware reset

Bit 1 When high, enables the hardware volume control to be shared with the audio interrupt. This bit is cleared by hardware reset.

Bit 0 When low, a write to the SB PRO master volume register will be translated into a write to the hardware master volume counters, mixer registers 60H and 62H. If high, the SB PRO master volume registers are, in effect, read-only. This bit is cleared by hardware reset.

New Interrupt Control -- Mixer Register 7F

7	6	5	4	3	2	1	0
MPU-401 Int Req	HW Vol Int Req	Audio 2 Int Req	Audio 1 Int Req	Interrupt Select			Output Enable

Bit 0 1 to enable select IRQ as an output in New Interrupt Mode.

Bit 3:1
0 0 0 Old Interrupt Mode
0 0 1 New Interrupt Mode -- IRQA
0 1 0 New Interrupt Mode -- IRQB
0 1 1 New Interrupt Mode -- IRQC
1 0 0 New Interrupt Mode -- IRQD
1 0 1 New Interrupt Mode -- IRQE

Bit 4 (Read Only) Audio 1 Interrupt Request. Set high from any of three possible sources:
1) Game-Compatible Interrupt AND'd with bit 4 of extended register B1.
2) Extended Mode DMA Transfer Complete Interrupt AND'd with both bit 4 and bit 5 of extended register B1.
3) FIFO Half-Empty Interrupt AND'd with both bit 4 and bit 6 of extended register B1.

Bit 5 (Read Only) Audio 2 Interrupt Request. AND'd with bit 6 of mixer register 7A.

Bit 6 (Read Only) HW Volume Interrupt Request. AND'd with bit 1 of mixer register 64.

Bit 7 (Read Only) MPU-401 Interrupt Request. Bits 7:5 of mixer register 40 must be set to 0,1,0 for this interrupt request to be active high.

This register is reset to zero by hardware reset.

Interrupts

There are four independent interrupt sources within the original ES1 888:

Audio 1	Map:	Bits 3:2 of extended register B1 selects among IRQA-D
	Output Enable:	Bit 4 of extended register B1
	Mask:	Bits 6:5 of extended register B1
Audio 2	Map:	Fixed to IRQE
	Output Enable:	Bit 6 of mixer register 7A
	Mask:	" " " " "
HW Volume	Map:	Bits 2:1 of mixer register 64
	Output Enable:	" " " " "
	Mask:	" " " " "
MPU-401	Map:	Bits 7:5 of mixer register 40
	Output Enable:	" " " " "
	Mask:	" " " " "

New Interrupt Mode

For backward compatibility, the above registers are still supported. However, a new method of sharing and mapping the interrupts has been added that should replace the old configuration method. In New Interrupt Mode, all four interrupt sources must share a single IRQ output, IRQA-E, determined by bits 3:1 of mixer register 7F. Edge-generation logic ensures that each pending interrupt request will correctly signal the interrupt controller. There is a single IRQ output enable, bit 0 of the same register.

New Interrupt Mode is enabled if any of bit 3:1 of mixer register 7F is high. If all three bits are low, then the ES1 888V acts exactly as the previous chips.

In New Interrupt Mode, each interrupt source has one or more mask bits:

Audio 1	Bit 4 of extended register B1 masks all audio 1 sources. Bit 6 of the same register masks the interrupt for extended mode DMA transfer complete. Bit 5 of the same register masks the interrupt for extended mode FIFO half-empty flag transition.
Audio 2	Bit 6 of mixer register 7A masks this interrupt source.
HW Volume	Bit 1 of mixer register 64 must be set high (share with audio) to enable this interrupt source.
MPU-401	Bits 7:5 of mixer register 40 must be set to 010 (share with audio) to enable this interrupt source.

Bits 7-4 of mixer register 7F provide for a convenient way to poll the four interrupt requests (after being masked by the mask bits listed above).

Note: Bits 3:2 of extended mode register B1H do not select the interrupt pin in New Interrupt Mode. They should be programmed to match the pin selected by mixer register 7F if possible for those programs that might read the BI register to determine the interrupt number.

Audio, FM and Joystick Address Configuration and Enable

1) The ES1 888V will be backward compatible to the ES1 888 for address configuration. For example, mixer register 40H will still act as before, and the old read-sequence-key will still act as before. However, the new configuration features should be used for all future designs.

2) The joystick will have its own chip enable so that it can be enabled independently of audio. The joystick will have four choices for base address: 200H, 201 H, 202H or 203H. The FM will also now have four choices for base address: 388H, 398H, 3A8H or 3B8H.

3) Method 1 of software configuration is read-sequence-key. It is enabled if input pin AMODE=O. There are now two different keys.

The old key sequence acts as in the original ES1888: it sets three bits of system control register 0 (CE, AS1, AS0) and is not always enabled. Specifically, it is enabled after hardware reset and after a 1 is written to bit 2 of mixer register 40H.

The new key sequence is always enabled (except if input pin AMODE=1). This is necessary because mixer register 40H is not accessible if the audio device is disabled. It sets all bits of SCR 0, including new bits that can be used to select the joystick and FM base addresses.

New read-sequence-key:

Read 22B
Read 229
Read 22F
Read 22D
Read 22D
Read 22F
Read 229

Any I/O read of the incorrect address (except DMA) resets the sequence.

Immediately after the key, perform three more I/O reads to set audio, joystick, and FM base addresses:

Read Audio Base Address	220, 230, 240, 250. Any other address leaves audio disabled (i.e., bits 2 of SCR 0 = 0).
Read Joystick Base Address	200-203. Any other address leaves joystick disabled (i.e., bits 3 of SCR 0 = 0).
Read FM Base Address	388, 398, 3A8, 388. Any other address leaves FM at 388 (i.e., bits 7-6 of SCR 0 = 0).

Note: all interrupts must be disabled when the key is being executed, until after the FM base address has been set. An I/O read from other than 22X should be done first in order to reset the key sequence.

Record Mixer Enhancement

The record mixer has two new inputs. The first is from the Music DAC. The second is from the Second DMA Channel DAC.

Record Mixer Registers

68H Microphone
69H Second DMA Channel
6AH AUXA/CD
6BH Music DAC
6CH AUXB
6EH Line

All are reset low by hardware reset but not by mixer reset.

Mixer Extension Register 48H - Serial Mode Miscellaneous Control

7	6	5	4	3	2	1	0
SE	2'S Comp	Serial Reset	Enable ES689 Interface	Active Low Sync	1: DSP Test Mode	E-able 1st DMA in SMOC	0

Bit 7: 1: Enable DSP serial port. This signal is synchronized with DCLK input rising edge. If DCLK is not running, changing SE will have no effect.

Bit 6: 1: Data is signed, 2's complement format
0: Data is unsigned (offset binary) format

Bit 5: 1: Serial Reset. Used to reset left/right sequencer for stereo serial modes so that the next sample transmitted is left channel data.

Bit4: 1: Enable ES689 serial interface.
0: Disable ES689 serial interface.

Bit 3: 1: Active low frame sync pulse.
0: Active high frame sync pulse.

Bit 2: Test mode: FSX, FSR, DCLK become outputs.

Bit 1: 1: In serial mode, connect first channel DMA (and game-compatible DMA) to second channel DAC. This allows game compatible audio to be heard when in serial mode. The second channel DAC gets its filter clock and volume control from the first channel.

0: In serial mode, the first channel DMA does not played. The second channel is connected to the second DAC.

Bit 0: Reserved. Write 0.

4) Method 2 of software configuration is system-control-register. It is enabled if input pin AMODE=1. Register El becomes read/write in the ES1 888V (used to be write only). SCR 0 is changed as follows:

7	6	5	4	3	2	1	0
FMA5	FMA4	JA1	JA0	Joystick Chip Enable	Audio Chip Enable	AS1	AS0

Bit 1:0 Base Address of Audio

0 0	220
0 1	230
I O	240
1 1	250

Bit 2 Audio Chip Enable

Bit 3 Joystick Chip Enable

Bit 5:4 Base Address of Joystick

0 0	200
0 1	201
1 0	202
I 1	203

Bit 7:6 Base Address of FM

0 0	388
0 1	398
I O	3A8
I 1	3B8

Note I: SCR 0 is reset to zero by hardware reset.
Note 2: SCR 0 is written during the new read-sequence-key method if AMODE=0, but not the *old* read-sequence-key.

5) Backward Compatibility -- mixer register 40H bit 1 and 0

Bit I of mixer register 40H, if set, enables joystick at 201 H *if audio is a/so enabled.* This bit when set overrides enable or address selected via bits 5-3 of SCR 0.

Bit 0 of mixer register 40H, if set, enables FM alias at base address specified by bits 7:6 of SCR 0.

Second Channel DMA Configuration

In the original ES1 888, the second channel DMA was forced to use DRQD/DACKBD. In the ES1 888V, the second channel DMA can use any of the four DRQ/DACKB pairs, except the one used by the first channel DMA.

Second Channel DMA Configuration -- Mixer **Register 7D**

7	6	5	4	3	2	1	0
0	0	0	0	1: FM Mix	1:Enable pulldown	DS1	DS0

Bit 1:0
- 0 0 Second channel DMA uses DRQA/DACKBA
- 01 Second channel DMA uses DRQB/DACKBB
- 1 0 Second channel DMA uses DRQC/DACKBC
- 11 Second channel DMA uses DRQD/DACKBD (reset default)

Bit 2
- 1: Enable pulldown on selected DRQ pin (reset default)
- 0: Disable pulldown on selected DRQ pin

Bit 3
- 1: Enable FM Mix Mode. In this mode the second channel DMA is synchronized and added to the FM output (49612.5 Hz).
- 0: Disable FM Mix Mode.

This register is reset to 07 by hardware reset.