CIO-DIO48, CIO-DIO48H
CIO-DIO96, CIO-DIO192

Digital I/O Board

User's Manual

Revision 4
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1 INTRODUCTION

This manual provides information on CIO-DIO48, CIO-DIO48H, CIO-DIO96 and CIO-DIO192 digital I/O boards and accessories. Throughout this manual we use CIO-DIO as a generic designation for the CIO-DIO48, CIO-DIO48H, CIO-DIO96 and CIO-DIO192. When required, due to the differences in the boards, the specific board name is used. The manual is organized into separate sections for those aspects of a product which are unique. Most issues are applicable to all of the digital boards.

The CIO-DIO48 has two 82C55 parallel-interface chips and a 50-pin connector. Each 82C55 controls 24 CMOS/TTL-compatible digital I/O pins. The 82C55 ports can be programmed as three groups of eight I/O each, or two ports of eight each, and two ports of four I/O each.

The CIO-DIO96 has the equivalent of two CIO-DIO48 circuits on a single board while the CIO-DIO192 equals four CIO-DIO48 circuits on a single board.

The CIO-DIO48H is a high-drive, 48-line I/O board. The I/O lines are capable of sourcing 15 mA and sinking 64 mA. The registers emulate 82C55 mode 0 control registers. Other 82C55 modes (1 or 2) cannot be programmed in the CIO-DIO48H. All of the information on the 82C55 in this manual applies also to the emmulated version of the 82C55 with the exception of the references to modes 1 and 2.

Each of the boards have the same connector pin-out and respond to the same software instructions. This manual includes information on configuring the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2 must procure a data book from Intel Corporation Literature Department.

Although the boards can be programmed directly to the I/O registers , we recommend that you use Universal Library software.

2 INSTALLATION

2.1 SOFTWARE

The board has a set of address switches and a jumper which may need to be set before installing the board in your computer. The simplest way to configure your board is to use the *Insta*Cal™ program provided with your board. *Insta*Cal will show you all available options, how to configure the various switches and jumpers to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically have access to the exact configuration of the board.

Please refer to the *Extended Software Installation Manual* regarding the installation and operation of *Insta*Cal. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to *Insta*Cal and/or your computer.

2.2 HARDWARE

BASE ADDRESS

The base address is the location that software writes to and reads from when communicating with the CIO-DIO. The base address switch sets the starting address for all communication to and from the board.

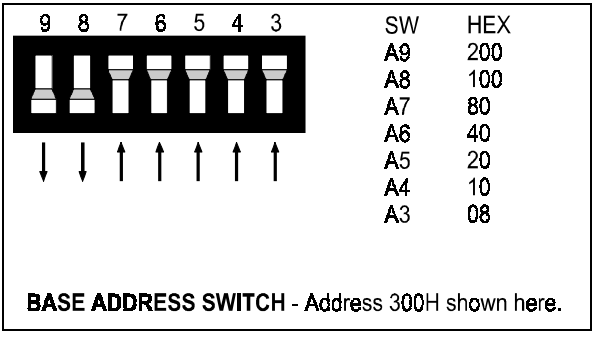


Figure 2-1. Base Address Switches

The base address switch on the CIO-DIO48 and CIO-DIO48H are identical to that shown in figure 2-1. The CIO-DIO96 has one less switch in the base address switch bank and the CIO-DIO192 has two less. This means that the CIO-DIO48(H) may be set at addresses that are a multiple of 8 (300h, 308h, 310h, etc..). The CIO-DIO96 may be set at addresses that are a multiple of 16 and the CIO-DIO192 at multiples of 32.

The board is set at the factory for a base address of 300h (768 decimal). Unless you have other boards in your PC at this address, leave the switch as it is set.

A complete address is constructed by calculating the HEX or decimal number which corresponds to all the address bits the CIO-DIO has been instructed to respond to. For example, shown in figure 2-1 are address 9 and 8 DOWN, all others UP. Switch A9 = 200h (512 decimal) and switch A8 = 100h (256 decimal). Added together they equal 300h (768 decimal).

NOTE

DISREGARD NUMBERS PRINTED ON THE SWITCH. REFER TO THE NUMBERS PRINTED IN WHITE ON THE BOARD.

Certain addresses are used by the PC, others are free and can be used by the CIO-DIO and other expansion boards.

Table 2-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	82C55 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI Mask (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE RESISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK	378-37F	Parallel Printer
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0FF-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	Parallel Printer
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

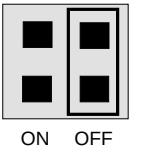
The CIO-DIO base address switch can be set for address in the range of 000h to 3E0h so it should not be hard to find a free address area for your CIO-DIO. If you are not using IBM prototyping cards or some other board which occupies these addresses, 300-31Fh are free to use.

Addresses not specifically listed, such as 390-39Fh, are free.

WAIT STATE JUMPER

Some CIO-DIO boards have a wait state jumper which can enable an on-board wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DIO board so that signals from slow devices (chips) will be valid.

The wait state generator on the CIO-DIO is only active when the CIO-DIO is being accessed. In general, the PC will not be slowed down by using the wait state.



WAIT STATE JUMPER BLOCK

Figure 2-2. Wait State Jumper

Because all PC expansion board buses are slowed to either 8MHz or 10MHz, the wait state generally is not required.

If you experience sporadic failures using the CIO-DIO boards, try enabling the wait state generator.

2.3 INSTALLING IN THE COMPUTER

1. Turn the power off.

2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

3. Locate an empty expansion slot in your computer.

4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DIO.

3 CABLING TO THE DIO CONNECTOR

3.1 CONNECTOR DIAGRAM

The I/O connector(s) for each of these boards is one or more 50-pin header connector accessible from the rear of the PC through the expansion backplate..

The connector accepts female 50-pin header connectors, such as the C50FF-2, a 2-foot cable with female connectors. One cable is required for the CIO-DIO48 (H), two are required for the CIO-DIO96 and four are required for the CIO-DIO192.

If frequent changes to signal connections or signal conditioning is required, please refer to the catalog for information on the CIO-TERM100, CIO-SPADE50 and CIO-MINI50 screw terminal boards.

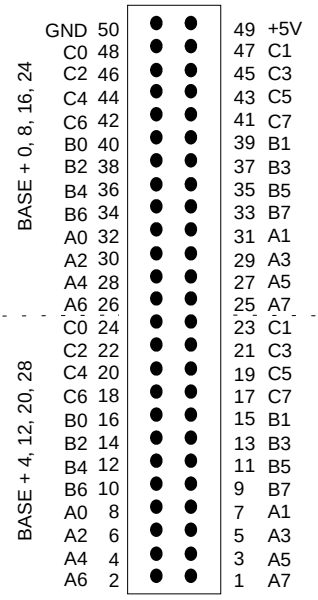


Figure 3-1. I/O Connector

3.2 SIGNAL CONNECTION

All the digital inputs and outputs on the CIO-DIO connector are TTL. Under normal operating conditions, the voltages on the I/O pins range from near 0 volts for the low state to near 5 volts for the high state.

The voltages and currents of external devices usually exceed these values. Because of this, external relays are usually employed to handle higher current and voltage loads.

In addition to load matching, digital signal sources often need to be filtered or “de-bounced”. Brief descriptions of digital interfacing is located in the section on Interface Electronics in this manual.

IMPORTANT NOTE

The CIO-DIO digital I/O board initializes all ports as inputs on power up and reset. A TTL input is a high impedance input. If you connect another TTL input device to a CIO-DIO board it will probably be turned ON every time the board is reset, or, it might be turned OFF instead. Remember, a CIO-DIO board which is reset is in INPUT mode.

To safeguard against unwanted signal levels, all devices being controlled by a CIO-DIO board should be tied low (or high, as required) by a resistor.

You will find positions for pull up and pull down resistor packs on your CIO-DIO board. To implement these, please turn to the application note on pull up/down resistors.

3.3 UNCONNECTED INPUTS FLOAT

Keep in mind that unconnected inputs float. If you are using a DIO board for input, and have unconnected inputs, ignore the data from those lines.

In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or may even track A0. It is unconnected and so is not specified. In the absence of a pull-up/down resistor, any input to a CIO-DIO which is unconnected is unspecified.

You do not have to tie input lines; unconnected lines will not affect the performance of connected lines. Simply mask out any unconnected bits in software.

4 REGISTER MAP

4.1 INTRODUCTION

Each CIO-DIO (except the CIO-DIO48H) is composed of 82C55 digital I/O chips. Each chip contains three data and one control register occupying four consecutive I/O locations. The number of I/O locations occupied by a CIO-DIO board is equal to four times the number of 82C55 chips on the board.

Note: The CIO-DIO48H does not use the 82C55 chip but emulates it.

The first address, or BASE ADDRESS, is determined by setting a bank of address switches on the board.

The register descriptions follow the format shown below:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

The numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the weights in Table 4-1 apply.

Table 4-1. Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

The registers and their function are listed on Table 4-2. Within each register are eight bits which may constitute a byte of data or be eight individual bit set/read functions.

Table 4-2. Board Registers

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE + 0	Port A Input	Port A Output
BASE + 1	Port B Input	Port B Output
BASE + 2	Port C Input	Port C Output
BASE + 3	None. No read back	Configure digital io
BASE + 4	Port A Input	Port A Output
BASE + 5	Port B Input	Port B Output
BASE + 6	Port C Input	Port C Output
BASE + 7	None. no read back	Configure digital IO
ADDITIONAL CIO-DIO96 & 192 ONLY		
BASE + 8	Port A Input	Port A Output
BASE + 9	Port B Input	Port B Output
BASE + 10	Port C Input	Port C Output
BASE + 11	None. No read back	Configure digital IO
BASE + 12	Port A Input	Port A Output
BASE + 13	Port B Input	Port B Output
BASE + 14	Port C Input	Port C Output
BASE + 15	None. no read back	Configure digital IO
ADDITIONAL CIO-DIO 192 ONLY		
BASE + 16	Port A Input	Port A Output
BASE + 17	Port B Input	Port B Output
BASE + 18	Port C Input	Port C Output
BASE + 19	None. No read back	Configure digital IO
BASE + 20	Port A Input	Port A Output
BASE + 21	Port B Input	Port B Output
BASE + 22	Port C Input	Port C Output
BASE + 23	None. no read back	Configure digital IO
BASE + 24	Port A Input	Port A Output
BASE + 25	Port B Input	Port B Output
BASE + 26	Port C Input	Port C Output
BASE + 27	None. No read back	Configure digital IO
BASE + 28	Port A Input	Port A Output
BASE + 29	Port B Input	Port B Output
BASE + 30	Port C Input	Port C Output
BASE + 31	None. No read back	Configure digital IO

4.2 DIGITAL I/O REGISTERS

PORT A DATA
BASE ADDRESS +0

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORT B DATA
BASE ADDRESS +1

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B can be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes, individual bits are more likely used.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BASE ADDRESS +2 (8-bit mode)

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

Port C can be used as one 8-bit port of either input or output, or it can be split into two, 4-bit ports which can independently be either input or output.

PORT C DATA
BASE ADDRESS +2 (4-bit nibble mode)

7	6	5	4	3	2	1	0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

The notation for the upper 4-bit port is CH3 to CH0, and for the lower, CL3 to CL0.

Although it can be split, every read and write to port C carries eight bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS
In 82C55 mode 0 configuration, ports configured for output hold the output data written. The output byte can be read back by reading a port configured for output.

INPUT PORTS
In 82C55 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), you will need to acquire an Intel data book and see the 82C55 data sheet.

DIGITAL CONTROL REGISTER
BASE ADDRESS +3

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
	Group A				Group B		

The 82C55 can be programmed to operate in Input/ Output mode (mode 0), Strobed Input/ Output mode (mode 1) or Bi-Directional Bus mode (mode 2).

The emmulated 82C55 (CIO-DIO48H) can be programmed to operate in Input/ Output mode (mode 0) only.

Included here is information on programming in mode 0. Those wishing to use the 82C55 in modes 1 or 2, must procure a data book from Intel Corporation Literature Department.

When the PC is powered up or RESET, the 82C55 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

The Ports A, B, C High and C Low can be independently programmed for input or output.

The two groups of ports, group A and group B, can be independently programmed in one of several modes. The most commonly used mode is mode 0, input/output mode. The codes for programming the 82C55 in this mode are shown in Table 4-4.

The codes for programming the CIO-DIO48H are shown in Table 4-5.

Table 4-4. 82C55 Configuration Codes

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

NOTE: D7 is always 1. D6, D5 and D2 are always 0 for 8255 mode 0.

Table 4-5. CIO-DIO48H Port Configuration Codes

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	0	0	OUT	OUT	OUT	OUT
0	0	0	1	1	1	OUT	OUT	OUT	IN
0	0	1	0	2	2	OUT	OUT	IN	OUT
0	0	1	1	3	3	OUT	OUT	IN	IN
0	1	0	0	8	8	OUT	IN	OUT	OUT
0	1	0	1	9	9	OUT	IN	OUT	IN
0	1	1	0	A	10	OUT	IN	IN	OUT
0	1	1	1	B	11	OUT	IN	IN	IN
1	0	0	0	10	16	IN	OUT	OUT	OUT
1	0	0	1	11	17	IN	OUT	OUT	IN
1	0	1	0	12	18	IN	OUT	IN	OUT
1	0	1	1	13	19	IN	OUT	IN	IN
1	1	0	0	18	24	IN	IN	OUT	OUT
1	1	0	1	19	25	IN	IN	OUT	IN
1	1	1	0	1A	26	IN	IN	IN	OUT
1	1	1	1	1B	27	IN	IN	IN	IN

NOTE: D7, D6, D5 and D2 are always 0 for emmulated mode 0.

5 ELECTRONICS AND INTERFACING

This short, simple introduction to the electronics most often needed by digital I/O board users covers a few key concepts. They are:

- Pull up/down resistors
- Transistors.
- Power MOSFETs
- Solid State Relays
- Voltage dividers.
- Low pass filters for digital inputs.
- Noise; sources and solutions.

IMPORTANT NOTE

WHENEVER THE CIO-DIO IS POWERED ON OR RESET, ALL PINS ARE SET TO HIGH IMPEDANCE INPUT.

The implication of this is that if you have output devices such as solid state relays, they can be switched on whenever the computer is powered on or reset. To prevent unwanted switching and to drive all outputs to a known, predefined state after power on or reset, pull all pins either high or low through a 2.2K ohm resistor.

To install pull up/down resistor packs, see the application note.

5.1 PULL UP & PULL DOWN RESISTORS

Whenever the CIO-DIO is powered on or reset, the control register is set to a known state. That state is mode 0, all ports in input mode.

When used as an output device to control other TTL input devices, the CIO-DIO applies a voltage level of near 0V for low and near 5V for high.

In input mode the CIO-DIO is 'high Z' or high impedance. If your CIO-DIO was connected to another input chip (the device you were controlling), the inputs of that chip are left floating whenever the CIO-DIO is in input mode.

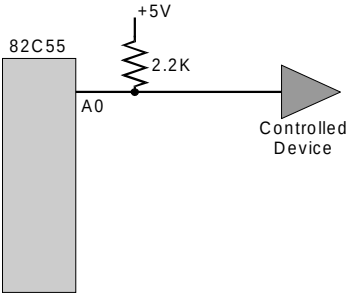
If the inputs of the device you are controlling are left to float, they can float up or down. The way they float is dependent on the characteristics of the

circuit and the electrical environment; and unpredictable. This is why it often appears that the CIO-DIO has gone 'high' after power up. The result is likely that the controlled device is turned on.

That is why need pull up/down resistors are needed.

Shown here is one CIO-DIO digital output with a pull-up resistor attached.

If the CIO-DIO is reset and enters high impedance input, the line is pulled high. At that point, both the CIO-DIO AND the device being controlled will sense a high signal.



82C55 Digital Output with pull-up resistor attached

Figure 5-1. Output with Pull-Up Resistor

If the CIO-DIO is in output mode, the CIO-DIO has more than enough power to override the pull-up resistor's high signal and drive the line low.

Of course, a pull-down resistor accomplishes the same task except that the line is pulled low when the CIO-DIO is reset. The CIO-DIO has sufficient enough power to drive the line high.

The CIO-DIO boards are equipped with positions for pull-up/down resistors Single Inline Packages (SIPs). The positions are marked RN1 through RN6 on the CIO-DIO48(H), RN1 through RN12 on the CIO-DIO96 and RN1 through RN24 on the CIO-DIO192. There may also be references to the ports designators A, B and C where applicable.

A 2.2K ohm, 8-resistor SIP is made of eight, 2.2K resistors all connected on one side to a common point and on the other, to a pin protruding from the SIP. The common pin to which all resistor are connected is one end of the SIP. The common line is marked with a dot.

The SIP can be installed as pull-up or pull-down. At each location, RN1 through RN24, there are 10 holes in a line. One end of the line is +5V, the other end is GND. The end connected to +5V is marked “HI” end connected to ground is marked “LO”. The exception to these markings is the CIO-DIO192, which has a key printed on the board indicating that the +5V

end is toward the top of the board and the grounded end is toward the bottom. The The eight holes in the middle are connected to the eight lines of the port, A, B, or C. Insert the SIP with the common pin in the +5V hole for pull-up or in the GND hole for pull-down.

A resistor value of 2.2K is recommended. Use other values only if you have calculated the necessity of doing so.

5.2 TTL TO SOLID STATE RELAYS

Many applications require digital outputs to switch power to high-current AC or DC powered devices and to monitor AC and DC voltages. Since high AC and DC voltages/currents cannot be controlled or read directly by the TTL digital lines of a CIO-DIO, intermediate relays are used.

Solid State Relays, allow control and monitoring of AC and high DC voltages and provide 750V isolation. Solid State Relays (SSRs) are the recommended method of interfacing to AC and high DC signals.

The most convenient way to use solid state relays with a CIO-DIO board is to purchase a Solid State Relay Rack. A SSR Rack has a circuit board with output buffer chips which are powerful enough to switch the SSRs. The board uses sockets for SSRs. SSR Racks are available from Measurement Computing Corp. and others.

If driving only one or two SSRs, all that is needed is a 74LS244 output buffer chip between the CIO-DIO output and the SSR. The SSR will need a 5 volt power source as well.

5.3 VOLTAGE DIVIDERS

An alternative method of measuring a signal which varies over a range greater than the input range of a digital input, is to use a voltage divider. When correctly designed, it can drop the voltage of the input signal to a safe level the digital input can accept.

Ohm's law states:

Voltage = Current x Resistance

Kirkoff's law states:

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

In a voltage divider, the voltage across one resistor in a series circuit is proportional to the total resistance divided by the one resistor (see formula below).

The object in a voltage divider is to choose two resistors having the proportions of the maximum voltage of the input signal to the maximum allowed input voltage.

The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the attenuation (A) is 2:1 or just 2.

$$R1 = (A-1) \times R2$$

For a given attenuation, pick a resistor and call it R2, the use this formula to calculate R1.

Digital inputs often require the use of voltage dividers. For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to a digital input. The voltage must be dropped to 5 volts max when on. The attenuation is 24:5 or 4.8.

Using the equation above, if R2 is 1K, R1 = (4.8–1) x 1000 = 3.8K.

Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

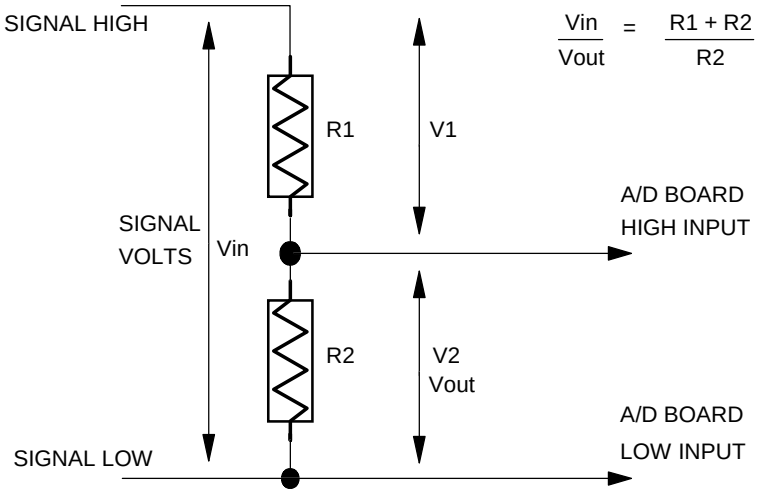


Figure 5-2. Voltage Divider Theory

NOTE The resistors, R1 and R2, are going to dissipate power in the divider circuit according to the equation $W = I^2 \times R$; (Current (I) = Voltage/Resistance). The higher the value of the resistance (R1 + R2), the less power dissipated by the divider circuit. Here is a simple rule:
For attenuation of <5:1, no resistor should be less than 10K.
For attenuation of > 5:1, no resistor should be less than 1K.

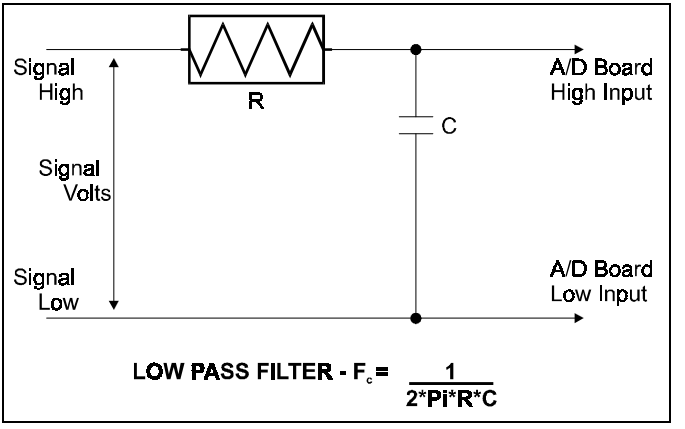
5.4 LOW PASS FILTER TO DE-BOUNCE INPUT

A low pass filter is placed on the signal wires between a signal and an A/D board. It prevents frequencies greater than the cut-off frequency from entering the A/D board's digital inputs.

The cut-off frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low-pass filter had a cut-off frequency of 30 Hz, interference associated with line voltage (60 Hz) would be mostly filtered out but a signal of 25 Hz would pass with less attenuation.

Also, in a digital circuit, a low-pass filter is often used to remove contact bounce noise signals from a switch or a relay contacts. Also, in a digital circuit, a low pass filter might be used to "de-bounce" (filter) an input from a switch or external relay. (Unless switch/relay contacts are mercury-wetted, they tend to bounce briefly on closure, generating a pulsating noise signal. This can easily lead to erroneous counts unless filtered out.)

A simple low-pass filter can be constructed from one resistor (R) and one



capacitor (C). The cut-off frequency is determined according to the formula:

$$Fc = \frac{1}{2 \pi R C}$$

$$R = \frac{1}{2 \pi C Fc}$$

Where π= 3.14...
R = ohms
C = Farads
Fc = cut-off frequency in cycles/second.

6 CIO-ERB24 & SSR-RACK24 CONNECTIONS

CIO-DIO48 family boards each provide digital I/O in groups of 48 bits. However, the many popular relay and SSR boards provide only 24 bits of I/O. The CIO-ERB24 and SSR-RACK24 each implement a connector scheme where all 48 bits of the CIO-DIO board can be used to monitor and control relays and/or SSRs. This configuration is shown in the block diagram below. The 24 bits of digital I/O on CIO-DIO connector pins 25 to 48 (base address +0 through +2) control the first relay board. The 24-bits of CIO-DIO on pins 1 to 24 control the second relay/SSR board on the daisy chain.

Use the C50FF-# cable for interconnections.

Alternately, use the SSR-RACK48 or the CIO-ERB48 series relay boards.

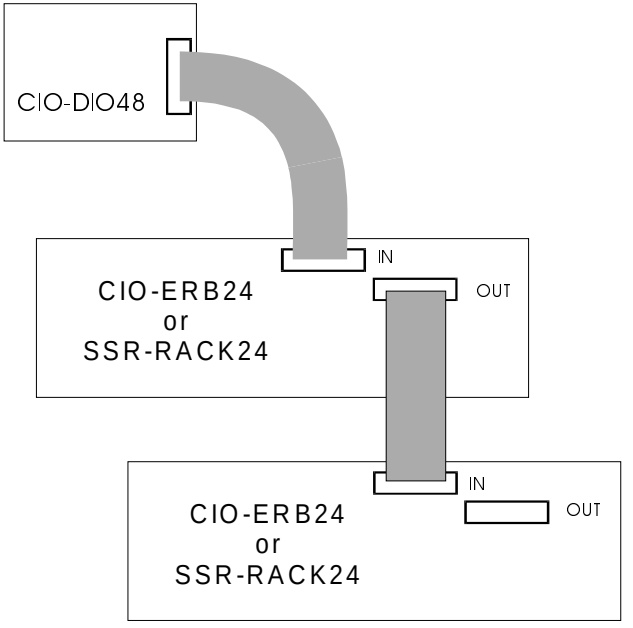
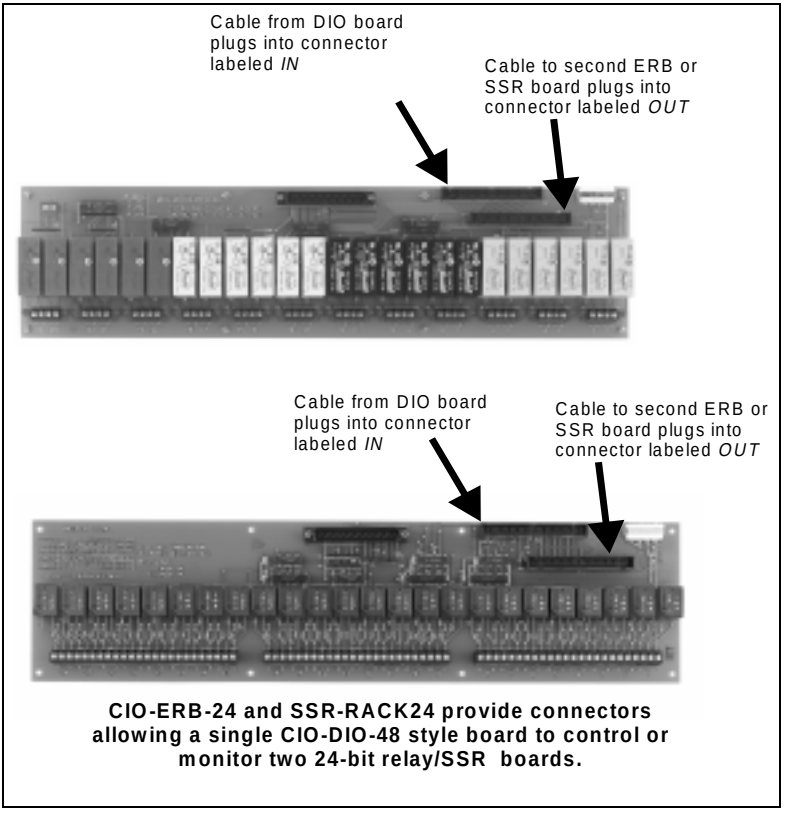


Figure 6-1. Cabling - CIO-DIO48 to CIO-ERB24 or SSR-RACK24 Boards



CIO-ERB-24 and SSR-RACK24 provide connectors allowing a single CIO-DIO-48 style board to control or monitor two 24-bit relay/SSR boards.

7 SPECIFICATIONS

Power consumption

+5V:

CIO-DIO48	150mA typical, 195mA max
CIO-DIO48H	700mA typical, 1200mA max
CIO-DIO96	160mA typical, 205mA max
CIO-DIO192	170mA typical, 220mA max

Digital Input / Output (CIO-DIO48, CIO-DIO96, CIO-DIO192)

Digital Type	82C55
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ -2.5mA
Output Low	0.4 volts max @ 2.5mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)

Digital Input / Output (CIO-DIO48H)

Digital Type	8255 mode 0 emulation
Output:	74S244
Input:	74LS373
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	2.4 volts min @ -15mA
Output Low	0.5 volts max @ 64 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)
Miscellaneous	Locations provided for installation of pull-up or pull-down resistors.

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	-20 to +70°C
Humidity	0 to 90% non-condensing

For your notes.

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

Part Number	Description
CIO-DIO48	Digital I/O Board
CIO-DIO48H	Digital I/O Board
CIO-DIO96	Digital I/O Board
CIO-DIO192	Digital I/O Board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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