Flip-Flop

Praktikum Rangkaian Digital

Ilmu Komputer IPB

2020

Flip-Flop

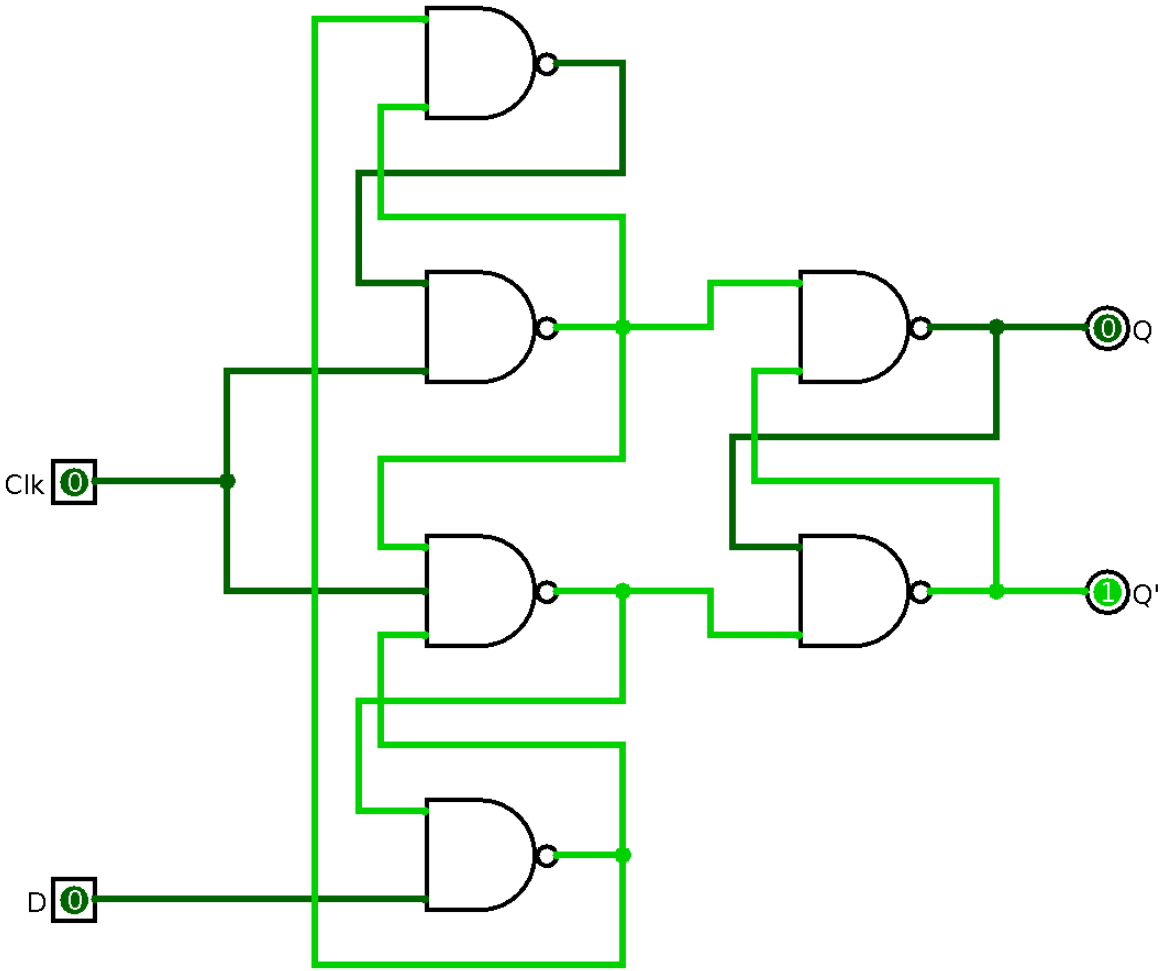
- *latch* bekerja pada level sinyal:
  - *state* dapat berubah selama sinyal kontrol aktif
  - operasi tidak *reliable*
- *flip-flop* hanya bekerja saat transisi sinyal:
  - *positive-edge*: dari *low* ke *high*
  - *negative-edge*: dari *high* ke *low*
  - *state* stabil, hanya berubah pada saat transisi sinyal

D Flip-Flop

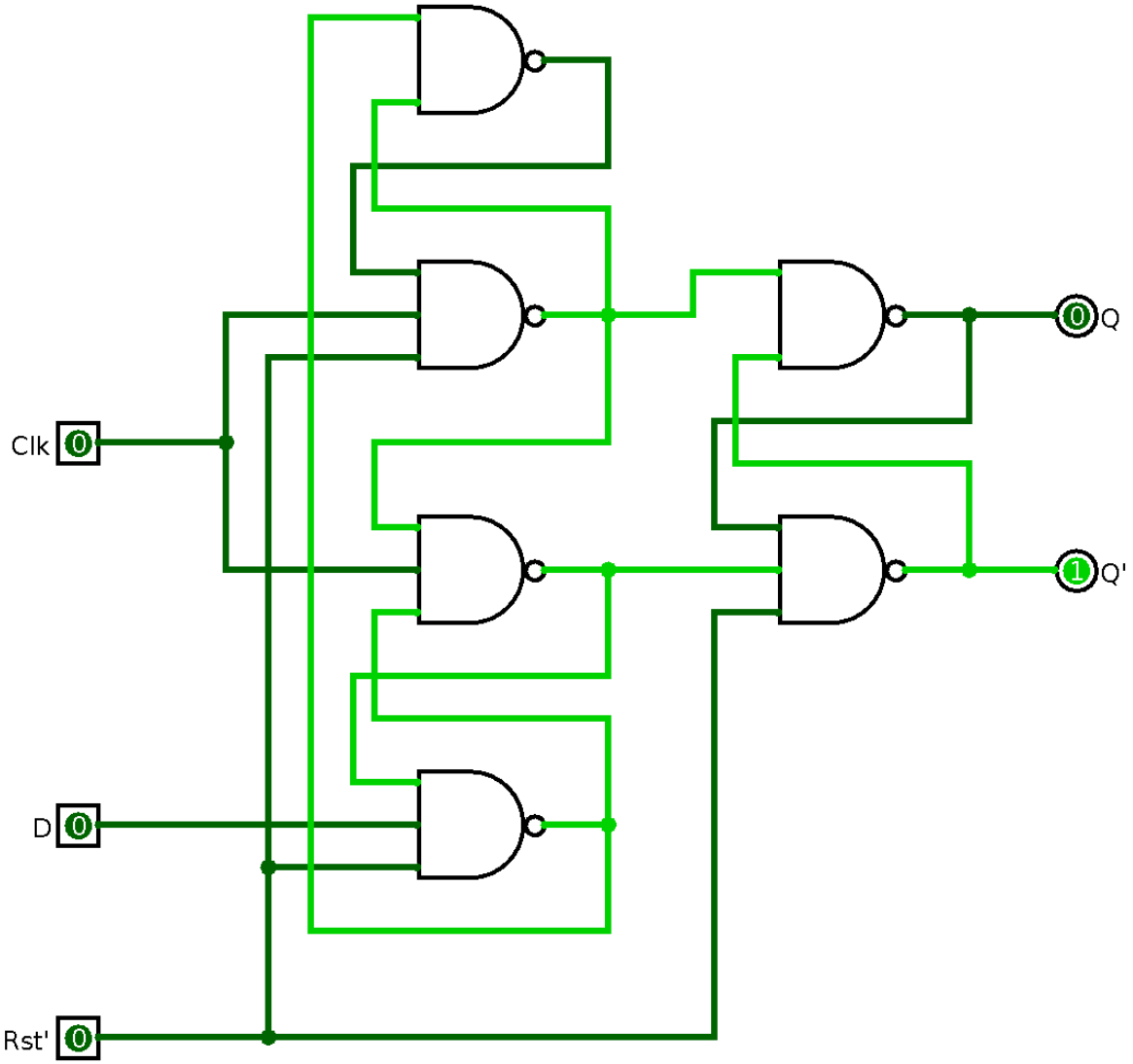
Tabel Karakteristik

D	Q_{t+1}	
0	0	*Reset*
1	1	*Set*

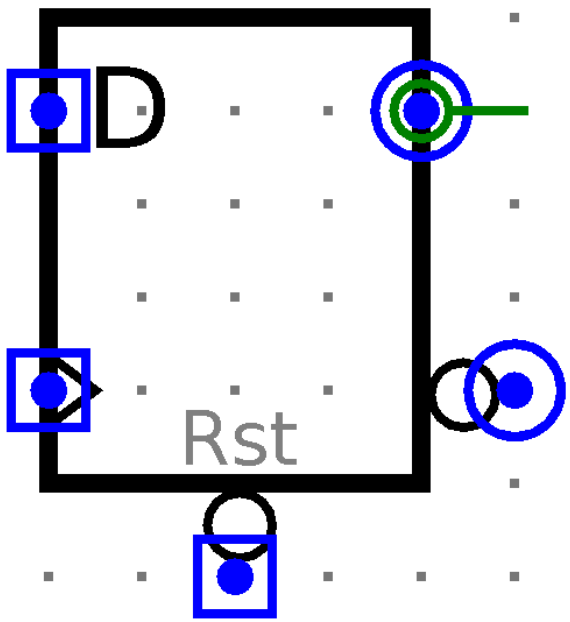
Simulasi: D Flip-Flop



Simulasi: D Flip-Flop with Asynchronous Reset



Simulasi: D Flip-Flop with Asynchronous Reset (IC)

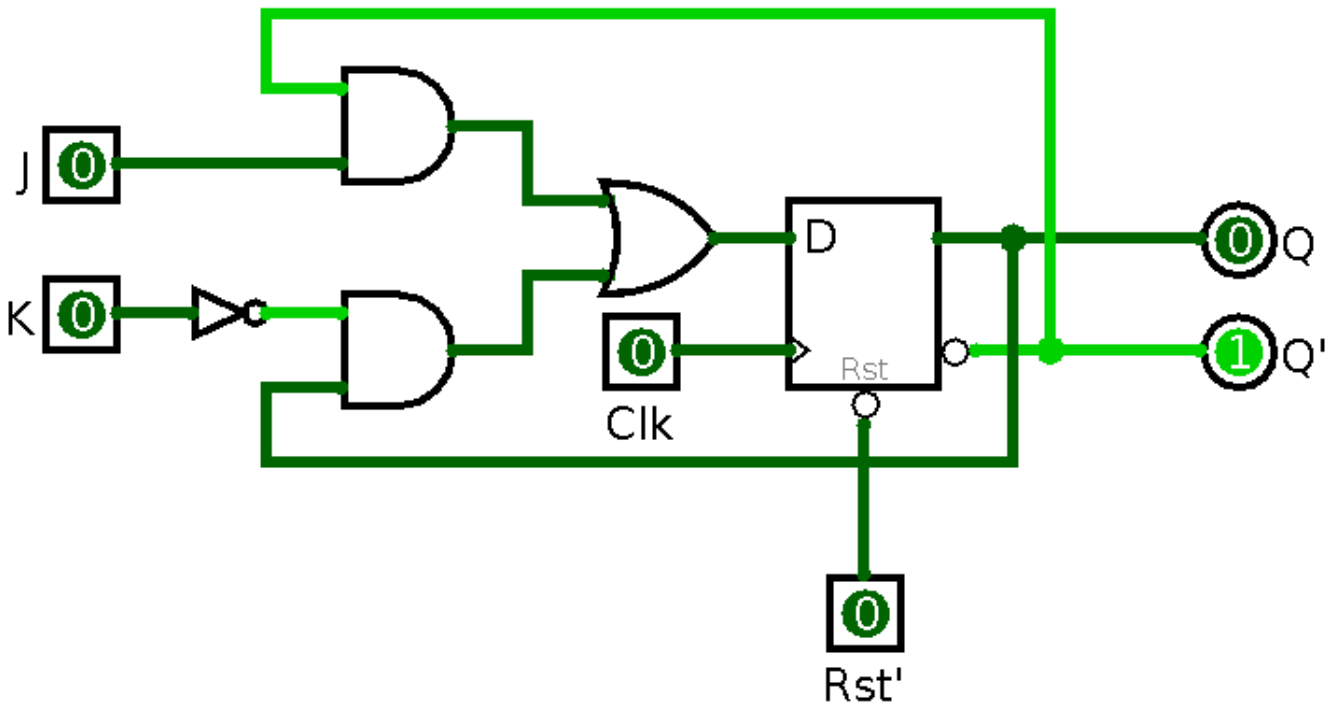


JK Flip-Flop

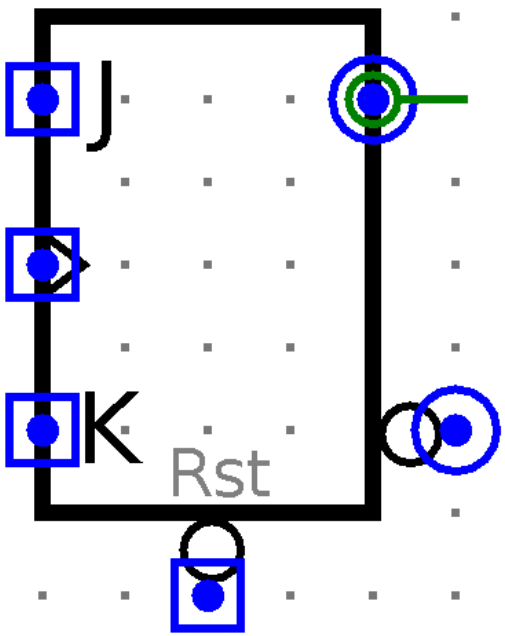
Tabel Karakteristik

J	K	Q_{t+1}	
0	0	Q_t	*No change*
0	1	0	*Reset*
1	0	1	*Set*
1	1	Q'_t	*Complement*

Simulasi: JK Flip-Flop



Simulasi: JK Flip-Flop (IC)

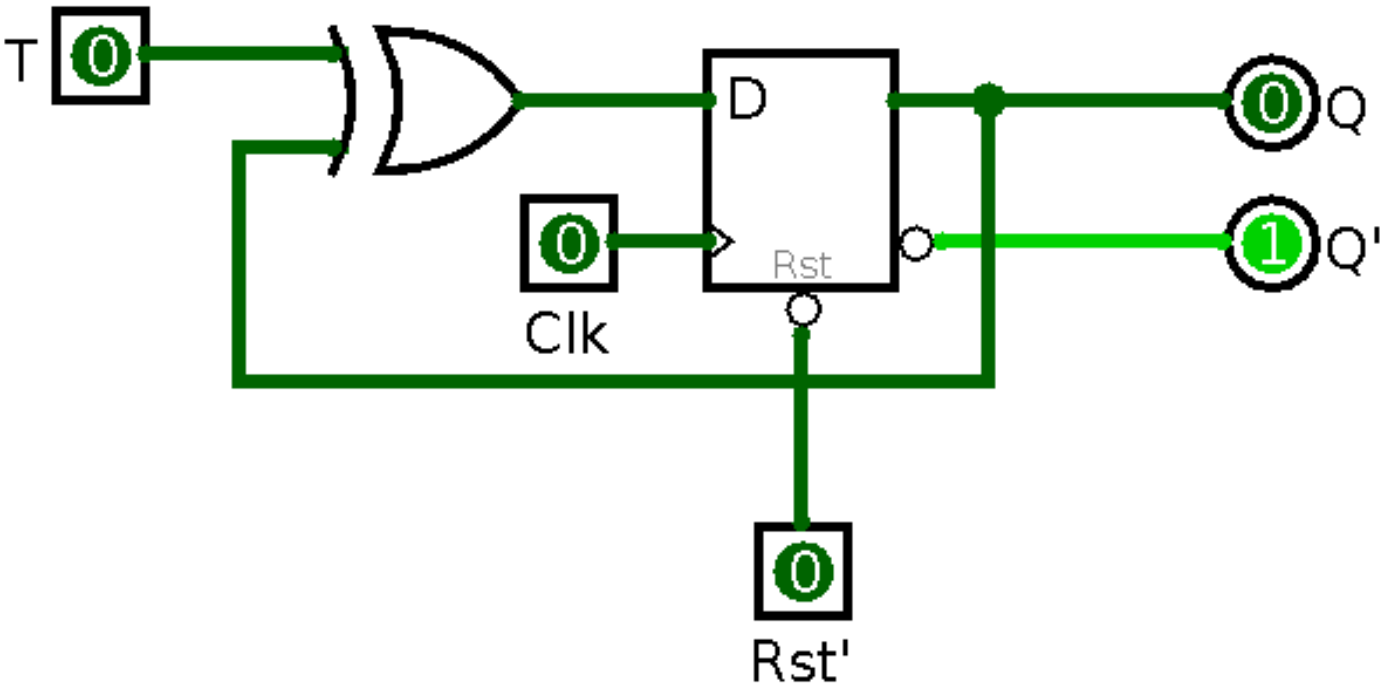


T Flip-Flop

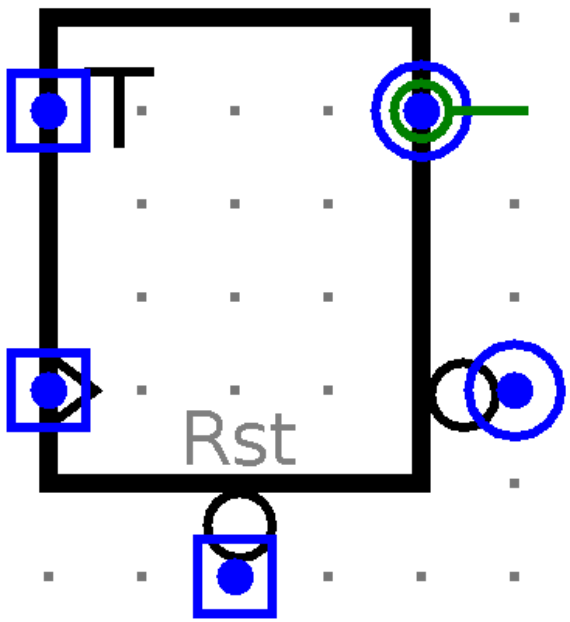
Tabel Karakteristik

T	Q_{t+1}	
0	Q_t	*No change*
1	Q'_t	*Complement*

Simulasi: T Flip-Flop

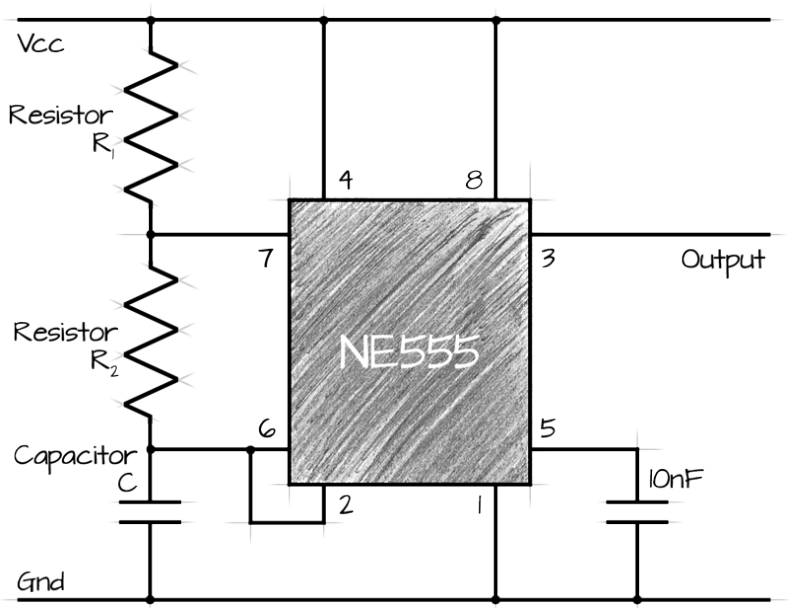


Simulasi: T Flip-Flop (IC)



Implementasi

Clock Generator[1]

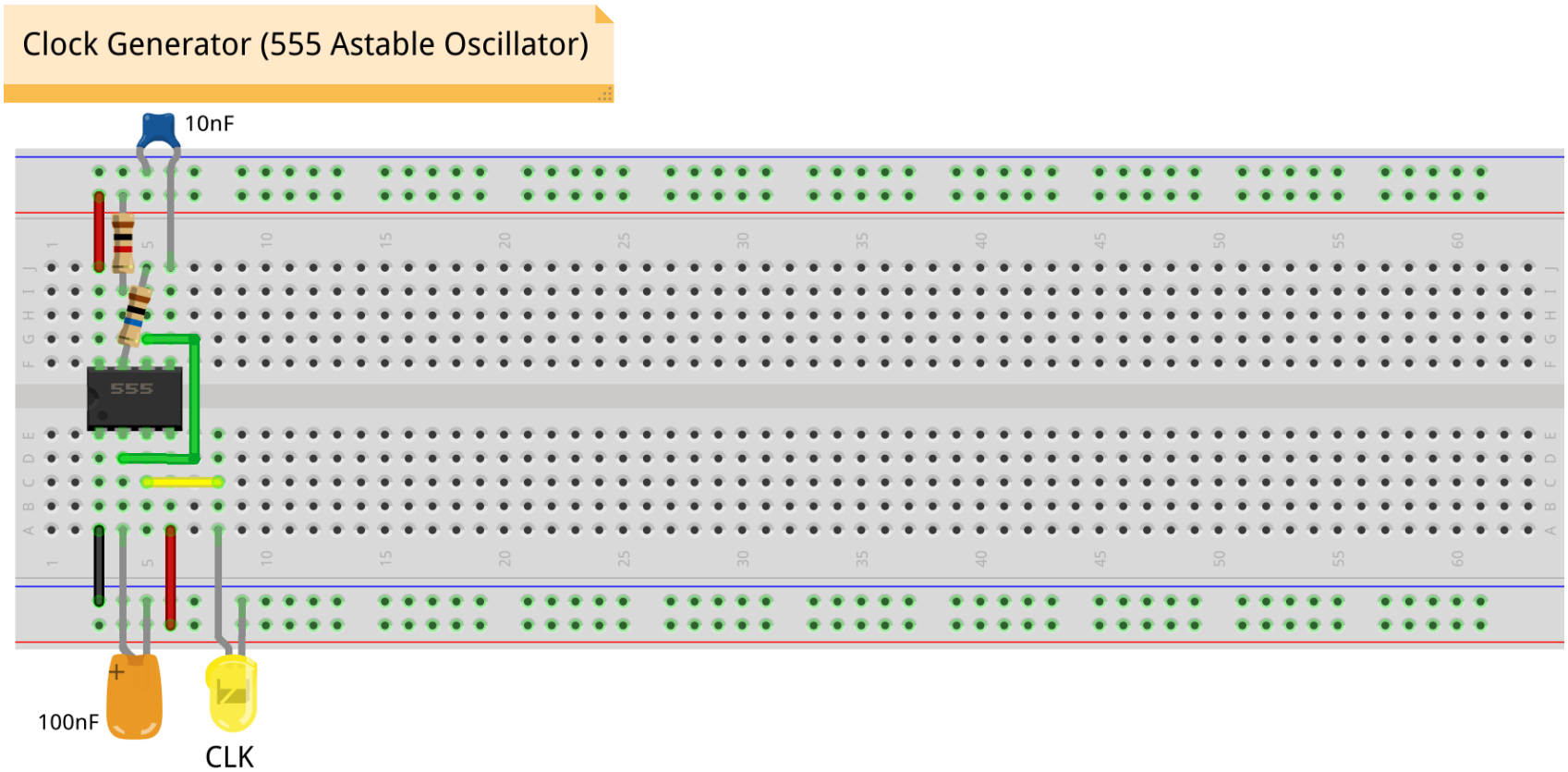


$R_1 = 1\ \text{k}\Omega,\ R_2 = 10\ \text{M}\Omega, C = 100\ \text{nF}$

$\rightarrow T = 1.4\ \text{s}$

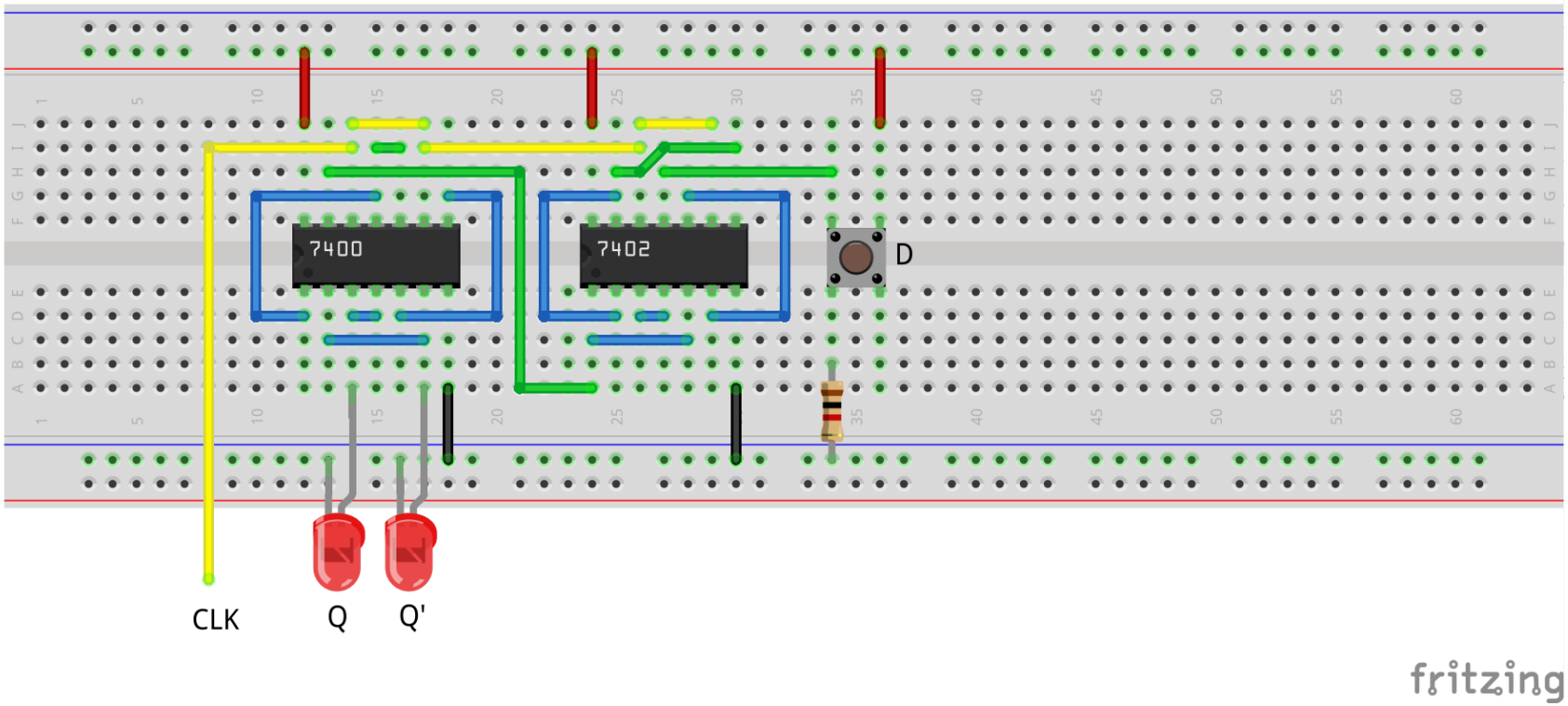
[1] http://www.ohmslawcalculator.com/555-astable-calculator

Clock Generator

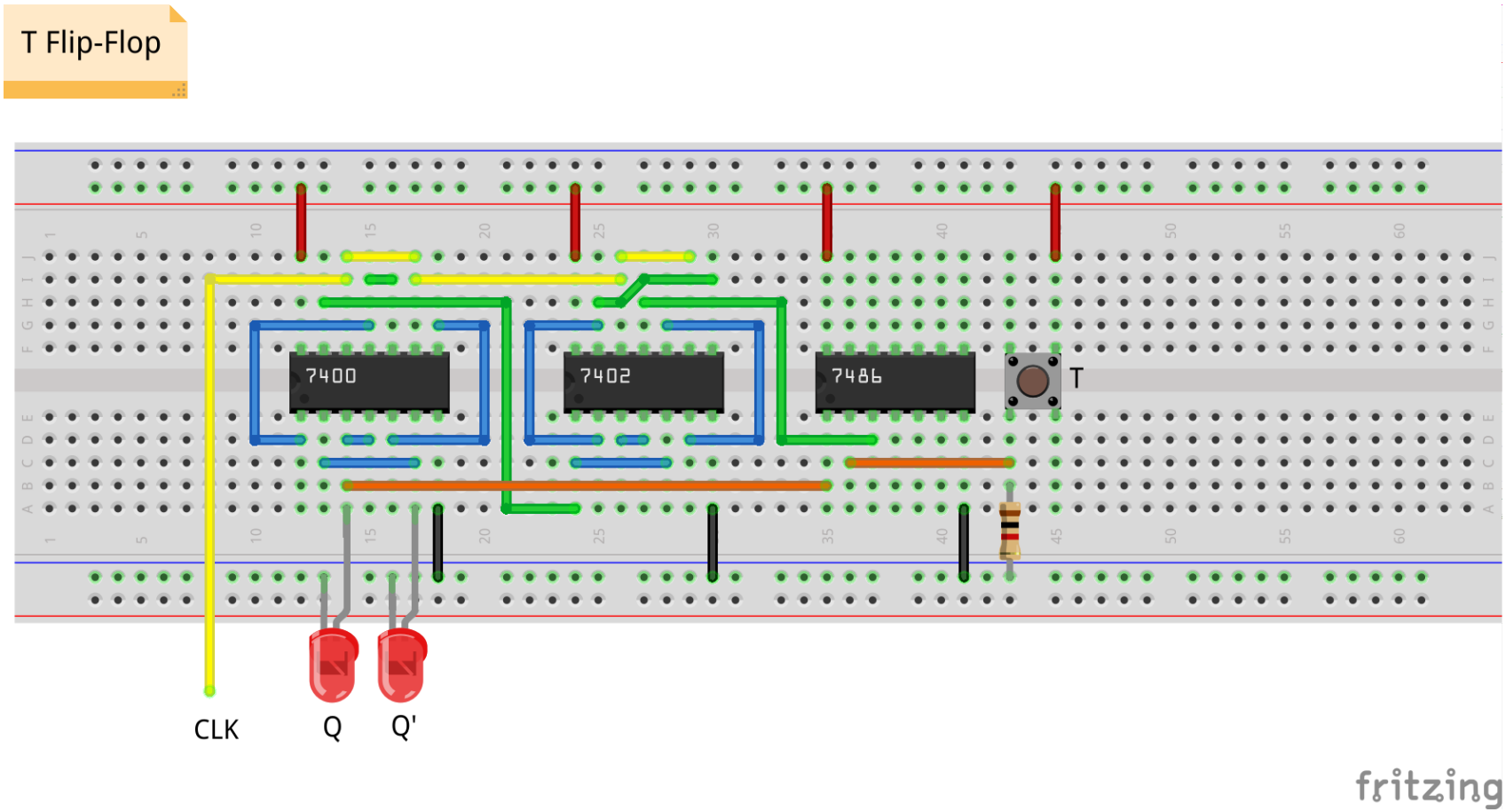


D Flip-Flop

D Flip-Flop (Master-Slave Positive-Edge)



T Flip-Flop



Tugas

Simulasi dan Implementasi Flip-Flop

- Buat simulasi pada Logisim:
  - D flip-flop (with reset)
  - JK flip-flop
  - T flip-flop
- Implementasikan pada *breadboard*:
  - clock generator
  - D flip-flop
  - T flip-flop
- Penilaian langsung pada saat praktikum oleh asprak