

Verilog

Praktikum Rangkaian Digital

Ilmu Komputer IPB

2020

Pengenalan

Verilog

- ▶ *Hardware description language* (HDL)
- ▶ Untuk merancang dan mensintesis rangkaian digital skala besar

Kompilasi Online

- ▶ https://www.tutorialspoint.com/compile_verilog_online.php
- ▶ Kode program ditulis pada panel sebelah kiri
- ▶ Jalankan dengan klik *Execute*
- ▶ Keluaran dapat dilihat pada panel sebelah kanan

Kompilasi pada Geany

- ▶ Simpan dalam *file* berekstensi *.v*
- ▶ Kompilasi dengan *iverilog*
- ▶ Keluaran dapat dilihat dalam *waveform*
- ▶ Pada Geany:
 - ▶ *build*: F9
 - ▶ *execute*: F5
 - ▶ *waveform*: menu *Build – Waveform*

Contoh Kode: XOR

```

/* xor.v */

module _xor(A, B, Y);
    input    A, B;
    output   Y;
    xor      (Y, A, B);
    // assign Y = A ^ B;
endmodule
    
```

```

module _xor_test;
    reg      A, B;
    wire     Y;
    _xor     test(A, B, Y);

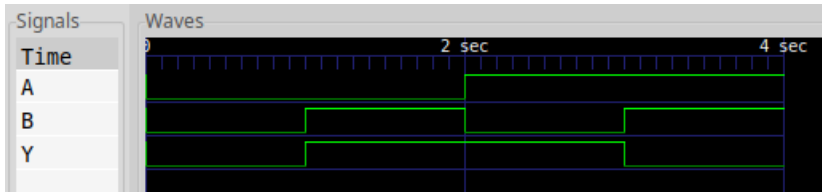
    initial begin
        $dumpvars;
        $monitor("%d: %b %b | %b", $time, A, B, Y);
        A = 0; B = 0;
        #1 A = 0; B = 1;
        #1 A = 1; B = 0;
        #1 A = 1; B = 1;
        #1 $finish;
    end
endmodule

```


Keluaran


VCD info: dumpfile dump.vcd opened for output.

```
0: 0 0 | 0
1: 0 1 | 1
2: 1 0 | 1
3: 1 1 | 0
```






Waveform uji modul _xor

 **codingground**
SIMPLY EASY CODING

Compile and Execute Verilog Online (Icarus v10.0) 

Execute | > Share | main.v | STDIN

```
1 module _xor(A, B, Y);
2     input  A, B;
3     output Y;
4     xor    (Y, A, B);
5 endmodule
6
7 module _xor_test;
8     reg    A, B;
9     wire   Y;
10    _xor    test(A, B, Y);
11
12    initial begin
13        $dumpvars;
14        $monitor("%d: %b %b | %b", $time, A, B, Y);
15        A = 0; B = 0;
16        #1 A = 0; B = 1;
17        #1 A = 1; B = 0;
18        #1 A = 1; B = 1;
19        #1 $finish;
20    end
21 endmodule
22
```

Result   

```
$iverilog -o main *.v
$vpv main
VCD info: dumpfile dump.vcd opened for output.
0: 0 0 | 0
1: 0 1 | 1
2: 1 0 | 1
3: 1 1 | 0
```

Kompilasi Verilog online

Sintaks

Deklarasi modul

- ▶ `module`
- ▶ `endmodule`
- ▶ `input`: masukan
- ▶ `output`: keluaran
- ▶ `wire`: koneksi internal

Gate

- ▶ not
- ▶ and
- ▶ or
- ▶ xor
- ▶ nand
- ▶ nor
- ▶ xnor

Assignment

- ▶ **assign**
- ▶ operator *bitwise*:
 - ▶ ~: NOT
 - ▶ &: AND
 - ▶ |: OR
 - ▶ ^: XOR
- ▶ operator *logical*:
 - ▶ !: NOT
 - ▶ &&: AND
 - ▶ ||: OR

Pengujian

- ▶ `reg`: masukan
- ▶ `wire`: keluaran
- ▶ `initial`
- ▶ `begin`
- ▶ `end`
- ▶ `#delay`

Sistem

- ▶ `$dumpvars`: aktifkan keluaran variabel
- ▶ `$monitor`: cetak variabel jika berubah nilainya
- ▶ `$time`: nilai waktu simulasi saat ini
- ▶ `$finish`: mengakhiri simulasi

Latihan

Latihan Soal di Buku

Kerjakan soal nomor:

- ▶ 3.31(a,b)
- ▶ 3.32(a,b)
- ▶ 3.34
- ▶ 3.39