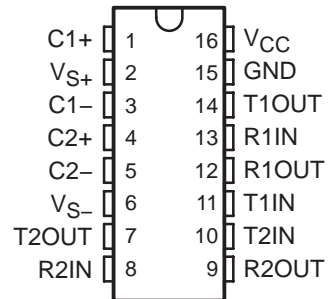


# MAX232, MAX232I DUAL EIA-232 DRIVERS/RECEIVERS

SLLS047L – FEBRUARY 1989 – REVISED MARCH 2004

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0- $\mu$ F Charge-Pump Capacitors
- Operates Up To 120 kbit/s
- Two Drivers and Two Receivers
- $\pm 30$ -V Input Levels
- Low Supply Current . . . 8 mA Typical
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1- $\mu$ F Charge-Pump Capacitors is Available With the MAX202
- Applications
  - TIA/EIA-232-F, Battery-Powered Systems, Terminals, Modems, and Computers

MAX232 . . . D, DW, N, OR NS PACKAGE  
MAX232I . . . D, DW, OR N PACKAGE  
(TOP VIEW)



## description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept  $\pm 30$ -V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MAX232N	MAX232N
	SOIC (D)	Tube of 40	MAX232D	MAX232
		Reel of 2500	MAX232DR	
	SOIC (DW)	Tube of 40	MAX232DW	MAX232
		Reel of 2000	MAX232DWR	
–40°C to 85°C	SOP (NS)	Reel of 2000	MAX232NSR	MAX232
	PDIP (N)	Tube of 25	MAX232IN	MAX232IN
	SOIC (D)	Tube of 40	MAX232ID	MAX232I
		Reel of 2500	MAX232IDR	
	SOIC (DW)	Tube of 40	MAX232IDW	MAX232I
		Reel of 2000	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**MAX232, MAX232I**  
**DUAL EIA-232 DRIVERS/RECEIVERS**

SLLS047L – FEBRUARY 1989 – REVISED MARCH 2004

**Function Tables**

**EACH DRIVER**

INPUT TIN	OUTPUT TOUT
L	H
H	L

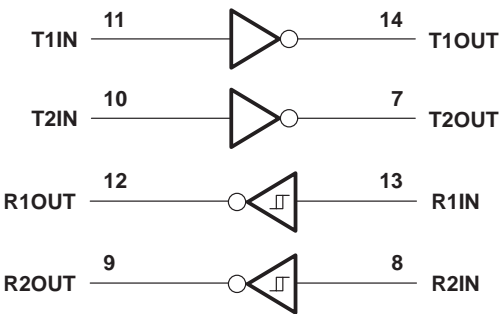
H = high level, L = low level

**EACH RECEIVER**

INPUT RIN	OUTPUT ROUT
L	H
H	L

H = high level, L = low level

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Input supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V_{S+}$	$V_{CC} - 0.3$ V to 15 V
Negative output supply voltage range, $V_{S-}$	–0.3 V to –15 V
Input voltage range, $V_I$ : Driver	–0.3 V to $V_{CC} + 0.3$ V
Receiver	$\pm 30$ V
Output voltage range, $V_O$ : T1OUT, T2OUT	$V_{S-} - 0.3$ V to $V_{S+} + 0.3$ V
R1OUT, R2OUT	–0.3 V to $V_{CC} + 0.3$ V
Short-circuit duration: T1OUT, T2OUT	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): D package	73°C/W
DW package	57°C/W
N package	67°C/W
NS package	64°C/W
Operating virtual junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to network GND.  
2. Maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage (T1IN, T2IN)	2			V
$V_{IL}$	Low-level input voltage (T1IN, T2IN)			0.8	V
R1IN, R2IN	Receiver input voltage			$\pm 30$	V
$T_A$	Operating free-air temperature	MAX232	0	70	°C
		MAX232I	–40	85	

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)**

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$I_{CC}$ Supply current	$V_{CC} = 5.5$ V, All outputs open, $T_A = 25^\circ\text{C}$		8	10	mA

‡ All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 1  $\mu\text{F}$  at  $V_{CC} = 5$  V  $\pm 0.5$  V.

# MAX232, MAX232I

## DUAL EIA-232 DRIVERS/RECEIVERS

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### DRIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	T1OUT, T2OUT R <sub>L</sub> = 3 kΩ to GND	5	7		V
V <sub>OL</sub>	Low-level output voltage‡	T1OUT, T2OUT R <sub>L</sub> = 3 kΩ to GND		–7	–5	V
r <sub>o</sub>	Output resistance	T1OUT, T2OUT V <sub>S+</sub> = V <sub>S–</sub> = 0, V <sub>O</sub> = ±2 V	300			Ω
I <sub>OS</sub> §	Short-circuit output current	T1OUT, T2OUT V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0		±10		mA
I <sub>IS</sub>	Short-circuit input current	T1IN, T2IN V <sub>I</sub> = 0			200	μA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

§ Not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Note 4)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R <sub>L</sub> = 3 kΩ to 7 kΩ, See Figure 2			30	V/μs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/μs
	Data rate	One TOUT switching		120		kbit/s

NOTE 4: Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

### RECEIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	R1OUT, R2OUT I <sub>OH</sub> = –1 mA	3.5			V
V <sub>OL</sub>	Low-level output voltage‡	R1OUT, R2OUT I <sub>OL</sub> = 3.2 mA			0.4	V
V <sub>IT+</sub>	Receiver positive-going input threshold voltage	R1IN, R2IN V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		1.7	2.4	V
V <sub>IT–</sub>	Receiver negative-going input threshold voltage	R1IN, R2IN V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	0.8	1.2		V
V <sub>hys</sub>	Input hysteresis voltage	R1IN, R2IN V <sub>CC</sub> = 5 V	0.2	0.5	1	V
r <sub>i</sub>	Receiver input resistance	R1IN, R2IN V <sub>CC</sub> = 5, T <sub>A</sub> = 25°C	3	5	7	kΩ

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

NOTE 4: Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

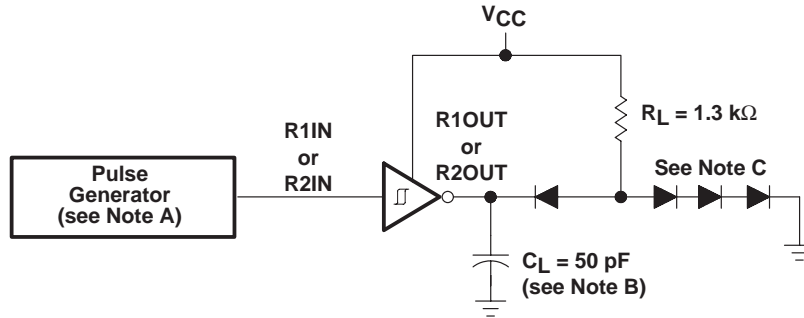
**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Note 4 and Figure 1)**

PARAMETER		TYP	UNIT
t <sub>PLH(R)</sub>	Receiver propagation delay time, low- to high-level output	500	ns
t <sub>PHL(R)</sub>	Receiver propagation delay time, high- to low-level output	500	ns

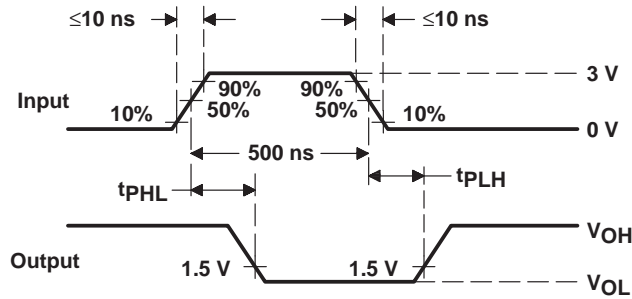
NOTE 4: Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.



## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

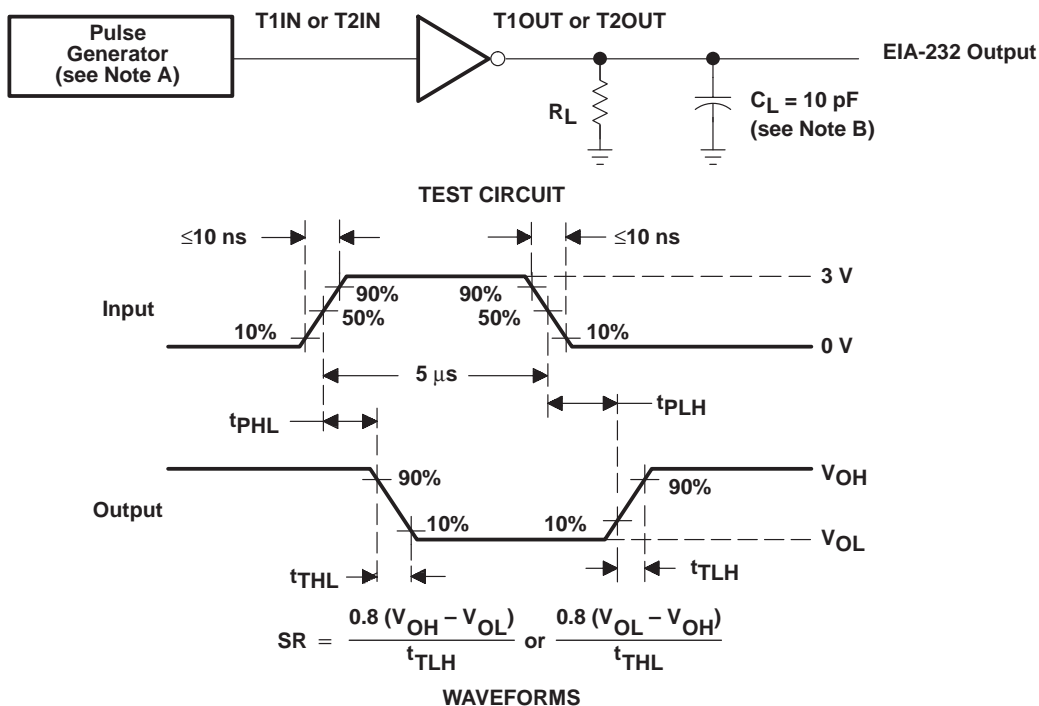
- NOTES: A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .  
B.  $C_L$  includes probe and jig capacitance.  
C. All diodes are 1N3064 or equivalent.

Figure 1. Receiver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements

# MAX232, MAX232I DUAL EIA-232 DRIVERS/RECEIVERS

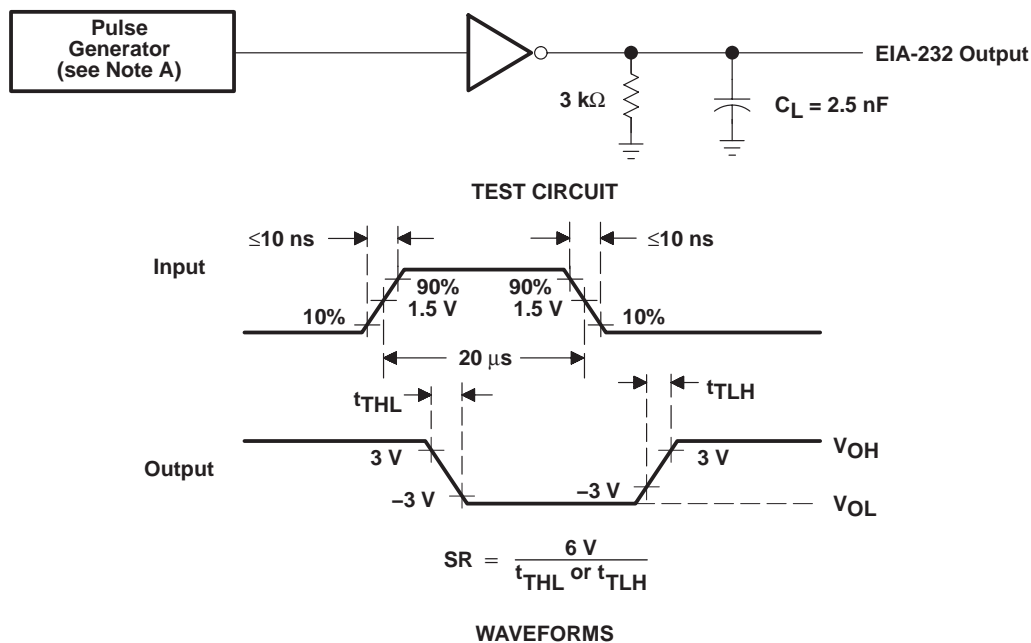
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## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .  
B.  $C_L$  includes probe and jig capacitance.

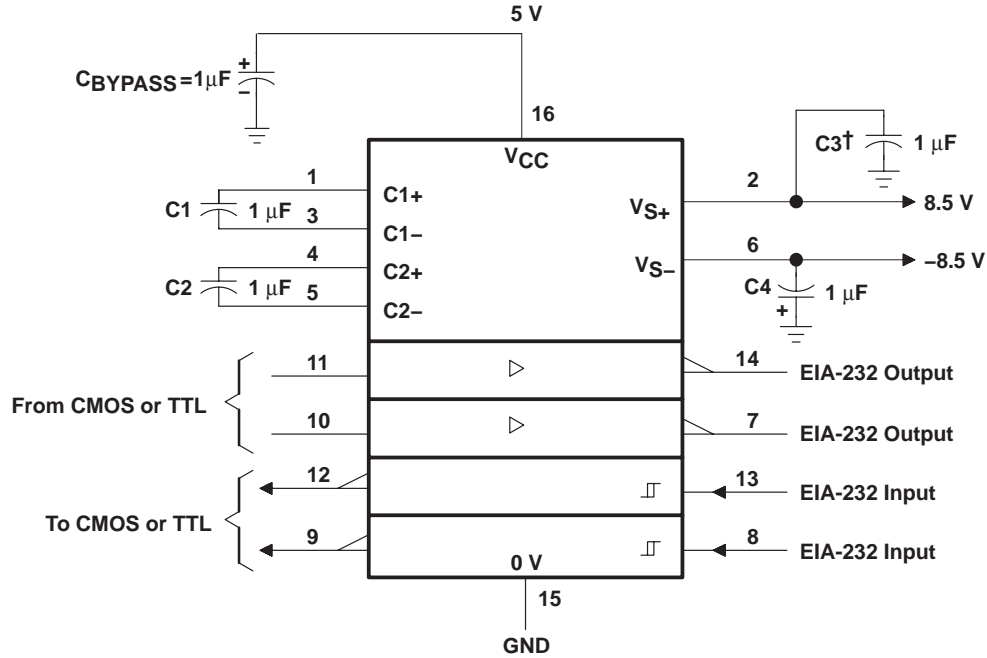
Figure 2. Driver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements (5- $\mu\text{s}$  Input)



NOTE A: The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .

Figure 3. Test Circuit and Waveforms for  $t_{THL}$  and  $t_{TLH}$  Measurements (20- $\mu\text{s}$  Input)

**APPLICATION INFORMATION**



† C3 can be connected to  $V_{CC}$  or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1- $\mu$ F capacitors shown, the MAX202 can operate with 0.1- $\mu$ F capacitors.

**Figure 4. Typical Operating Circuit**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
MAX232D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
MAX232INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

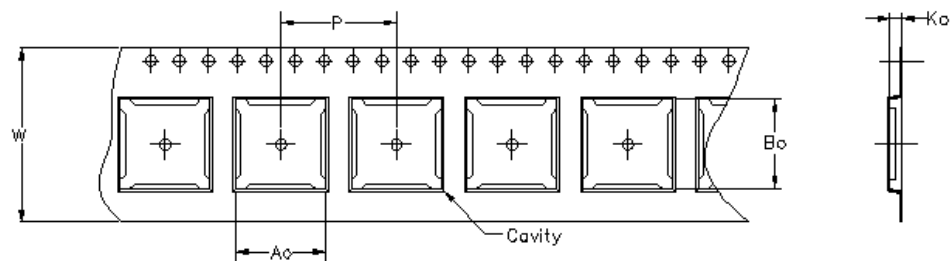
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

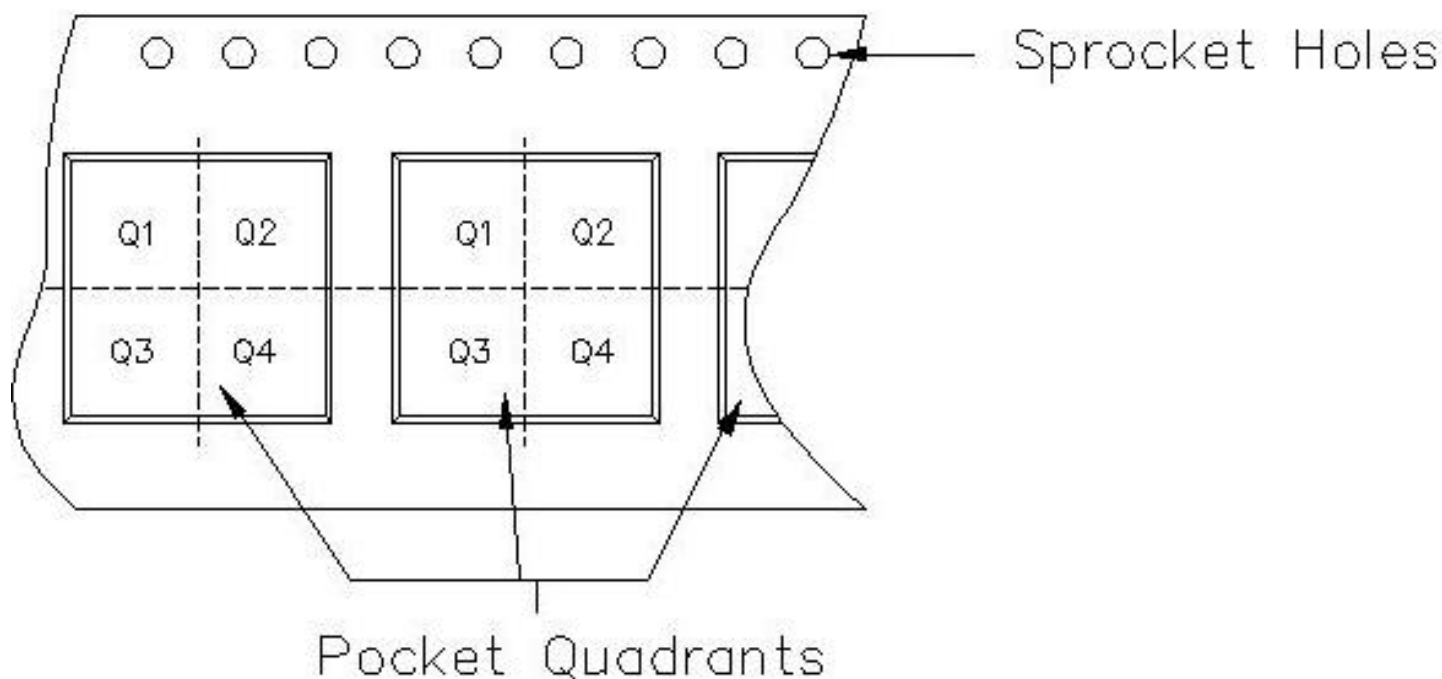
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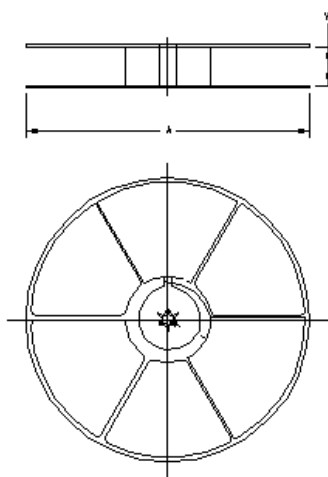
Carrier tape design is defined largely by the component length, width, and thickness.

$A_0$ = Dimension designed to accommodate the component width.
$B_0$ = Dimension designed to accommodate the component length.
$K_0$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



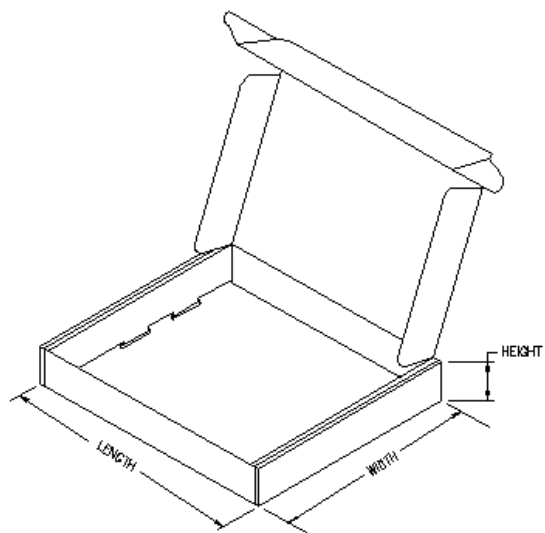
## TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232DR	D	16	FMX	330	16	6.5	10.3	2.1	8	16	Q1
MAX232DR	D	16	MLA	330	16	6.5	10.3	2.1	8	16	Q1
MAX232DWR	DW	16	TAI	330	16	10.75	10.7	2.7	12	16	Q1
MAX232IDR	D	16	FMX	330	16	6.5	10.3	2.1	8	16	Q1
MAX232IDWR	DW	16	TAI	330	16	10.75	10.7	2.7	12	16	Q1
MAX232NSR	NS	16	MLA	330	16	8.2	10.5	2.5	12	16	Q1



## TAPE AND REEL BOX INFORMATION

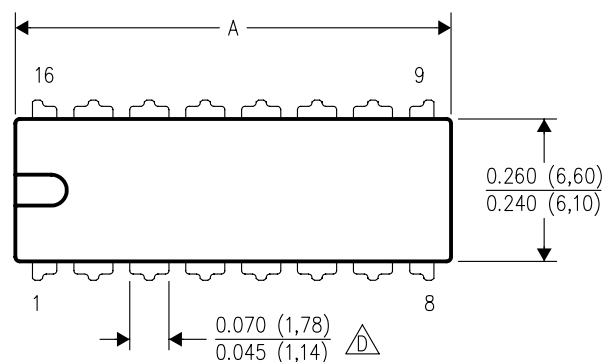
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
MAX232DR	D	16	FMX	342.9	336.6	28.58
MAX232DR	D	16	MLA	342.9	336.6	28.58
MAX232DWR	DW	16	TAI	346.0	346.0	33.0
MAX232IDR	D	16	FMX	342.9	336.6	28.58
MAX232IDWR	DW	16	TAI	346.0	346.0	33.0
MAX232NSR	NS	16	MLA	342.9	336.6	28.58



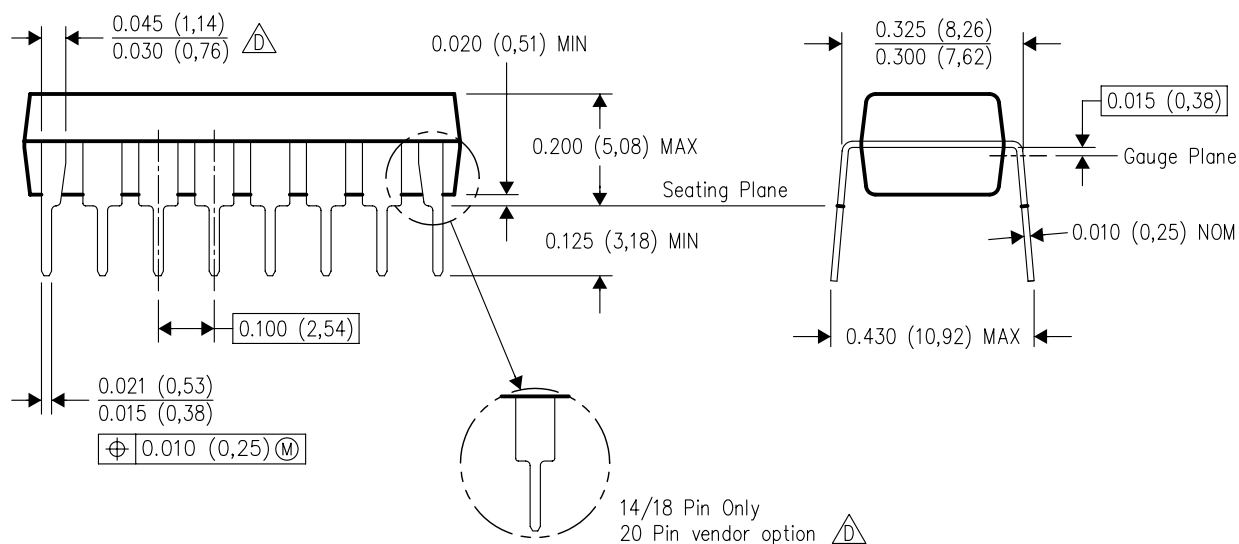
N (R-PDIP-T\*\*)

16 PINS SHOWN



## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

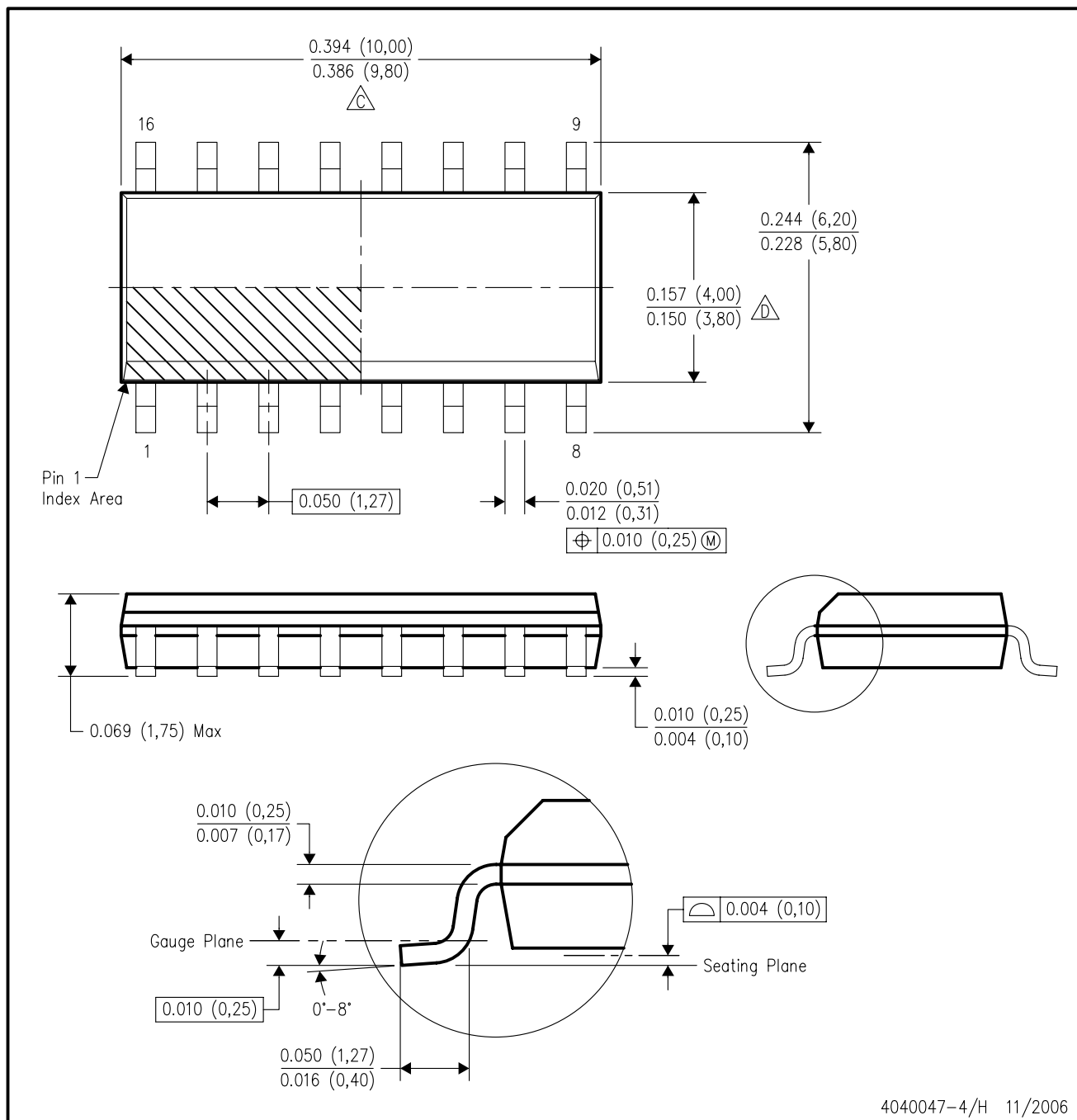


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



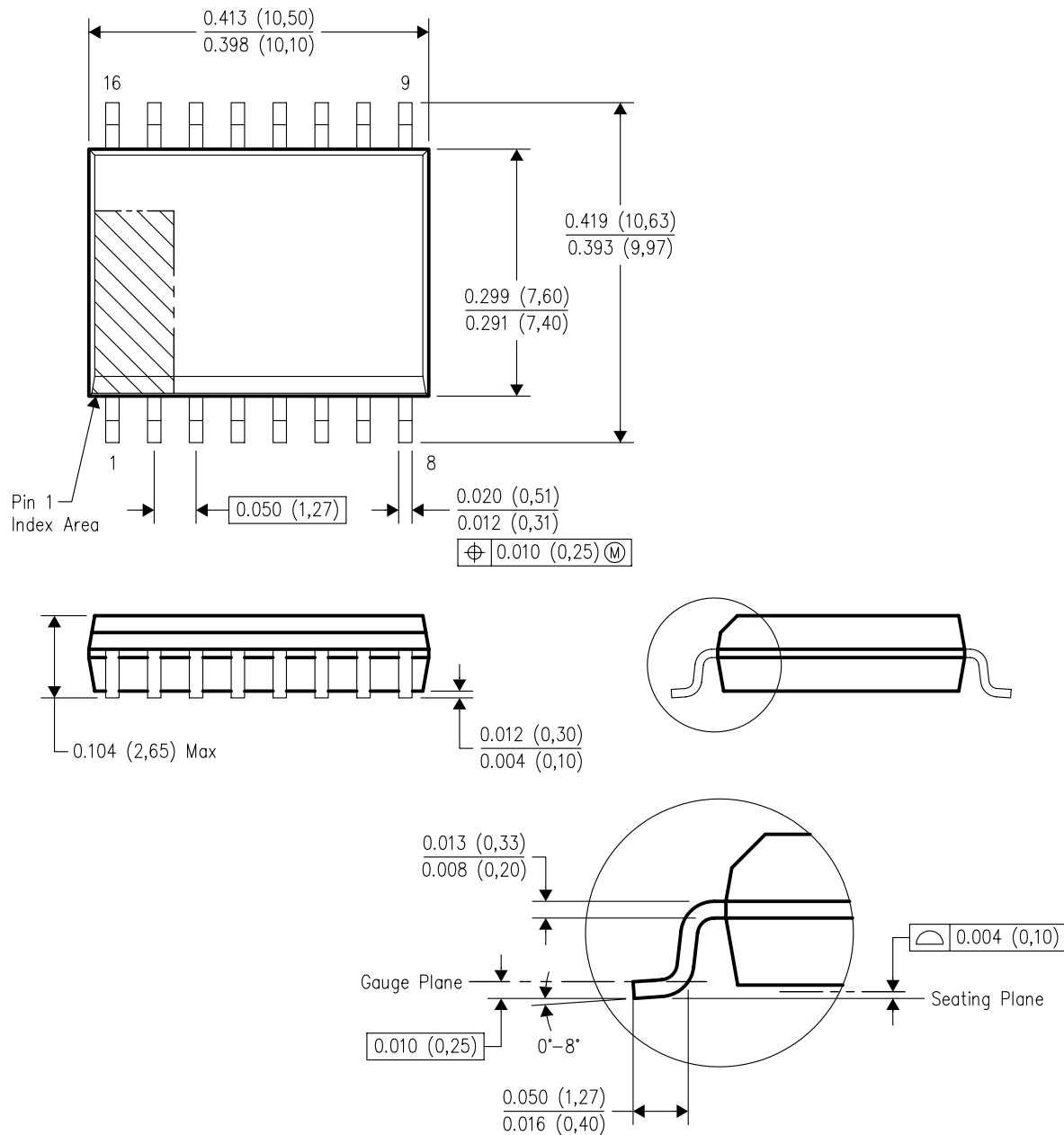
4040047-4/H 11/2006

## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

## DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AA.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## IMPORTANT NOTICE

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