



MIN-YAN HSIEH

Electrical Engineer & Software Engineer
with 2+ years experience



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<https://github.com/ax0080?tab=repositories>

Major

- RISC-V and ARM-Based CPU
- ESL and DFT Design
- Mix-Signal Circuit Design
- GPU and AI Accelerator Design
- AMBA and Bus Protocol
- Machine Learning, Deep Learning
- Compiler Design
- Image Processing
- Quantitative Trading
- Natural Language Processing(NLP)

Education & Awards

Sep 2023 – Present

World Quant Brain, Golden Level in World Quant Brain Alphathon NYC

- Develop Diverse Alpha Analyze, and Optimize for Performance
- WorldQuant Research Consultant for Advanced Alpha analysis

Sep 2022 – Present

National Yang Ming Chiao Tung University

- PhD Candidate in Electrical and Computer Engineering
- Advised by Prof. Chung-Chih Hung

Sep 2019 – June 2022

National Yang Ming Chiao Tung University

- Bachelor's Degree in Electrical and Computer Engineering



Experience

Project Manager(PM), Google Developer Student Club(GDSC) Core Team, September 2023 – June 2024



HTML, CSS, Javascript, jQuery, PHP, .NET, Database, Algorithm, Machine Learning, Deep Learning

- A website that helps us to optimize the school timetable and maximize the general courses we may get
- Use AI to generate a customized and suitable timetable for every student

R&D Engineer, Taiwan Electronic System Design Automation(TESDA) June 2023 – Present



UVM, Test Plan, Design Verification, Computer Architecture, Compiler Design, RISC-V, DLA, GPU, AHB, AXI, PCIe, MIPI, DDR5

- ESL and DFT Design, RISC-V CPU and SoC Design Verification
- NPU, APU and Deep Learning Accelerator(DLA) Development
- AMBA Protocol and SPI, UART, I2C, JTAG, PCIe, MIPI, UCIe and DDR5
- Core, Cache, Fabric, Memory, Codec

All Digital Phase-Locked Loop Program Research Assistant, Novatek Microelectronics Corp. Sep 2022 – August 2024



Matlab, Simulink, Virtuoso, Tapeout, ADC, PLL, PCB Design, Digital Signal Processing(DSP), Delta-Sigma Modulator(DSM)

- Research about fractional Digital Phase-Locked Loop
- Low power and low noise ADPLL applied to RF systems

Computer Vision Development Intern, Industrial Technology Research Institute(ITRI) May 2023 – June 2023



Python, Pytorch, Tensorflow, Machine Learning, Deep Learning

- Use Deep Learning technique to realize object detection
- Image recognition to fulfill the unmanned store

Special Topics in Analog Mixed-Signal Circuit Design, MediaTek September 2022 – January 2023



HSPICE, Matlab, Virtuoso, ADC, SerDes, PLL, CTLE, CDR

- Flash ADC, SAR ADC, Delta-Sigma ADC, Pipelined ADC Design
- CTLE, RX DFE, CDR, Driver, Serializer, Multiplexer, TX FIR Design
- PLL and Ring Oscillator Design

Summer Internship Program in IC Design, RICHTEK Technology July 2022 – August 2022



HSPICE, Finesim, Virtuoso, Spectre, Oscilloscope, Hall Transducer

- Two-stage OP, Folded-cascode OP, LDO analysis and simulation
- Oscillator and bandgap reference circuit analysis
- IC Measurement