



MIN-YAN HSIEH

Electrical Engineer

Electrical and Computer Engineer with 2+ Years Experience in Analog and Mix-signal IC Design, Digital IC Design and Design verification, Development of EDA Tools

Contact



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<https://ax0080.github.io/merwyn.github.io/>

Relevant Skills

- Programming
C/C++, MATLAB, Python
- EDA TOOL
Quartus, Lattice, Modelsim, HSPICE, Virtuoso, Spectre, Verilog, System Verilog
- Equipment Expertise
Oscilloscope, VOM meter, Function Generator, Hall Transducer, FPGA

Major

- Analog Circuit Design
- ESL and DFT Design
- Communication Systems Design and Signal Processing
- RF Microelectronics
- All Digital Phase-Locked Loop
- Analog to Digital Converter
- Mix-Signal Circuit Design

Education

Sep 2022 - Present

National Yang Ming Chiao Tung University

- PhD Candidate in Electrical and Computer Engineering

Sep 2019 - June 2022

National Yang Ming Chiao Tung University

- Bachelor's Degree in Electrical and Computer Engineering

Experience

June 2023 - Present

R&D Engineer

Taiwan Electronic System Design Automation(TESDA)

System Verilog, Design Verification, Computer Architecture, Compiler Design

- Electronic System Level (ESL) and DFT Design, SoC Verification
- NPU, APU and Deep Learning Accelerator(DLA) Development
- AMBA Protocol and SPI, UART, I2C, JTAG Design and Verification

Sep 2022 - August 2024

All Digital Phase-Locked Loop Program

Novatek Microelectronics Corp.

Matlab, Simulink, Virtuoso, Spectre, Tapeout

- Research about fractional Digital Phase-Locked Loop
- Low power and low noise ADPLL applied to RF systems

September 2022 - January 2023

Special Topics in Analog Mixed-Signal Circuit Design

National Yang Ming Chiao Tung University & MediaTek

HSPICE, Matlab, Virtuoso, Spectre, ADC, SerDes, PLL

- Flash ADC, SAR ADC, Delta-Sigma ADC, Pipelined ADC Design
- CTLE, RX DFE, CDR, Driver, Serializer, Multiplexer, TX FIR Design
- PLL and Ring Oscillator Design

July 2022 - August 2022

Summer Internship Program in IC Design

RICHTEK Technology

HSPICE, Finesim, Virtuoso, Spectre, Oscilloscope, Hall Transducer

- Two-stage OP, Folded-cascode OP, LDO analysis and simulation
- Oscillator and bandgap reference circuit analysis

Sep 2020 - June 2022

Special Projects and NYCU ECE Projects Competition

National Yang Ming Chiao Tung University

HSPICE, Virtuoso, Spectre

- LDO with ESR Compensation Design and simulation
- Low-power low-noise CMOS amplifier design