

# NAND Gate using MOSFETs

By : Ayush Agarwal ; B Tech , Electronics Engineering , IIT BHU Varanasi ;

ayush.agarwal.ece20@itbhu.ac.in

**1. Abstract –** This paper presents a technique for creating CMOS combinational circuits using discrete MOSFET transistors. The material presented in this paper is suitable as per B Tech level studies in electronics and is not meant as such for higher use . The nmos and pmos transistors have been approximated as ideal switches for the purpose of the discussion . This paper is to be submitted to IITH Analog Hackathon .

## 2.Introduction -

Complementary Metal-Oxide Semiconductors (CMOS) logic devices are the most common devices used today in the high density, large number transistor count circuits found in everything from complex microprocessor integrated circuits to signal processing and communication circuits. The CMOS structure is popular because of its inherent lower power requirements, high operating clock speed, and ease of implementation at the transistor level. The paper consists of constructing simple NAND gate out of both p and n channel Metal Oxide Semiconductor Field Effect Transistors (MOSFET) .

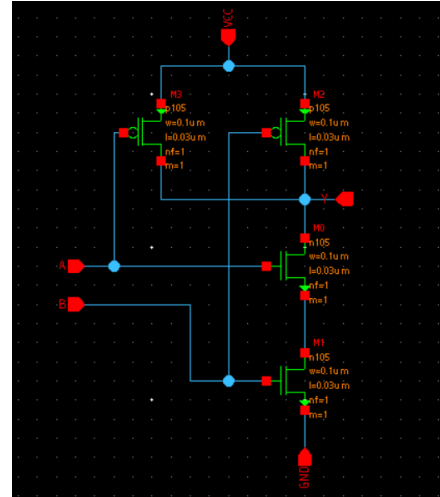
## 3.Reference Circuit Details –

A logic gate is an essential physical device that implements a Boolean function. They are significant building block for efficient performance of circuits . NAND gate is known as a “Universal Gate” since all other logic gates can be expressed in terms of NAND gate .

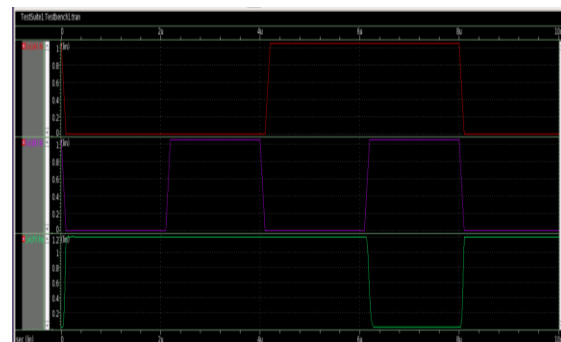
Let A and B be the inputs and Y be the output of the NAND gate . Then the output should be low when both the inputs A and B are high , otherwise the output should be high . This information can be easily encapsulated in the truth table given below :

Table 1 Truth table of NAND gate				
A	B	Pull down network	Pull up network	Output Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

## 4.Reference Circuit Design –



## 5.Reference Waveforms –



A – 0 0 1 1 0

B – 0 1 0 1 0

Y – 1 1 1 0 1

## 6.Reference Papers and Journals –

[\(PDF\) Semi-custom Layout Design and Simulation of CMOS NAND Gate | IJEEE APM - Academia.edu](#)

[Transistor Level Implementation of CMOS Combinational Logic Circuits \(unm.edu\)](#)

