UDYAM'22

ICHIP (ROUND-01)

We are surrounded by a wide variety of data. Each form of data has some importance and by analyzing a set of such data, we are able to understand the past and even predict the future to some extent.

Most of the data available today is in form of images and videos. There are social media pages where millions of images are uploaded daily. Thus, understanding and including image data in our study becomes very important.

Image processing is a method to perform some operations on an image, in order to get an enhanced image or to extract some useful information from it. It is a type of signal processing in which input is an image and output may be image or characteristics/features associated with that image.

In this round we would explore the fundamentals of digital image and design a hardware/Chip to perform very basic operations on the input image.

Before we dive into hardware modelling, it is important that we understand how images are represented digitally. You can follow the links here to enhance your understanding of an image.

→ www.geeksforgeeks.org/digital-image-processing-basics
→ https://www.youtube.com/watch?v=15aqFQQVBWU

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TASK :

You are provided with a grayscale test image which you can download from the link provided below.

https://drive.google.com/file/d/1WrvF9w-czUcnnCqYYILIlX4qmyFGavW9/view?usp=sharing

You are required to design the prototype of a chip which takes the pixel values as input and perform some tasks depending on the state of the 'select' signal.

State of 'select' signal	Operation
2'b00	Increase brightness by 'value'
2,b01	Decrease brightness by 'value'
2'b10	Binarize the image using 'threshold'
2'b11	Invert the image

where

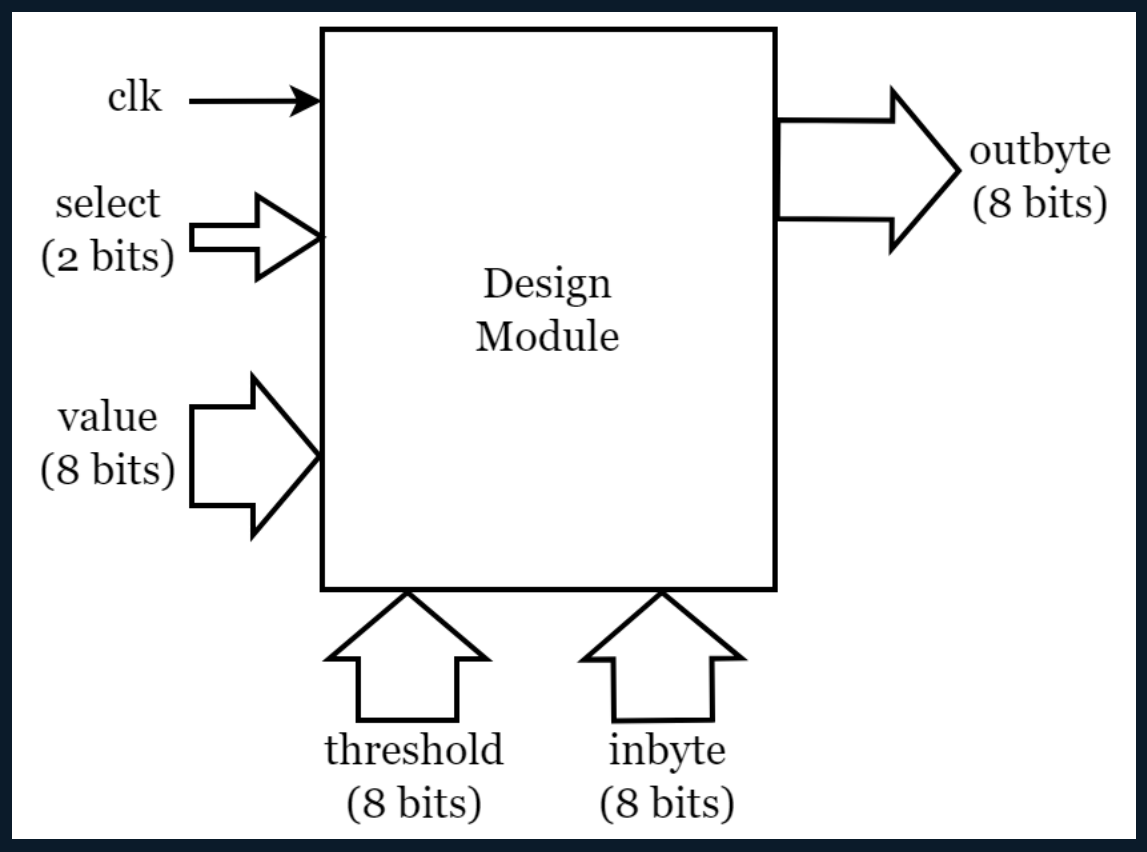
'value' & 'threshold' can be entered by the user.

[Take 'value' = 60 (decimal) & 'threshold' = 160 (decimal) for simulations]

[Hint:

Verilog cannot directly read .jpg files but can read .txt files with hex values using system function $readmemh !!
Try converting the given .jpg file into .txt file using MATLAB or Python.]

Design of prototype :



Owing to limitations in resources, the design module has been fixed by the company as above. Your job is to implement this design module in Verilog and provide a suitable testbench to accomplish the task.

Constraints :

1. Clock Frequency for simulation should be 100 GHz
2. Load entire image into a memory (array of 8 bit registers) of suitable size in the testbench and then supply 8bits (i.e. each pixel value) to the design module at every positive edge of clock.
3. Store each Byte of the output in another memory and finally write its content to a .txt file using $writememh function.
4. Use MATLAB or Python to read this created .txt file to see the result.

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Judging Criteria :

1. How closely you adhere to the given constraints.
2. The final result of the simulation.

Some Tips :

1. Use YouTube or Blogs on internet to learn about grayscale images and about increasing/ decreasing, binarizing and inverting a grayscale image.
2. Take help from YouTube videos in case you have trouble converting image data to text file or vice-versa.
3. The main objective of the event is to learn how hardware circuits work. So, the goal of this round should not just be completing the problem statement but also to visualize the working of hardware circuit that you have created.

Submission :

Create a folder with the following files :

- Text Files of design module and testbench module
- Snapshot of the timing diagram obtained after simulation
- Four (.jpg) grayscale images obtained after simulation taking one state of 'select' at a time.

Upload a single zip file on D2C before the deadline.

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