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Lab 7 - Digital Logic
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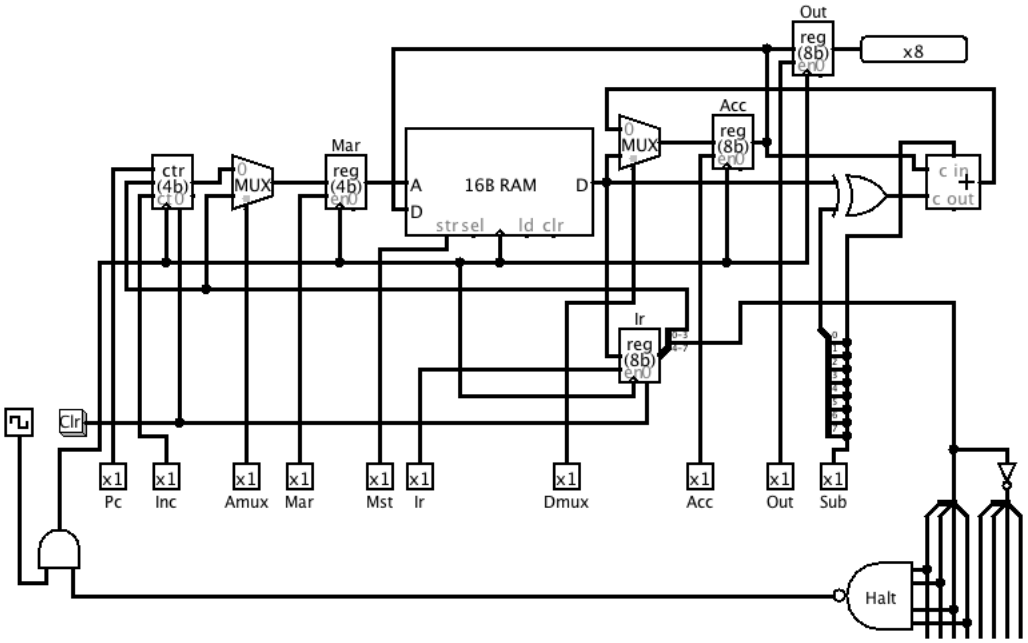
Lab 7

Part 1

- 1-5)



- 6)
  The control code for this circuit has 10 bits.

Part 3

- 1)

Control Code										Action
Pc	Inc	$Amux$	Mar	Mst	Ir	$Dmux$	Acc	Out	Sub	$f(src) \rightarrow dst$
0	1	0	1	0	0	0	0	0	0	$PC \rightarrow MAR; inc(PC)$
0	0	0	0	0	1	0	0	0	0	$Mem(MAR) \rightarrow IR$

- 2)
  Out - 0101001110
  Hlt - 0101010000 (with the right contents at location 01)

- 3)

- a)
  The initial value of the PC and IR are both 0.
- b)
  0101001110
- c)
  0x00 - 0x?? Anything can be here, as long as the most significant digit isn't F, since that will produce a halt signal in the machine. The contents at this address will be sent to the output pin.
  0x01 - 0xF? The most significant has to be F to produce a halt signal to the machine.

- 4)
  The instruction fetch control sequence works as expected. It takes three clock toggles to output the contents at 0x00 and halt.

Part 4

- 1)

Control Code										Action
Pc	Inc	$Amux$	Mar	Mst	Ir	$Dmux$	Acc	Out	Sub	$f(src) \rightarrow dst$
0	1	1	1	0	1	0	0	0	0	$IR \rightarrow MAR$
0	0	1	1	1	0	0	0	0	0	$ACC \rightarrow Mem(MAR)$

  The instruction sequence works as expected.

- 2)
  Once the halt instruction is loaded into the IR, game over; you can't toggle the clock anymore.