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Lab 2 - Digital Logic
October 12, 2013

Lab 2 - Adding Stuff Up

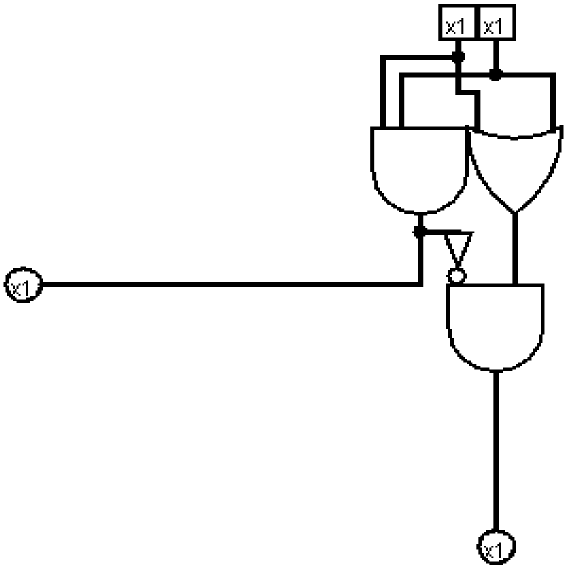
- Part 1 - One Bit Half Adder

1.

A	B	Cout	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

2. $Sum \equiv (A \vee B) \wedge \neg(A \wedge B)$
   $Cout \equiv (A \wedge B)$

3. *One Bit Half Adder*

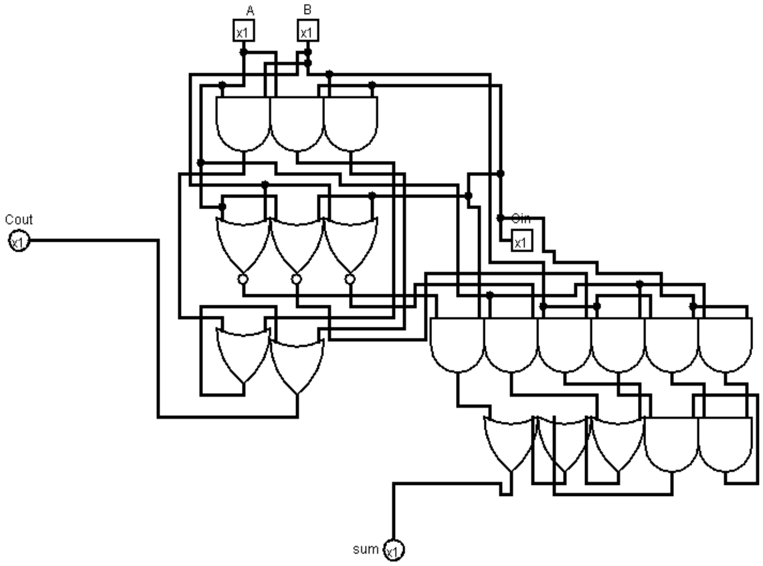


- Part 2 - One Bit Full Adder

1.

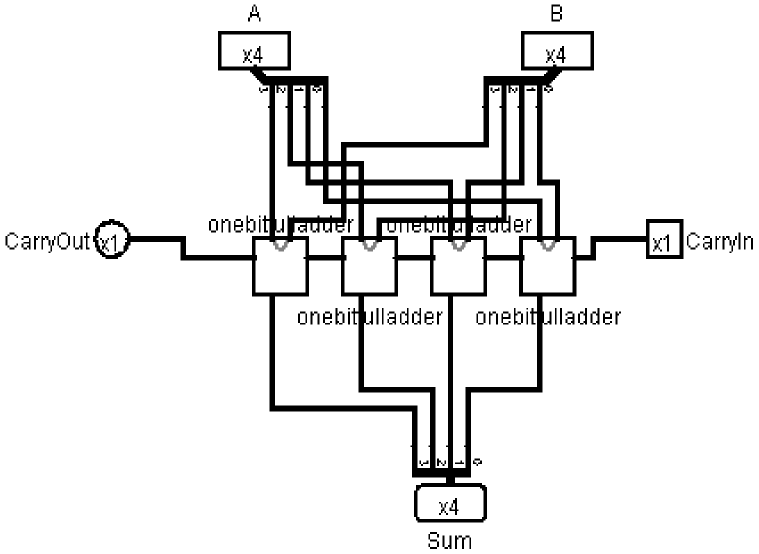
A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

2. $Sum \equiv (\neg A \wedge \neg B \wedge Cin) \vee (\neg A \wedge B \wedge \neg Cin) \vee (A \wedge \neg B \wedge \neg Cin) \vee (A \wedge B \wedge C)$
   $Cout \equiv (B \wedge Cin) \vee (A \wedge Cin) \vee (A \wedge B)$
3. *One Bit Full Adder*



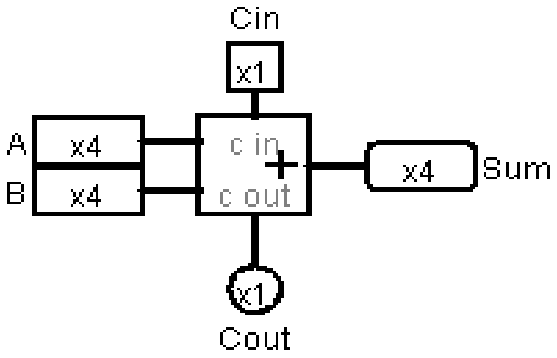
- Part 3 - 4-bit Adder

1. *Four Bit Adder*



- Part 4 - Logisim 4-bit Adder

1. *Logisim Four Bit Adder*



- Questions about a 4-bit Adder

  1. $0_{10}to15_{10}$
  2. *4-bit adder table:*

Bin. A input	Bin. B input	Bin. sum	Dec. A input	Dec. B input	Dec. Sum	Carry
0000	0111	0111	0	7	7	0
1100	0101	0001	12	5	17	1
0101	0101	1010	5	5	10	0
0111	1111	0110	7	12	22	1
0010	0110	1000	2	6	8	0

  3. The only constraint are that the inputs can only be 4 bit unsigned integers, and because of this the circuit will always produce a result that is meaningful considering that there is also a carry out bit.
  4. The carry out pin signifies the 5th bit in the sum.
  5. The four bit adder will use the carry out pin as the ”fifth bit” for the sum.