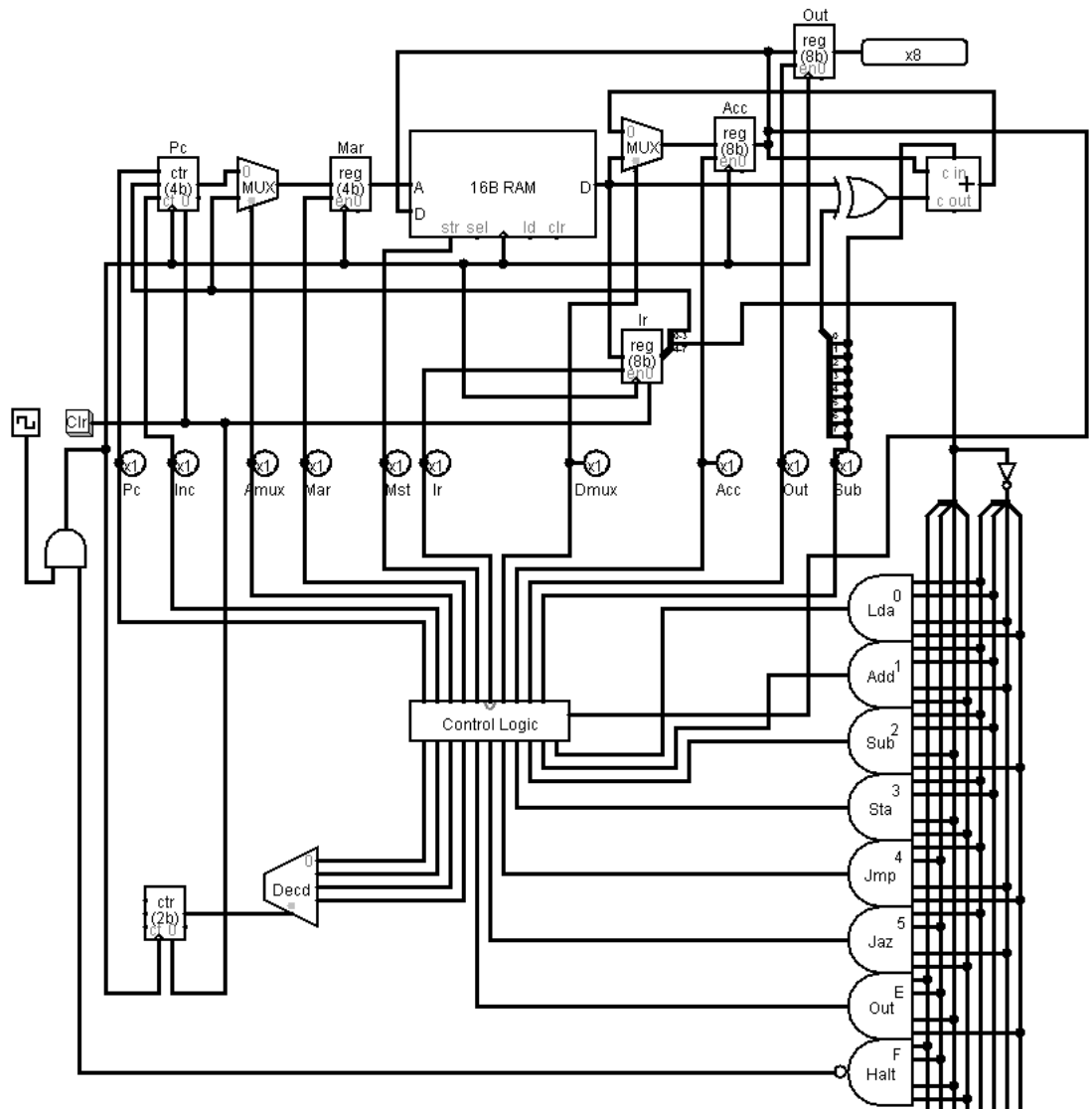
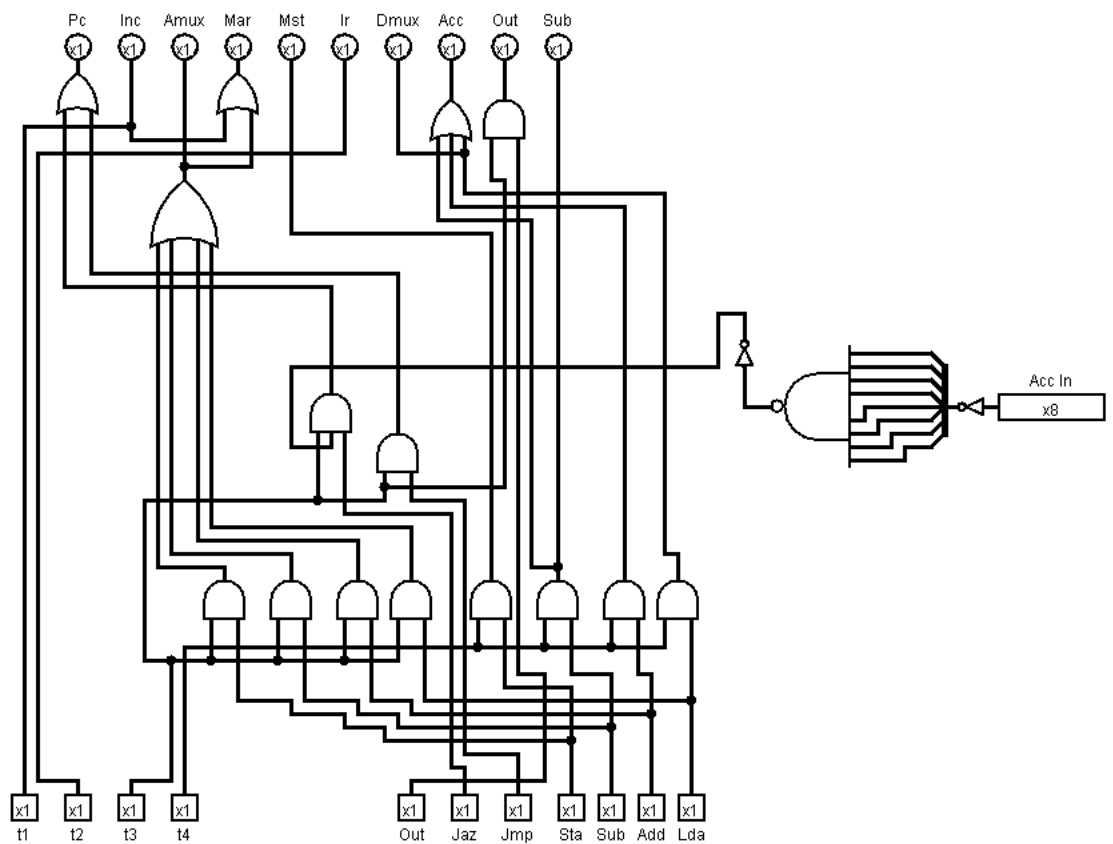


Lab 8

- 1)
Main:



Control Logic Component:



2)

I loaded up the ram with the following instructions and data. As you can see it includes all of the available instructions.

| | | | | | |
|---|-----|-----|----|-----|----|
| | 0 | 0f | 2e | 54 | 41 |
| | 4 | 1e | 1e | 3d | ee |
| A | 8 | ff | 00 | 00 | 00 |
| D | c | 00 | 00 | 02 | 08 |
| | str | sel | ld | clr | |

After clocking it until Halt, the result was this:

| | | | | | |
|---|-----|-----|----|-----|----|
| | 0 | 0f | 2e | 54 | 41 |
| | 4 | 1e | 1e | 3d | ee |
| A | 8 | ff | 00 | 00 | 00 |
| D | c | 00 | 04 | 02 | 08 |
| | str | sel | ld | clr | |

And the output pin was four:

