SEGA SG-1000

To VDP (TMS9918)

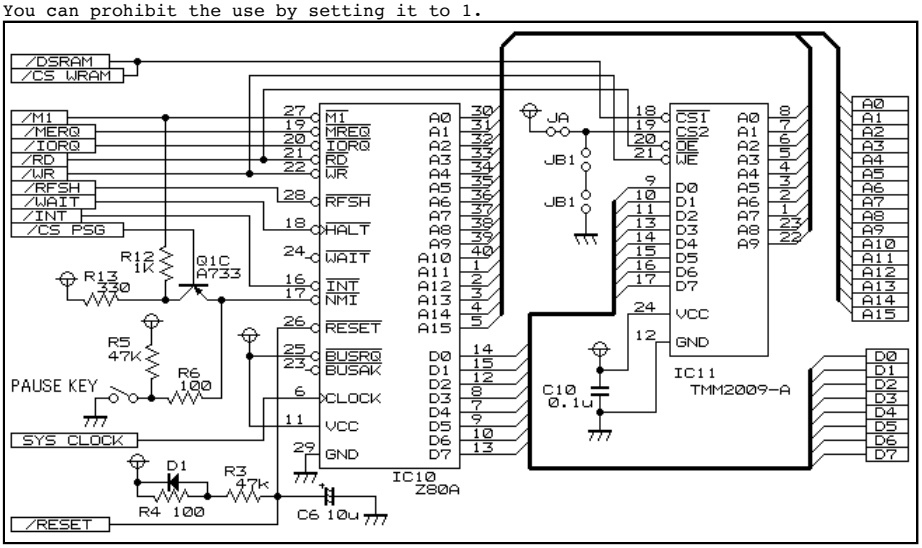
SEGA SG-1000 specs

CPU	D780C-1 (Z80A) 3.579MHz
VDP	TMS9918A
PSG	SN76489
ROM	Supplied by slot
RAM	1KB (expandable)
V-RAM	16KB

Cut down the parts that can be used in the SC-3000 game to the minimum
The area around the input I / O port is slightly different, but the optional SK-1100 covers it.
The simplicity of the main circuit is interesting (it's a pity that PSG access is weighted)
Actually, porting overseas software is often secretly done and good.
The structure is quite similar to ColecoVision, so it should be easy to port (the bottleneck is that the interrupts are different).

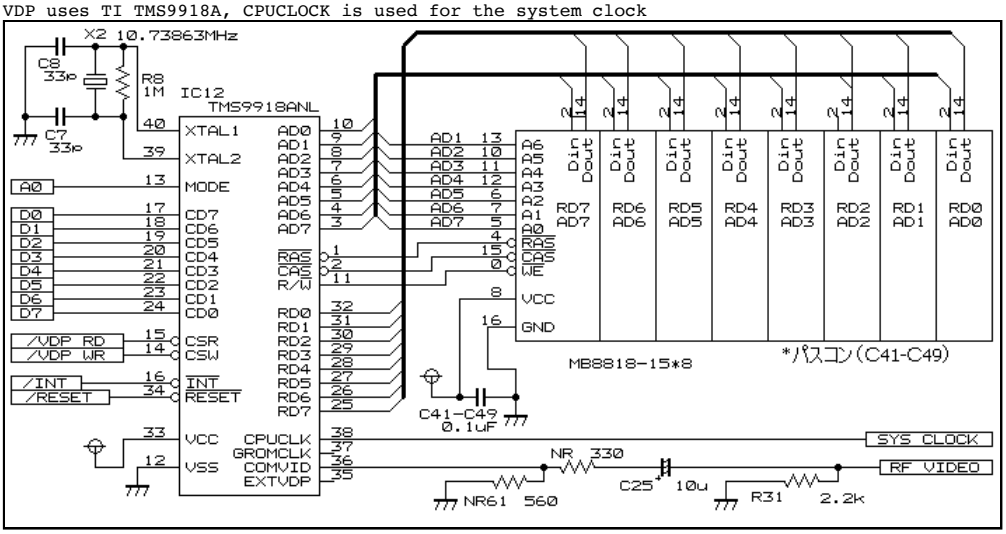
CPU

CPU uses Z80A Clock is about 3.579MHz
Interrupt is assigned to mode 1, NMI is assigned to the pause key, and INT is assigned to VSYNC.
Also, the IC used in the work RAM (IC11)
With TMM2009-A, jumper JA is shorted, JB1 and JB2 are cut.
For TMM2009-B, short jumpers JB1 and JB2 to cut JA.
/ ORAM is connected to / CS of SRAM in the main body
You can prohibit the use by setting it to 1.



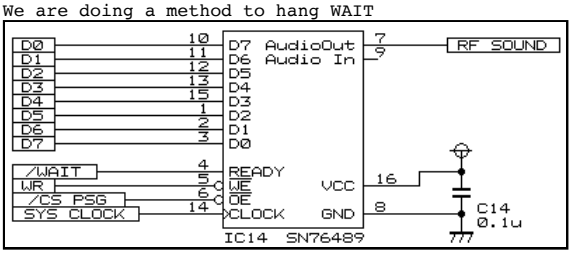
VDP

VDP uses TI VMS9918A, CPUCLOCK is used for the system clock



PSG

SN76489AN is used, the clock is 3.759MHz,
MSB is connected to D0 and LSB is connected to D7.
READY is connected to CPU / WAIT
SN76489 receives the command
Since it takes 32 clocks, it is necessary to stop the CPU.
There is also a way to provide a latch, but SG-1000 is for cost reasons.
We are doing a method to hang WAIT

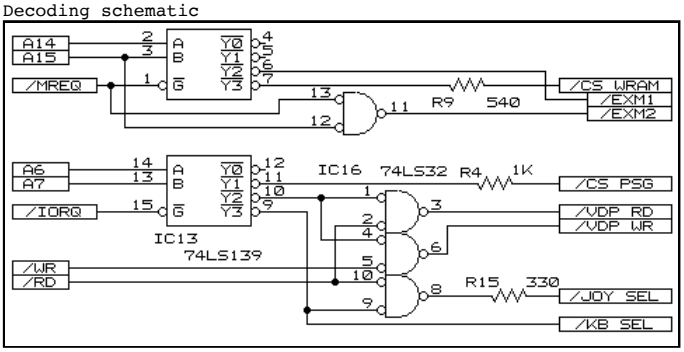


ROM
ROM is not built in the main body,
It will be supplied by cartridge or card
Large capacity like mega ROM
Controlled by the mapper of the cartridge (portrait of Loretta)

RAM
SG-1000 internal RAM is 1K bytes (0C000H-0C3FFH)
The RAM inside the SG-1000II main unit is 2K bytes (0C000H-0C7FFH).
Disable the use of RAM in the main unit from the cartridge (B3 is always 1)
It is designed so that RAM that overlaps with the main work can be added.
Overseas, insert it between the main unit and the ROM cartridge with an extended RAM expander.
There is hardware that can be done

B4 can be added as / CS and 08000H-0BFFFH can be added as RAM or ROM.

Decoding schematic



08000H-0BFFFH: / EXM1
000000H-07FFFH: / EXM2
0C000H-0FFFFH: / CS WRAM

I / O port
With SG-1000, only A7 and A6
Since it controls the port, it is separated by 040H.
Only use specific addresses to maintain compatibility with other models
  000H-03FH: Unused
  040H-07FH: PSG SN76489AN using port 07FH
  080H-0BFH: VDP TMS9918A port 0BEH-0BFH used
  0C0H-0FFH: JOY, using SK-1100 port 0DCH-0DFH

Port 07FH
  PSG port
  When you access it, it will take about 32 clocks of WAIT.

Port 0BEH-0BFH
  VDP port

Port 0DCH
  Used to identify the joypad and the main unit Shared with SK-1100
  For SG-1000 only
    d7: JOY2 pin 2 (DOWN) 1 = off, 0 = on
    d6: JOY2 1 pin (UP) 1 = off, 0 = on
    d5: JOY19 pin 9 (2 buttons) 1 = off, 0 = on
    d4: JOY1 6-pin (1 button) 1 = off, 0 = on
    d3: JOY1 4-pin (RIGHT) 1 = off, 0 = on

d2: JOY1 pin 3 (LEFT) 1 = off, 0 = on
d1: JOY1 pin 2 (DOWN) 1 = off, 0 = on
d0: JOY1 pin 1 (UP) 1 = off, 0 = on

Port 0DDH
For SG-1000 only
d7: Fixed with pin 1 of IC21 74LS257 (unused)
d6: Fixed with pin 1 of IC21 74LS257 (unused)
d5: Fixed with 6-pin 1 of IC21 74LS257 (unused)
d4: CON terminal 1 = off, 0 = on
d3: JOY2 9-pin (2 buttons) 1 = off, 0 = on
d2: JOY2 6-pin (1 button) 1 = off, 0 = on
d1: JOY2 4-pin (RIGHT) 1 = off, 0 = on
d0: JOY2 pin 3 (LEFT) 1 = off, 0 = on

Port 0DCH-0DFH: For SK-1100
8255 is used and 0DCH-0DFH is used.
PA is 0DCH, PB is 0DDH, PC is 0DEH, CW is 0DFH.
The lower 3 bits of 0DEH become the key select
No. In the case of 0 to 6, port 0DDH and port 0DCH become keyboard data and read the data as PB and PA.
No. In the case of 7, port 0DDH and port 0DCH read the data as the JOY terminal of the main unit.

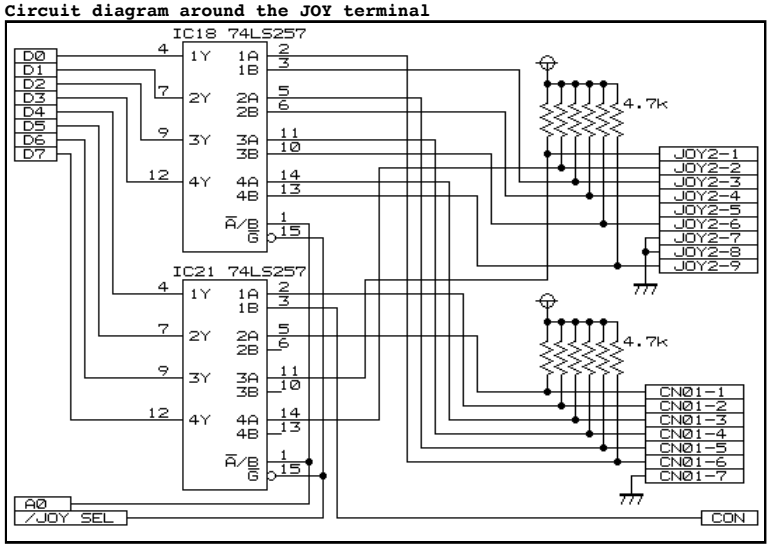
For arcade boards
Port 0DCH
d7: 2P START
d6: 1P START
d5: JOY1 2 button
d4: JOY1 1 button
d3: JOY1 right
d2: JOY1 left
d1: Below JOY1
d0: Above JOY1

Port 0DDH
d7: coin
d6: Service SW
d5: JOY2 2 button
d4: JOY2 1 button
d3: JOY2 right
d2: JOY2 left
d1: Below JOY2
d0: Above JOY2

Port 0DEH
Used for DIP SW.

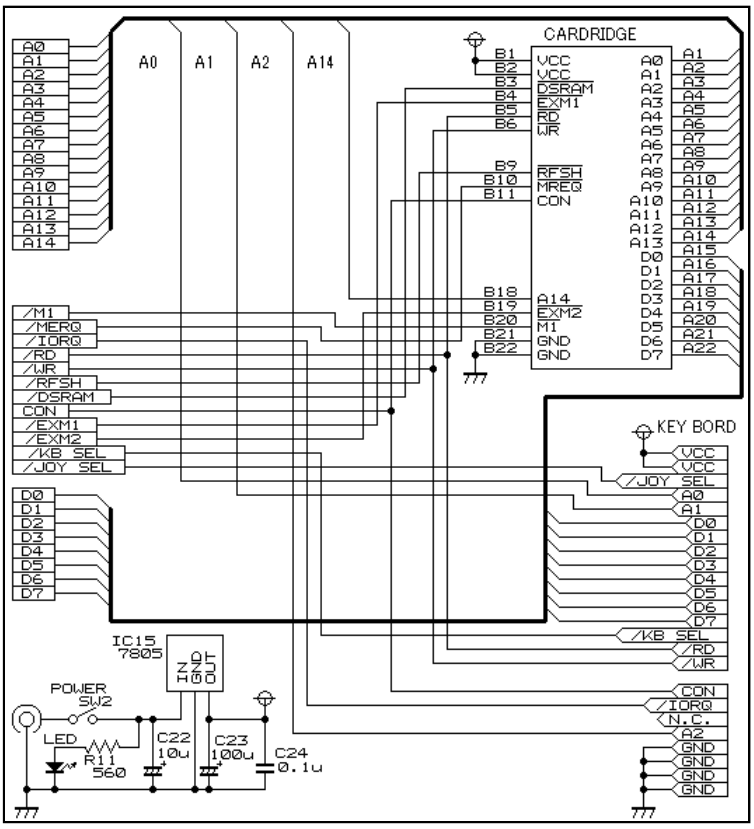
Port 0DFH
8255 (custom chip depending on the board) CW

Circuit diagram around the JOY terminal



Use is prohibited by setting 3 pins (/ JOY SEL) = 1 of the expansion terminal.
1P JOYSTICK is attached directly to the main body, but it can be made into a connector as an option.

Circuit diagram of connectors, etc.



/ DSNA of B3 terminal seems to mean that RAM in the main body is selected by opening this terminal.
SG-1000 has / M1 on B20

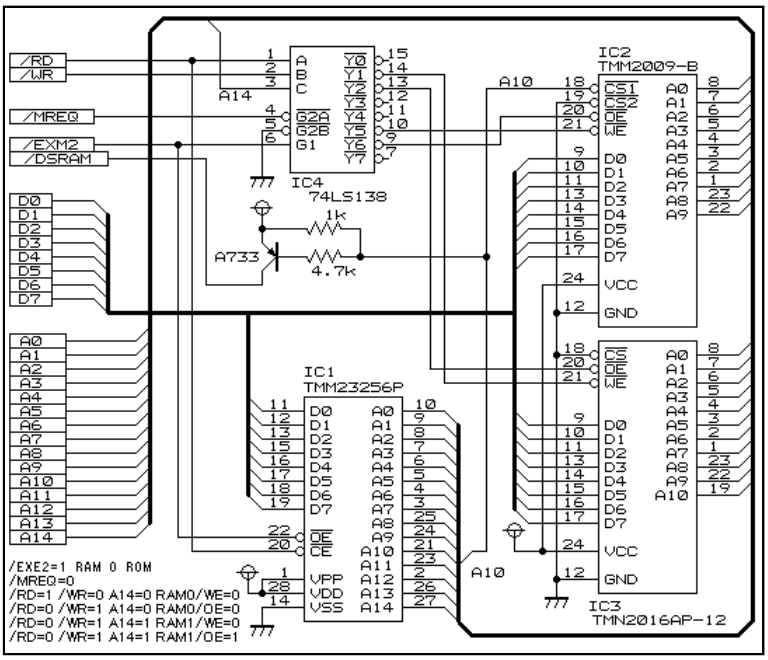
Memory expander
Peripherals that expand memory to port MSX games are out in Taiwan
1KB or 2KB is not enough for the main memory
It has the lowest capacity of 8KB within the MSX standard.

Extended type of RAM8KB (unconfirmed)
  A type that expands by mounting SRAM on 0C000H-0DFFFH
  This type seems to be able to start without a memory expander in MARK III or later.

Type with MSX BIOS (unconfirmed)
  It has the same address as the minimum MSX BIOS (unused addresses jump to 00000H)
  The game itself will have the same address as MSX

    00000H-01FFFH ROM BIOS used for games
    02000H-03FFFH RAM Work for games
    04000H-07FFFH ROM game body 0
    08000H-0BFFFH ROM game body 1?
    0C000H-0C3FFH RAM BIOS work

BASIC LEVEL II B circuit diagram (ROM32KB RAM1KB + 2KB)



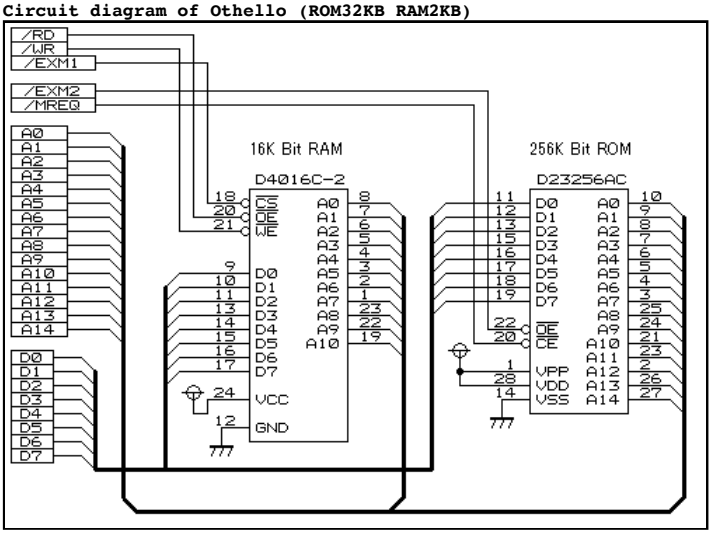
/ EXM2 = 1 is an access after 08000H
/ Y1 and / Y2 of LS138 are / RD, / WR, A14 = 0
SRAM 2KB is 08000H-087FFH / RD, / WR

/ Y5 and / Y6 of LS138 are / RD, / WR, A14 = 1, A10 = 0
SRAM 1KB is 0C000H-0C3FFH / RD, / WR

The RAM of the main body is a mirror and is used as 0C400H-0C7FFH.
At least in software, 08000H-087FFH, 0C000H and 0C7FFH
Test memory is done.

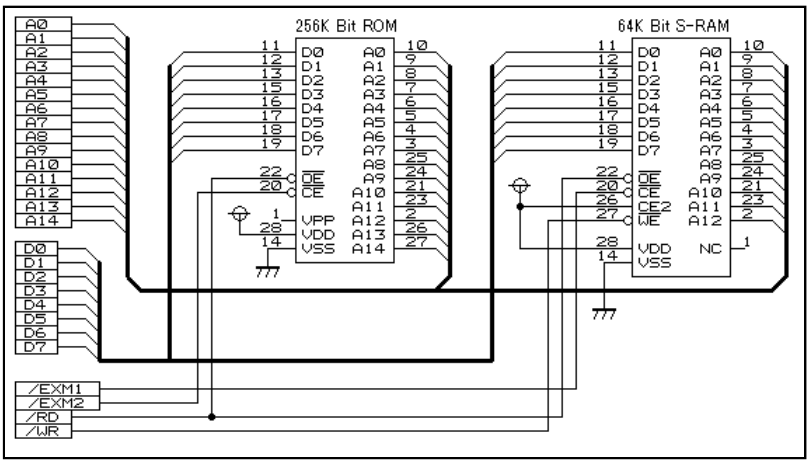
/ DSNRA is N.I. It seems that IC2 is not used in C's FG-2000.

Circuit diagram of Othello (ROM32KB RAM2KB)



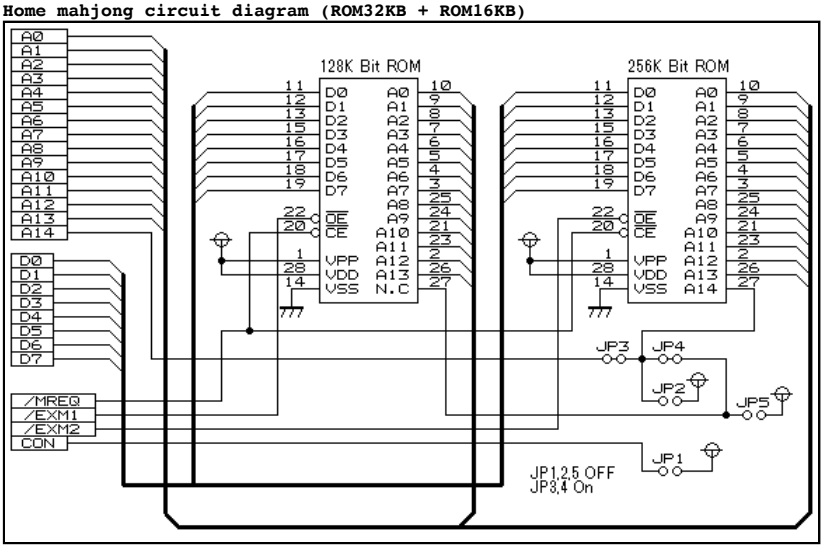
The 2K byte RAM of the cartridge is used as a work area (08000H-087FFH).
BOARD 171-5044
ROM D23256AC 040 8529K7
RAM D4016C-2

Circuit diagram of The Castle (ROM32KB RAM8KB)



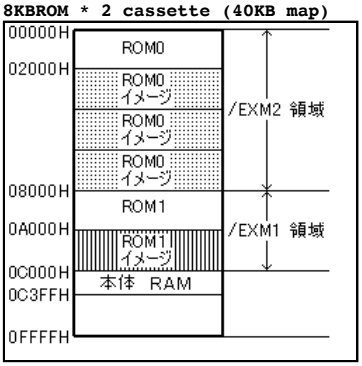
The 8K byte RAM of the cartridge is used as a work area (08000H-09FFFH).

Home mahjong circuit diagram (ROM32KB + ROM16KB)



The total ROM capacity is 48KB (00000H-0BFFFH).
The jumper is designed so that 3 and 4 are short and connected to A14 (the 128KBit of JP4 is meaningless).

8KBROM * 2 cassette (40KB map)



There is one that uses two UVEP-ROM2764.
/ One in the area of EXM2 (00000H-07FFFH)
/ One in the area of EXM1 (08000H-0BFFFH)
There is no address decoder and only two ROMs are installed.
Therefore, the content of 000000H-01FFFH is 02000H-07FFFH as a mirror image.
The content of 08000H-09FFFFH is 0A000H-0BFFFH as a mirror image.

In order to use this type of software with the emulator, it may be better to include the image part as well.
At a minimum, the image part of ROM0 must be filled with some data.
This is because the data in ROM1 is not placed in 08000H.

Older versions of Congo Bongo, Chanon Baseball, Challenge Derby
The Monaco Grand Prix is a type with ROM0 of 16KB + ROM1 of 8KB
Sega pachinko is a type with ROM0 of 8KB + ROM1 of 2KB

D23256AC 040 8529K7 + D4016C-2 171-5044 Othello 256KBit + 16KBit RAM af4f14bc
TMM23256P 8126 SL21 171-5044 SC-3000 BASIC Level IIA
TMM23256P 8126 SL21 + TMM2009P-B + TMM2016AP-12 171-5143 (There is also a note of 171-5145 for some reason) For BASIC Level IIB SK-1100
TMM23256P-8160 8444AAA 171-5177 256KBit Champion Boxing

MPR-5546 171-5177 Sinbad Mystery 256KBit
MPR-5977 171-5177 Safari Race 256KBit
MPR-6100 171-5177 256KBit Champion Boxing
MPR-6102 + MPR6103 171-5180 Home Mahjong 256KBit + 128KBit
MPR-6145 171-5147 Flicky 256KBit
MPR-6381 171-5177 Champion Baseball
MPR-6485 171-5177 GP WORLD Ver B 256KBit 942adf84
MPR-6487 171-5177 Konami's Hyper Sports 256KBit

MPR-10159 171-5382 The Castle 256KBit + 64KBit RAM
MPR-10517 171-5363-01 Portrait of Loretta 1MBit 323f357f

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