Unmanned Solar Powered Airship Concept Evaluation

Critical Design Report

Electrical Power System

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Normative References

Table 1 – *Normative References for this document*

Document title	**Doc. Ref. No.**	**Doc. status**
Preliminary Design Report - Electrical Power System	USPACE-PDR-EPS-A1	Review
Preliminary Design Report	USPACE-PDR-A1	Review

Acronyms

APR Array Power Regulator

BCR Battery Charge Regulator

BJT Bipolar Junction Transistor

CDR Critical Design Review

COTS Commercial Of-The-Shelf

DM Development Model

ECSS European Cooperation for Space Standardization

EMI Electromagnetic Interference

EPS Electrical Power System

FM Flight Model

GaAs Gallium Arsenide

IC Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

LiPo Lithium-Polymer

MEA Main Error Amplifier

MPP Maximum Power Point

MPPT Maximum Power Point Tracking

MPPTU Maximum Power Point Tracking Unit

NTC Negative Temperature Coefficient

OpAmp Operational Amplifier

PCB Printed Circuit Board

PDR Preliminary Design Review

PSA Pressure Sensitive Adhesive

PWM Pulse Width Modulated

SAR Solar Array Regulator

SA Solar Array

TBD To Be Decided

TV Thermal Vacuum

UAV Unmanned Aerial Vehicle

UVP Under Voltage Protection

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1 Introduction

The Electrical Power System (EPS) provides power to motors, the on-board computer, communication system and payloads. Power is mainly supplied from solar cells but can also be supplied from a battery, when solar power is not available or insufficient.

1.1 Changes from PDR to CDR

Table 2 lists major design changes from the EPS Preliminary Design Review (PDR) report.

Table 2 – *U-SPACE EPS design changes from PDR to CDR*

Area of change	**Changed parameter**	**Argumentation for change**
Total power budget	increased to $> 40\,W$	Airship total mass and size are increased thus requiring much more power for the motors
Solar cells	New part	Old solar cell was much heavier than listed in manufacturer datasheet due to a glass cover
Total system cost	increased to $> 12000\,SEK$	Increased power and new light-weight solar cells are more expensive
Solar cell mounting	New part	New solar cell is flexible instead of rigid and can be mounted with Pressure Sensitive Adhesive (PSA)

2 Functional and Technical Requirements

This section describes the functional and technical EPS requirements along with the expected EPS performance.

2.1 Functional Requirements

Below are listed the primary functional EPS requirements:

- Provide adequate power to motors, other subsystems and payloads
- Proof that flying on solar energy is possible i.e more power produced than consumed

Additional desired requirements are:

- Scalable and flexible system architecture allowing the EPS to be upgraded to higher power levels or re-used in different applications (rover, Unmanned Aerial Vehicle (UAV) etc.)
- Robust design allowing flight in more extreme conditions (altitude, weather etc.)
- Provide adequate protection circuits for battery and loads to prevent any major failure and damage to other subsystem components.
- Optimal design and high performance to increase power capability and minimize system mass

2.2 Technical Requirements

The EPS technical requirements are listed in table 3.

Table 3 – *Technical requirements for the EPS*

Description	Symbol	Value
Minimum power output	$P_{Out,min}$	$40\,W$
Maximum mass	W_{EPS}	$1000\,g$ including solar arrays
Maximum cost	-	$4000\,SEK$[a]
Output voltages	$V_{Mainbus}$, V_{5V}	$6.0-9.2\,V$ un-regulated and $5\,V$ regulated
Maximum output current (worst case)	$I_{Out,max}$	$10.8\,A$
Regulator phase margin	-	$60\,deg$
Regulator gain margin	-	$10\,dB$
Control loop bandwidth	-	$> 10\,kHz$
Operational temperature	T_{max}, T_{min}	$-20°C\,to + 25°C$
Battery capacity	C_{Bat}	$> 5\,Wh$

[a]Initial budget for 2 students.

2.3 Mission and Environmental Constraints

This section discusses the system challenges imposed by the operation environment.

Solar Array Temperature

As was discussed in [1], the optimal operating voltage of the solar cells change with temperature. The EPS must be able to generate optimal power from the solar cells in the full expected temperature range of the environment.

Solar Incidence Angle

The launch site of U-SPACE is near Kiruna at 67.5° northern latitude. In summer solstice, at midday, the solar incidence angle, from local horizontal, is $alpha_{sun} = 46\,\text{deg}$[1, eq. 1]. The solar cell output current drops with the Kelly cosine function as shown in figure 1. To minimize power losses due to inclined solar incidence, **MSE!** (**MSE!**) design must consider the optimal mounting position and angle of the solar panels.

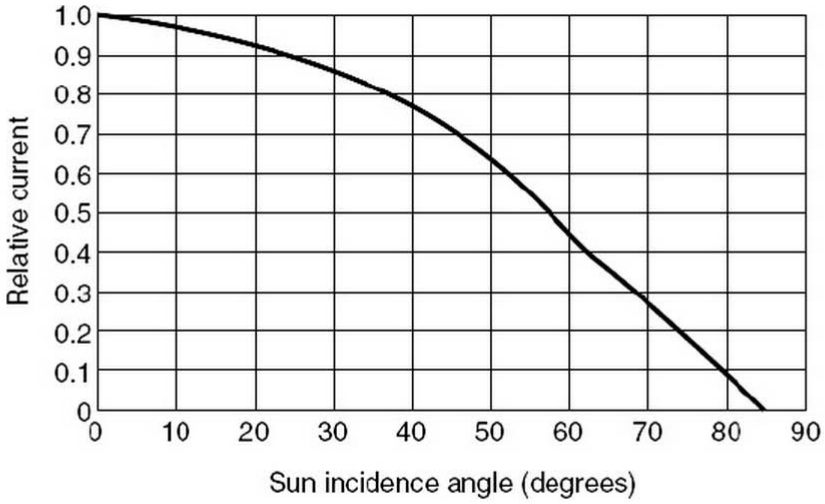

Figure 1.22 Kelly cosine curve for PV cell at sun angles form 0 to 90°.(Ref:3)

Figure 1 – *Kelly cosine function showing how solar cell photo current depends on sun incidence angle*

Solar Array Shading

Shading on the solar panels, for example caused by airship stabilizer structures or objects in the landscape, can cause a significant drop in the cell output voltage, as described in [**Mukund**]. Bypass diodes can be used to partly mitigate this issue. However, since the airship is only expected to fly at altitudes above terrain and buildings the only shading possibly expected is from the airship structure hence the **MSE!** design must consider this restriction.

Battery Temperature

One of the most sensitive and temperature critical EPS components is the battery. It is important that it stays within its safety temperature limits. In the proposed design, only temperature monitoring is supplied. Therefore, flight may only be allowed when outdoors temperature is well within the allowed battery temperature range. Otherwise a battery heater and more sophisticated thermal design may be necessary.

2.4 Expected Performance

The expected EPS performance values are listed in Table 4.

Table 4 – *Expected performance of the EPS*

Power conversion efficiency(overall)	$80 - 90\%$
Power output(overall)	$\sim 57 - 65\,W$
Battery capacity	$7.3\,Wh$
Mass	$\sim 910\,g$
Total cost	$\sim 12000\,SEK$[a]

[a]Solar cells are significantly more expensive than anticipated. A request for more funds is under preparation.

3 Critical Design

The overall EPS diagram is shown in Figure 2. An Array Power Regulator (APR) controls the operating voltage of the solar panel and supplies an unregulated mainbus. The mainbus voltage is mainly controlled by the battery voltage. A DC-DC regulator provides a regulated $5\,V$ supply to subsystems and payloads.

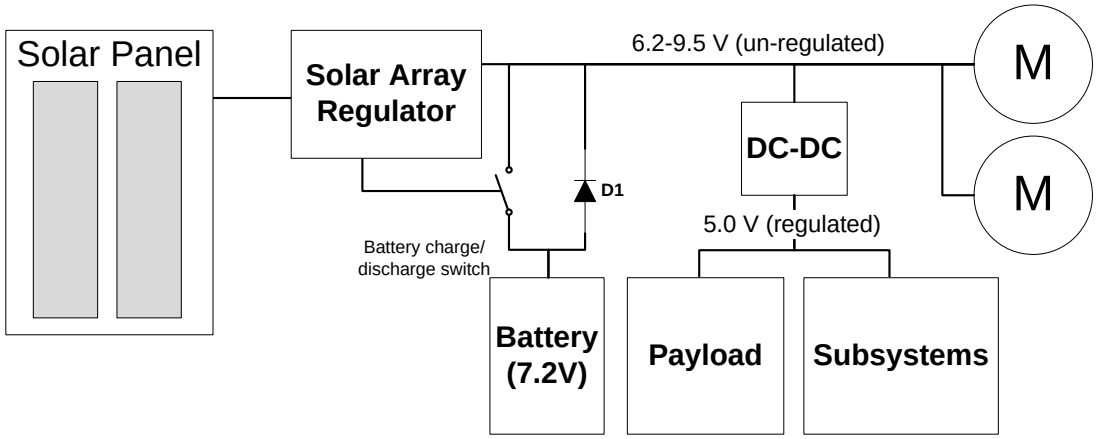

Figure 2 – *EPS simple blockdiagram*

3.1 Solar Array Design

The *PowerFilm RC7.2-75(PSA)* solar cell is selected shown to the left in Figure 3. Table 5 lists the important specifications for this cell.

Table 5 – *Specifications of chosen solar cell*

Description	**Symbol**	**Value**
Nominal output current	I_{cell}	$100\,mA$
Nominal output voltage	V_{cell}	$7.2V$
Nominal output power	P_{cell}	$0.72\,W$
Dimensions	-	$270\,mm \times 90\,mm \times 0.2\,mm$
Weight	W_{cell}	$7.6\,g$
No. of required cells	N_{cells}	100^a
Total solar panel area	P_{panel}	$2.43\,m^2$ (assuming 100 % fill factor)

[a] [2] offers good discount for +100 units order

The solar panel is an array of 50 parallel connected strings of two series solar cells as shown to the right in Figure 3. The nominal output voltage and current are thus:

$$V_{panel} = 2V_{cell} = 14.4\,V$$
$$I_{panel} = 50I_{cell} = 5\,A \tag{1}$$

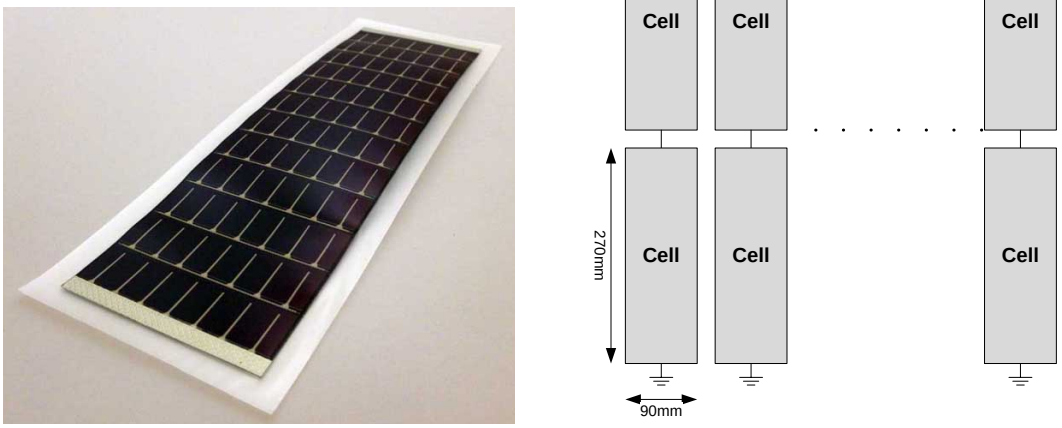

Figure 3 – *PowerFilm solar cell(left), Solar array configuration(right)*

Since only two cell are in series, it is estimated that bypass diodes are not very beneficial for mitigating shading issues, as was discussed in Section 2.3, and hence are not included in the design.

3.2 Array Power Regulator

The APR must control the optimal the solar panel operating voltage by applying a Maximum Power Point Tracking (MPPT) as well as limit the output mainbus voltage. A simple step-down buck converter topology is preferred for a number of reasons:

- simple circuit analysis and low components count
- no inherent **RHPZ!** (**RHPZ!**) in contrary to the standard boost topology
- step-down topology calls for a high input voltage which leads to low input current thus minimizing ohmic losses and the forward voltage drop loss from the reverse protection diode also becomes relatively smaller

3.2.1 Buck Converter

The ideal transfer function for the buck converter shown in Figure 4 is given as

$$V_{out} = D\,V_{in} \tag{2}$$

where D is the duty cycle of the MOSFET. It is seen that the converter is able to control the output voltage by varying the duty cycle. The duty cycle is set by a Pulse Width Modulated (PWM) controller which provides input to a high-side MOSFET driver. A Main Error Amplifier (MEA) measures the mainbus output voltage to generate a control signal for the PWM controller, thus limiting the output voltage. An LM3477 chip is selected which combines PWM controller, MEA and gate driver in one single Integrated Circuit (IC).
The **CM!** (**CM!**) control scheme is adopted due to its excellent dynamic abilities[REF] simplifying the feedback regulator design. A low impedance $10\,m\Omega$ precision sense resistor measures the inductor current slope. To avoid current mode instabilities[REF], which can occur with **CM!** control, the LM3477 adds $103\,mV$ slope compensation[REF] to the current sense signal.

The converter switching frequency, f_{switch}, is chosen relatively high to $500\,kHz$. The increased switching losses are out-weighted by the fact that the low input voltage limits these losses and high frequency allows the inductor and filter components to be made smaller thus limiting the resistive losses which are expected to dominate converter losses due to the relatively high currents.

The inductor current ripple, ΔI_L, is given by

$$\Delta I_L = \frac{V_{in} - V_{out}}{L\,f_{switch}} D \tag{3}$$

where L is the inductance and f_{switch} the converter switching frequency. The inductor current ripple is usually limited to about $10\,\%$ of the maximum output current which was given in Table 3 as $10.8\,A$. Thus the minimum required inductance is calculated to

$$L = \frac{V_{in} - V_{out}}{\Delta I_L\,f_{switch}} D = \frac{14.4\,V - 7.4\,V}{1.08\,A 500\,kHz} \cdot 0.514 = 6.7\,uH \tag{4}$$

A $10\,uH$ inductor is chosen giving a current ripple of $0.72\,A$, the converter will enter **DCM!** (**DCM!**) at light loads when the load current drops below $0.36\,A$ which is unlikely to happen in most operating modes.

For the converter output capacitor, a component is chosen which has very low **ESR!** (**ESR!**) and high capacitance to limit the output voltage ripples.

Current Sense Amplifier

With an inductor current ripple of $0.72\,A$ the current sense voltage slope is only

$$v_{sense} = \Delta I_L \cdot R_{sense} = 0.72\,A \cdot 10\,m\Omega = 7.2\,mV \tag{5}$$

It is recommended that the slope compensation is equal to or the double of the sense slope[REF], however the minimum compensation slope is limited to $103, mV$ by the LM3477 chip. Thus the sensed slope signal must be amplified with a gain of around 20 being suitable. This also has the advantage of eliminating some of the typical noise susceptibility in the current sense signal. The current sense circuit in Figure 4 consists of two differential OpAmps which amplifies the current sense slope. Resistive voltage dividers are placed on the OpAmp inputs to scale down the input voltage signals to always be below the $5\,V$ OpAmp supply voltage.

3.2.2 Maximum Power Point Tracker

In [1] it was decided to use a Maximum Power Point Tracking Unit (MPPTU) with the APR to increase solar panel efficiency during changing environment conditions.

The APR with MPPT can operate in three different operation regions:

- Battery discharge - when the solar panel input power is insufficient to cover the load power demand, the battery is slowly discharged in order to maintain the output voltage. The MPPTU controls the input voltage.
- Battery charge - when the solar array input is greater than the load power, excessive power is used to recharge the battery. The MPPTU controls the input voltage.
- Input power limitation - when the battery is fully charged, the regulator will operate the solar array at a non-optimal voltage, thus limiting the input power to keep the output voltage at a maximum limit. The extra potential input power is dissipated as heat externally on the solar arrays.

It is preferred to implement an analog MPPTU mainly since this makes the circuit independent on a control signal from a more complicated external **MCU!** (**MCU!**) or **DSP!** (**DSP!**) thus allowing a flexible plug'n-play system to be implemented.

The MPPT has not been completely designed yet.

3.3 Battery Design

An Ansmann Lithium-Polymer (LiPo) Racing Pack 2S1P 30C battery is selected. The battery specifications are listed in Table 6

Table 6 – *Specification of chosen battery*

Description	Symbol	Value
Chemistry	-	Li-Polymer
Nominal voltage	V_{bat}	$7.4\,V$
Capacity	C_{bat}	$2.1\,Ah$ / $15.54\,Wh$
Weight	W_{bat}	$122\,g$
Dimensions	-	$105\,mm \times 35.2\,mm \times 17\,mm$
Maximum fast charge current	$I_{charge,max}$	$3\,A$
Maximum discharge current (continuous)	$I_{discharge,max}$	$63\,A$

3.3.1 Battery Charge Regulator

From the battery datasheet, maximum charge current is $I_{REG} = 3\,A$. From the Battery Charge Regulator (BCR) datasheet, the minimum current sense resistor value is calculated as

$$\begin{aligned} R_{sense} &= \frac{V_{FCS}}{I_{REG}} \\ R_{sense} &= \frac{120\,mV}{3\,mA} = 40\,m\Omega \end{aligned} \tag{6}$$

A $50\,m\Omega$ current sense resistor is selected leading to a charge current of $2.4\,A$. The required thermal rating of the pass transistor is calculated as

$$P_{max} = (V_{in,max} - V_{bat,min}) \cdot I_{charge} = (9.5\,V - 5.5\,V) \cdot 2.4\,A = 9.6\,W \tag{7}$$

A TPCA8102 P-channel MOSFET is selected as charge transistor. It has a peak power dissipation rating of $42\,W$ and $1.6\,W$ continuous ($10\,s$) and $R_{DS(ON)} = 4.5\,m\Omega$. At $2.4\,A$ charge current, the heat dissipation is well below the maximum allowed value.

Voltage Feedback Divider

To charge the battery, the main bus output voltage must be above the **UVLO!** (**UVLO!**) maximum start threshold at $8.9\,V$. $9.5\,V$ is selected, to allow some margin. The PWM controller voltage feedback input must be $1.270\,V$ thus determining the feedback voltage divider resistor values to $R_{FB1} = 12.9\,k\Omega$ and $R_{FB2} = 2\,k\Omega$.

3.4 Complete EPS Diagram

The complete EPS diagram is shown in Figure 4. For providing the $5\,V$ regulated voltage to the payloads, Commercial Of-The-Shelf (COTS) DC-DC regulator(s) are used. The battery charging/discharging is controlled by the Solar Array Regulator (SAR).

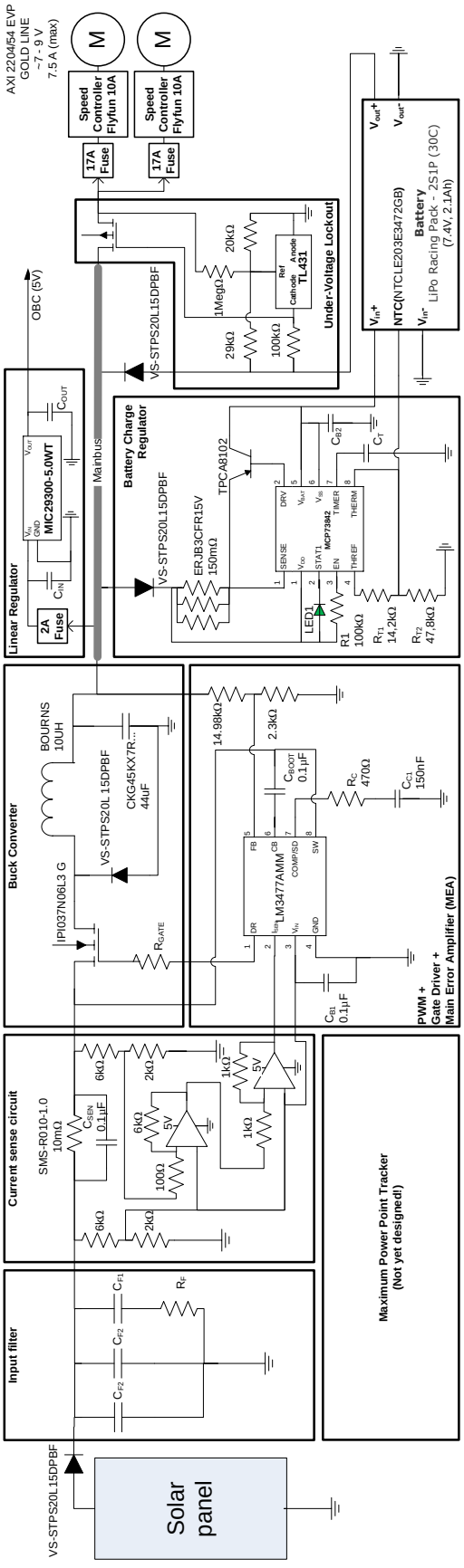

Figure 4 – *EPS detailed block diagram diagram*

3.5 External Interfaces

The interfaces of the EPS external are listed in table 7.

Table 7 – *External interfaces*

External interface	**Implementation**
Solar cells mounting	PSA
DC-DC regulators	Mounted on PCB which sits in system housing. Thermal contact points should be included, to remove internal heat dissipation.
Battery telemetry	Analog signals to Microcontroller
Mounting of batteries	To Be Decided (TBD)
Supply voltages	$6.0 - 9.2\,V$ (unregulated) and $5.0\,V$(regulated)

3.6 Telemetry and Telecommands

The required/recommended telemetry and telecommands, EPS , are listed in table 8.

Table 8 – *Telemetry and telecommands*

Telemetry	**Data rate/frequency**	**Data size**
Battery voltage	Every 30 sec	2 bytes
Battery temperature	Every 5 sec	2 bytes

4 Test and Verification of Design

4.1 Preliminary Verification of Design

TBD...

4.2 Design Models and Verification Methods

PSpice Simulations

PSpice transient and average simulation models of the SAR will be created. These will help in the design and testing of the regulator performance and system stability during transient loading.

Development Model

A Development Model (DM) will be build using self-made "mini-mount" pads and mainly surface-mount components, to minimize parasitic effects. System stability will be tested using a Network Analyzer and MPPT performance will be tested in a Thermal Vacuum (TV) chamber cycling the solar array temperature.

Flight Model

If time allows, a dedicated Flight Model (FM) will be build, using a custom designed Printed Circuit Board (PCB) schematic layout. An optimized PCB layout will minimize the system mass and size while maximizing the efficiency and system robustness.

5 Resources and Scheduling

5.1 Main Tasks

TBD...

5.2 Parts List and Costs

TBD...

5.3 Electronics Ground Support Equipment (EGSE)

TBD...

References

[1] M. Olsen, D. Agten, and Z. Hao. *Preliminary Design Report - Electrical Power System*. Tech. rep. USPACE-PDR-EPS-A1. Luleå University of Technology, 2012.

[2] Avnet Express. *RC7.2-75 PSA*. http://avnetexpress.avnet.com. 2012.