Unmanned Solar Powered Airship Concept Evaluation

Critical Design Report

Electrical Power System

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Normative References

Table 1 – *Normative References for this document*

Document title	**Doc. Ref. No.**	**Doc. status**
Preliminary Design Report - Electrical Power System	USPACE-PDR-EPS-A1	Review
Preliminary Design Report	USPACE-PDR-A1	Review

Acronyms

BCR Battery Charge Regulator

BJT Bipolar Junction Transistor

CC Constant Current

CDR Critical Design Review

CM Current Mode

DCM Discontinuous Conduction Mode

DM Development Model

DSP Digital Signal Processor

ECSS European Cooperation for Space Standardization

EGSE Electronic Ground Support Equipment

EMC Electromagnetic Compatibility

EMI Electromagnetic Interference

EPS Electrical Power System

ESR Equivalent Series Resistor

FM Flight Model

IC Integrated Circuit

LDO Low-dropout

LiPo Lithium-Polymer

MCU Micro-Controller Unit

MEA Main Error Amplifier

MGSE Mechanical Ground Support Equipment

MPPT Maximum Power Point Tracking

MPPTU Maximum Power Point Tracking Unit

MSE Mechanical Structure and Envelope

NTC Negative Temperature Coefficient

OpAmp Operational Amplifier

PCB Printed Circuit Board

PDR Preliminary Design Review

PSA Pressure Sensitive Adhesive

PTC Positive Temperature Coefficient

PWM Pulse Width Modulation

RHPZ Right Half Plane Zero

SAR Solar Array Regulator

SMD Surface-Mount Device

SPA Solar Powered Airship

TBD To Be Decided

UAV Unmanned Aerial Vehicle

UVLO Under-Voltage Lock-Out

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1 Introduction

The Electrical Power System (EPS) provides power to motors, the on-board computer, communication system and payloads. Power is mainly supplied from solar cells but can also be supplied from a battery, when solar power is not available or insufficient.

1.1 Changes from PDR to CDR

Table 2 lists major design changes from the EPS Preliminary Design Review (PDR) report.

Table 2 – *U-SPACE EPS design changes from PDR to CDR*

Area of change	**Changed parameter**	**Argumentation for change**
Total power budget	Increased to $> 40\,W$	Airship total mass and size are increased thus requiring much more power for the motors
Solar cells	New part	Old solar cell was much heavier than listed in manufacturer datasheet due to a glass cover
Total system cost	Increased to $> 12000\,SEK$	Increased power and new light-weight solar cells are more expensive
Solar cell mounting	New part	New solar cell is flexible instead of rigid and can be mounted with Pressure Sensitive Adhesive (PSA)
Battery	New part	A battery that supports much higher discharge currents has been selected which simplifies current limiting circuitry and improves battery efficiency

2 Functional and Technical Requirements

This section describes the functional and technical EPS requirements along with the expected EPS performance.

2.1 Functional Requirements

The primary functional EPS requirements are:

- Provide adequate power to motors, other subsystems and payloads
- Proof that flying on solar energy is possible i.e more power produced than consumed

Additional desired requirements are:

- Scalable and flexible system architecture allowing the EPS to be upgraded to higher power levels or re-used in different applications (rover, Unmanned Aerial Vehicle (UAV) etc.)
- Robust design allowing flight in more extreme conditions (altitude, weather etc.)
- Provide adequate protection circuits for battery and loads to prevent any major failure and damage to other subsystem components.
- Optimal design and high performance to increase power capability and minimize system mass

2.2 Technical Requirements

The EPS technical requirements are listed in table 3.

Table 3 – *Technical requirements for the EPS*

Description	**Symbol**	**Value**
Minimum power output	$P_{out,min}$	$40\,W$
Maximum mass	$W_{EPS,max}$	$1000\,g$ including solar arrays
Maximum cost	-	$4000\,SEK$[a]
Output voltages	$V_{mainbus}$, V_{5V}	$6.0-9.5\,V$ un-regulated and $5\,V$ regulated
Maximum output current (worst case)	$I_{out,max}$	$10.8\,A$
Operational temperature	T_{min}, T_{max}	$-20°C\,to + 25°C$
Battery capacity	C_{bat}	$> 5\,Wh$

[a]Initial budget for 2 students

2.3 Mission and Environmental Constraints

This section discusses the system challenges imposed by the operation environment.

Solar Array Temperature

As was discussed in [1], the optimal operating voltage of the solar cells change with temperature. The EPS must be able to generate optimal power from the solar cells in the full expected temperature range of the environment. This can be achieved using a Maximum Power Point Tracking Unit (MPPTU) which will be discussed in Section 3.3.2

Solar Incidence Angle

The flight location of U-SPACE is near Kiruna at 67.5° northern latitude. In summer solstice, at midday, the solar incidence angle from local horizontal is $\alpha_{sun} = 46°$[1, eq. 1]. The solar cell output current drops with the Kelly cosine function as shown in figure 1. To minimize power losses due to inclined solar incidence, Mechanical Structure and Envelope (MSE) design must consider the optimal mounting position and angle of the solar panels.

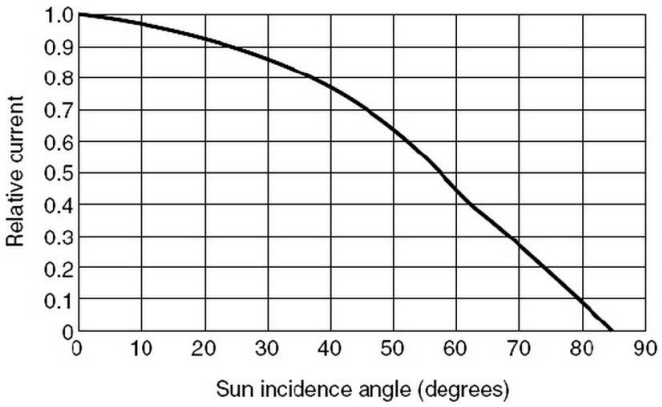


Figure 1.22 Kelly cosine curve for PV cell at sun angles form 0 to 90°.(Ref:3)

Figure 1 – *Kelly cosine function showing how solar cell photo current depends on sun incidence angle*

Solar Array Shading

Shading on the solar panels, for example caused by airship stabilizer structures or objects in the landscape, can cause a significant drop in the cell output voltage, as described in [2, p. 165]. Bypass diodes can be used to partly mitigate this issue. However, since the airship is only expected to fly at altitudes above terrain and buildings the only shading possibly expected is from the airship structure hence the MSE design must consider this restriction.

Battery Temperature

One of the most temperature critical EPS components is the battery which must stay within its safety temperature limits. In the proposed design, only temperature monitoring is offered therefore, flight is only allowed when outdoors temperatures are well within the allowed battery temperature range. Otherwise a battery heater and more sophisticated thermal design may be necessary.

2.4 Expected Performance

The expected EPS performance values are listed in Table 4.

Table 4 – *Expected performance of the EPS*

Description	**Symbol**	**Value**
Power conversion efficiency(overall)	-	$80 - 90\%$
Power output(overall)	P_{out}	$\sim 57 - 65\,W$
Battery capacity	C_{bat}	$7.3\,Wh$
Mass	W_{EPS}	$\sim 910\,g$
Total cost	-	$\sim 12000\,SEK$[a]

[a]Solar cells are significantly more expensive than anticipated. A request for more funds is under preparation.

3 Critical Design

The basic EPS diagram is shown in Figure 2. A Solar Array Regulator (SAR) controls the operating voltage of the solar array and supplies an unregulated mainbus. The mainbus voltage is mainly controlled by the battery voltage. A DC-DC regulator provides a regulated $5\,V$ supply to subsystems and payloads. Motors are supplied from the unregulated mainbus.

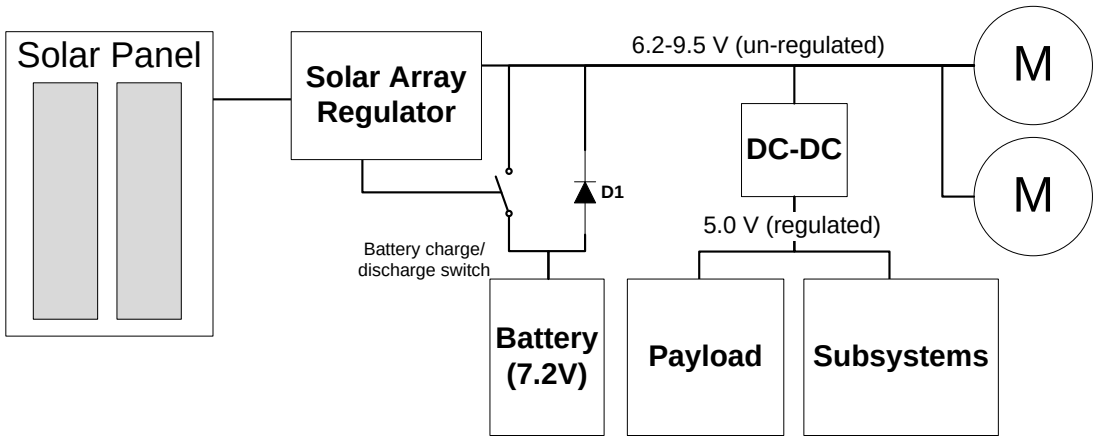


Figure 2 – *EPS simple blockdiagram*

3.1 Battery Design

In [1] it was decided that a Li-ion type battery was suitable for the EPS. An *Ansmann Lithium-Polymer (LiPo) Racing Pack 2S1P 30C* battery is selected with the specifications as listed in Table 5.

Table 5 – *Specification of chosen battery*

Description	**Symbol**	**Value**
Chemistry	-	Li-Polymer
Nominal voltage	V_{bat}	$7.4\,V$
Capacity	C_{bat}	$2.1\,Ah$ / $15.54\,Wh$
Weight	W_{bat}	$122\,g$
Dimensions	-	$105\,mm \times 35.2\,mm \times 17\,mm$
Maximum fast charge current	$I_{charge,max}$	$3\,A$
Maximum discharge current (continuous)	$I_{discharge,max}$	$63\,A$

3.1.1 Battery Charge Regulator

The Battery Charge Regulator (BCR) must control the charge rate of the battery such that the charge current limit is not exceeded and cut off the charge current when the battery is fully charged. Temperature monitoring is usually also required to inhibit charging if the battery temperature is outside its safety limits.

An *MCP73842* Li-ion battery charge regulator Integrated Circuit (IC) is selected. It employs three different charge modes: low-charge for deeply discharged batteries, Constant Current (CC) charge and trickle charging as well as inputs for temperature monitoring. The battery maximum charge current was in Table 5 given as $3\,A$. From the *MCP73842* datasheet, the minimum current sense resistor value is calculated as

$$\begin{aligned} R_{sense} &= \frac{V_{FCS}}{I_{REG}} \\ R_{sense} &= \frac{120\,mV}{3\,A} = 40\,m\Omega \end{aligned} \tag{1}$$

A $50\,m\Omega$ current sense resistor is selected leading to a charge current of $2.4\,A$. The worst-case thermal dissipation in the MOSFET happens when the battery is charged from its minimum charge state

$$P_{max,MOSFET} = (V_{in,max} - V_F - V_{bat,min}) \cdot I_{charge} = (9.5\,V - 0.3\,V - 5.5\,V) \cdot 2.4\,A = 8.88\,W \tag{2}$$

where $V_{in,max}$ is the maximum mainbus voltage, V_F the expected Schottky diode forward voltage drop and $V_{bat,min}$ is the preconditioning threshold voltage of the BCR IC. An *SUP75P03-07-E3* P-channel MOSFET is selected which is rated for a peak power dissipation of $187\,W$, well above the minimum requirement provided that suitable thermal design is applied, most likely also including a heat sink.

Calculations on heat sink requirements still remain to be done.

Future Improvements

As was calculated above, significant power may be lost in the BCR MOSFET. This is due to the selected BCR IC which requires an input voltage of around $9.5\,V$ (including a Schottky diode forward voltage drop and some design margin). In future, the BCR could be designed to allow operation with an input voltage only slightly above the battery voltage thus minimizing the charge losses and the thermal requirements of the MOSFET.

3.1.2 Battery Temperature Monitoring

The selected LiPo battery is rated, in charge-mode, for the temperature interval 0 to $+45°C$. For temperature measuring, a $4.7\,k\Omega$ *NTCLE203E3472GB0* thermistor is selected which has a Beta Value, $B = 3977\,K$. Since the battery temperature is measured using

an external thermistor, thus the temperature response is likely to be somewhat slower, an extra $5°C$ thermal design margin is added. The required resistance values of the BCR temperature control resistors are determined from the *MCP73842* datasheet as

$$\begin{aligned} R_{cold} &= R_{25}\, e^{B(\frac{1}{T}-\frac{1}{T_0})} = 4.7\,k\Omega\, e^{3977\,K(\frac{1}{278\,K}-\frac{1}{298\,K})} = 12.28\,k\Omega \\ R_{hot} &= 4.7\,k\Omega\, e^{3977\,K(\frac{1}{313\,K}-\frac{1}{298\,K})} = 2.48\,k\Omega \\ R_{T1} &= 2\frac{R_{cold}R_{hot}}{R_{cold}-R_{hot}} = 6.2\,k\Omega \\ R_{T2} &= 2\frac{R_{cold}R_{hot}}{R_{cold}-3R_{hot}} = 12.6\,k\Omega \end{aligned} \tag{3}$$

where R_{25}, R_{cold} and R_{hot} are the thermistor resistance values at room temperature, the low and high temperature limits respectively. R_{T1} and R_{T2} are the required BCR temperature control resistors setting the required temperature interval.

If the sensed battery temperature falls outside the $+5$ to $+40°\,C$ region, battery charging will be inhibited. The technical requirements from Table 3 requires the EPS to operate down to $-20°\,C$. Hence some insulation and/or heating of the battery may be necessary or flight must be disallowed at outdoors temperatures much below $+5°\,C$.

3.1.3 Battery Under-Voltage Lock-Out

To prevent over-discharge of the battery, a battery Under-Voltage Lock-Out (UVLO) circuit is added as shown in Figure 5. An *TL431* precision shunt regulator IC is selected. The lock-out voltage is given as

$$V_{UVLO} = V_{ref}(1+\frac{R_1}{R_2}) = 2.5\,V(1+\frac{29\,k\Omega}{20\,k\Omega}) = 6.125\,V \tag{4}$$

where V_{ref} is the *TL431* build-in voltage reference. If the battery voltage drops below this value, the gate voltage to the P-type MOSFET is pulled high thus opening the switch. The $1\,M\Omega$ resistor adds about $200\,mV$ hysteresis.

The UVLO circuit only cuts out the motor power line. Thus payloads remain supplied and the battery is still slowly drained. This design has been chosen to allow telemetry and telecommand capability during a heavy battery discharge event. In this case, it is expected that all payloads and on-board computers enter a low power consumption mode, to extend the remaining battery supply time. If the battery voltage drops below $5.62\,V$, the $5\,V$ payload power supply shuts down and all telemetry and telecommand capabilities will be lost.

3.2 Solar Array Design

The main driver for selecting the solar cell is to choose a part which is very light-weight and easy to mount on the Solar Powered Airship (SPA). A *PowerFilm RC7.2-75(PSA)*

solar cell is selected as shown in Figure 3. This is a very light-weight flexible solar cell with a PSA backside for mounting. Table 6 lists the solar cell specifications.

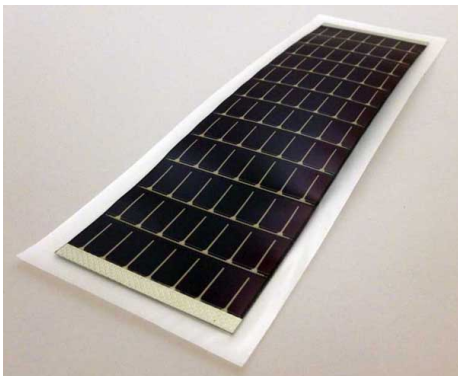
Table 6 – *Specifications of chosen solar cell*

Description	**Symbol**	**Value**
Nominal output current	I_{cell}	$100\,mA$
Nominal output voltage	V_{cell}	$7.2V$
Nominal output power	P_{cell}	$0.72\,W$
Dimensions	-	$270\,mm \times 90\,mm \times 0.2\,mm$
Weight	W_{cell}	$7.6\,g$
No. of required cells	N_{cells}	100^a
Total solar array area	A_{array}	$2.43\,m^2$ (assuming 100 % fill factor)

[a] [3] offers good discount for +100 units order

The solar array is an array of 50 parallel connected strings of two series solar cells as shown in Figure 3. The nominal output voltage and current are given as

$$\begin{aligned} V_{array} &= 2 \cdot V_{cell} = 14.4\,V \\ I_{array} &= 50 \cdot I_{cell} = 5\,A \end{aligned} \tag{5}$$



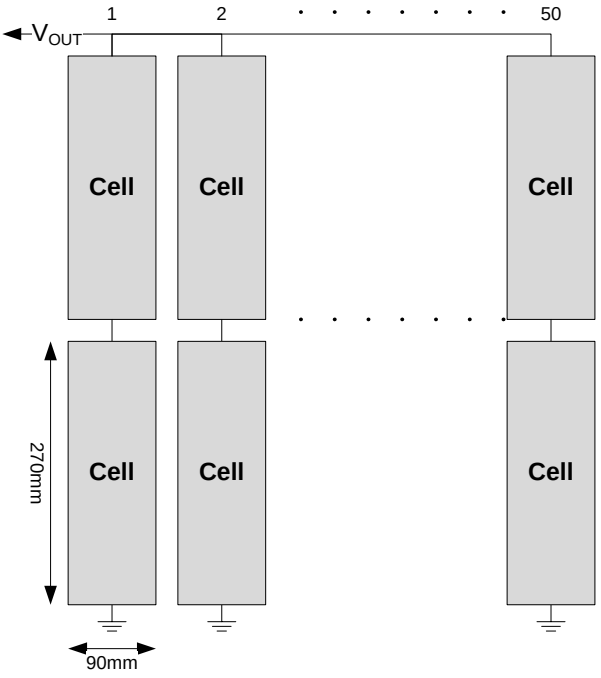


Figure 3 – *PowerFilm solar cell(left), solar array configuration(right)*

Since only two cells are in series, it is estimated that bypass diodes are not very beneficial for mitigating shading issues, as was discussed in Section 2.3, and hence are not

included in the design.

3.3 Solar Array Regulator

The SAR must control the optimal the solar array operating voltage as well as limit the output mainbus voltage. A simple step-down buck converter topology is preferred for a number of reasons:

- simple circuit analysis and low components count
- no inherent Right Half Plane Zero (RHPZ) in contrary to the standard boost topology
- step-down topology calls for a high input voltage which leads to low input current thus minimizing ohmic losses and the relative forward voltage drop loss from the reverse protection diode

3.3.1 Buck Converter Circuit Design

The ideal transfer function for the buck converter shown in Figure 5 is given as

$$V_{out} = D\,V_{in} \tag{6}$$

where D is the duty cycle of the MOSFET switch, V_{in} the solar array voltage and V_{out} the mainbus voltage. The duty cycle is controlled by a Pulse Width Modulation (PWM) controller which provides input to a high-side MOSFET driver. A Main Error Amplifier (MEA) measures the mainbus output voltage to generate a control signal for the PWM controller. An *LM3477* chip is selected which combines PWM controller, MEA and gate driver in one IC.

The Current Mode (CM) control scheme is adopted due to its excellent dynamic abilities[4, sec. 12-3-6] and simplified feedback regulator design. A low resistance $10\,m\Omega$ precision sense resistor measures the inductor current slope. The *LM3477* has build-in slope compensation to avoid current mode instabilities[4, sec. 12-1].

The converter switching frequency, f_{switch}, is chosen relatively high to $500\,kHz$. The increased switching losses are expected to by out-weighted by the fact that the low operating voltage limits switching losses and high frequency allows the inductor and filter components to be made smaller thus limiting system mass and the resistive losses in the inductor copper wires which are expected to dominate converter losses due to the relatively high currents.

The inductor current ripple, ΔI_L, can be calculated as

$$\Delta I_L = \frac{V_{in} - V_{out}}{L\,f_{switch}} D \tag{7}$$

where L is the inductance and f_{switch} the converter switching frequency. The inductor current ripple is usually limited to about 10 % of the maximum output current which was given in Table 3 as $10.8\,A$. Thus the minimum required inductance is calculated to

$$L = \frac{V_{in} - V_{out}}{\Delta I_L\, f_{switch}} D = \frac{14.4\,V - 7.4\,V}{1.08\,A \cdot 500\,kHz} \cdot 0.514 = 6.7\,uH \tag{8}$$

A $10\,uH$ inductor is chosen giving a current ripple of about $0.72\,A$. If the load current drops below $0.36\,A$, which is unlikely to happen in most operating modes, the converter will enter Discontinuous Conduction Mode (DCM).

For the converter output capacitor, a component is chosen which has very low Equivalent Series Resistor (ESR) and high capacitance to limit the output voltage ripples.

Current Sense Amplifier

With an inductor current ripple of $0.72\,A$ the current sense voltage slope is only

$$v_{sense} = \Delta I_L \cdot R_{sense} = 0.72\,A \cdot 10\,m\Omega = 7.2\,mV \tag{9}$$

It is recommended that the slope compensation is equal to or the double of the sense slope[4, sec. 12-1], however the minimum compensation slope is limited to $103\,mV$ by the *LM3477* chip. Thus the sensed slope signal must be amplified with a gain of around 20 being suitable. This also has the advantage of eliminating some of the typical noise susceptibility in the current sense signal. The current sense circuit in Figure 5 consists of two differential OpAmps which amplifies the current sense slope. Resistive voltage dividers are placed on the OpAmp inputs to scale down the input voltage signals to always be below the $5\,V$ OpAmp supply voltage.

Input Filter

An input filter is placed in front of the buck converter, mainly to draw a continuous current from the solar array. It also reduces the converter Electromagnetic Compatibility (EMC) issues. One challenge with the input filter is that it effects the dynamic properties of the converter and if not properly designed, it can degrade the control feedback loop performance. A damping network in the filter is also necessary to avoid instabilities[4, sec. 10-3].

A usable filter has been designed based on PSpice simulations. However thorough analysis still remains to be done to optimize the filter design.

3.3.2 Maximum Power Point Tracker Unit

In [1] it was decided to use a MPPTU with the SAR to increase solar array efficiency during changing environment conditions. The SAR with Maximum Power Point Tracking (MPPT) can operate in three different operation regions:

- Battery discharge - when the solar array input power is insufficient to cover the load power demand, the battery is slowly discharged in order to maintain the output voltage. The MPPTU controls the input solar array voltage.
- Battery charge - when the solar array input is greater than the load power, excessive power is used to recharge the battery. The MPPTU controls the input solar array voltage.
- Input power limitation - when the battery is fully charged, the regulator will operate the solar array at a non-optimal voltage, thus limiting the input power to keep the output voltage at a maximum limit. The extra potential input power is dissipated as heat externally on the solar arrays.

It is preferred to implement an analog MPPTU mainly since this makes the circuit independent on a control signal from a more complicated external Micro-Controller Unit (MCU) or Digital Signal Processor (DSP) thus allowing a flexible plug'n-play system to be implemented. One challenge with an analog MPPTU is the typical need for expensive analog multipliers[5]. Since the required multiplier only needs to be a 1st quadrant type (only two positive inputs), it is believed that a low-cost multiplier can be build using standard discrete components[6].

The MPPTU design still remains to be completed.

3.3.3 Mode Transitions

As was discussed in Section 3.3.2, the SAR can operate in three different main modes. The transition between the modes is controlled by the mainbus output voltage as shown in Figure 4. If the SAR input power is lower than the load power, the battery will discharge and the mainbus voltage will follow the battery voltage. Once the input power is larger than the load power, the mainbus capacitor will quickly be charged to a voltage higher than the battery voltage. Once the mainbus capacitor voltage crosses the $9.2\,V$ charge threshold, the BCR starts to charge the battery. If the input power is still higher than the combined battery charge power and load power, the mainbus capacitor voltage continues to rise until reaching $9.5\,V$ where the SAR enters the input power limitation mode. The battery may still be charging in this mode. Since the battery is charged with constant current, the input power may be lower than the combined charge and load power but higher than the load power alone. Hence an oscillatory state between battery charge and discharge mode may rise whose frequency depends on the mainbus capacitance which should therefore be large.

The $9.20\,V$ battery charge threshold voltage is calculated from

$$V_{charge,threshold} = V_{UVLO,BCR} + V_F = 8.90\,V + 0.3\,V = 9.20\,V \tag{10}$$

where $V_{UVLO,BCR}$ is the worst-case UVLO threshold voltage of the BCR IC and V_F is the reverse protection diode forward voltage drop.

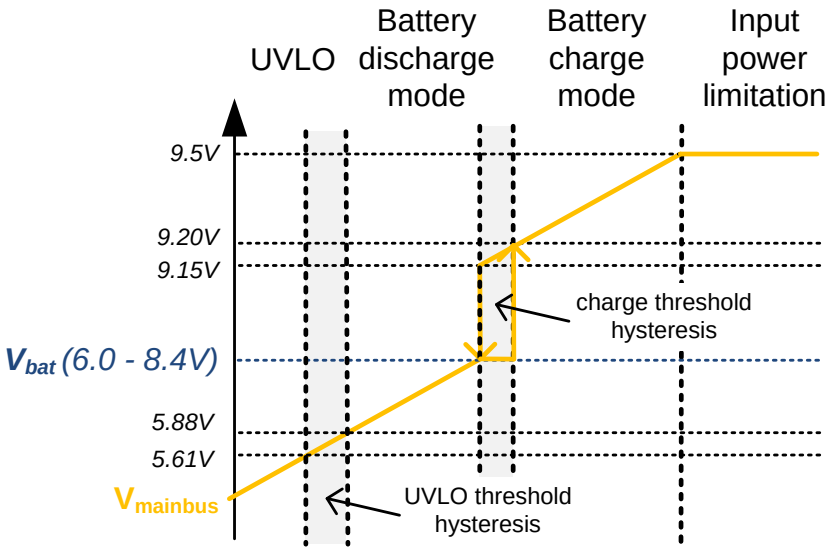


Figure 4 – *Different SAR operation modes as function of mainbus voltage*

3.4 5V Regulator

To provide a regulated $5\,V$ supply for the on-board computer and payloads, a *MIC29300-5* Low-dropout (LDO) regulator is selected. A $2\,A$ resettable Positive Temperature Coefficient (PTC) fuse is added to protect the loads from excessive currents and to protect the battery in case of a payload short-circuit failure.

3.5 Complete Electrical Power System Diagram

The complete EPS diagram is shown in Figure 5. Two $17\,A$ fuses are added in front of the motors, to protect the battery from a motor short-circuit failure.

3.6 External Interfaces

The interfaces of the EPS external are listed in table 7.

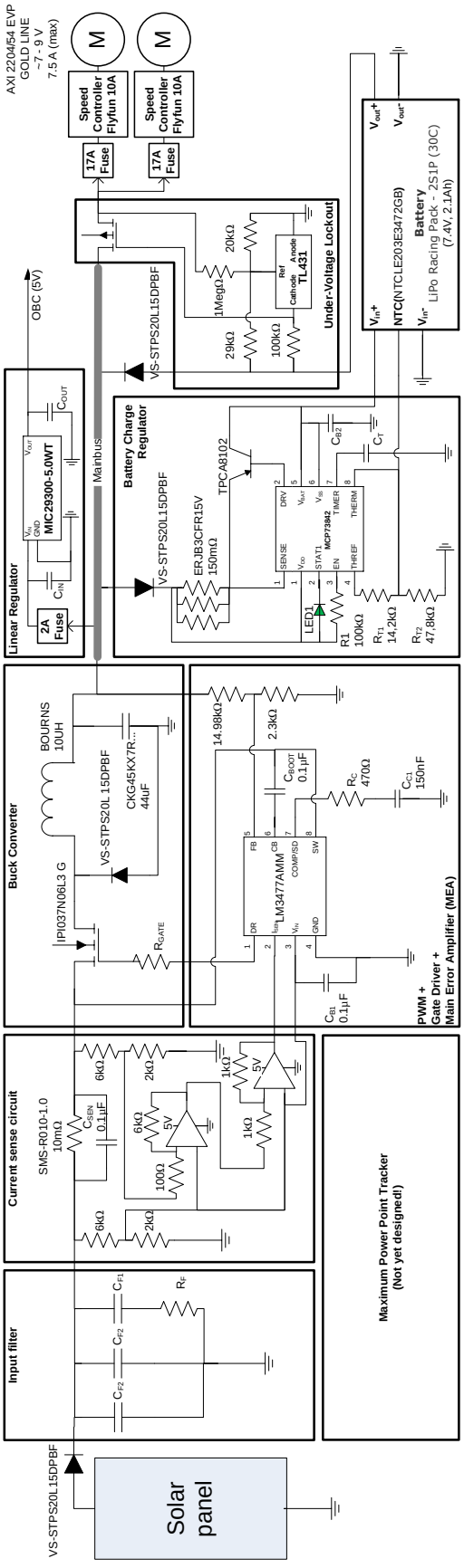


Figure 5 – *EPS detailed block diagram*

Table 7 – *External interfaces*

External interface	Type	Implementation
Solar cells mounting	Mechanical	To Be Decided (TBD) (possibly using PSA)
Power electronics mounting	Mechanical	Mounted on a Printed Circuit Board (PCB) which sits in the cargo bay, attached with screws
Battery mounting	Mechanical	Mounted in cargo bay with strips or Velcro. Thermal insulation with styrofoam or similar material should be added to protect against cold temperatures.
EPS telemetry	Electrical	Analog signals to Microcontroller. Electrical connector interface still remains TBD
EPS telecommands	Electrical	TBD
Output voltages	Electrical	$6.0 - 9.5\,V$ (unregulated) and $5.0\,V$(regulated)

3.7 Telemetry and Telecommands

The suggested EPS telemetries are listed in Table 8 and the suggest telecommands in Table 9. Not all telemetries or the telecommands are part of the initial EPS design and will only be implemented if time and ressources allow it.

The exact electrical configuration and interface connectors still remains to be designed.

Table 8 – *EPS telemetry*

Telemetry	Data rate	Data size	Data range
Battery voltage	Every 5 sec	2 bytes	TBD
Battery temperature	Every 5 sec	2 bytes	TBD
BCR status	Every 5 sec	1 byte	high($5\,V$), low($0\,V$) and $1\,Hz$ 50% duty cycle ripple[1]
UVLO status	Every 5 sec	1 byte	$0\,V$(nominal operation), $5\,V$(under-voltage lock-out)
Mainbus voltage	Every 5 sec	2 bytes	TBD
Solar array temperature	Every 5 sec	2 bytes	TBD
Solar array voltage	Every 1 sec	2 bytes	TBD

Table 9 – *EPS telecommands*

Telecommand	Command format	Description
Battery charge inhibit	TBD	Battery charging can be remotely terminated in case of battery anomalies
Solar array voltage set	TBD	When MPPT is running, the solar array operating voltage can manually be set to mitigate any malfunction in the MPPT algorithm

4 Test and Verification of Design

This section describes the various design models used to develop the EPS along with the expected functional test to be executed.

4.1 EPS Design Models

4.1.1 EPS PSpice Simulations

A transient PSpice simulation model of the whole EPS is currently being implemented. The completed PSpice models are shown in Appendix A.1. These will help in the design and testing of the regulator performance and system stability during transient loading as well as the interactions between the different circuits.

In future, it is desired also to implement transient PSpice models for the solar array[7], MPPTU, battery[8], motors and BCR.

4.1.2 EPS Development Model

An EPS Development Model (DM) is currently being build as seen in Figure 6. The prototype PCB is realized using self-made "mini-mount" PCB pads as shown in Appendix A.2. These pads are attached, using a simple glue roller, on a complete copper ground plane. This design approach allows a compact layout which reduces parasitic effects. Also any IC package can be supported and parts can easily be moved around if the design changes.

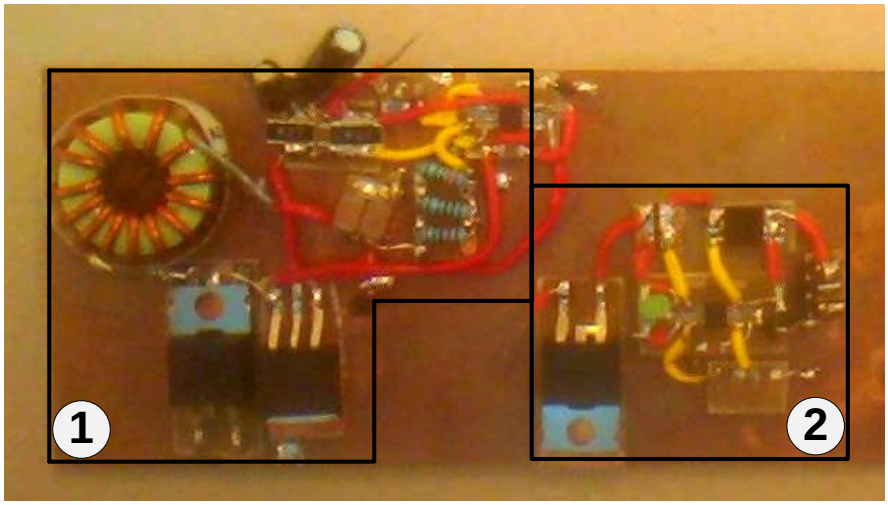


Figure 6 – *EPS prototype - **1**:SAR, **2**:BCR*

Development Model Status

The SAR is working but shows signs of CM instability which is expected to be caused by the missing current sense amplifier circuit and input filter. Development progress is currently awaiting delivery of components.

The BCR is also working however excessive heating of the MOSFET was experienced. A new part rated for higher power dissipation has been selected and is currently awaiting delivery.

4.1.3 EPS Flight Model

If time allows, a dedicated Flight Model (FM) will be build, using a custom designed PCB schematic layout. An optimized PCB layout will minimize the system mass and size while maximizing the efficiency and system robustness.

4.2 EPS Test Program

Table 10 lists all necessary and desired test of the EPS. Priority "1" tests are all required while priority "2" tests will only be realized if time and resources allow it.

Table 10 – *EPS Test Program*

Subsystem	Condition/Mode	Test Description	Pri.
SAR	Mainbus voltage limitation	With more input power than load power, SAR must be able to maintain a stable $9.5\,V$ output voltage also during transient loading	1

-	Maximum power handling	With an input and load power slightly above the maximum expected solar array power, no SAR components must overheat or otherwise malfunction	1
-	MPPT	TBD	2
-	Mode transitions	SAR must be able to change between MPPT, battery charge and discharge mode without loosing mainbus voltage regulation or causing other malfunctions	2
-	Feedback loop stability	Regulator bandwidth, gain- and phase margins should be measured with a Network Analyzer	2
-	EMC	Electromagnetic emissions should be measured with a Spectrum Analyzer, especially with concerns to the telecommunication systems	2
BCR	CC and trickle charging	CC charge at $2.4\,A$ and trickle charge mode entered when battery voltage reaches $8.4\,V$ should be verified	1
-	Charge inhibit at high/low temperatures	While battery is charging, battery thermistor is heated/cooled in thermal oven/fridge to slightly above/below the specified temperature limits and charging should be terminated	1
UVLO	Power cut-off and recovery	Reducing input voltage below calculated threshold voltage should open switch and switch should close again when input voltage is increased above the threshold	1
Battery	Dynamic model	Test approach is described in [9]	2
Solar cell	I-V specifications	short-circuit current, open-circuit voltage, current and voltage at the **MPP!** (**MPP!**) should be determined from an irradiance test	2

-	Temperature coefficients	Solar cell temperature coefficients should be determined be measuring the I-V characteristics at different temperatures within the expected temperature interval	2
Fuses	Temperature variation	The PTC resettable fuses should be tested at nominal, minimum and maximum expected temperatures to verify acceptable functionality	1

5 Resources and Scheduling

5.1 Main Tasks

TBD...

5.2 Parts List and Costs

Table 11 lists all ordered EPS parts (including one order which is expected to be placed in the near future). The calculated costs does not including invoicing or shipping costs.

Table 11 – *EPS Parts List*

Part	**Part Name**	**Supplier**	**Cost**[1]	**Qty.**
SAR current sense resistor	FCSL110R010FER	Farnell(US)	31.52	2
SAR power diode	MBR3050CT	Farnell	9.24	3
SAR power MOSFET	IPI037N06L3 G	Farnell	19.32	4
SAR mainbus capacitor	CKG45NX5R1C226M	Farnell	38.72	4
PWM, MEA and MOSFET driver	LM3477AMM	Farnell	16.37	5
SAR inductor	2101-H-RC	Farnell(US)	25.13	2
PCBs	CIF - AA15	Farnell	67.42	4
Battery(obsolete)	PA-L60	Farnell	294.28	2
Battery	LiPo Racing Pack 2S1P	Ansmann	N/A[2]	1
Reverse protection diode	VS-STPS20L15DPBF	Farnell	24.56	6
BCR	MCP73842-840I/UN	Farnell	13.61	2
BCR Transistor(obsolete)	TPCA8102(TE12L,Q)	Farnell	28.5	2

Table 11 – *EPS Parts List*

Part	**Part Name**	**Supplier**	**Cost**[1]	**Qty.**
Current limit Bipolar Junction Transistor (BJT)(obsolete)	2STN2540	Farnell	7.84	5
Current limit MOSFET(obsolete)	IRLML6401PBF	Farnell	6.41	2
BCR current sense resistor	ERJB3CFR15V	Farnell	1.97	5
Current limit sense resistor(obsolete)	ERJB2BFR33V	Farnell	4.83	5
Current limit sense resistor 2(obsolete)	ERJA1BJR27U	Farnell	5.30	5
Power limit BJT(obsolete)	STN888	Farnell	5.49	5
Solar cell	RC7.2-75(PSA)	Eco Power Shop	230.08	2
Solar cell(obsolete)	MC-SP0.8-NF-GCS	Farnell	66.51	2
LDO regulator	MIC29300-5.0WT	Farnell	74.85	2
Current sense OpAmp	LTC6362CMS8# PBF	Farnell	32.31	2
Thermistor	NTCLE203E3472GB0	Farnell	8.64	5
Motor fuses	RGEF1000	Farnell	6.46	5
LDO regulator fuses	MC36248	Farnell	1.41	5
BCR MOSFET	SUP75P03-07-E3	Farnell	31.51	2
UVLO linear shunt regulator	TL431AILPME3	Farnell	1.36	5
UVLO MOSFET	SUP75P03-07-E3	Farnell	31.51	2
Total cost			2707.6	

5.3 Electronics Ground Support Equipment

The Electronic Ground Support Equipment (EGSE) in Table 12 is mainly required for testing of the EPS.

Table 12 – *Required EGSE*

Instrument	**Required Specifications**
Network Analyzer	Up to about $\sim 1\,MHz$
Spectrum Analyzer	TBD
Power supply	$75\,W$ output power at $\sim 15\,V$
Heating and cooling chamber(s)	$-20°C$ to $+45°C$ and allow small wires to be pulled through chamber

5.4 Mechanical Ground Support Equipment

The required Mechanical Ground Support Equipment (MGSE) is mainly for PCB manufacturing, i.e. UV light source, photo developing facility, etching facility, drills, cutters etc.

References

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[5] Z. Liang, R. Guo, and A. Huang. "A New Cost-Effective Analog Maximum Power Point Tracker for PV Systems". In: *IEEE* (2010).

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[9] M. Chen and A. R. Gabriel. "Accurate Electrical Battery Model Capable of Predicting Runtime and I-V Performance". In: *IEEE Transactions on Energy Conversion* (2006).

Appendices

A EPS

A.1 PSpice Simulations

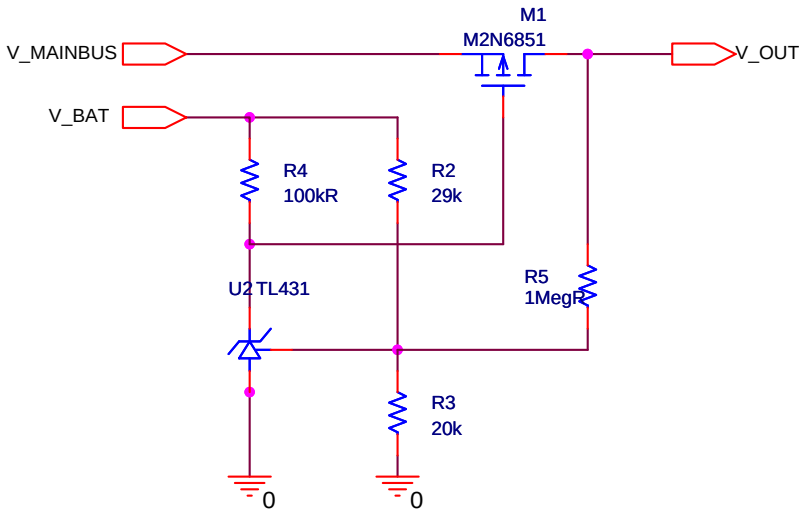

Figure 7 – *EPS UVLO circuit PSpice simulation*

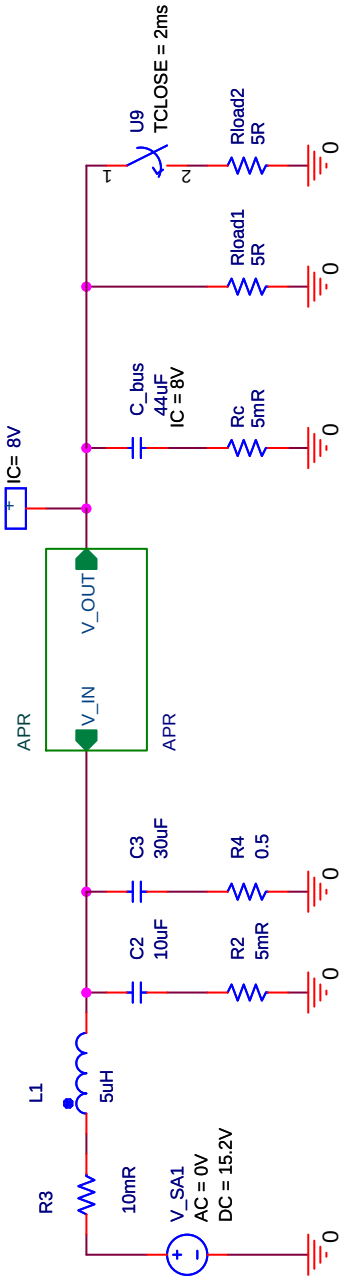

Figure 8 – *EPS mainbus PSpice simulation*

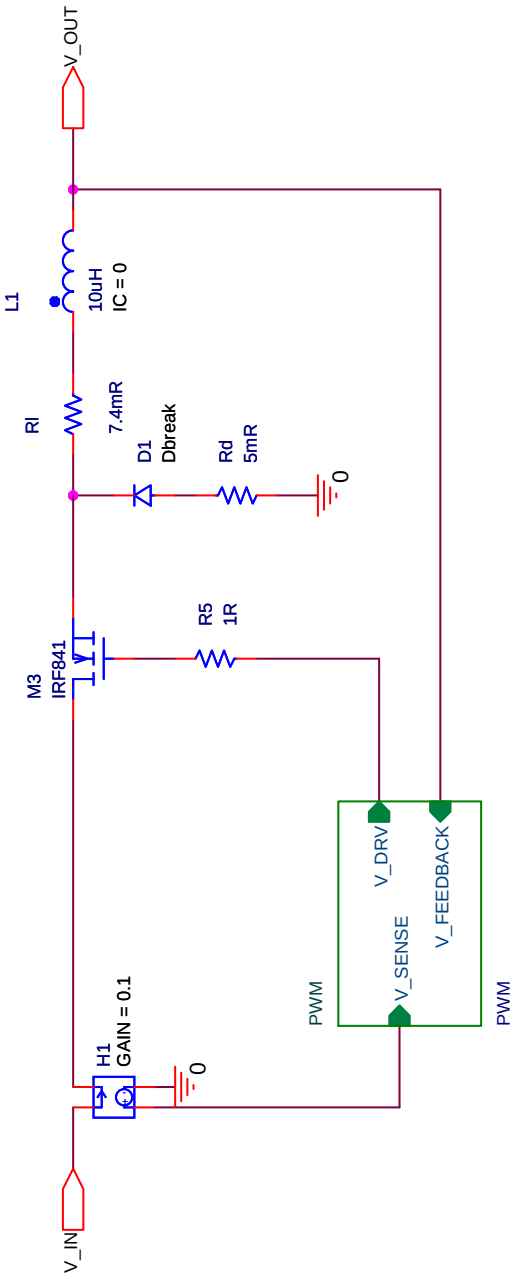

Figure 9 – *EPS SAR PSpice simulation*

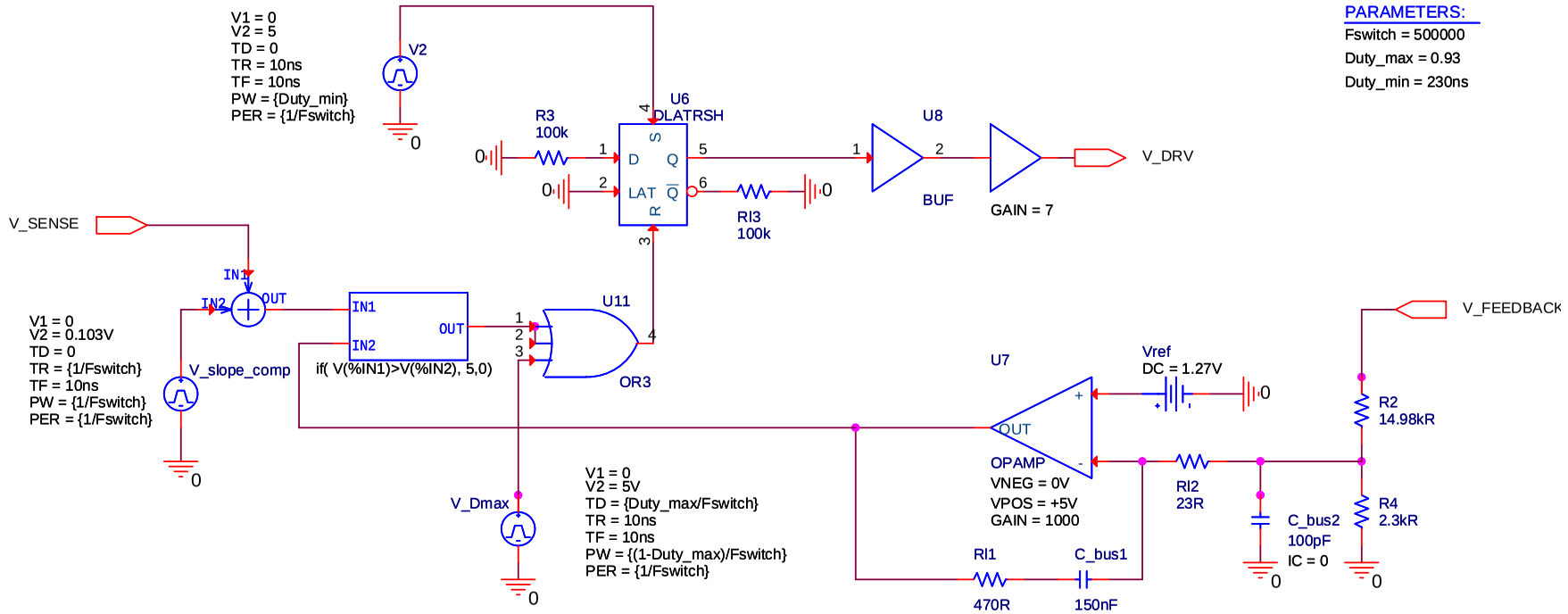

Figure 10 – *EPS PWM controller PSpice simulation*

A.2 Mini-Mount Image

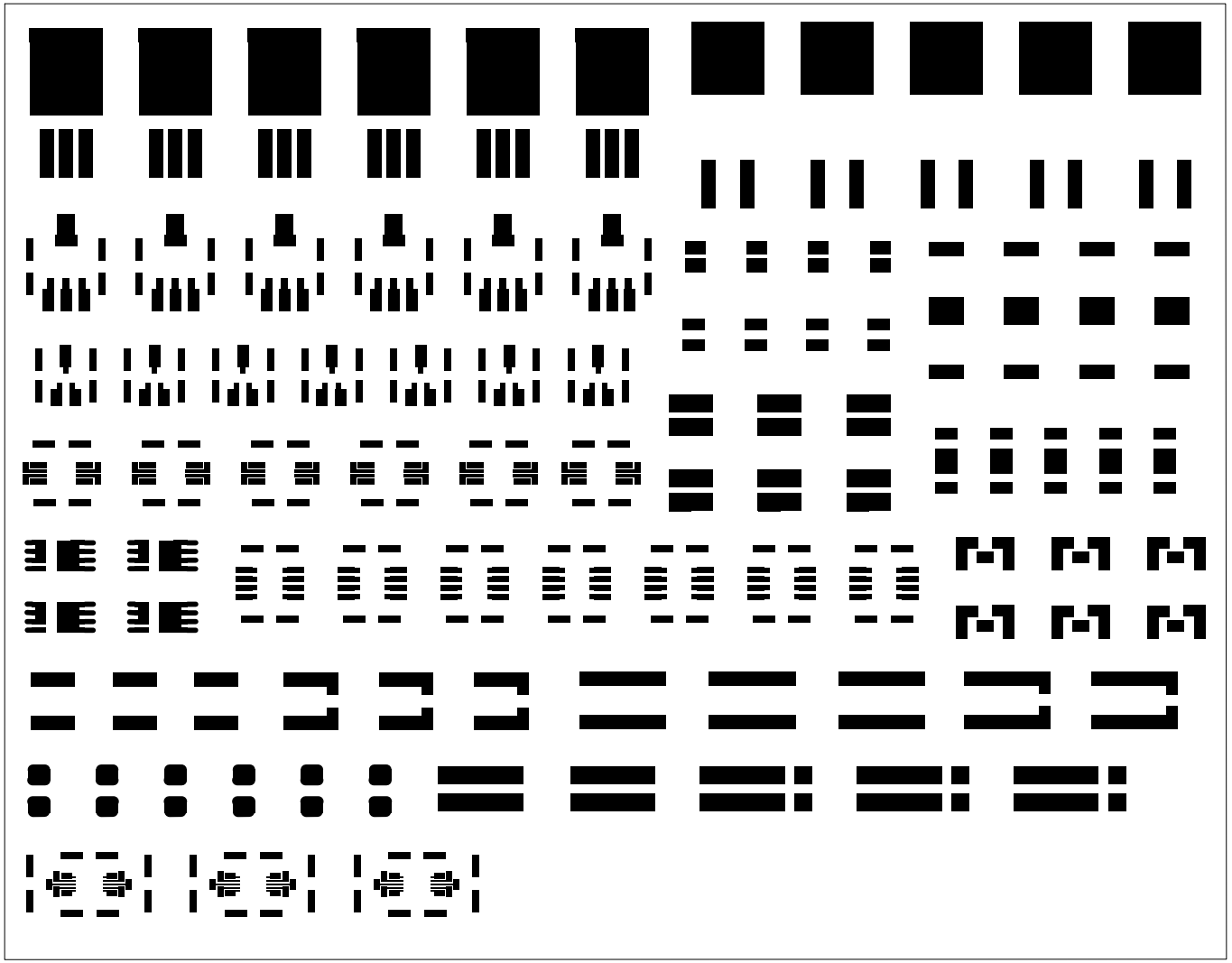

Figure 11 – *Mini-mount prototype patches*