Integrated EEPROM's

Single channel, monochrome on-screen display

overview

The AT7456E is a single-channel, monochrome follow-up screen with integrated EEPROM Display generator with integrated video driver, sync separator, video splitter Off and EEPROM, improve the integration of the system, effectively reduce the system cost Book.

AT7456E adopts 512 user-configurable Programming characters, suitable for global markets.

AT7456E can conveniently display various information in arbitrary characters and sizes, Such as company logo, commonly used graphics, time, date, etc.

The AT7456E is preloaded with 512 characters and graphics, and can be SPI compatible serial interface for in-circuit programming.

AT7456E is available in 28-pin TSSOP package, operating temperature range (-40°C ~+85ÿÿÿ

characteristic

ÿ 512 user-defined characters or graphics stored in EEPROM

ÿ Character size is 12×18 pixels

ÿ Flashing, inverted and background control characters

ÿ Brightness can be set line by line

ÿ Display up to 16 rows x 30 columns of characters

ÿ Video driver output with attenuation compensation

ÿ *LOS, VSYNC , HSYNC* and clock output ÿ Built-in sync generator, and external composite sync signal can be input

ÿ Compatible with NTSC and PAL

ÿ SPI compatible serial interface

ÿ Factory with pre-programmed character set

application

Security Monitoring System

security camera

industrial monitoring

indoor entertainment system

Handheld Measuring Instruments

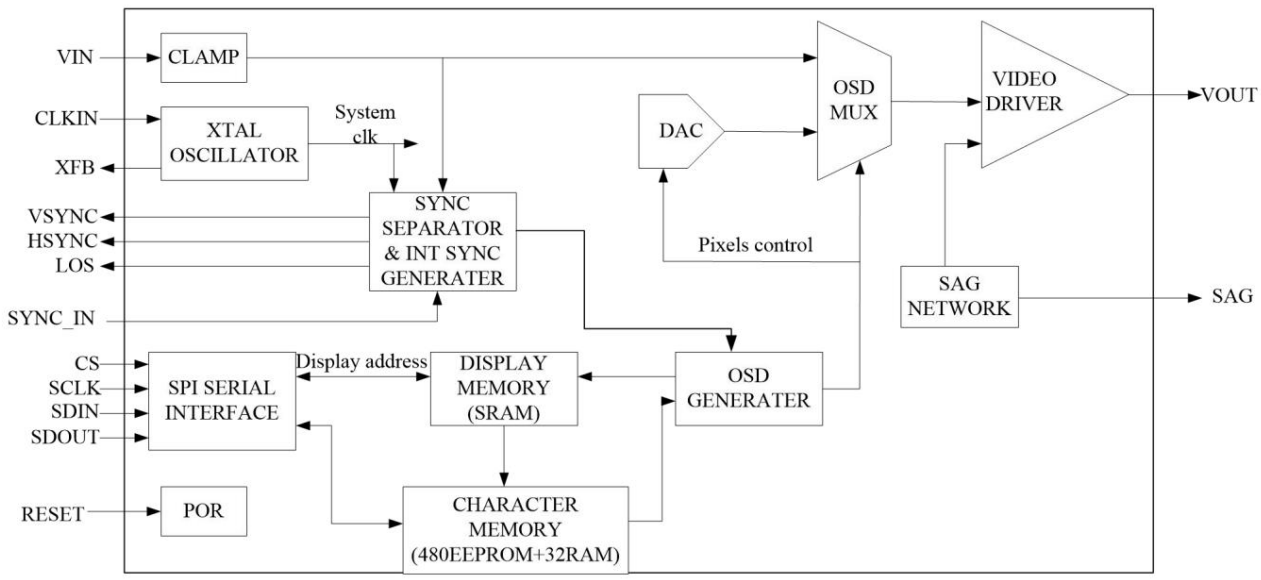
consumer electronics

Order Information

AT7456E	HTSSOP28	Chinese

Note: AT7456E is compatible with MAX7456, but some adjustments are required for the application program, see the application information section (Page35) for details.

Block diagram of circuit function structure



Extreme working conditions:

AVDD to AGND ....-0.3V to +6V

DVDD to DGND..... .....-0.3V to +6V

PVDD to PGND..... .....-0.3V to +6V

AGND to DGND..... .....-0.3V to +0.3V

AGND to PGND..... .....-0.3V to +0.3V

DGND to PGND..... .....-0.3V to +0.3V

VIN, VOUT, SAG to AGND.....-0.3V to (VAVDD + 0.3V)

HSYNC ,*VSYNC* , LOS to AGND .....-0.3V to +6V

RESET to AGND .....-0.3V to (VAVDD + 0.3V)

CLKIN, CLKOUT, XFB to DGND .....-0.3V to (VDVDD + 0.3V)

SDIN, SCLK, *CS* SDOUT to DGND.....-0.3V to (VDVDD + 0.3V)

Maximum Continuous Current into VOUT.....±100mA

Continuous Power Dissipation (TA = +70°C)

28-Pin TSSOP (derate 27mW/°C above +70°C).....2162mW*

Operating Temperature Range .....-40°C to +85°C

Junction Temperature.....+150°C

Storage Temperature Range .....-60°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Electrical characteristic parameters:

(VAVDD = +3.15V to +5.25V, VDVDD = +3.15V to +5.25V, VPVDD = +3.15V to +5.25V, TA = TMIN to TMAX. Typical values are at VAVDD= VDVDD = VPVDD = +5V, TA = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	VAVDD		3.15	5	5.25	IN
Digital Supply Voltage	VDVDD		3.15	5	5.25	IN
Driver Supply Voltage	VPVDD		3.15	5	5.25	IN
Analog Supply Current	IAVDD	VIN= 1VP-P(100% white flat field signal), VOUT load, RL= 150ÿ	2.0	2.2	2.5	mA
Digital Supply Current	IDVDD	VIN= 1VP-P(100% white flat field signal), VOUT load, RL= 150ÿ	16	43.1	60	mA
Driver Supply Current	IPVDD	VIN= 1VP-P(100% white flat field signal), VOUT load, RL= 150ÿ	4.0	6.0	10	mA
NONVOLATILE MEMORY						
Data Retention		TA= +25°C		100		Years
Endurance		TA= +25°C		100,000		Stores
DIGITAL INPUTS *(CS* , **SDIN,** *RESET* **, SCLK)**						
Input High Voltage	HIV		2.0	2.1		IN
Input Low Voltage	WILL			1.4	0.8	IN
Input Hysteresis	VHYS			50		mV
Input Leakage Current		VIN= 0 or VDVDD			±10	uA
Input Capacitance	CIN			5		pF
DIGITAL OUTPUTS (SDOUT, CLKOUT, HSYNC,VSYNC , **LOS)**						
Output High Voltage	VOH	ISOURCE= 4mA (SDOUT, CLKOUT)	2.4	4.88		IN
Output Low Voltage	VOL	ISINK= 4mA		0.16	0.45	IN
Tri-State Leakage Current		SDOUT, *CS* = VDVDD			±10	uA
CLOCK INPUT (CLKIN)						
Clock Frequency				27		MHz
Clock-Pulse High			14	18.4		ns
Clock-Pulse Low			14	18.8		ns
Input High Voltage			0.65 x VDVDD			IN

Input Low Voltage				0.3 x VDVDD V		
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Leakage Current		VIN= 0V or VDVDD		±5	±50	uA
CLOCK OUTPUT (CLKOUT)						
Duty Cycle		5pF and 10kÿto DGND	40	51.6	60	%
Rise Time		5pF and 10kÿto DGND		3.2		ns
Fall Time		5pF and 10kÿto DGND		3.6		ns
VIDEO CHARACTERISTICS						
DC Power-Supply Rejection		VAVDD= VDVDD= VPVDD= 5V; VIN= 1VP-P, measured at VOUT		40		dB
AC Power-Supply Rejection		VAVDD= VDVDD= VPVDD= 5V; VIN= 1VP-P, measured at VOUT; f = 5MHz; power-supply ripple = 0.2VP-P		30		dB
Short-Circuit Current		VOUT to PGND		200	230	mA
Line-Time Distortion	LTD	Figures 1a, 1b			0.5	%
Output Impedance	SALT	Figures 1a, 1b		0.22		Oh
Gain		Figures 1a, 1b	1.89	2.0	2.11	V/V
Black Level		At VOUT, Figures 1a, 1b		1.26AGND+1.5V		
Input-Voltage Operating Range	COME	Figures 1a, 3 (Note 2)	0.5		1.2	VP-P
Input-Voltage Sync Detection Range	VINSD	Figures 1a, 3 (Note 3)	0.5		2.0	VP-P
Maximum Output-Voltage Swing VOUT	Figures 1a, 1b		2.4	2.66		VP-P
Output-Voltage Sync Tip Level				0.7		IN
Large Signal Bandwidth (0.2dB)	BW	VOUT= 2VP-P, Figures 1a, 1b		6		MHz
VIN to VOUT Delay				20		ns
Differential Gain	DG			0.5		%
Differential Phase	DP			0.5		Degrees
OSD White Level		VOUT 100% white level with respect to black level	1.25	1.33	1.45	IN
Horizontal Pixel Jitter		Between consecutive horizontal lines		24		ns
Video Clamp Settling Time				32		Lines
OSD CHARACTERISTICS						
OSD Rise Time		OSD insertion mux register OSDM[5,4,3] = 011b		68		ns
OSD Fall Time		OSD insertion mux register OSDM[5,4,3] = 011b		68		ns
OSD Insertion Mux Switch Time		OSD insertion mux register OSDM[2,1,0] = 011b		110		ns

Time characteristic parameters:

(VAVDD = +3.15V to +5.25V, VDVDD = +3.15V to +5.25V, VPVDD = +3.15V to +5.25V, TA = TMIN to TMAX. Typical values are at VAVDD= VDVDD = VPVDD = +5V, TA = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP MAX UNITS	
SPI TIMING				
SCLK Period	tCP		100	ns
SCLK Pulse-Width High	tCH		40	ns
SCLK Pulse-Width Low	tCL		40	ns
$\overline{CS}$ Fall to SCLK Rise Setup	tCSS0		30	ns
$\overline{CS}$ Fall After SCLK Rise Hold	tCSH0		0	ns
$\overline{CS}$ Rise to SCLK Setup	tCSS1		30	ns
$\overline{CS}$ Rise After SCLK Hold	tCSH1		0	ns
$\overline{CS}$ Pulse-Width High	tCSW		100	ns
SDIN to SCLK Setup	tDS		30	ns
SDIN to SCLK Hold	tDH		0	ns
SDOUT Valid Before SCLK	tDO1	20pF to ground	25	ns
SDOUT Valid After SCLK	tDO2	20pF to ground	0	ns
$\overline{CS}$ High to SDOUT High Impedance	tDO3	20pF to ground	300	ns
$\overline{CS}$ Low to SDOUT Logic Level	tDO4	20pF to ground	20	ns
$\overline{HSYNC}$,$\overline{VSYNC}$, **AND LOS TIMING**				
THE, $\overline{VSYNC}$. $\overline{HSYNC}$ Valid before CLKOUT Rising Edge	tDOV	20pF to ground	30	ns
VOUT Sync to $\overline{VSYNC}$ Falling Edge Delay	tVOUT-VSF	NTSC external sync mode, Figure 4	375	ns
		PAL external sync mode, Figure 6	400	
VOUT Sync to $\overline{VSYNC}$ Rising Edge Delay	tVOUT-VSR	NTSC external sync mode, Figure 4	400	ns
		PAL external sync mode, Figure 6	425	
$\overline{VSYNC}$ Falling Edge to VOUT Sync Delay	tVSF-VOUT	NTSC internal sync mode, Figure 5	40	ns
		PAL internal sync mode, Figure 7	45	
$\overline{VSYNC}$ Rising Edge to VOUT Sync Delay	tVSR-VOUT	NTSC internal sync mode, Figure 5	32	ns
		PAL internal sync mode, Figure 7	30	
VOUT Sync to $\overline{HSYNC}$ Falling Edge Delay	tVOUT-HSF	NTSC and PAL external sync mode, Figure 8	310	ns
VOUT Sync to $\overline{HSYNC}$ Rising Edge Delay	tVOUT-HSR	NTSC and PAL external sync mode, Figure 8	325	ns
$\overline{HSYNC}$ Falling Edge to VOUT Sync Delay	tHSF-VOUT	NTSC and PAL internal sync mode, Figure 9	115	ns
$\overline{HSYNC}$ Rising Edge to VOUT Sync Delay	tHSR-VOUT	NTSC and PAL internal sync mode, Figure 9	115	ns
All Supplies High to $\overline{CS}$ Low	tPUD	Power-up delay	50	ms
NVM Write Busy	tNVW	27MHz CLK	3.4/4.2	ms

Note 1: See the standard test circuits of Figure 1. RL = 75 unless otherwise specified. All digital input signals are timed from a voltage level of (VIH + VIL) / 2. All parameters are tested at TA = +85°C and values through temperature range are guaranteed by design.

Note 2: The input-voltage operating range is the input range over which the output signal parameters are guaranteed (Figure 3).

Note 3: The input-voltage sync detection range is the input composite video range over which an input sync signal is properly detected and the OSD signal appears at VOUT. However, the output voltage specifications are not guaranteed for input signals exceeding the maximum specified in the input operating voltage range (Figure 3).

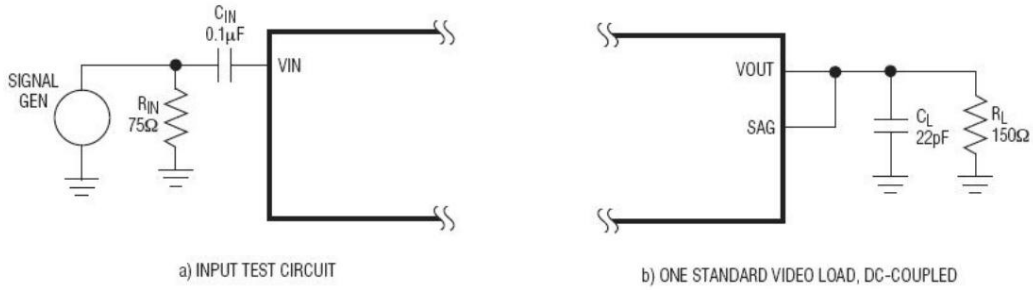


Figure 1. Standard Test Circuit

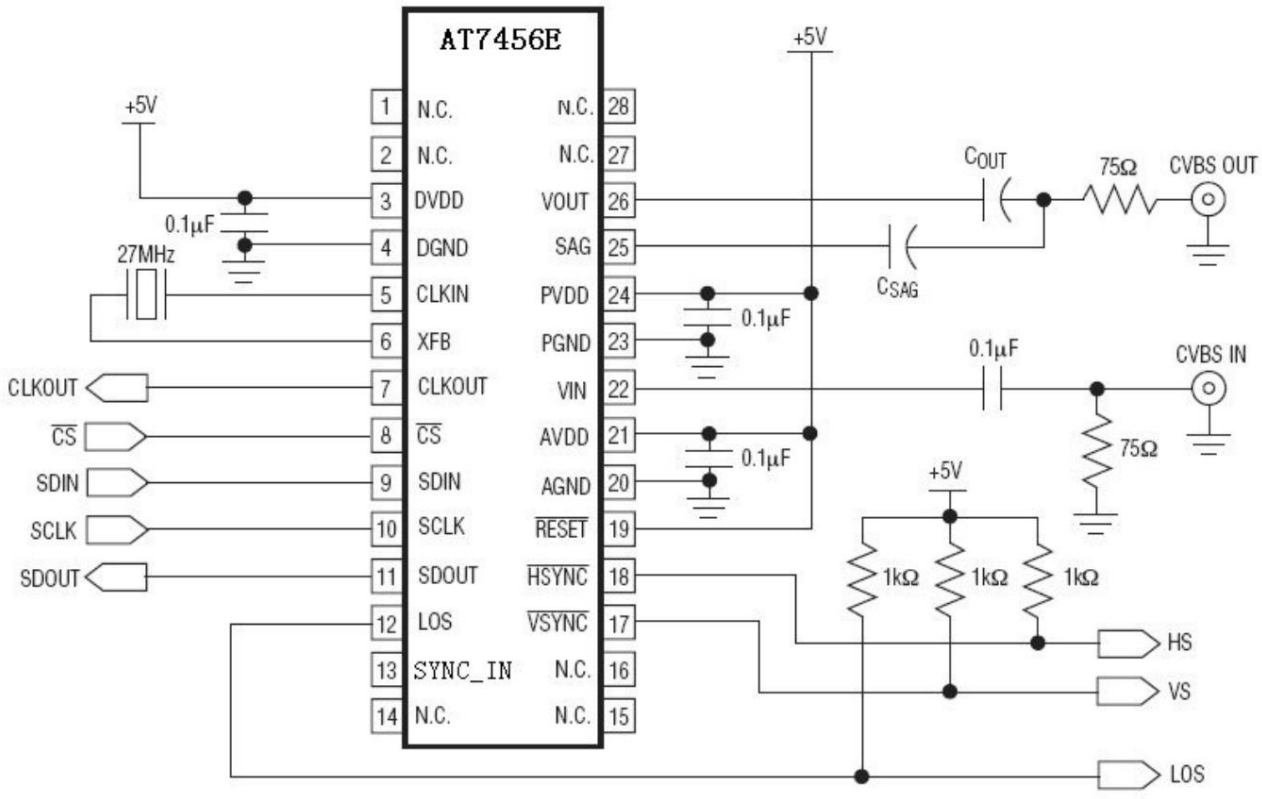


Figure 2. Typical Operating Circuit

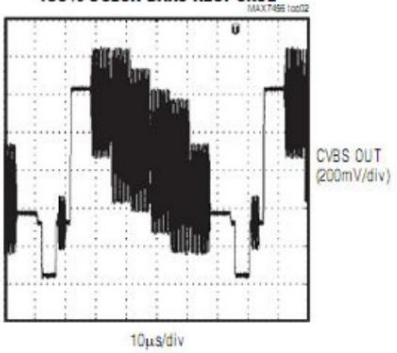
Pin description:

pin name		Function
1, 2, 13–16, 27, 28	NC	is not connected, internally floating
3	DVDD	Digital power input, connect a 0.1uF bypass capacitor to DGND.
4	DGND	digital ground
5	CLKIN	Crystal Connection 1, connect a parallel transistor oscillator between CLKIN and XFB, or use a 27MHz system reference clock to drive CLKIN directly.
6	XFB	Crystal oscillator connection 2, connect a parallel transistor oscillator between CLKIN and XFB, if using 27MHz system reference clock to drive CLKIN directly, XFB is floating.
7	CLKOUT	Clock output, 27MHz logic level output system clock.
8	$\overline{CS}$	low level active chip select input, when $\overline{CS}$ is high level, SDOUT becomes high resistance.
9	SDIN	Serial data input, data is read in at the rising edge of SCLK.
10	SCLK	Serial clock input, clocks data input to SDIN and output from SDOUT, duty cycle must be between 40% and 60%.
11	SDOUT	Serial data output, the data is read out on the falling edge of SCLK. When *CS* is high level, it becomes high resistance.
12	THE	Loss of Synchronization Output (Open Drain). LOS goes high when the VIN sync pulse is missing for 32 consecutive cycles. When 32 consecutive valid sync pulses are received When rushing, LOS goes low. Connect through a 1Kÿ pullup resistor to the positive power supply of DVDD or another compatible sink device.
13	SYNC_IN	External composite sync signal input
17	$\overline{VSYNC}$	*Field sync output (open drain). VSYNC goes low during video input field sync. VSYNC can be recovered from VIN or at* Internally generated in internal synchronous mode. Connect through a 1Kÿ pullup resistor to the positive power supply of DVDD or another compatible sink device.
18	$\overline{HSYNC}$	Line Synchronous Output (Open Drain). HSYNC goes low during video input line sync . HSYNC can be recovered from VIN or at Internally generated in internal synchronous mode. Connect through a 1Kÿ pullup resistor to the positive power supply of DVDD or another compatible sink device.
19	$\overline{RESET}$	System reset input. The minimum RESET pulse width is 1uS. 50ms after the rising edge of RESET, all SPI registers are reset to their default values. During this time, read and write access to the registers is not possible. 40us after the rising edge of RESET, all display units in the display memory are reset bit to the default value 00H.
20	AGND	analog ground
21	AVDD	Analog power input, connect a 0.1uF bypass capacitor to AGND.
22	COME	PAL or NTSC CVBS video input
23	PGND	drives ground, at a point allied to AGND
24	PVDD	Driver power input, connect a 0.1uF bypass capacitor to PGND.
25	SAG	Voltage decay correction input, if not used must be connected to VOUT, refer to Figure 1b.
26	VOUT	video output
-	EP	Exposed Pad. Internally connected to AGND, connect EP to the AGND plane for better thermal performance. Do not use EP as a ground connection for displacement.

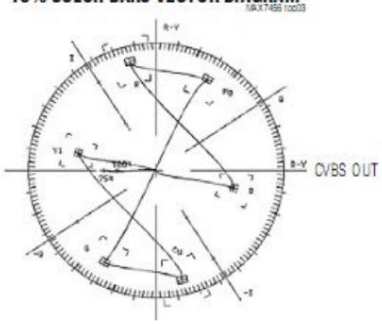
Typical operating characteristics:

(VAVDD = +5V, VDVDD = +5V, VPVDD = +5V, TA = +25°C, unless otherwise noted. See the Typical Operating Circuit of Figure 2, if applicable.)

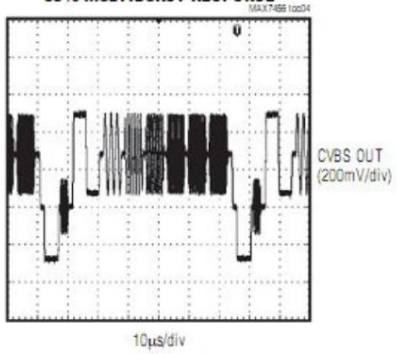
100% COLOR BARS RESPONSE



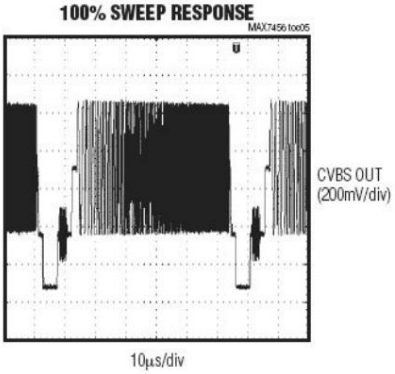
75% COLOR BARS VECTOR DIAGRAM



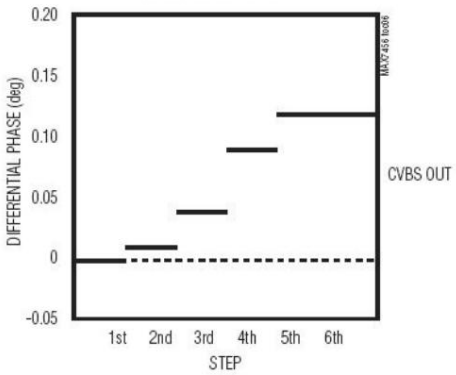
60% MULTIBURST RESPONSE



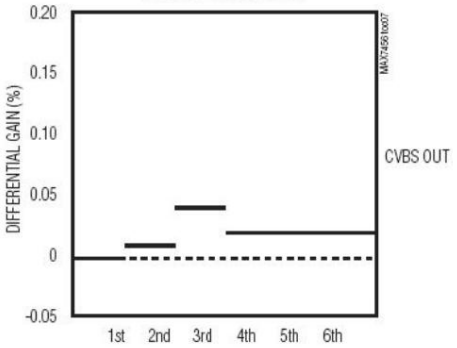
100% SWEEP RESPONSE



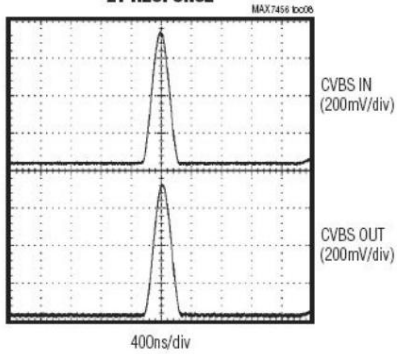
DIFFERENTIAL PHASE



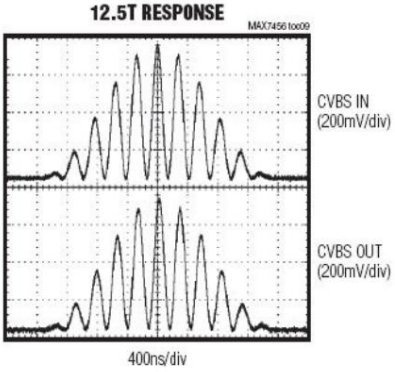
DIFFERENTIAL GAIN



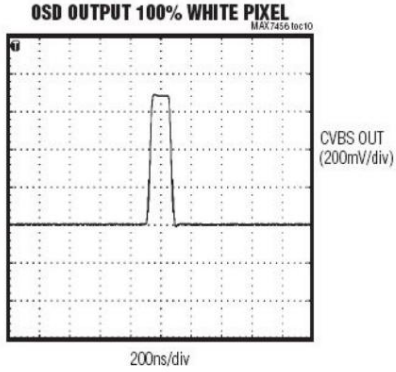
2T RESPONSE



12.5T RESPONSE

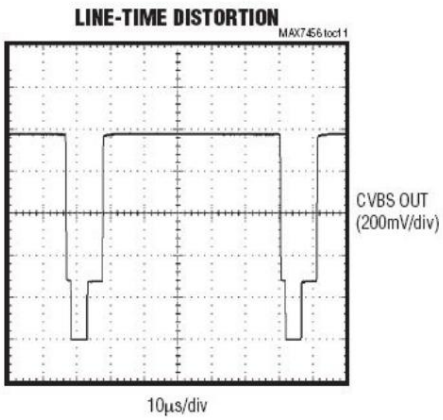


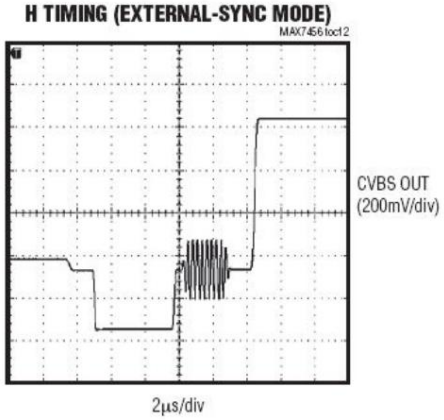
OSD OUTPUT 100% WHITE PIXEL

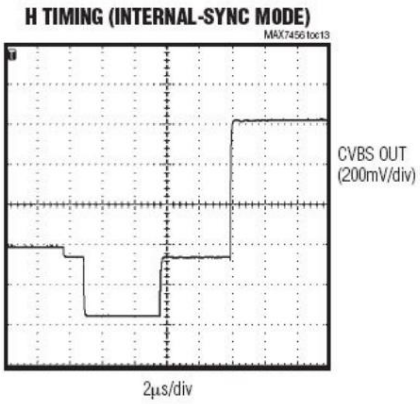


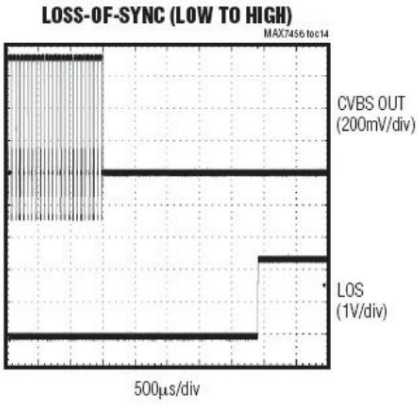
Typical operating characteristics:

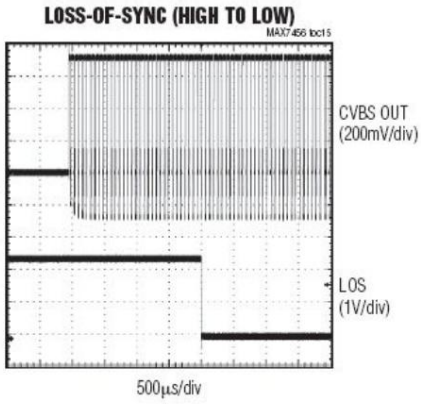
(VAVDD = +5V, VDVDD = +5V, VPVDD = +5V, TA = +25°C, unless otherwise noted. See the Typical Operating Circuit of Figure 2, if applicable.)











Circuit function detailed description:

The AT7456E single-channel monochrome on-screen display (OSD) generator integrates User defined OSD and loads all functions required for output signal. AT7456E can receive NTSC or PAL composite video signal. Device package Includes Input Clamp, Sync Separator, Video Timing Generator, OSD Insertion Multiplexer device, non-volatile character memory, display memory, OSD generator, crystal oscillator Oscillator and SPI compatible interface to read/write OSD data and video driver etc. In addition, AT7456E also improves vertical synchronization (VSYNC), horizontal synchronization (HSYNC) and loss of synchronization (LOS) output signals for system synchronization. The clock output signal (CLKOUT) supports daisy-chaining of multiple devices. 512 user-defined 12×18 pixel character sets are preloaded and compatible with the input Multiplexes the incoming video streams to produce a CVBS signal with OSD video output. exist Up to 512 12×18 pixel characters can be reset in NVM. Made in NTSC In the formula, 13 lines × 30 characters are displayed. In PAL format, display 16 lines ×30 characters. When no video signal is input, use the AT7456E's internal Video timing generator, still can display OSD image.

video input

VIN of AT7456E can receive standard NTSC or PAL CVBS signal Number. The video signal input must be AC-coupled with a 0.1uF capacitor, and clamped internally. A 0.1uF input coupling capacitor is required to ensure the specified line time Distortion (LTD) and video clamp settling time. Video clamp settling time varies with input In-coupling capacitance changes proportionally, while LTD changes inversely proportional to capacitance.

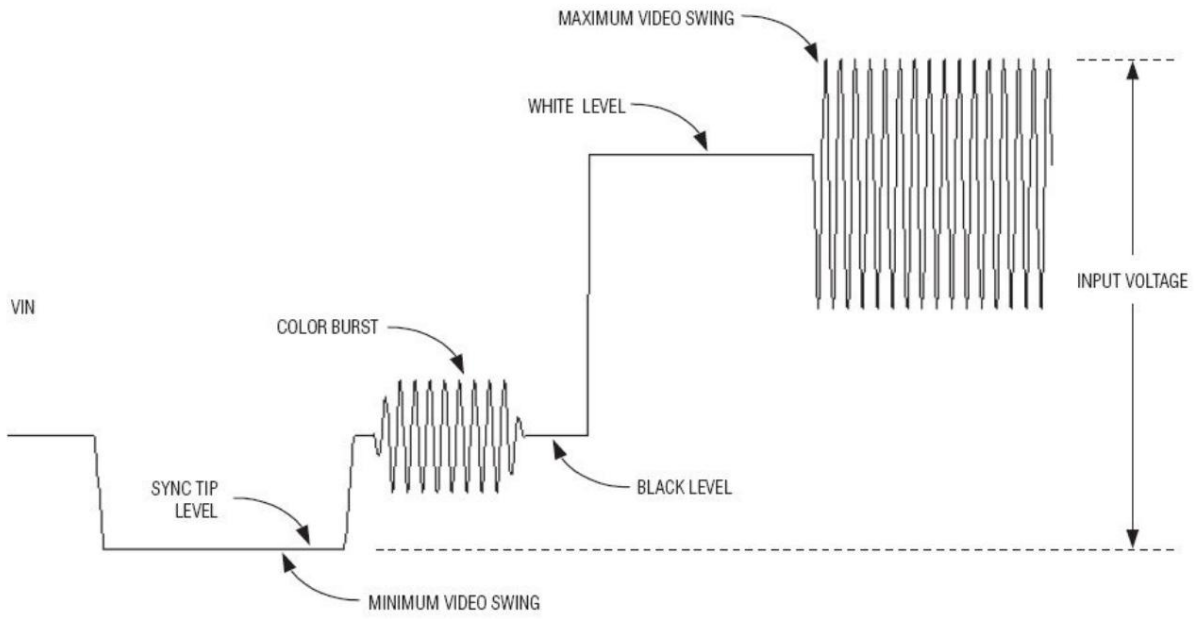


Figure 3. Terminology

Definition Input Clamp

The clamp of the AT7456E is a DC reconstruction circuit, on a line-by-line basis, using The input coupling capacitor corrects the DC offset of the input signal and clamps the synchronous head of VIN bit at approximately 560mV. The established DC level at VIN can be used for on-chip synchronization detection and video processing functions. This circuit also removes low frequency noise, such as 60Hz Buzz or other added low-frequency noise.

Sync Separator The

Sync Separator detects the composite sync pulses of the video input and extracts the timing information, generating *HSYNC and VSYNC signals; also used for internal* OSD synchronization and loss of synchronization (LOS) detection. If 32 consecutive line cycles on VIN No sync signal detected, LOS goes high, if 32 Continuous horizontal sync signal, it becomes low level. During LOS state, when VM0[5] = 0 (Video Mode 0 Register, bit 5), only OSD is present on VOUT. At this time, the input image at VOUT is set to the gray level determined by VM1[6:4]. Table 1 lists all synchronization modes.

Video Timing Generator

The video timing generator is a digital circuit that generates all internal and external (/HSYNC and /VSYNC) timing signals. /HSYNC and /VSYNC can be the same as VIN step, or run independently of the input in internal synchronous mode. Video Timing Generator Capable of generating NTSC or PAL timing using the same 27MHz crystal (see Refer to Figure 4 to Figure 9).

crystal oscillator

An internal crystal oscillator generates the system clock used by the video timing generator. The oscillator uses a 27MHz crystal, and can also be externally controlled by the CLKIN terminal 27MHz TTL clock driven. In external clock mode, connect to CLKIN A 27MHz TTL input clock, XFB terminal floating.

External synchronous composite signal selection By setting VM0[7]=1, you can select externally separated composite synchronous signal input.

表1. 视频同步模式

VIDEO MODE	VIN	$\overline{VSYNC}$	$\overline{HSYNC}$	LOS	VOUT
Auto Sync Select Mode VM0[5, 4] = 0x	Video	Active	Active	Low	V_{IN} + OSD
	No input	Active	Active	High	OSD only
External Sync Select VM0[5, 4] = 10	Video	Active	Active	Low	V_{IN} + OSD
	No input	Inactive (high)	Inactive (high)	High	DC
Internal Sync Select VM0[5, 4] = 11	Video	Active	Active	High	OSD only
	No input	Active	Active	High	OSD only

X = 无关。

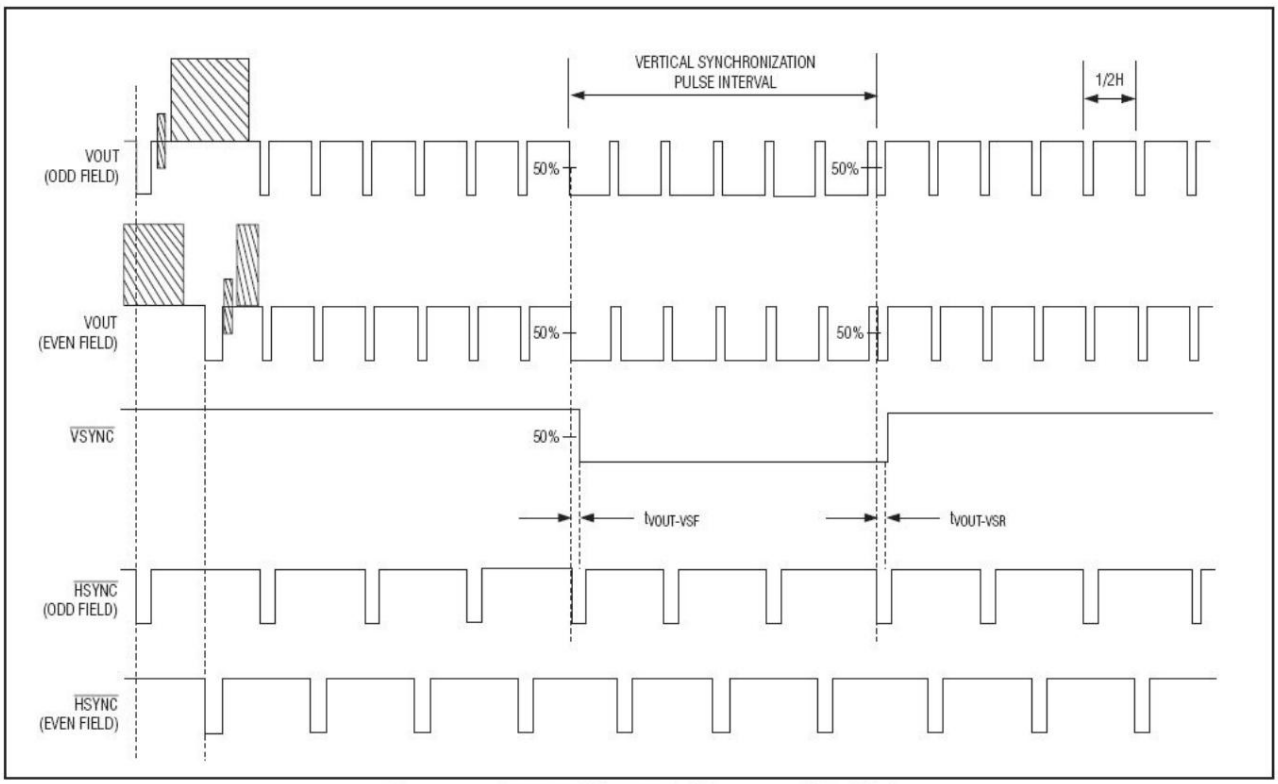


图4. VOUT、$\overline{VSYNC}$和$\overline{HSYNC}$时序(NTSC，外同步模式)

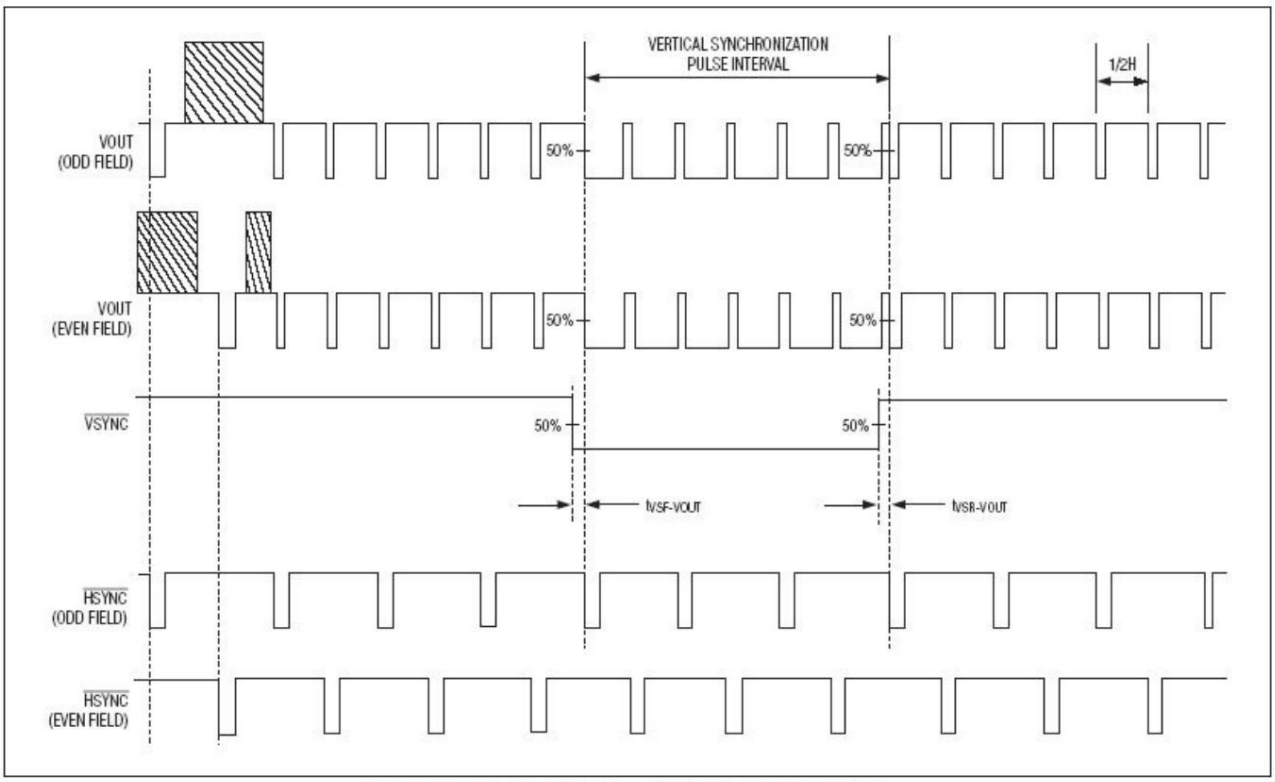


图5. VOUT、$\overline{VSYNC}$和$\overline{HSYNC}$时序(NTSC，内同步模式)

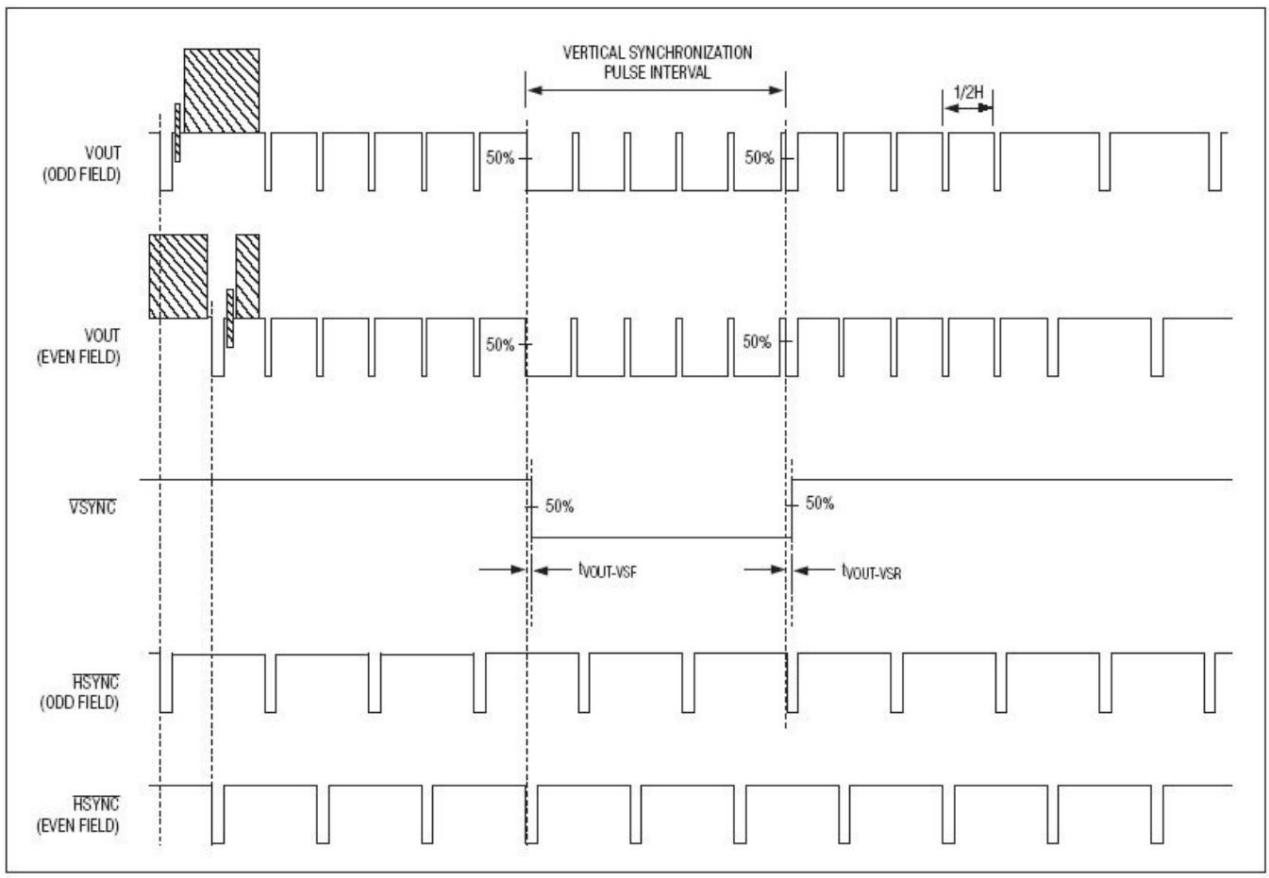


图6. VOUT、$\overline{VSYNC}$和$\overline{HSYNC}$时序(PAL，外同步模式)

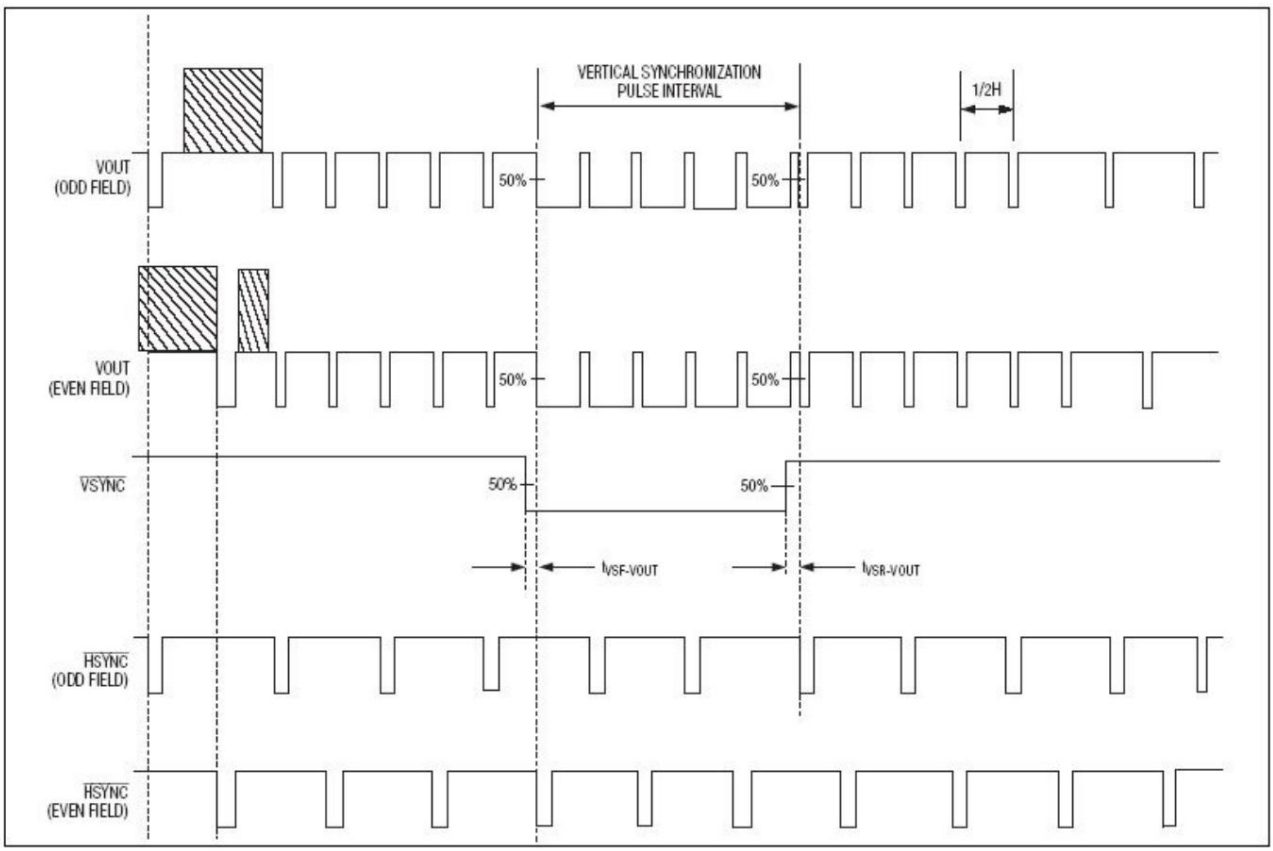


图7. VOUT、$\overline{VSYNC}$和$\overline{HSYNC}$时序(PAL，内同步模式)

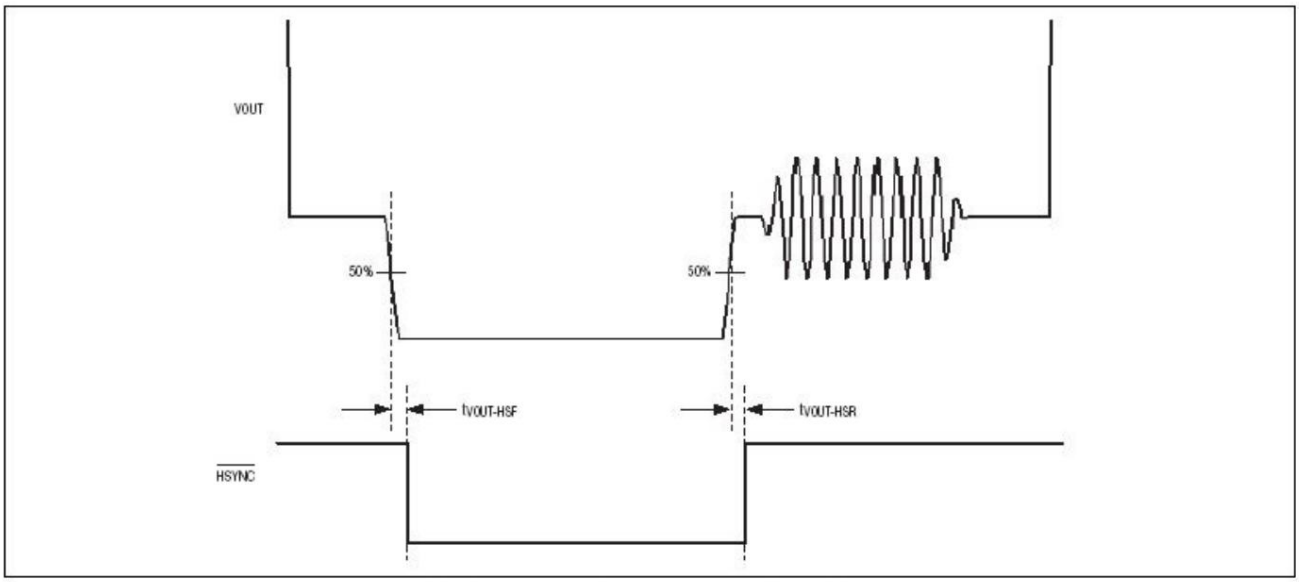


图8. VOUT和$\overline{HSYNC}$行同步时序(NTSC和PAL，外同步模式)

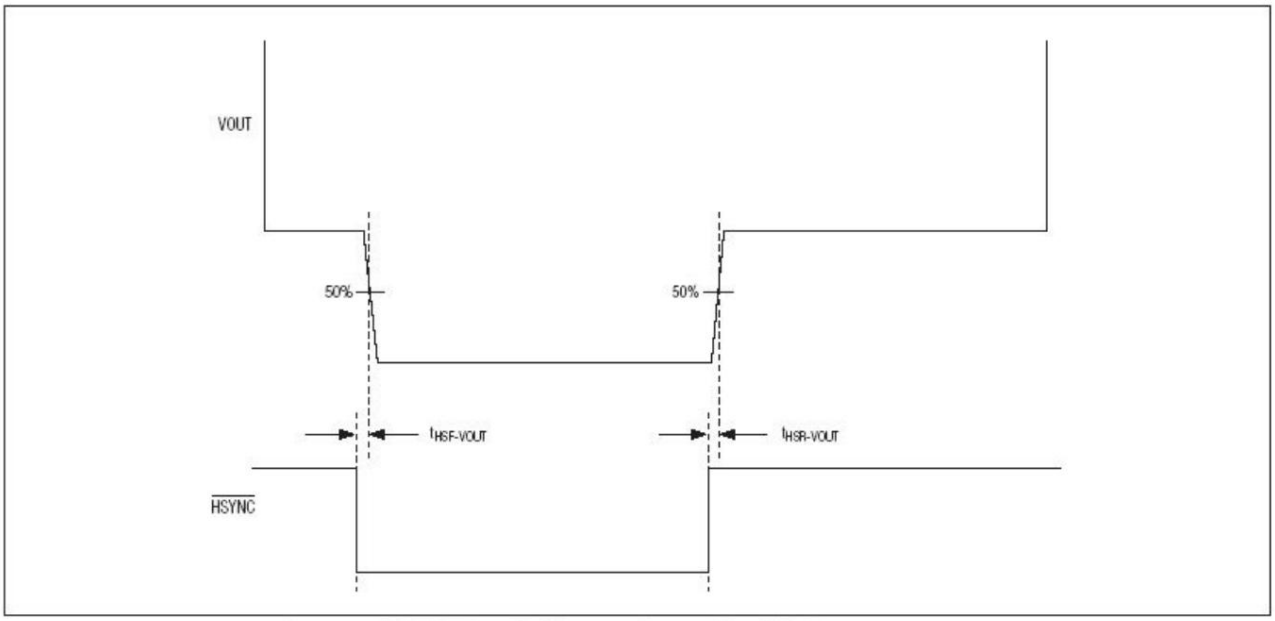


图9. VOUT和HSYNC行同步时序(NTSC和PAL，内同步模式)

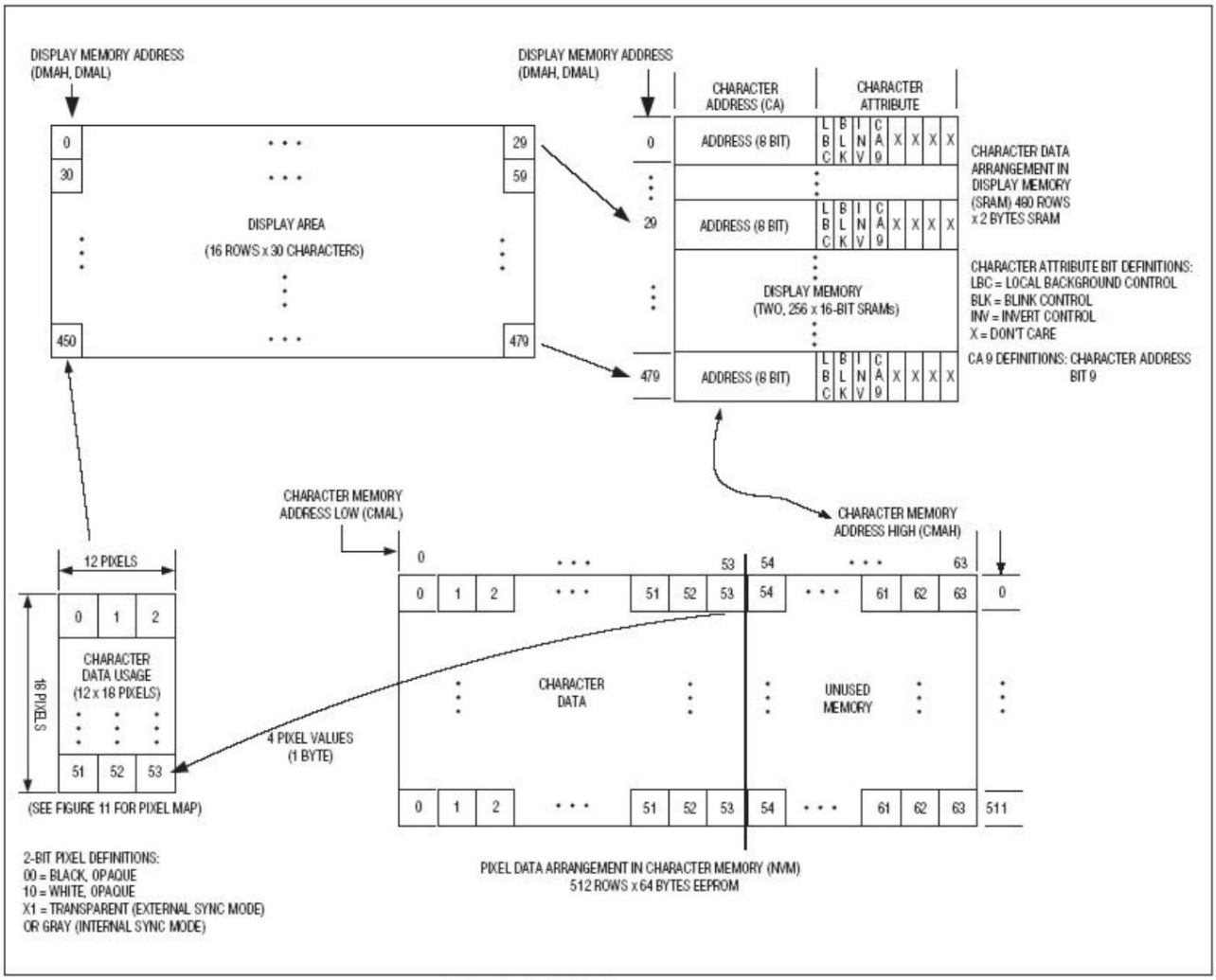


图10. 各种参数定义

Display memory (SRAM)

The display memory stores 480 character addresses that point to the Characters of NVM character memory. Users can set through SPI compatible serial port Displays the contents of memory. The display memory address corresponds to the fixed ground of the monitor address (refer to Figure 10). On-field blanking device writes to display memory, which prevents OSD Momentary dimming of the image. /VSYNC can be used as host processor interrupt, start Write display memory operation to achieve the above functions.

Character memory

Character memory is 480 rows x 64 bytes wide non-volatile memory (NVM) and 32 rows × 64 bytes wide volatile memory (SRAM), storing characters or or graphics, the characters shown in Figure 12 are preloaded at the factory. Users can use SPI Compatible with the serial port to set the contents of the character memory. Each row contains an OSD A description of the character. Each character consists of 12 rows × 18 columns of pixels, each A pixel is represented by 2-bit data with three states: white, black or transparent. Therefore, each character requires 54 bytes of pixel data (Fig. 11ÿÿ

NVM needs to read and write all characters (64 bytes) at once, through what is called mirroring Memory implementation of RAM. 64 bytes of temporary mirror RAM containing selected words All pixel data of symbols (CMAH[7:0]) are used as a buffer for NVM read and write operations (Figure 13). NVM is always accessed through mirrored RAM, so two operation steps. When writing characters to NVM, the user first utilizes 54 8 Bit SPI write operation writes to mirror RAM, then executes a mirror RAM write command Order, similarly, when reading the pixel of a character, the pixel data of the character is first Read into the mirror RAM, and then read the required pixel data from the mirror RAM to the SPI port.

On-Screen Display (OSD) Generator

The OSD generator is based on the character memory and row brightness registers (RB0-RB15) content, sets the brightness of each pixel.

OSD Insertion Multiplexer

The OSD insertion multiplexer selects between the OSD pixels and the input video signal select. OSD image sharpness is inserted by the OSD into the multiplexer (OSDM) register OSD rise and fall time bits and OSD insertion mux switch time bits for control. This register controls the OSD image sharpness and color crosstalk/brightness crosstalk balance between. Decreasing the time setting sharpens pixels, but may increase color crosstalk/luminance crosstalk. The optimal setting depends on the requirements of the actual application, thus, it can be Set by user.

Video output driver

The AT7456E includes a video output driver with a gain of 2. drive maximum output The output swing is 2.4Vp-p, and the signal bandwidth is up to 6MHz (attenuation is less than or equal to 0.2dB). The driver outputs can drive two 150ÿ standard video loads.

voltage decay correction

Circuit requirements and material for output coupling capacitors can be reduced by voltage rolloff manage size and reduce linear time distortion to an acceptable level. Voltage Decay Correction for Composed of Coaxial Cable and Output Coupling Capacitors with Back-Matched Resistors to 150ÿ High pass filter for low frequency compensation. The cutoff point of this circuit must be low enough to Can pass the field synchronization interval (PAL less than 25Hz, NTSC less than 30Hz), to Avoid field tilt. Traditionally, the cutoff point is less than 5Hz, and the coupling capacitor must be very Large, typically greater than 330uF. The AT7456E reduces this capacitor value and uses two A smaller capacitor (COUT and CSAG) is replaced, effectively reducing the coupling capacitance Cost and volume, while obtaining acceptable line-time distortion (Table 2). if Not used, connect SAG to VOUT.

Table **2. SAG** Corrected Capacitor Values

COUT(ÿF)	**CSAG(ÿF)**	**LINE-TIME DISTORTION (% typ)**
470	-	0.2
100	-	0.4
100	22	0.3
47	47	0.3
22	22	0.4
10	10	0.6

serial interface

SPI compatible serial port to set working mode and OSD data. Read function supports write verification and read status (STAT), display memory data output (DMDO) and word Symbol Memory Output (CMDO) register.

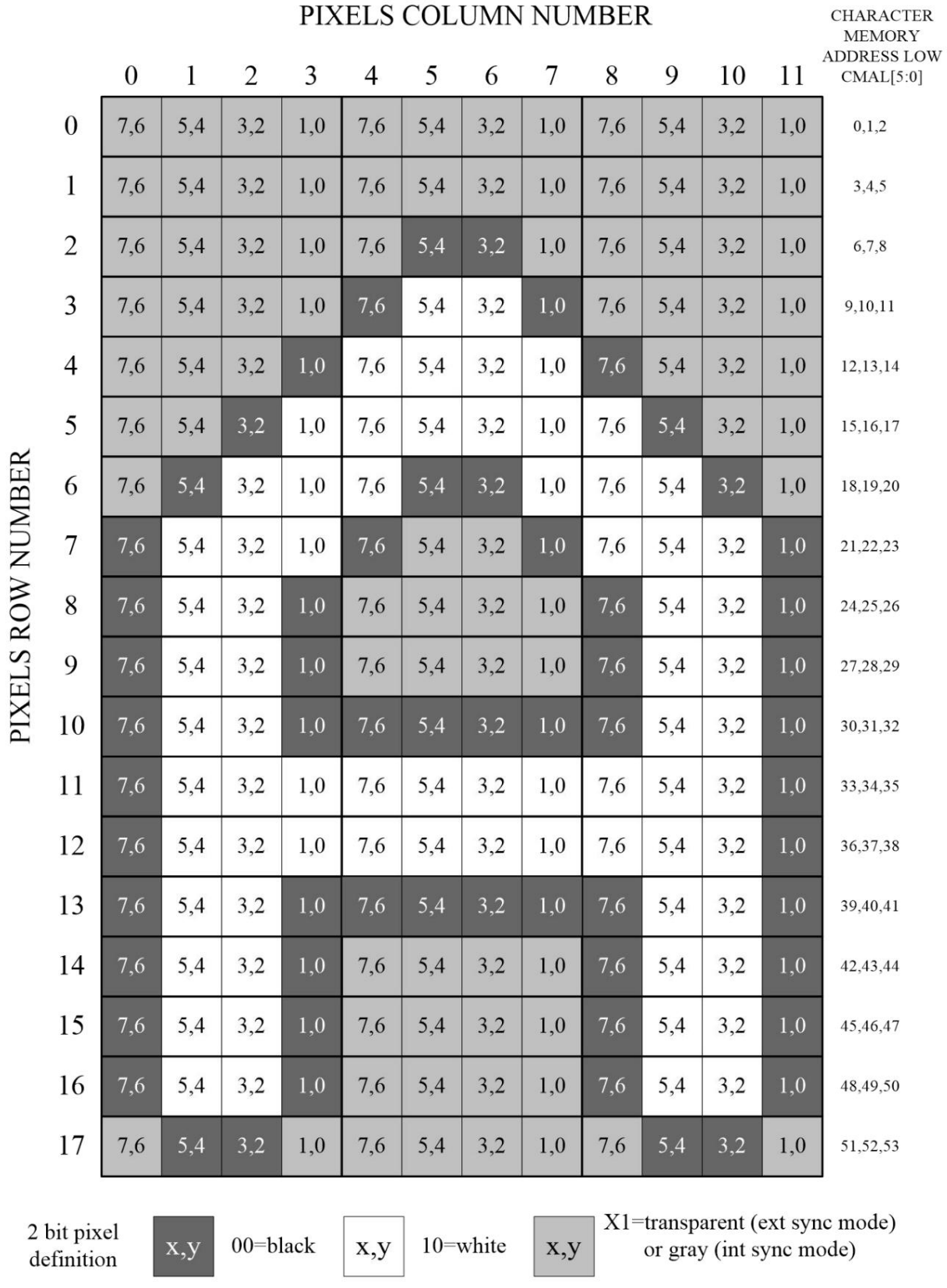
read and write operations

AT7456E supports interface clock (SCLK) up to 10MHz. As shown in Figure 15 Data writing, Figure 16 is reading data from AT7456E. Pulling *CS* low enables the string mouth. Data is clocked into SDIN on the rising edge of SCLK. When *CS* goes high, the Data is latched into the input register. If *CS* goes high in the middle of a transfer Ping, the operation failed (that is, the data was not written into the register). CS After going low, the device waits for the first byte input on SDIN to Determines the type of data transfer performed.

The SPI command is 16 bits long, the upper 8 bits (MSB) represent the register address, and the lower 8 bits The bits (LSB) represent the data (Figure 15 and Figure 16). There are two exceptions to this configuration Condition:

1) Displays the auto-increment write modulus used for memory or character memory accesses formula is an 8-bit operation (Figure 21). When performing a display memory auto-increment write In operation, 8-bit address is generated internally, and the serial port only needs 8-bit data.

2) When 16 is the working mode, the character data read from the display memory is 24 Bit operation (8-bit address and 16-bit data), refer to Figure 20.



picture 11. Character Data Usage (Pixel Mapping)

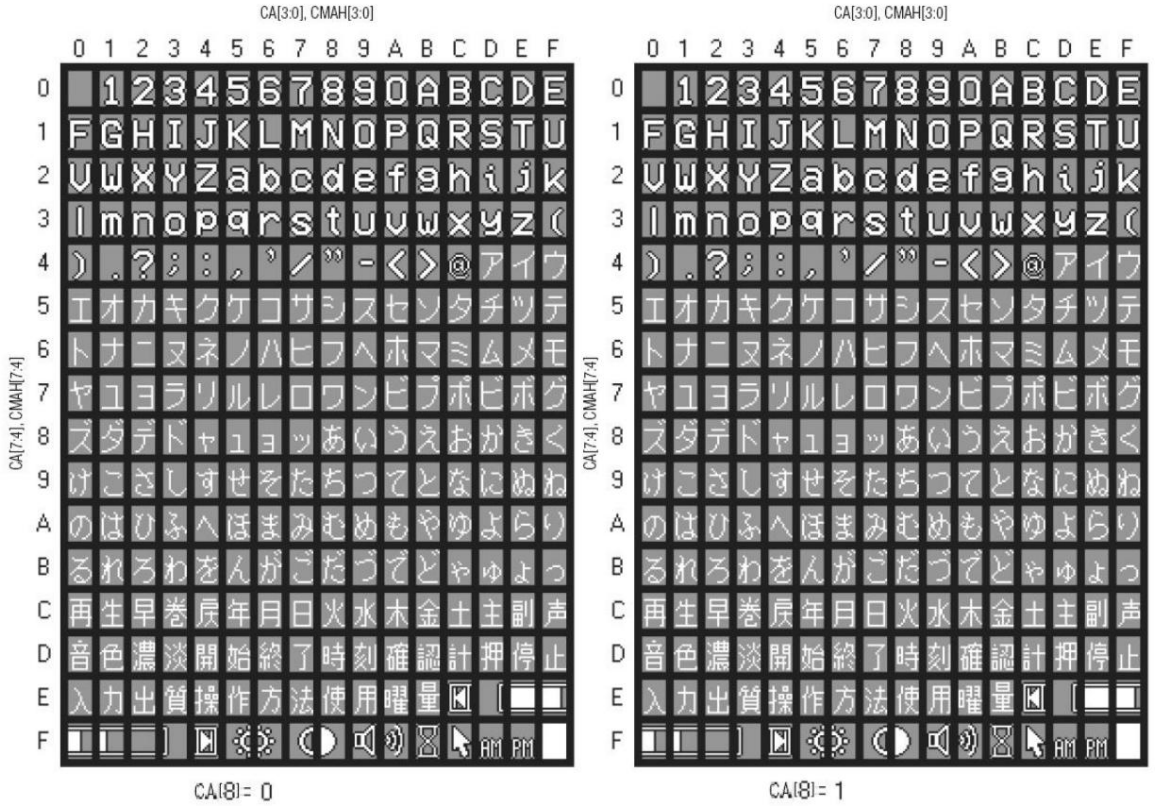
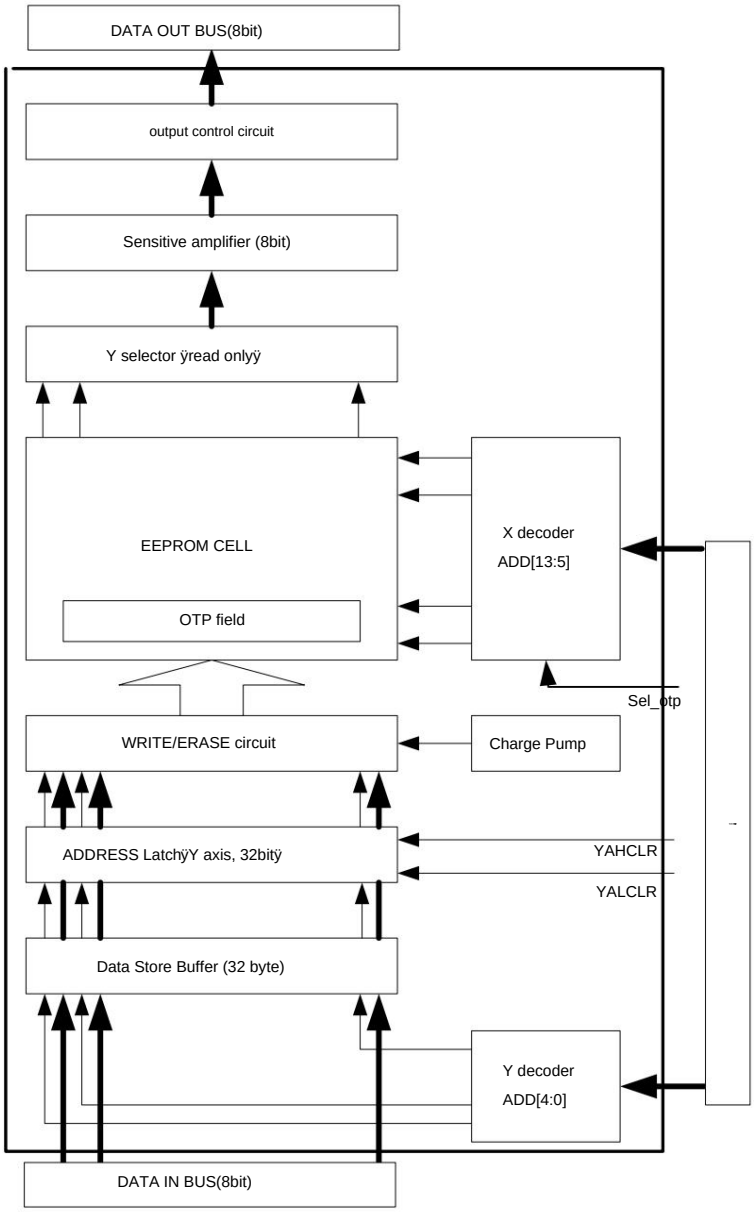


图12. 字符地址映射(默认字符集)



picture *13 EEPROM* structure diagram

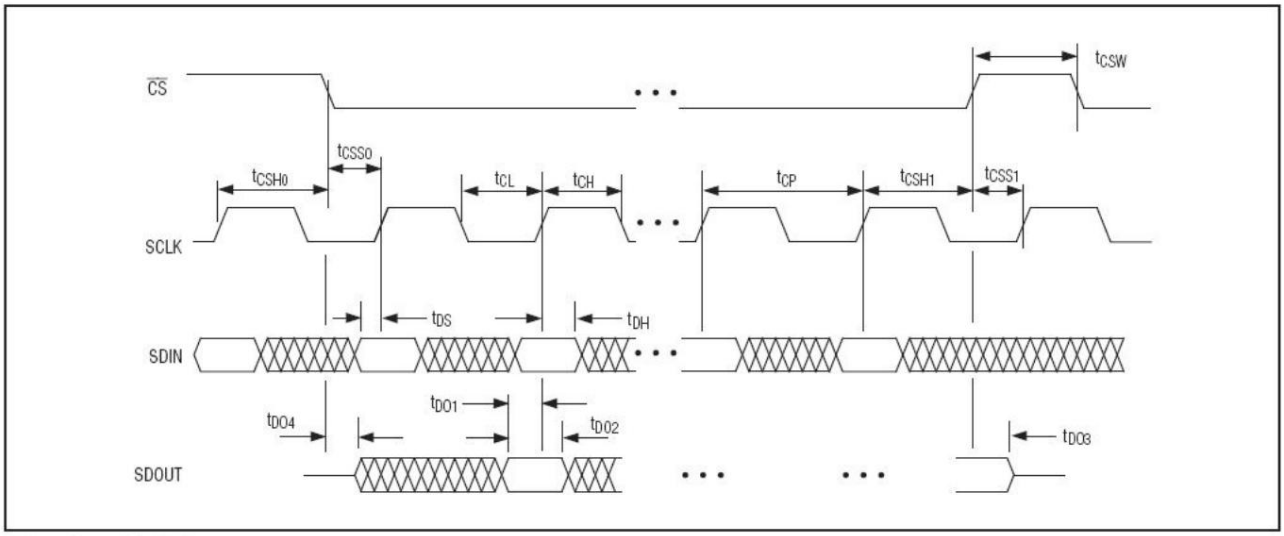


图14. 串口时序详述

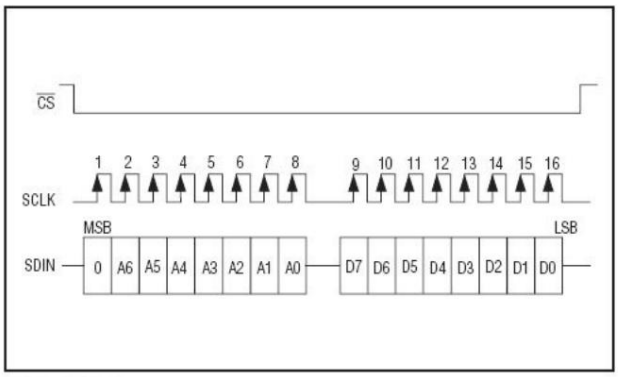


图15. 写操作

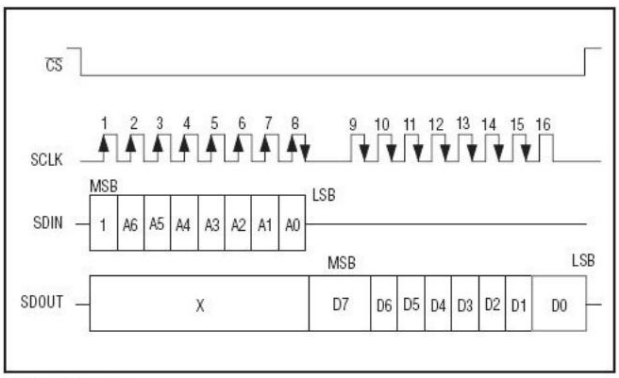


图16. 读操作

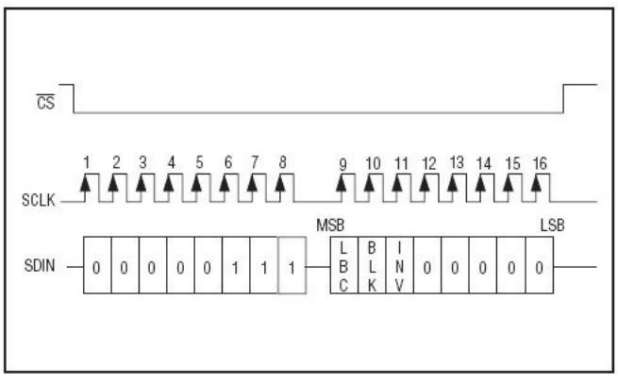


图17. 在8位工作模式下，写入字符属性字节

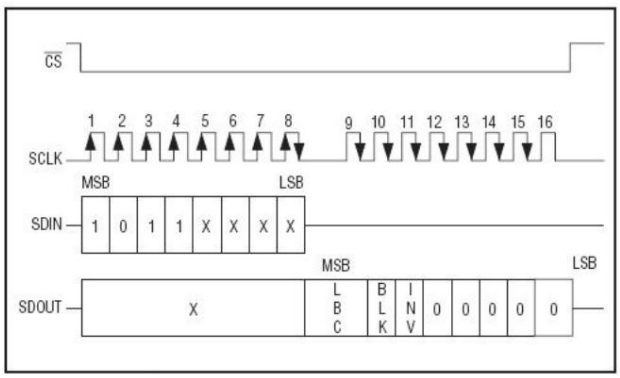


图18. 在8位工作模式下，读取字符属性字节

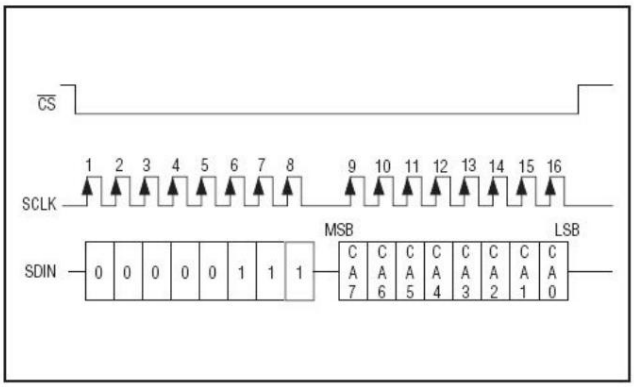


图19. 在8位和16位工作模式下，写入字符地址字节

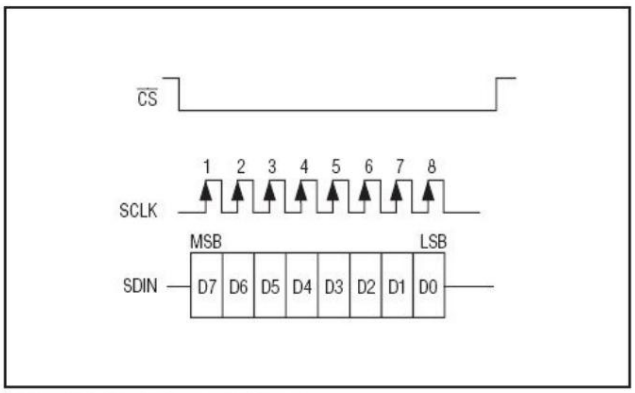


图21. 自动递增模式下的写操作

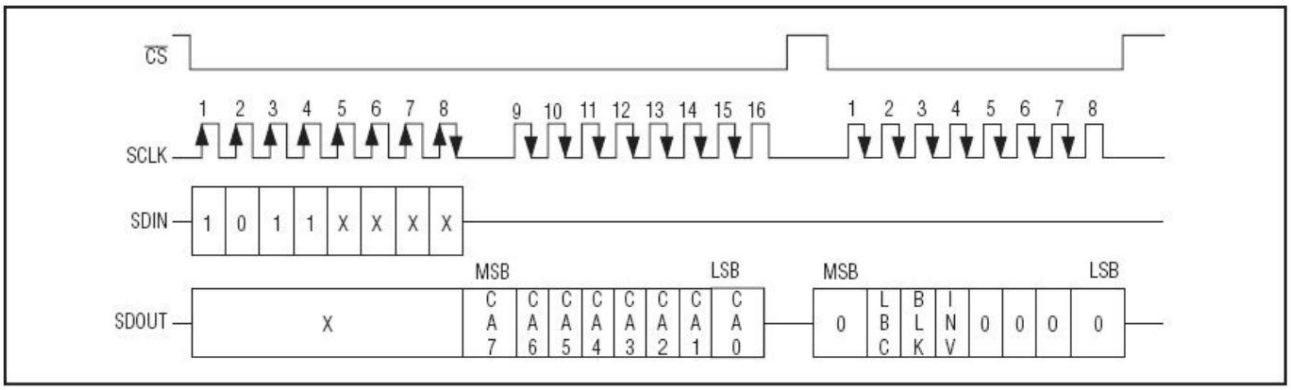


图20. 在16位工作模式下，读取字符地址和字符属性字节

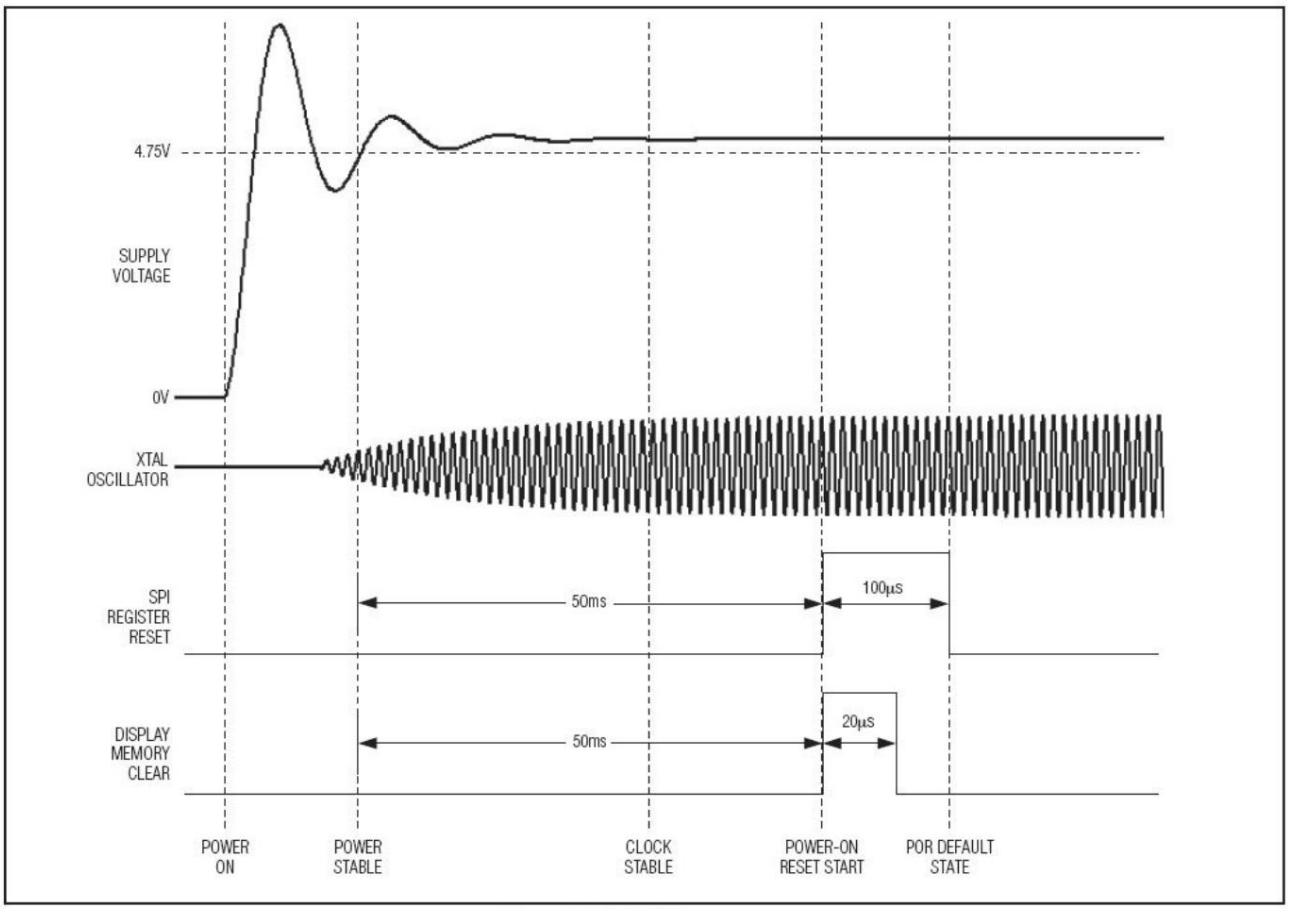


图22. 上电复位顺序

power on reset

The power-on reset circuit (POR) of AT7456E provides an internal reset signal,

Start working after the power supply voltage stabilizes. The user can put *RESET* on power-up

The signal is pulled high directly. An internal reset signal resets all registers to default values,

Clear display register. The power-on reset process takes 50ms, in order to avoid

Desired result, read/write operations are not allowed during this time. Generally in power supply

After the voltage is stable and the 27MHz clock signal is stable, the display register is reset.

The user should avoid SPI operation during this time to prevent undesired

fruit. The user needs to query STAT[5] to confirm that the reset sequence is complete (Fig.

22ÿÿ

software reset

AT7456E has a software reset bit (VM0[1]), when the bit is high, the display memory is cleared, except for

the OSD black level register (OSDBL),

All registers are reset to default values. After 100us (typical value), you can query

STAT[6] confirms whether the reset process is complete.

hardware reset

AT7456E provides a hardware reset input (RESET) for normal power-on

Performs a complete reset of the device during this period, and its function is the same as POR. When

RESET is driven to low level, keep it for more than 1us, and then pull it high, all registers

The register is reset to the default value, and all positions of the display register are reset to the default value

00H, the user can read/write the AT7456E registers after 50ms

write operation. When RESET is pulled high, you can query STAT[5] to confirm whether the reset

sequence is complete. RESET has higher priority than software reset bit.

AT7456E register description

All SPI registers are listed in Table 3 to access AT7456E operation, including A description of the SPI operation steps required for the memory. Registers used in this data sheet

Including display memory and character memory access, etc., cannot be directly accessed through the SPI port The format is REGISTER_NAME[BIT_NUMBERS]. For example, video mode

Accesses display and character memory. Please refer to the Application Information section for access to The first bit of the Formula 0 register is represented as VM0[1].

Table 3 Register Mapping

WRITE ADDRESS	READ ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	Note
00H	80H	VM0	Video Mode 0	ÿ
01H	81H	VM1	Video Mode 1	
02H	82H	WITH	Horizontal Offset	
03H	83h	YOUR	Vertical Offset	
04H	84H	DMM	Display Memory Mode	ÿ
05H	85H	DMAH	Display Memory Address High	ÿ
06H	86 H	DMAL	Display Memory Address Low	ÿ
07h	87h	DMDI	Display Memory Data In	ÿ
08H	88h	CMM	Character Memory Mode	ÿ
09H	89h	CMAH	Character Memory Address High	ÿ
0AH	8AH	CMAL	Character Memory Address Low	ÿ
0BH	8BH	CMDI	Character Memory Data In	ÿ
0CH	8CH	OSDM	OSD Insertion Mux	
10H	90h	RB0	Row 0 Brightness	
11H	91h	RB1	Row 1 Brightness	
12H	92h	RB2	Row 2 Brightness	
13H	93h	RB3	Row 3 Brightness	
14H	94H	RB4	Row 4 Brightness	
15H	95h	RB5	Row 5 Brightness	
16H	96h	RB6	Row 6 Brightness	
17H	97h	RB7	Row 7 Brightness	
18H	98h	RB8	Row 8 Brightness	
19H	99h	RB9	Row 9 Brightness	
1AH	9AH	RB10	Row 10 Brightness	
1BH	9BH	RB11	Row 11 Brightness	
1CH	9CH	RB12	Row 12 Brightness	
1DH	9DH	RB13	Row 13 Brightness	
1EH	9EH	RB14	Row 14 Brightness	
1FH	9FH	RB15	Row 15 Brightness	
6CH	EACH	OSDBL	OSD Black Level	
-	AX	STAT	Status	
-	BxH	DMDO	Display Memory Data Out	ÿ
-	Cx ONLY	CMDO	Character Memory Data Out	ÿ

X = don't care

ÿNote 1ÿOnly when STAT[5]=0 and DMM[2]=0 can it be written and read without restriction.

ÿNote 2ÿOnly when DMM[2]=0, it can be written, and read is not limited.

ÿNote 3ÿThe character display needs to be turned off first (VM0[3]=0), and then it can be written after STAT[5]=0, and the read is not restricted.

Video Mode Register (VM0)

Write address = 00H, read address = 80H.

Read/write access: unlimited.

When writing this register, the following conditions must

be met: 1) STAT[5]=0, the character register (NVM) is not busy.

2) DMM[2]=0, the display memory (SRAM) is not being cleared.

BIT	DEFAULT	FUNCTION
7	0	Composite Sync Source 0 = AT7456E sync splitter split 1 = external input
6	0	Video Standard Select 0 = NTSC 1 = PAL
5, 4	00	Sync Select Mode (Table 1) 0x = Autosync select (external sync when LOS = 0 and internal sync when LOS = 1) 10 = External 11 = Internal
3	0	Enable Display of OSD Image 0 = Off 1 = On
2	0	Vertical Synchronization of On-Screen Data 0 = Enable on-screen display immediately 1 = Enable on-screen display at the next VSYNC
1	0	Software Reset Bit When this bit is set, all registers are set to their default values and the display memory is cleared. The user does not need to write a 0 afterwards. SPI operations should not be performed during this time or unpredictable results may occur. This register is not accessible for writing until the display memory clear operation is finished (typically40us).
0	0	Video Buffer Enable 0 = Enable 1 = Disable (VOUT is high impedance)

X = don't care

Video Mode Register (VM1)

Write address = 01H, read address = 81H.

Read/write access: unlimited.

BIT	DEFAULT	FUNCTION
7	0	Background Mode (See Table 4) 0 = The Local Background Control bit (see DMM[5] and DMDI[7]) sets the state of each character background. 1 = Sets all displayed background pixels to gray. The gray level is specified by bits VM1[6:4] below. This bit overrides the local background control bit. **Note:In** internal sync mode, the background mode bit is set to 1.
6, 5, 4	100	Background Mode Brightness (% of OSD White Level) 000 = 0% 001 = 7% 010 = 14% 011 = 21% 100 = 28% 101 = 35% 110 = 42% 111 = 49%
3, 2	01	Blinking Time (BT) 00 = 2 fields (33ms in NTSC mode, 40ms in PAL mode) 01 = 4 fields (67ms in NTSC mode, 80ms in PAL mode) 10 = 6 fields (100ms in NTSC mode, 120ms in PAL mode) 11 = 8 fields (133ms in NTSC mode, 160ms in PAL mode)
1, 0	11	Blinking Duty Cycle (On : Off) 00 = BT : BT 01 = BT : (2 x BT) 10 = BT : (3 x BT) 11 = (3 x BT) : BT

Horizontal Position Register (HOS)

Write address = 02H, read address = 82H.

Read/write access: unlimited (Fig. 23).

BIT	DEFAULT	FUNCTION
7, 6	00	Don't Care
5–0	10 0000	Horizontal Position Offset (OSD video is not inserted into the horizontal blanking interval) 00 0000 = Farthest left (-32 pixels) * * 10 0000 = No horizontal offset * * 11 1111 = Farthest right (+31 pixels)

Vertical Position Register (VOS)

Write address = 03H, read address = 83H.

Read/write access: unlimited (Fig. 23).

BIT	DEFAULT	FUNCTION
7, 6, 5	000	Don't Care
4–0	1 0000	Vertical Position Offset (OSD video can be vertically shifted into the vertical blanking lines) 0 0000 = Farthest up (+16 pixels) * 1 0000 = No vertical offset * 1 1111 = Farthest down (-15 pixels)

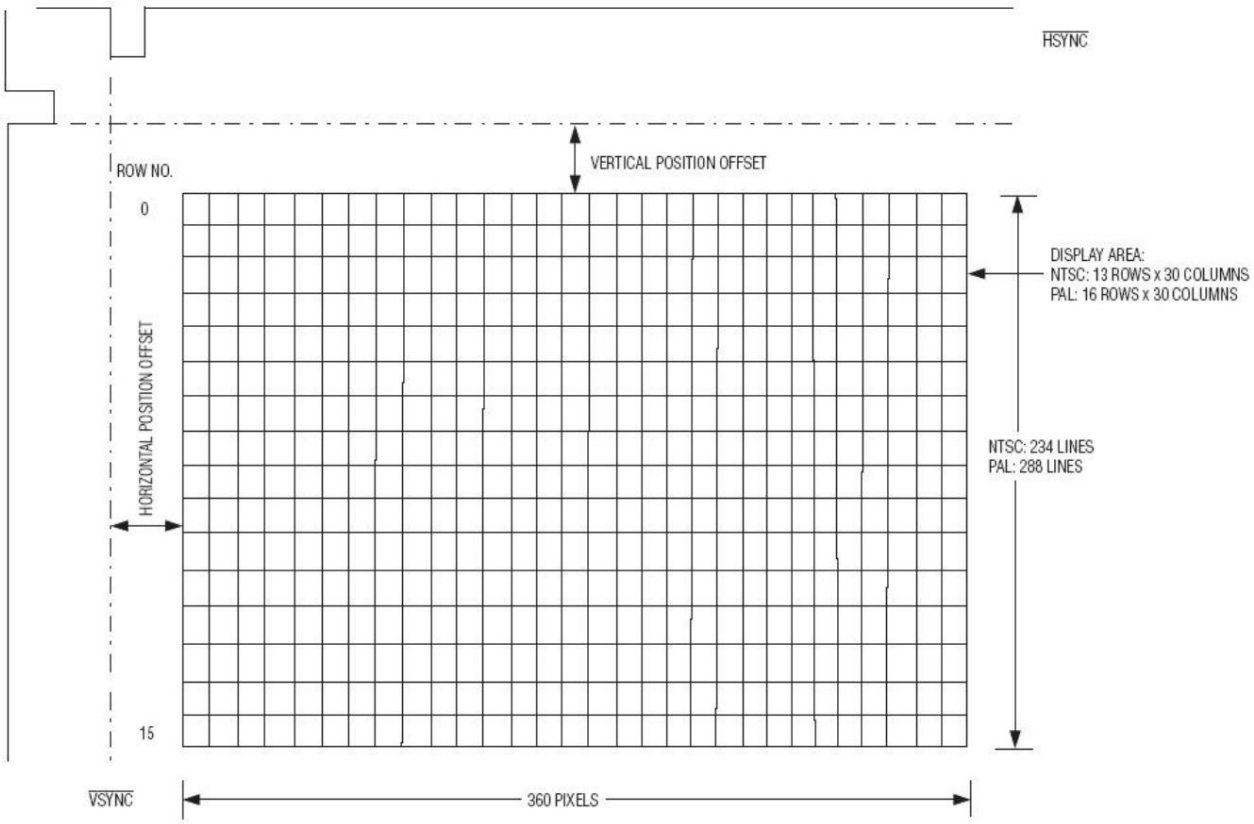


Figure 23. Character display area

Display Memory Mode Register (DMM)

Write address = 04H, read address = 84H.

Read/write access: unlimited.

When writing to this register, the following conditions must be met: DMM[2]=0, indicating that the memory is not being cleared.

BIT	DEFAULT	FUNCTION
7	0	Character memory auto-increment mode It is used to speed up character writing (mainly for SRAM to store characters). Similar to the auto-increment mode of the display memory, setting the auto-increment mode After the formula, the current CMAH[7:0] and CMAL[6] (corresponding to CMAH[8]) will be used as the selection address of 512 characters. Subsequent continuous writing through the SPI interface 54 groups of 8-bit data correspond to the character content to be written, and the character pixel address is automatically incremented during this process. After completion, set the CMM register to write to the character memory, This bit is automatically cleared. 0 = disabled 1 = enable
6	0	Operation Mode Selection 0 = 16-bit operation mode The 16-bit operation mode increases the speed at which the display memory can be updated. When writing to the display memory, the attribute byte is not entered through the SPI-compatible interface. It is entered automatically by copying DMM[5:3] to a character's attribute byte when a new character is written, thus reducing the number of SPI write operations per character from two to one (Figure 19). When in this mode, all characters written to the display memory have the same attribute byte. This mode is useful because successive characters commonly have the same attribute. This mode is distinct from the 8-bit operation mode where a character attribute byte must be written each time a character address byte is written to the display memory (see Table 5). When reading data from the display memory, both the Character Address byte and Character Attribute byte are transferred with the SPI-compatible interface (Figure 18). 1 = 8-bit operation mode The 8-bit operation mode provides maximum flexibility when writing characters to the display memory. This mode enables writing individual Character Attribute bytes for each character (see Table 5). When writing to the display memory, DMAH[1] = 0 directs the data to the Character Address byte and DMAH[1] = 1 directs the Character Attributes byte to the data. This mode is distinct from the 16-bit operation mode where the attribute bits are automatically copied from DMM[5:3] when a character is written.
5	0	Local Background Control Bit, LBC (see Table 4) Applies to characters written in 16-bit operating mode. 0 = Sets the background pixels of the character to the video input (VIN) when in external sync mode. 1 = Sets the background pixels of the character to the background mode brightness level defined by VM1[6:4] in external or internal sync mode. **Note:In** internal sync mode, the local background control bit behaves as if it is set to 1.
4	0	Blink Bit, BLK Applies to characters written in 16-bit operating mode. 0 = Blinking off 1 = Blinking on **Note:** Blinking rate and blinking duty cycle data in the Video Mode 1 (VM1) register are used for blinking control. In external sync mode: when the character is not displayed, VIN is displayed. In internal sync mode: when the character is not displayed, background mode brightness is displayed (see VM1[6:4]).
3	0	Invert Bit, INV Applies to characters written in 16-bit operating mode (see Figure 24). 0 = Normal (white pixels display white, black pixels display black) 1 = Invert (white pixels display black, black pixels display white)

BIT	DEFAULT	FUNCTION
2	0	Clear Display Memory 0 = Inactive 1 = Clear (fill all display memories with zeros) **Note:This** bit is automatically cleared after the operation is completed (the operation requires 40ÿs). The user does not need to write a 0 afterwards. The status of the bit can be checked by reading this register. This operation is automatically performed: a) On power-up b) Immediately following the rising edge of RESET c) Immediately following the rising edge of CS after VM0[1] has been set to 1
1	0	Vertical Sync Clear Valid only when clear display memory = 1, (DMM[2] = 1) 0 = Immediately applies the clear display-memory command, DMM[2] = 1 1 = Applies the clear display-memory command, DMM[2] = 1, at the next VSYNC time
0	0	Auto-Increment Mode Auto-increment mode increases the speed at which the display memory can be written by automatically incrementing the character address for each successive character written. This mode reduces the number of SPI commands, and thus the time needed to write a string of adjacent characters. This mode is useful when writing strings of characters written from left-to-right, top-to-bottom, on the display (see Table 5). 0 = Disabled 1 = Enabled When this bit is enabled for the first time, data in the Display Memory Address (DMAH[0] and DMAL[7:0]) registers are used as the starting location to which the data is written. When performing the auto-increment write for the display memory, the 8-bit address is internally generated, and therefore only 8-bit data is required by the SPI-compatible interface (Figure 21). The content is to be interpreted as a Character Address byte if DMAH[1] = 0 or a Character Attribute byte if DMAH[1] = 1. This mode is disabled by writing the escape character 1111 1111. If the Clear Display Memory bit is set, this bit is reset internally.

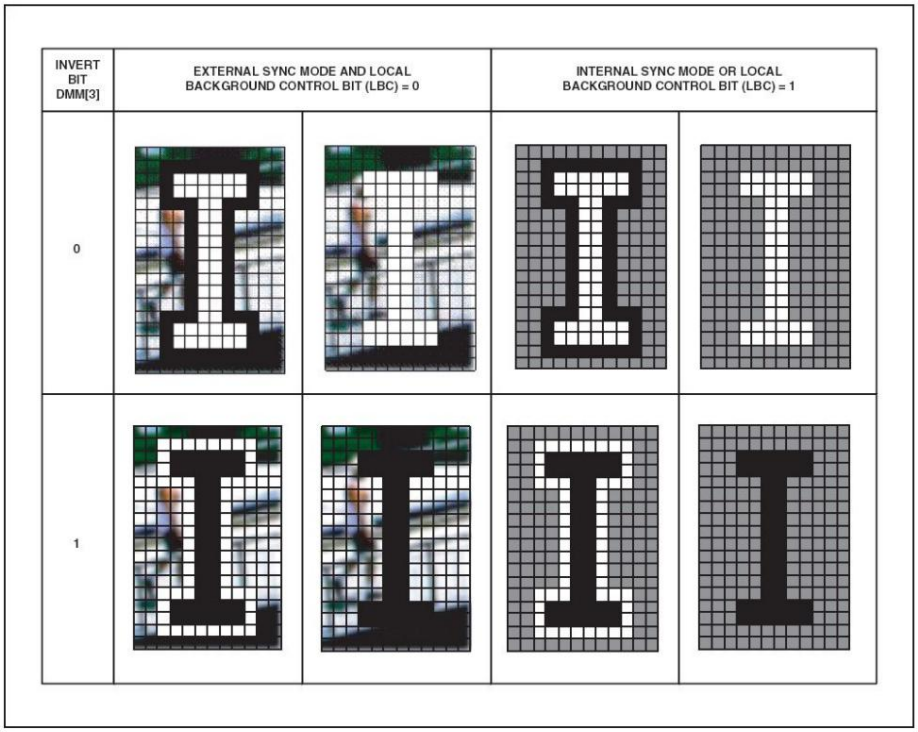


Figure 24. Example of Character Attribute Bits: Inverted Color and Local Background Control

Table **4.** Character Background Controls

SYNC MODE	BACKGROUND MODE, VM1[7]	LOCAL BACKGROUND CONTROL BIT, LBC DMM[5], DMDI[7]	CHARACTER BACKGROUND PIXEL
External	0	0	Input Video
	0	1	Gray
	1	X	Gray
Internal	X	X	Gray

X = don't care

Display Memory Address High Register (DMAH)

Write address = 05H, read address = 85H.

Read/write access: unlimited.

When writing to this register, the following conditions must be met: DMM[2]=0, indicating that the memory is not being cleared.

BIT	DEFAULT	FUNCTION
7–2	0000 00	Don't Care
1	0	Byte Selection Bit This bit is valid only when in the 8-bit operation mode (DMM[6] = 1). 0 = Character Address byte is written to or read (DMDI[7:0] contains the Character Address byte). 1 = Character Attribute byte is written to or read (DMDI[7:0] contains the Character Attribute byte).
0	0	Display Memory Address Bit 8 This bit is the MSB of the display-memory address. The display-memory address sets the location of a Caracter on the display (Figure10). The lower order 8 bits of the display-memory address is found in DMAL[7:0].

Display Memory Address Low Register (DMAL)

Write address = 06H, read address = 86H.

Read/write access: unlimited.

When writing to this register, the following conditions must be met: DMM[2]=0, indicating that the memory is not being cleared.

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Display Memory Address Bits 7–0 This byte is the lower 8 bits of the display-memory address. The display-memory address sets the location of a character on the display (Figure 10). The MSB of the display-memory address is DMAH[0].

Display Memory Data Input Register (DMDI)

Write address = 07H, read address = 87H.

Read/write access: unlimited.

When writing to this register, the following conditions must be met: DMM[2]=0, indicating that the memory is not being cleared.

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Character Address or Character Attribute byte to be stored in the display memory. 8-Bit Operation Mode (DMM[6] = 1) If DMAH[1] = 0, the content is to be interpreted as a Character Address byte, where Bits 7–0 = Character Address bits, CA[7:0] (Figure 12). If DMAH[1] = 1, the content is to be interpreted as a Character Attribute byte where Bit 7 = Local Background Control bit, LBC (Figure 24 and Table 4) Bit 6 = Blink bit, BLK Bit 5 = Invert bit, INV (see Figure 24) Bit 4 = Character Address bitsÿCA[8] Bit 3–0 = 0 (The LBC, BLK, and INV bits are described in the Display Memory Mode register.) 16-Bit Operation Mode (DMM[6] = 0) The content is always interpreted as a Character Address byte where bits 7–0 = CA[7:0] (Figure 12). Auto-Increment Mode (DMM[0] = 1) The character address CA[7:0] = FFH is reserved for use as an escape character that terminates the auto-increment mode. Therefore, the character located at address FFH is not available for writing to the display memory when in auto-increment mode. In all other modes, character FFH is available.

CHARACTER MEMORY MODE REGISTER (CMM)

Write address = 08H, read address = 88H.

Read/write access: unlimited.

When writing this register, the following conditions must

be met: 1) STAT[5]=0, the character register (NVM) is not busy.

2) VM0[3]=0, OSD is disabled.

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Only whole characters (54 bytes) can be written to or read from the nonvolatile character memory (NVM) at one time. This is done through the (64 byte) shadow RAM (Figure 13). The shadow RAM is accessed through the SPI port one byte at a time. The shadow RAM is written to and read from NVM by the following procedures: **Writing to NVM** 1010 XXXX = Write to NVM array from shadow RAM. The 64 bytes from shadow RAM are written to the NVM array at the character-memory address location (CMAH, CMAL) (Figure 13). The character memory is busy for approximately5ms during this operation. During this time, STAT[5] is automatically set to 1. The Character Memory Mode register is cleared and STAT[5] is reset to 0 after the write operation has been completed. The user does not need to write zeros afterwards. **Reading from NVM** 0101 XXXX = Read from NVM array into shadow RAM. The 64 bytes corresponding to the character-memory address (CMAH, CMAL) are read from the NVM array into the shadow RAM (Figure 13). The character memory is busy for approximately 30us during this operation. The CMM register is cleared after the operation is completed. The user does not need to write zeros afterwards. During this time, STAT[5] is automatically set to 1. STAT[5] is reset to 0 when the read operation has been complete. If the display has been enabled (VM0[3] = 1) or the character memory is busy (STAT[5] = 1), NVM read/write operation commands are ignored and the corresponding registers are not updated. However, all the registers can be read at any time. For all the character-memory operations, the character address is formed with Character Memory Address High (CMAH[7:0]) and Character Memory Address Low (CMAL[7:0]) register bits (Figures 11, 12, and 13).

X = don't care

CHARACTER MEMORY ADDRESS HIGH REGISTER (CMAH)

Write address = 09H, read address = 89H.

Read/write access: unlimited.

When writing to this register, the following conditions must be met:

1) STAT[5]=0, the character register (NVM) is not busy.

2) VM0[3]=0, OSD is disabled.

BIT	DEFAULT	FUNCTION
7–0	0000 0000	Character Memory Address Bits These 8 bits & CMAL[6]point to a character in the character memory (512 characters total in NVM) (Figures 10 and 12).

CHARACTER MEMORY ADDRESS LOW REGISTER (CMAL)

Write address=0AH, read address=8AH.

Read/write access: unlimited.

When writing this register, the following conditions must

be met: 1) STAT[5]=0, the character register (NVM) is not busy.

2) VM0[3]=0, OSD is disabled.

BIT	DEFAULT	FUNCTION
7,	0	Don't Care
6	0	Character Memory Address Bits Bit CA9: used as CA[8] This bit & CMAH point to a character in the character memory (512 characters total in NVM) (Figures 10 and 12).
5–0	00 0000	Character Memory Address Bits These 6 bits point to one of the 64 bytes (only 54 used) that represent a 4-pixel group in the character (Figures 10 and 11).

CHARACTER MEMORY DATA IN REGISTER (CMDI)

Write address = 0BH, read address = 8BH.

Read/write access: unlimited.

When writing to this register, the following conditions must be met:

1) STAT[5]=0, the character register (NVM) is not busy.

2) VM0[3]=0, OSD is disabled.

BIT	DEFAULT	FUNCTION
7, 6	THAT	Leftmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
5, 4	THAT	Left center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
3, 2	THAT	Right center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
1, 0	THAT	Rightmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)

NA=not applicable

OSD insertion multiplexing register (OSDM)

Write address = 0CH, read address = 8CH.

Read/write access: unlimited.

BIT	DEFAULT	FUNCTION
7, 6	00	Don't Care
5, 4, 3	011	OSD Rise and Fall Time—typical transition times between adjacent OSD pixels 000: 20ns (maximum sharpness/maximum cross color artifacts) 001: 30ns 010: 35ns 011: 60ns 100: 80 ns 101: 110ns (minimum sharpness/minimum cross color artifacts)
2, 1, 0	011	OSD Insertion Mux Switching Time–typical transition times between input video and OSD pixels 000: 30ns (maximum sharpness/maximum cross color artifacts) 001: 35ns 010: 50ns 011: 75ns 100: 100ns 101: 120ns (minimum sharpness/minimum cross color artifacts)

Row N Brightness Registers (RB0-RB15)

Address = 10H + row number, write address = 10H to 1FH, read address = 90H to 9FH.

Read/write access: unlimited.

The first line has a line number of 0, and the best line has a line number of 13 in NTSC and 15 in PAL (refer to Figure 23).

BIT	DEFAULT	FUNCTION
7–4	0000	Don't Care
3, 2	00	Character Black Level —All the characters in row N use these brightness levels for the black pixel, in % of OSD white level. 00 = 0% 01 = 10% 10 = 20% 11 = 30%
1, 0	01	Character White Level —All the characters in row N use these brightness levels for the white pixel, in % of OSD white level. 00 = 120% 01 = 100% 10 = 90% 11 = 80%

OSD Black Level Register (OSDBL)

Write address = 6CH, read address = ECH.

Read/Write Access: This register contains 4 factory preset bits [3:0], which cannot be modified. Therefore, when modifying the 4th bit, read this register first, modify the 4th bit 4 bits, and then write back the updated bytes.

BIT	DEFAULT	FUNCTION
7–5	000	Don't Care
4	1	OSD Image Black Level Control This bit enables the alignment of the OSD image black level with the input image black level at VOUT. Always enable this bit following power-on reset to ensure the correct OSD image brightness. 0 = Enable automatic OSD black level control 1 = Disable automatic OSD black level control
0–3	xxxx	These bits are factory preset. To ensure proper operation of the AT7456E, do not change the values of these bits.

Xxxx = factory default - may be any one of 16 values. This value is permanently stored in the AT7456E and is always restored to the factory default value after power-on reset or hardware reset.

Status Register (STAT)

Read address = AxH.

Read/Write Access: Read Only.

BIT	DEFAULT	FUNCTION
7	THAT	Don't Care
6	THAT	Reset Mode 0 = Clear w hen power- up reset mode is comp lete. Occurs 50ms (typ) following stable VD D (F.22) 1 = S et when in power- up r eset m ode
5	THAT	Character Memory Status 0 = Available to be written to or read from 1 = Unavailable to be written to or read from
4	THAT	$\overline{\text{VSYNC}}$Output Level 0 = Active during vertical sync time 1 = Inactive otherwise
3	THAT	$\overline{\text{HSYNC}}$Output Level 0 = Active during horizontal sync time 1 = Inactive otherwise
2	THAT	Loss-of-Sync (LOS) 0 = Sync Active. Asserted after 32 consecutive input video lines. 1 = No Sync. Asserted after 32 consecutive missing input video lines.
1	THAT	0 = NTSC signal is not detected at VIN 1 = NTSC signal is detected at VIN
0	THAT	0 = PAL signal is not detected at VIN 1 = PAL signal is detected at VIN

NA = not applicable.

X = don't care.

Display Memory Data Output Register (DMDO)

Read address = BxH.

Read/Write Access: Read Only.

When writing to this register, the following conditions must be met: DMM[2]=0, indicating that the memory is not being cleared.

BIT	DEFAULT	FUNCTION
7–0	THAT	Character Address or Character Attribute byte to be read from the display memory. 8-Bit Operation Mode (DMM[6] = 1): If DMAH[1] = 0, the content is to be interpreted as a Character Address byte, where Bits 7–0 = Character Address bits, CA[7:0] (Figure 12) If DMAH[1] = 1, the content is to be interpreted as a Character Attribute byte where Bit 7 = Local Background Control bit, LBC (see Figure 24 and Table 4) Bit 6 = Blink bit, BLK Bit 5 = Invert bit, INV (see Figure 24) Bit 4 = Character Address bitsÿCA[8] Bit 3–0 = 0 The LBC, BLK, and INV bits are described in the Display Memory Mode register. 16-Bit Operation Mode (DMM[6] = 0): The content is to be interpreted as a Character Address byte, where Bits 7–0 = CA[7:0] (see Figure 12) followed by a Character Attribute byte, where Bit 7 = 0 Bit 6 = Local Background Control bit, LBC (see Figure 24 and Table 4) Bit 5 = Blink bit, BLK Bit 4 = Invert bit, INV (see Figure 24) Bit 3 = Character Address bitsÿCA[8] Bit 2–0 = 0 The LBC, BLK, and INV bits are described in the Display Memory Mode register.

NA = not applicable.

X = don't care.

Character Memory Data Output Register (CMDO)

Read address = CxH.

Read/Write Access: Read Only.

When writing to this register, the following conditions must be met:

1) STAT[5]=0, the character register (NVM) is not busy.

2) VM0[3]=0, OSD is disabled.

BIT	DEFAULT	FUNCTION
7, 6	THAT	Leftmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
5, 4	THAT	Left center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
3, 2	THAT	Right center pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)
1, 0	THAT	Rightmost pixel. 00 = Black, 10 = White, 01 or 11 = Transparent (see Figure 11)

NA = not applicable.

X = don't care.

application information

Character memory operation

Only whole characters (54

bytes of pixel data). This can be done with (64 bytes) mirrored RAM

now (refer to Figure 13). Through the SPI port, each access to the mirrored RAM

one byte. Write or read image from NVM with one SPI command

RAMÿ

Steps to Write Character Bytes to **NVM** Character Memory

Write a new character: 1)

Write VM0[3]=0, disable OSD image display, delay **30us** to do subsequent operations. 2) Write

CMAH[7:0]ÿxxH,

select the character to be written (0-255)

(Figure 10 and Figure 13).

3) Write CMAL[7:0]=xxH to select 4 pixel bytes (0-63) in the character to be written (Figure 10

and Figure 13). CMAL[6] acts as CA[8] to select the character block (0-255) (256-511)

to be written.

4) Write CMDI[7:0]ÿxxH to set the pixel value of the selected part of the character (Fig.

11 and Figure 13).

5) Repeat steps 3 and 4, keeping the value of CMAL[6] consistent until all 54 bytes of character

data are loaded into mirror RAM.

6) Write CMM[7:0] = 1010xxxx from mirrored RAM to NVM array (Figure 13). During this

operation, when the character memory is busy

The interval is about 5ms. It can be confirmed whether the NVM write process is

completed by reading the status of STAT[5].

Write VM0[3]=1 to enable OSD image display. Write a new

character in auto-increment mode: 1) Write

VM0[3]ÿ0, disable OSD image display, delay **30us**

Do follow-up operations.

2) Write CMAH[7:0]=xxH, CMAL[6]=xH to select the character (0-511) to be written (Figure 10

and Figure 13).

3) Write DMM[7]=1 to set the auto-increment mode. 4) Write data in

character pixel order, which is a single-byte operation. automatic delivery

In increasing mode, the address of CMDI[7:0] is set automatically. After a write

operation, the character memory address is automatically incremented until all 54

Bytes are loaded into mirrored RAM.

5) Write CMM[7:0] = 1010xxxx from mirrored RAM to NVM array (Figure 13). During this

operation, when the character memory is busy

The interval is about 5ms. It can be confirmed whether the NVM write process is

completed by reading the status of

STAT[5]. 6) Write VM0[3]=1 to enable OSD image display. Modify

existing characters: 1)

Write VM0[3]ÿ0, disable OSD image display, delay **30us**

Do follow-up operations.

2) Write CMAH[7:0]ÿxxH, select the character (0-255) to be modified (Figure 10 and Figure

13).

3) Write CMM[7:0]ÿ0101xxxx, and read character data from NVM into mirror RAM (Figure 13) .

pay attention.

4) Write CMAL[7:0]=xxH to select 4 pixel bytes (0-63) in the character to be modified (Figure 10

and Figure 13). CMAL[6] acts as CA[8] to select the character block (0-255) (256-511)

to be written.

5) Read CMDO[7:0]ÿxxH, read 4 pixel data words to be modified

section (Figure 11 and Figure 13).

6) Modify the 4-pixel byte as required. 7) Write

CMDI[7:0]=xxH to write the modified 4 pixel data bytes back to the mirror RAM (Figure 11 and

Figure 13). 8) Repeat steps 4 to 7 as needed, during

which the value of CMAL[6] should be

Consistent until all pixels are loaded into mirror RAM.

9) Write CMM[7:0]ÿ1010xxxx to write mirror RAM data into NVM (Figure 13). During this

operation, the character memory is busy

The typical time is 5ms. STAT[5] can be read to confirm the completion of the NVM

write process.

10) Write VM0[3]=1 to enable OSD image display. To read character

bytes from character memory

1) Write VM0[3]=0, disable OSD image display, delay **30us** to do subsequent operations. 2)

Write

CMAH[7:0]=xxH, CMAL[6]=xH to select the

Characters (0-511) (Figure 10 and Figure 13).

3) Write CMM[7:0]ÿ0101xxxx, and read character data from NVM into mirror RAM (Figure 13).

This process takes 30us and requires

pay attention.

4) Write CMAL[7:0]ÿxxH, select 4 characters in the characters to be read

Prime bytes (0-63) (Figure 10 and Figure 13).

5) Read CMDO[7:0]=xxH, read the 4 pixel bytes selected by the data (Figure 11 and Figure 13).

6) Repeat step 4 and step 5 to read other bytes of 4 pixel data. 7) Write VM0[3]=1 to

enable OSD image display.

show memory operation

The following two steps support the viewing of the OSD image, when reading and writing the display memory

These steps are not required:

1) Write VM0[3]=1, enable OSD image display, delay **10us** to

Do follow-up operations.

2) Write OSDBL[4]=0 to enable automatic OSD black level control. This ensures correct OSD

image brightness. This register contains 4 factory preset bits [3:0], these bits cannot

be modified. Therefore, when modifying bit 4, first read OSDBL[7:0], modify bit 4, and

then write back the updated byte.

Clear Display Memory Procedure

Write DMM[2]=1 to start clearing display memory operation, this operation

Generally it takes 40us. Display memory cannot be written again until the clear operation is complete.

memory mode register. After the operation is completed, DMM[2] is automatically reset to zero.

In **8-** bit mode, the steps to write to the display memory

The 8-bit mode of operation is the most flexible when writing characters to display memory. this pattern
Each character is supported to be written to a separate character attribute byte (refer to Table 5).
This mode is different from the 16-bit working mode. In the 16-bit working mode, when writing a character, its
character attribute byte is automatically copied from DMM[5:3] (Fig.
19ÿÿ
Write DMM[6]=1, select 8-bit working mode.
Write character address bytes to display memory:
1) Write DMAH[1]=1 to write the highest bit of character address. 2) Write DMAH[0]=x to
select MSB, write DMAL[7:0]=
xxH to select the low-order data of the character data address to be written. the address
The position of the characters on the display is determined (Figure 10).
3) Write the highest bit CA9 of the character address to be written into the display memory
into DMDI[7:0] (refer to Figure 10 and Figure 19). 4) Write DMAH[1]=0 to
write character address byte. DMAH[0] and DMAL[7:0] remain unchanged. 5) Write the character address
byte (CA[7:0]) to be written into the display
memory
into DMDI[7:0] (refer to Figure 10, Figure 12, and Figure 19). Write character attribute
byte to display memory: 1) Write DMAH[1]=1 to write
character attribute byte. 2) Write DMAH[0]=x to select MSB, write DMAL[7:0]=

xxH to select the low-order data of the character data address to be written. the address
The position of the characters on the display is determined (Figure 10).
3) Write the character attribute byte to be written to the display memory to DMDI[7:0]
in (refer to Figure 10 and Figure 19).

In **16** -bit mode, the steps to write to the display memory

The 16-bit mode of operation increases the refresh rate of the display memory because, writing
When a new character, DMM[5:3] is automatically copied to the character attribute byte, from
And reduce the number of SPI write operations for each character from two to one (Figure 19).
In this mode, all characters written to display memory have the same attributes
byte. This mode is useful because consecutive characters usually have the same properties. Should
The mode is different from the 8-bit working mode, in the 8-bit working mode, but the character address word
Every time a section is written to display memory, the character attribute byte must be written (see
Exam Table 5). The setting of CA9 bit is not supported in 16-bit working mode, so the display
The character address written in the memory can only access 0-255. 1)
Write DMM[6]=0 to select 16-bit working mode. 2) Write DMM[5:3]ÿxxx, set local
background control (LBC), blink (BLK) and inversion (INV) attribute bits, in 16-bit working mode

These settings apply to all characters written to display memory when
superior.
3) Write DMAH[0]=x, select the MSB of the character data address to be written, write DMAL[7:0]=xxH,
select the lower address. This address determines the position of the character on the display (see
Figure 10).
4) Write the character address byte (CA[7:0]) to be written to the display memory into DMDI[7:0]. Store these
bytes together with the data from DMM[5:3]
character attribute bytes (Figure 12 and Figure 19).

In auto-increment mode, the steps to write to display memory

Auto-increment mode automatically increments the character address for each successively written character, thus
The speed of writing to display memory has been improved. From left to right on the display, from top
This mode can be used when writing strings. This mode reduces the SPI command
The number of (please refer to Table 5). CA9 bit setting is not supported in auto-increment mode
Please keep the corresponding bit of CA9 as 0 when writing. Therefore the display memory writes
The entered character address can only access 0-255.
In **8** -bit working mode: 1)
Write DMAH[1]=0, select whether to write character address byte; write
DMAH[1]=1, choose whether to write character attribute byte.
2) In auto-increment mode, write DMAH[0]=X to select the MSB of the start address, write DMAL[7:0]=XX to
select the low address data of the start address. This address determines the position of the first
character on the display
(Refer to Figure 10 and Figure 21).
3) Write DMM[0]=1 to set the auto-increment mode. 4) Write DMM[6]=1 to select
8-bit working mode. 5) Write CA data in a specific character sequence, display
the text on the screen,
This is a single byte operation. In auto-increment mode, the address of DMDI[7:0] is set automatically.
After a write operation, the display memory address is automatically incremented,
until the end of the displayed memory address.
6) Write CA=FFh to end auto-increment mode. Note: In auto-increment
mode, the character stored in CA[7:0]=FFh cannot be used, and the read operation is invalid until the end
of auto-increment mode.
In **16** -bit working mode:
1) In auto-increment mode, write DMAH[0]=X to select the MSB of the start address; write DMAL[7:0]=XX
to select the low bit of the start address
address data. This address determines the location of the first character on the display (please
Refer to Figure 10 and Figure 21).
2) Write DMM[0]=1 to set the auto-increment mode. 3) Write DMM[6]=0 to select
16-bit working mode. 4) Write DMM[5:3]=XXX, set the local background control
(LBC), blinking (BLK) and inversion (INV) attributes that will be applied to all characters

bit, in 16-bit mode, these settings will be applied to write to the display
on all characters in display memory.
5) Write the CA data in a specific character order and display the text on the screen. These will be stored
together with the character attribute bytes from DMM[5:3], please
Refer to Figure 19. This is a single byte operation. Auto-increment mode, automatic
Set the address of DMDI[7:0]. After a write operation, the display memory address is automatically
incremented until the end of the display memory address.
6) Write CA=FFh to end auto-increment mode. Note: In auto-increment
mode, the memory stored in CA[7:0]=FFh cannot be used
characters, read operations are invalid until the end of auto-increment mode.

In **8-** bit mode, the steps to read the display memory

1) Write DMM[6]=1 to select 8-bit working mode.

2) Write DMAH[1]=0, read character address byte; or write
DMAH[1]=1, read character attribute byte.

3) Write DMAH[0], select the address MSB of the data to be read (Fig.
10ÿÿ

4) Write DMAL[7:0], select the MSB of the data address to be read
low data (Figure 10).

5) Read DMDO[7:0] to read the number from the selected location in the display memory
According to (Figure 10).

In **16** -bit mode, the steps to read the display memory

1) Write DMM[6]=0 to select 16-bit working mode.

2) Write DMAH[0]=x, select the MSB of the character data address to be read
Write DMAL[7:0]=xxH to select the low-order data of the required address. the place
The address determines the position of the character on the display (refer to Figure 10).

3) Read DMDO[15:0] to read a character from the selected location in display memory
address byte and character attribute byte. character ground when the first data byte
address (CA[7:0]), the second byte contains the character attribute bits (Figure 20).
Note that for read operations, the bit arrangement of the character attribute byte is different from that for write
Bit arrangement during input operation. Please refer to display memory data output register
device (DMDO) section and Figure 20, to understand the read operation on the attribute bit
Description of median permutation.

Note: If the internal display memory read operation request and the SPI display store operation
occur at the same time, ignore the internal read operation request, during this time, the character display
The display may dim momentarily. Please refer to the Synchronizing OSD Updates section.

Synchronize **OSD** updates

If the internal display memory read operation request and the SPI display store operation are issued simultaneously
occurs, the character display may dim momentarily. Writing to the display during the vertical blanking interval
The memory prevents *momentary dimming of the OSD image. Use VSYNC as the host*
Processor interrupt to initiate a write to display memory for this function
able. Alternatively, the OSD image can be disabled synchronously before writing to the display memory,
Enable synchronously after writing (please refer to VM0[3:2]).

Multiple **OSDs** with a common clock

AT7456E raises a TTL clock output (CLKOUT), which can drive another
CLKIN pin of the AT7456E. Using an external clock driver can drive two
One or more AT7456E components, this arrangement can be achieved through a chip with a crystal oscillator
The AT7456E component provides the clock signal, reducing system cost (Figure 25).

OPERATING MODE	AUTO-INCREMENT T MODE DISABLED DMM[0] = 0	No. OF READ OPERATIONS	No. OF WRITE OPERATIONS	AUTO-INCREMENT T MODE ENABLED DMM[0] = 1	No. OF WRITE OPERATIONS
16-Bit Mode DMM[6] = 0	One-time setup Per character	2 3	1 3	One-time setup Per character	6 1
8-Bit Mode DMM[6] = 1	One-time setup Per character	1 6	1 6	One-time setup Per character	6 1

Table 5. Display memory access modes and SPI operation

The actual execution time comparison table of each operation command

	control commands	The judgment of whether the action is completed is based on MAX7456(min)	AT7456E(min)	AT7456E(typical)ÿ
power on reset	nRESET = 1 ÿ	STAT[6] = 0	39ms	39ms	50ms
hardware reset	nRESET = 0 nRESET = 1 ÿ	STAT[5] = 0	39ms	39ms	50ms
software reset	VM0[1] = 1	DMM[2] = 0	9us	28us	40us
clear video memory	DMM[2] = 1	DMM[2] = 0	9us	28us	40us
Off character display	VM0[3] = 0	STAT[5] = 0	0us	0 ~ 18us	30us
Open character display	VM0[3] = 1	STAT[5] = 0	0us	0 ~ 4us	10us
writing library	CMM = 0xa0	STAT[5] = 0	10ms	3.4/4.2ms	5ms
Read word library	CMM = 0x50	STAT[5] = 0	0.5us	22 us	30us

ÿNote 1ÿ nRESET keeps high level during power-on .

[Note 2] To control nRESET after the power supply is stable, first pull nRESET low, and then pull it high after maintaining it for 1us.

[Note 3] When using, if the user adopts the method of fixed delay, please refer to the typical value for the design of the delay parameters.

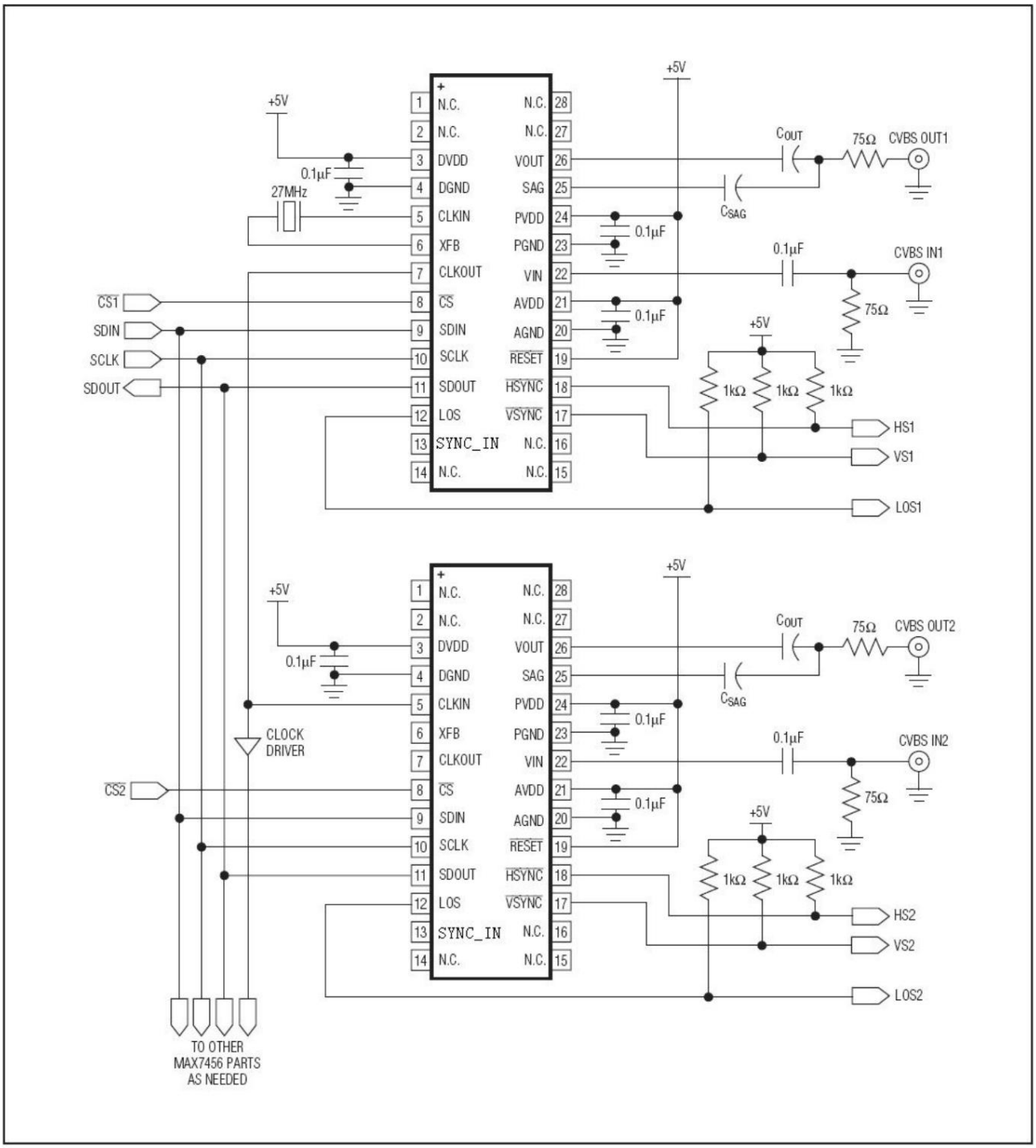
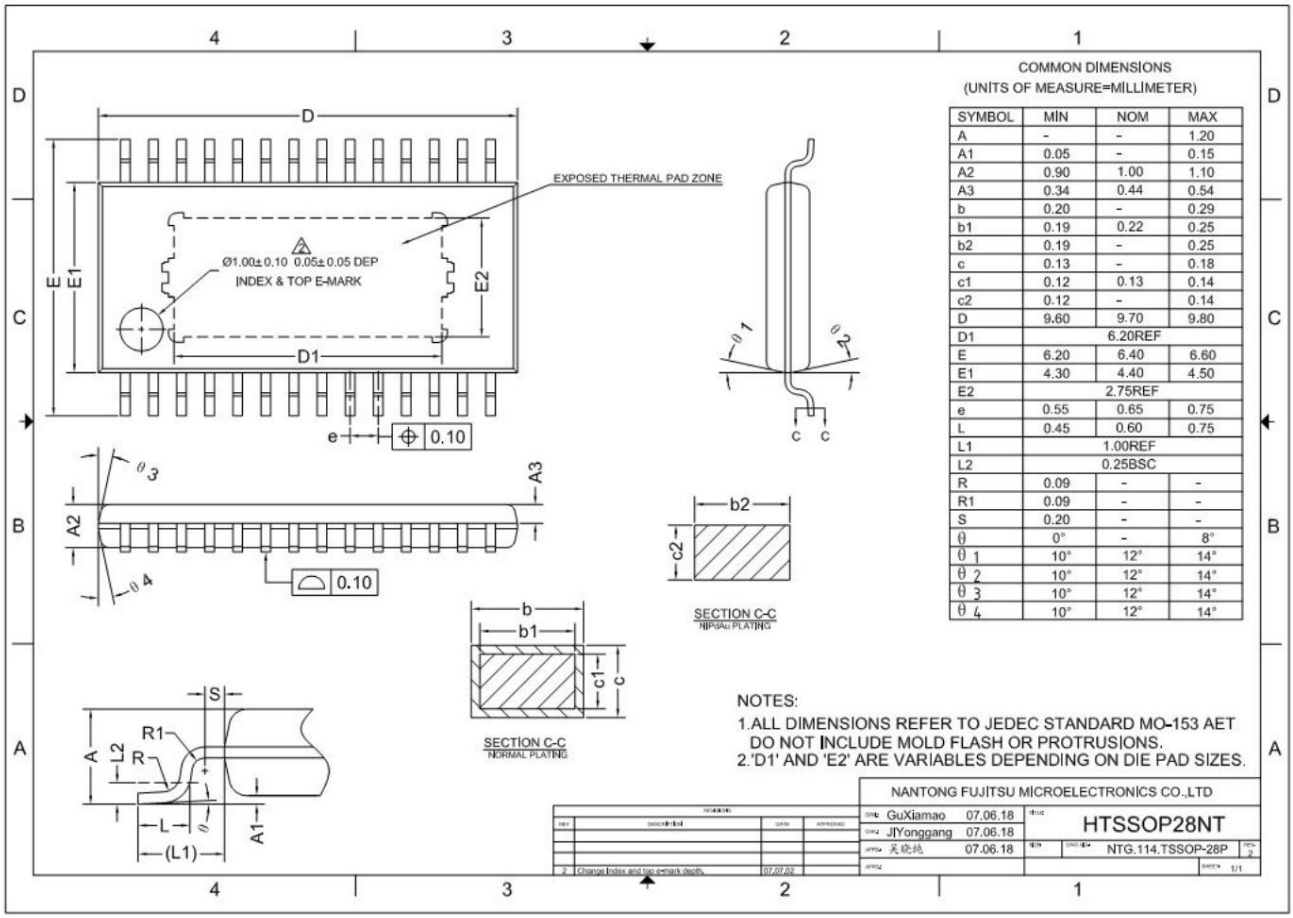


Figure 25. Typical Multiple OSDs with Daisy-Chained Clocks



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.10
A3	0.34	0.44	0.54
b	0.20	-	0.29
b1	0.19	0.22	0.25
b2	0.19	-	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
c2	0.12	-	0.14
D	9.60	9.70	9.80
D1		6.20REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.75REF	
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ	0°	-	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°