BeagleBone AI -64

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REVISION HISTORY

DATE	REVISION	DESCRIPTION OF CHANGES	AUTHOR
05 Aug 2021	BeagleBone AI TDA4VM_SCH_V1.0_210805	Initial Release, Frist prototype, 25PCS PCBA. 1. Page 25: Changed M.2_UART_WAKE# from CPU Pin AB2 to AE21. 2. Page 27: Changed MPU Linux debug UART from UART4 to UART0. Changed P9 Pin 42 from CPU Pin AC2_AB3 to AC2_AJ21. 3. Page All: Renumbered the part reference according to the placement on PCB.	Junqing.Xin
27 Oct 2021	BeagleBone AI -64_SCH_V1.01_211027	1. Page 7 13: Changed R81 R90 R92 R98 R99 from 500R 0.1% to 499R 1%. 2. Page 16: Connected VDDA_1P8_DSITX filtered supply to VDDA_1P8_MLB power group; Connected VDDA_0P8_USB filtered supply to VDDA_0P8_UFS power group. 3. Page 18: Replaced 2-T, 0.1uF 0201 cap C250(TI SCH C409) to 3-T, 1uF 0402; Removed 2-T, 0.1uF 0201 cap C247(TI SCH C414). 4. Page 20: Changed R162 from 1K to 10K. 5. Page 22: Changed LED1-LED6 color from blue to green to match the original white BBAI. Changed the power of LED6 from "VSYS_3V3" to "VSYS_IO_3V3". 6. Page 27: Changed mikroBUS header J10 from one slot to three slots to mate with the ribbon cable. Changed the power of J10(MCU mikroBUS Header) from "VSYS_IO_3V3" to "VSYS_3V3", so the MCU header could be in always-on domain. 7. Page 31: Changed FAN header J1 from 3Pin_DIP_2.54MM to 4Pin_SMD_1.25MM header. Changed "W23_UART4_RXD" to "W23_FAN_PWM", "W28_UART4_TXD" to "W28_FAN_TACH". 8. Page 32: Removed the PMIC programming header J1 and multiplexer IC U34 SN74CBTLV3257PWR. Changed R15 from 10K to 0R, R13 from 10K to DNP. 9. Page 33: Changed R23 from 10K to 0R, R18 from 10K to DNP. 10. Page 34: Removed R310=0R from the power net "VSYS_IO_3V3" to increase the current from 4A to 6A. Changed the power of CSI, DSI, M.2 connector from "VSYS_3V3" to "VSYS_IO_3V3", so the power can be turned off by GPIO "EN_3V3IO_LDSW" of PMIC.	Junqing.Xin
19 Nov 2021	BeagleBone AI -64_SCH_V1.02_211119	1. Page 23: Changed USB2.0 Hub U20 TI_TUSB4041IPAPR to USB3.0 Hub TI_TUSB8041RGCR. 2. Page 24: Changed Type-C port USB signal from HS to HS+SS, and connected SS to each side of the cable. Added CC logic IC TI_TUSB322IRWBR(used by BB AI AM57 RevA1), which can operate as sink application (UFP) default. 3. Page 26: Added some test points, which are used for TI testing only. 4. Page 31: Added RC filter(R392=49.9R, C548=33pF, R393=0R) to CS and VOUT pins of DCDC IC U3 TI_LM5141RGER to debug the OV output issue. 5. Page 34: Changed the power of ethernet & USB3.0 hub from TI_TLV75801PDBVR(LDO, 0.5A) to TI_TPS74801DRCR(LDO, output current 1.5A). 6. Page 17 18: Changed C341, C479...12PCS 10uF feed through capacitor from Murata_NFM18HC106D0G3L(10uF 0603, Out of Stock) to Murata_NFM21PS106B0J3D(10uF 0805). Second Release, Second prototype, 20PCS PCBA.	Junqing.Xin

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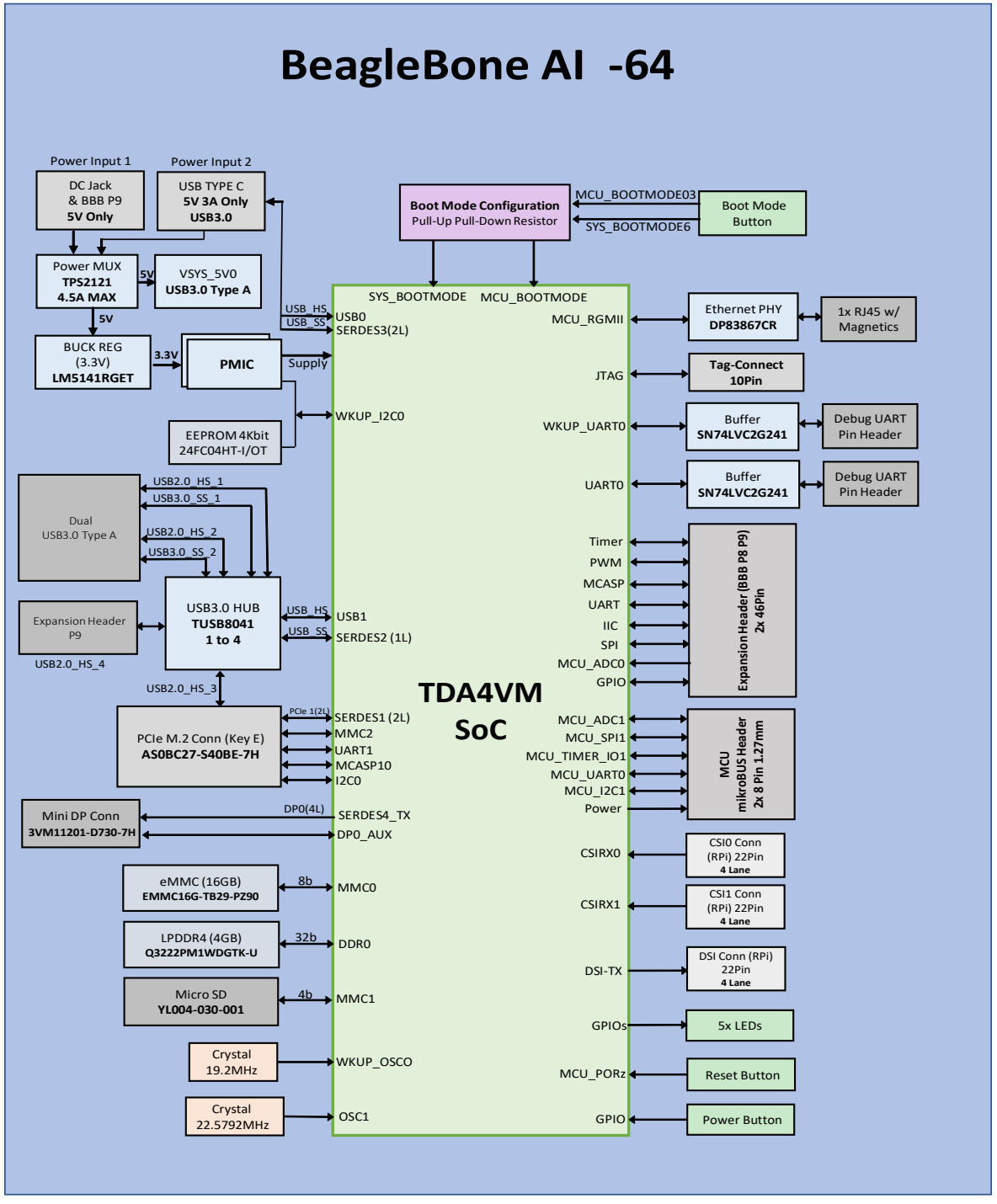
SYSTEM BLOCK DIAGRAM



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3-Phase DUAL PMIC PDN Recommended for New Designs
(3-Phase Buck supplying VDD_CPU)

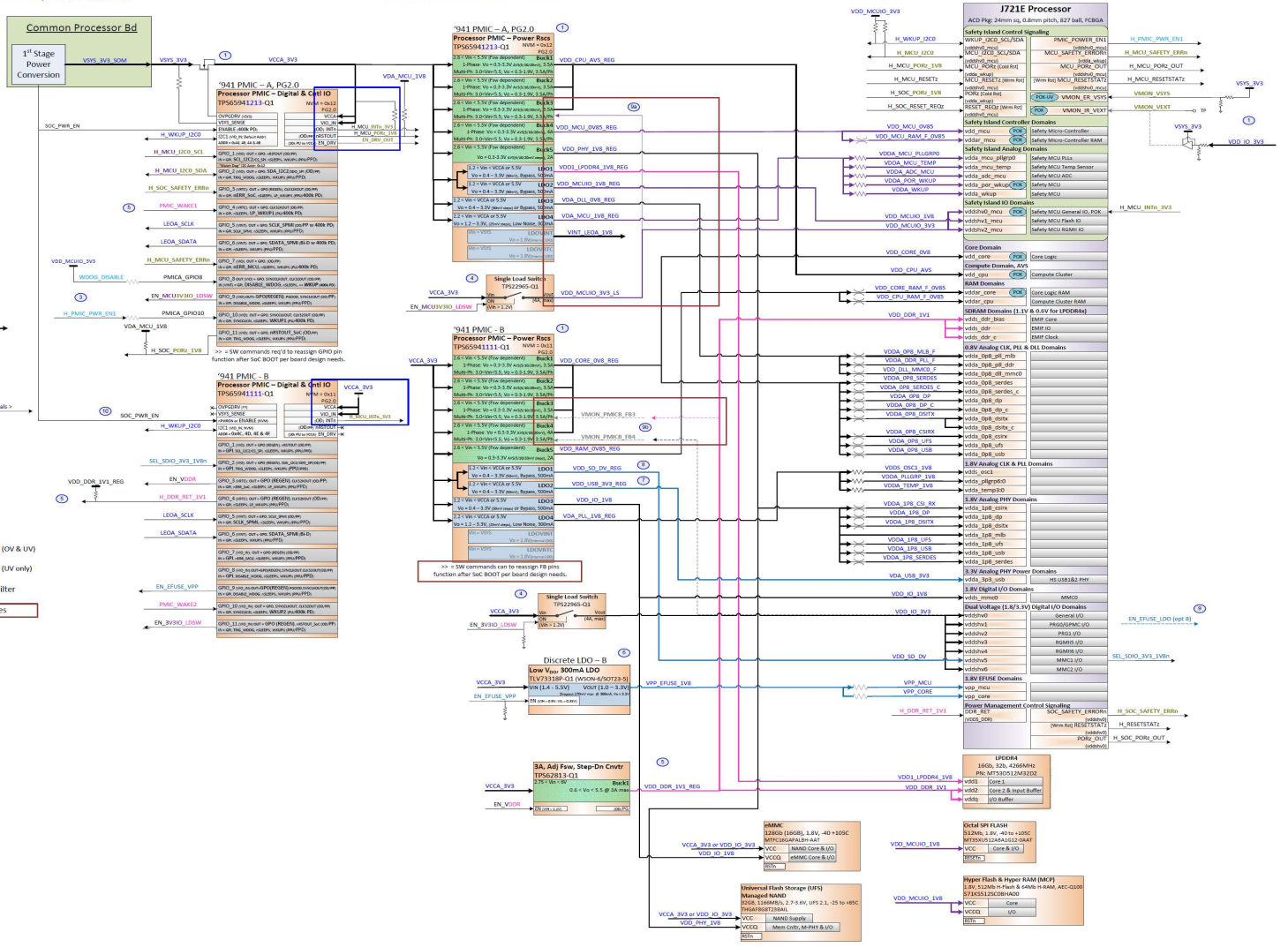
DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0C
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594**1213**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **13**, PG2.0)
Leo PMIC-B, PN TPS6594**1111**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **12**, PG2.0)

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable system with independent MCU & Main power for FFI
3. SDRAM: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
5. Low power modes: MCU Only & DDR Retention
6. Signaling Levels: MCU & Main Dual VIO
7. End Product Options:
   a. Compliant high-speed SD Card
   b. Compliant USB 2.0 data eye
   c. HS SoC Efuse programming on-board

V0.14	1/27/2021	1. Added example of VDD_IO_3V3 OV/UV monitoring by SoC's VMON_IR_VEXT input connection option to voltage buffer & voltage R-div needed to interface with SoC's internal R-div network optimized for monitoring 1.8V power rails. 2. Added 2x ext voltage monitoring inputs options for OV/UV monitoring by Hera PMIC of any safety critical system power rails. Hera's quad buck config can reassign remote sense feedback inputs (FB3 & FB4) for power rail monitoring. 3. Updated notes 1 & 9 accordingly.
V0.15	2/13/2021	Following final PMIC NVM review for defining new common PN ("1213") for Leo PG2.0 used in PDN-0C & -1A: 1. Update notes 2. Changed PMIC-A FB3 VMON input to be connected to VCCA_3V3 since VDD_MCUIO_3V3 rail is not supported, see note 9a. 3. Added PMIC-B FB3 & FB4 assignment for VMON by SW after SoC boot for ext power rail monitoring options, see note 9b.
V0.16	3/2/2021	1. Removing discrete load switch from supplying PMIC's VIO_IN since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related "Note #2" has been removed.



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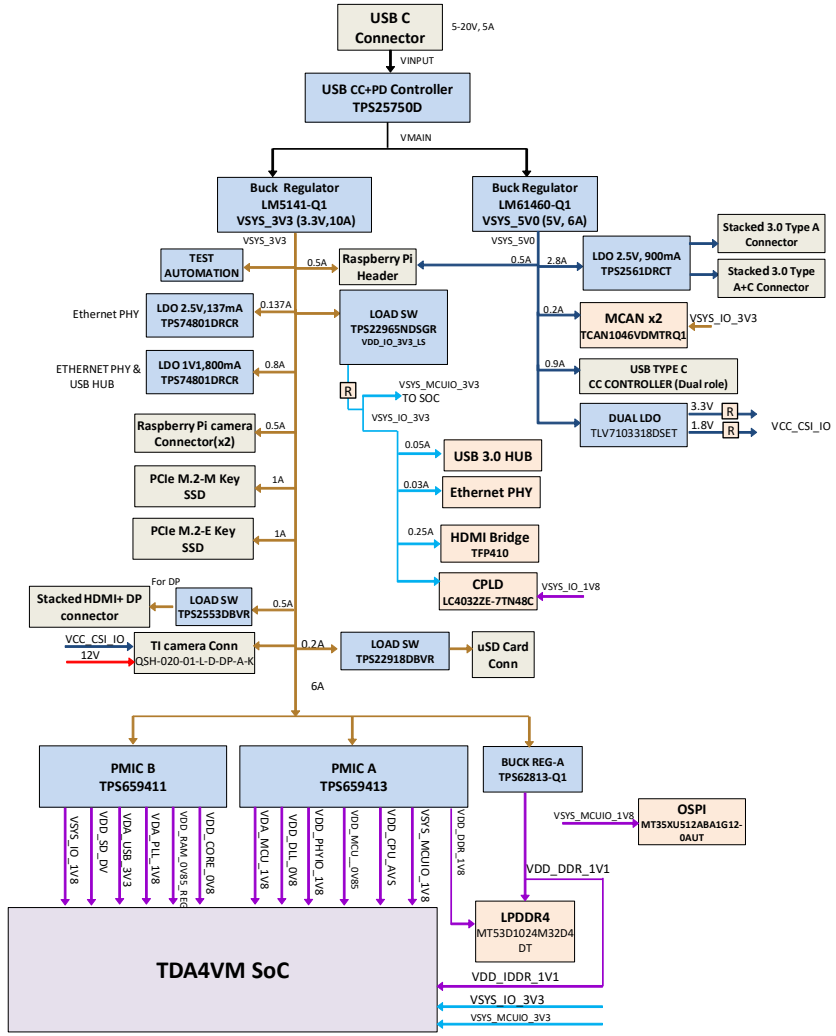
POWER FLOW DIAGRAM

Will updated in DVT



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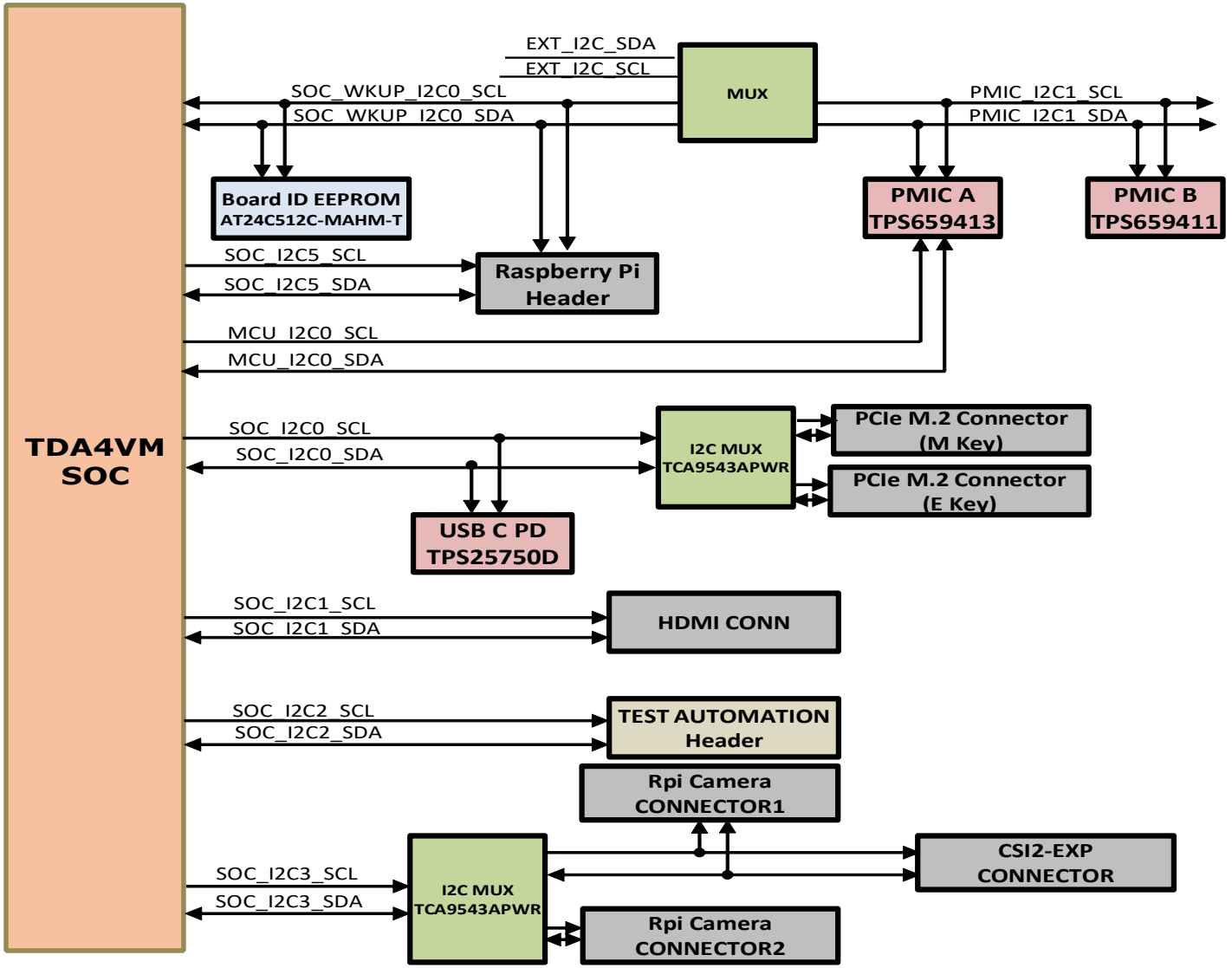
Will updated in DVT

I2C TREE



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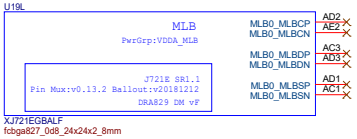
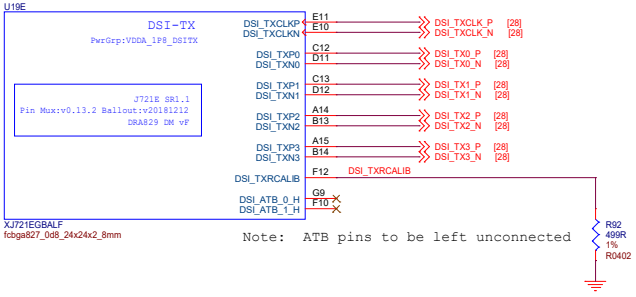
MLB

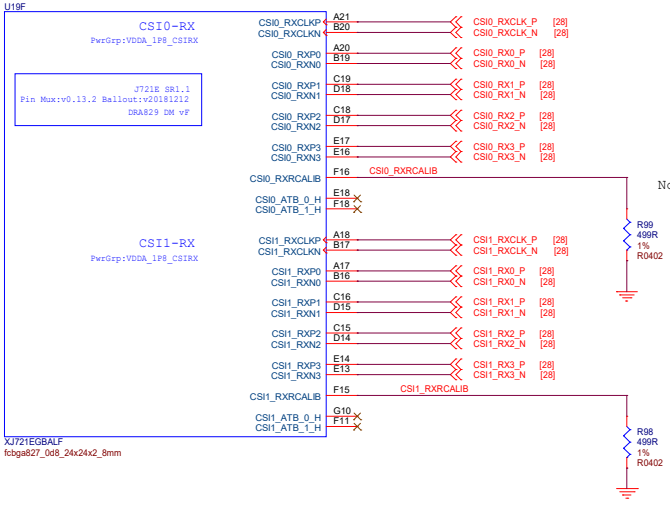


DSI



Note: ATB pins to be left unconnected

CSI Interface



Note: ATB pins to be left unconnected

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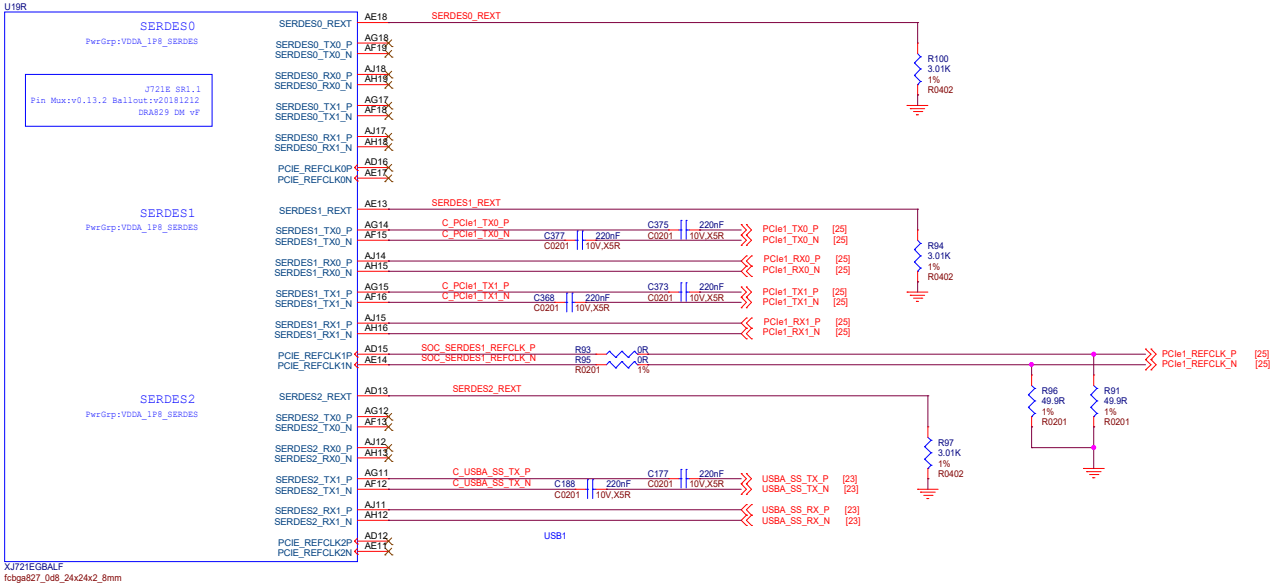
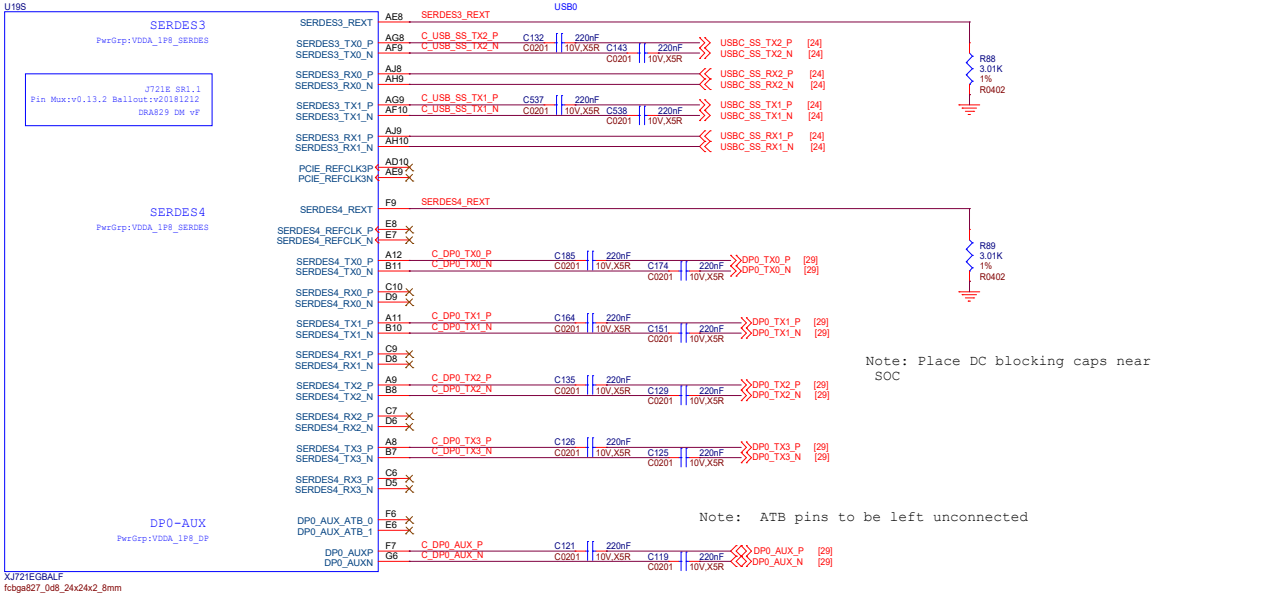
SERDES





Note: Place DC blocking caps near SOC

Note: ATB pins to be left unconnected

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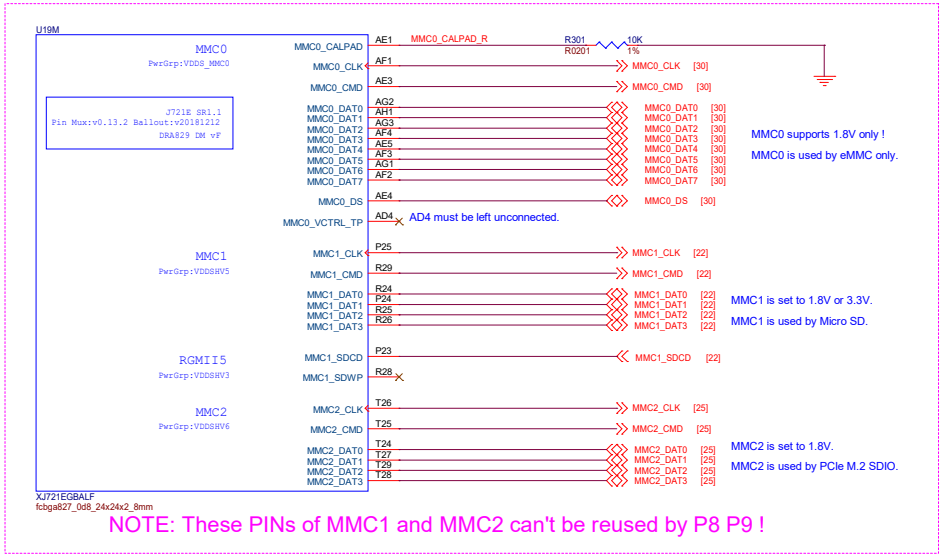
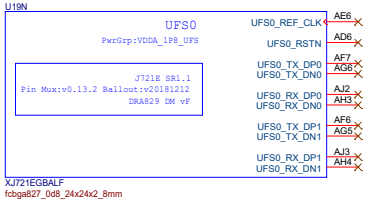
MMC Interface



NOTE: These PINs of MMC1 and MMC2 can't be reused by P8 P9 !

UFS Interface



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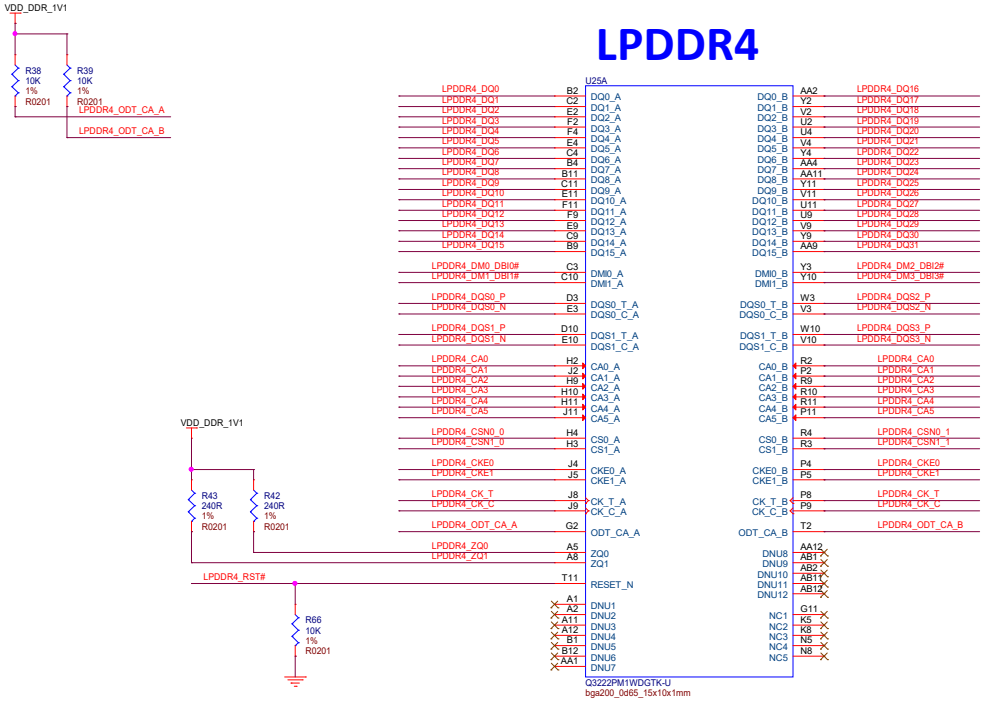
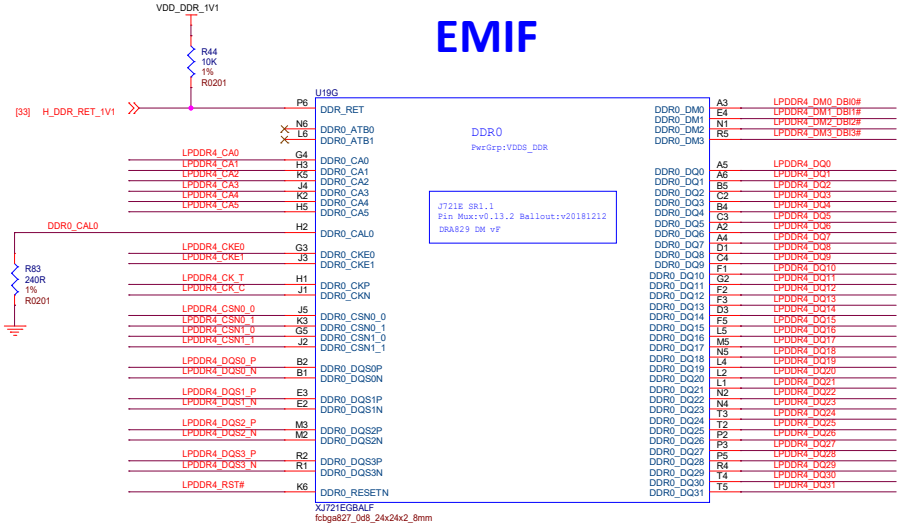
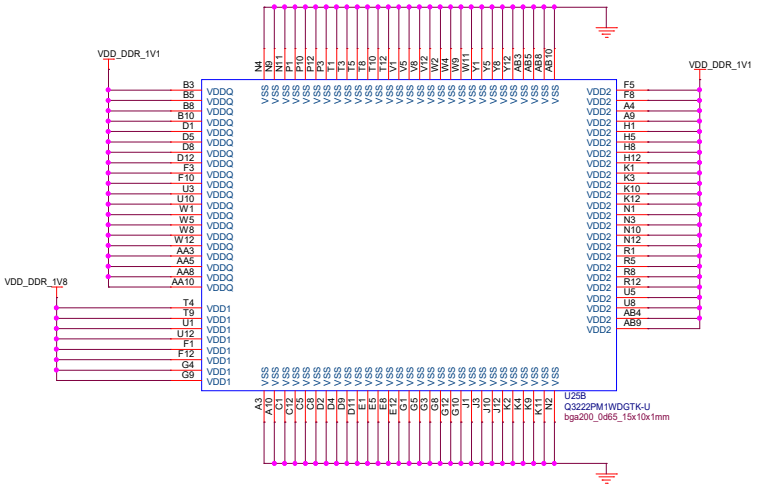
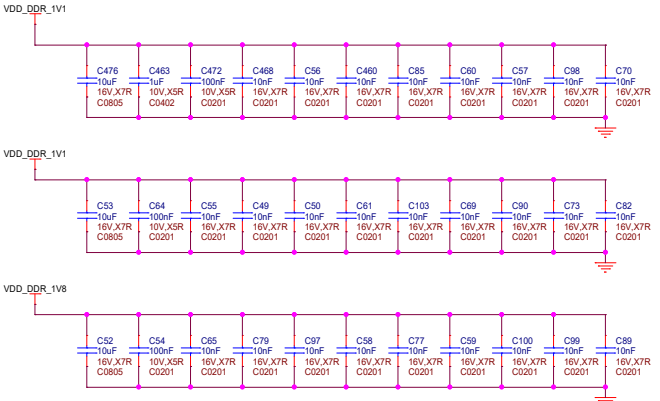
LPDDR4



EMIF







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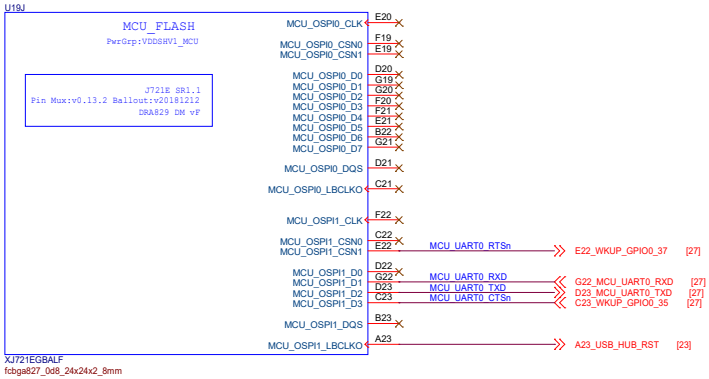
MCU OSPI



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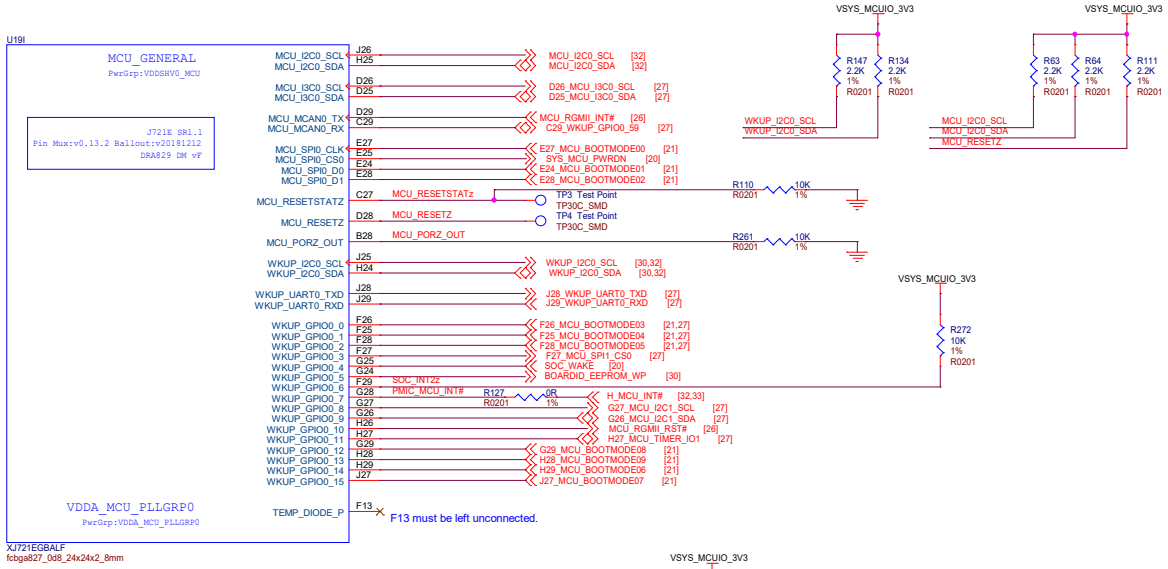
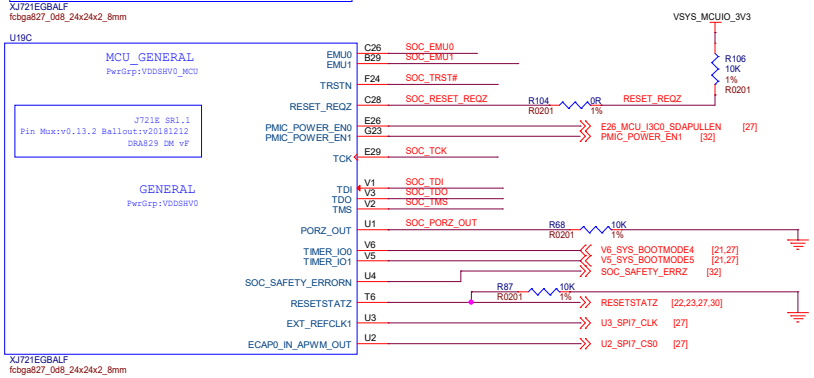
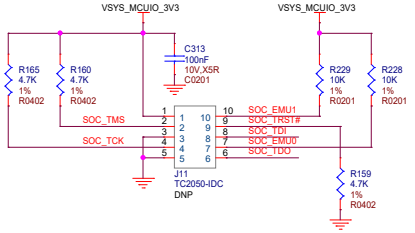
MCU & MAIN GENERAL IO, OSC CLKS

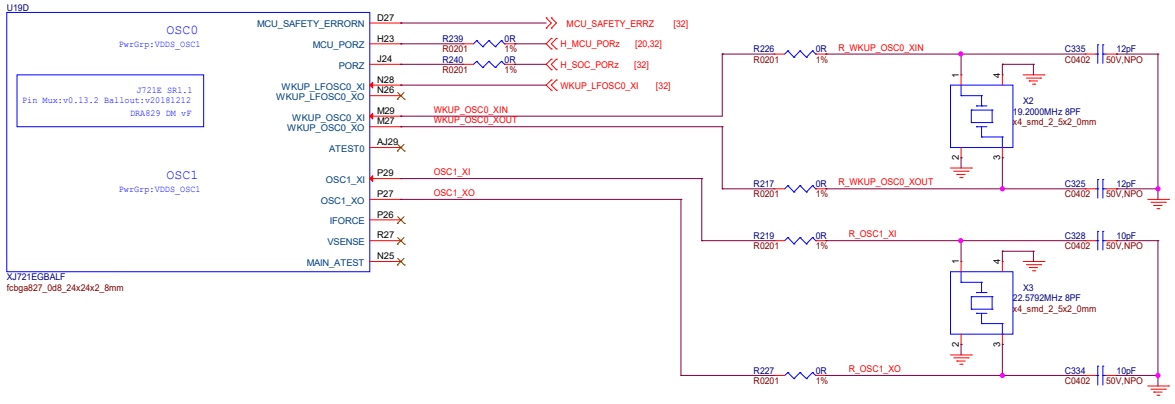




Tag-Connect



OSC



CLKS

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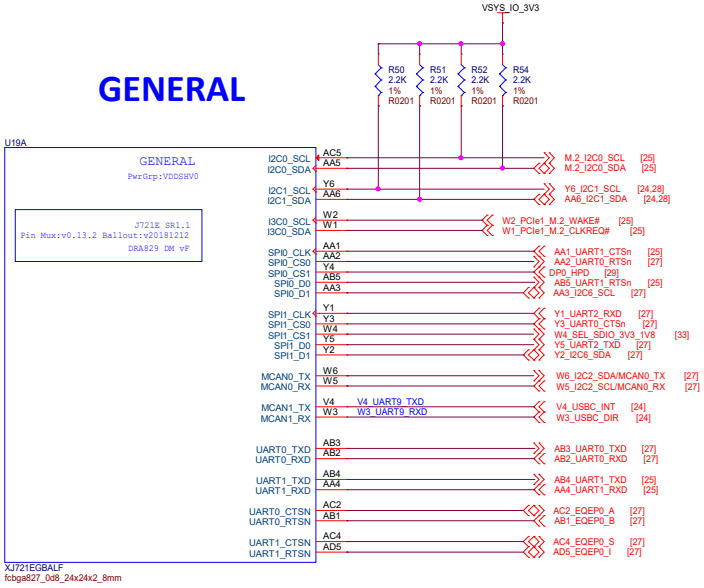
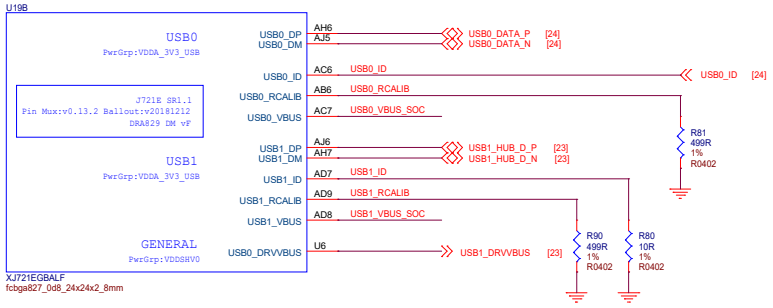
GENERAL



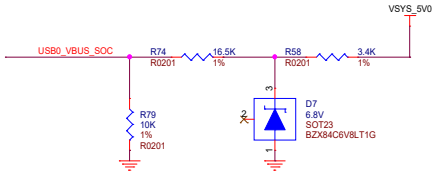
USB



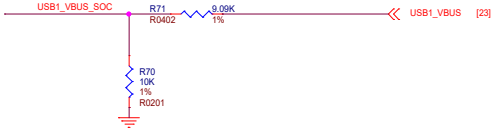
USB1_ID Pulled low. J7 SoC in Host Mode.

USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V VBUS



Note: Recommended VBUS circuit for embedded Hub



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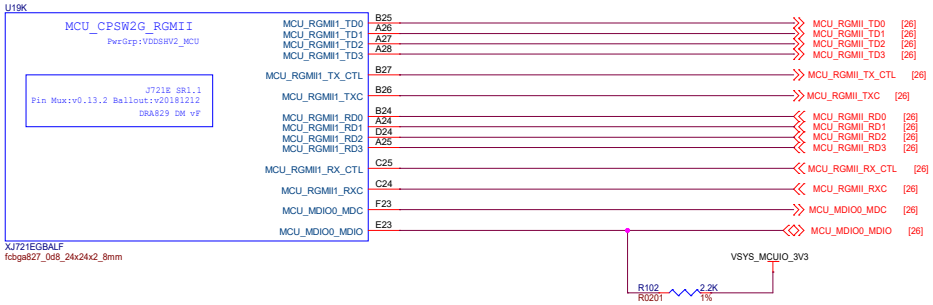
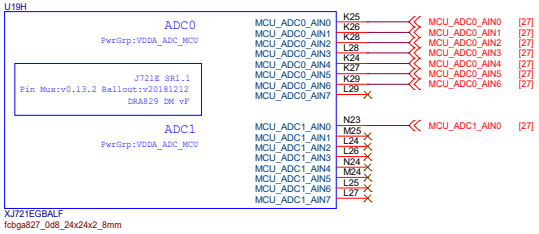
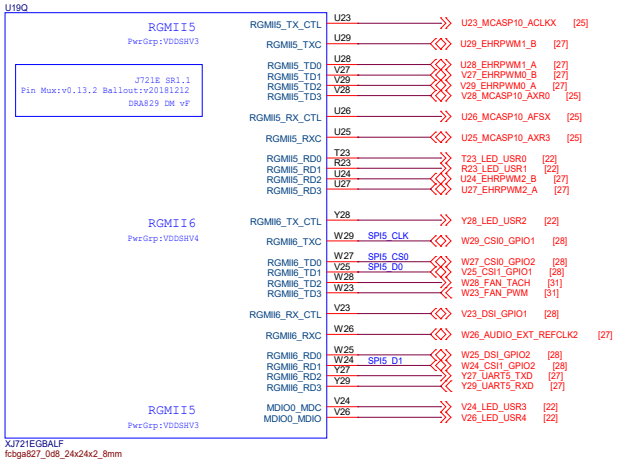
MCU_RGMII



MCU ADCs



MAIN RGMII



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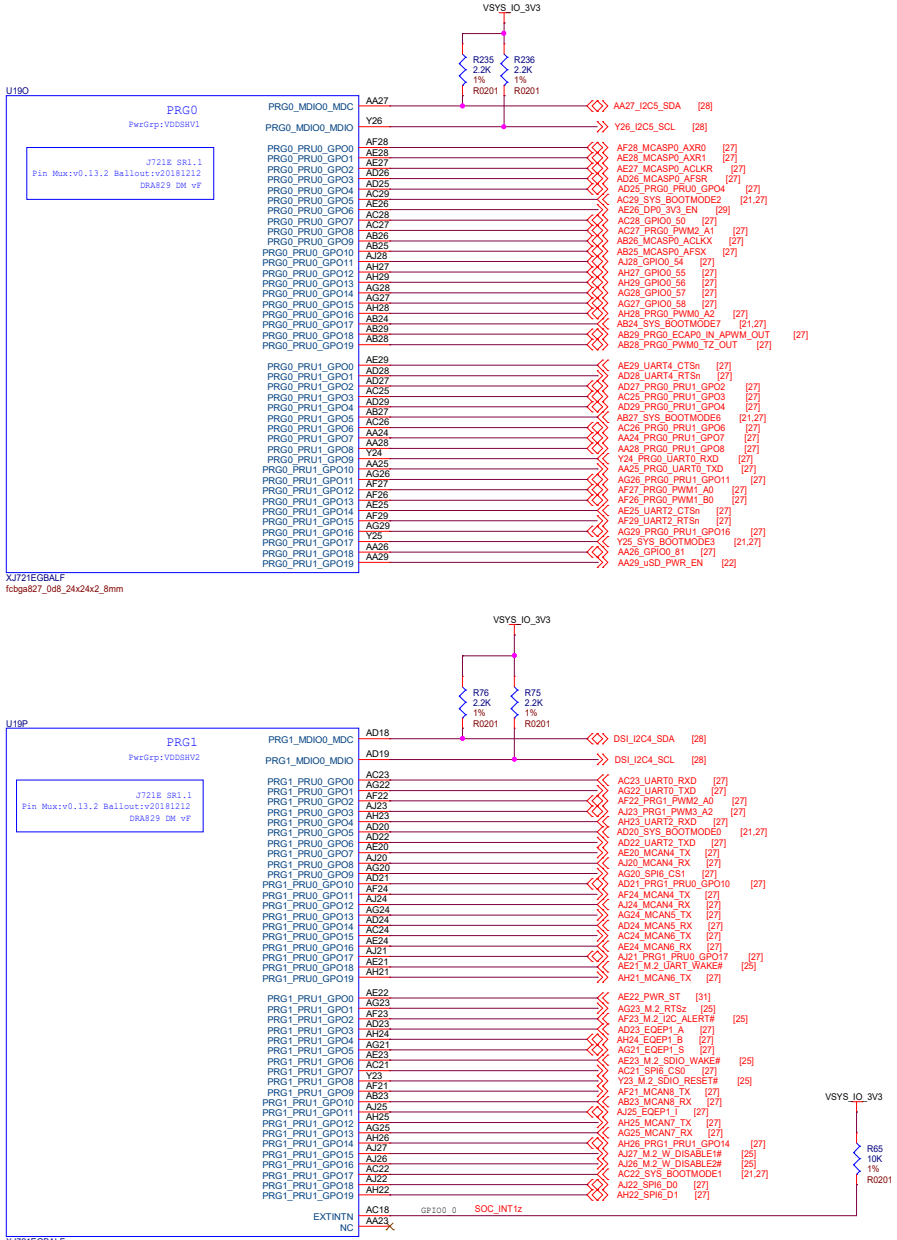
PRG0 & PRG1



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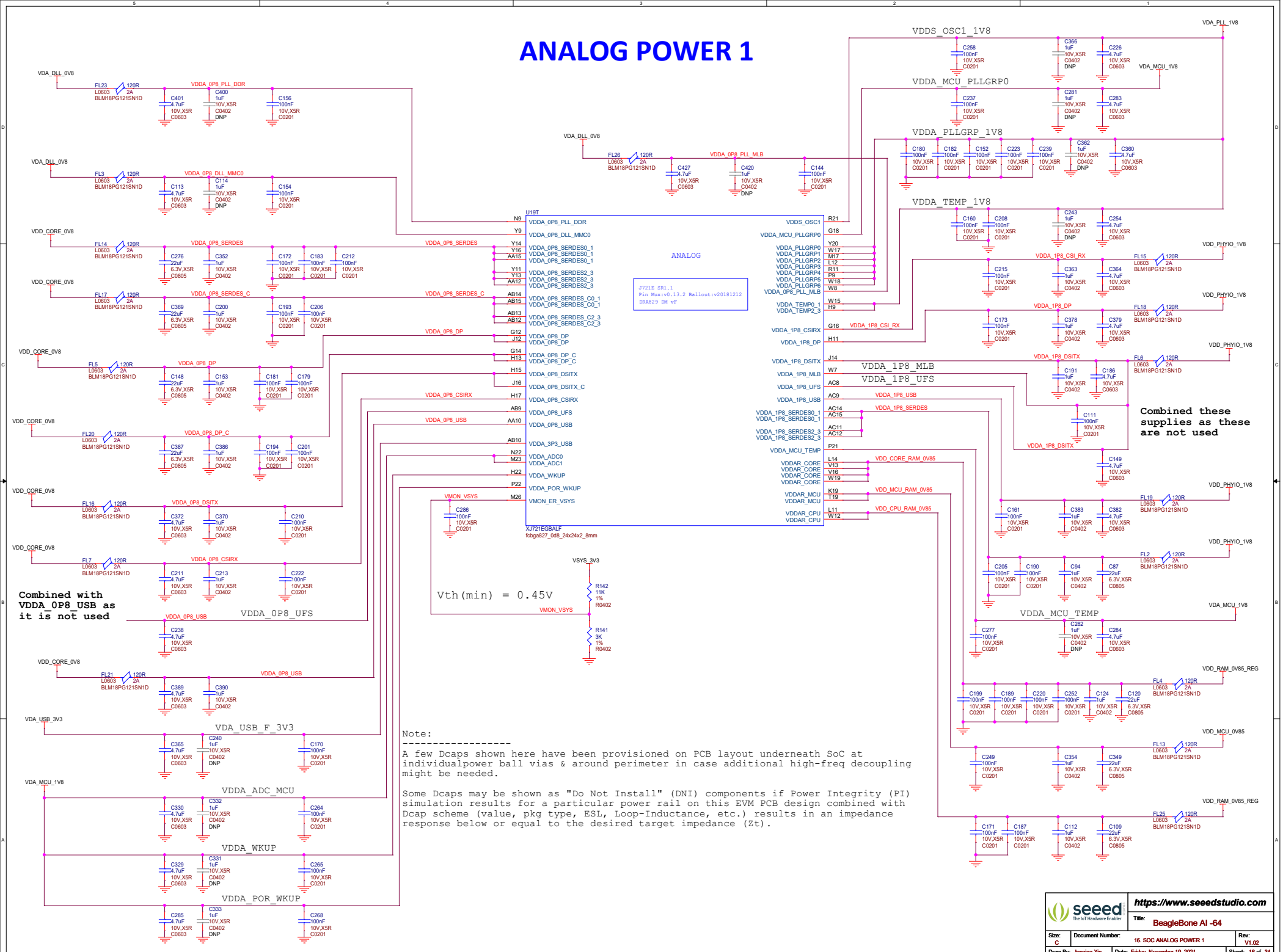
ANALOG POWER 1



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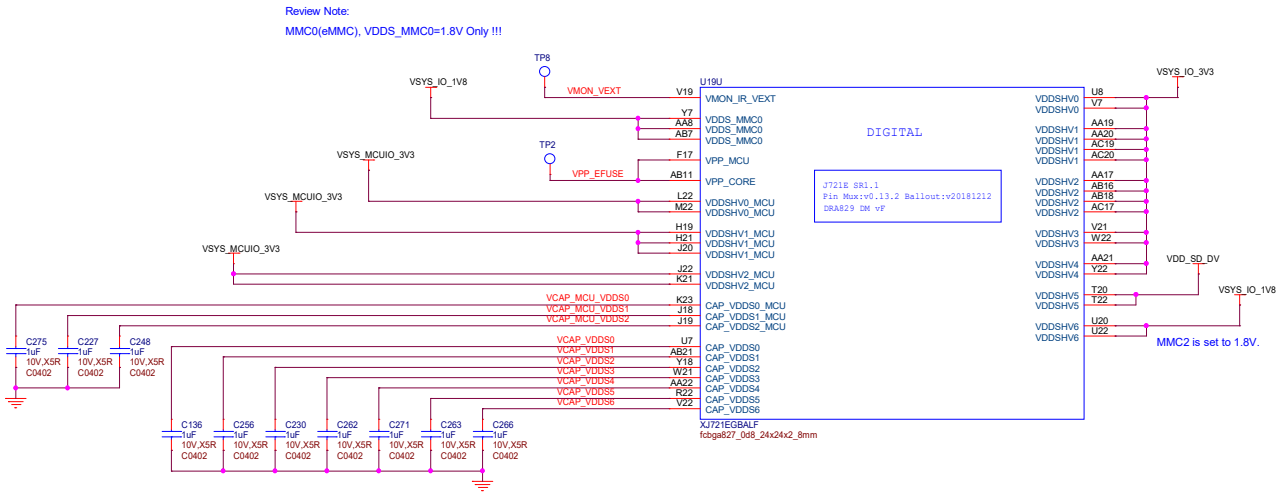
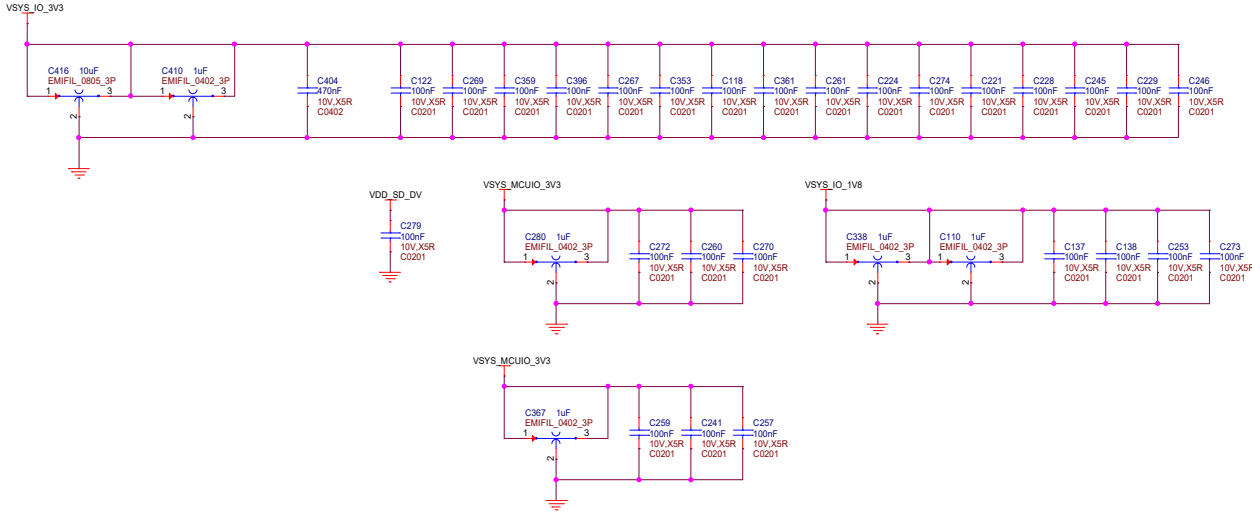
DIGITAL POWER 2





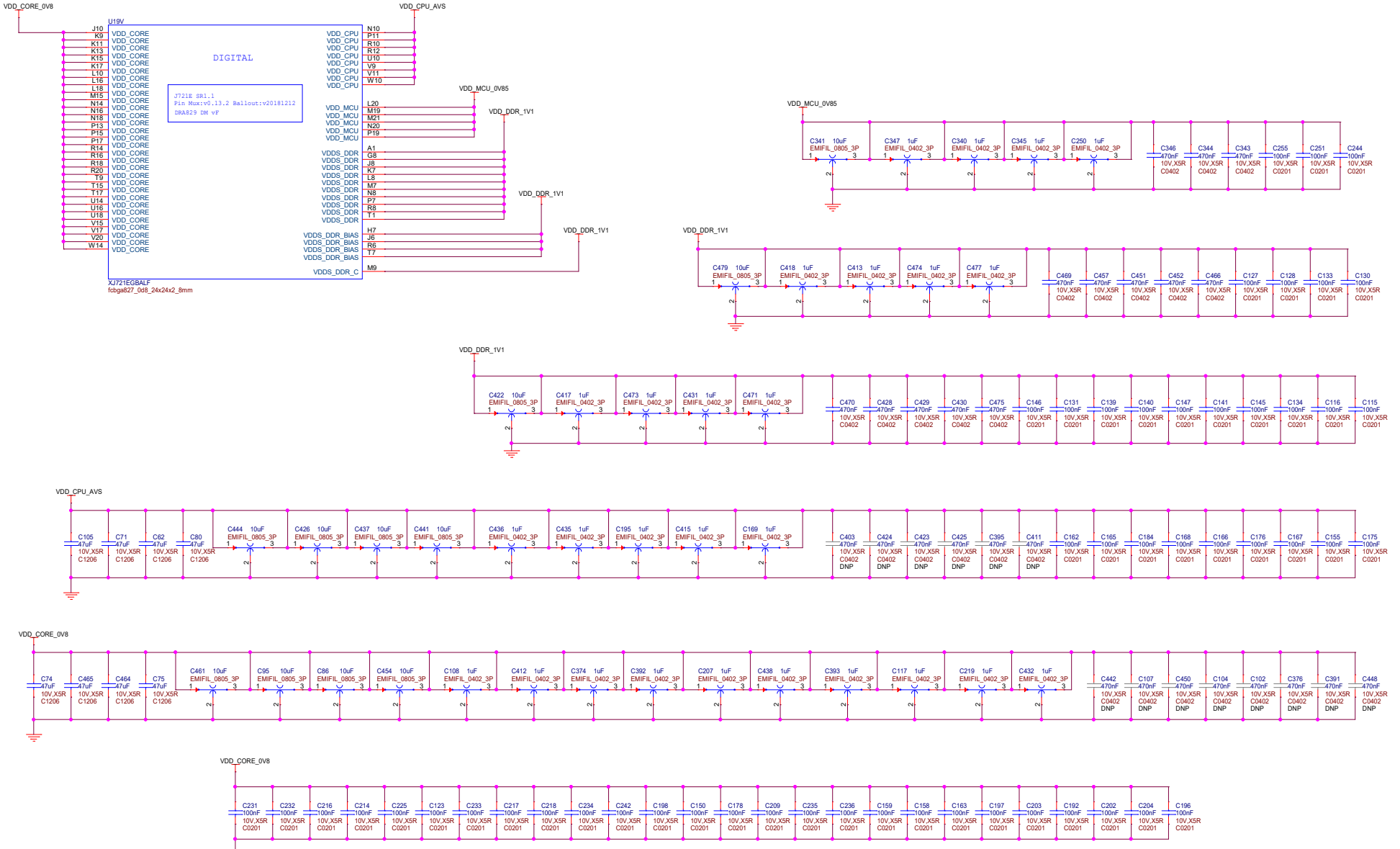
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI -64	
Size: C	Document Number: 17. SOC DIGITAL POWER 2	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 17 of 34

DIGITAL POWER 3



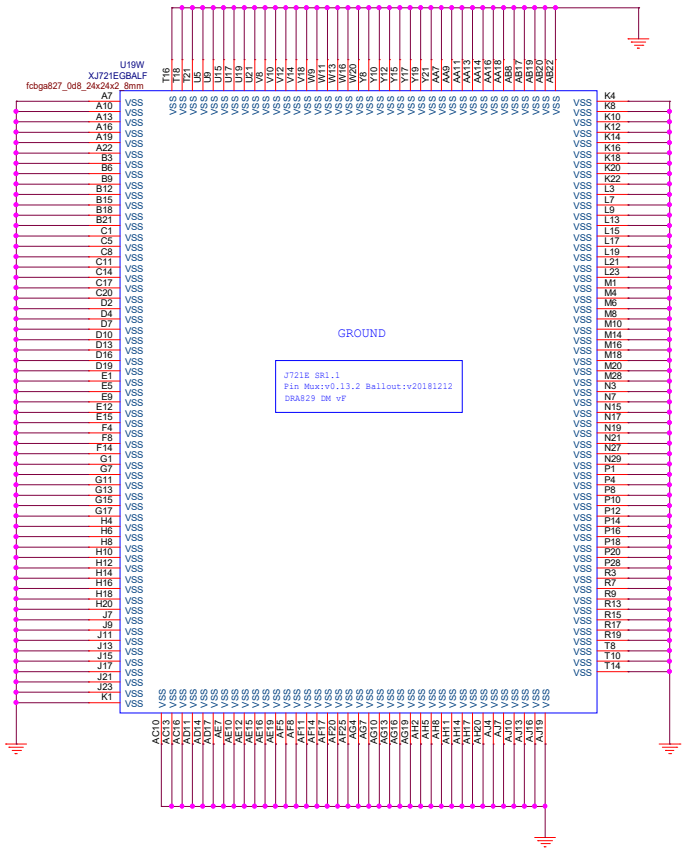
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

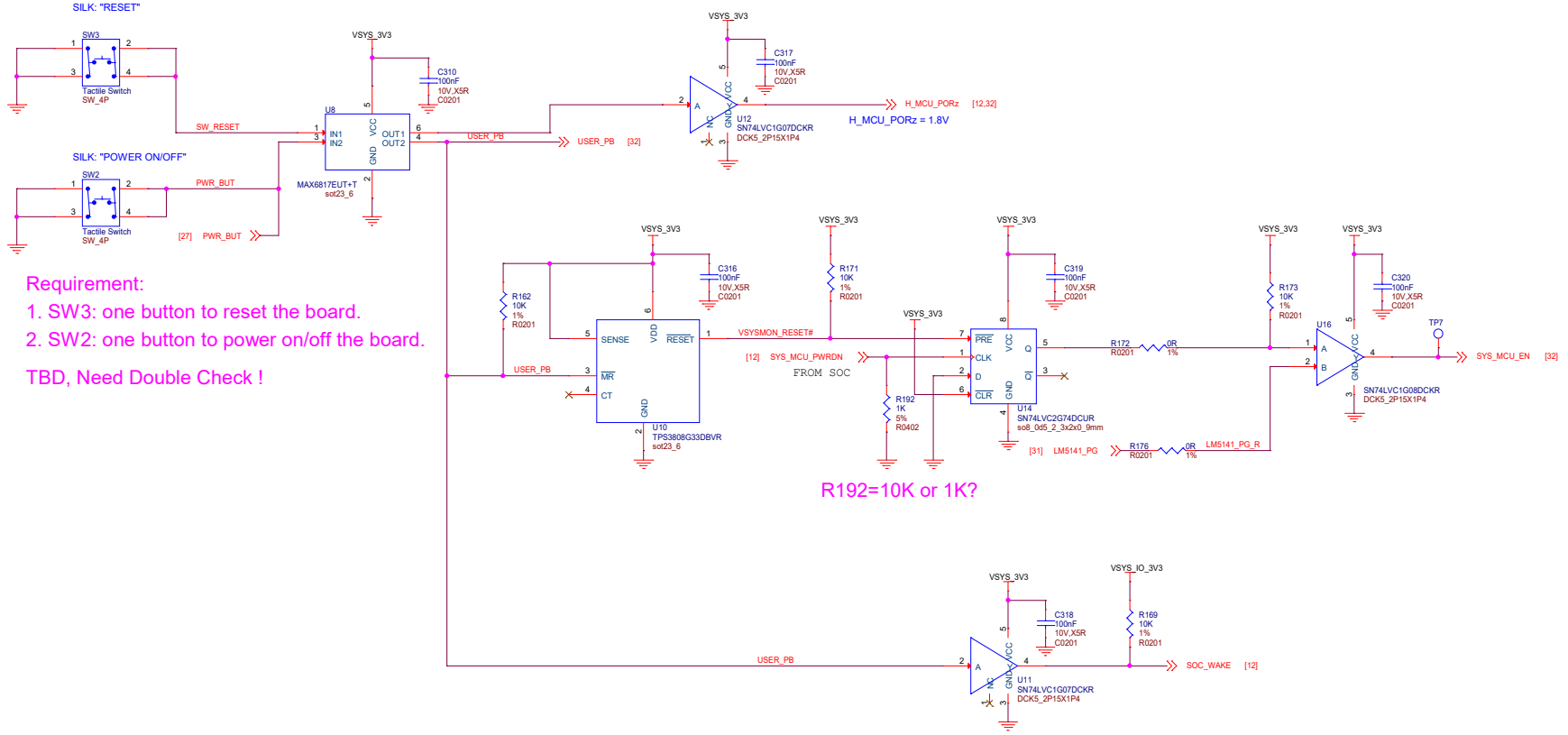
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI -64	
Size: C	Document Number: 18. SOC DIGITAL POWER 3	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 18 of 34

SOC GROUND

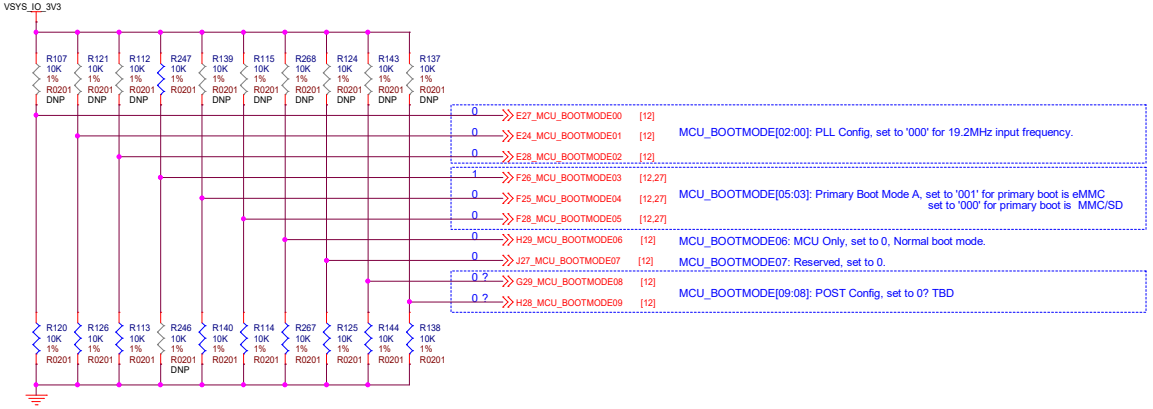


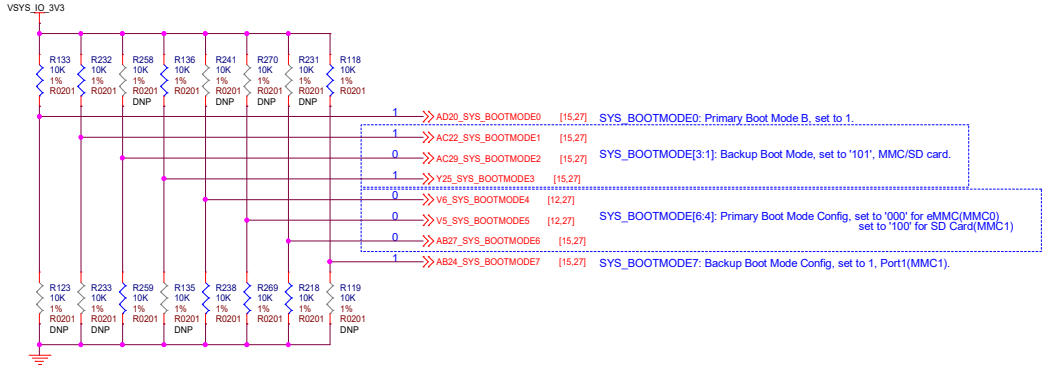
seeed The IoT Hardware Enabler		https://www.seeedstudio.com	
		Title: BeagleBone AI -64	
Size: C	Document Number: 19. SOC GND		Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021		Sheet: 19 of 34

RESET, POWER ON/OFF BUTTONs

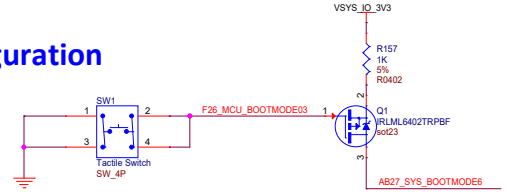


seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI -64	
Size: C	Document Number: 20. RESET, POWER BUTTONs	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 20 of 34





Boot Mode Configuration



Push-button SW1	Primary Boot Mode	Backup Boot Mode	MCU_BOOTMODE05	MCU_BOOTMODE04	MCU_BOOTMODE03	SYS_BOOTMODE6	SYS_BOOTMODE5	SYS_BOOTMODE4
Open	eMMC(MMC0)	SD Card(MMC1)	0	0	1	0 (Port 0)	0 (8-bit)	0 (1.8V)
Closed	SD Card(MMC1)	SD Card(MMC1)	0	0	0	1 (Port 1)	0 (4-bit)	0 (Filesystem mode)

Primary boot with BOOT normal-open push-button selecting eMMC port 0 (open) or MMC/SD port1 (closed).

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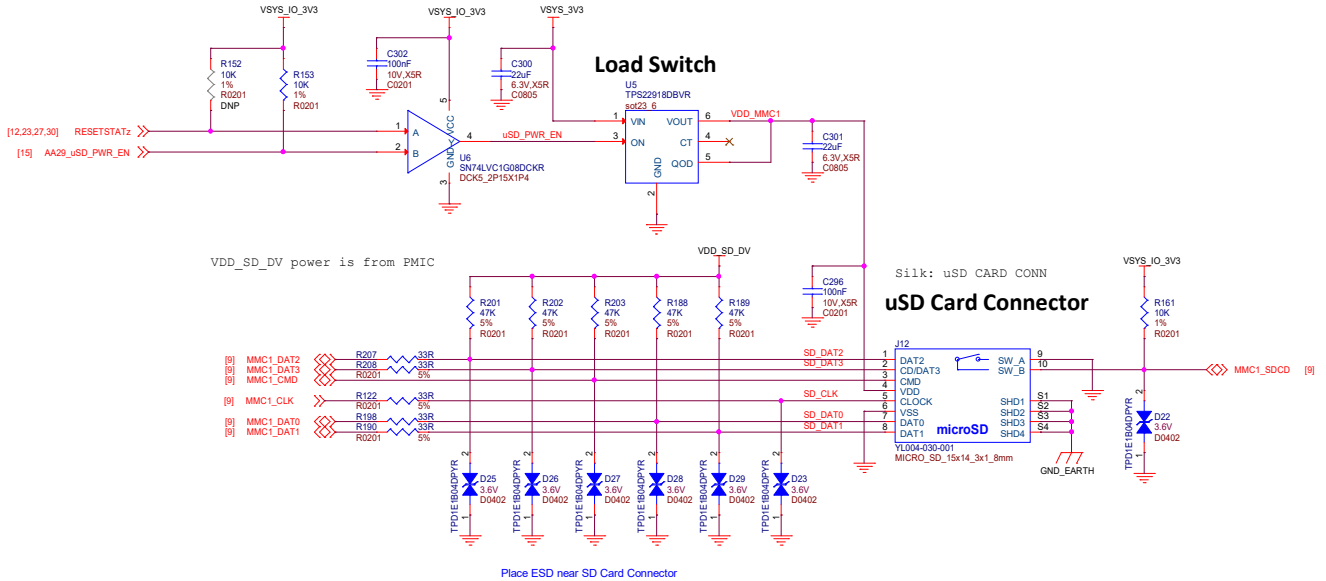
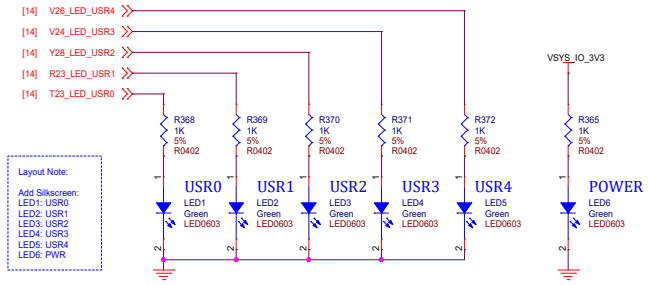
	Title: BeagleBone AI -64	
Size: C	Document Number: 21. Boot Mode Configuration	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 21 of 34

Micro SD CARD INTERFACE

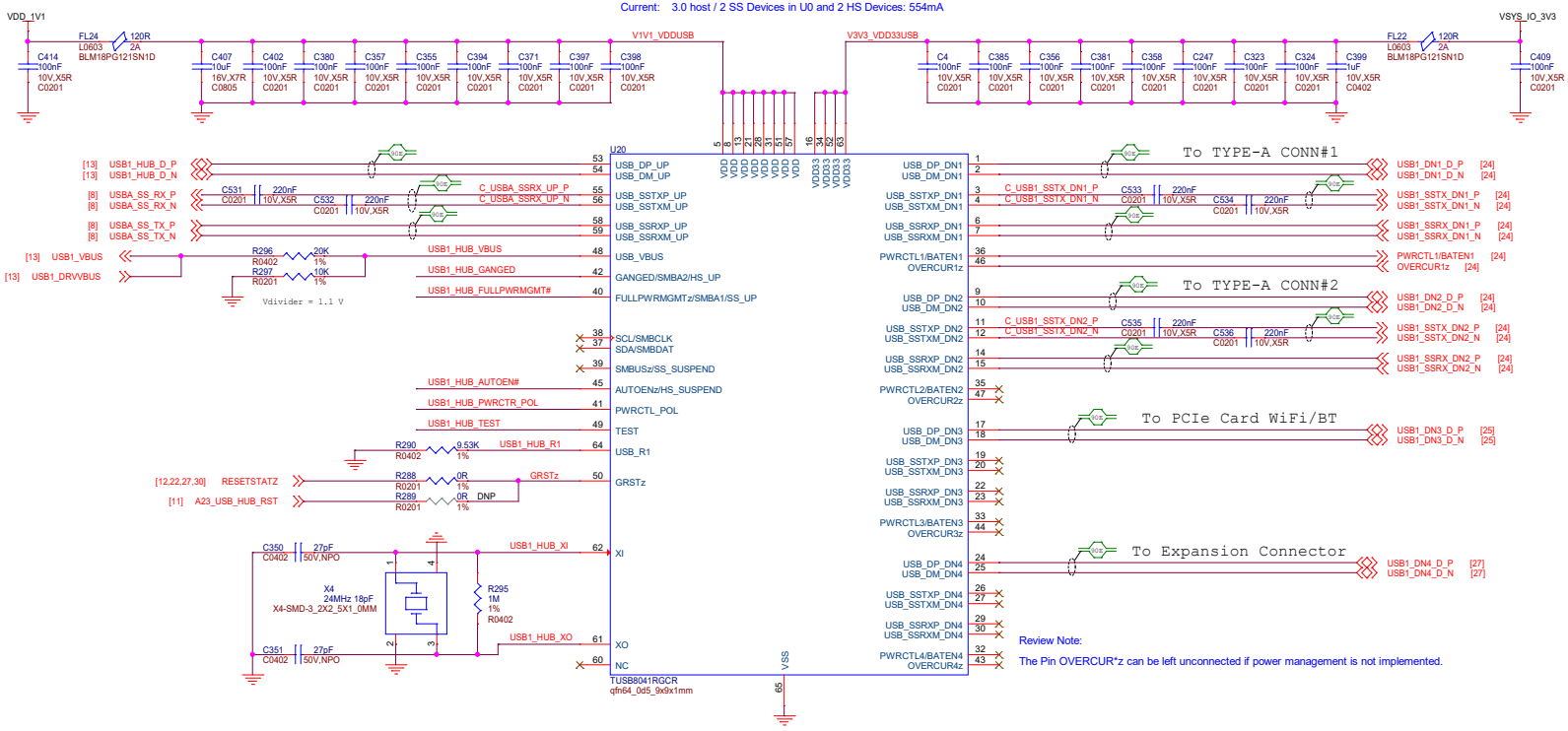


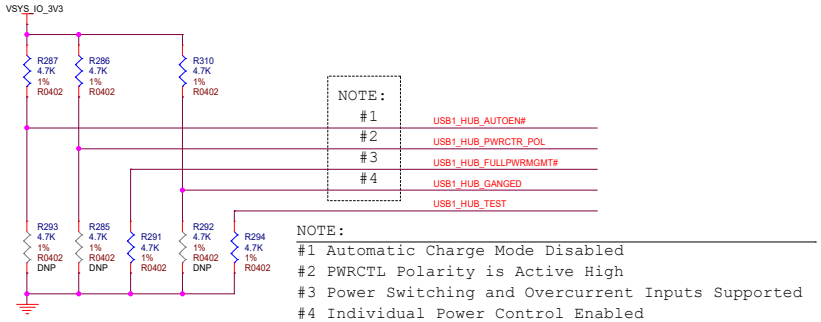
LEDs



seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI -64	
Size: C	Document Number: 22. MICRO SD, LEDs	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 22 of 34

USB 3.0 HUB





NOTE:

#1 Automatic Charge Mode Disabled

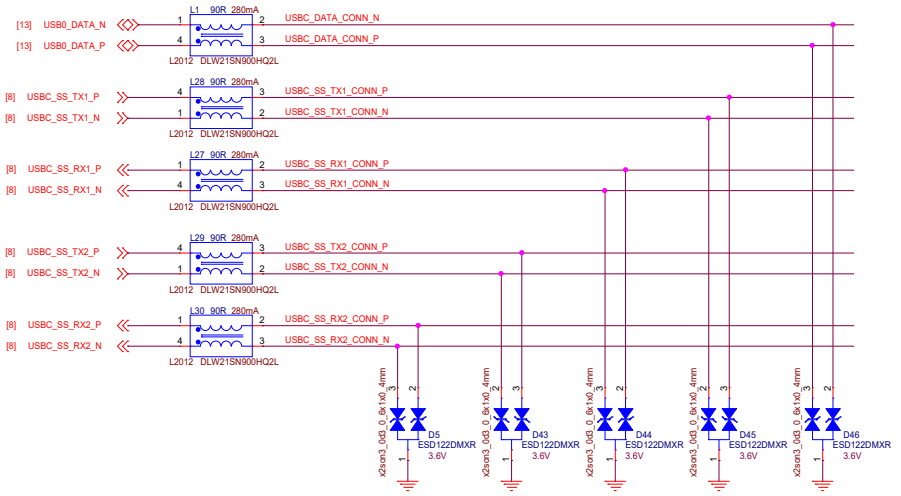
#2 PWRCTL Polarity is Active High

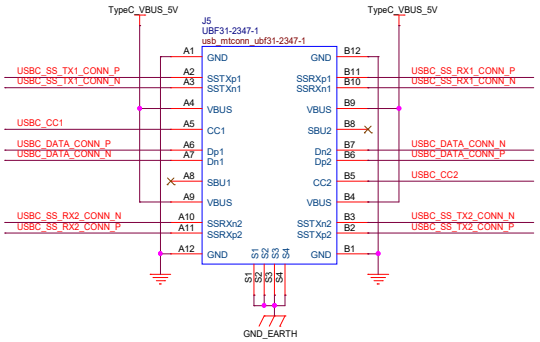
#3 Power Switching and Overcurrent Inputs Supported

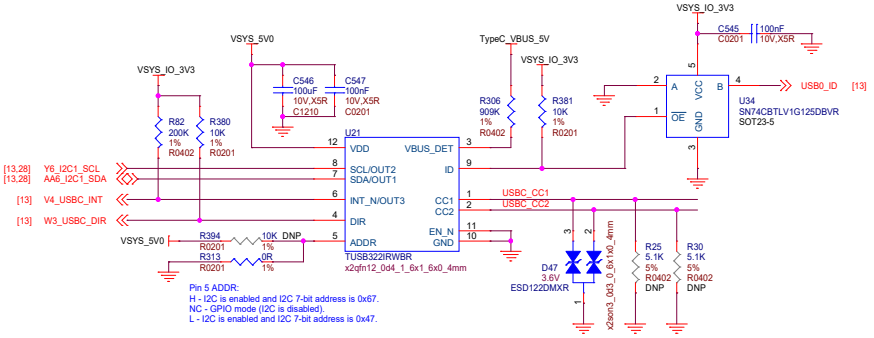
#4 Individual Power Control Enabled

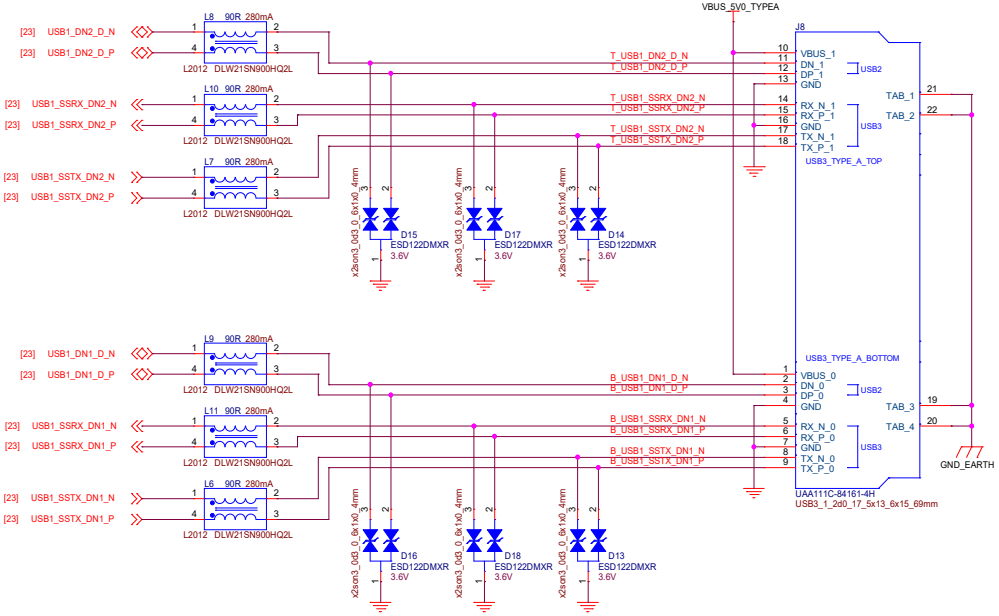
seeed The IoT Hardware Enabler	https://www.seeedstudio.com		
	Title: BeagleBone AI -64		
Size: C	Document Number: 23. USB 3.0 HUB		Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021		Sheet: 23 of 34

TYPE-C USB 3.0 Sink Application (UFP) Default

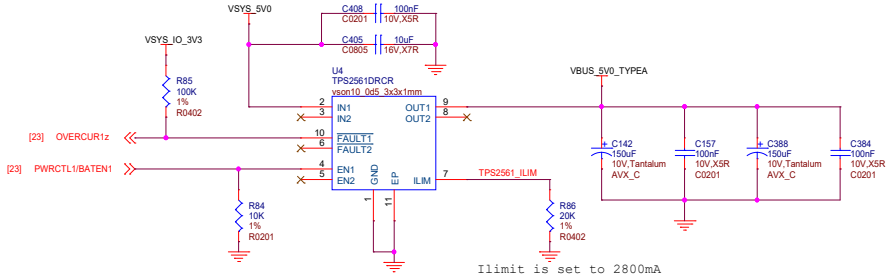








USB 3.0 DUAL TYPE-A



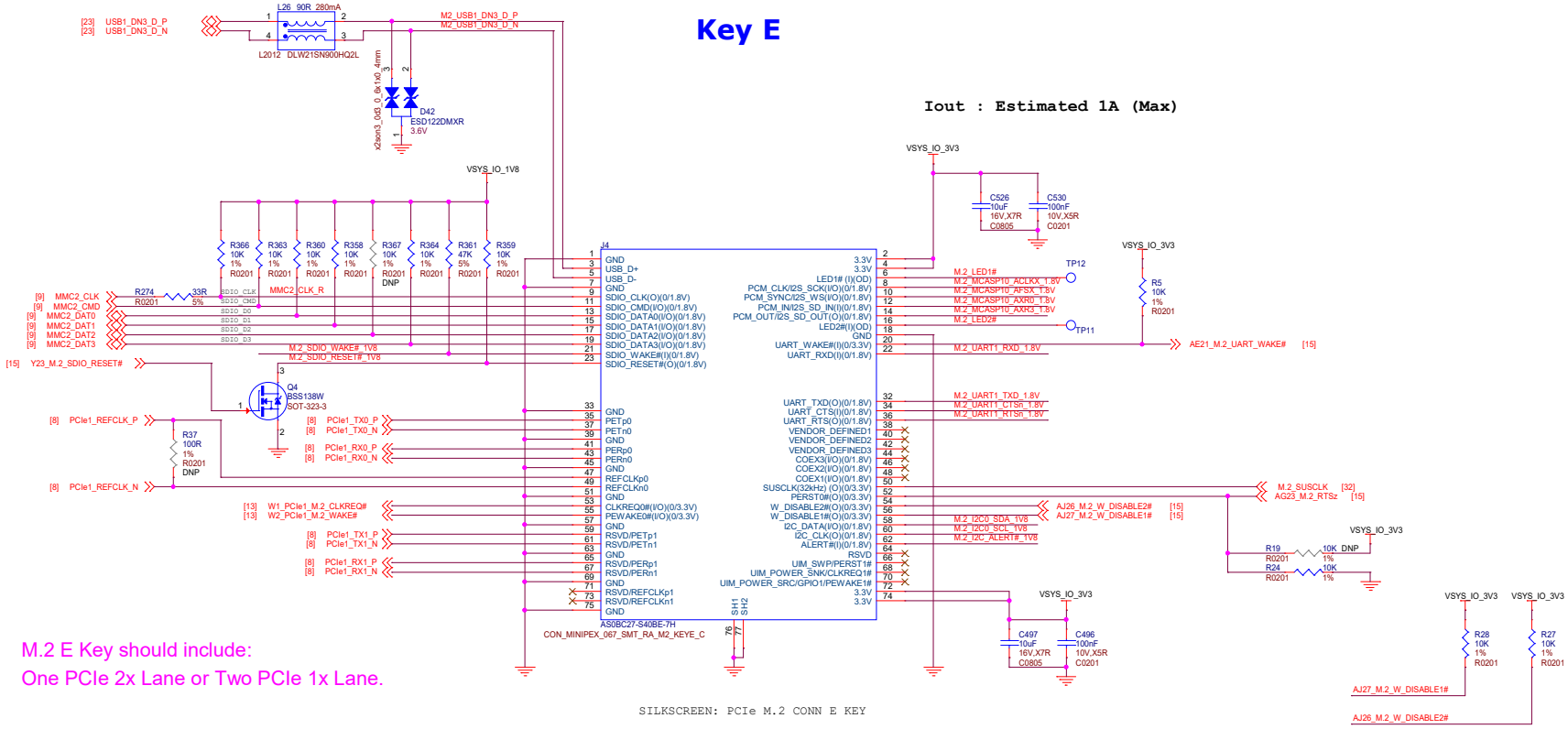
Review Note: C138=C119=100uF can or may be replaced by 150uF AVX_TLJB157M010R0500.

seeed The IoT Hardware Enabler	https://www.seeedstudio.com		
	Title: BeagleBone AI -64		
Size: C	Document Number: 24. USB 3.0 TYPE A, TYPE C		Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021		Sheet: 24 of 34

PCIe_M.2_INTERFACE - SDIO

Key E

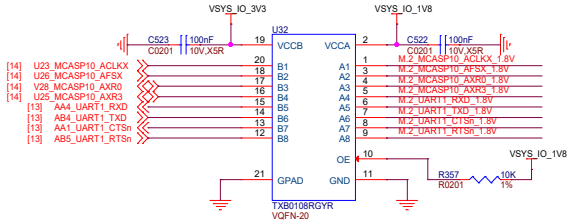
Iout : Estimated 1A (Max)



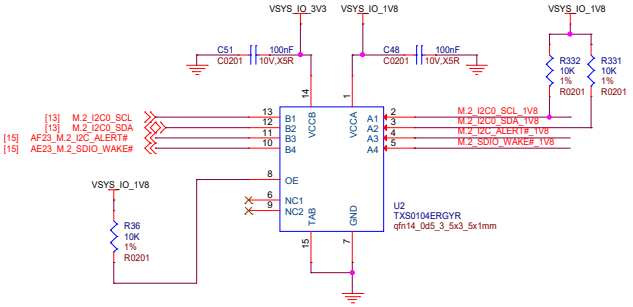
M.2 E Key should include:
One PCIe 2x Lane or Two PCIe 1x Lane.

SILKSCREEN: PCIe M.2 CONN E KEY

3.3V To 1V8 Level translator



3.3V To 1V8 Level translator



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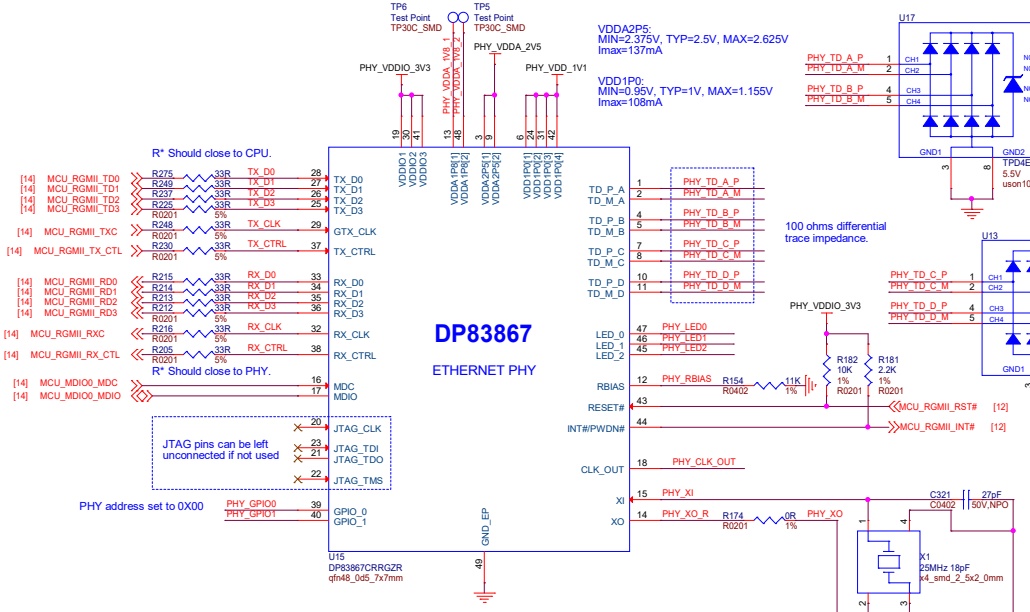
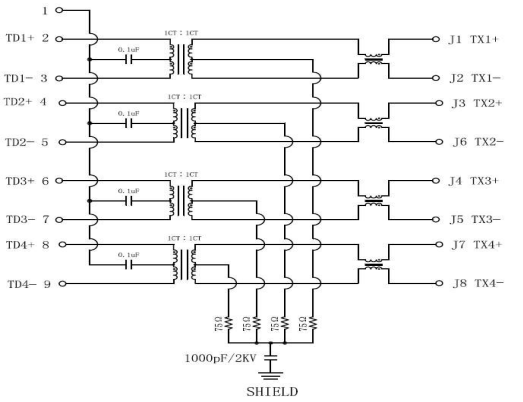
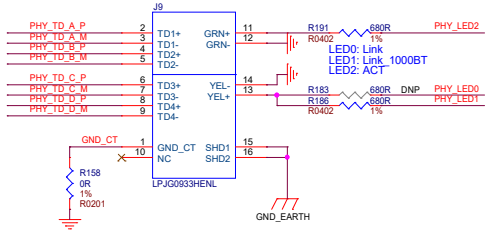
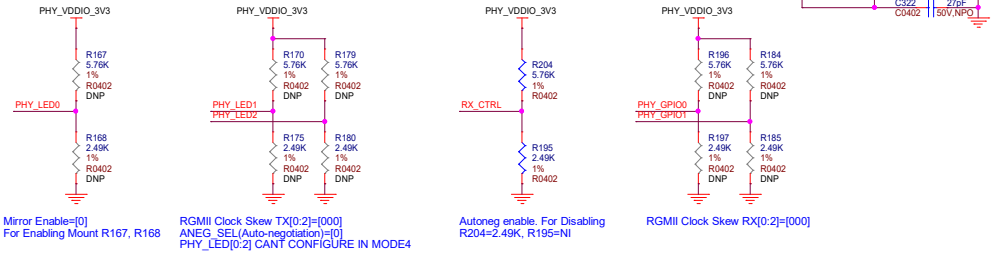
	Title: BeagleBone AI -64	
Size: C	Document Number: 25. PCIe_M.2_Key E	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 25 of 34

GB ETHERNET



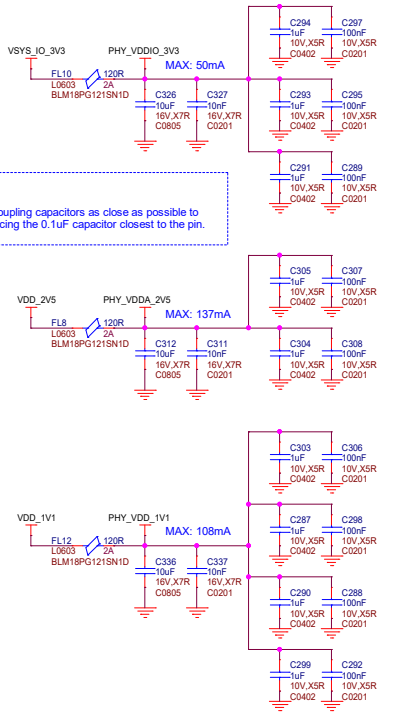






Layout Note:

Place 1uF and 0.1uF decoupling capacitors as close as possible to component VDD pins, placing the 0.1uF capacitor closest to the pin.

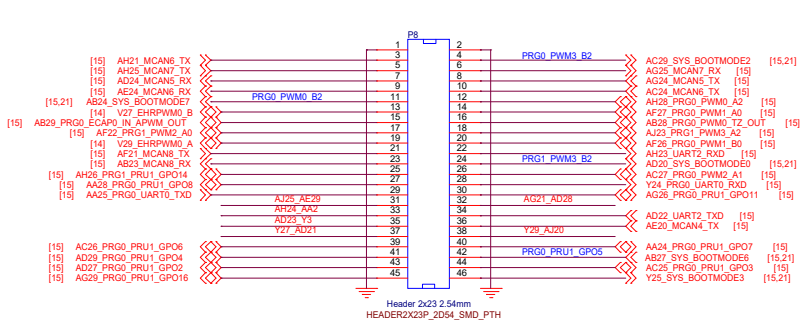


Review Note:

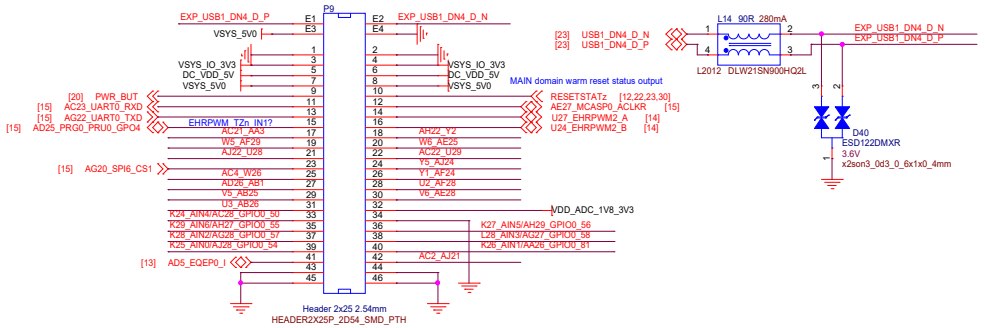
These test points are used for TI testing only!

PHY_CLK_OUT	R386 0201	33R 5%	PHY_CLK_OUT_TP	TP1 Test Point TP30C_SMD
PHY_GPIO0	R387 0201	33R 5%	PHY_GPIO0_TP	TP17 Test Point TP30C_SMD
PHY_GPIO1	R388 0201	33R 5%	PHY_GPIO1_TP	TP18 Test Point TP30C_SMD
PHY_LED0	R389 0201	33R 5%	PHY_LED0_TP	TP19 Test Point TP30C_SMD
PHY_LED1	R390 0201	33R 5%	PHY_LED1_TP	TP20 Test Point TP30C_SMD
PHY_LED2	R391 0201	33R 5%	PHY_LED2_TP	TP21 Test Point TP30C_SMD

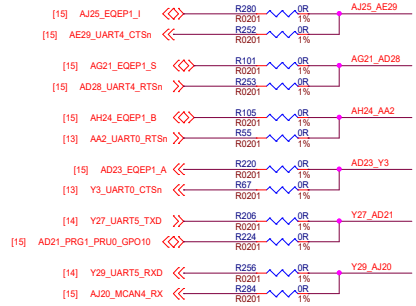
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI -64	
Size: C	Document Number: 26. MCU GB ETHERNET	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 26 of 34



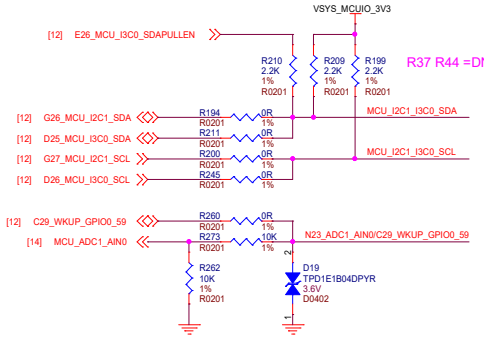
EXPANSION HEADER P8



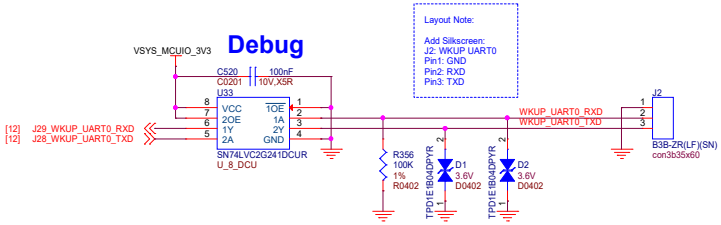
EXPANSION HEADER P9



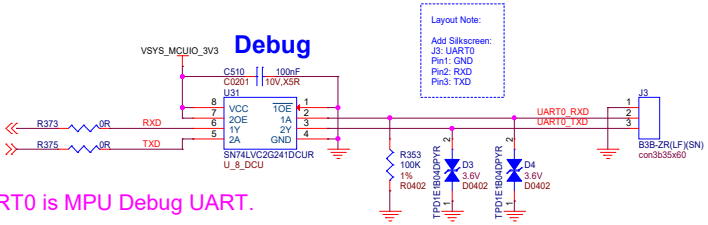
MCU mikroBUS Header



Debug



Debug



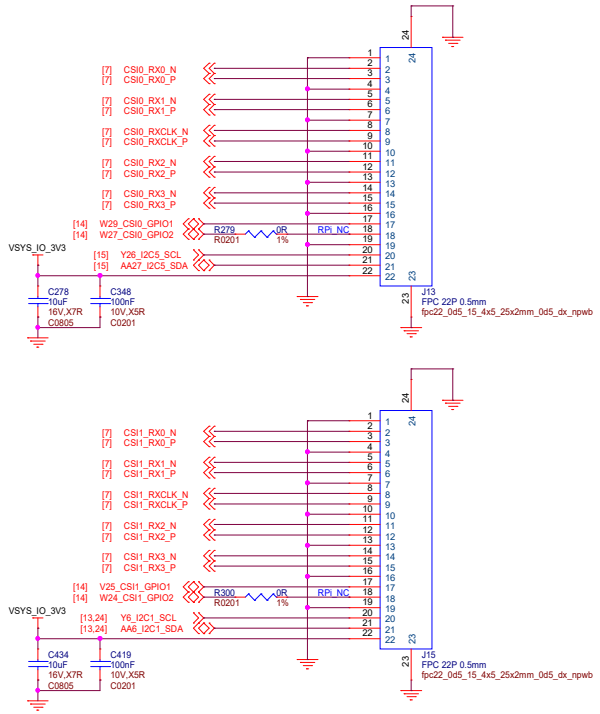
UART0 is MPU Debug UART.

seeed The IoT Hardware Enabler	https://www.seeedstudio.com		
	Title: BeagleBone AI -64		
Size: C	Document Number: 27. P8 P9, mikroBUS Header		Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 27 of 34	

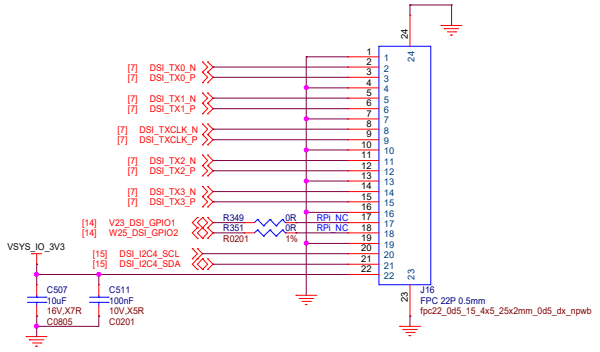
NOTE:
The RPi camera connector is 3.3V only (GPIO and IIC)!

80	SCL0	IIC Clock pin (Raspberry Pi GPIO45) Typically used for Camera and Displays Internal 1.8K pull up to `CM4_3.3V`
81	+5V (Input)	4.75V-5.25V Main power input
82	SDA0	IIC Data pin (Raspberry Pi GPIO44) Typically used for Camera and Displays Internal 1.8K pull up to `CM4_3.3V`
97	Camera_GPIO	Typically used to Shutdown the camera to reduce power. Reassigning this pin to another function isn't recommended. `CM4_3.3V` signalling

Raspberry Pi Camera Connector x4 Lane

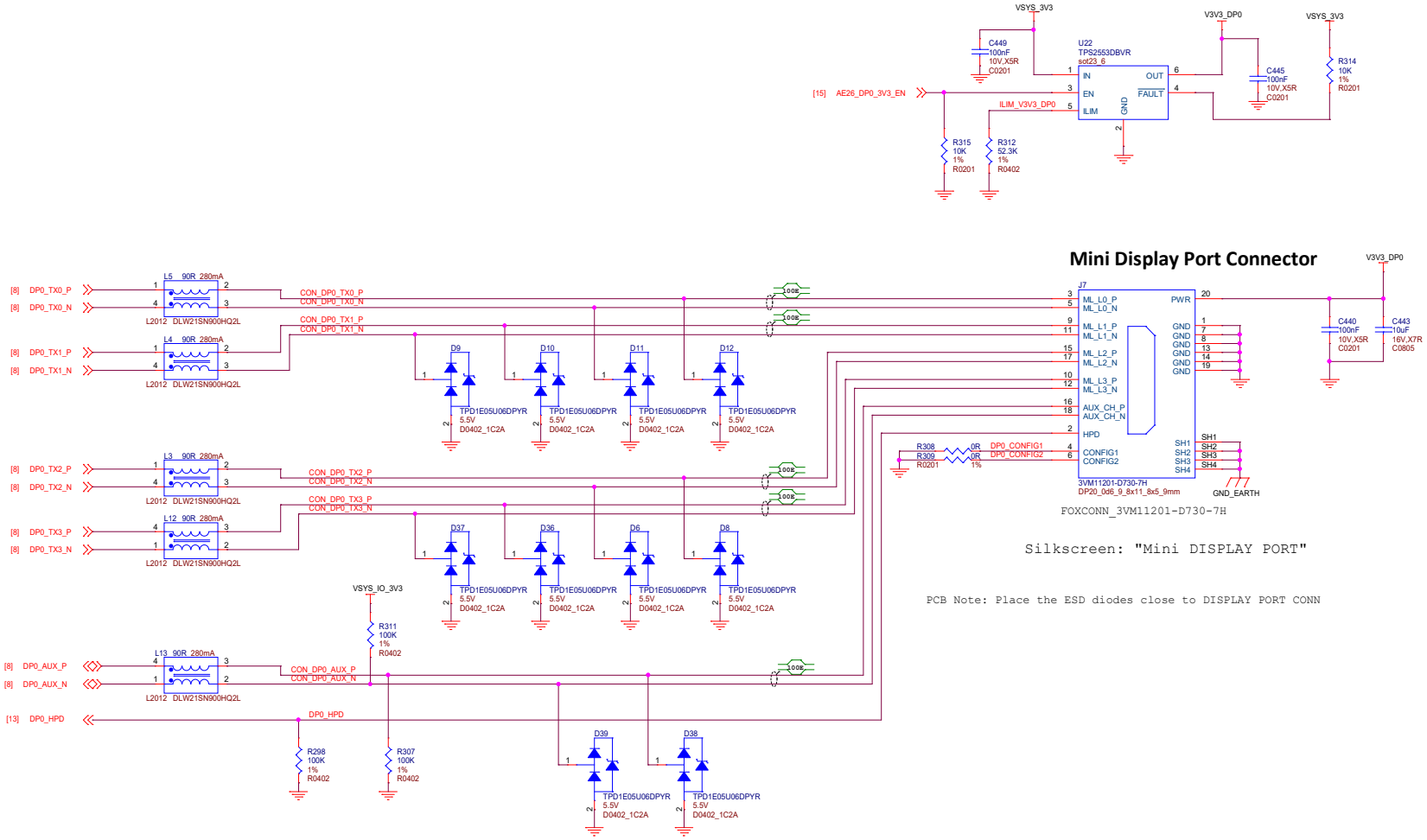


Raspberry Pi Display Connector x4 Lane



seeed The IoT Hardware Enabler	https://www.seeedstudio.com		
	Title: BeagleBone AI -64		
Size: C	Document Number: 28. Raspberry Pi CSI DSI		Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021		Sheet: 28 of 34

Mini DISPLAY PORT INTERFACE

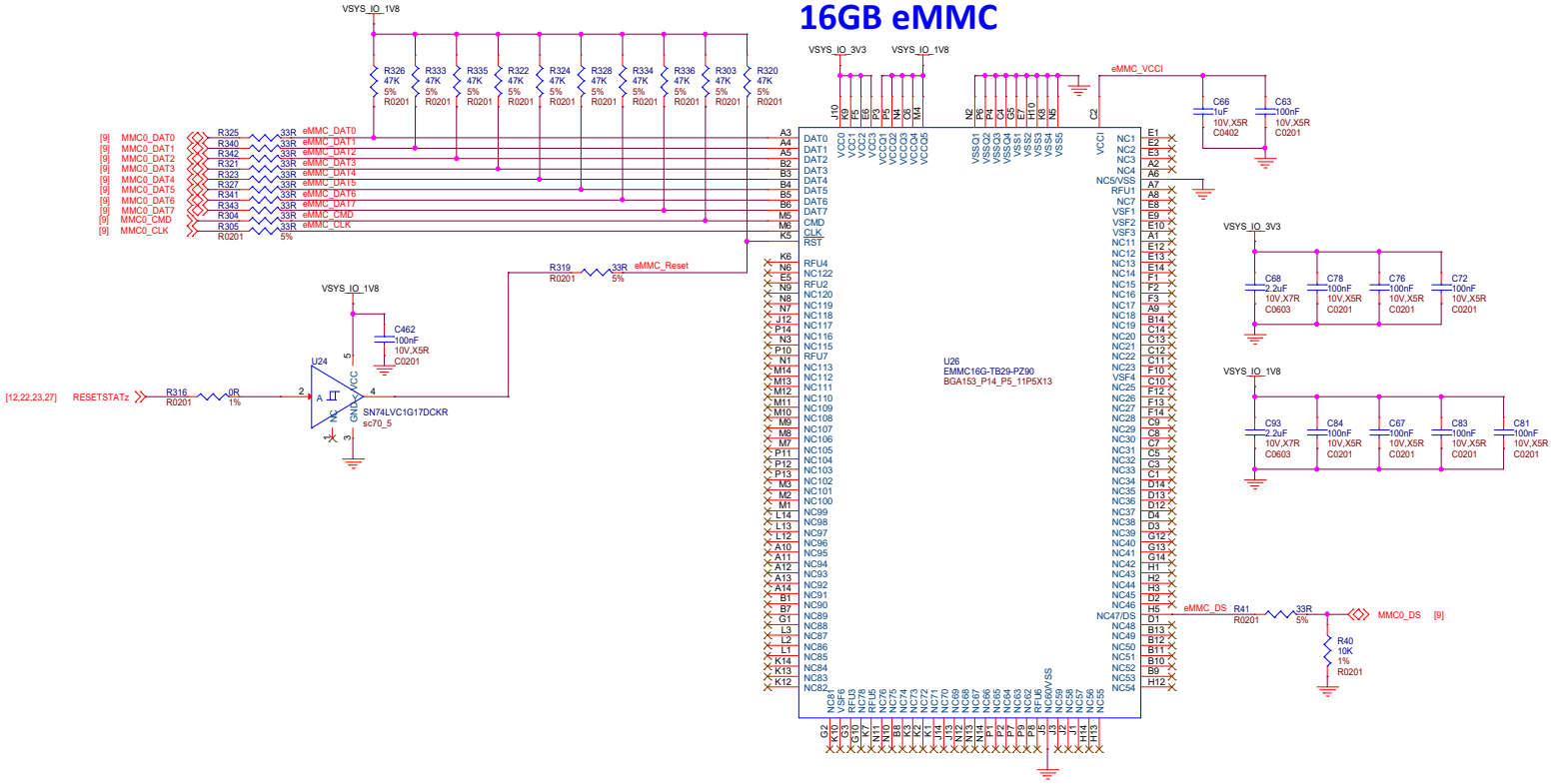


Silkscreen: "Mini DISPLAY PORT"

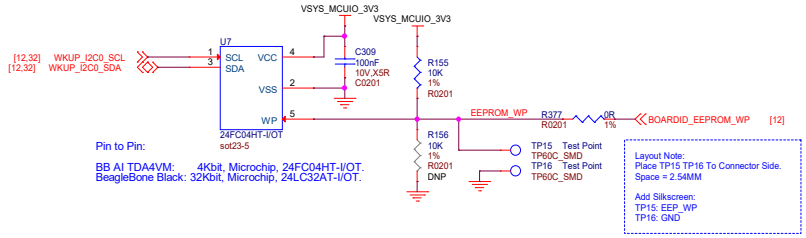
PCB Note: Place the ESD diodes close to DISPLAY PORT CONN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI -64	
Size: C	Document Number: 29. DISPLAY PORT	Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021	Sheet: 29 of 34

16GB eMMC



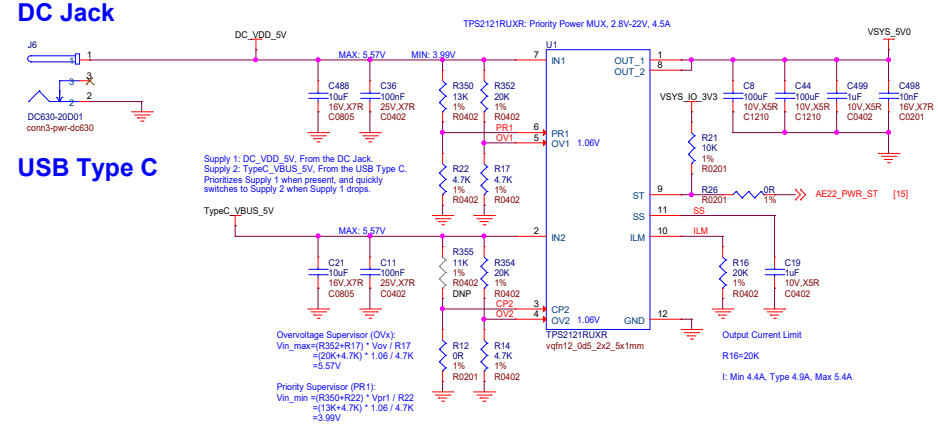
BOARD ID EEPROM 4Kbit



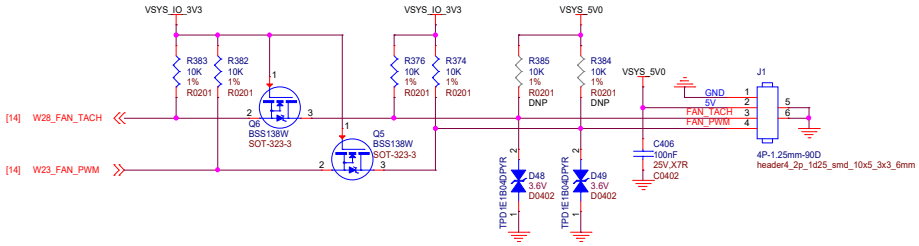
seeed The IoT Hardware Enabler	https://www.seeedstudio.com		
	Title: BeagleBone AI -64		
Size: C	Document Number: 30. eMMC, EEPROM		Rev: V1.02
Draw By: Junqing.Xin	Date: Friday, November 19, 2021		Sheet: 30 of 34

DC Jack

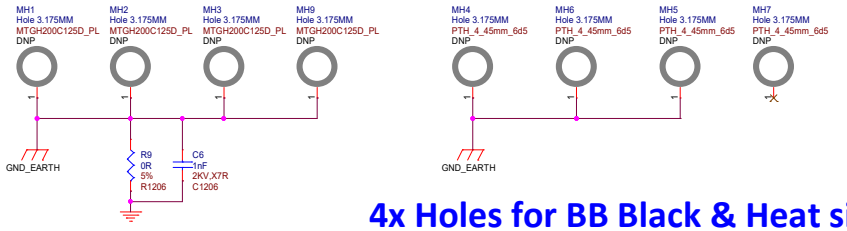
USB Type C



FAN HEADER

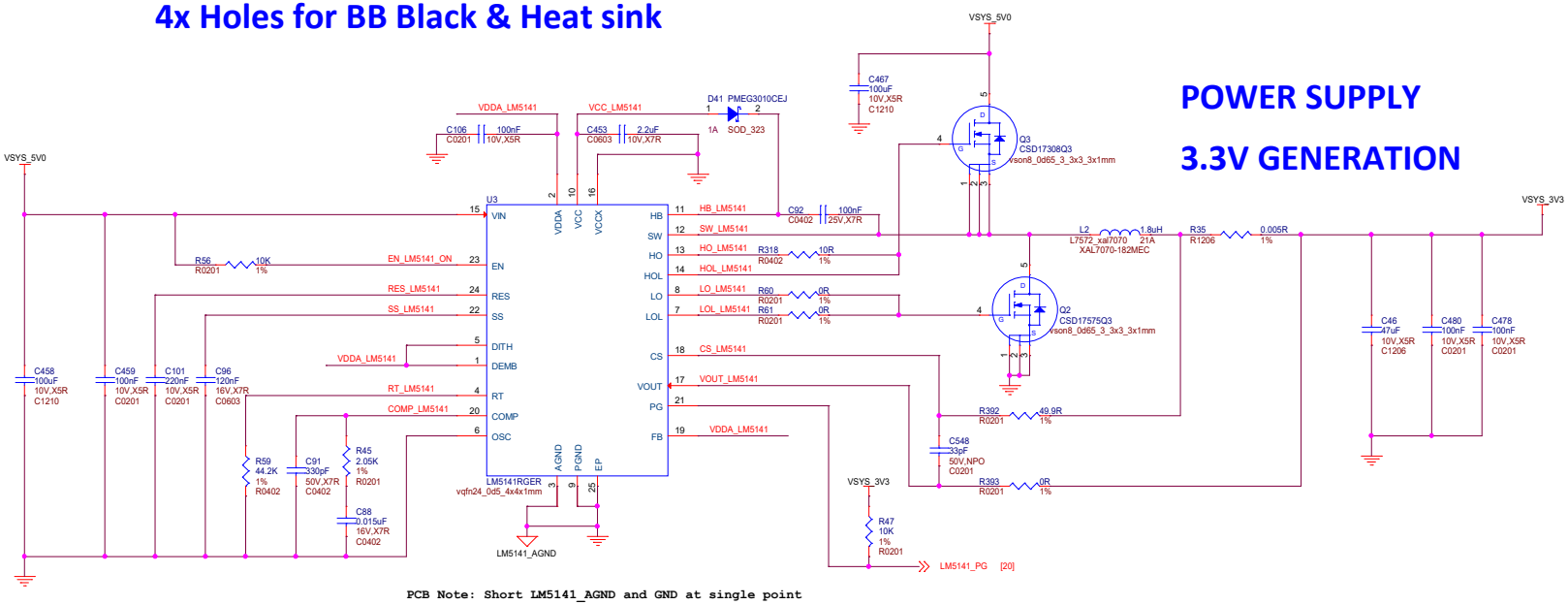


4x Holes for BB Black & Heat sink



POWER SUPPLY

3.3V GENERATION



PCB Note: Short LM5141_AGND and GND at single point

TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 5.5V
Vout1 = 3.3V@8A
Ta = 25 deg

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EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)

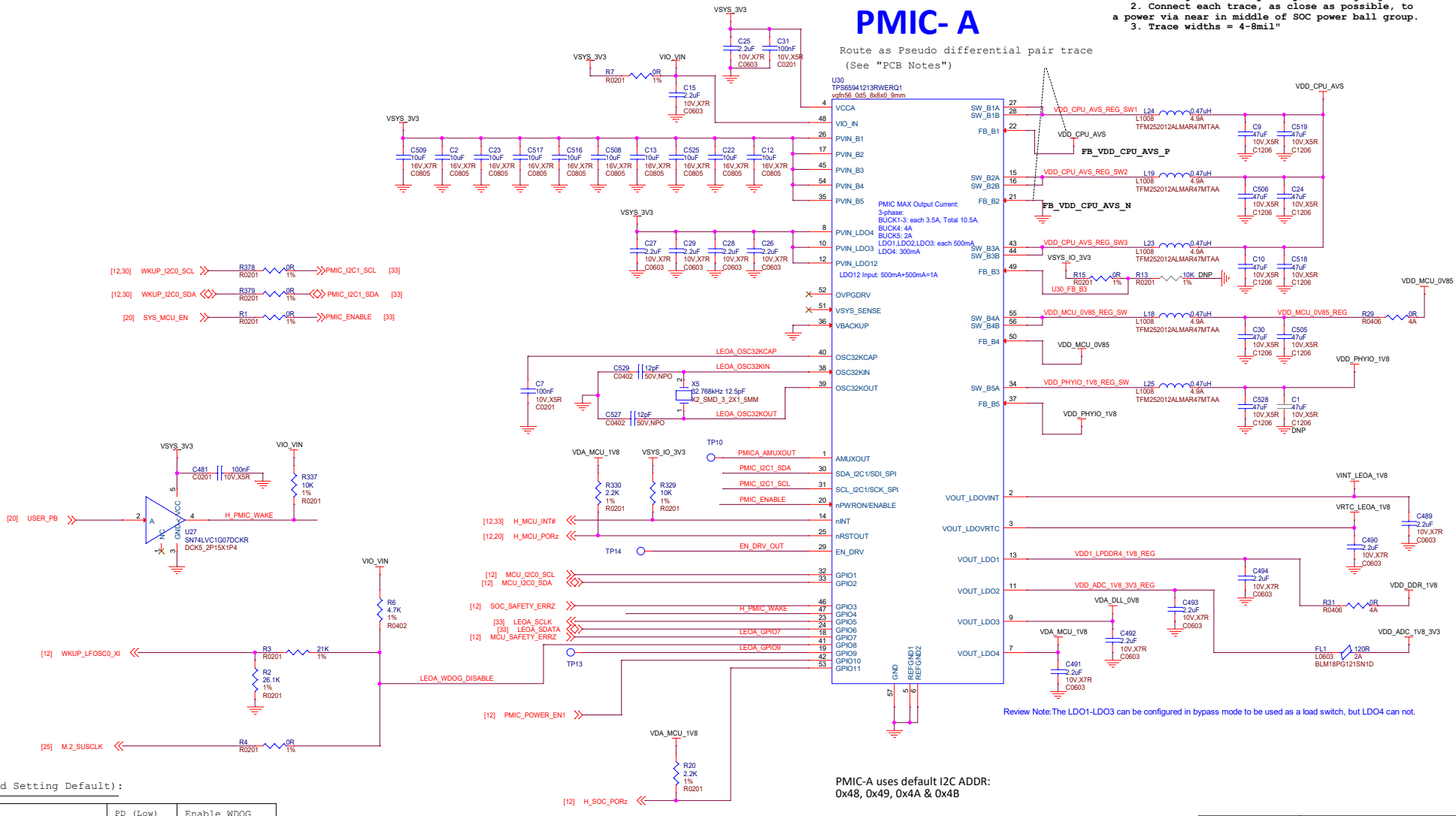
(3-Phase Buck supplying VDD_CPU)

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC- A

Route as Pseudo differential pair trace
(See "PCB Notes")



PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

(EVM Bd Setting Default):

LEOA_WDOG_DISABLE	PD (Low)	Enable WDOG
	PU (High)	Disable WDOG

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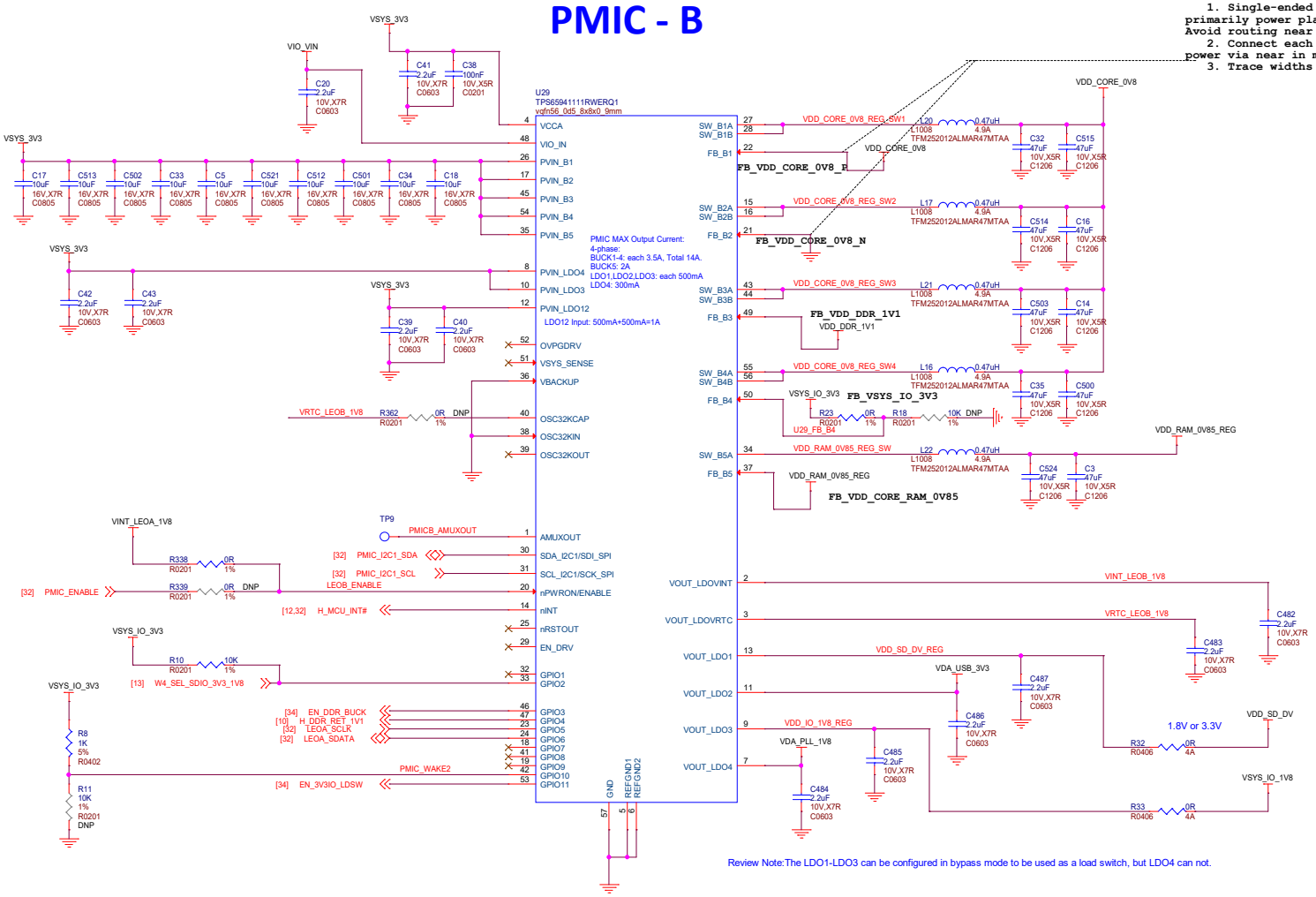
PMIC - B

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

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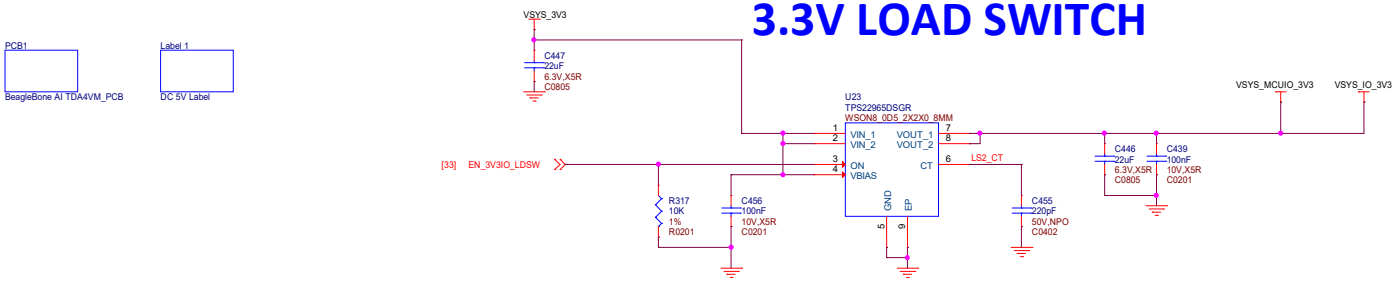
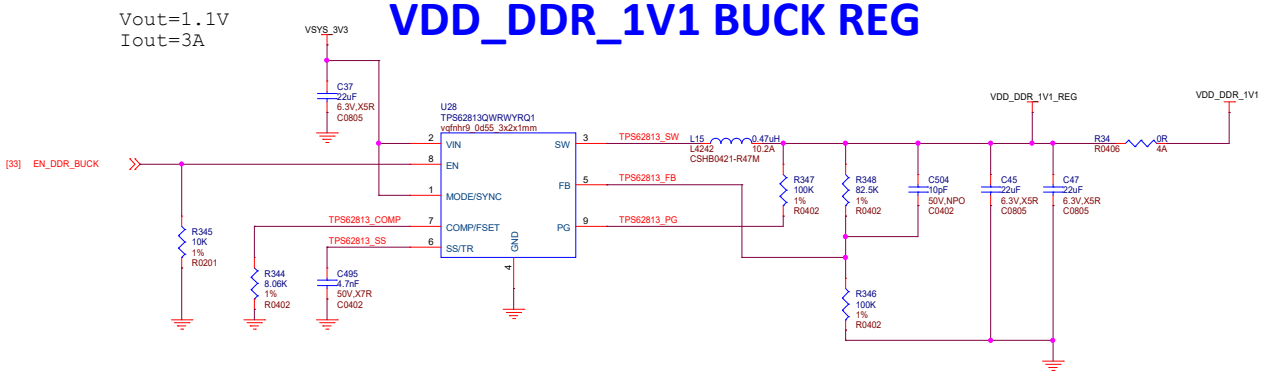
3.3V LOAD SWITCH

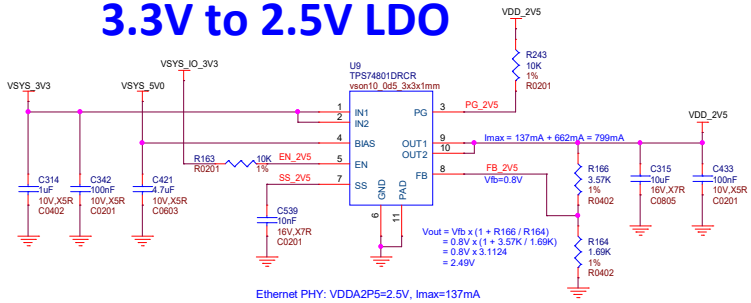


VDD_DDR_1V1 BUCK REG



ETHERNET POWER

3.3V to 2.5V LDO



Ethernet PHY: VDDA2P5=2.5V, Imax=137mA

LDO U18 Power In=2.5V, Imax=662mA

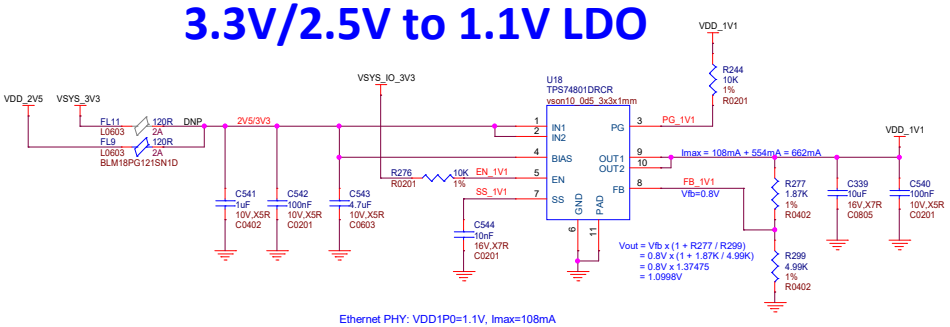
Total: Imax= 137mA + 662mA = 799mA

Power Consumption: (3.3V-2.5V) * 0.799A = 0.6392W

Thermal Junction-to-ambient: 0.6392W * 44.2°C/W=28.25°C

USB3.0 HUB & ETHERNET POWER

3.3V/2.5V to 1.1V LDO



Ethernet PHY: VDD1P0=1.1V, Imax=108mA

USB3.0 HUB: VDD=1.1V, Imax=554mA

Total: Imax = 108mA + 554mA = 662mA

Power Consumption: (2.5V-1.1V) * 0.662A = 0.9268W

Thermal Junction-to-ambient: 0.9268W * 44.2°C/W=40.96°C

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