BeagleBone AI -64

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REVISION HISTORY

DATE	REVISION	DESCRIPTION OF CHANGES	AUTHOR
21 Dec 2021	BeagleBone AI-64_SCH_Rev B_211221	1. Initial Production Release, 425PCS PCBA. 2. The PCB Revision for this board is Rev B.	Junqing.Xin
02 Jun 2022	BeagleBone AI-64_SCH_Rev B1_220602	1. There is no changes in SCH, but only updated the PCB Footprint for production. 2. The PCB Revision for this board is Rev B1.	Junqing.Xin

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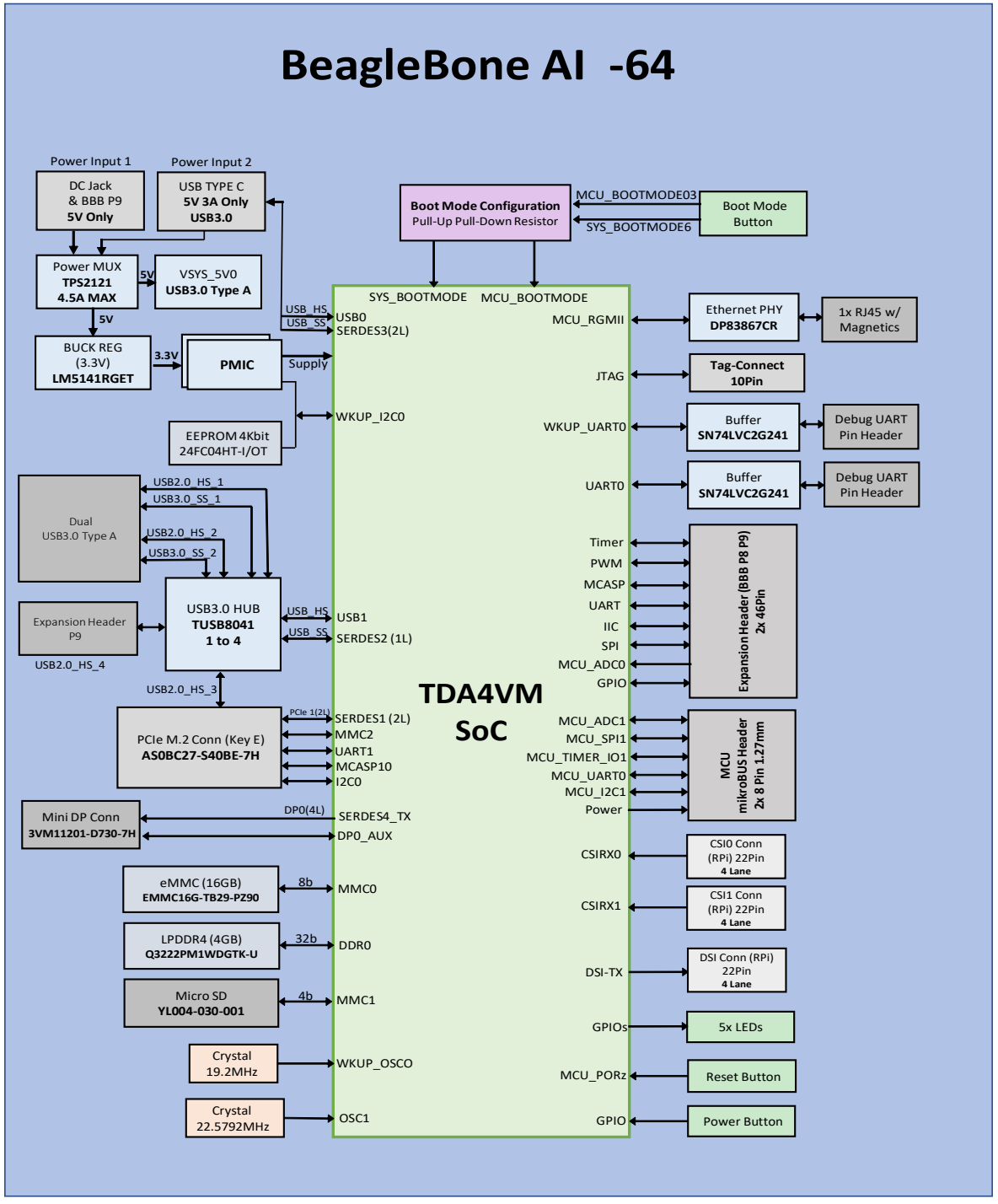
SYSTEM BLOCK DIAGRAM



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3-Phase DUAL PMIC PDN Recommended for New Designs
(3-Phase Buck supplying VDD_CPU)

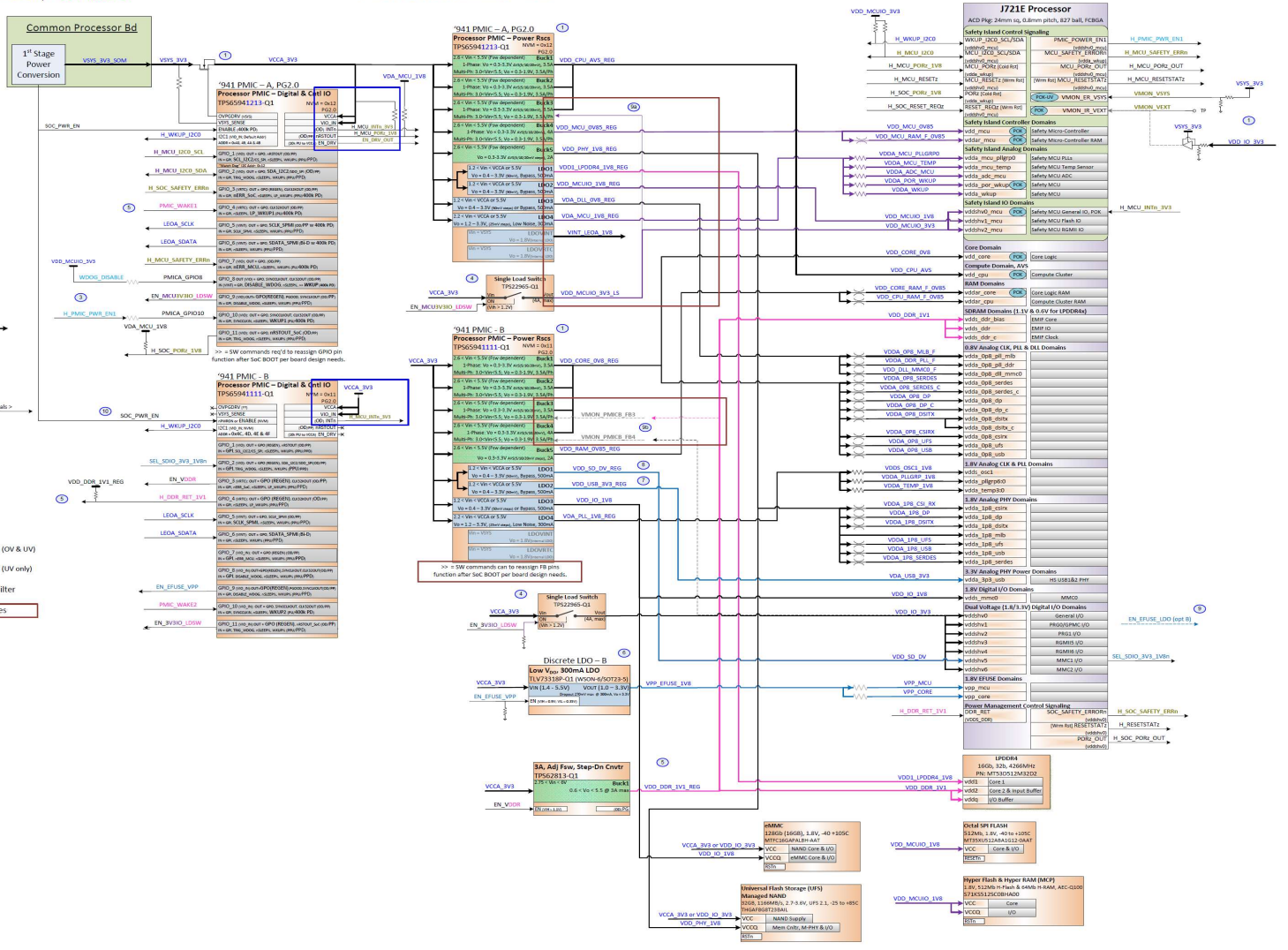
DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0C
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594**1213**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **13**, PG2.0)
Leo PMIC-B, PN TPS6594**1111**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **12**, PG2.0)

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable system with independent MCU & Main power for FFI
3. SDRAM: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
5. Low power modes: MCU Only & DDR Retention
6. Signaling Levels: MCU & Main Dual VIO
7. End Product Options:
   a. Compliant high-speed SD Card
   b. Compliant USB 2.0 data eye
   c. HS SoC Efuse programming on-board

V0.14	1/27/2021	1. Added example of VDD_IO_3V3 OV/UV monitoring by SoC's VMON_IR_VEXT input connection option to voltage buffer & voltage R-div needed to interface with SoC's internal R-div network optimized for monitoring 1.8V power rails. 2. Added 2x ext voltage monitoring inputs options for OV/UV monitoring by Hera PMIC of any safety critical system power rails. Hera's quad buck config can reassign remote sense feedback inputs (FB3 & FB4) for power rail monitoring. 3. Updated notes 1 & 9 accordingly.
V0.15	2/13/2021	Following final PMIC NVM review for defining new common PN ("1213") for Leo PG2.0 used in PDN-0C & -1A: 1. Update notes 2. Changed PMIC-A FB3 VMON input to be connected to VCCA_3V3 since VDD_MCUIO_3V3 rail is not supported, see note 9a. 3. Added PMIC-B FB3 & FB4 assignment for VMON by SW after SoC boot for ext power rail monitoring options, see note 9b.
V0.16	3/2/2021	1. Removing discrete load switch from supplying PMIC's VIO_IN since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related "Note #2" has been removed.



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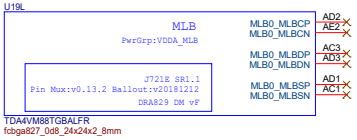
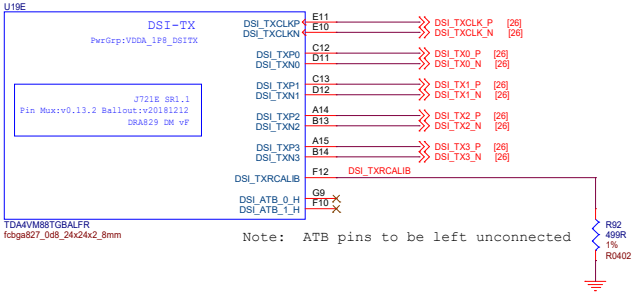
MLB

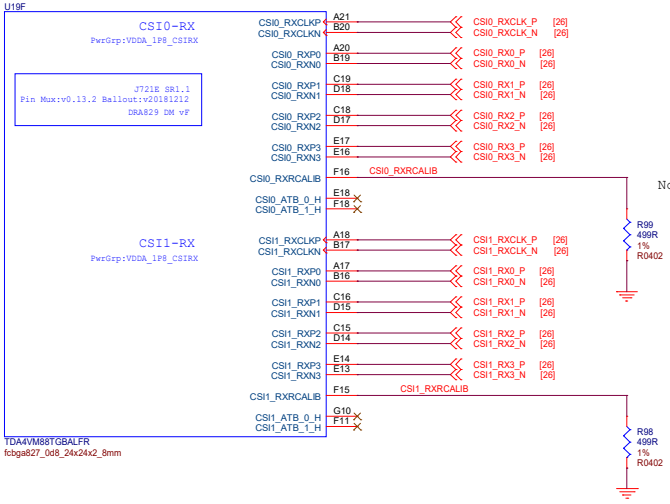


DSI



Note: ATB pins to be left unconnected

CSI Interface



Note: ATB pins to be left unconnected

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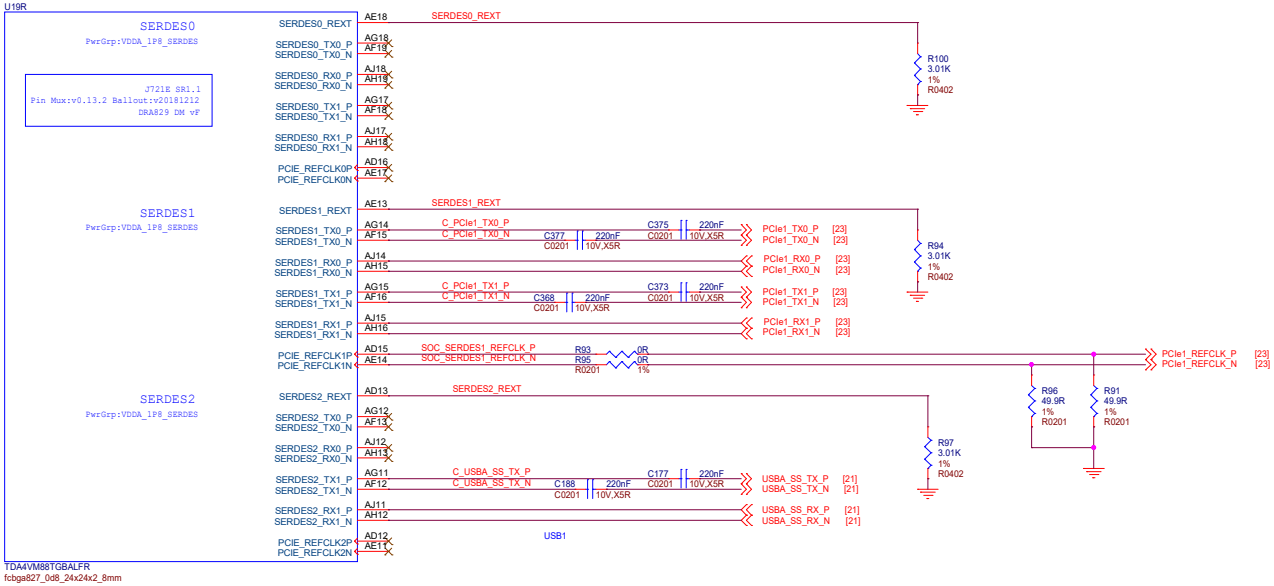
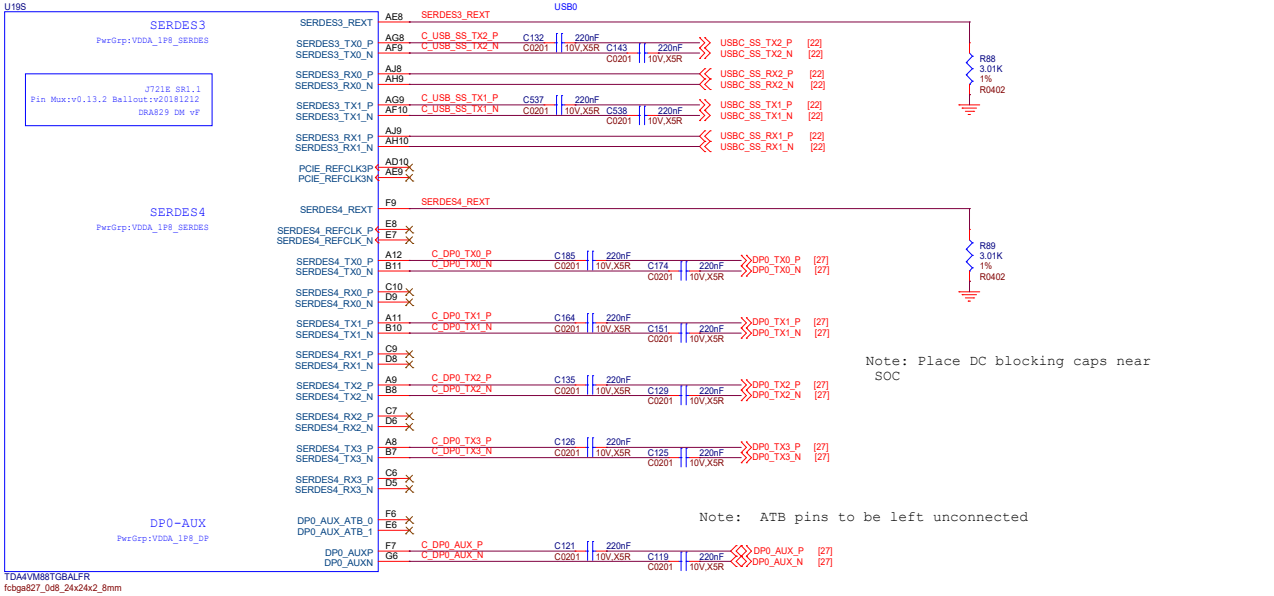
SERDES





Note: Place DC blocking caps near SOC

Note: ATB pins to be left unconnected

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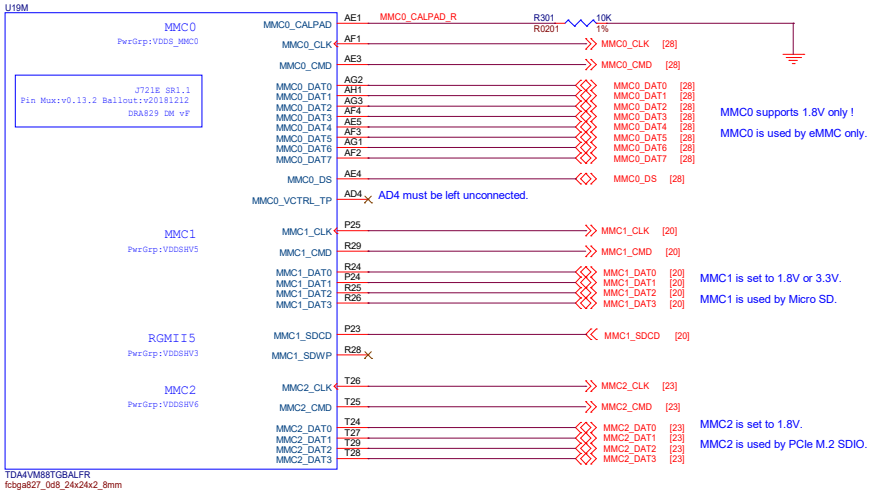
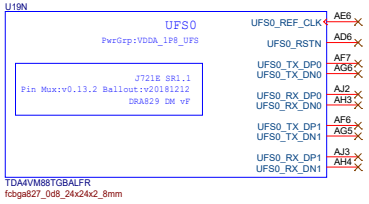
MMC Interface



UFS Interface



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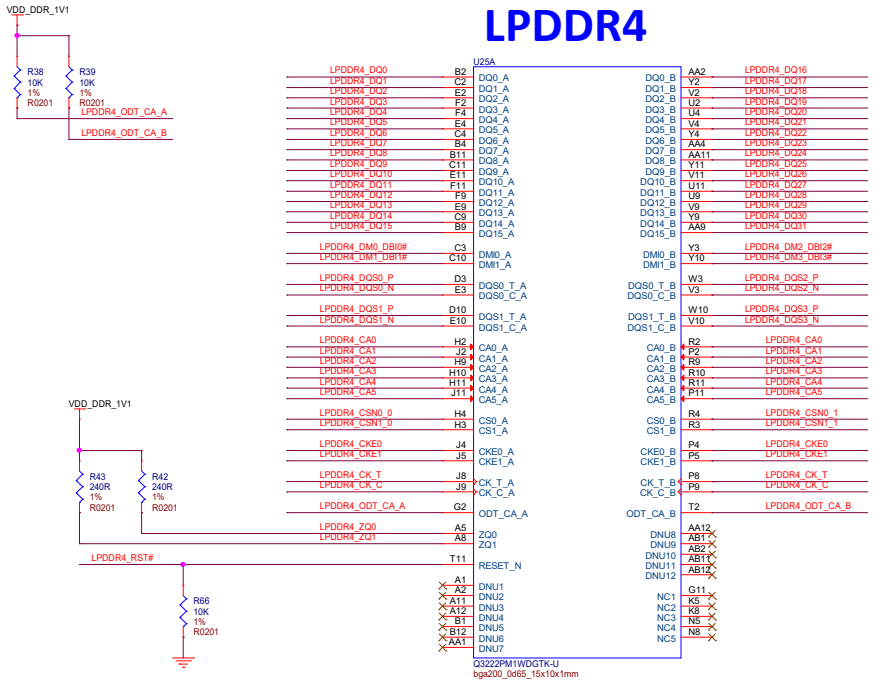
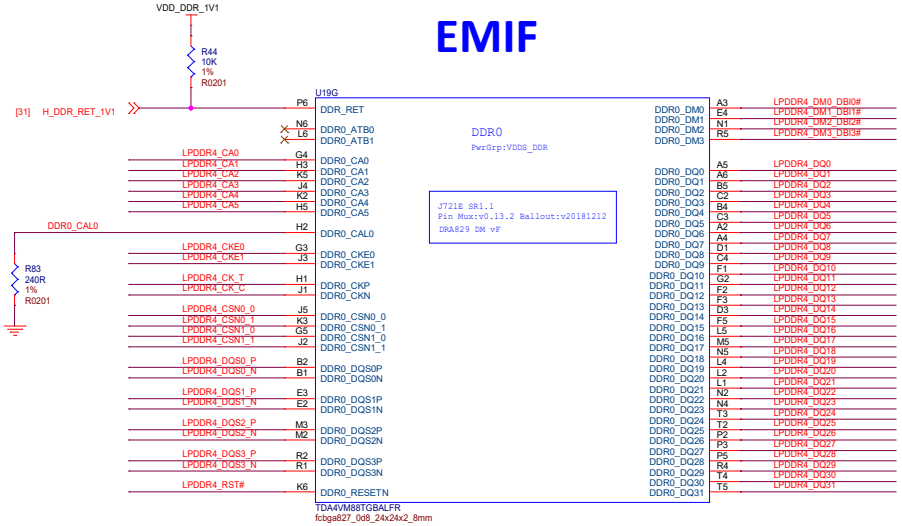
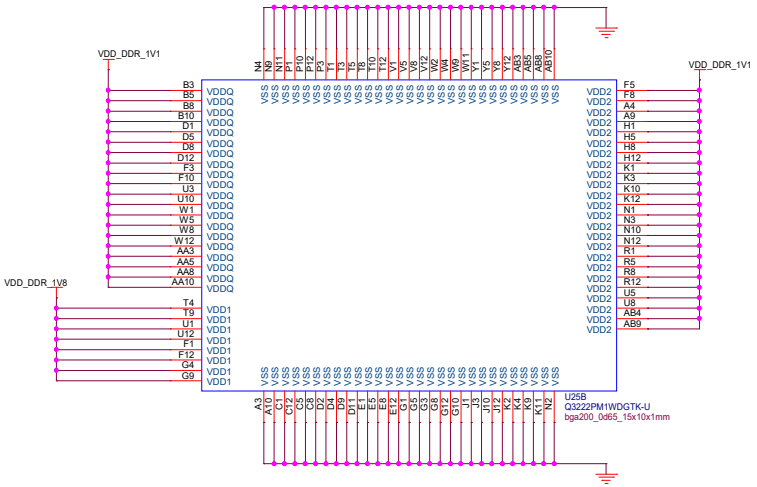
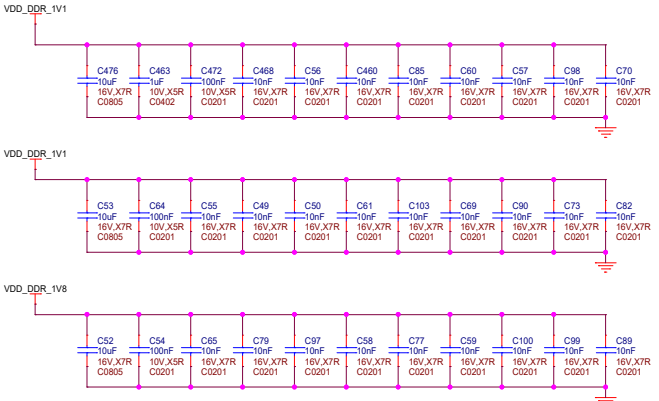
LPDDR4



EMIF







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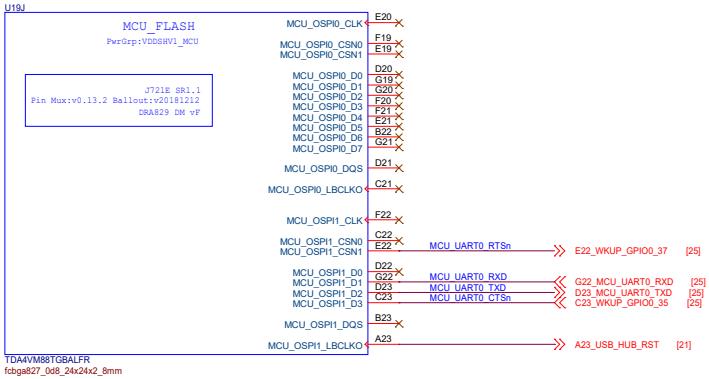
MCU OSPI



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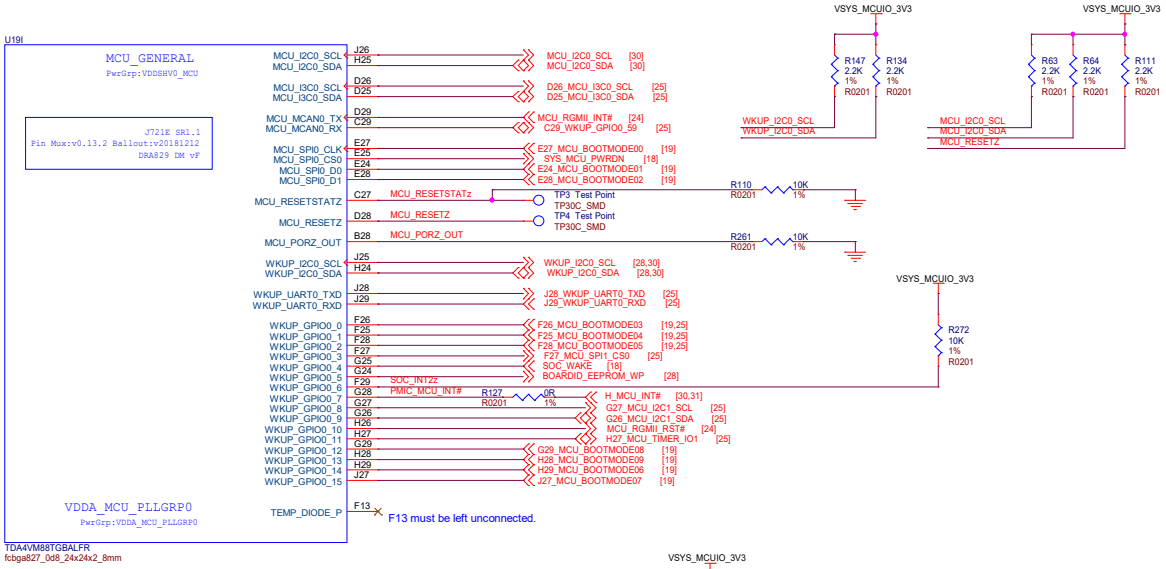
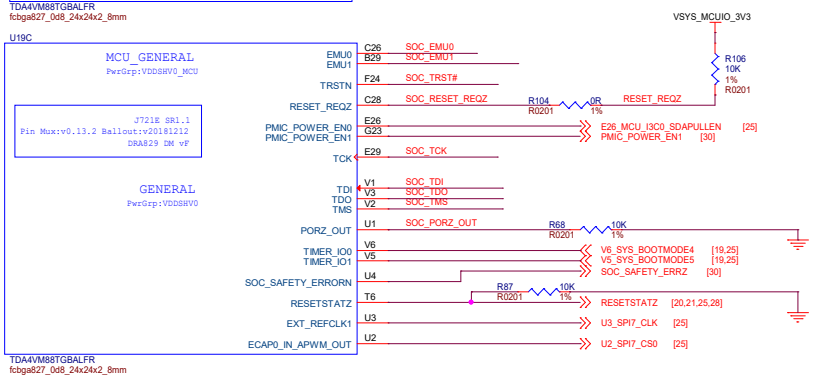
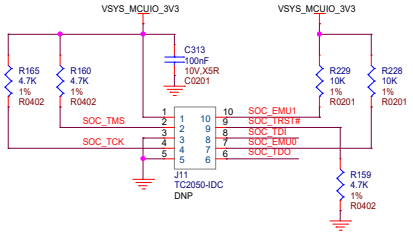
MCU & MAIN GENERAL IO, OSC CLKS

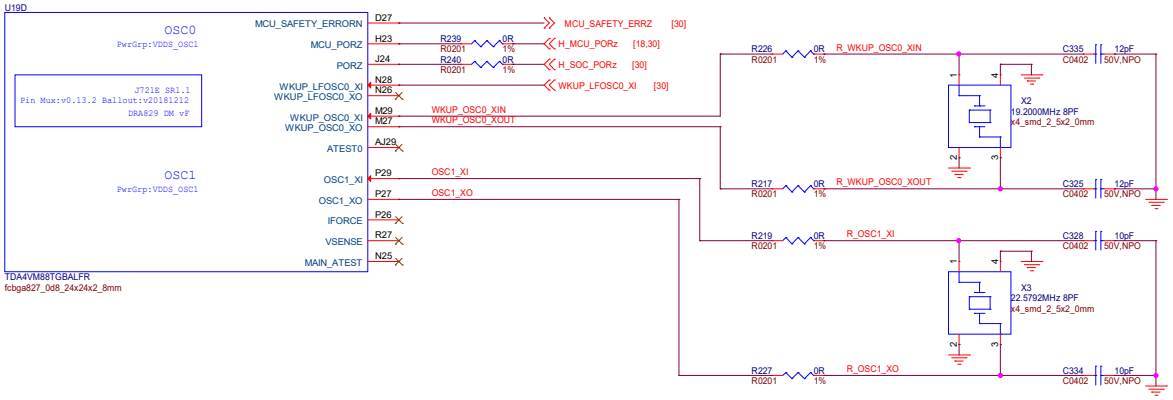




Tag-Connect



OSC



CLKS

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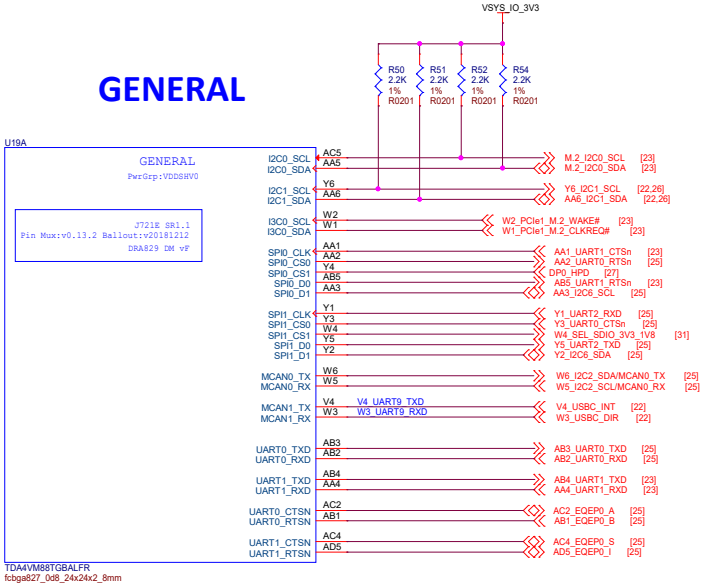
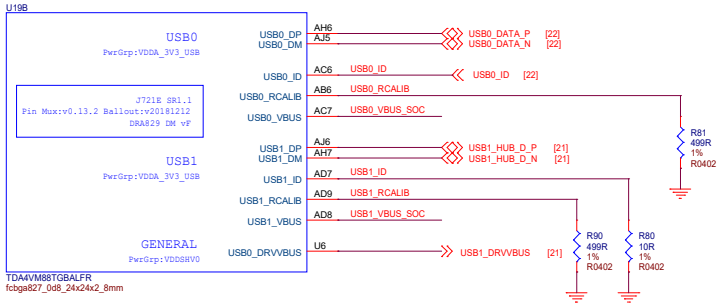
GENERAL



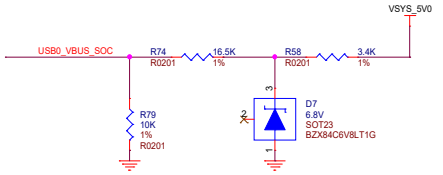
USB



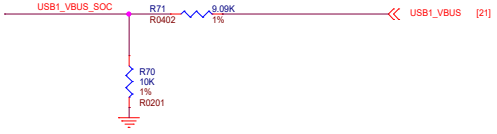
USB1_ID Pulled low. J7 SoC in Host Mode.

USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V VBUS



Note: Recommended VBUS circuit for embedded Hub



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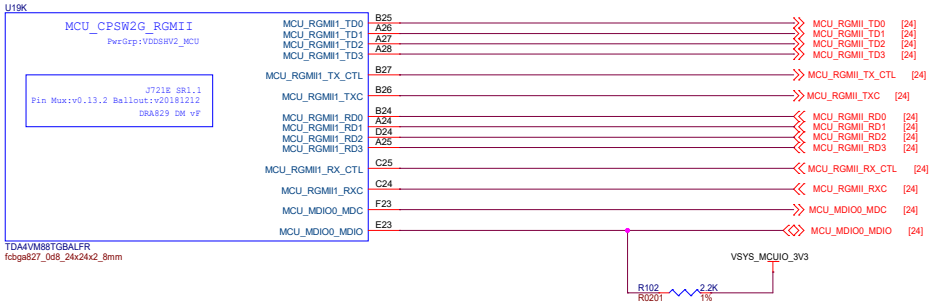
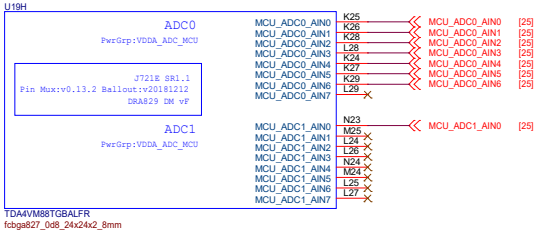
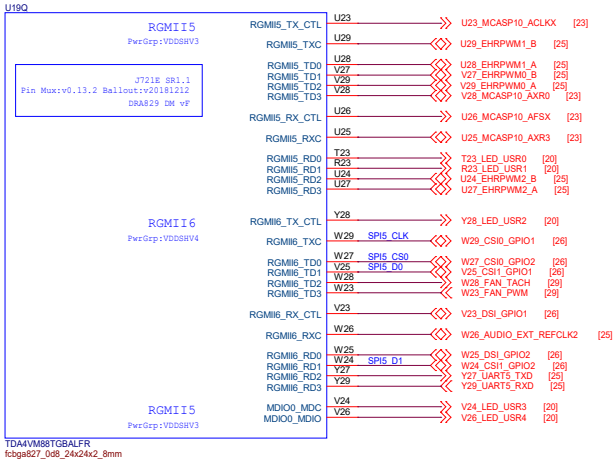
MCU_RGMII



MCU ADCs



MAIN RGMII



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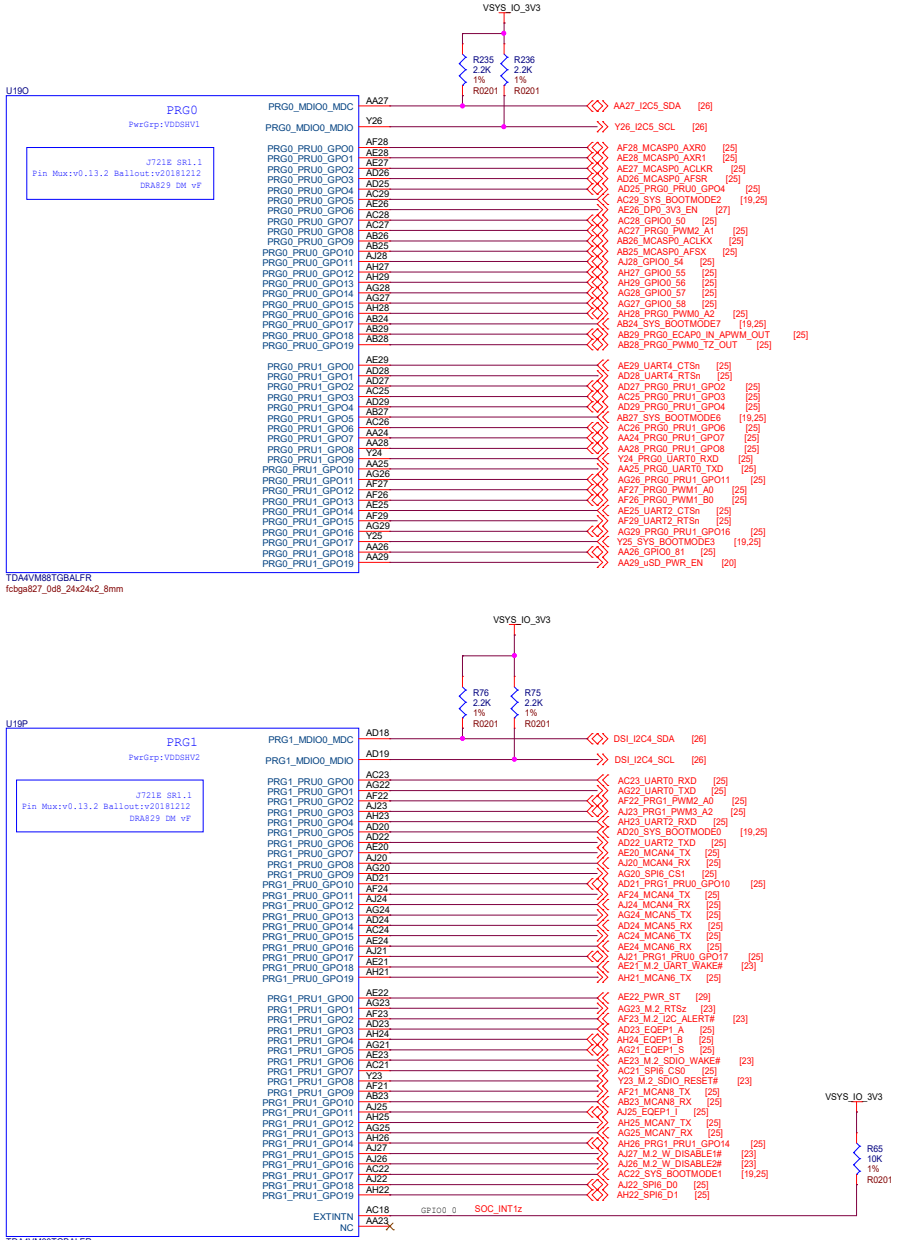
PRG0 & PRG1



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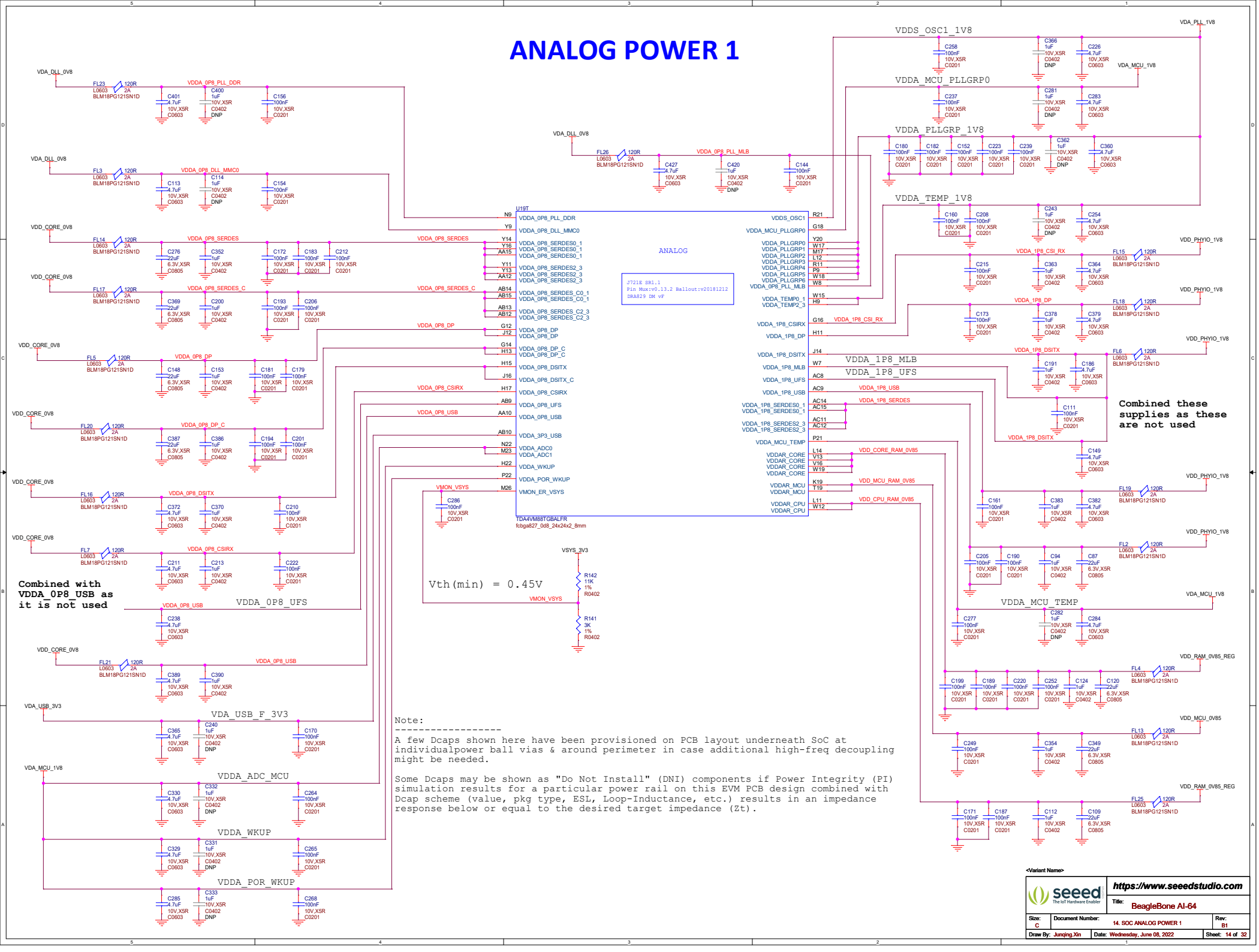
ANALOG POWER 1



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

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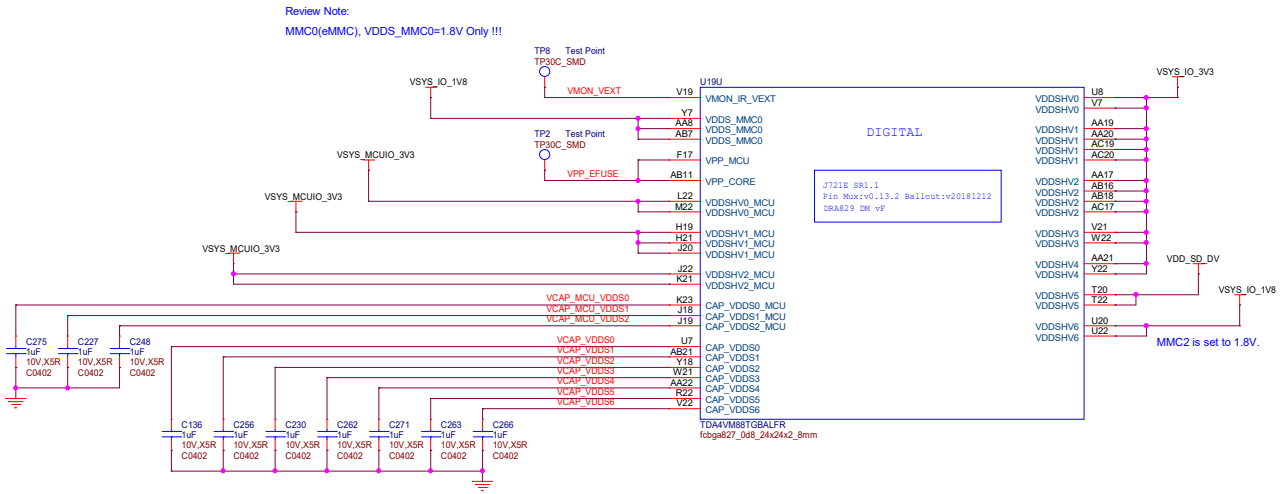
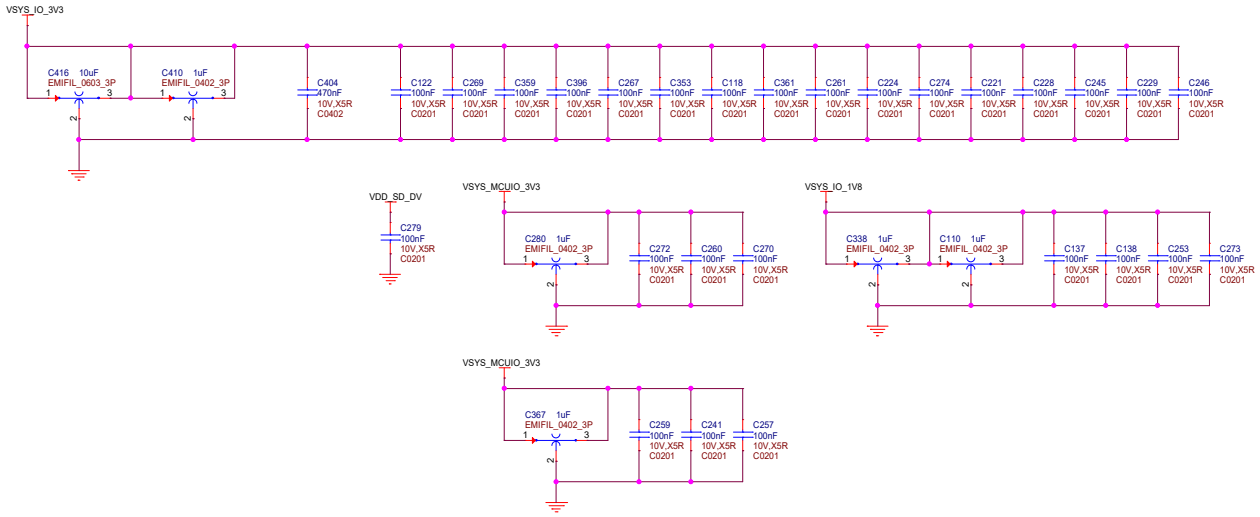
DIGITAL POWER 2





Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

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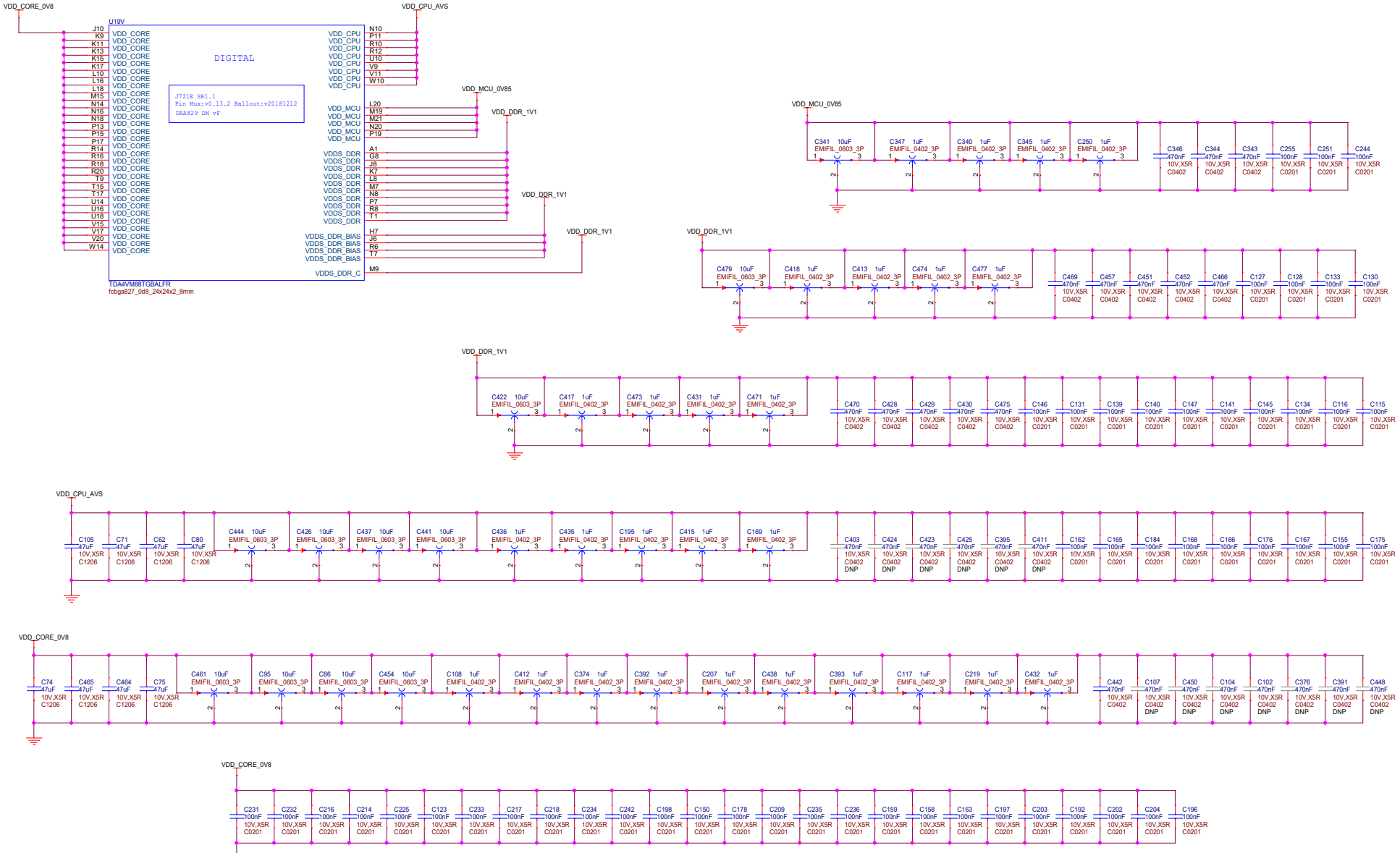
DIGITAL POWER 3



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

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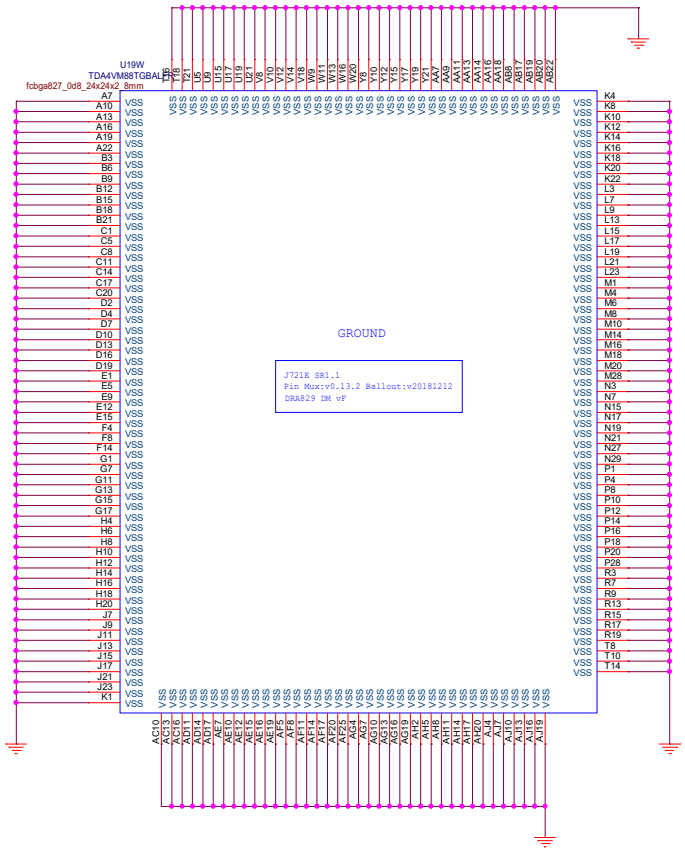
SOC GROUND



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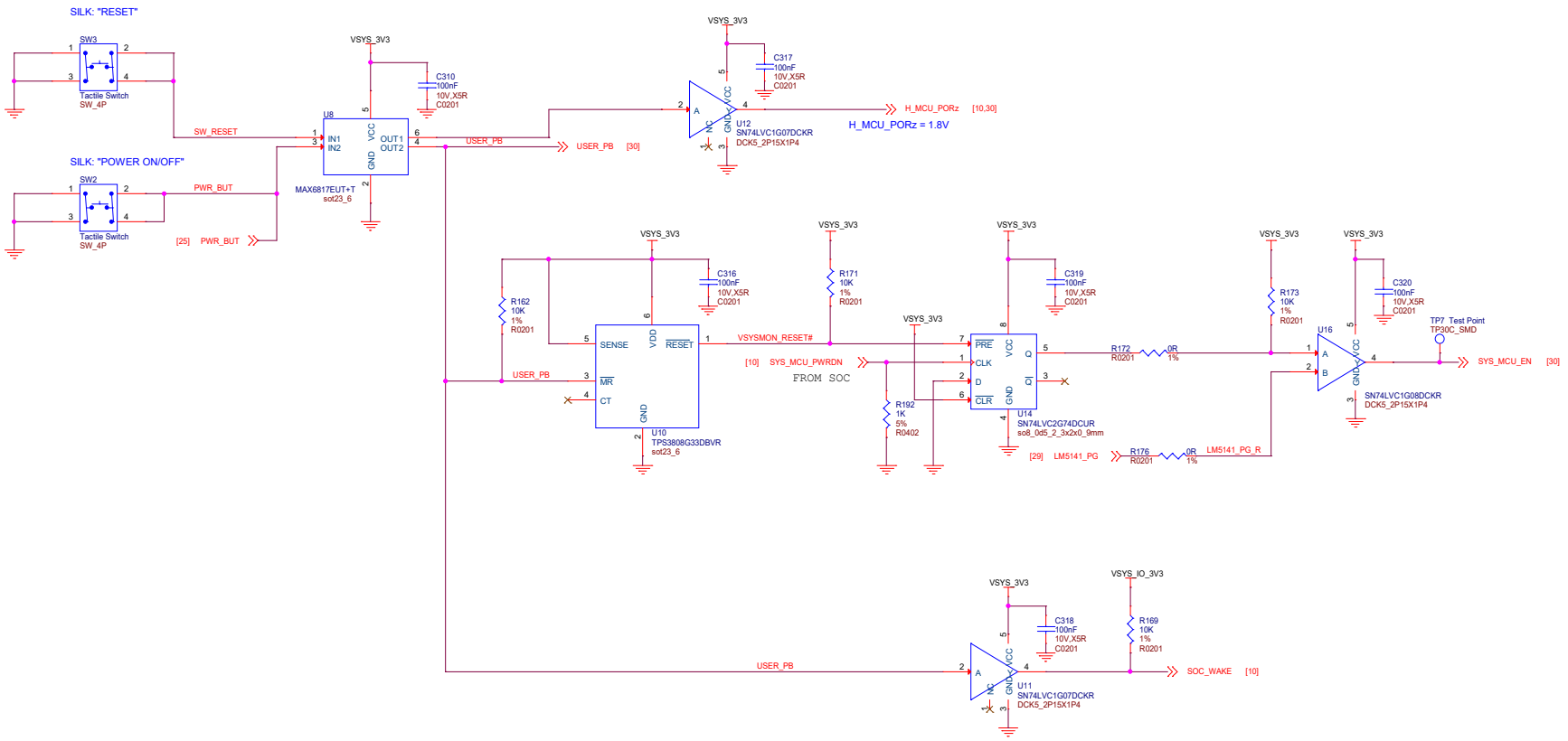
RESET, POWER ON/OFF BUTTONs



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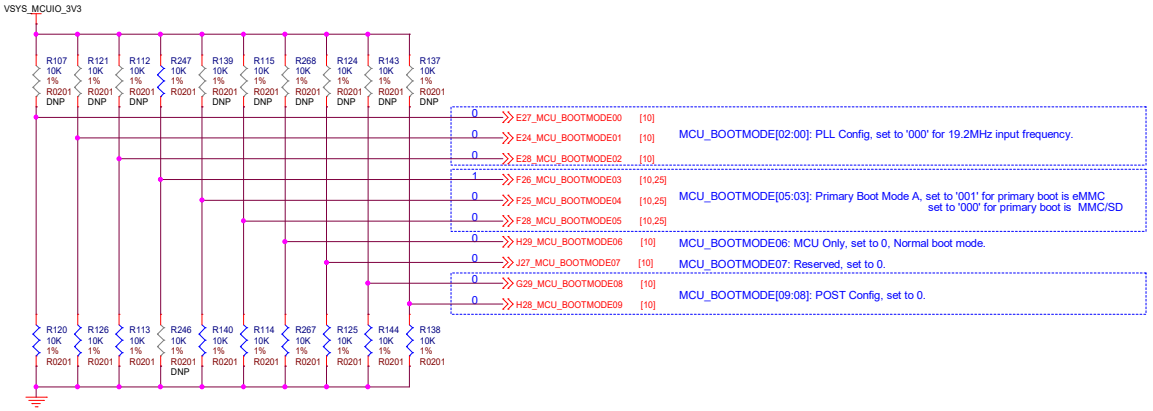
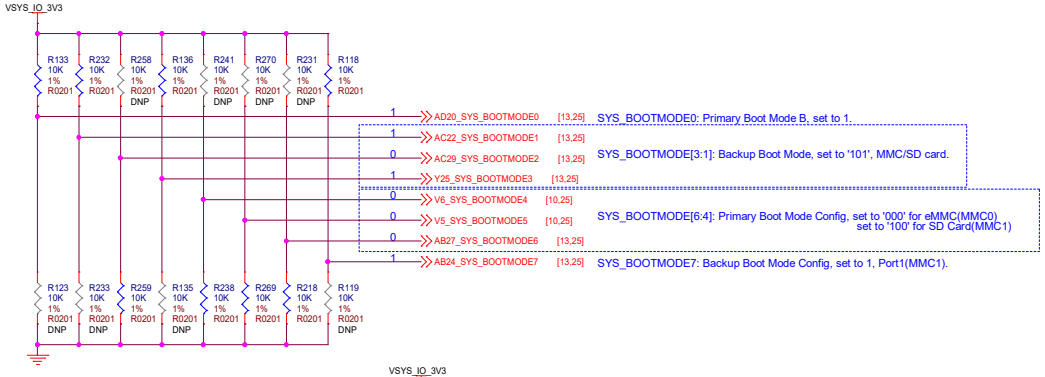
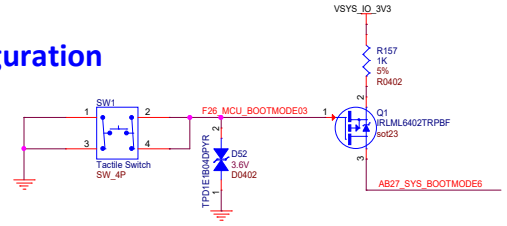




Boot Mode Configuration



Push-button SW1	Primary Boot Mode	Backup Boot Mode	MCU_BOOTMODE05	MCU_BOOTMODE04	MCU_BOOTMODE03	SYS_BOOTMODE6	SYS_BOOTMODE5	SYS_BOOTMODE4
Open	eMMC(MMC0)	SD Card(MMC1)	0	0	1	0 (Port 0)	0 (8-bit)	0 (1.8V)
Closed	SD Card(MMC1)	SD Card(MMC1)	0	0	0	1 (Port 1)	0 (4-bit)	0 (Filesystem mode)

Primary boot with BOOT normal-open push-button selecting eMMC port 0 (open) or MMC/SD port1 (closed).

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Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022
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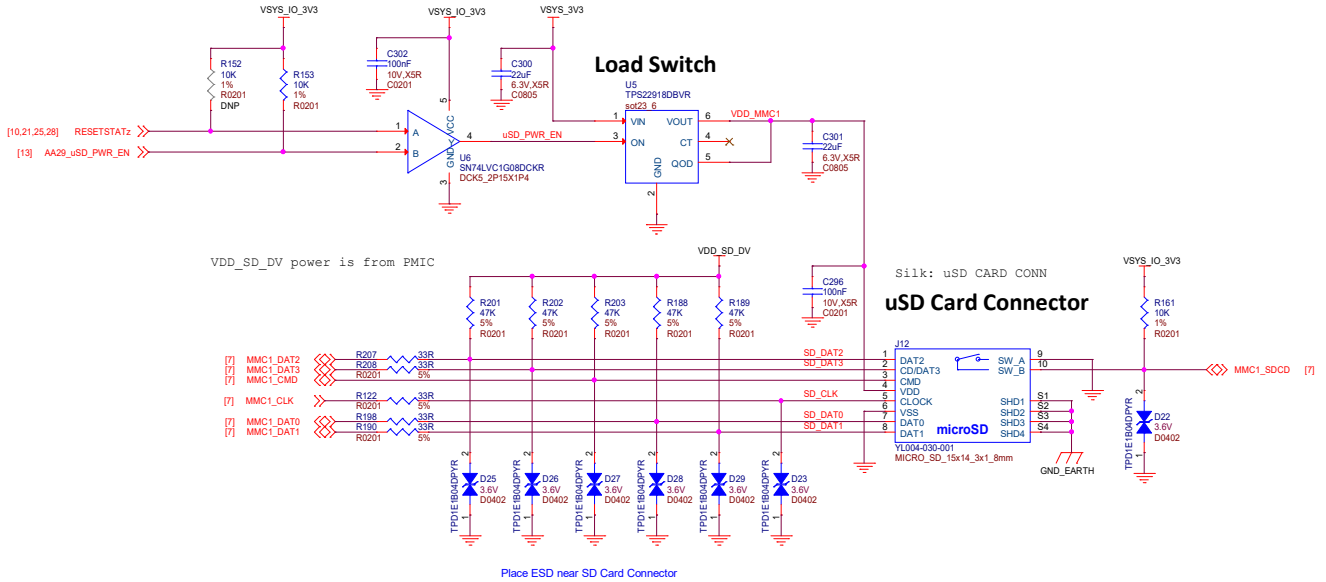
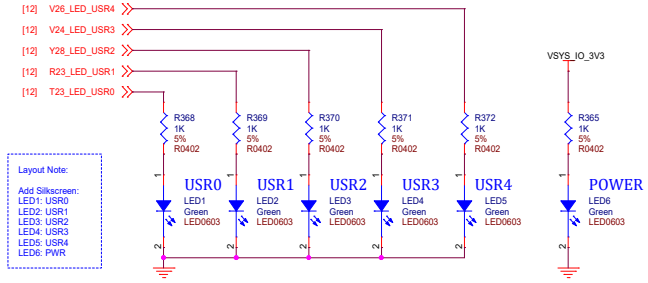
Micro SD CARD INTERFACE



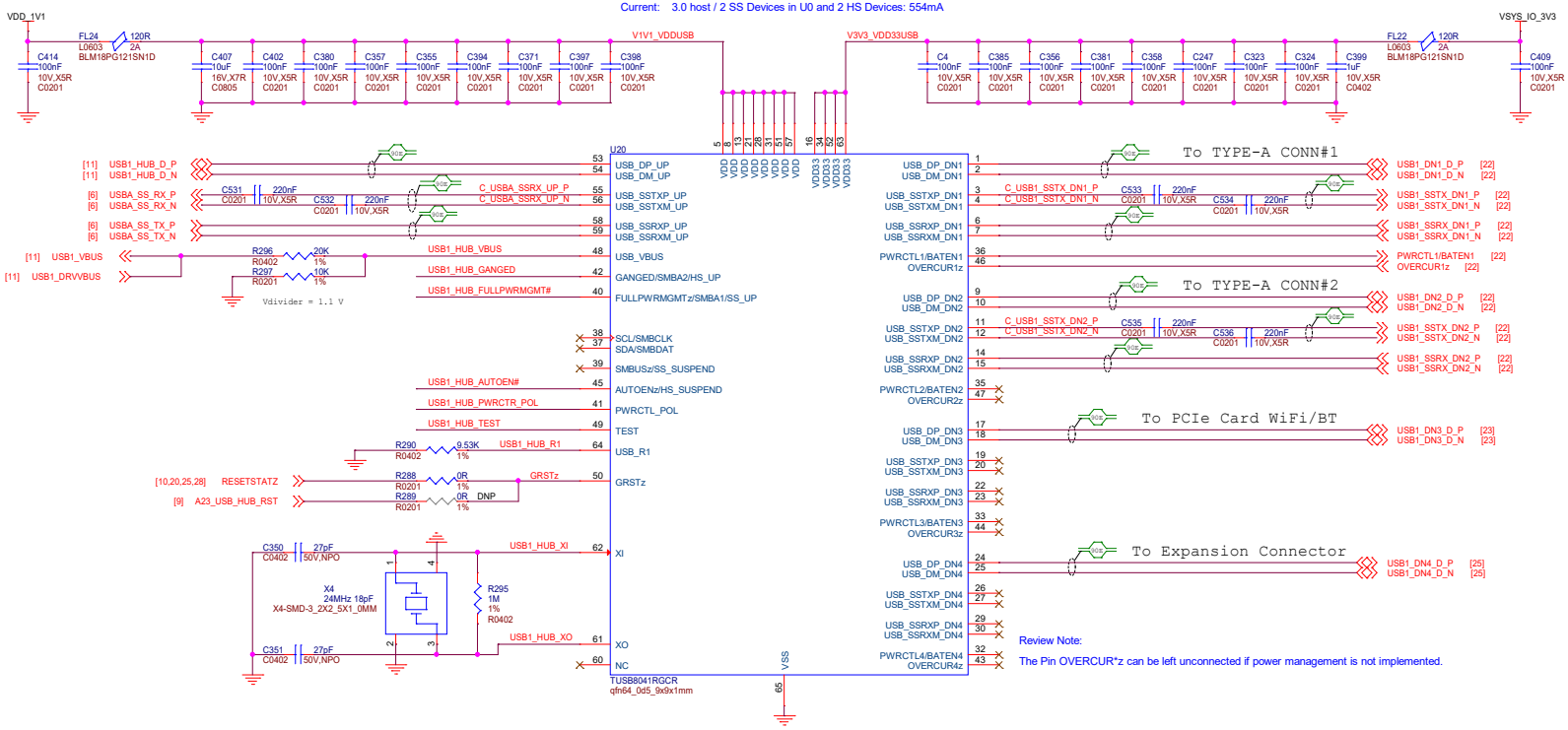
LEDs

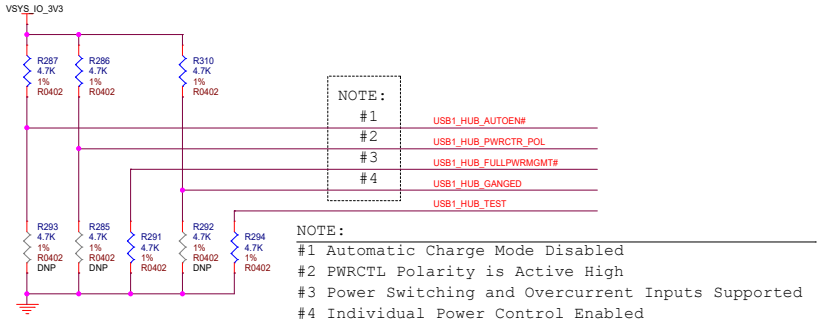


<Variant Name>

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 20. MICRO SD, LEDs	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 20 of 32

USB 3.0 HUB





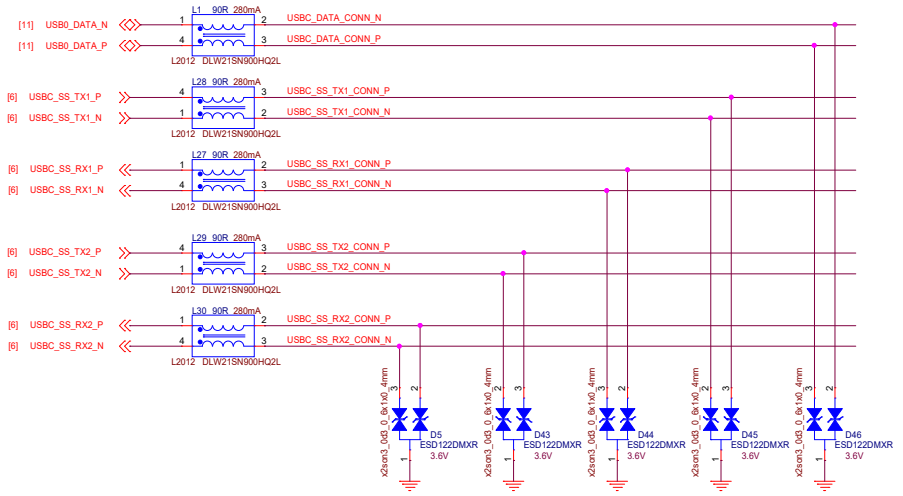
NOTE:

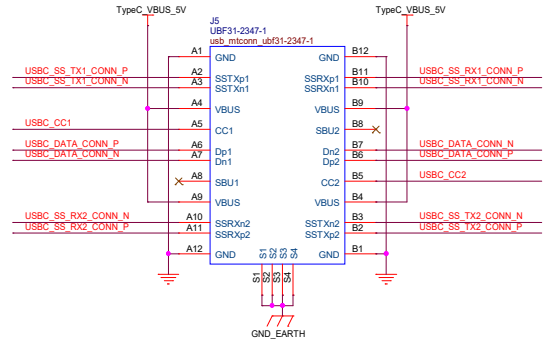
#1 Automatic Charge Mode Disabled
#2 PWRCTL Polarity is Active High
#3 Power Switching and Overcurrent Inputs Supported
#4 Individual Power Control Enabled

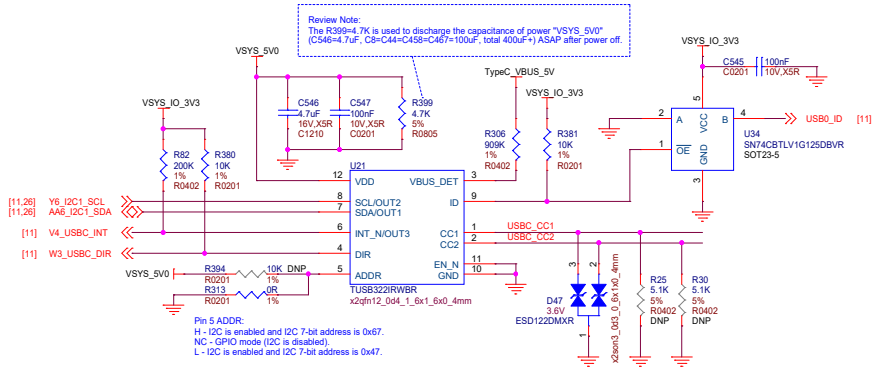
<Variant Name>

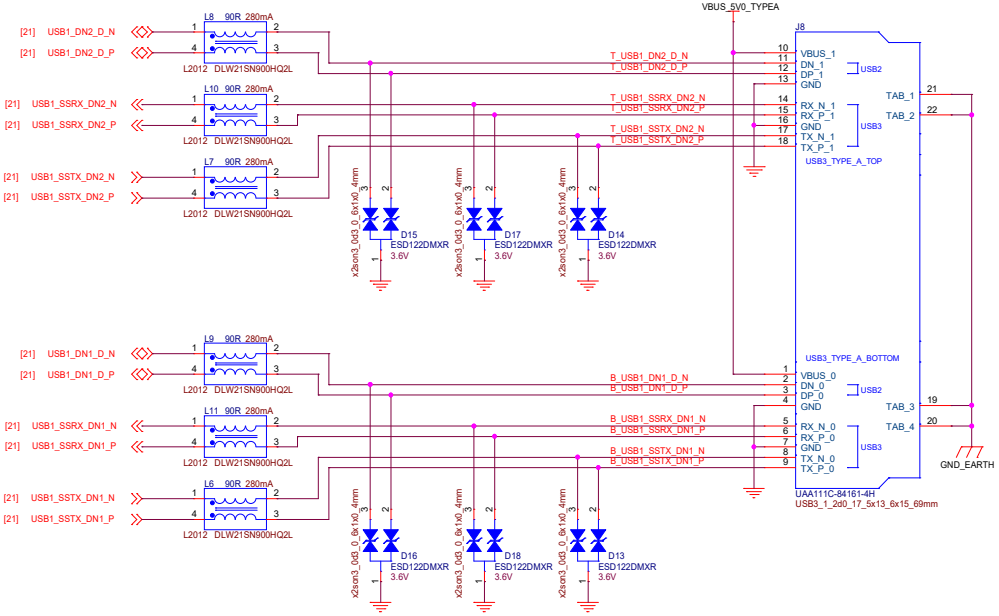
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 21. USB 3.0 HUB	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 21 of 32

TYPE-C USB 3.0 Sink Application (UFP) Default

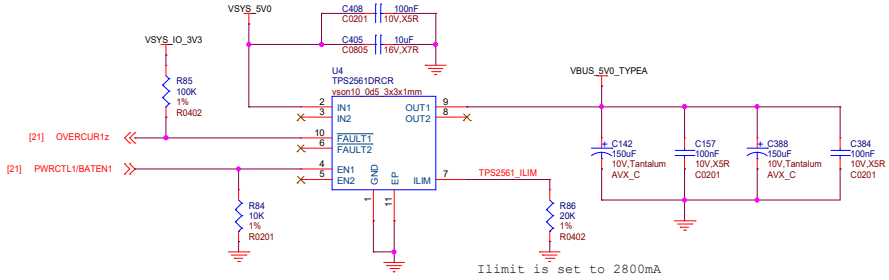








USB 3.0 DUAL TYPE-A



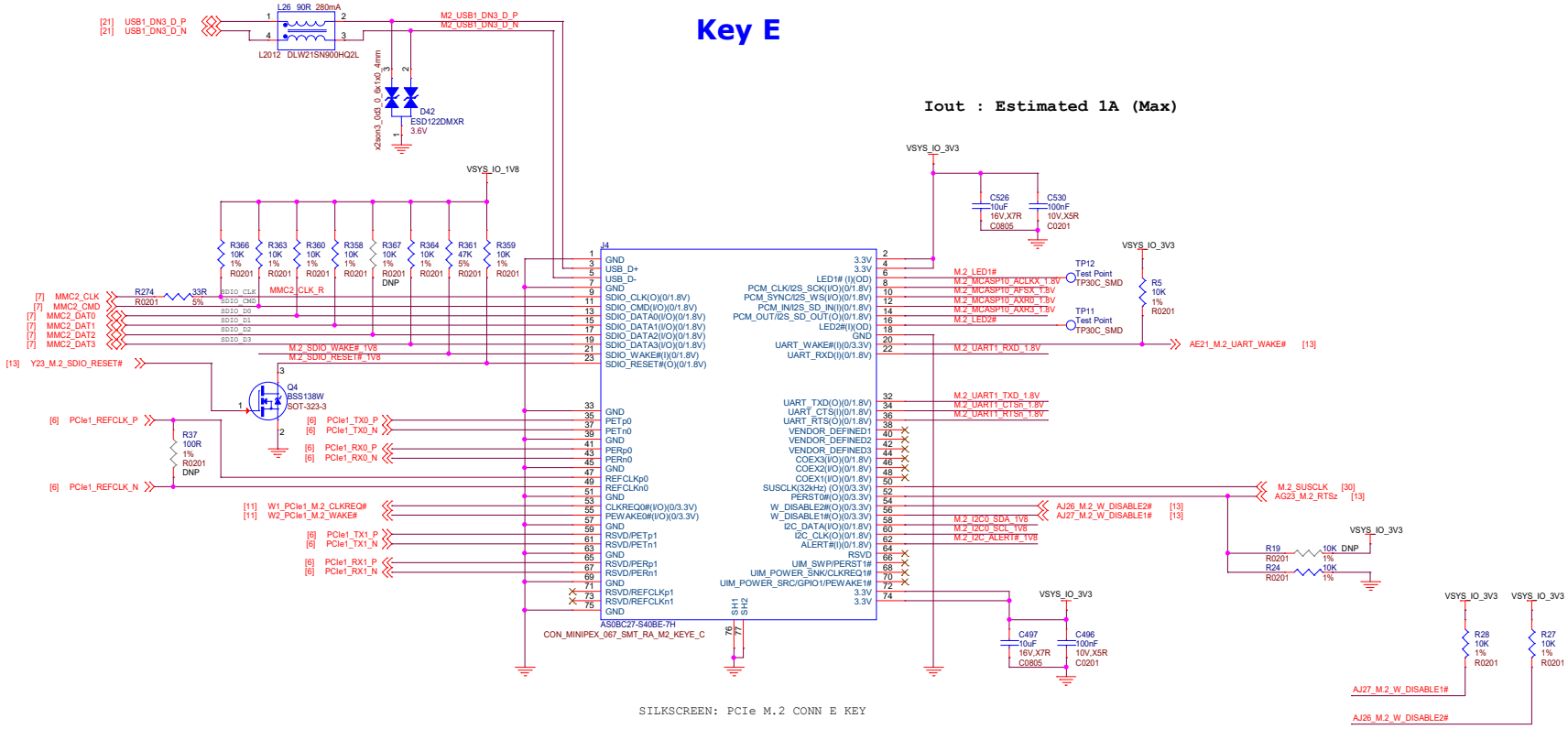
<Variant Name>

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 22. USB 3.0 TYPE A, TYPE C	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 22 of 32

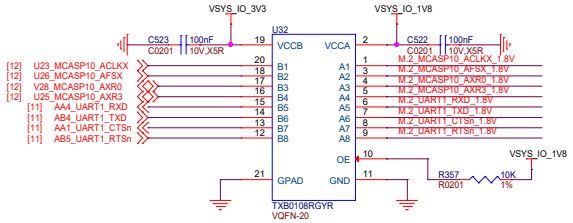
PCIe_M.2_INTERFACE - SDIO

Key E

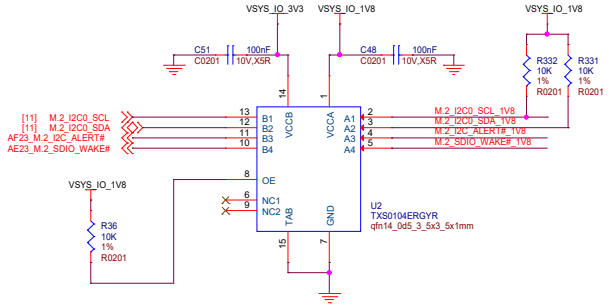
Iout : Estimated 1A (Max)

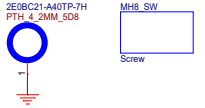


3.3V To 1V8 Level translator



3.3V To 1V8 Level translator

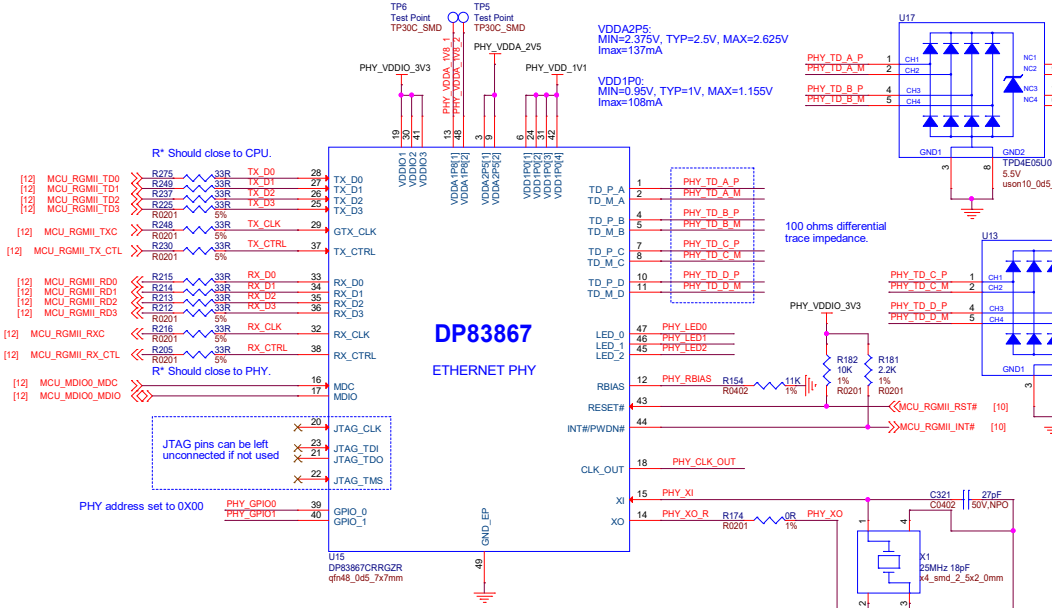


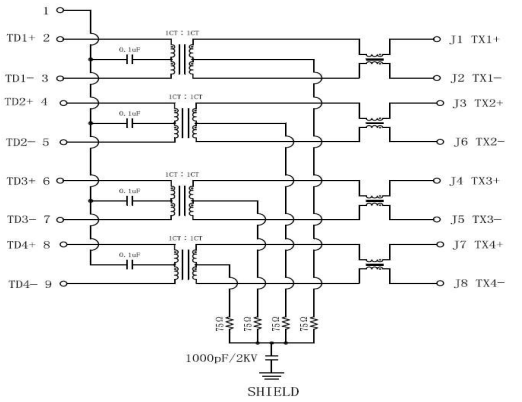


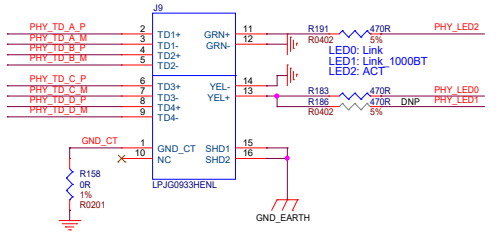
<Variant Name>

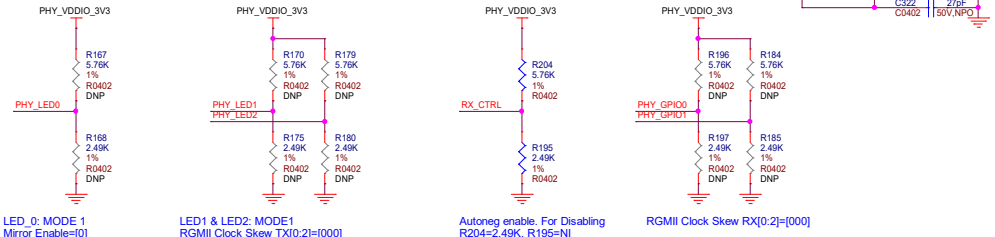
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 23. PCIe_M.2_KEY E	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 23 of 32

GB ETHERNET



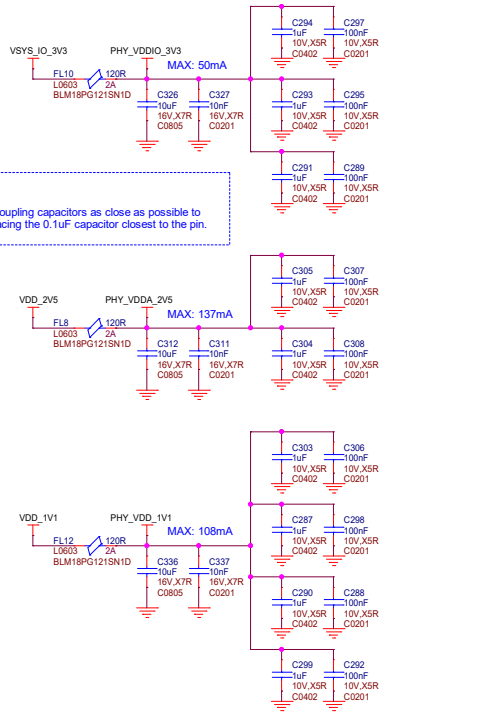






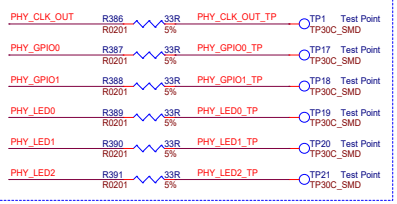
Layout Note:

Place 1uF and 0.1uF decoupling capacitors as close as possible to component VDD pins, placing the 0.1uF capacitor closest to the pin.



Review Note:

These test points are used for TI testing only!



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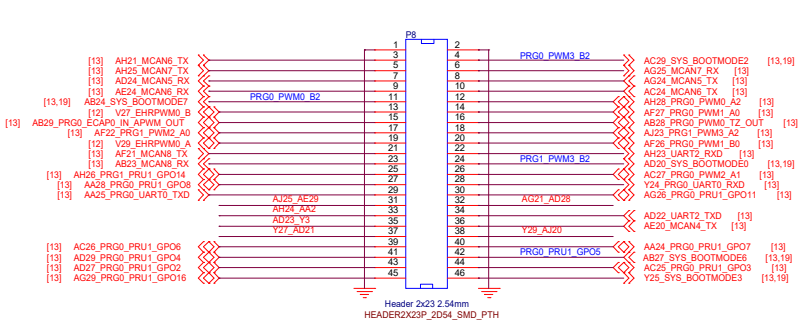
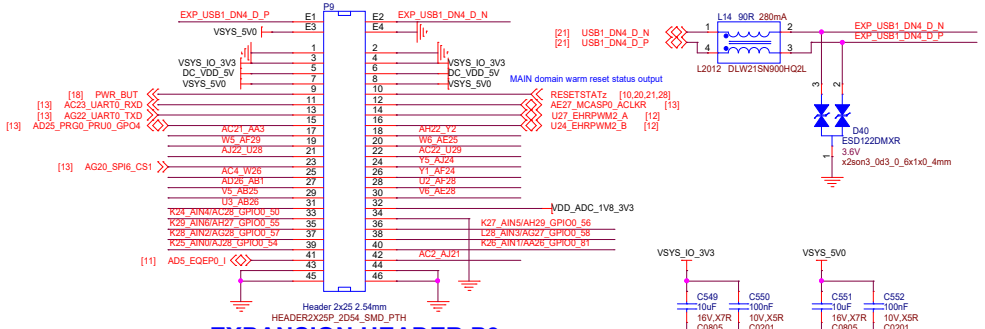
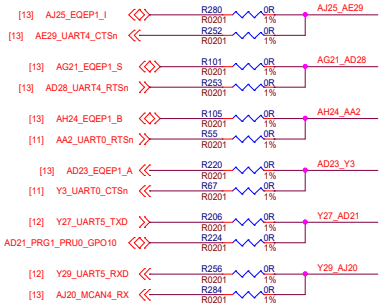
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 24. MCU GB ETHERNET	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 24 of 32

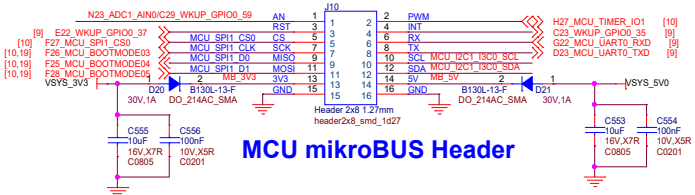


EXPANSION HEADER P8

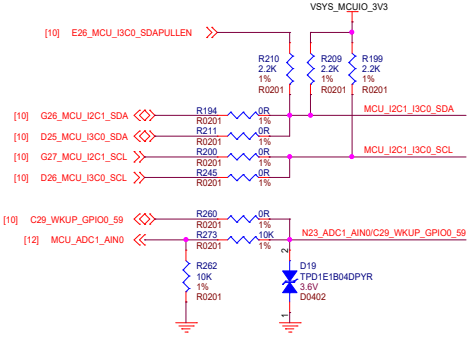


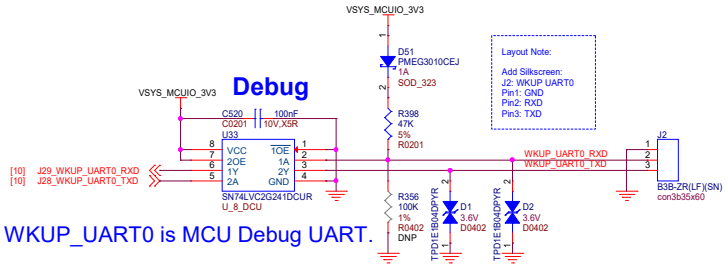
EXPANSION HEADER P9



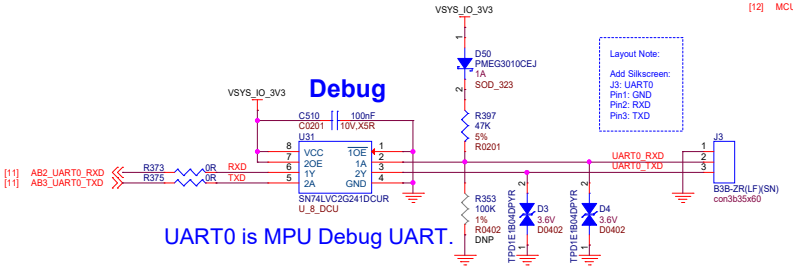


MCU mikroBUS Header

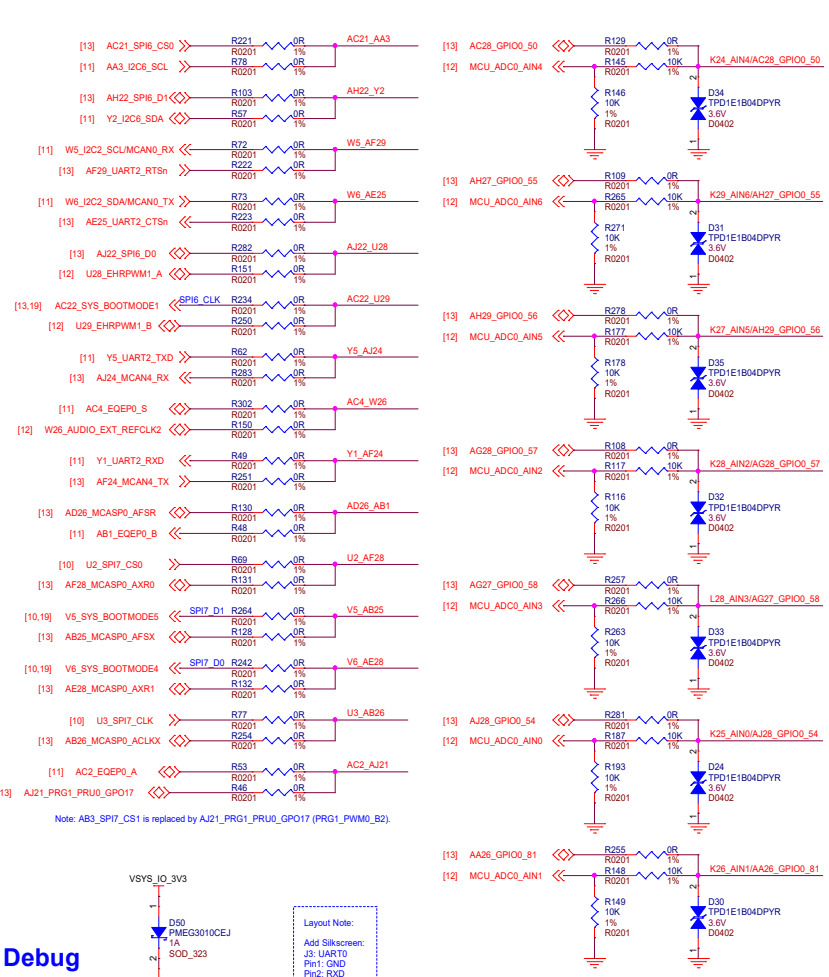




WKUP_UART0 is MCU Debug UART.



UART0 is MPU Debug UART.



<variant_name>

seeed The IoT Hardware Enabler	https://www.seeedstudio.com		
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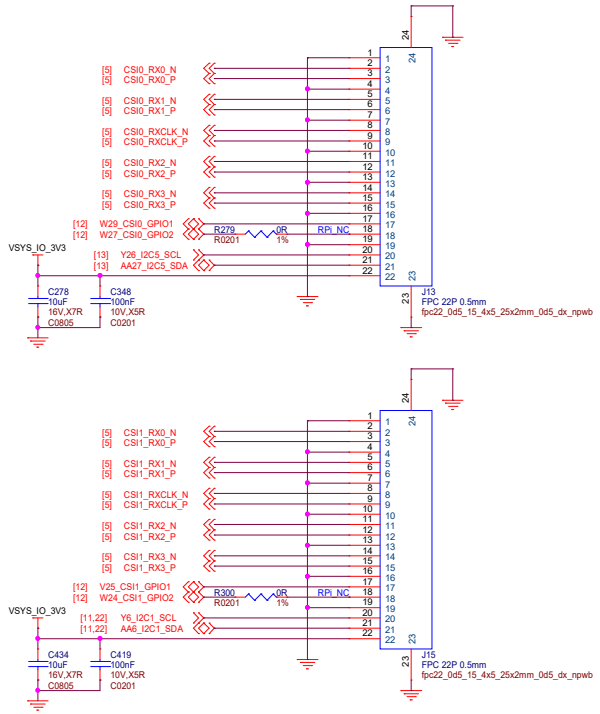
Size: C	Document Number: 25. P8 P9,mikroBUS HEADER,DEBUG		Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 25 of 32	

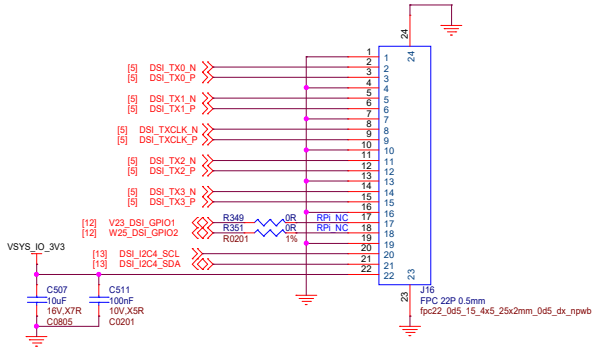
NOTE:
The RPi camera connector is 3.3V only (GPIO and IIC)!

80	SCL0	IIC Clock pin (Raspberry Pi GPIO45) Typically used for Camera and Displays Internal 1.8K pull up to CM4_3.3V
81	+5V (Input)	4.75V-5.25V Main power input
82	SDA0	IIC Data pin (Raspberry Pi GPIO44) Typically used for Camera and Displays Internal 1.8K pull up to CM4_3.3V
97	Camera_GPIO	Typically used to Shutdown the camera to reduce power. Reassigning this pin to another function isn't recommended. CM4_3.3V signalling

Raspberry Pi Camera Connector x4 Lane



Raspberry Pi Display Connector x4 Lane



<Variant Name>

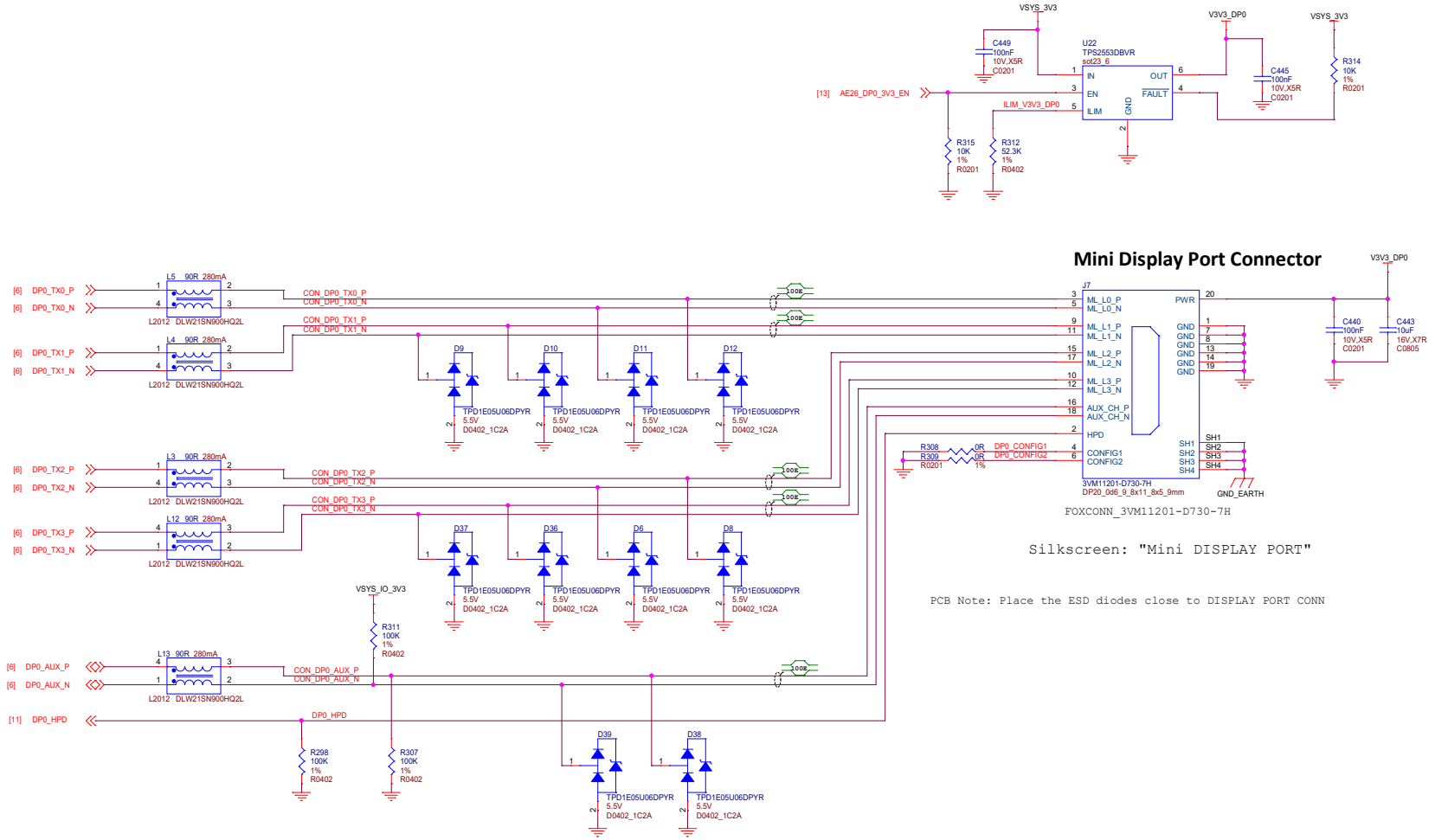
seeed The IoT Hardware Enabler

https://www.seeedstudio.com

Title: BeagleBone AI-64

Size: C	Document Number: 26. Raspberry Pi CSI DSI	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 26 of 32

Mini DISPLAY PORT INTERFACE



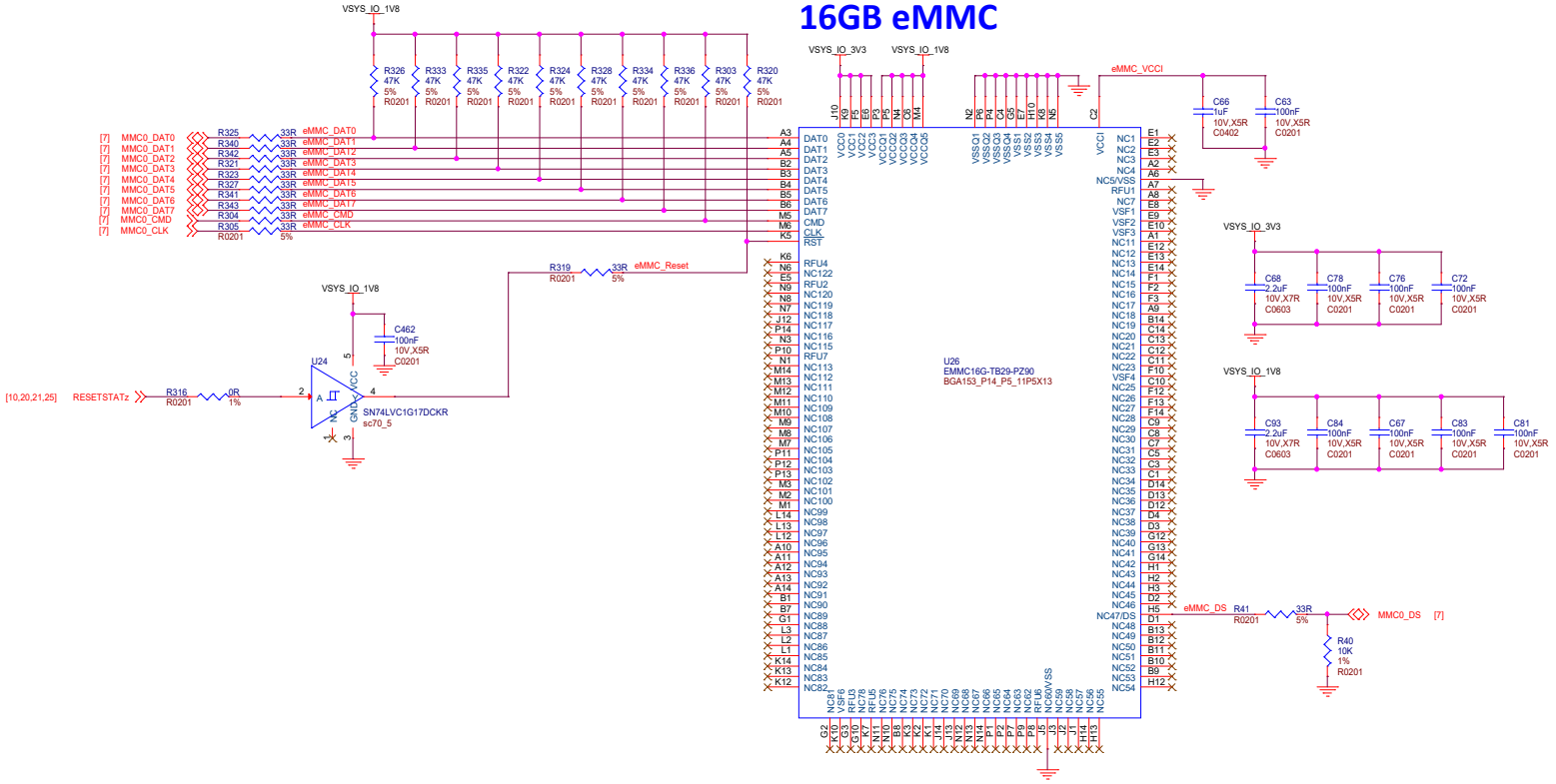
Silkscreen: "Mini DISPLAY PORT"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN

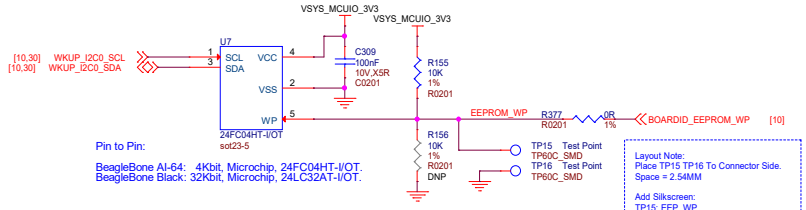
<Variant Name>

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 27. DISPLAY PORT	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 27 of 32

16GB eMMC



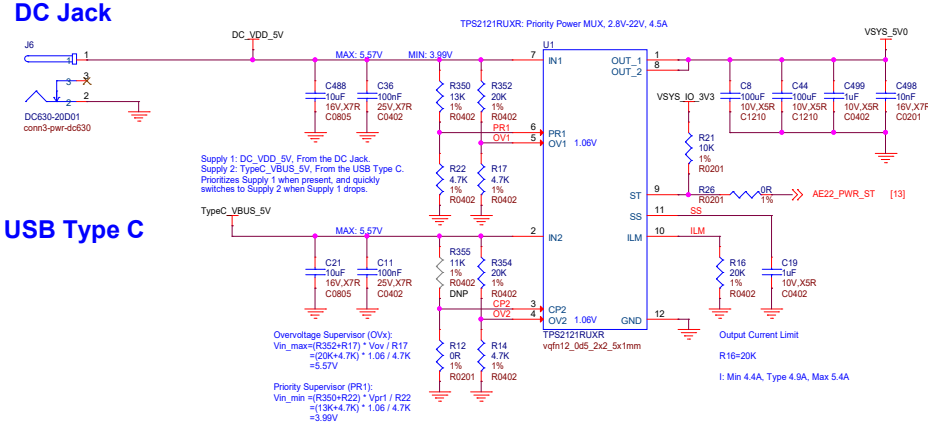
BOARD ID EEPROM 4Kbit



<Variant Name>

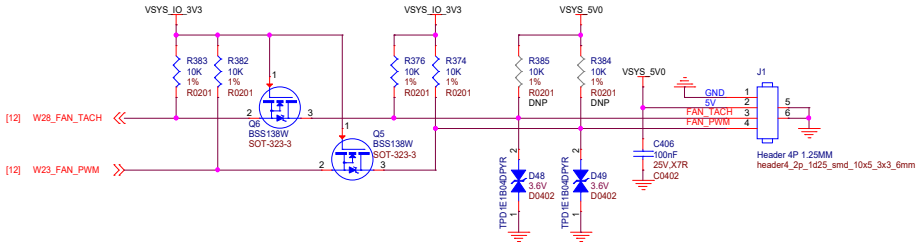
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 28. eMMC, EEPROM	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 28 of 32

DC Jack

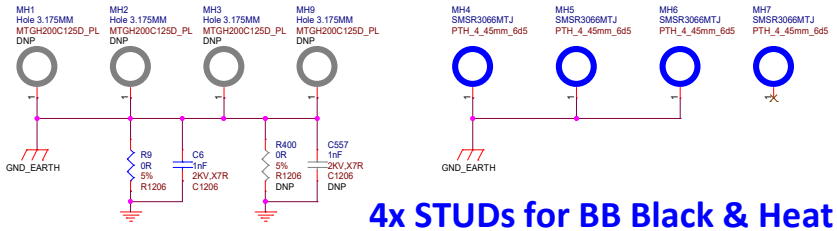


USB Type C

FAN HEADER

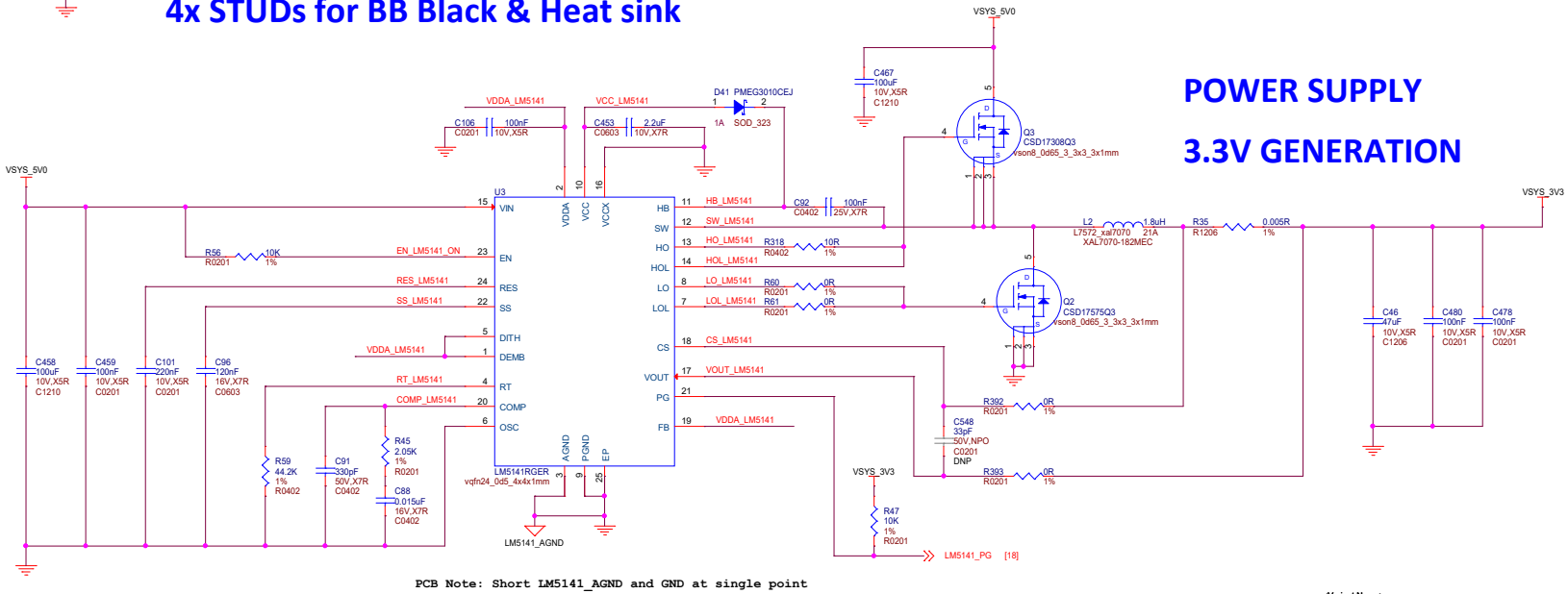


4x STUDs for BB Black & Heat sink



POWER SUPPLY

3.3V GENERATION



PCB Note: Short LM5141_AGND and GND at single point

TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 5.5V
Vout1 = 3.3V@8A
Ta = 25 deg

<Variant Name>

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 29. POWER INPUT 5V	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 29 of 32

EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)

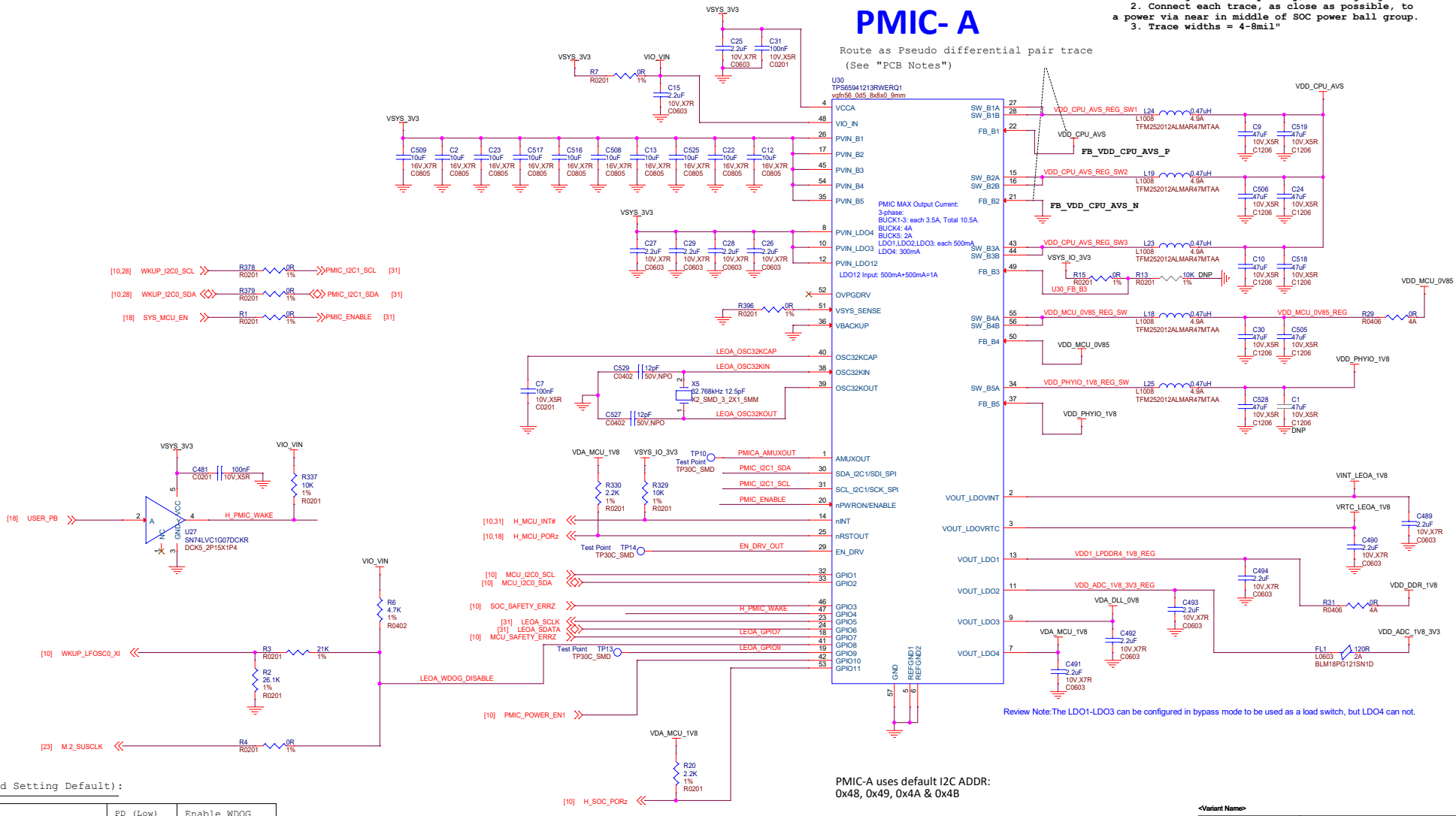
(3-Phase Buck supplying VDD_CPU)

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC- A

Route as Pseudo differential pair trace
(See "PCB Notes")



PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

(EVM Bd Setting Default):

LEOA_WDOG_DISABLE	PD (Low)	Enable WDOG
	PU (High)	Disable WDOG

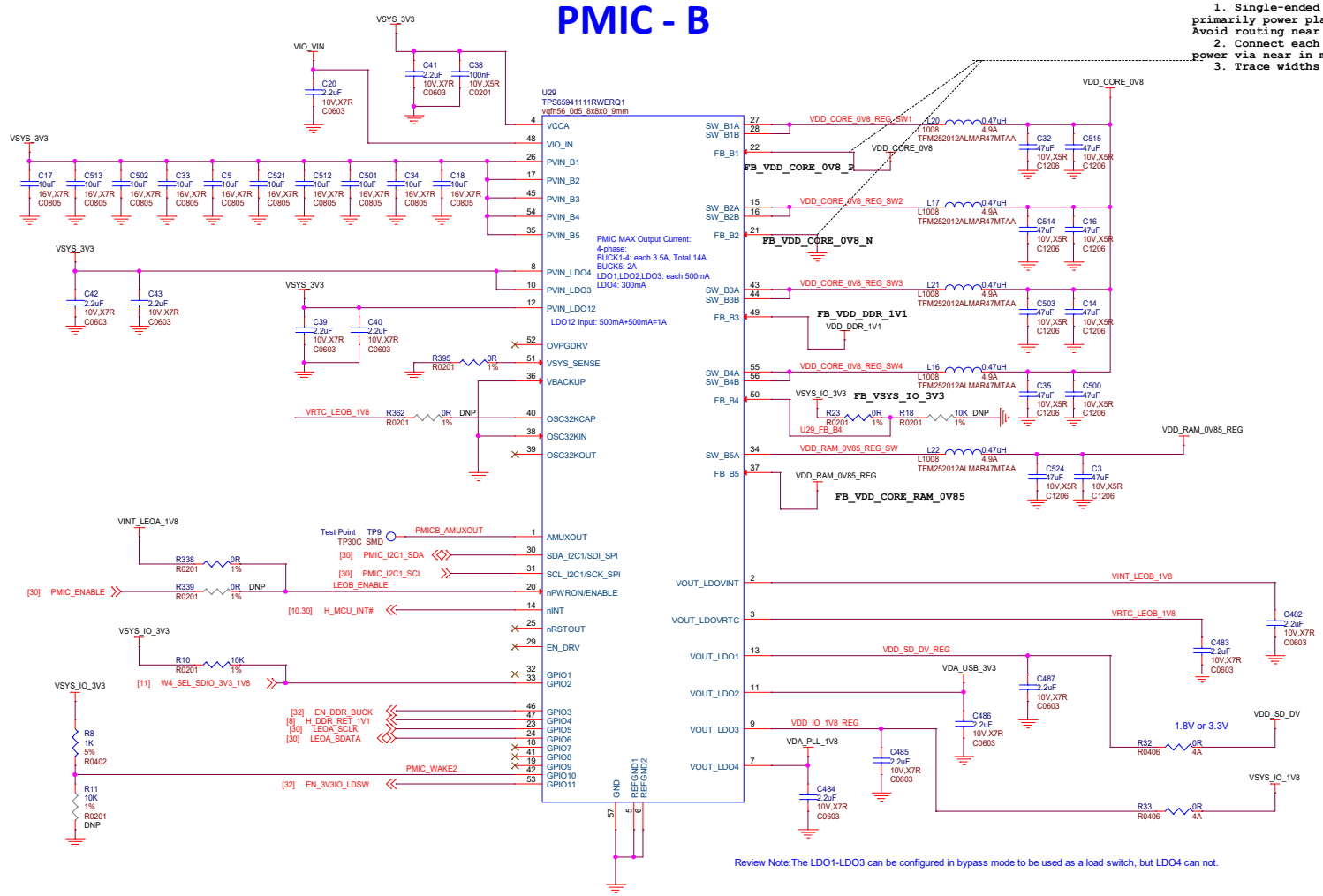
<Variant Name>

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 30. PMIC A	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 30 of 32

PMIC - B

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



Review Note:The LDO1-LDO3 can be configured in bypass mode to be used as a load switch, but LDO4 can not.

PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

<Variant Name>

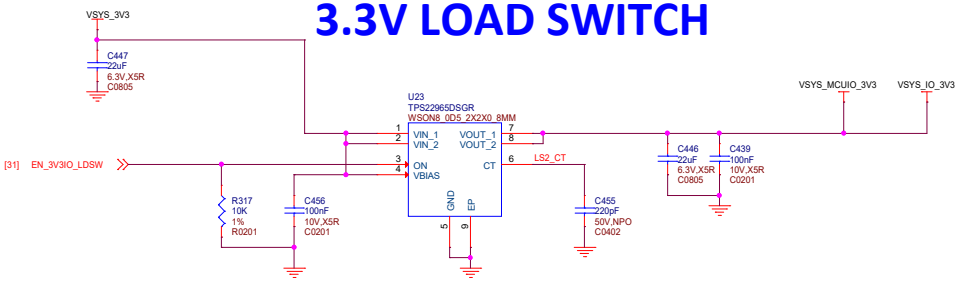
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 31. PMIC B	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 31 of 32

PCB1
BeagleBone AI-64_PCB

Label 1
DC 5V Label

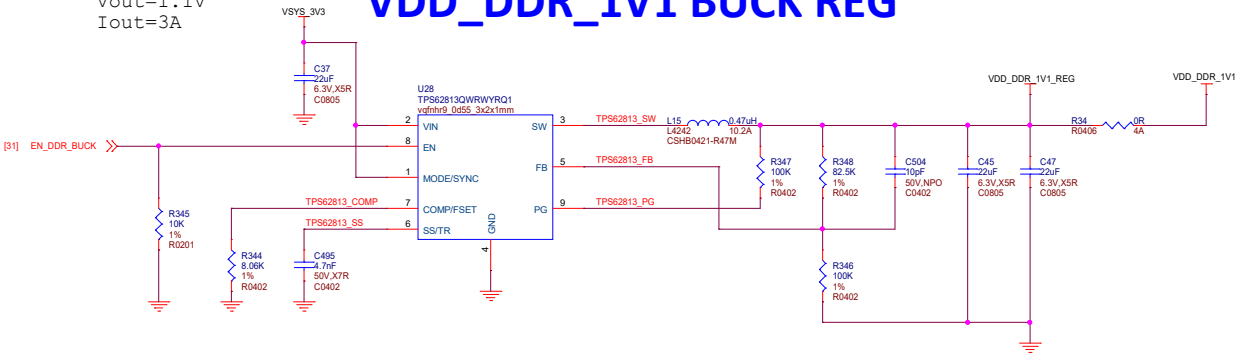
Label 2
SN Label

3.3V LOAD SWITCH



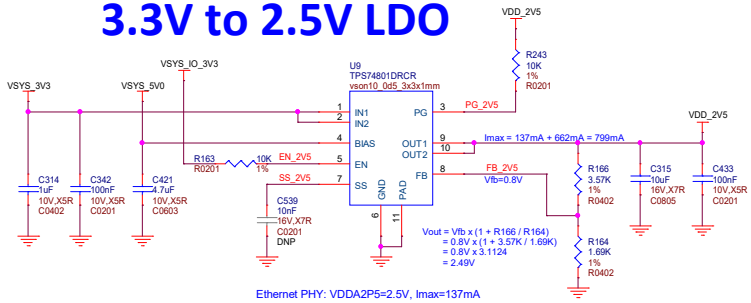
VDD_DDR_1V1 BUCK REG

Vout=1.1V
Iout=3A



ETHERNET POWER

3.3V to 2.5V LDO



Ethernet PHY: VDDA2P5=2.5V, Imax=137mA

LDO U18 Power In=2.5V, Imax=662mA

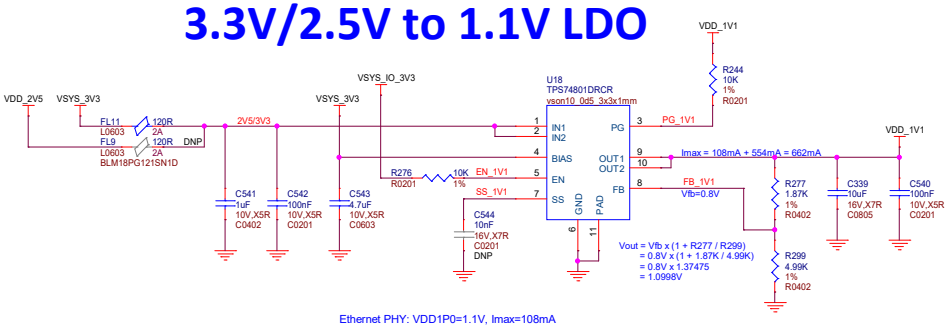
Total: Imax= 137mA + 662mA = 799mA

Power Consumption: (3.3V-2.5V) * 0.799A = 0.6392W

Thermal Junction-to-ambient: 0.6392W * 44.2°C/W=28.25°C

USB3.0 HUB & ETHERNET POWER

3.3V/2.5V to 1.1V LDO



Ethernet PHY: VDD1P0=1.1V, Imax=108mA

USB3.0 HUB: VDD=1.1V, Imax=554mA

Total: Imax = 108mA + 554mA = 662mA

Option 1: VIN_2V5/3V3 = 3.3V

Power Consumption: (3.3V-1.1V) * 0.662A = 1.4564W

Thermal Junction-to-ambient: 1.4564W * 44.2°C/W=64.37°C

Option 2: VIN_2V5/3V3 = 2.5V

Power Consumption: (2.5V-1.1V) * 0.662A = 0.9268W

Thermal Junction-to-ambient: 0.9268W * 44.2°C/W=40.96°C

<Variant Name>

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: BeagleBone AI-64	
Size: C	Document Number: 32. LOAD SWITCHES, POWER SUPPLY	Rev: B1
Draw By: Junqing.Xin	Date: Wednesday, June 08, 2022	Sheet: 32 of 32