# FPGA Application Week 3 Homework

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## Contents



# 1 Exercise 3-1 Create a project and a Verilog file

## 1.1 Create a project named "ex3_half_adder"

1. Click "New Project Wizard" in the "File" menu. (Figure 1)
2. Click "Next" in the "New Project Wizard" window. (Figure 2)
3. Select project working directory, named project name, click "Finish". (Figure 3)

## 1.2 Create a Verilog file named "ex3_half_adder.v"

1. Click "New" in the "File" menu. (Figure 4)
2. Click "Verilog HDL File" in the "New" window. (Figure 5)
3. Click "Save As" in the "File" menu. (save the file with the default name it suggest which is the same as the current project.) (Figure 6)
4. Type in codes in the "ex3_half_adder.v" file and save it. (Figure 7)

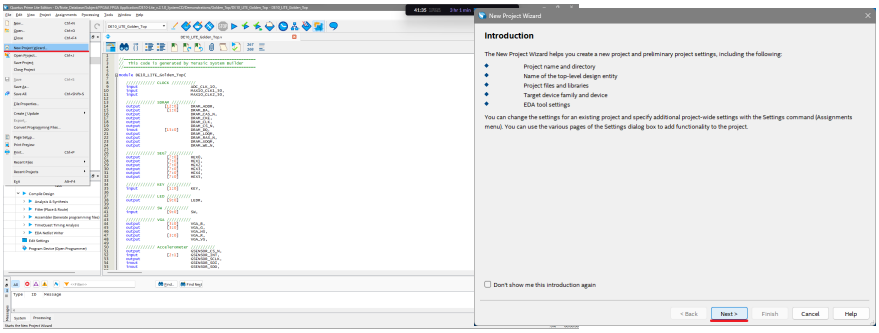

Figure 1: Select New Project Wizard




Figure 2: New Project Wizard

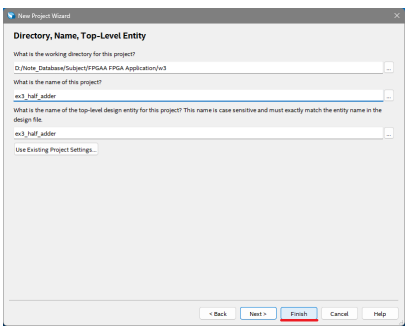


Figure 3: Select new project details

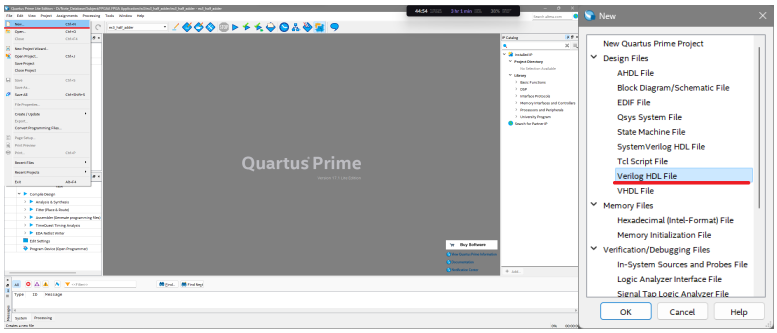


Figure 4: Select new file




Figure 5: Select Verilog HDL File

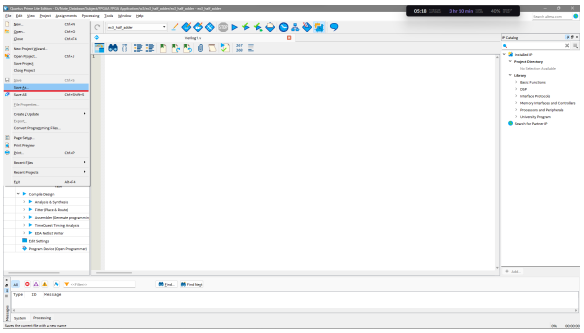

Figure 6: Save new file

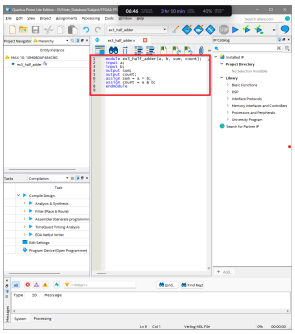

Figure 7: Type in codes

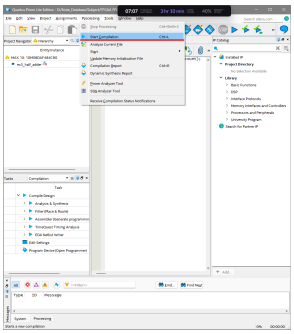

Figure 8: Start compilation

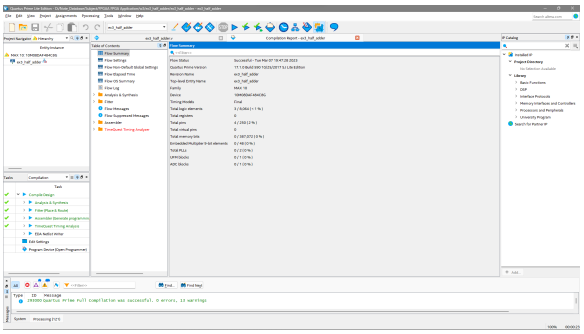

Figure 9: Check compilation result

5. Click "Start Compilation" in the "Processing" menu. (Figure 8)
6. Check compilation result. (Figure 9)

## 1.3 Create a testbench file named "test.v"

1. Click "New" in the "File" menu. (Figure 10)
2. Click "Verilog HDL File" in the "New" window. (Figure 11)
3. Save the file with the name "test.v". (naming is not limited) (Figure 12)
4. Type in codes in the "test.v" file and save it. (Figure 13)
5. Click "Files" in the "Project Navigator" window. (Figure 14)
6. Select "Files" option to see all files in the project. (Figure 15)
7. Click "Settings" in "Assignments" window. (Figure 16)
8. Click "Simulation" in "Settings" window. (Figure 17)
9. Modify the settings. (Figure 18)
10. Click "Test Benches". (Figure 19)
11. Click "New" in "Test Benches" window. (Figure 20)
12. Navigate to the "test.v" file and select it. (Figure 21)
13. Click "Add" in "Test Benches" window. (Figure 22)
14. Click "OK" in "New Test Bench Settings". (Figure 23)
15. Click "OK" in "Test Benches". (Figure 24)

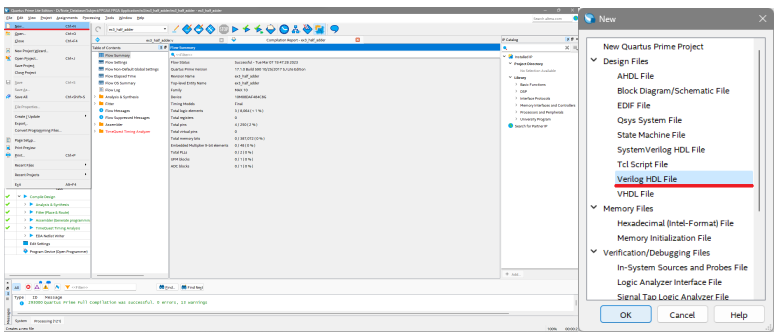

Figure 10: Select new file




Figure 11: Select Verilog HDL File

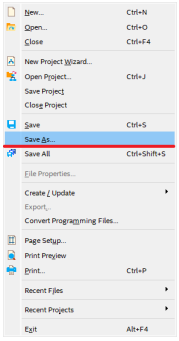


Figure 12: Save new file

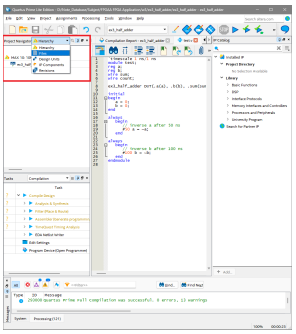

Figure 13: Type in codes

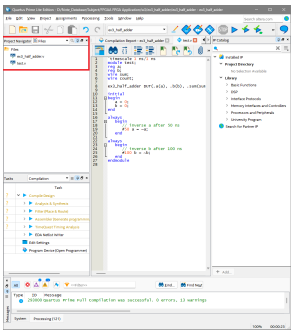

Figure 14: Open "Files" option

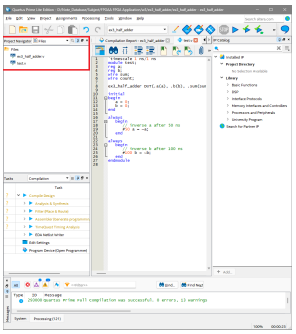

Figure 15: Select "Files" option

16. Click "OK" in "Settings". (Figure 25)
17. Click "Start Compilation" in the "Processing" menu. (Figure 26)
18. Check compilation result. (Figure 27)
19. Switch to "ModelSim" window. (Figure 28)

## 2 Exercise 3-2 Observe the simulation result

This section is to inspect simulation result of a half adder circuit. The circuit diagram is shown in Figure 29. The truth table of the circuit is shown in Table 1. The simulated waveform is shown in Figure 30. The simulation result is shown in Table 2. The detail of simulation result at specific time is shown in Figure 31 to 34. The simulation result is consistent with the truth table. The simulation result is also consistent with the waveform. In order to generate the circuit diagram from the Verilog file, click "Netlist Viewers/RTL-Viewer" in "Tools" menu.

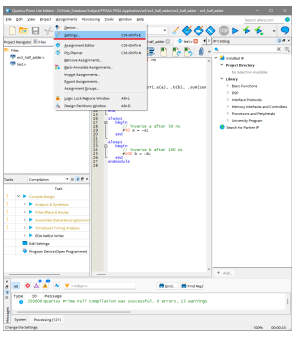

Figure 16: Click "Settings"

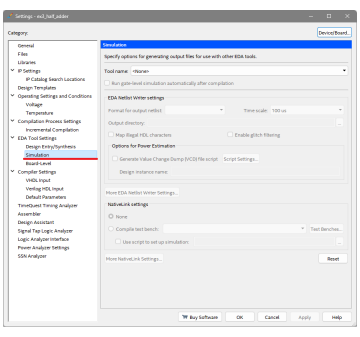

Figure 17: Click "Simulation"

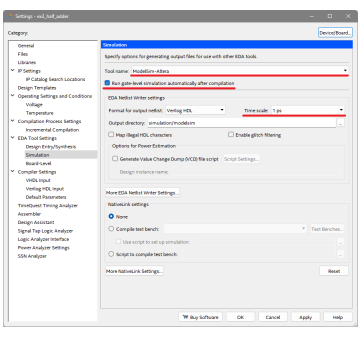

Figure 18: Modify the settings

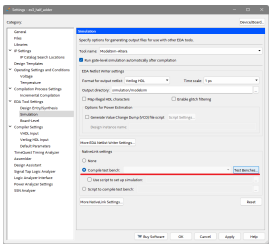

Figure 19: Click "Test Benches"

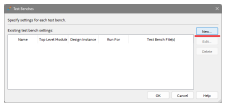

Figure 20: Click "New"

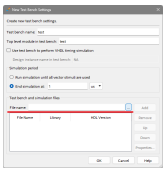

Figure 21: Navigate to "test.v" file

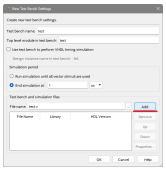

Figure 22: Click "Add"

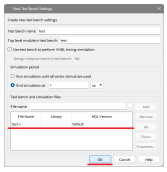

Figure 23: Click "OK"

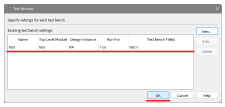

Figure 24: Click "OK"

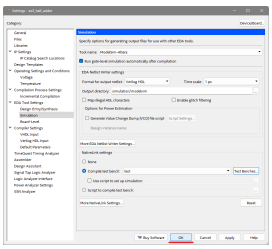

Figure 25: Click "Start Simulation"

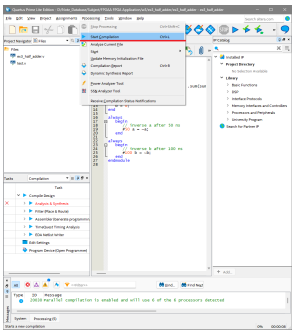

Figure 26: Click "Start Compilation"

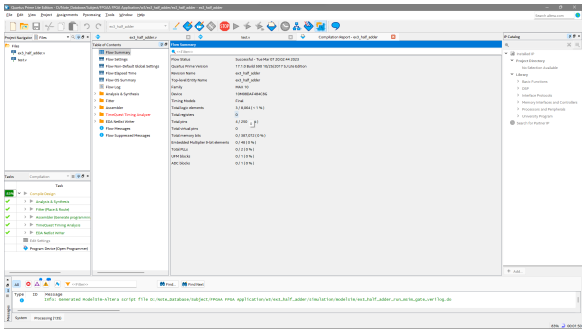

Figure 27: Click "Start Simulation"

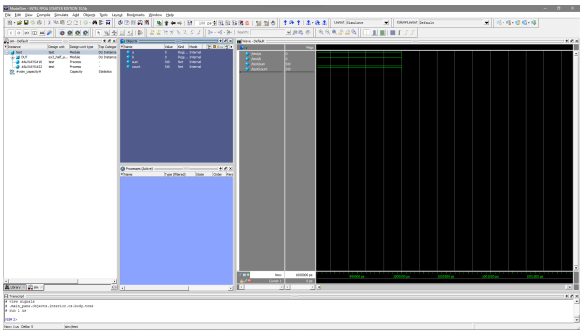

Figure 28: Check the simulation result with automatic opened waveform window

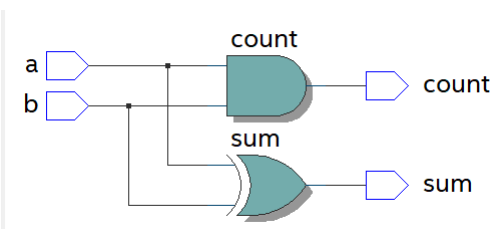


Figure 29: Circuit diagram of a half adder

| a | b | sum | count |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Table 1: Truth table of a half adder

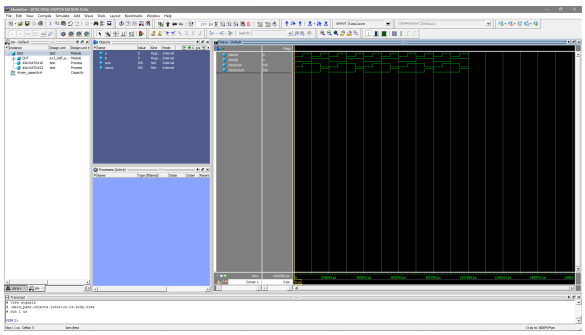

Figure 30: Waveform of a half adder

| a | b | sum | count |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Table 2: Simulation result of a half adder

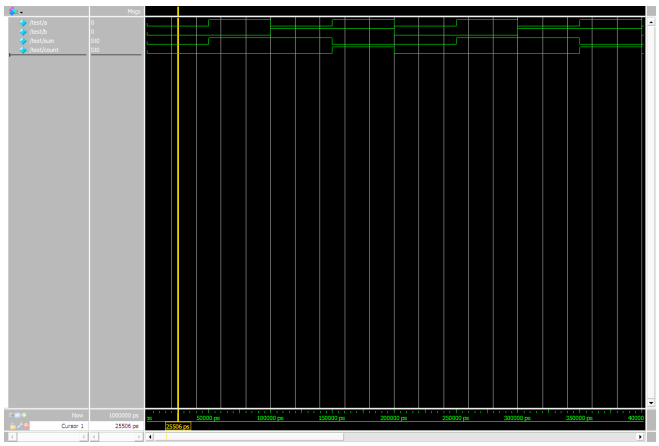

Figure 31: Simulation result at 25ns

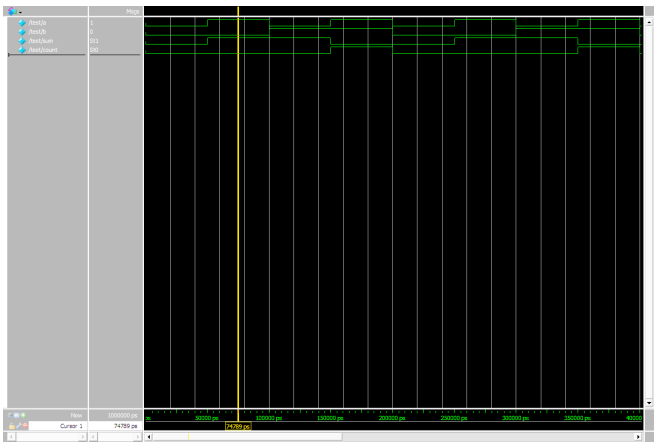

Figure 32: Simulation result at 75ns

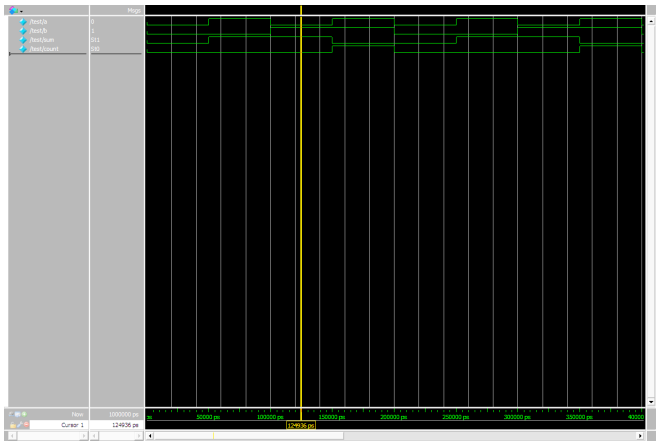

Figure 33: Simulation result at 125ns

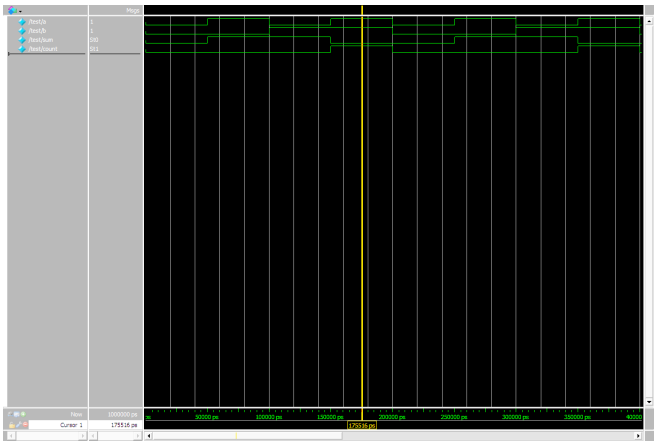

Figure 34: Simulation result at 175ns

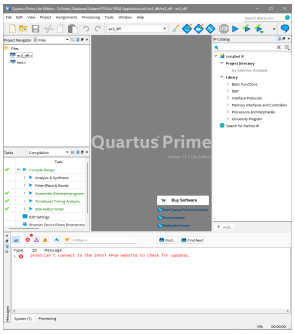

Figure 35: D flip-flop project

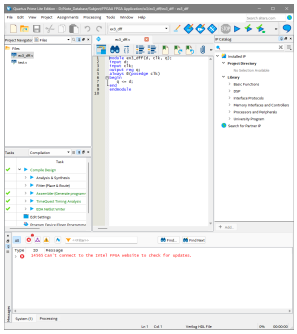

Figure 36: D flip-flop code

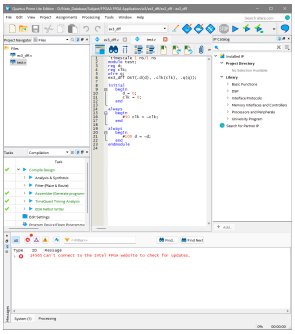

Figure 37: Test code

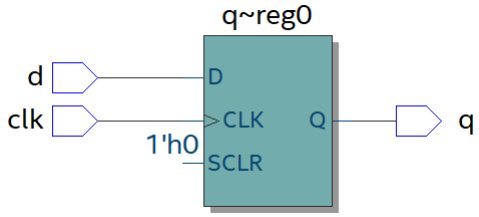


Figure 38: Circuit diagram of a D flip-flop

| clk | d | q | q' |
|---|---|---|---|
| ↑ ≫ | 0 | 0 | 1 |
| ↑ ≫ | 0 | 1 | 0 |
| ↑ ≫ | 1 | 0 | 0 |
| ↑ ≫ | 1 | 1 | 1 |

Table 3: Truth table of a D flip-flop

# 3 Exercise 3-3 Create and simulate a D flip-flop

The following list are the requirements to complete this exercise.

1. Create a project named "ex3_dff". (Figure 35)
2. Create a Verilog file named "ex3_dff.v". (Figure 36)
3. Create a testbench file named "test.v". (Figure 37)
4. Run the simulation.
5. Observe the simulation result.

The circuit diagram is shown in Figure 38. The truth table of the circuit is shown in Table 3. The simulated waveform is shown in Figure 39. The simulation result is shown in Table 4. The detail of simulation result at specific time is shown in Figure 40 to 43. The simulation result is consistent with the truth table. The simulation result is also consistent with the waveform.

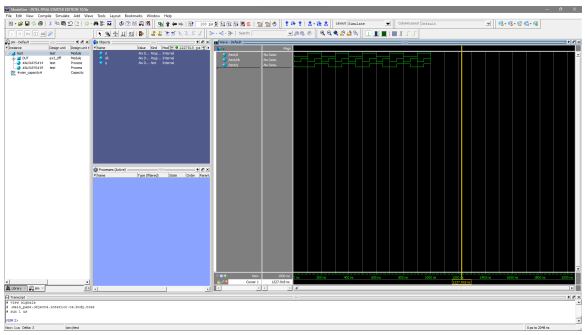

Figure 39: Simulation result

| d | q | q' | time |
|---|---|---|---|
| 0 | 0 | 1 | 57ns |
| 1 | 1 | 0 | 157ns |
| 0 | 0 | 1 | 257ns |
| 1 | 1 | 0 | 357ns |

Table 4: Simulation result of a D flip-flop

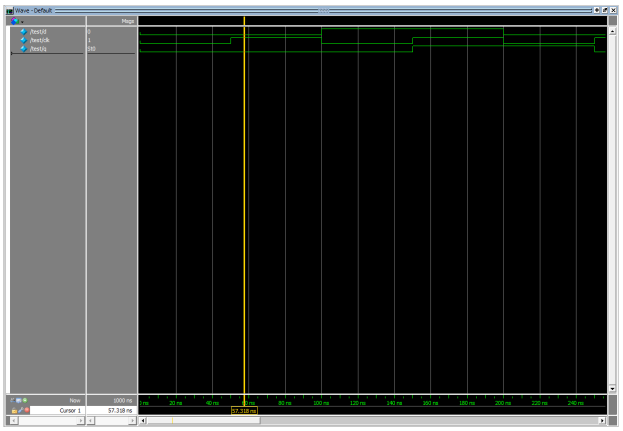

Figure 40: Simulation result at 57ns

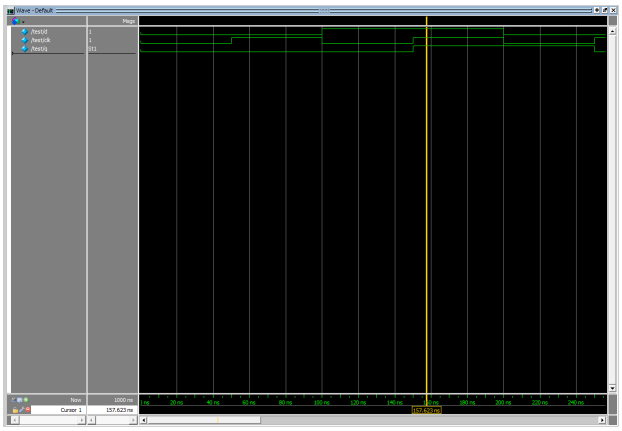

Figure 41: Simulation result at 157ns

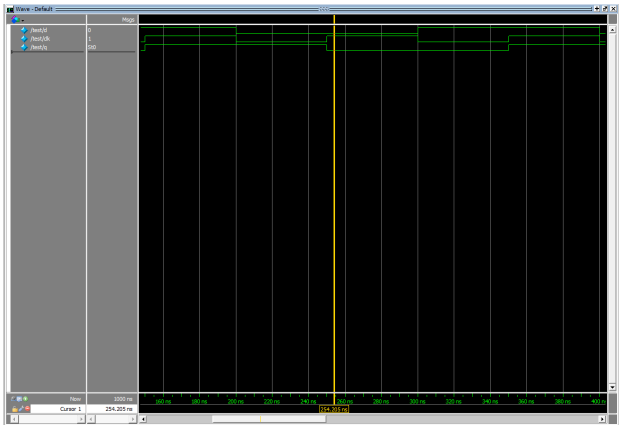

Figure 42: Simulation result at 257ns

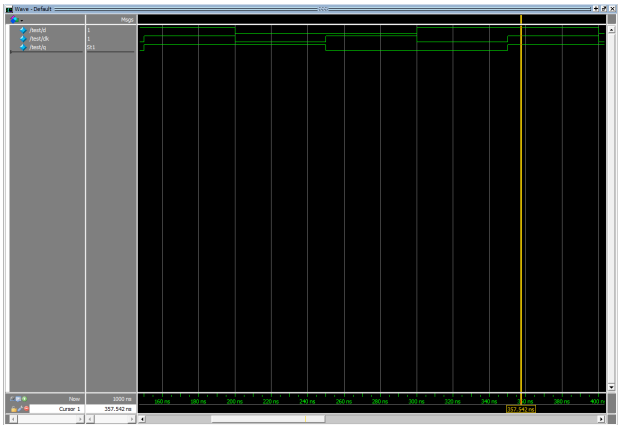

Figure 43: Simulation result at 357ns