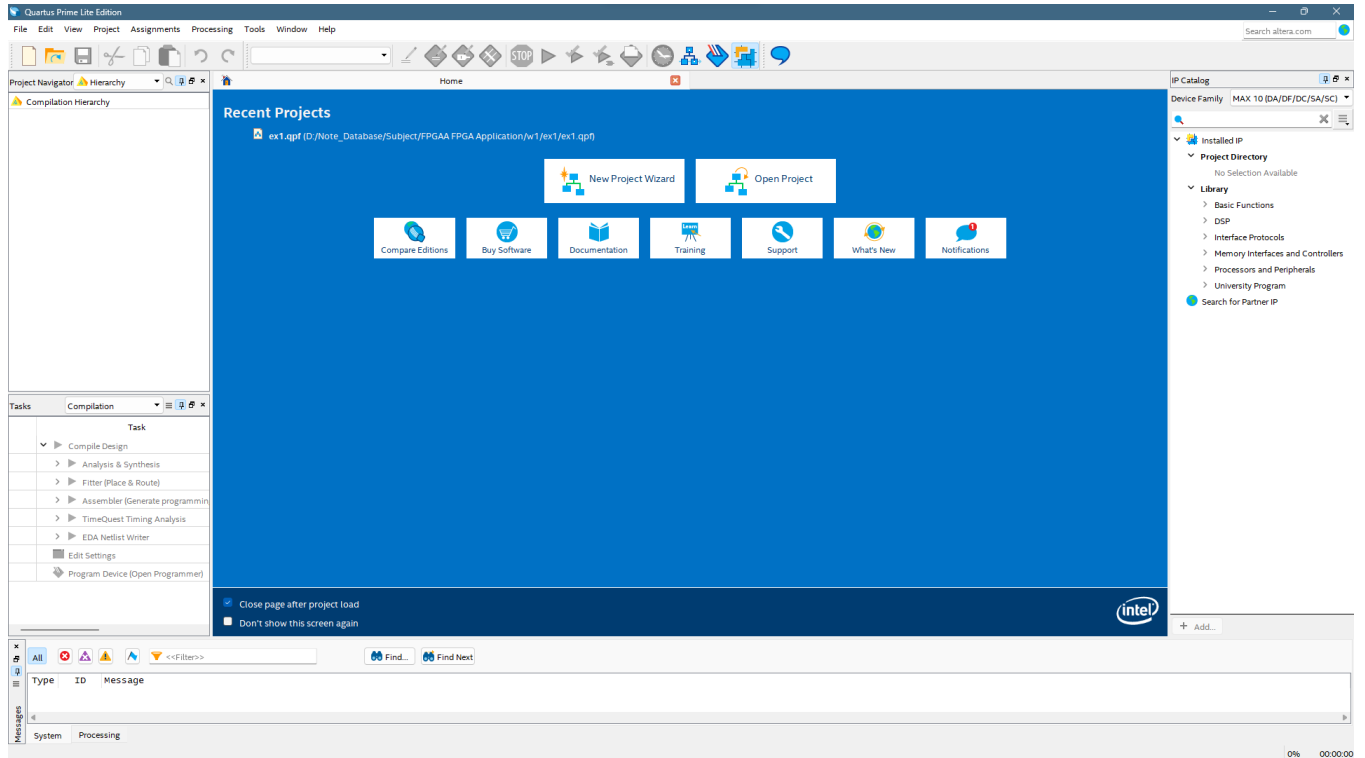


FPGA Application Week 1 Homework

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Exercise 1-1 Software Installation



Exercise 1-2 OR2 circuit with input A, B output Y

The screenshot displays the Quartus Prime Lite Edition software interface. The main window shows the 'Flow Summary' for a project named 'ex1'. The flow summary indicates that the compilation was successful on Tuesday, February 14, 2018, at 29:23. The project is configured for a MAX 10 10M08DAF484C8G device. The flow summary table lists various resources and their usage:

Resource	Usage
Quartus Prime Version	17.1.0 Build 590 10/25/2017 S.J. Lite Edition
Revision Name	ex1
Top-level Entity Name	ex1
Family	MAX 10
Device	10M08DAF484C8G
Timing Models	Final
Total logic elements	2 / 8,064 (< 1 %)
Total registers	0
Total pins	3 / 250 (1 %)
Total virtual pins	0
Total memory bits	0 / 387,072 (0 %)
Embedded Multiplier 9-bit elements	0 / 48 (0 %)
Total PLBs	0 / 2 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)

The 'Tasks' pane on the left shows the compilation process, including 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programming file)', 'TimeQuest Timing Analysis', 'EDA Netlist Writer', 'Edit Settings', and 'Program Device (Open Programmer)'. The 'Messages' pane at the bottom shows a successful compilation message: '293000 Quartus Prime Full compilation was successful. 0 errors, 13 warnings'.