Mid-Optical Processing Board

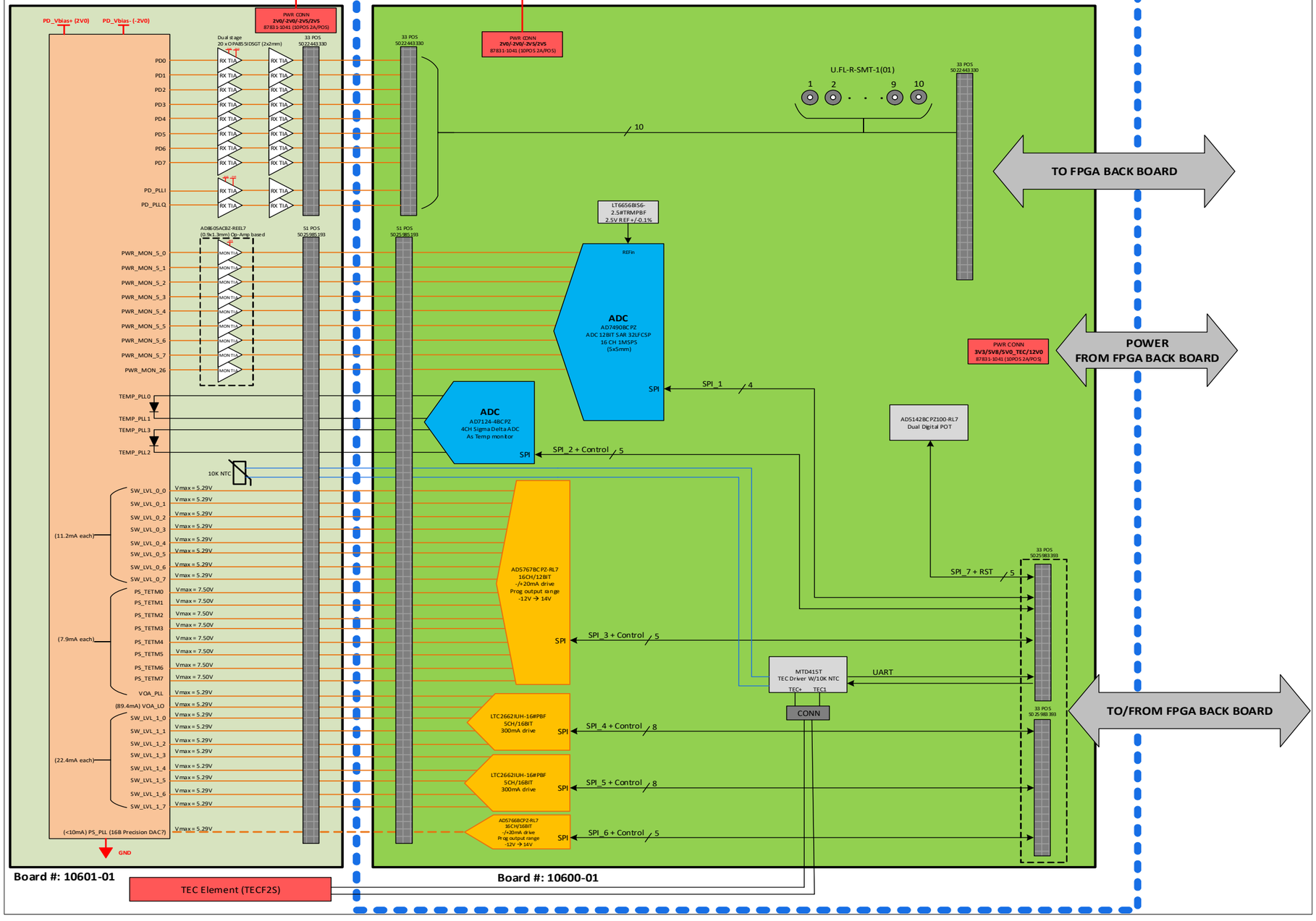
TABLE OF CONTENTS

REVISION HISTORY

REVISION	DATE	CHANGE DETAILS
0.1	26 March 2021	First Release
0.2	26 April 2021	Updated schematics based after customer's review Ref: <Lark-E Front Middle Schematic Review Notes (From customer)?
0.3	17 May 2021	Pin swap on J60 as per Layout input
0.4	24 May 2021	Pin swap on J57 to enable 180 deg flip

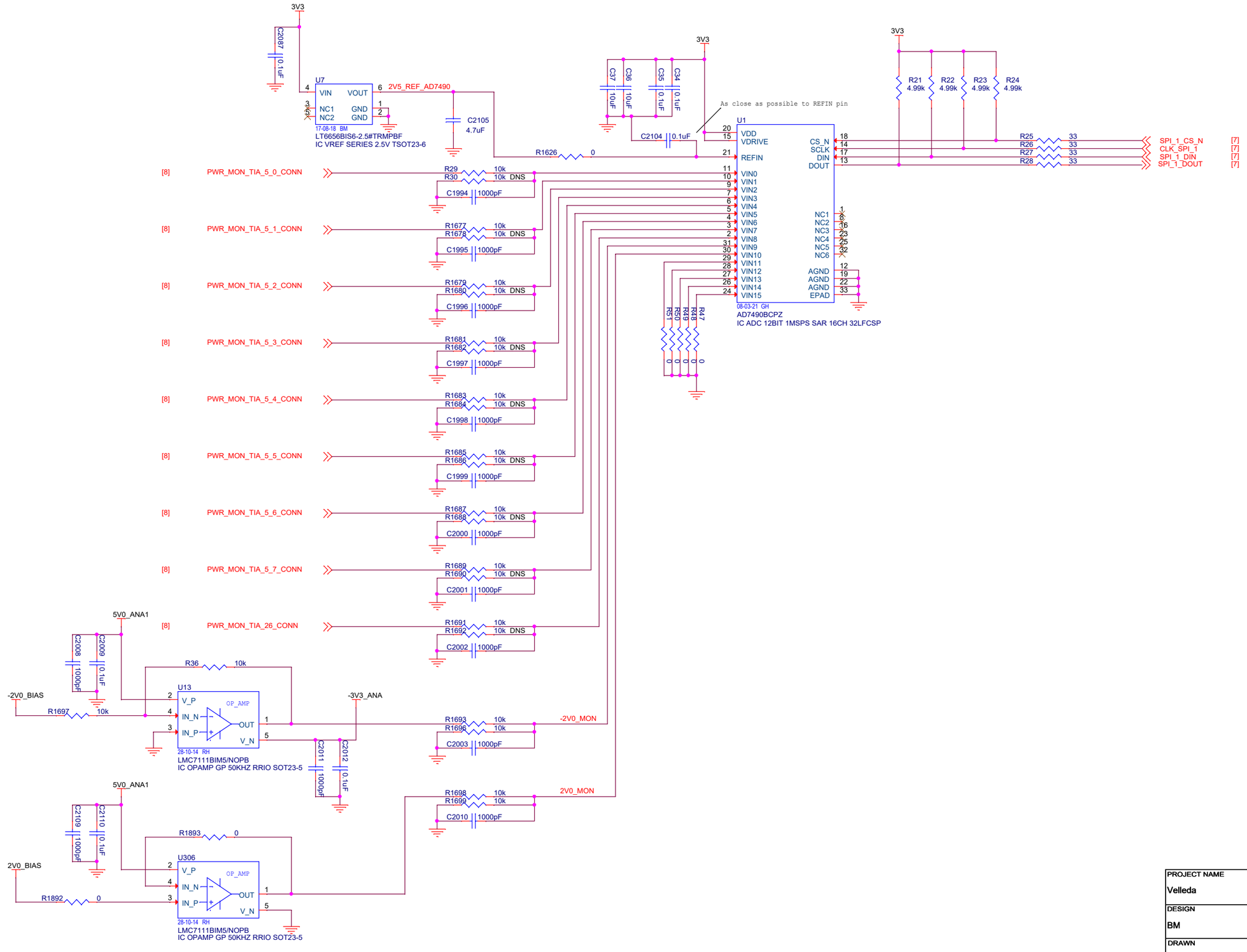
PROJECT NAME	Velleda
DESIGN	BM
DRAWN	BM
CHECK	ID
	Fidus Systems 555 Legget Drive, Suite 800
TITLE	Mid-Optical Processing Board
SUBTITLE	Table of Contents and Revision History
DRAWING NUMBER	SK-10600-01
REVISION	0.4
RELEASE DATE	24 May 2021
SHEET	1 OF 11

Current Schematic Block Diagram



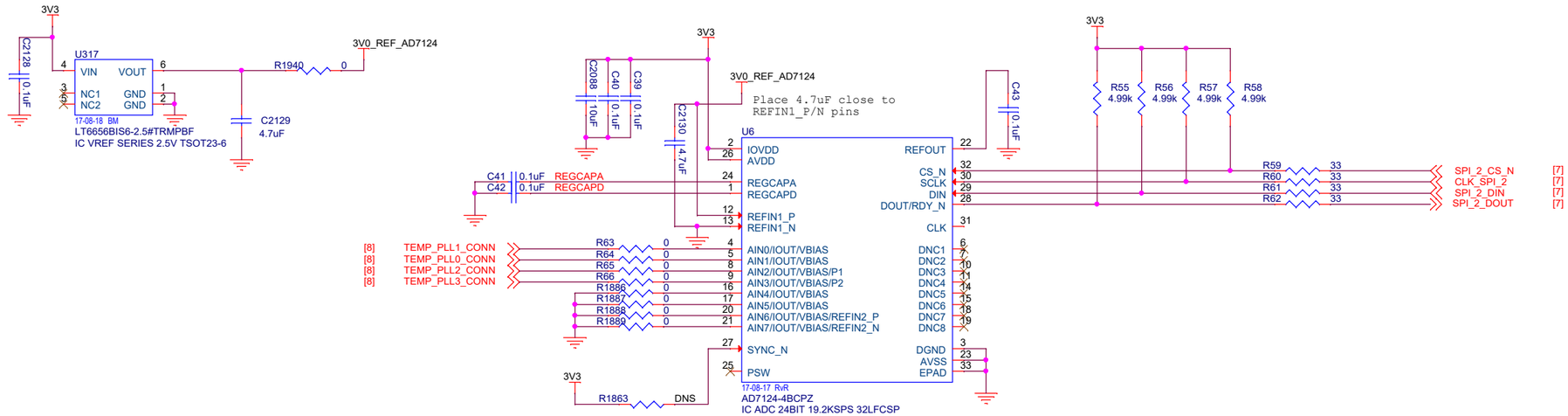
TO BE UPDATED

PROJECT NAME	Velleda
DESIGN	BM
DRAWN	BM
CHECK	ID
	fidus — Fidus Systems, 555 Legget Drive, Suite 800
TITLE	Mid-Optical Processing Board
SUBTITLE	Block Diagram
DRAWING NUMBER	SK-10600-01
REVISION	0.4
RELEASE DATE	24 May 2021
SHEET	2 OF 11

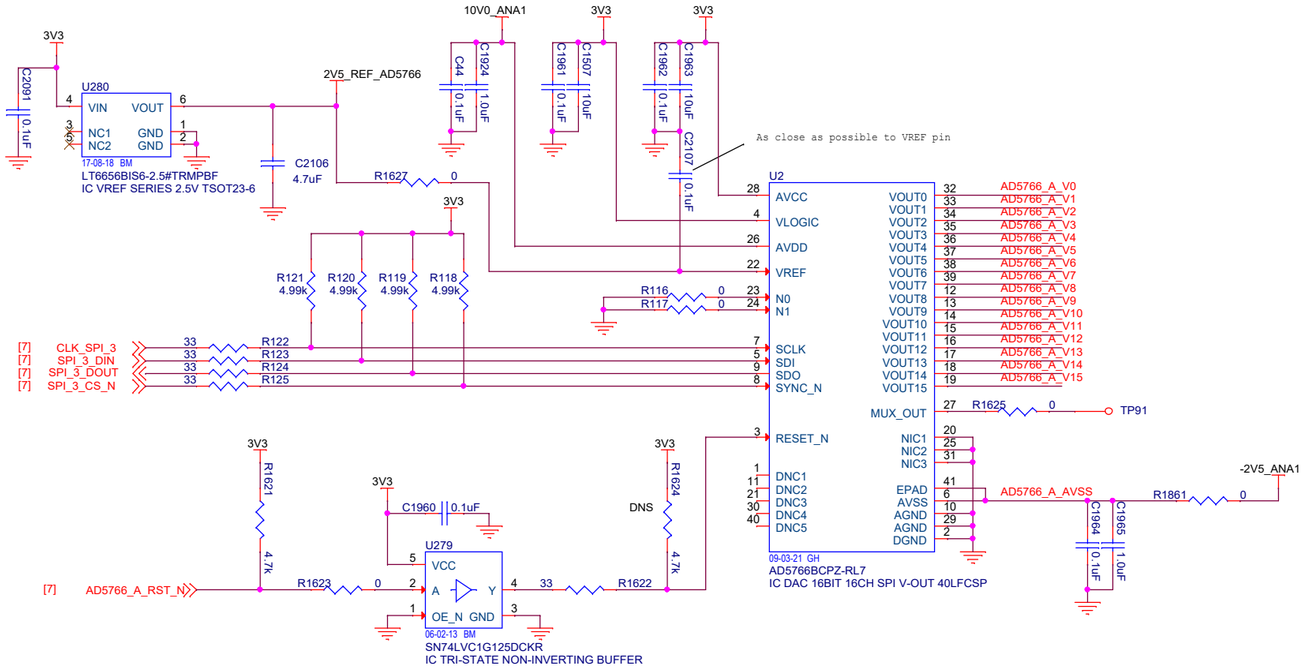


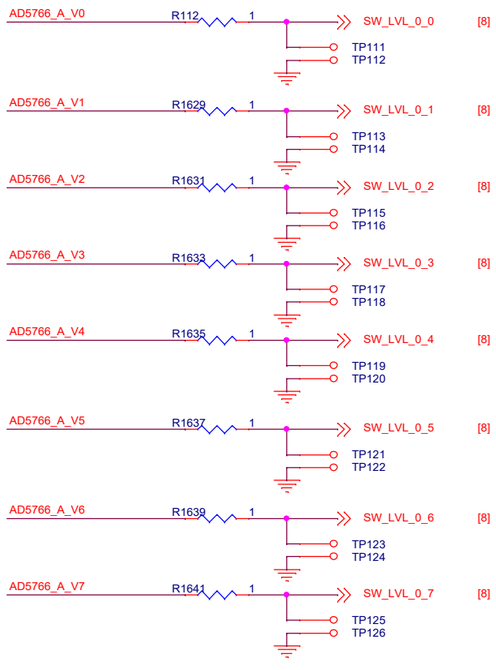
PROJECT NAME	Velleda
DESIGN	BM
DRAWN	BM
CHECK	ID
	Fidus Systems 555 Legget Drive, Suite 800
TITLE	Mid-Optical Processing Board
SUBTITLE	Power Monitor ADC
DRAWING NUMBER	SK-10600-01
REVISION	0.4
RELEASE DATE	24 May 2021
SHEET	3 OF 11

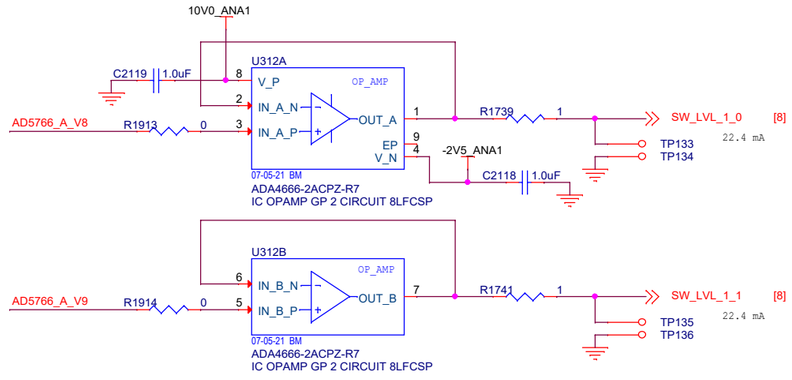
To be replaced with: LT6656BIS6-3#TRMPBF

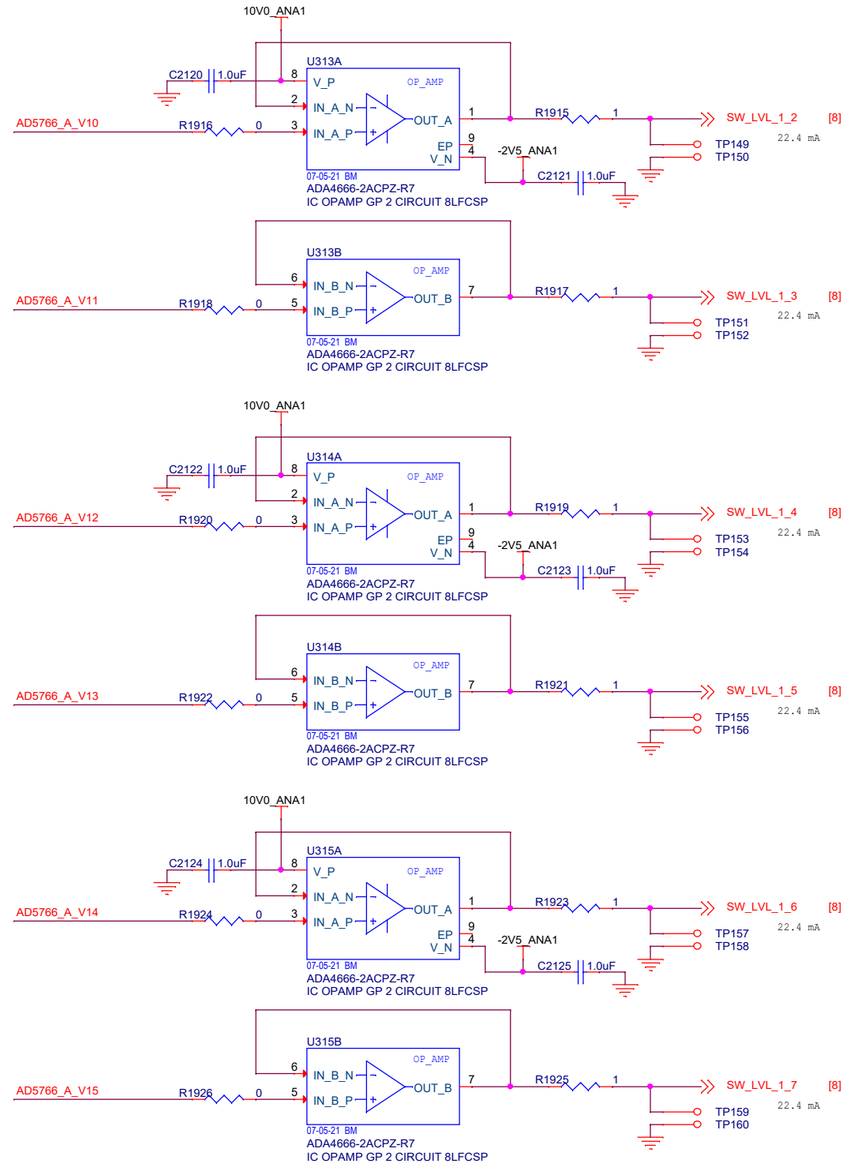


PROJECT NAME: Velleda	fidus	Fidus Systems 555 Legget Drive, Suite 800
DESIGN: BM	TITLE: Mid-Optical Processing Board	
DRAWN: BM	SUBTITLE: Temperature PLL ADC	
CHECK: ID	DRAWING NUMBER: SK-10600-01	REVISION: 0.4
	RELEASE DATE: 24 May 2021	SHEET: 4 OF 11

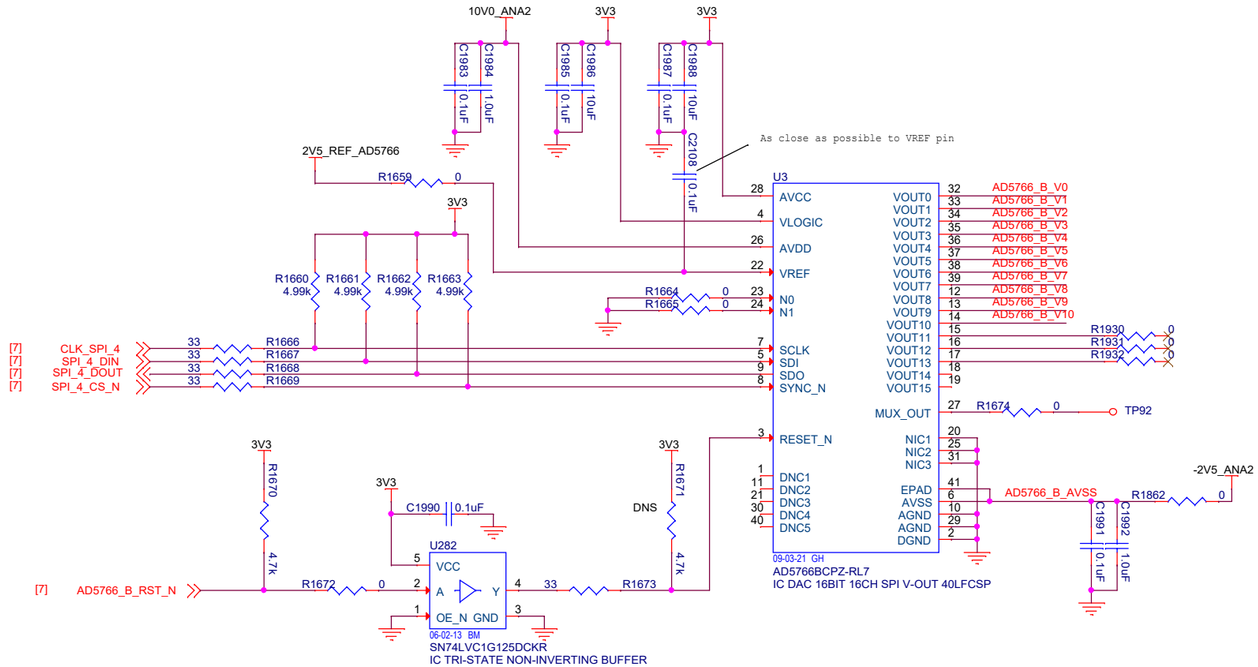




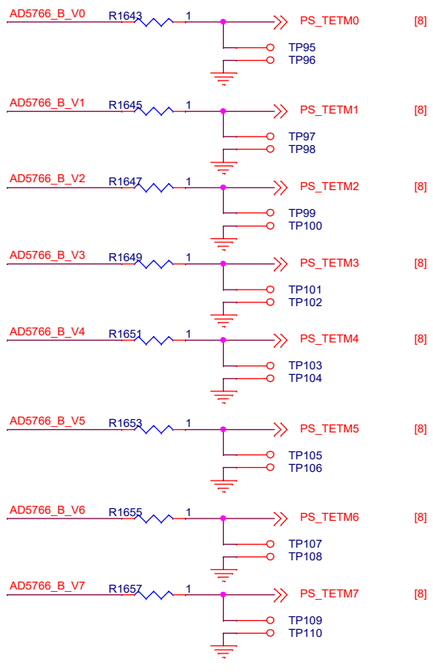


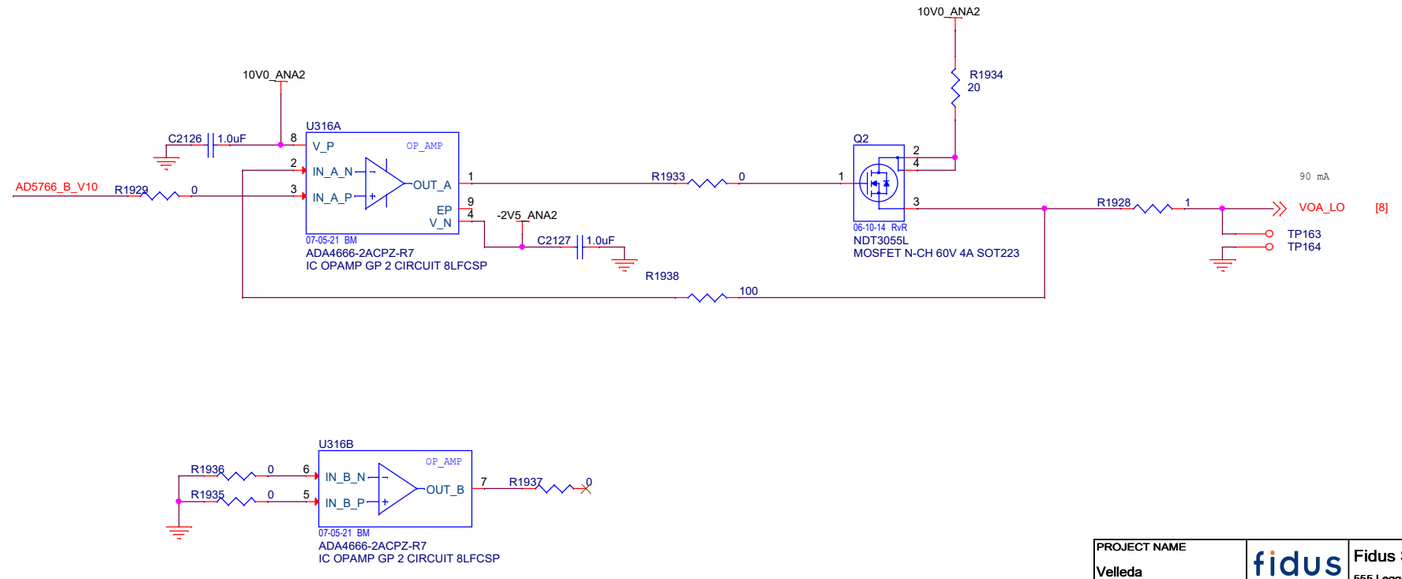


PROJECT NAME	Velleda
DESIGN	BM
DRAWN	BM
CHECK	ID
	fidus Fidus Systems, 555 Legget Drive, Suite 800
TITLE	Mid-Optical Processing Board
SUBTITLE	Heaters DACs 1/2
DRAWING NUMBER	SK-10600-01
REVISION	0.4
RELEASE DATE	24 May 2021
SHEET	5 OF 11



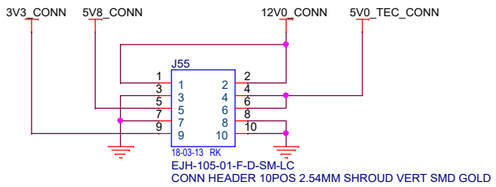
Vmax=7.5V (PS_TETMx) - 7.9mA



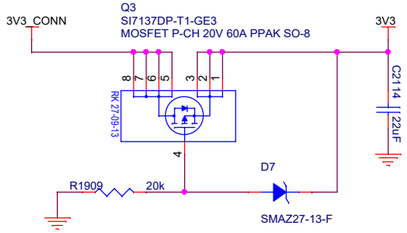


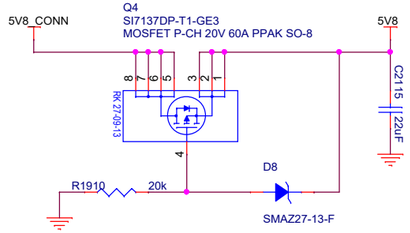
PROJECT NAME: Velleda	fidus	Fidus Systems, 555 Legget Drive, Suite 800
DESIGN: BM	TITLE: Mid-Optical Processing Board	
DRAWN: BM	SUBTITLE: Heaters DACs 2/2	
CHECK: ID	DRAWING NUMBER: SK-10600-01	REVISION: 0.4
	RELEASE DATE: 24 May 2021	SHEET: 6 OF 11

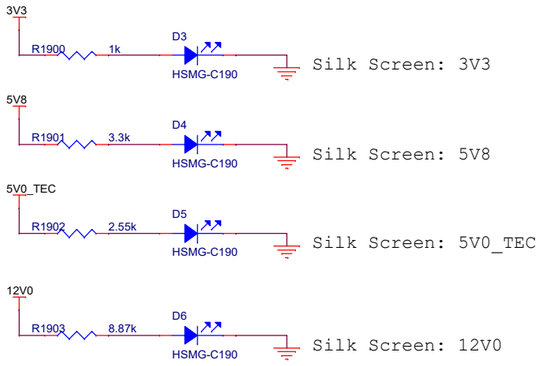
INPUT POWER FROM FPGA BOARD

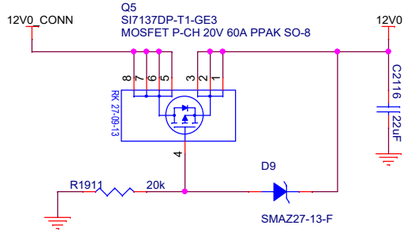


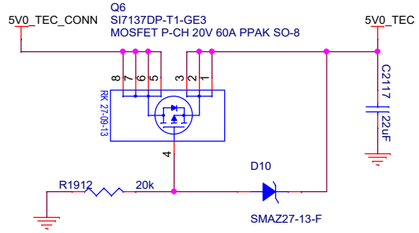
Silk Screen: Main PWR



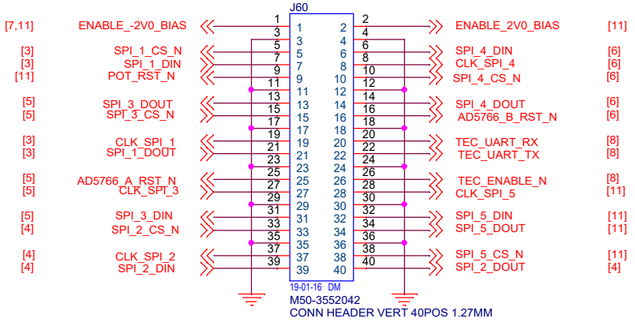


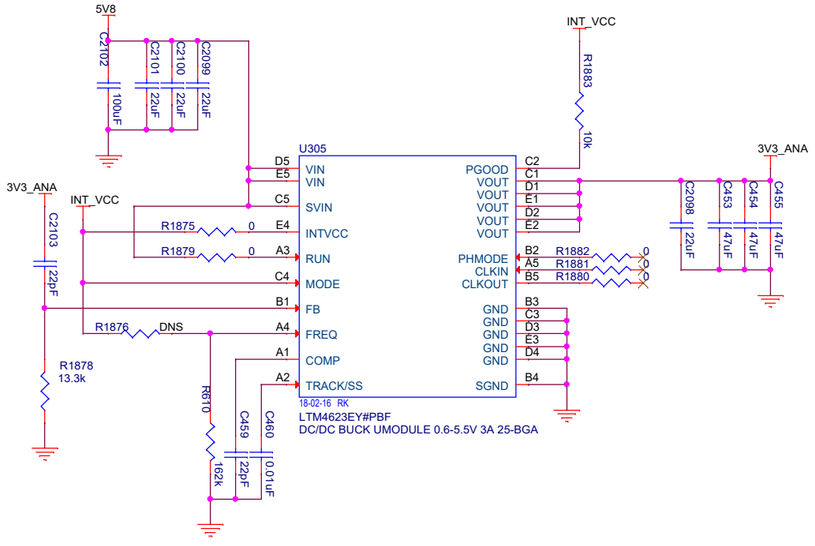






Silk Screen: SPI & CTRL





PROJECT NAME: Velleda	fidus	Fidus Systems 555 Legget Drive, Suite 800
DESIGN: BM	TITLE	Mid-Optical Processing Board
DRAWN: BM	SUBTITLE	Digital Interface Connectors
CHECK: ID	DRAWING NUMBER: SK-10600-01	REVISION: 0.4
	RELEASE DATE: 24 May 2021	SHEET: 7 OF 11

POWER TO OPTICAL HEAD BOARD

-2V5_ANA2 2V5_ANA2 -2V0_BIAS 2V0_BIAS -2V5_ANA1 2V5_ANA1

J59

18-03-13 RK
87831-1041
CONN HEADER MALE 10POS VERT LOCK

Silk Screen: Lark PWR

FROM OPTICAL HEAD BOARD

Silk Screen: RX TIA from Lark

J56

[9] PD6_TIA_CONN_IN
[9] PD4_TIA_CONN_IN
[9] PD2_TIA_CONN_IN
[9] PD0_TIA_CONN_IN
[9] PD_I_CONN_IN

PD7_TIA_CONN_IN [9]
PD5_TIA_CONN_IN [9]
PD3_TIA_CONN_IN [9]
PD1_TIA_CONN_IN [9]
PD_Q_CONN_IN [9]

I and Q are to be routed differentially

07-04-21 BM
5022443330
CONN FFC BOTTOM 33POS 0.50MM R/A

J64 J62 J65

For Both J64 and J65

Silk Screen:
Jumper pins 2-3 ---> Access to Lark NTC via J57 (Default)
Jumper pins 1-2 ---> Access to NTC via J62 (External)

RK 18-03-13
393570002
CONN TERM BLK 2POS SIDE ENT 3.5MM PCB

NTC_0_CONN
NTC_1_CONN

5V0_TEC C2084 10uF

U299
VDD VREF R1857 0 NTC_1
NTC_0 R1856 0 TEMP
TX RX R1853 R1852 TEC_UART_TX [7] TEC_UART_RX [7]
TEC_N TEC_P R1854 R1855 J61
R1898 1k ENABLE_N
STATUS R1896 0
DNC2 DNC1 GND GND GND GNDS

25-03-21 RW
MTD415T
TEC DRIVER SMT 1.5A COMPATIBLE W/10K THERMISTOR

18-03-13 RK
393570002
CONN TERM BLK 2POS SIDE ENT 3.5MM PCB

5V0_TEC C2111 0.1uF
U307
VCC A Y OE_N GND
06-02-13 BM
SN74LVC1G125DCKR
IC TRI-STATE NON-INVERTING BUFFER

5V0_TEC R1894 1k R1895 1k
D2 GRN RED
31-07-14 DB
HSMF-C165
LED BICOLOR HER/GN DIFF 0603 SMD

5V0_TEC C2112 0.1uF
3V3 C2113 0.1uF
U311
VCCA VCCB A B DIR GND
R1897 0 R1899 1k TEC_ENABLE_N [7]

08-04-14 RK
SN74LVC1T45DBVR
IC BUS TRANSCVR TRI-ST SOT23-6

GREEN = Temp within defined temp window
RED = Temp outside programmed temp window

Silk Screen: HTR and MON from Lark

J57

NTC_1_CONN
NTC_0_CONN

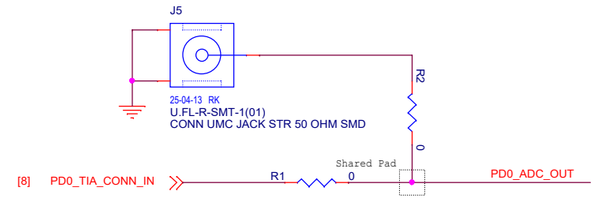
[6] PS_TETM2
[4] TEMP_PLL0_CONN
[5] SW_LVL_1_1
[4] TEMP_PLL1_CONN
[6] PS_PLL
[5] SW_LVL_1_0
[6] PS_TETM0
[6] PS_TETM1
[5] SW_LVL_0_0
[3] PWR_MON_TIA_5_6_CONN
[3] PWR_MON_TIA_5_5_CONN
[3] PWR_MON_TIA_5_4_CONN
[3] PWR_MON_TIA_5_3_CONN
[3] PWR_MON_TIA_5_2_CONN
[3] PWR_MON_TIA_5_1_CONN
[3] PWR_MON_TIA_5_0_CONN

VOA_LO [6]
SW_LVL_0_7 [5]
PS_TETM7 [6]
SW_LVL_1_7 [5]
PWR_MON_TIA_5_7_CONN [3]
SW_LVL_0_6 [5]
PWR_MON_TIA_26_CONN [3]
PS_TETM6 [6]
SW_LVL_1_6 [5]
SW_LVL_0_5 [5]
SW_LVL_1_5 [5]
PS_TETM5 [6]
SW_LVL_1_4 [5]
SW_LVL_1_3 [5]
SW_LVL_0_4 [5]
PS_TETM4 [6]
SW_LVL_0_3 [5]
TEMP_PLL3_CONN [4]
SW_LVL_1_2 [5]
PS_TETM3 [6]
TEMP_PLL2_CONN [4]
SW_LVL_0_2 [5]
SW_LVL_0_1 [5]
VOA_PLL [6]

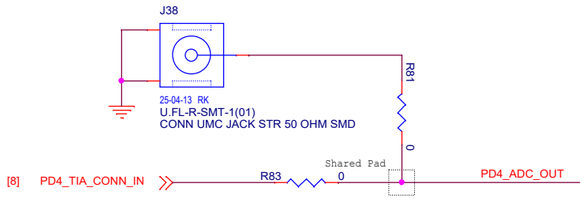
07-04-21 BM
5025985193
CONN FPC 51POS 0.30MM R/A

PROJECT NAME: Velleda	fidus	Fidus Systems, 555 Legget Drive, Suite 800
DESIGN: BM	TITLE: Mid-Optical Processing Board	
DRAWN: BM	SUBTITLE: Analog Input Connectors	
CHECK: ID	DRAWING NUMBER: SK-10600-01	REVISION: 0.4
	RELEASE DATE: 24 May 2021	SHEET: 8 OF 11

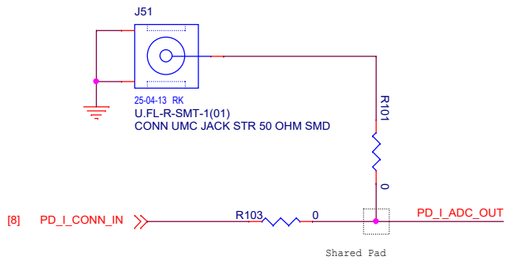
Silk Screen: RX0



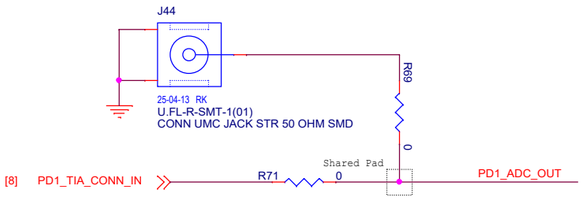
Silk Screen: RX4



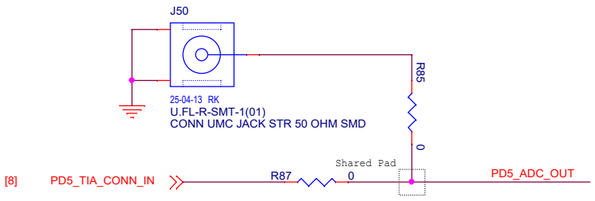
Silk Screen: RX_I



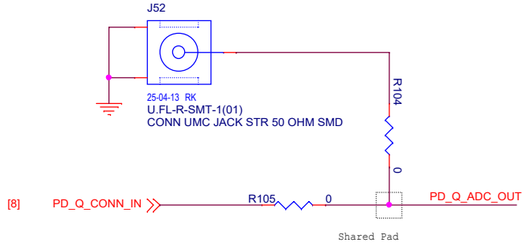
Silk Screen: RX1



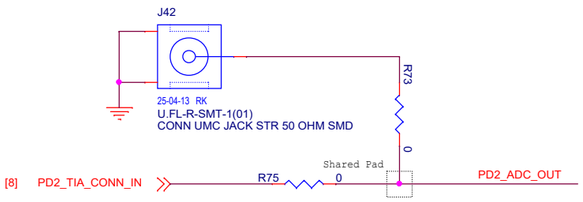
Silk Screen: RX5



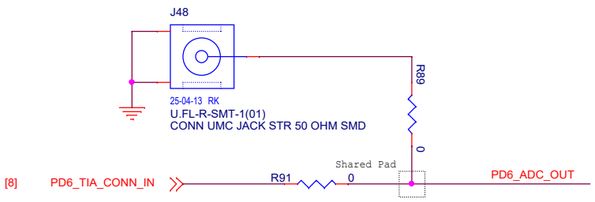
Silk Screen: RX_Q



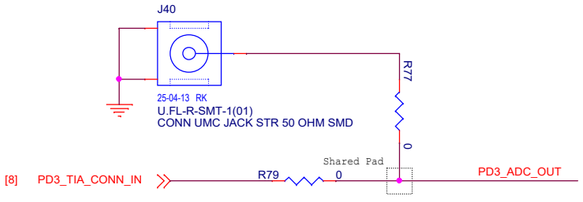
Silk Screen: RX2



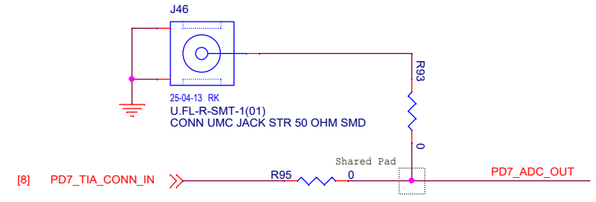
Silk Screen: RX6



Silk Screen: RX3

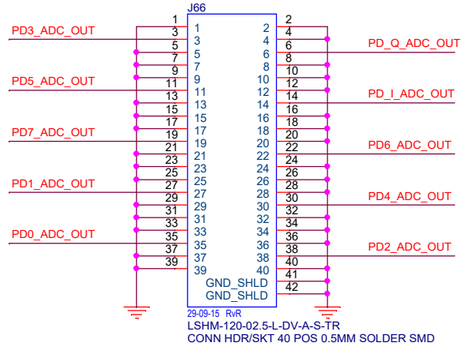


Silk Screen: RX7



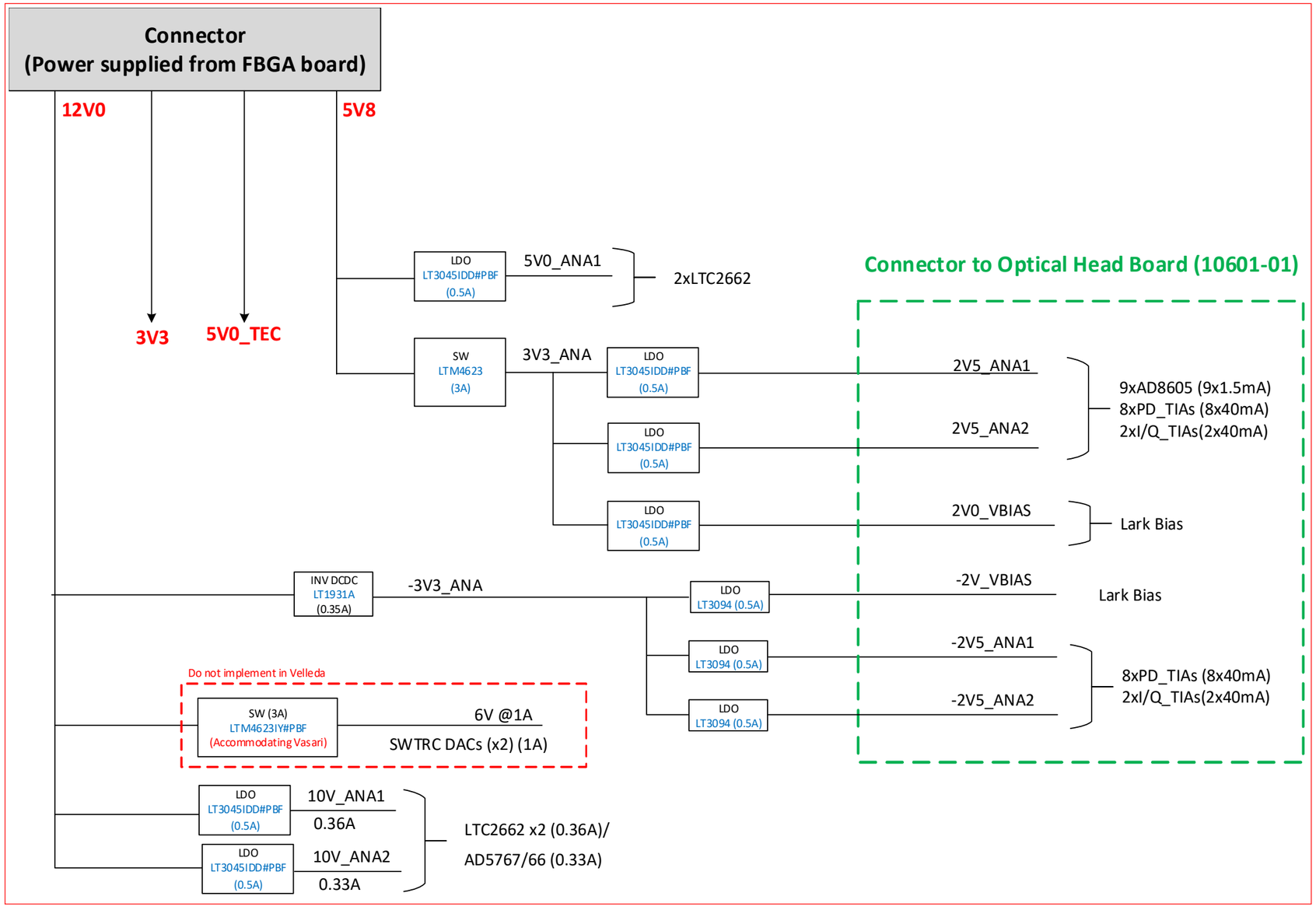
TO FPGA BACK-END BOARD

Silk Screen: RX TIA to Back-End board



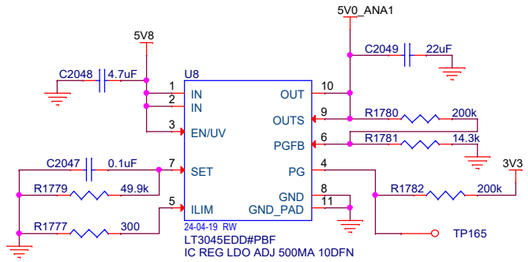
I and Q are to be routed differentially

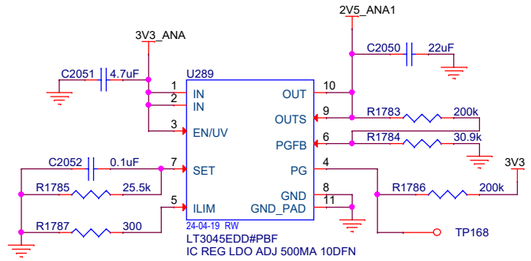
PROJECT NAME: Velleda	fidus — Fidus Systems, 555 Legget Drive, Suite 800
DESIGN: BM	TITLE: Mid-Optical Processing Board
DRAWN: BM	SUBTITLE: Analog Output Connectors & U.FL
CHECK: ID	DRAWING NUMBER: SK-10600-01 — REVISION: 0.4
	RELEASE DATE: 24 May 2021 — SHEET: 9 OF 11

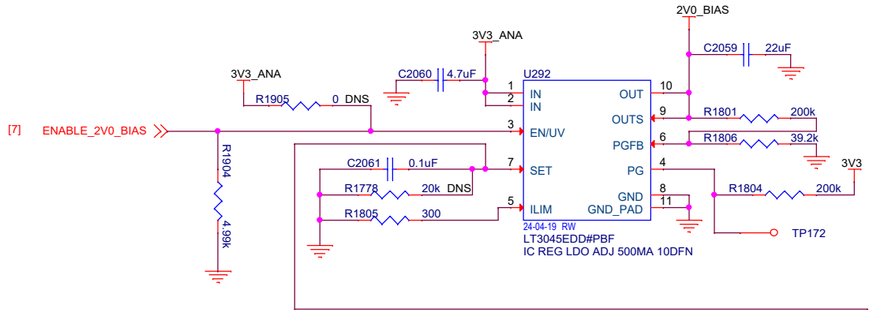


PROJECT NAME	Velleda
DESIGN	BM
DRAWN	BM
CHECK	ID
	fidus Fidus Systems, 555 Legget Drive, Suite 800
TITLE	Mid-Optical Processing Board
SUBTITLE	Power Block Diagram
DRAWING NUMBER	SK-10600-01
REVISION	0.4
RELEASE DATE	24 May 2021
SHEET	10 OF 11

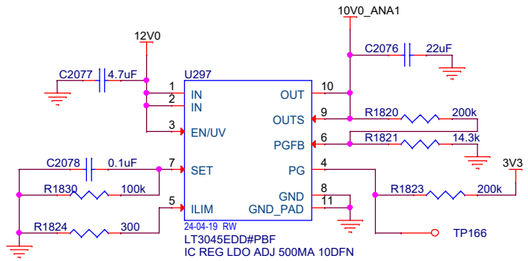
Optical Head Board supply

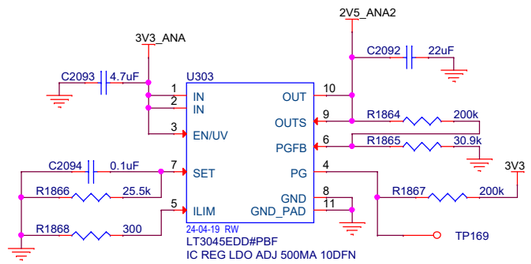


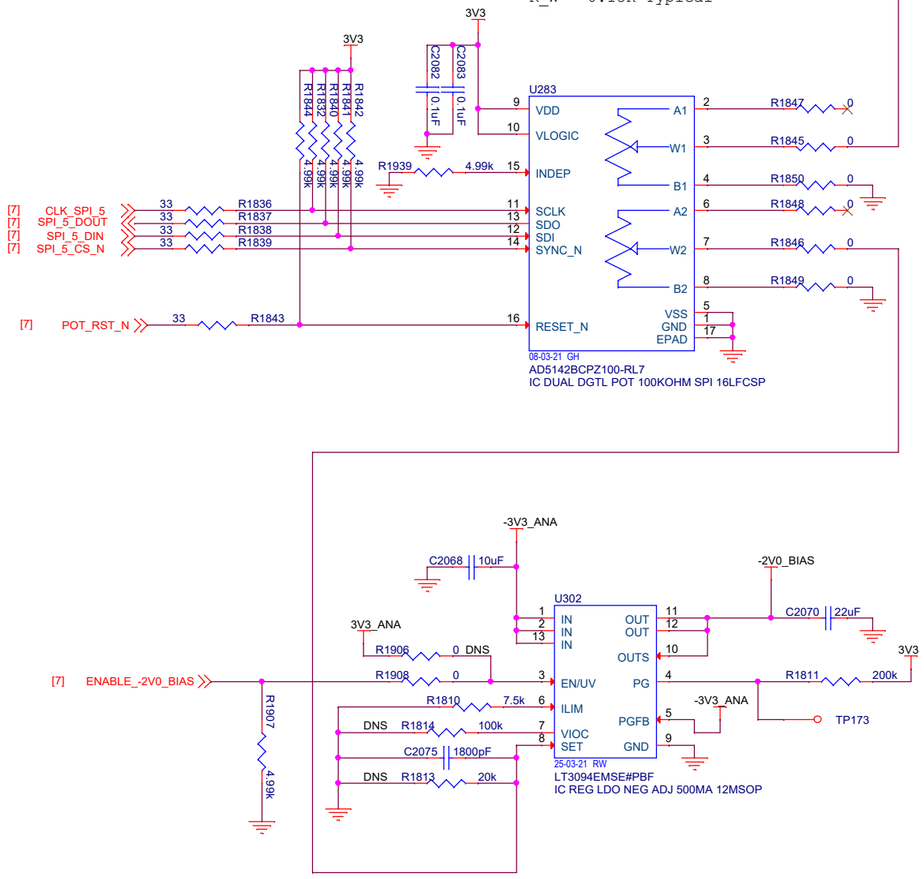




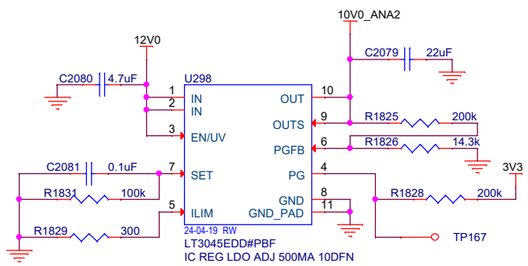
Optical Head Board supply

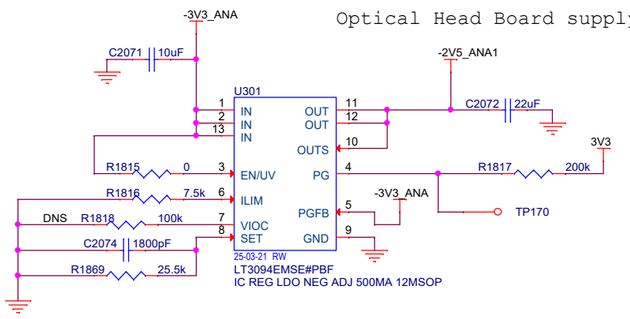




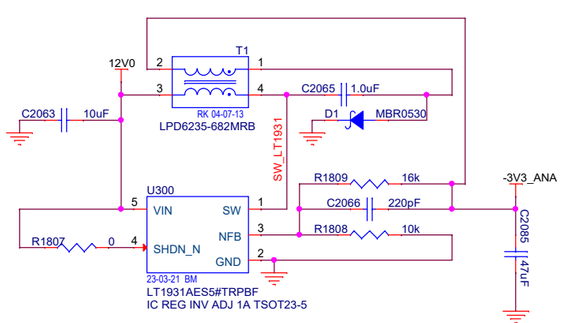


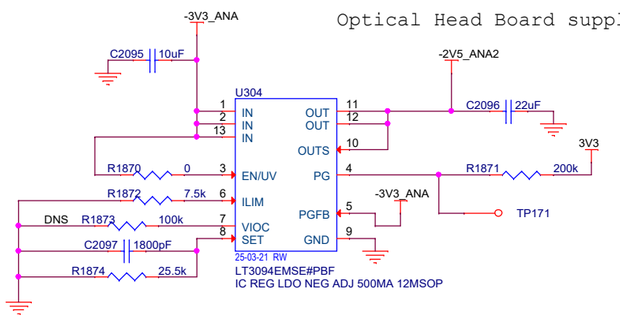
Optical Head Board supply





Optical Head Board supply





PROJECT NAME: Velleda	fidus — Fidus Systems, 555 Legget Drive, Suite 800	
DESIGN: BM	TITLE: Mid-Optical Processing Board	
DRAWN: BM	SUBTITLE: Power	
CHECK: ID	DRAWING NUMBER: SK-10600-01	REVISION: 0.4
	RELEASE DATE: 24 May 2021	SHEET: 11 OF 11