Advt. No.: IITJ/R&D(Advt.)/2022-23/53   11 Nov 2022

Project Recruitment

Applications are invited from the citizen of India for filling up the following temporary position in the Sponsored Research Project at this Institute. The position is purely temporary, initially for a period of 06 Months, and same extendable but co-terminus with the duration of the project, on contractual basis with consolidated pay. The requisite qualification, experience and others details are given below:

1.	Project No.	S/SERB/BK/20220068
2.	Project Title	Specification-guided Design of Intelligent, Secure and Dependable Hardware Architectures for Edge Computing Applications
3.	Name of the Project Investigator	Dr. Binod Kumar
4.	Duration for initial appointment	06 Months
5.	Name of the Post	Junior Research Fellow
6.	Post	01
7.	Consolidate Pay	Rs. 31,000/-HRA
8.	Minimum Qualification and Experience	Eligibility: B.E/B.Tech. in ECE/CSE/Electronics and GATE qualified Desirable Qualification: M.E./M. Tech. (VLSI) or M.E./M. Tech. (Microelectronics), Knowledge in Python/C/C++
09.	Brief description of Project	This project aims to develop hardware designs for the implementation of Artificial Intelligence (AI) algorithms on different computing devices. The goal is to enable intelligent computation on different end-use devices rather than computing on remote servers. Different aspects of hardware design such as security, dependability and robustness would also be considered during development.
10.	Job Description	The JRF will have the responsibility to carry out research and development activities for the project. Specifically, the candidate shall have to implement hardware designs for the realization of different AI algorithms under the constraints of resources such as limited power, limited area, and requirements of high accuracy and low latency. For example- trying to implement accurate image classification on mobile devices. The skills such as understanding of

		neural networks and the basics of deep learning would be a strong plus. Once the designs are finalized, these designs would be implemented on FPGA boards to validate their performance of these designs. The candidate would get opportunity to carry out research activities & publish in collaboration with other reputed worldwide universities. The project also targets the development of co-design techniques (where the neural network architecture is discovered jointly with the hardware design on which the discovered neural network will be implemented). The project aims to develop techniques that are at the industrial level and the candidate can build a very strong profile for preparing himself/herself for System-on-chip (SoC) architect/hardware design engineer/design verification engineer roles at top semiconductor companies. The project would also target any viable option of product development from the developments.
10.	Maximum Age	30 Years

The candidates possessing the requisite qualification and experience should apply through the ONLINE process up to **18 December 2022**. The candidates are advised to send a soft copy of the application with all relevant documents to *recruitment_rnd@iitj.ac.in* (*Please mention the advertisement number in the subject line of the email*).*No need to send a hard copy*.

General Instructions to Applicant(s)

1.	The post(s) is purely temporary and contractual for a period of 06 months, and extension based on satisfactory performance, but co-terminus with the duration of the project
2.	Application which is incomplete, not in prescribed format, without photograph or unsigned will be summarily rejected.
3.	Certificate in support of experience should be in proper format i.e. it should be on the organizations letter head, bear the date of issue, specific period of work, name and designation of the issuing authority along with his signature.
4.	Institute reserves the right to: a. Fix, modify or revise the eligibility conditions, age and selection criteria as per its requirements, at any time. b. Fill up the post, not to fill up the post or cancel the advertisement in whole or partly without assigning any reason. c. Place a reasonable limit on the total number of candidates to be called for the Written Test and/or Skill Test, Interview.
5.	The Institute shall verify the antecedents or documents submitted by a candidate at the time of appointment or during the tenure of the service. In case, it is detected that the documents submitted by the candidates are fake or the candidate has a clandestine antecedents/background and has suppressed the said information, then his/her services shall be terminated.
6.	Higher initial pay may be given to exceptionally qualified/deserving candidate.

7.	No TA/DA shall be paid to the candidates for attending the interview.
8.	No correspondence will be entertained from candidates regarding interview and reasons for not being called for interview.
9.	Canvassing in any form will be a disqualification.
10.	No interim correspondence will be entertained.
11.	No need to send hard copy.

Officer In-charge
Research & Development