IIT JODHPUR

FORMAL VERIFICATION (EEL7770) MINOR-1

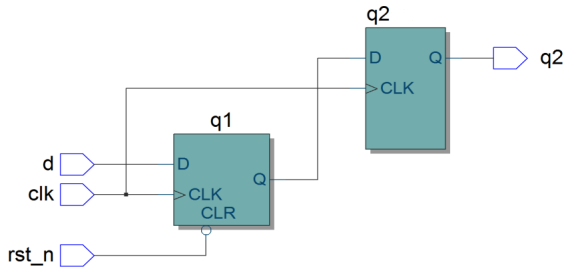
Full marks: 15, Time Limit: 1 Hour

Instructions:

1. **Answers should be brief and to the point. Unnecessary/Unrelated explanations in the answers should be avoided.**
2. **You are advised to adopt mathematical reasoning and symbols in all your answers, as far as possible. In case of any kinds of doubt/confusion, kindly take valid assumptions and answer the questions.**
3. **This exam is OPEN-BOOK. However, it is strongly advised to NOT waste time by looking up to the reference materials for every question.**

Q1. [2] Z. Kohavi (a famed scientist on automata theory) gave the below theorem that is known by his name now (Kohavi's Theorem): **Two states of a given FSM with n states are equivalent if and only if they (i.e., those 2 states) are (n-1)-equivalent.** Prove this theorem with any method.

Q2. [2 + 1] We want to implement the following gate level netlist:



Suppose the RTL designer wrote the following code to implement the above structure:

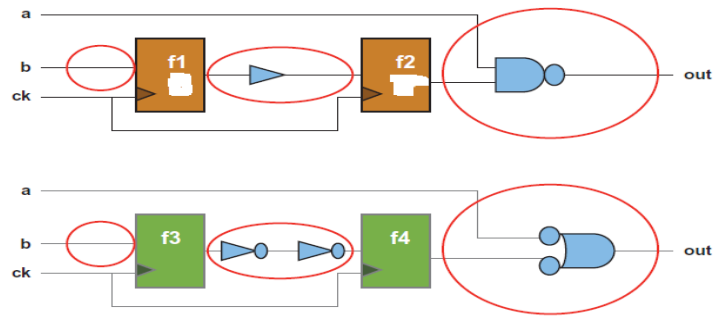
```
module Example_1 ( q2 ,d ,clk ,rst_n);
output q2 ;
input d , clk,rst_n;
reg q2 ,q1;

always @( posedge clk  or negedge rst_n )
if ( ! rst_n ) q1 <= 1 'b0 ;
else
begin
q1 <= d ;
q2 <= q1 ;
end
endmodule
```

Is the above RTL equivalent to the designers intention (i.e. the netlist portion shown above)? If your answer is NO, what would be the correct RTL code?

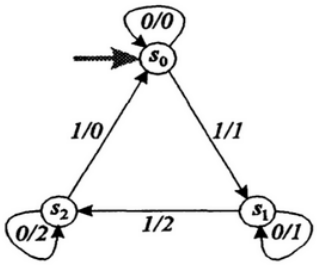
Q3. [3] Provide a formal representation/implementation of a half-adder (1-bit) and full-adder (1-bit) design?

Q4. [2] Consider the following case of 2 design implementations:

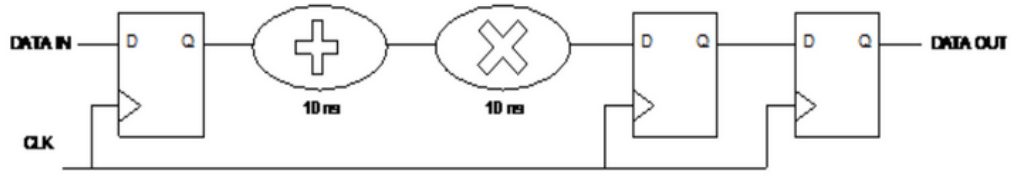


What will be the result when you perform sequential equivalence checking (SEC) on the above designs? Justify your answer.

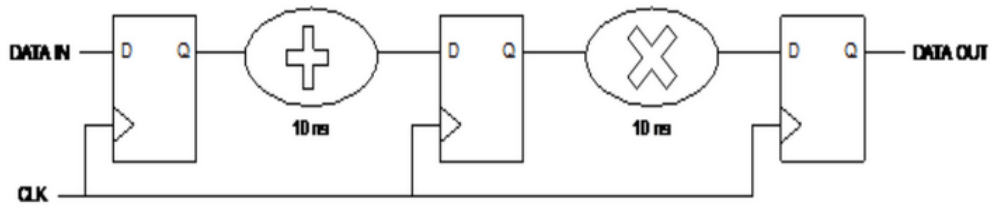
Q5. [3] With any formal method, prove that the below state transition graph represents a modulo-3 counter. (i.e., it counts 3 distinct states, 0, 1, 2) ?



Q6. [2] Retiming is a popular concept in VLSI design flow to increase the operating frequency of the design. Primarily this technique involves shifting locations of the flip-flops to adjust the delays of the combinational paths in the circuit. Argue in a formal way that the following two designs (first-before retiming, second-after retiming) are equivalent? [+ means an adder block, X means a multiplier block].



Before retiming



After retiming