IIT JODHPUR

Major Examination: EEL3090 Embedded System (May'24)

Guidelines (Total time: 120 minutes, Maximum Marks: 30):

- **NO clarification is required in any question.** In case of any doubt, assume whatever you wish to and state that in your answer. Please provide all steps of your answer very clearly.

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1. Suppose you are employed as an embedded engineer in a startup named as Bharat Defence Pvt. Ltd. (BDPL). You are asked to explain the role of a real-time operating system (which you are going to deploy) to the project lead of a missile tracking system that is being developed by BDPL. Provide your justification with an analytical model from a task scheduling viewpoint. [3]

2. An embedded system is being programmed and subsequently debugged for its application in some kind of robotics application. It is observed that the system is unable to boot. On later debugging, it is revealed that at both memory locations 0x00000000 and 0x00000004 are empty. Suggest any reason as to why this system is not booting up? [2]

3. Explain with a block diagram the necessity of a CPU in a system that is to be used for air quality monitoring in an area in the city that is known to have poor AQI (air quality index) ? [3]

4. A servo motor (shown below) can rotate approximately 180 degrees (90 in each direction) in following ways: a) Position 0 degree (1.5 ms pulse) is middle, b) Position 90 degrees (2 ms pulse) is all the way to the left, c) Position -90 degrees (1 ms pulse) is all the way to the right We use
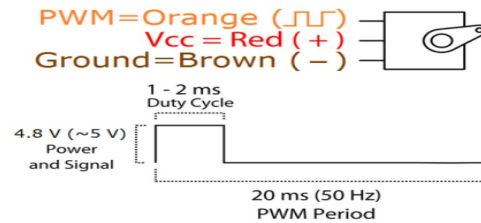
   Timer 1 Channel 1 to drive the servo motor. Suppose Timer 1 is driven by a clock of 16 MHz in up counting mode. Design PSC and ARR values for the above output signal in Mode 1. Find the following CCR1 value in order to: a) Turn the servo motor to position degree 0, b) Turn the servo motor to position degree 90, c) Turn the servo motor to position degree -90? [5 Marks]

PWM Mode	Counting Mode	Logic High	Logic Low
Mode 1	Up-counting	CNT < CCR	CNT ≥ CCR
	Down-counting	CNT ≤ CCR	CNT > CCR
Mode 2	Up-counting	CNT ≥ CCR	CNT < CCR
	Down-counting	CNT > CCR	CNT ≤ CCR

5. Suppose the SysTick interrupt occurs when PC = 0x08000044, XPSR (special-purpose program status registers) = 0x00000020, SP = 0x20000200, LR = 0x08001000. Consider the following program fragment (shown on next page). a) When executing the instruction "BX LR", how does the processor know whether it is exiting a standard subroutine or an interrupt service routine? b) The main program notices that the value of register r3 is not incremented even through the interrupt handler SysTick_Handler has been executed many times. Explain why? [1.5 + 1]

Memory Address	Instruction
	__main PROC
	…
0x08000044	MOV r3, #0
	…
	ENDP
	SysTick_Handler PROC
	EXPORT SysTick_Handler
0x0800001C	ADD r3, r3, #1
0x0800001E	ADD r4, r4, #1
0x08000020	BX lr
	ENDP

6. Compare two methods of responding external events: polling and interrupts. Discuss the advantage and disadvantage of each approach? [1.5 + 1.5]

7. The SysTick timer has a 24-bit down counter. If 4.194 MHz oscillator is used as the SysTick's input clock, can this SysTick generate an interrupt every minute? Give your explanation. [1.5]

8. Suppose an oscillator of frequency 16MHz is selected to drive ADC. Software configures the sampling time as 20 cycles, and the resolution as 12 bits. What is the maximum number of ADC conversions per second performed by this ADC module? [1.5]

9. You are to implement one-directional communication between two microcontrollers (sender and receiver) using two pins PA0 and PA1. The sender microcontroller programs these pins as output and the receiver programs them as input. PA0 is used as the control and PA1 is used to transfer the actual data. The bit-level protocol works as follows:
When it has data to transmit, the sender sends a pulse on PA0, which is a low for 2 ms, followed by a high for 2 ms. The first bit of transmission (on PA1) immediately follows, with each bit sent lasting for exactly 2 ms. Each 4-bit transmission is preceded by a pulse on PA0. The time between transmissions can be any value greater than or equal to zero. See in the timeline below that the first byte transferred is 0x29. Note that each byte of data is transmitted as two 4-bit nibbles with the bit order as 0,1,2,3 then 4,5,6,7. The vertical arrows mark when you should read the input data. You may assume that PA1 and PA0 are initialized to inputs.

   - What is the half-byte succeeding the byte 0x29 in the below timeline? [0.5 mark]
   - The overall goal of the communication is to transfer data from the sender to the receiver. Please write the function that receives one byte of PA1 data. Also write the main driver program. You may assume that you are given a function Delay1ms(). You may also assume that the software execution time is negligible compared to the Delay function. [4 marks]
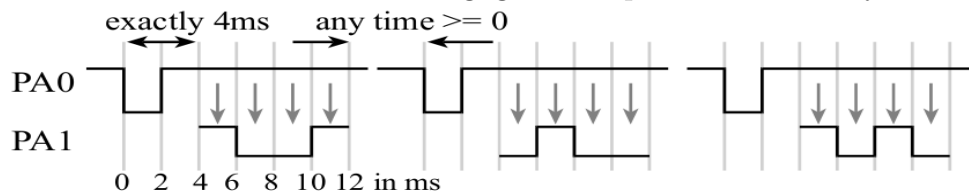
   - What is the maximum achievable bandwidth in bits/sec for this communication scenario given the above constraints? [1 mark]

10. It is known that addresses of all the interrupt handlers (aka interrupt service routines) are stored one after the other starting from 0x00000104, find P if the location where address of Pth interrupt handler is stored is known as 0x000004CC? [1 mark]

11. What data structure to use to stream data from an ISR to main program given the situation where data arrives into the ISR bursts but is processed one byte at a time in main? Why? [1 mark]

12. Mention any one use of polling/interrupt while performing an experiment with an ultrasonic sensor for an unknown distance measurement? [1 mark]