IIT JODHPUR

Major Examination: EEL7210 Hardware Software Co-Design (May'24): OPEN-BOOK

Guidelines (Total time: 120 minutes, Maximum Marks: 35):

- Please read the question paper very carefully (both sides of this paper).
- Usage of internet is **NOT** allowed.
- **NO clarification is required in any question.** In case of any doubt, assume whatever you wish to and state that in your answer. Step-wise marks would be awarded wherever applicable.

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1. Design a datapath in hardware for the program shown in the below Figure. Allocate the required registers and operators. Indicate the control inputs required by the data-path, and condition flags generated by the datapath. [5 Marks]

```
unsigned char mysqrt(unsigned int N) {
unsigned int x,j;
x = 0;
for(j= 1<<7; j != 0; j>>=1) {
x = x + j;
if( x*x > N)
x = x - j;}
return x;}
```

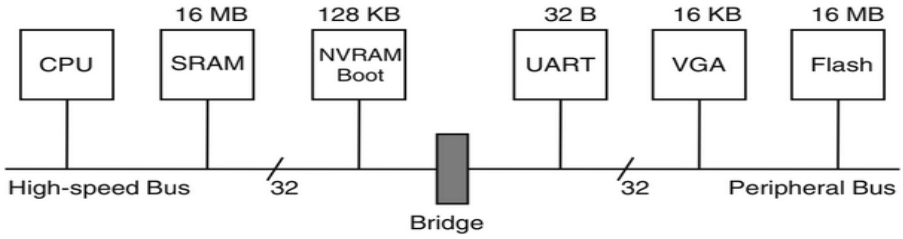
2. A custom-built processor performs operations on a stream of samples. The samples appear at fixed rate. The samples are processed using an algorithm A. Which of the following optimizations will reduce the energy consumption E needed to process a single sample? The answer for each question is one of: yes, no, impossible to decide? Please give reasons also. [1.5 + 1.5 + 1.5 + 1.5]
   - a) Rewrite the algorithm A so that it requires fewer MOPS from the processor (MOPS = Million Operations per Second). Does this reduce the energy consumption E?
   - b) Add a custom instruction B that will make algorithm A complete in only half the clock cycles. You can assume the power consumed by added hardware is negligible. Does this reduce the energy consumption E?
   - c) Increase the clock frequency of processor. Does this reduce the energy consumption E?
   - d) Lower the voltage of the processor. Does this reduce the energy consumption E?
3. Consider the following table having values of different parameters as listed below:

Parameter	Value
Time taken for each instruction (32 bit) execution by CPU	5 cycles
Power drawn for each instruction execution by CPU	0.2 nW
Time taken for each integer 1 operation by accelerator	2 cycles
Time taken for memory access (from DRAM) of inputs for 1 operation	10 cycles
Time taken for memory access (from SRAM) of inputs for 1 operation	6 cycles
Frequency of clock fed to accelerator/CPU	1 GHz
Time taken for data transfer between accelerator and CPU	4 cycles

Assume that we need to run an application for which an initial partitioning between software and hardware has been attempted. The software portion consists of 500 functions and each such

function has to be converted into fixed and variable number of instructions (32 bit/4 bytes length). The fixed component is 10 instructions for each function and the variable component depends on the numbering of the function e.g., function 1 gets converted into 1 instruction, function 2 gets converted into 2 instructions, ... function n gets converted into n instructions. The hardware component is essentially targeted to act as an accelerator that is helping the CPU. It is known that this accelerator can deliver 1500 GOPS/s performance. It is known that the SRAM is of the capacity 200 KB only. Devise a scheme to fit the software portion into the available resources (SRAM + DRAM etc.) by some optimization or a revisit of the partitioning solution (i.e., moving software into hardware etc.)? You can take proper assumptions (such as 1 software instruction is equivalent to 3 hardware operations from performance standpoint) and use the latency/energy/memory capacity values mentioned in the above Table? [6 Marks]

4. You have to design a memory map for the SoC shown in below Figure. The system contains a high-speed bus and a peripheral bus, both of them with a 32-bit address space and both of them carrying words (32 bit). The components of the system include a RISC, a 16 MB RAM memory, 128 KB of non-volatile program memory, a 16 MB Flash memory. In addition, there is a VGA peripheral and a UART peripheral. The VGA has a 16 KB video buffer memory, and the UART contains 32 bytes of transmit/receive registers. [6 marks]



5. A C function has ten inputs and ten outputs, all of them integers. The function takes 1,000 cycles to execute in software. You need to evaluate if it makes sense to build a coprocessor for this function. Assume that the function takes K cycles to execute in hardware, and that you need Q cycles to transfer a word between the software and the coprocessor over a system bus. Based on your assessment, draw the complete system diagram. Derive an analytical relationship between the fixed values K & Q for optimal system performance? [2 + 3 Marks]

6. Below is the hardware architecture of of an embedded machine vision system. Critically analyze the possibilities of hardware software co-design in the below system? Devise an analytical model for performance estimation? (Note: IMU stands for Inertial Measurement Unit, LDRAM refers to Low-power dynamic random access memory. Hint: For performance estimation, use all/some of the parameters listed in the Table provided as part of Question no. 3 above.) [7 marks]