# IIT JODHPUR

## Minor Examination: EEL71090 ML in VLSI CAD (Feb'25): TAKE-HOME

Guidelines (Total time: 1 week, Maximum Marks: 20):

- Please read the question paper very carefully .
- **Attempt any one question ONLY**. All questions carry equal marks.
- **Please refer to Assignment-1 for further details**.

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1. Suppose you convert high-level design codes such as C/C++ into RTL format via Generative AI techniques like LLM. Report the quality of the generated RTL (Verilog/VHDL) through analysis of a minimum of 30 to 50 such converted RTL design descriptions. The following parameters could be utilized for this characterization of the output from the LLM technique (You are encouraged to add any more parameters to the below list):

   - Number of lines in RTL design
   - Number of reg, wire variables
   - Number of lines in procedural blocks
   - Number of if-else blocks
   - Number of assign statements
   - Number of input/output signals

   Include features from simulation of generated RTL also if you have performed the simulation of RTL files with testbench generated again from LLM.

2. Generate assertions (preferably in SystemVerilog format) from RTL descriptions. Report the quality of assertions generated from the analysis of a minimum of 30 to 50 RTL designs. The following parameters could be utilized for this characterization of the output from the LLM technique (You are encouraged to add any more parameters to the below list):

   - Total number of SVA generated
   - Number of variables in each SVA
   - Temporal depth (no. of clock cycles) in each SVA
   - Length of antecedent and consequent in each SVA

   Include features from simulation of the generated assertions also if you have performed the simulation of the assertions within the testbench generated again from LLM.

3. Develop a RTL linter using AI techniques or from scratch through understanding of the Verilog/VHDL language syntax. Check the performance of the RTL linter on multiple designs for common RTL-related errors such as syntax issues, incorrect functionality errors etc.

4. Develop an automatic methodology for combinational-sequential design/circuit generation given input-output (I/O) pairs using any ML method. Utilize the dataset uploaded as part of Assignment-1 and comment on the accuracy of your methodology.

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