IIT JODHPUR

Minor Examination: EEL7770 Formal Verification (Sept'24) [OPEN-BOOK]

Guidelines (Total time: 120 minutes, Maximum Marks: 25):

- Please read the question paper very carefully. **NO clarification is required in any question.** In case of any doubt, assume whatever you wish to and state that in your answer.

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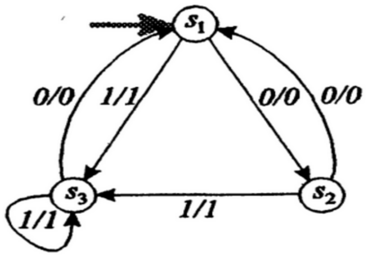
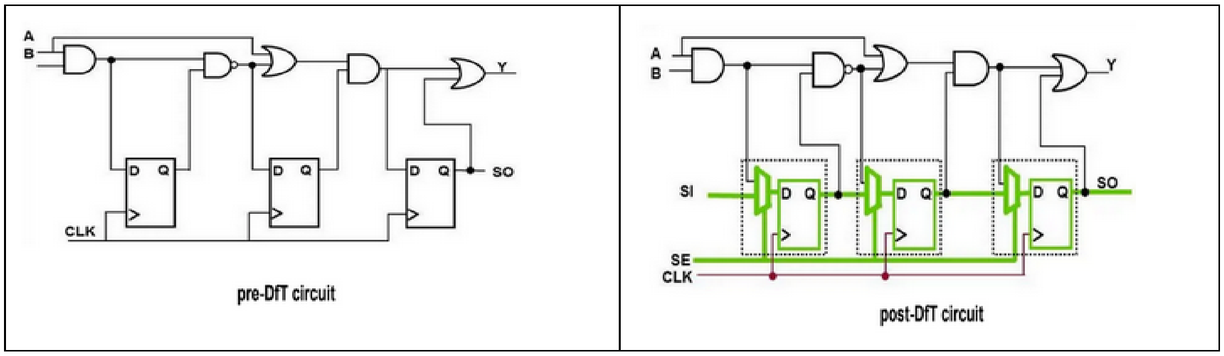
1. Majority voting is a simple technique for implementing any scheduling/arbitration logic in digital systems. Consider that we have a 4-input majority voting module design (meaning that if majority of inputs are 1, the output is 1 else if majority of inputs are 0, the output is 0). In case of a tie, this system favours 1 (i.e., output is 1 in case of a tie). Please represent this design in a formal yet compact manner? [4 Marks]

2. Justify that in the below state transition graph, all state pairs are equivalent (Hint: There are 3 state pairs: {s1,s2}, {s2,s3} and {s3,s1}). [3 Marks]



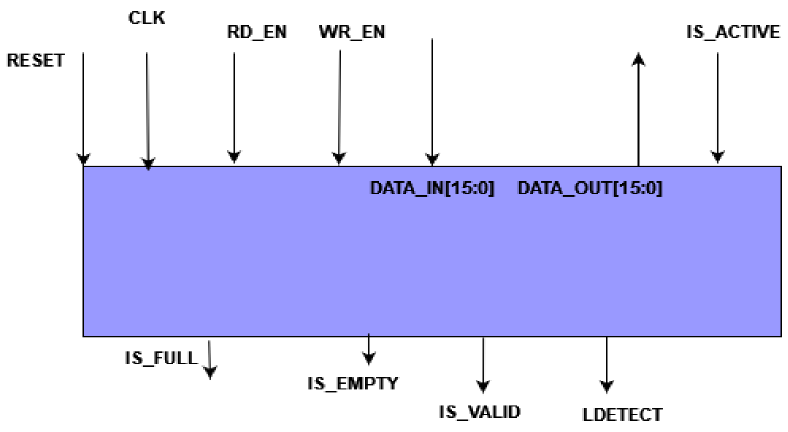
3. Design-for-testability (DfT) methodology requires that the design be modified to make it testable post fabrication. Primarily, we need to insert multiplexers into our design such that for every flip-flop of the design, an additional path is created that allows the propagation of external scan input (SI) in a manner similar to shift-register operation depending on the value provided to scan enable (SE) input of the respective multiplexers.



   Argue that pre-DFT circuit shown above is logically equivalent to post-DFT circuit? If not, explain why? [4 Marks]

4. You are tasked to verify the design of a First In First Out (FIFO) that is an important component in many memory designs. In FPGA implementations, these are often stacked to form Block Random Access Memories (BRAM). The specifications are listed as below (CLK and RESET are the clock and reset inputs to the design):

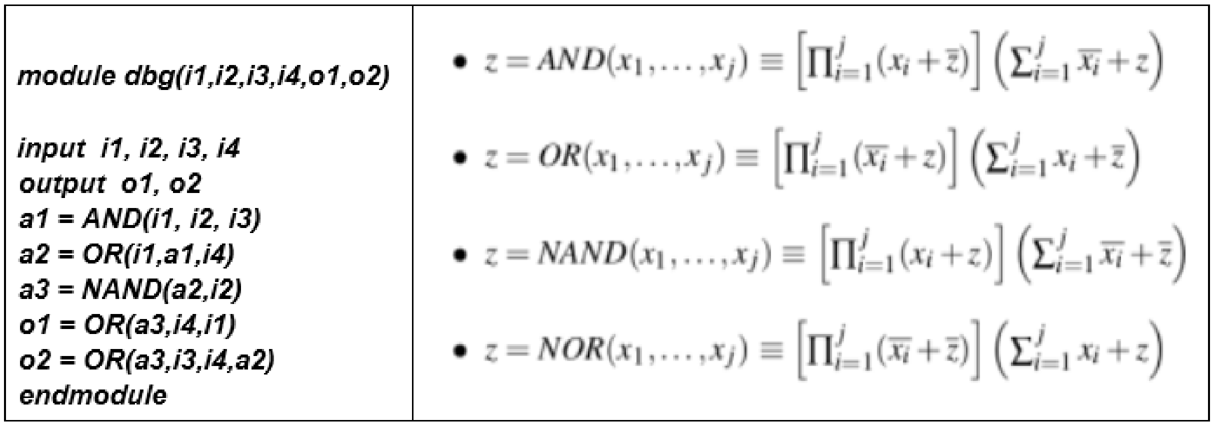
   - DATA_IN[15:0] and DATA_OUT[15:0] are respectively 16 bit data input and data output ports.



- If RD_EN is high, read from FIFO is allowed, if WR_EN is high, write to FIFO can be performed.
- Either read from or write into FIFO can happen if and only if IS_ACTIVE is high.
- IS_EMPTY is transmitted if and only if the FIFO is empty, IS_FULL is transmitted if only if the FIFO is full.
- LDETECT is transmitted as the last data block detection signal which is high if and only if the FIFO contains just BLOCK_SIZE number of data items.
- IS_VALID becomes high as soon as the valid output data are available on the DATA_OUT port.

What formal technique you can apply for carrying out this verification? How? [1 + 5 Marks]

5. During the debug of a design, it was found that the logic bug can be traced to the following module (shown in left-hand side of the figure below). Utilize satisfiability (SAT) to obtain the input sequence (values of i1,i2,i3,i4) such that both the outputs are 1 (i.e., o1=1 and o2=1). You may refer to the right hand side of the below figure for obtaining the satisfiability expressions of the gates (Note that you need to observe/interpret very carefully the multiplication and summation symbols in the following expressions). [5 Marks]



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module dbg(i1,i2,i3,i4,o1,o2)

input  i1, i2, i3, i4
output  o1, o2
a1 = AND(i1, i2, i3)
a2 = OR(i1,a1,i4)
a3 = NAND(a2,i2)
o1 = OR(a3,i4,i1)
o2 = OR(a3,i3,i4,a2)
endmodule
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- $z = AND(x_1,\ldots,x_j) \equiv \left[\prod_{i=1}^{j}(x_i+\overline{z})\right]\left(\sum_{i=1}^{j}\overline{x_i}+z\right)$
- $z = OR(x_1,\ldots,x_j) \equiv \left[\prod_{i=1}^{j}(\overline{x_i}+z)\right]\left(\sum_{i=1}^{j}x_i+\overline{z}\right)$
- $z = NAND(x_1,\ldots,x_j) \equiv \left[\prod_{i=1}^{j}(x_i+z)\right]\left(\sum_{i=1}^{j}\overline{x_i}+\overline{z}\right)$
- $z = NOR(x_1,\ldots,x_j) \equiv \left[\prod_{i=1}^{j}(\overline{x_i}+\overline{z})\right]\left(\sum_{i=1}^{j}x_i+z\right)$

6. Suppose you are working as a formal verification engineer. For the verification of a logic block, you have written a design property as *A1: It is NOT possible that along some paths, request remains high until acknowledgment starts arriving.* Your colleague has written another property as *B1: It is possible that for all paths, request is high till acknowledgement has NOT arrived.* Is *A1* same/equivalent as *B1*? Please justify your answer. [3 Marks]