IIT JODHPUR

Major Examination: Network-on-Chip (Nov'24) [OPEN-BOOK]

Guidelines (Total time: 180 minutes, Maximum Marks: 50):

- Answer **to-the-point** ONLY. Writing unnecessary statements/lengthy answers may attract penalty.
- Usage of the internet in any form to seek assistance is **NOT** allowed.
- Use mathematical reasoning and symbols as far as possible in all your answers.
- Any answer remotely similar to AI/LLM tool-generated text would lead to **NEGATIVE** marks.

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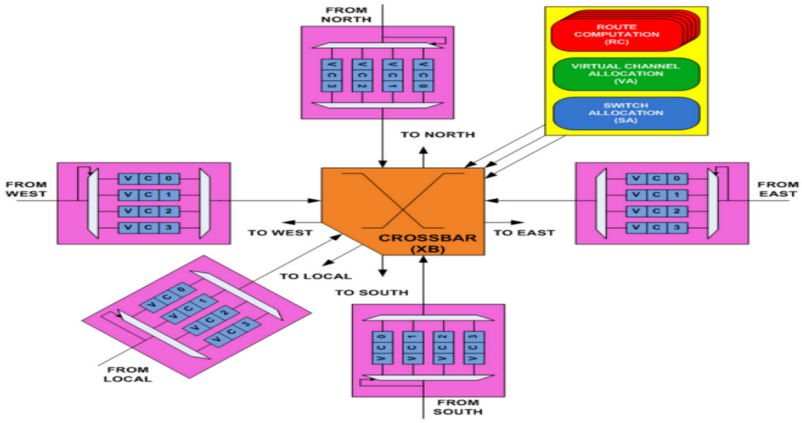
1. Different kinds of permanent faults in the NoC router architecture lead to misrouting, deadlock, traffic hot spots, packet loss, and increased latency. Hence, reliable router architecture is necessary to avoid these undesirable scenarios. **Consider the following generic router architecture as shown below. Devise a reliable router micro-architecture and find the coverage of your router design against different kinds of permanent faults (that can occur in route computation (RC) unit) ?** [4 + 3 marks]



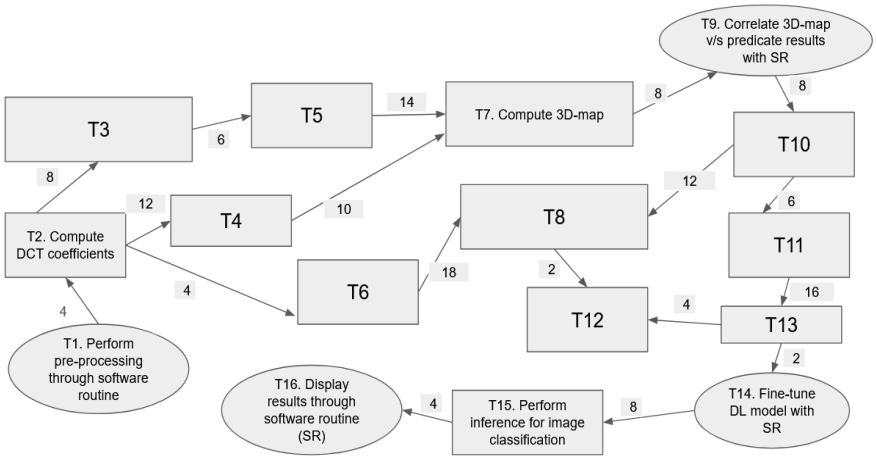
2. Consider the following routing protocol in a 2D mesh topology, where the columns are numbered from 1 to N and following restrictions are applied:

   - A packet in an even column is not allowed to make the following two turns: east to north and east to south.
   - A packet in an odd column is not allowed to make the following two turns: north to west and south to west.
   - A packet cannot make a U-Turn.

   Check if the above routing protocol is useful (one characteristic of protocol usefulness is that it is free of deadlocks)? [4 marks]

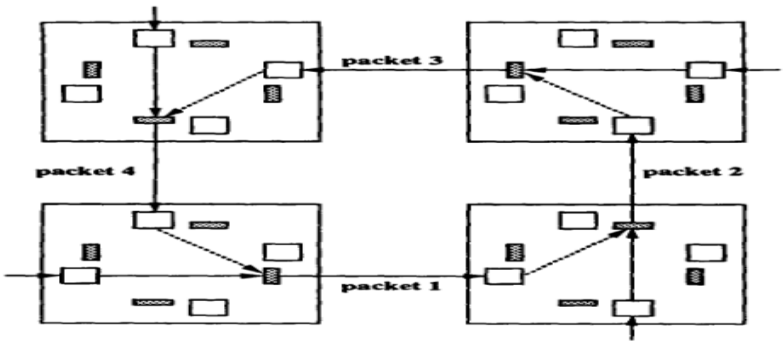
   Hint: Duato's theorem suggests that a routing function is deadlock-free if there are no cycles in its channel dependency graph.

3. Consider the design of an intelligent image processing system (I2PS). Task graph of I2PS is shown as below where few task names are provided whereas other tasks are simply numbered. These tasks need to be completed through either processor (shown by ellipse in below diagram) or custom logic (shown by rectangle in below diagram). The edges in the below diagram denote the



communication bandwidth between the respective components (equal to the number on the edge multiplied by 10 bytes). The components can also be clustered together to complete all the tasks. You are provided the information that the average hop latency (over physical link) is 6 ns, average throughput is 3 packets/cycle and the entire task graph may lead to an approximate traffic of 3K packets. **Develop a topology if we decide the processor/logic component interconnection by NoC concepts. How can you optimize the processor/logic component-router interconnection to maximize the throughput of this network and enabling the data transfer in the range of 100 to 120 ns in the worst-case scenario?** [3 + 4 marks]

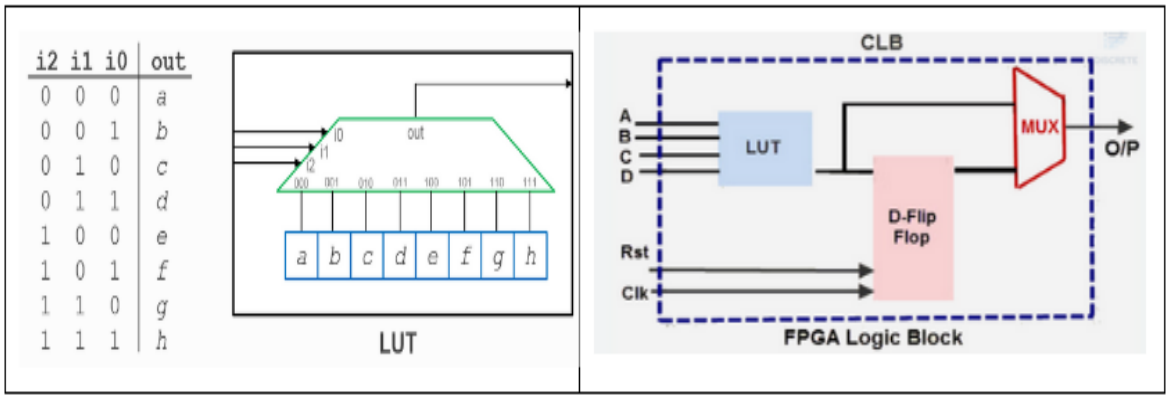
4. Wormhole flow control is a widely popular mechanism of controlling the traffic within a NoC. Consider the scenario shown below. There is a deadlock situation involving four routers and four packets in a 2D-mesh configuration. **How can this problem be resolved?** It is known to you that turn models can ensure deadlock-free routing algorithms. [5 marks]



Basically, the turn models provide a systematic methodology to the development of maximally adaptive routing algorithms through the following approach:

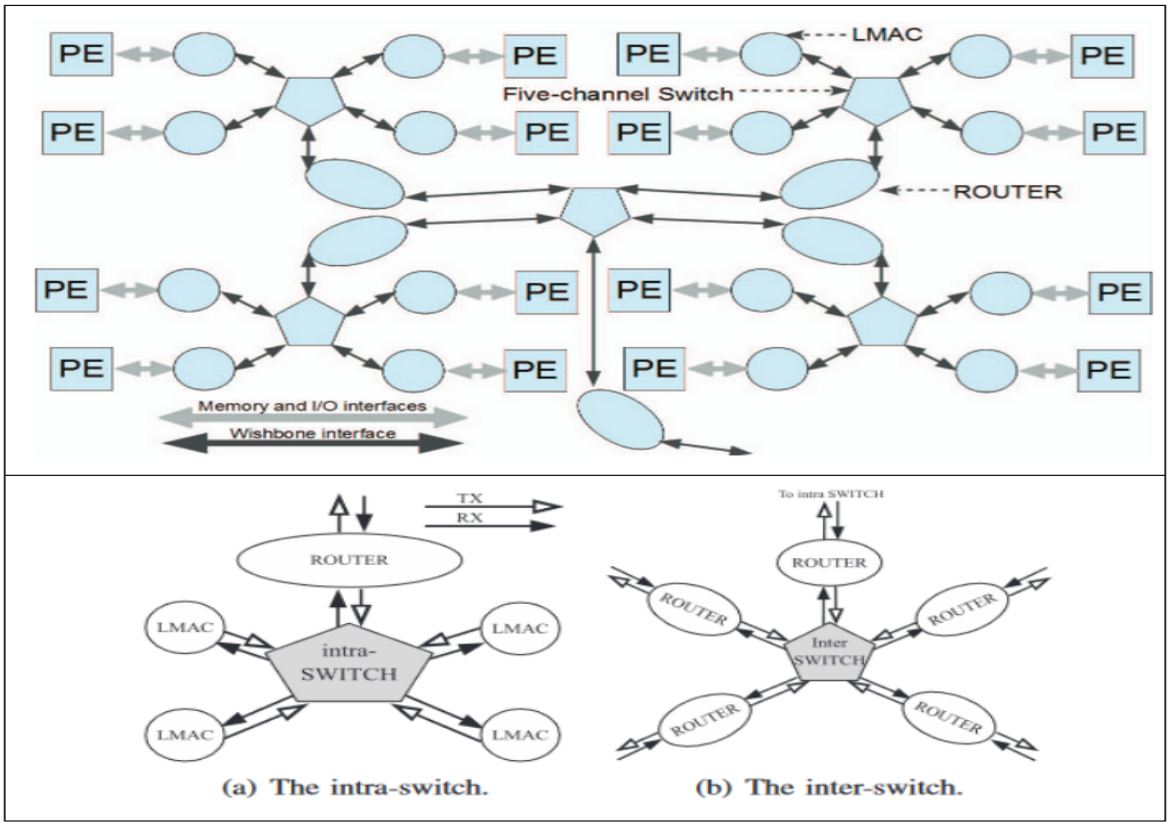
- Classify channels according to the direction in which they route packets
- Identify the turns that occur between one direction and another
- Identify the simple cycles these turns can forms
- Prohibit (ie., restrict) one turn in each cycle

5. Before manufacturing NoC designs, it is advisable to synthesize them over FPGAs. FPGA consist of look-up tables (LUTs) and configurable logic block (CLB). Below is an illustration of FPGA internal blocks. **Consider the above components (LUT, flip-flops) as basic building blocks, deduce a mapping procedure to check the functionality of a NoC system with a pipelined router microarchitecture? Note that you can check the functionality of**



a NoC system only if you are able to map all the different components (like arbiter, crossbar etc.) on the supplied FPGA platform. [7 marks]

6. While connecting a large number of processor components (or, processing elements) and memory blocks, it is required to properly use interconnection between these components. As accessing memory typically takes a large number of cycles, one idea is to use local memories that need to be tightly integrating with these memories. These memories can be managed through specialized controllers. Below figure shows one such connection where 16-node star topology where Local Memory Access Controllers (LMACs) are utilized for the interconnection (considering memory is a part of PE itself). **With a detailed/mathematical justification, deduce the routing algorithm that is ideally suited for this topology where the primary constraint is to minimize the latency as far as possible?** [6 marks]



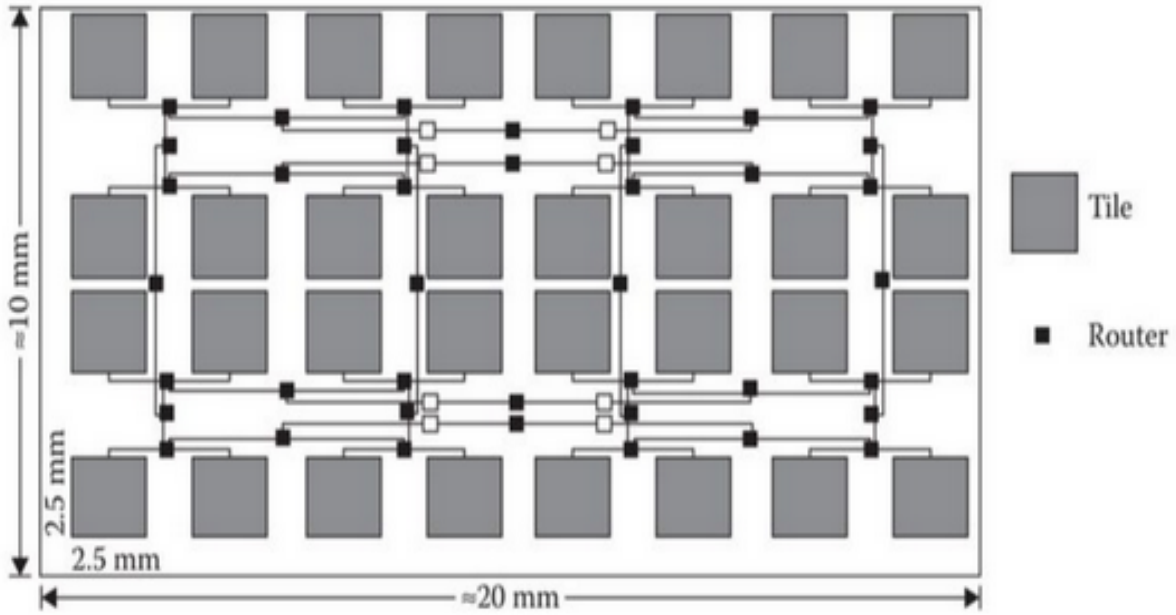
The pentagon structures in the above figure indicate the switches (elaborated in lower portion) that connect the different LMACs with the routers in the complete setup.

7. Consider the parameters mentioned in below Table:

Sl. No.	Parameter	Value
1	Average hop latency	8 ns
2	Buffer Length	4 bytes
3	Time to write one bit in buffer	0.1 ns
4	Time taken to decode address	0.8 ns
5	Packet Length	4 bytes
6	Header Length	1 byte
7	Time taken to allocate switch	0.6 ns
8	Time taken to traverse switch	3 ns
9	Body Length	2.5 bytes
10	Tail Length	0.5 byte
11	Time taken to compute a route (source to destination)	1 ns

Assuming a 5-stage pipelined router (Buffer Write, Routing Computation, Switch Allocation, Switch Traversal, Link Traversal), if we wish to design NoC with this router, **find out the total time taken by 1 packet to travel from Router A to the next Router B?** [4 marks]

8. Below is the diagram of Mesh-of-Tree (MoT) based interconnection of different tiles in a System-on-Chip (SoC). Using the parameter values as mentioned in Table of the previous question and any other realistic assumption if required, **find out the average time taken to travel from one corner to the diagonally opposite corner?** [5 marks]



9. The number of virtual channels (VCs) is an important parameter in enhancing the performance of router design in a NoC. **Propose a router design methodology/mechanism where we can vary the number of VCs per physical channel based on the traffic pattern?** [5 marks]
