IIT JODHPUR

Minor Examination: EEL7210 Hardware Software Co-Design (Feb'25): OPEN-BOOK

Guidelines (Total time: 120 minutes, Maximum Marks: 25, Usage of internet is **NOT** allowed):

- Please read the question paper very carefully (both sides of this paper).
- **NO clarification is required in any question. If you ask the invigilator any question, -5 marks penalty would be awarded.** In case of any doubt, assume whatever you wish to and state that in your answer. Step-wise marks would be awarded wherever applicable.

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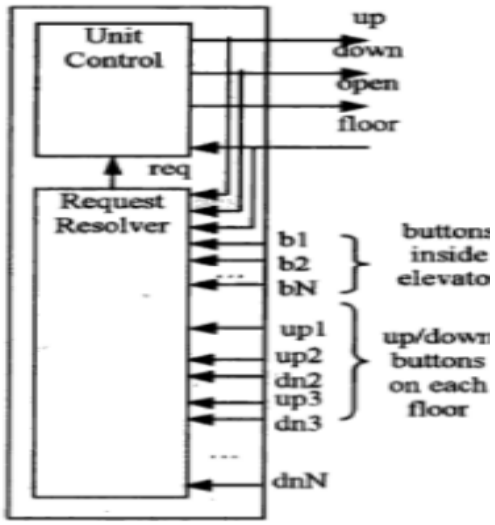
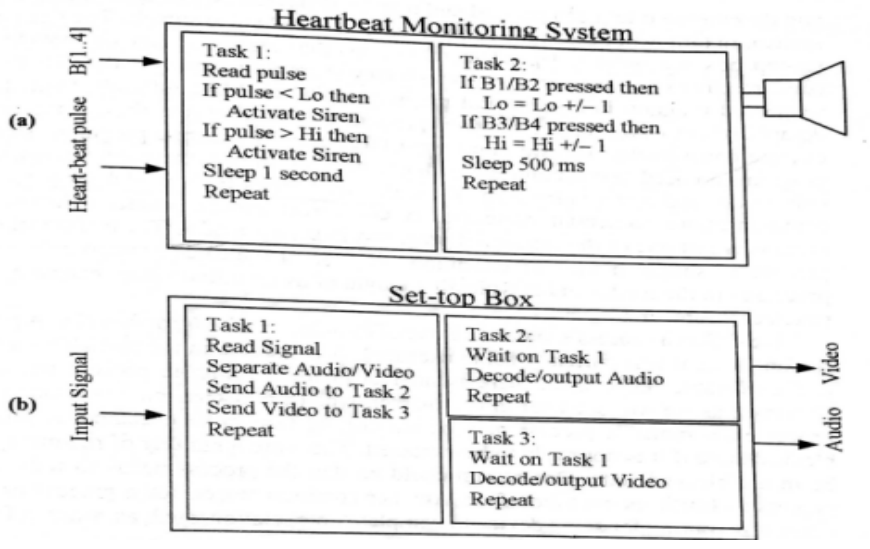
1. Suppose you are provided the specification of a lift controller: **Move the elevator either up or down to reach the requested floor. Once at requested floor, open the door for at least 10 seconds, and keep it open until the requested floor changes. Ensure the door is never open while moving. Don't change directions unless there are no higher requests when moving up or no lower requests when moving down.** How can you represent the



above system? What is the critical factor in deciding the system latency? [2 + 2]

2. Below are two examples of real-life embedded systems. What are the probable benefits of a co-design approach to develop the below systems? If you are convinced about co-design, implement this system otherwise present a hardware/software-only solution? [3 + 3]



3. Consider a scenario where we wish to connect a ARM CPU with four other peripherals either via AHB interconnection protocol/APB bridge: on-chip memory (OCM), flash memory, hardware peripherals and analog-to-digital converter (ADC). Given that the total system address space spans from 0xA0000000 to 0xE0000000. Assume that the ADC requires a capacity of 0.05 GB, on-chip memory is 1 GB, the flash memory is 1.25 GB and the perpherals utilize the remaining memory space. Find address boundaries of each block and draw all system connections properly if the goal is to process analog inputs? [3]

4. You are employed in a deep-tech startup named as "BharatSystemDesign". This startup designs a hardware-based obfuscation scheme for credit card security in the following manner. Given the credit card number "CN" is a 4-digit number (digit can be from 2 to 9), it transforms "CN" into "RCN" as follows: if digit is odd, cube it else square it. How can we design the authenticator hardware system in order to achieve real-time performance? Evaluate your design in terms of latency and try to optimize it? [3 + 2]

5. You are asked to design an object detection task by the startup employing you. Suppose that you have received an inventory that has the components with parameters listed as above. You have

Parameter	Value
Time taken for each INT instruction (32 bit) fetch & decode by CPU	5 cycles
Time taken for each FP instruction (32 bit) fetch & decode by CPU	6 cycles
Power drawn for each INT instruction fetch & decode by CPU	0.2 nW
Power drawn for each FP instruction fetch & decode by CPU	0.5 nW
Power drawn for each integer ALU operation by CPU	0.5 nW
Time taken for each integer ALU operation by CPU	4 cycles
Power drawn for each FP ALU operation by CPU	2 nW
Time taken for each FP ALU operation by CPU	7 cycles
Time taken for memory access (from DRAM) of inputs	10 cycles
Time taken for memory access (from SRAM) of inputs	6 cycles
Capacity of DRAM	8 MB
Capacity of SRAM	10KB
Frequency of clock being fed to CPU	1 GHz

   primarily 2 choices: a CPU having values as mentioned above and a hardware/ASIC that has a collection of 4 similar ALUs (2 FP-type and 2-INT type with respective control circuitry) within the same area as the CPU. To outshine your colleagues in this startup, you decide to explore if co-design would be a better option then to conventional methods. You are told by the compiler team that the executable (generated from the application) has approximately 10K instructions (40% involve FP operations, remaining are INT-operand instructions). You decide to simultaneously somehow optimize the latency and the power dissipation of the system using co-design approach. Note that most instructions in this executable are data-related and hence computationally intensive. For all such data-related instructions, it can be assumed that they can be fed to the respective ALUs present in the ASIC made available to you. Show your calculations and your design that you need to present to your boss in order to get the approval of implementation. [Please assume any missing data that you may need to solve this question.] [2 + 2]

6. A large number of deep learning models such as Transformers require matrix multiplication in some form. Suggest the datapath and control structures (if any) that would be required to implement this multiplier design given two large matrices (first of dimension AxB and second of dimension BxC). In this particular problem, is there any scope of hardware-software co-design approach? [3]