IIT JODHPUR

Minor-2 Examination: EEL7210 Hardware Software Co-Design (Mar'24): OPEN-BOOK

Guidelines (Total time: 60 minutes, Maximum Marks: 20):

- Please read the question paper very carefully (both sides of this paper).
- Usage of internet is **NOT** allowed.
- **NO clarification is required in any question. If you ask the invigilator any question, -5 penalty would be awarded.** In case of any doubt, assume whatever you wish to and state that in your answer. Step-wise marks would be awarded wherever applicable.

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1. Consider a scenario where we wish to connect a ARM CPU with four other peripherals either via AHB interconnection protocol/APB bridge: a multi-functionality keyboard, on-chip memory, flash memory and analog-to-digital converter (ADC).
   (a) Given that the total system address space that is available to us spans from 0x00000000 to 0xC0000000. Assume that the keyboard requires a memory capacity of 0.25 GB, on-chip memory is 1 GB, the flash memory is 1.25 GB and the ADC is allowed to utilize the remaining memory space. Find address boundaries of each peripheral and draw all system connections properly?
   (b) Given that CPU is running at a clock frequency of 1.25 GHz however, the APB bridge requires a slower clock. So, the APB bridge receives the CPU clock after division by the contents of a register named as PRESCALE. Given that the contents of PRESCALE register is 0x0D, find the time taken for one word transfer by the keyboard in the best possible scenario? [3 + 1]

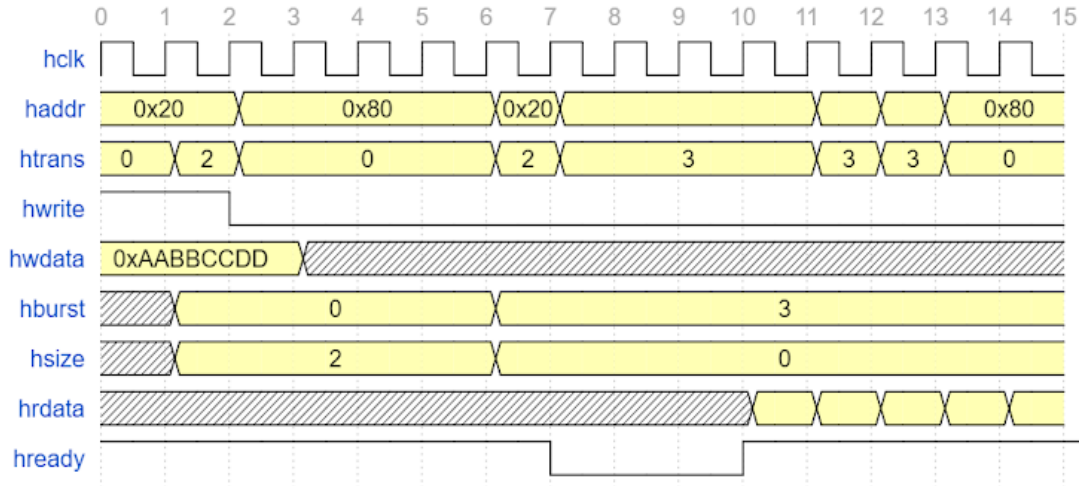
2. Consider the following table having values of different parameters as listed below:

Parameter	Value
Time taken for each instruction (32 bit) execution by CPU	5 cycles
Power drawn for each instruction execution by CPU	0.2 nW
Time taken for each integer MAC operation by accelerator	2 cycles
Power drawn for each integer MAC operation by accelerator	0.3 nW
Power drawn for each integer MAC operation by CPU	0.5 nW
Time taken for each integer MAC operation by CPU	4 cycles
Time taken for memory access (from DRAM) of inputs for MAC operation	10 cycles
Time taken for memory access (from SRAM) of inputs for MAC operation	6 cycles
Capacity of DRAM	8 MB
Capacity of SRAM	10 KB
Frequency of clock fed to accelerator/CPU	1 GHz
Time taken for data transfer between accelerator and CPU	4 cycles

   Given a scenario where a face recognition task is to be executed by your design. As components, you have got a CPU with parameters shown in the above table, a hardware accelerator capable of executing multiply accumulate (MAC) operations, external SRAM, external DRAM with the parameters listed above and an on-chip memory (having a capacity of 48.5 KB). You have few options for developing your design: (a) all execution on CPU along with memory access from DRAM only (b) all execution on CPU along with memory access both from DRAM and SRAM (c) instruction execution on a CPU along with MAC operation handled by accelerator and memory access both from DRAM and SRAM (d) CPU along with accelerator and memory access only from SRAM, and (e) CPU along with accelerator and memory access only from DRAM. Develop your

design (i.e., show the final design components with interconnections and all relevant calculations) in order to minimize power consumption and maximize performance given that this application is compiled as 12K instructions and two chunks of 8K and 5K MAC operations. Note: For simplicity, we can assume that each MAC operation is a single-byte instruction (8 bits). [2 + 2 + 3]

3. Assume that you are working as a verification engineer in a semiconductor company. You simulated one AHB-Lite protocol implementation to get the below simulation dump: [2 + 2 +2 + 1]



- (a) Please identify as how many write and read bursts take place in above dump?
- (b) Please fill up the values of **haddr** at the blank locations in above dump?
- (c) Mention the values of **hrdata** at the blank (empty) locations in above dump?
- (d) From the above diagram, identify the number of bytes of data that are read by the slave during the read transaction?

4. Re-design (i.e., suggest some changes to the standard implementation) the APB protocol to manage transfers between a master (operational at 90 MHz) and two slaves with different clock frequencies: slave 1 (running at 90 MHz) and slave 2 (running at 60 MHz)? [2]
