IIT JODHPUR

Minor Examination: EEL7770 Formal Verification (OPEN-BOOK)

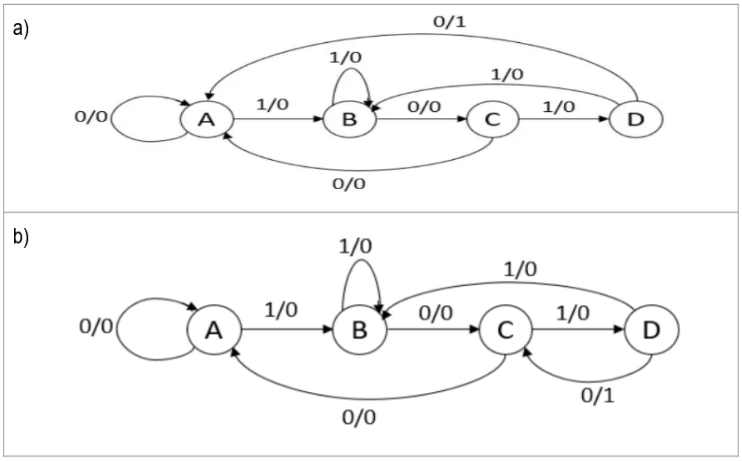
Guidelines (Total time: 120 minutes, Maximum Marks: 25):

- Please read the question paper very carefully. **NO clarification is required in any question.** In case of any doubt, assume whatever you wish to and state that in your answer.
- Usage of assistance from internet/any LLM tool is NOT allowed.

---

1. Canonical forms are important for representing the designs in order to perform their formal verification. Let's say we want to represent 2-bit adders canonically. ROBDD is one technique for representing the designs canonically. Briefly explain how you can obtain the ROBDD of this adder for the **sum** output. How can the same ROBDD extended for representing 3-bit adders? [2+2]

2. You are an intern in a semiconductor company. You were asked to implement a finite state machine model (as shown in a) below) for some design. Another intern has implemented the finite state machine model (as shown in b) below) for the same some design. Are both these FSM models equivalent? What is the application (i.e., usage) of the design corresponding to this FSM? [3+1]

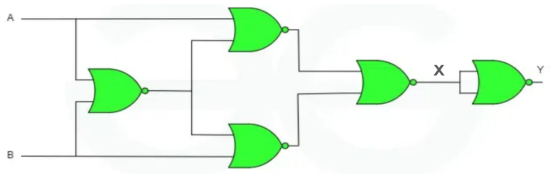


3. Consider the state transition table as shown below.

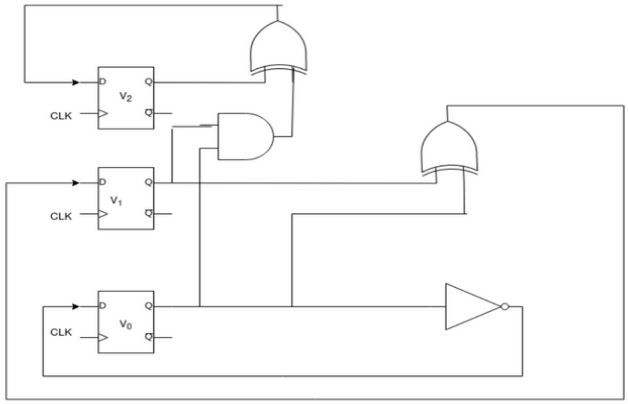
Input Sequence	Present State	Next State $X=0$	Next State $X=1$	Present Output $X=0$	Present Output $X=1$
reset	A	B	C	0	0
0	B	D	E	0	0
1	C	F	G	0	0
00	D	H	I	0	0
01	E	J	K	0	0
10	F	L	M	0	0
11	G	N	P	0	0
000	H	A	A	0	0
001	I	A	A	0	0
010	J	A	A	0	0
011	K	A	A	0	0
100	L	A	A	0	1
101	M	A	A	1	0
110	N	A	A	0	0
111	P	A	A	0	0

With a proper formulation, find the equivalent states for the below design? What is the final number of states in this FSM after reducing the state to the maximum extent possible? How? [3+2]

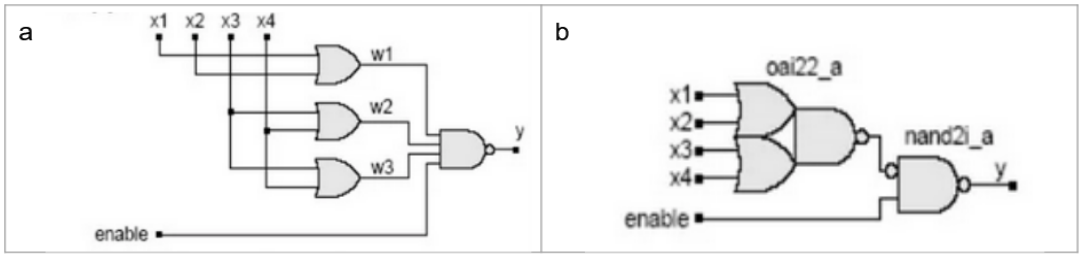
4. In the diagram below, your manager has asked you to prove that if A=B=1, X can never be 0 in the below design block With the help of suitable satisfiability formulation? [3]



5. Counters are very important logical components in digital systems. Therefore, formal verification is utilized to check the correctness of these counters in an exhaustive manner. Using any suitable formal verification technique, check if this counter design reaches the count of 4? As shown, v_0, v_1 and v_2 are three flip-flops, therefore, you need to check if it is possible to reach the state of 100 ($v_2v_1v_0$). Also, you are requested to compute the reachable states of this design (reachable states are those which we can reach starting from the initial/reset state.) ? [3 + 1.5]



6. With any formal technique, prove that design shown in (a) is equivalent to that shown in (b)? Hint: oai22_a is a complex logic gate meaning OR-AND-INVERT functionalities. [2.5]



7. In a job interview, you are provided with the below SystemVerilog(SV) code and asked that how you can formally verify this design [Hint: logic is a data type in SV similar to reg data type in Verilog]? [2]

```
module design1 (input clock, input reset,input cx, input cy,output x,
output y);
logic x; logic y;
always @(posedge clock)
if (reset) begin
x <= 1'b1;
y <= 1'b0;
end else begin
x <= !y && cx;
y <= !x && !cx && cy;
end
endmodule
```