

SIMPLE AS POSSIBLE (SAP-1)

TTL COMPUTER PLANS

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INTRODUCTION

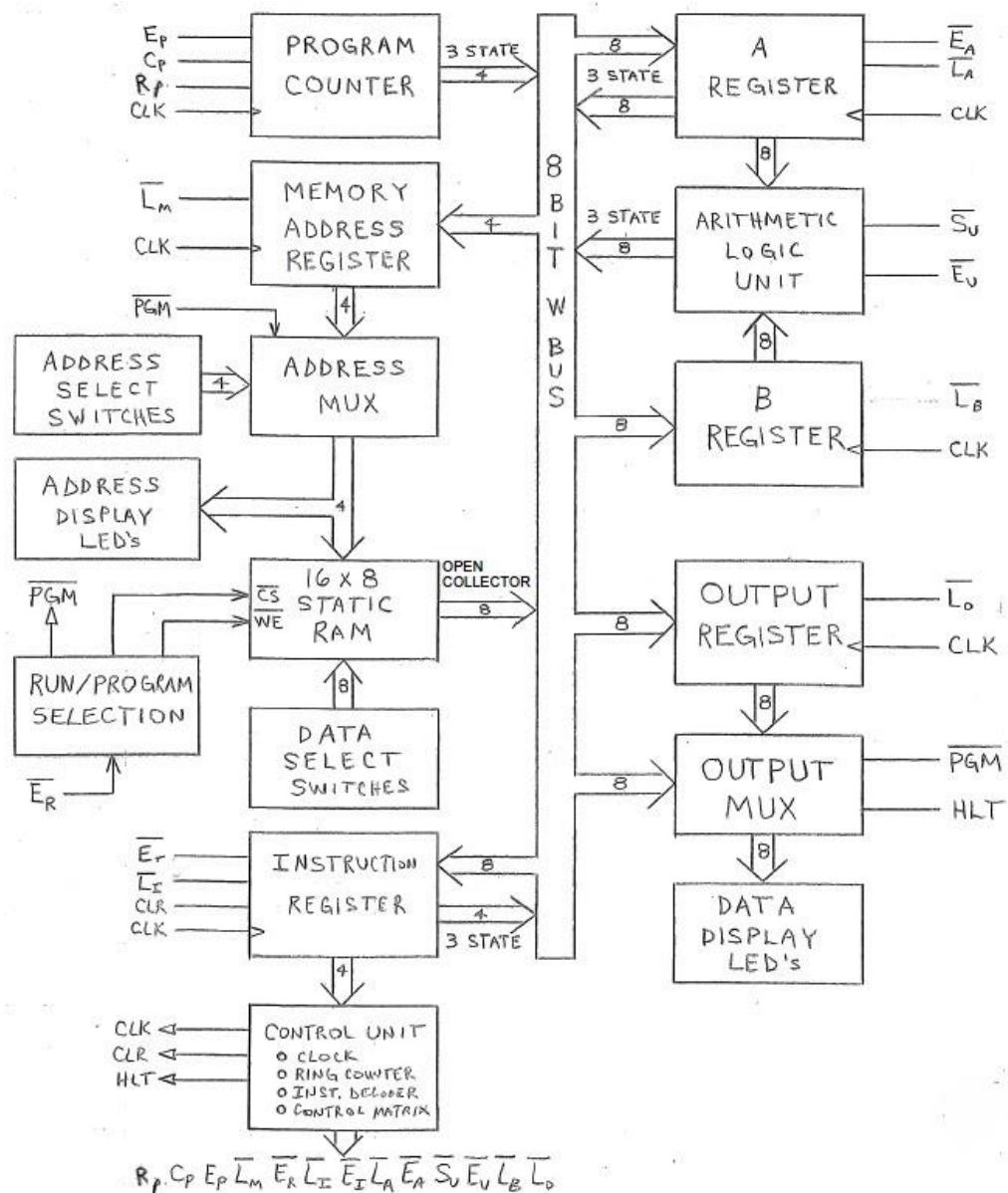
These plans can be used to build a working SAP-1 Computer, as described by Albert Paul Malvino in his book, [Digital Computer Electronics, An Introduction to Microcomputers, Second Edition 1982](#).

The SAP-1 Computer is mainly useful for academic purposes -- it can only perform addition and subtraction operations, but is nonetheless a great project to build.

ARCHITECTURE

The SAP-1 features a 4-bit address bus, five 8-bit registers and 16 bytes of RAM. Each instruction takes 6 cycles -- 3 fetch and 3 execute. The computer is bus-oriented, with outputs to the 8-bit W Bus three-state or open-collector, allowing for orderly data transfers.

The following is the SAP-1 architecture:



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The following is a description of the SAP-1 architecture:

- The Program Counter (PC) (74LS293) is part of the control unit that counts from 0000 to 1111. The PC provides the address of the next instruction to be fetched and executed. Programs are stored at the beginning of memory, with the first instruction at binary address 0000, the second instruction at 0001, the third at address 0010, etc.
- The Static RAM (2x 7489) stores instruction and data words (your program). The RAM is 16 bytes by 8 bits. During a computer run, the RAM receives the 4-bit address from the MAR and a read operation is performed. The instruction or data word stored in the RAM is placed on the W Bus for use as required.
- Address and Data Select Switches provide for sending 4 address bits and 8 data bits to the RAM. The Address MUX (74LS157) allows either the Address Select Switches or the MAR (described below) to be routed to the RAM.
- The Memory Address Register (MAR) (74LS173) holds the address of the Program Counter, which is later used as the 4-bit address to the RAM, where a read operation is performed.
- The Instruction Register (2x 74LS173) consists of two nibbles. The high order nibble holds the instruction that is sent to the instruction decoder. The low order nibble is the address of the data.
- The A Register (or Accumulator) (74LS377) is a buffer register that stores intermediate answers during a computer run.
- The B Register (74LS377) is a buffer register used in arithmetic operations during a computer run. It supplies the number to be added or subtracted from the contents of the A Register (Accumulator).
- The Arithmetic Logic Unit (ALU) (2x 74LS283 and 2x 74LS86) consists of a 2's complement Adder-Subtractor. The Adder-Subtractor is asynchronous (unclocked).
- The Output Register (74LS377) is the computer's output port. At the end of a computer run, the accumulator contains the answer to the problem being solved. The A Register (Accumulator) is transferred to the Output Register via the OUT instruction. The result is displayed on the Output LED's via the Display Select MUX after a HLT (Halt) instruction.
- The Binary Displays (Address Bus and W Bus/Output Port) are used to assist with programming and/or viewing RAM data, observing computer operation and displaying program results.
- The Control Unit includes the following four functions:
 1. Controlled Clock
U4A, a NAND Schmidt Trigger (74LS132) RC oscillator is used for the SAP-1 clock circuit, instead of the 555 timer circuit shown by Malvino. The frequency out of U4A is $0.8/(R * C)$, which using the components selected is $0.8/(2000 * 0.0001) \sim 4$ Hz. U2A, a 74LS74 D flip-flop divides the frequency by 2, resulting in a clock of about 2 Hz.

U1, a dual JK 74LS76A flip-flop provides the SAP-1 Start/Stop control. Using the asynchronous CLR and PRE inputs on U1A, fed by the SPDT momentary START pushbutton with pull-ups, the Q output is normally low. Pressing START sets Q high; when START is released, Q falls low, toggling U1B. When U1B's Q output is high, the U4A NAND Schmidt Trigger RC oscillator is enabled.

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The computer can be paused during a run by pressing the START pushbutton to toggle U1B's Q output low. Pressing START once again will resume operation.

The HLT instruction clears U1B, thus disabling the oscillator.

U3 is used to select either Manual-Mode Single-Step pulses or Auto-Mode clock pulses.

U40, a 74LS221 dual one-shot, provides a 50ms pulse for each press of the SINGLE-STEP pushbutton.

2. Ring Counter

The ring counter is a 6-bit circulating shift register, with a single high bit circulating at any time. Each ring word represents one T-state, with a total of six states. Instructions are fetched during the first three T-states and executed in the remaining three T-states.

The ring counter consists of six D flip-flops made with two IC's, one 74LS175 and one 74LS74. The counter is initialized to 000001 on power-up with R4 and C6 and after power-up via the CLR signal. The counter rotates the single high bit on each clock (CLK) pulse.

3. Instruction Decoder

The instruction decoder deciphers an opcode to produce one of six output signals: LDA, ADD, SUB, OUT, HLT or JMP.

4. Control Matrix

The control matrix generates 13 microinstructions that tell the computer what to do at the proper time in conjunction with the Ring Counter. The control signals are as follows:

R _P	Reset Program Counter (PC)
C _P	Increment Program Counter (PC)
E _P	Enable Program Counter (PC) to W Bus
<u>L_M</u>	Load Memory Address Register (MAR)
<u>E_R</u>	Enable RAM to W Bus
<u>L_I</u>	Load Instruction Register (IR)
<u>E_I</u>	Enable Instruction Register to W Bus
<u>L_A</u>	Load A Register
<u>E_A</u>	Enable A Register to W Bus
<u>S_U</u>	Subtract B Register from A Register (A = A + B')
<u>E_U</u>	Enable ALU to W Bus
<u>L_B</u>	Load B Register
<u>L_O</u>	Load Output Register

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INSTRUCTIONS

There are 6 instructions: LDA, ADD, SUB, JMP, OUT and HLT. The JMP instruction, not part of Malvino's design, was added to allow for continuous operation.

Instruction Opcodes are:

Mnemonic	Opcode	Description
LDA	0000	Load Accumulator (A)
ADD	0001	$A = A + B$
SUB	0010	$A = A - B$
JMP	0011	Jump to location 0000
OUT	1110	Copy Accumulator to Output Port
HLT	1111	Stop processing

Instructions are entered as a 4-bit Opcode (entered in D4-D7) and a 4-bit Operand (as direct address, entered in D0-D3).

DESIGN

The computer design requires 36 Low Power Schottky (LS TTL) family chips and 4 standard family TTL chips. Substitutions with newer family types, such as ALS should be possible, but have not been tested.

The physical design is based on using a 4.5 x 6.5 inch perf-board (0.1 inch centers) with DIP and DB25 wire-wrap sockets, 30AWG wire-wrap, and soldered bare copper wire for the power supply rails. The perf-board is installed in an enclosure on standoffs. Hard-wired connections to switches, pushbuttons and LED's are made using insulated copper wire to DB25 plugs. The board can be removed from the enclosure by disconnecting the two DB25 plugs.

A 120Vac to 9Vac 1A wall-mount transformer is used for the computer's power supply, which also includes a full-wave bridge rectifier and 7805C voltage regulator. This SAP-1 design requires about 0.53A at 5Vdc during operation.

Sources of supply for parts could be jameco.com and/or digikey.com.

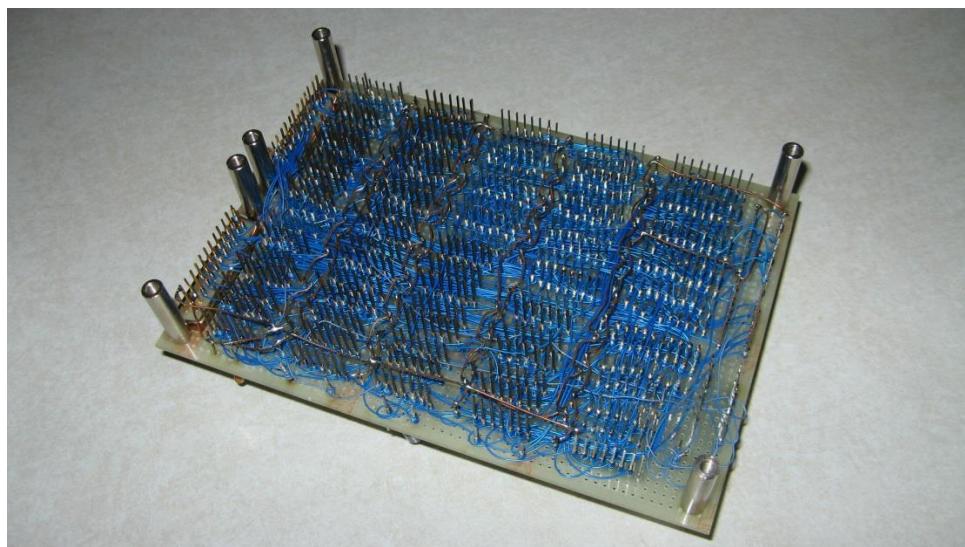
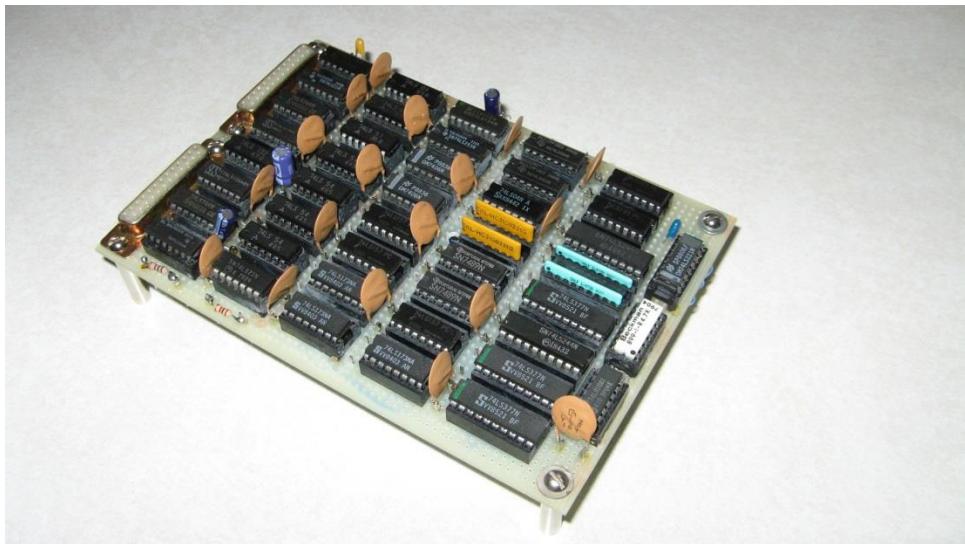
Changes from the design as presented by Mr. Malvino include:

- Control RAM enable signal \overline{CE} renamed to $\overline{E_R}$
- Ring counter outputs named T0 – T5 rather than T1 – T6
- IC's used for the Control Matrix, Ring Counter and Program Counter were changed
- Controlled clock circuit and oscillator were changed
- CLEAR, START, AUTO/MANUAL and STEP pushbuttons and switch circuits were changed
- Added a JMP instruction, with the addition of one more control signal R_p
- Added a Display Select MUX so the 8 bit LED's can display either the W Bus status or the Output Port status after a HLT (Halt) instruction.
- Added Address Bus LED's
- Modified power supply design
- 7489 with open-collector outputs used, instead of 74189 with tri-state outputs (either will work)

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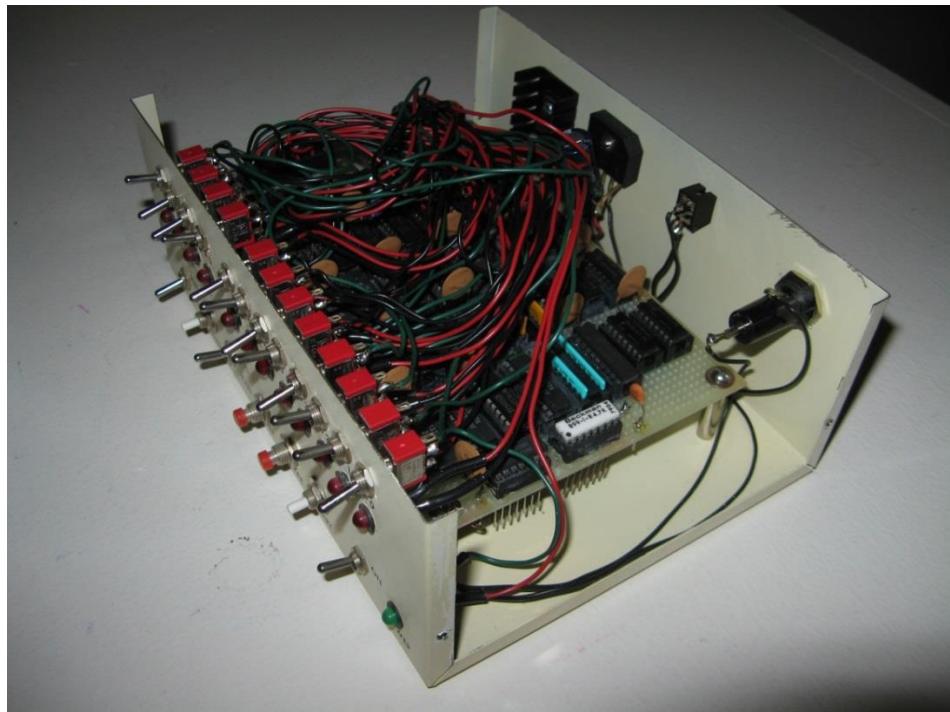
CONSTRUCTION PHOTOS

The following photos show the initial construction of the SAP-1 on perf-board. The use of DB25 wire-wrap sockets P1 and P2 allows for the board to be completely removed from the enclosure.



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The following photo shows the initial SAP-1 perf-board design mounted in the enclosure. The fuse holder, power supply connector, bridge rectifier and voltage regulator with heatsink are mounted on the back wall.



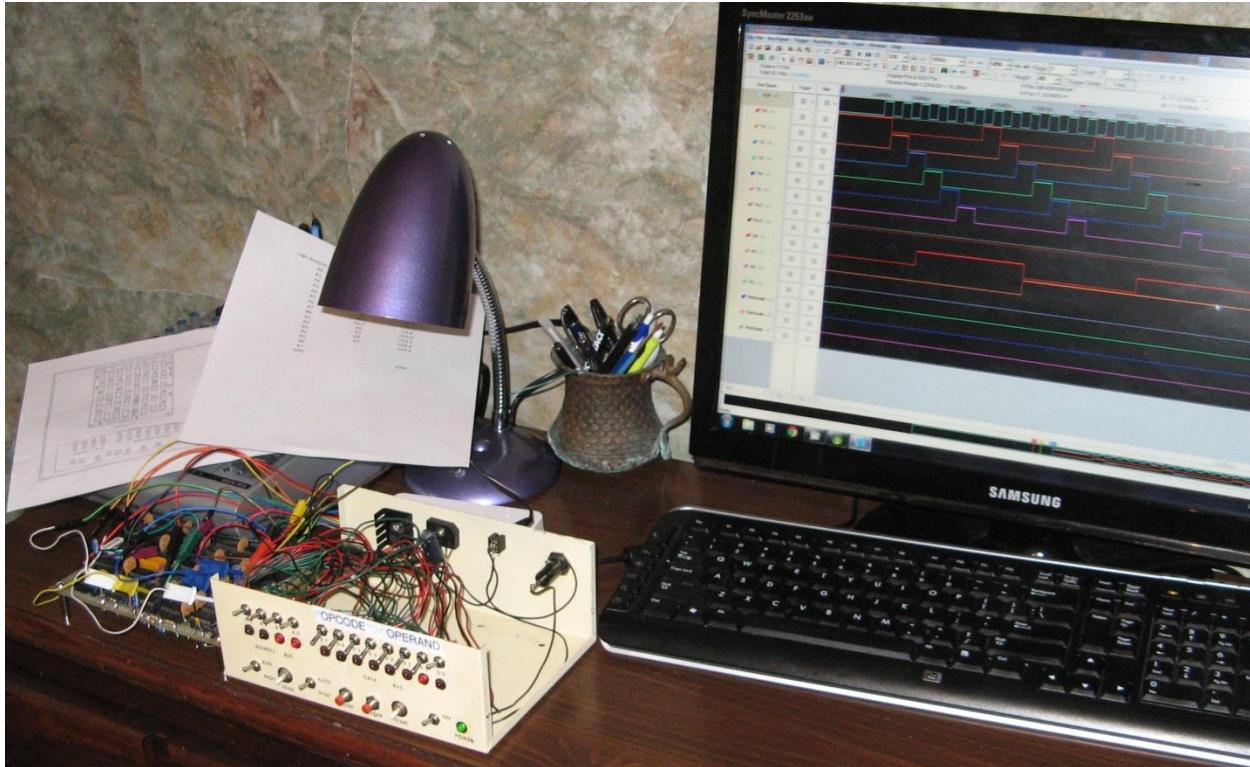
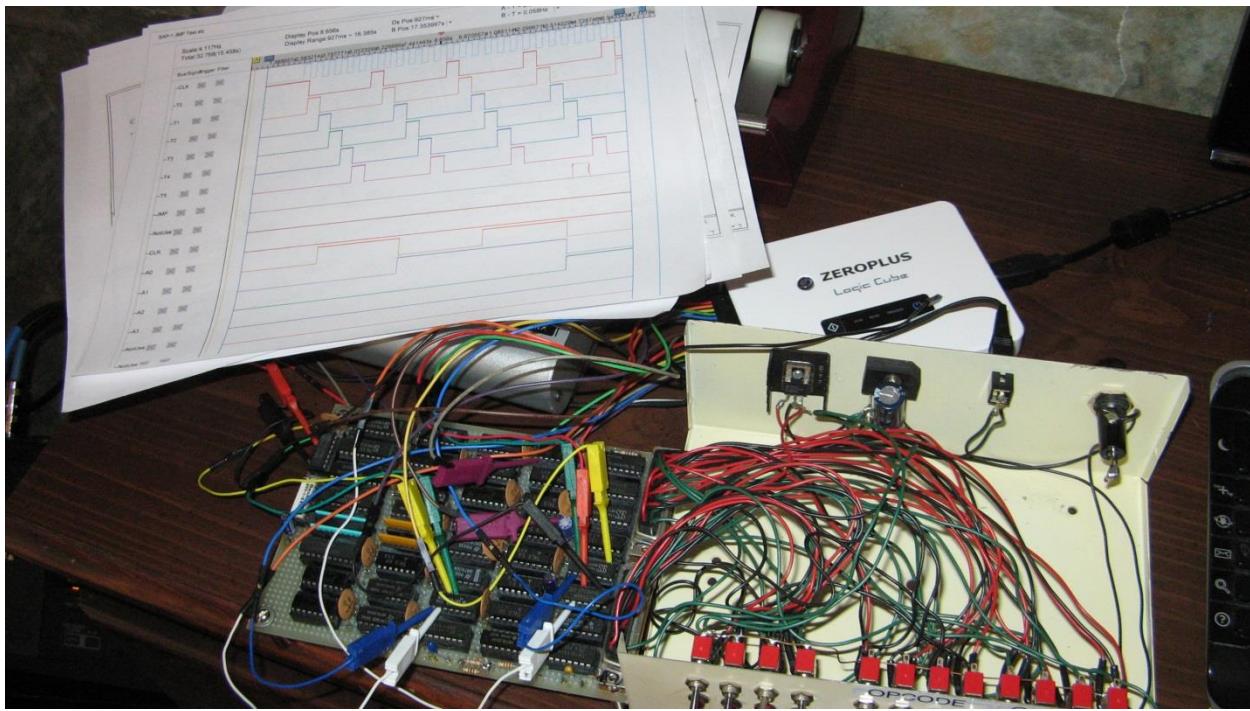
The following photo shows the front panel of the SAP-1 in operation:



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SAP-1 IN TEST

The following photos show the SAP-1 being tested with a Zeroplus USB Logic Analyzer.



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PROGRAMMING AND RUNNING THE SAP-1

Entering a Program

1. Set the RUN / PROG selector switch to PROG (program mode).
2. Select the desired memory location with the Address Bus switches A0 to A3.
3. If entering instructions, enter the Instruction Opcode using Data Bus switches D4 to D7. Then, enter the Instruction Operand using Data Bus switches D0 to D3 and press the LOAD pushbutton. If entering data constants, set the W (Data) Bus switches D0 to D7 as desired and press the LOAD pushbutton.

Running a Program

Programs can be run in AUTO or MANUAL (Single-Step) mode. The AUTO / MAN selector switch sets the desired mode. Assuming you want to run a program in Auto, proceed with the following:

1. Set the AUTO / MAN selector switch to AUTO (automatic mode).
2. Set the RUN / PROG selector switch to RUN (run mode).
3. Press the CLEAR pushbutton to reset the program counter to memory location zero. Note – on the first run after powering up the SAP-1, this step is not necessary.
4. Press the START pushbutton.

During a program run, the computer can be paused by pressing the START pushbutton. Press the START pushbutton again to resume operation.

To run a program in Single-Step mode, proceed as follows:

1. Set the AUTO / MAN selector switch to MAN (manual mode).
2. Set the RUN / PROG selector switch to RUN (run mode).
3. Press the CLEAR pushbutton to reset the program counter to memory location zero. Note – on the first run after powering up the SAP-1, this step is not necessary.
4. Press the STEP pushbutton to single-step through your program.

Demo Program

The following Demo can be used to verify operation. A link to my YouTube video showing this program in operation can be found on the following page.

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The program does this: $65 + 47 - 24 + 3 + 16 + 7 = 114$ (binary 01110010, hex 72). Two memory locations are not used. Data constants are entered in locations \$A to \$F.

ADDRESS	MNEMONIC	OPCODE	OPERAND
0000	LDA	0000	1010
0001	ADD	0001	1011
0010	SUB	0010	1100
0011	ADD	0001	1101
0100	ADD	0001	1110
0101	ADD	0001	1111
0110	OUT	1110	0000
0111	HLT	1111	0000
1010	DATA	0100	0001
1011	DATA	0010	1111
1100	DATA	0001	1000
1101	DATA	0000	0011
1110	DATA	0001	0000
1111	DATA	0000	0111

A YouTube video, [SAP-1 TTL Computer Demo -- Entering and Running a Program](#), is available for reference.

OPTIONAL ADDITION

Two 7-segment LED's can be added to the Output Register to enable continuous hexadecimal monitoring of the output while the binary display is cycling through instructions. This makes for an interesting addition for little cost.

This option uses two Fairchild DM9368 7-Segment Decoder/Driver integrated circuits and two LN514RK 0.4" Common Cathode 7-Segment LED's.

The two IC's are identified as U41 and U42, and the 7-Segment LED's are LED1 and LED2.

Connections are made to the Output Register U35 from the two 9368's as shown on the following page.

I used two 16-pin DIP wire-wrap sockets mounted on a small perf-board, which was then mounted in the enclosure.

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9368 Pin	Name	U42 (High Digit)	U41 (Low Digit)
1	A1	U35-15	U35-5
2	A2	U35-16	U35-6
3	LE	U35-10 (GND)	U35-10 (GND)
4	RBO	N/C	N/C
5	RBI	U35-20 (Vcc)	U35-20 (Vcc)
6	A3	U35-19	U35-9
7	A0	U35-12	U35-2
8	GND	U35-10 (GND), LED2-3, LED2-14	U35-10 (GND), LED1-3, LED1-14
9	e	LED2-7	LED1-7
10	d	LED2-8	LED1-8
11	c	LED2-10	LED1-10
12	b	LED2-13	LED1-13
13	a	LED2-1	LED1-1
14	g	LED2-11	LED1-11
15	f	LED2-2	LED1-2
16	Vcc	U35-20 (Vcc)	U35-20 (Vcc)

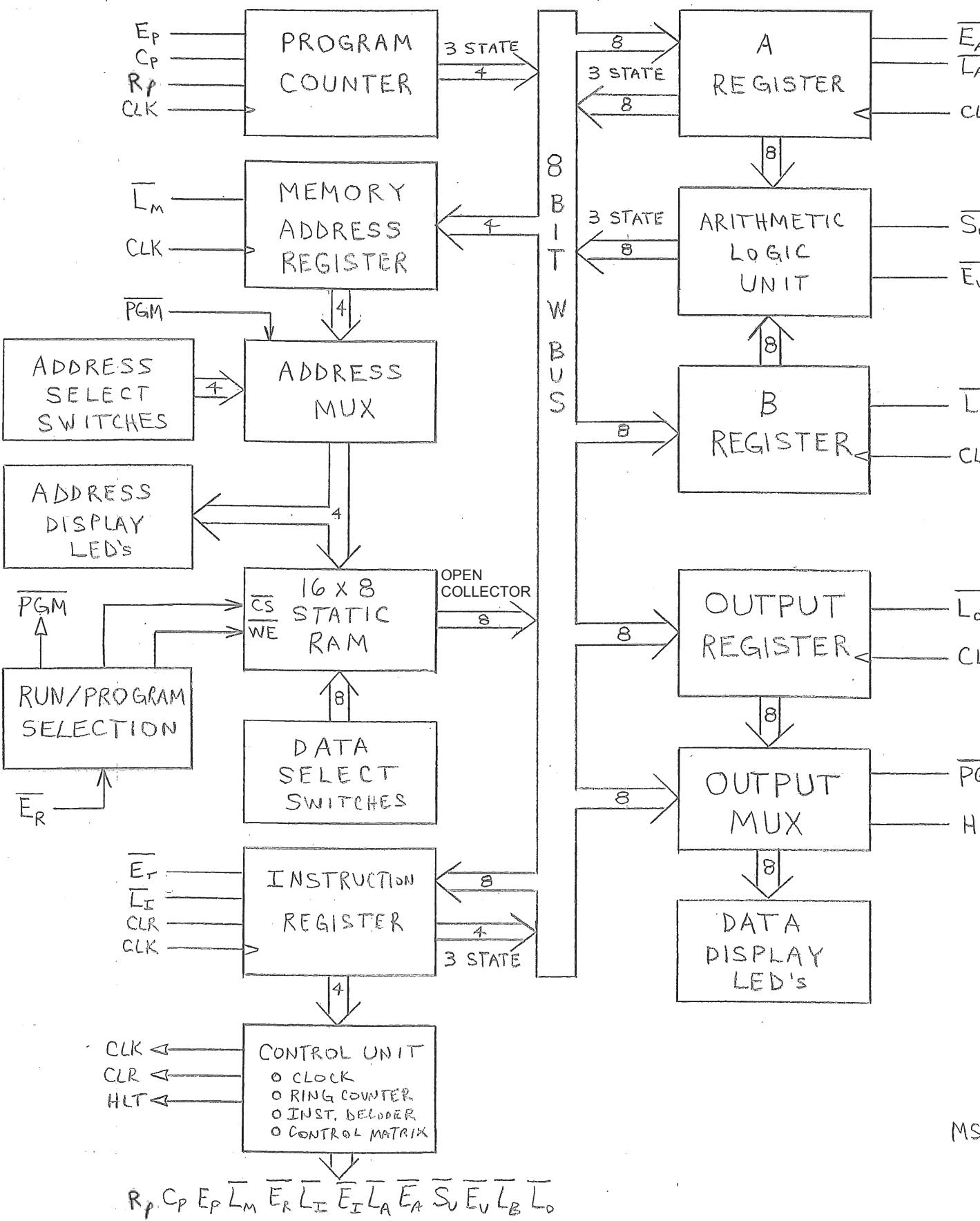
The following shows the SAP-1 displaying the result of the Demo program in binary and hexadecimal on the 7-Segment two-digit display.



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Attachment: Perf-board layout, BOM, schematics

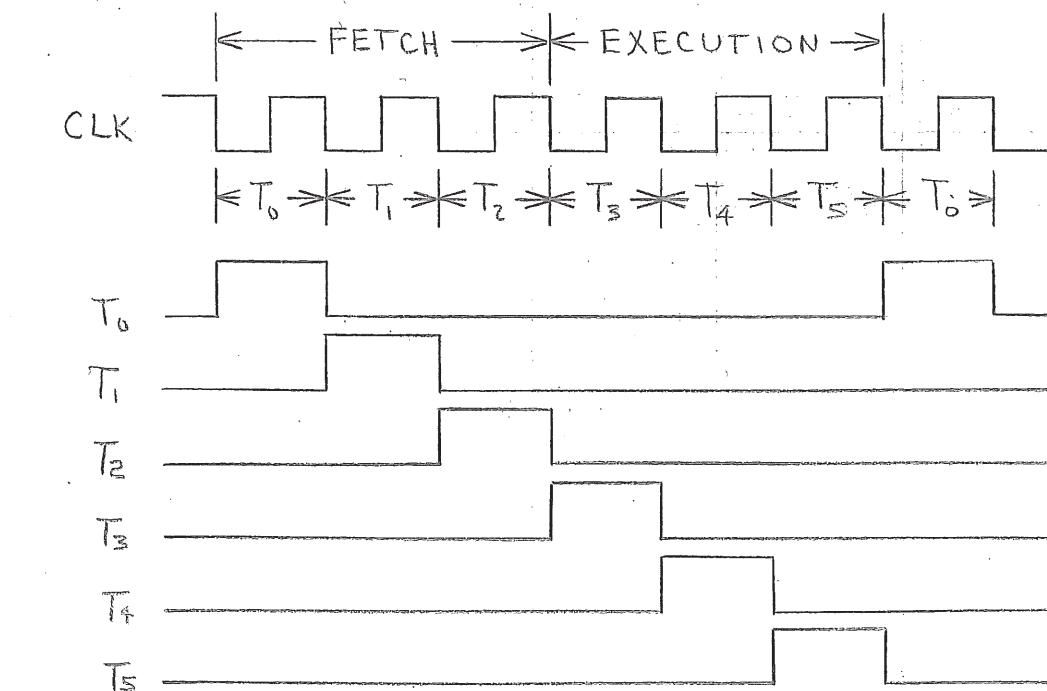
SAP-1 ARCHITECTURE



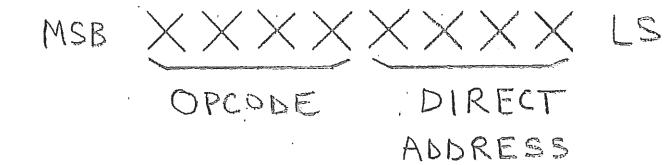
INSTRUCTION CYCLES

INSTRUCTION MNE-MONIC	OP-CODE	FETCH CYCLE		EXECUTION CYCLE		
		ADDRESS PHASE T_0	MEMORY PHASE T_1	INCREMENT PHASE T_2	EXECUTION PHASE 1 T_3	EXECUTION PHASE 2 T_4
LDA	0000	$MAR \leftarrow PC$ $E_p \ \overline{L}_m$	$IR \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_i$	$PC = PC + 1$ C_p	$MAR \leftarrow ADDR$ $\overline{E}_i \ \overline{L}_m$	$A \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_A$
ADD	0001	$MAR \leftarrow PC$ $E_p \ \overline{L}_m$	$IR \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_i$	$PC = PC + 1$ C_p	$MAR \leftarrow ADDR$ $\overline{E}_i \ \overline{L}_m$	$B \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_B$
SUB	0010	$MAR \leftarrow PC$ $E_p \ \overline{L}_m$	$IR \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_i$	$PC = PC + 1$ C_p	$MAR \leftarrow ADDR$ $\overline{E}_i \ \overline{L}_m$	$B \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_B$
OUT	1110	$MAR \leftarrow PC$ $E_p \ \overline{L}_m$	$IR \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_i$	$PC = PC + 1$ C_p	$OUT \leftarrow A$ $\overline{E}_A \ L_o$	DO NOTHING DO NOTHING
JMP	0011	$MAR \leftarrow PC$ $E_p \ \overline{L}_m$	$IR \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_i$	$PC = PC + 1$ C_p	$PC = 0000$ R_p	DO NOTHING DO NOTHING
HLT	1111	$MAR \leftarrow PC$ $E_p \ \overline{L}_m$	$IR \leftarrow (RAM)$ $\overline{E}_r \ \overline{L}_i$		CLEAR'S CLOCK CONTROL FLIP-FLOP WHICH HALTS THE COMPUTER	

CLOCK AND TIMING PULSES



INSTRUCTION FIELDS



BILL OF MATERIALS

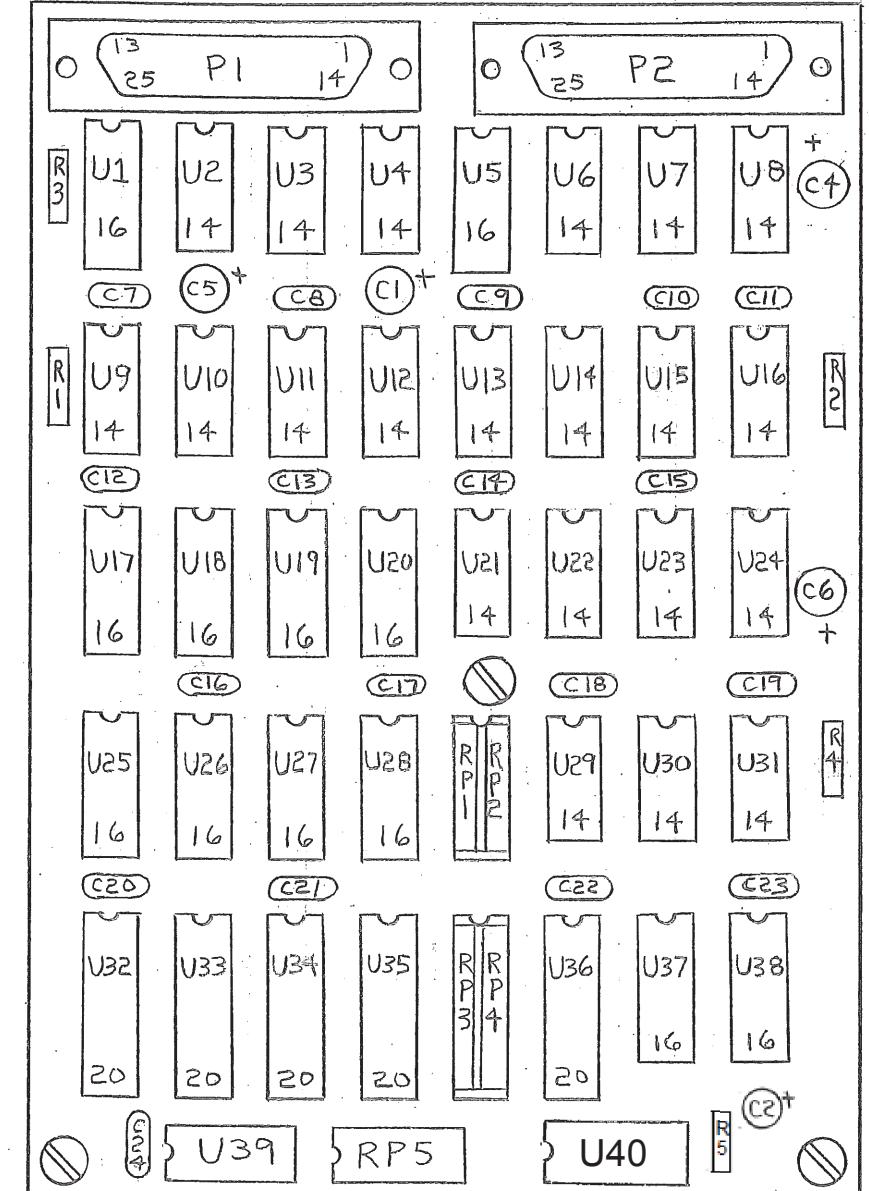
Designator	Description	Device	Pins
U1	Dual JK Flip Flop	74LS76	16
U2,6	Dual D Flip Flop	74LS74	14
U3	Quad Tri-State Buffer	74LS125	14
U4	Quad NAND Schmitt Trigger	74LS132	14
U5	Quad D Flip Flop	74LS175	16
U7,8,9	Dual 4-In AND Gate	74LS21	14
U10,11,12,13	4 Wide AND/OR/INV Gate	74LS54	14
U14	Dual 2 Wide AND/OR/INV Gate	74LS51	14
U15,39	Quad 2-In NAND Gate	74LS00	14
U16,29	Hex Inverter	74LS04	14
U17,18,25	Tri-State Quad D Register	74LS173	16
U19,20,26	Quad 2 to 1 MUX	74LS157	16
U21,22	Hex Inv. (open collector)	7406	14
U23	4 Bit Binary Counter	74LS293	14
U24	Quad Tri-State Buffer	74LS126	14
U27,28	64 Bit (16x4) Static RAM	7489	16
U30,31	Quad 2-In Exclusive OR Gate	74LS86	14
U32,33,35	Octal Flip Flop (Tri-State)	74LS377	20
U34,36	Octal Tri-State Buffer	74LS244	20
U37,38	4 Bit Binary Full Adder	74LS283	16
U40	Dual Monostable Multivibrator	74LS221	16
R1	2K 1/4W Carbon Resistor	Axial Mtg	
R2	1K 1/4W Carbon Resistor	Axial Mtg	
R3,R4	100 1/4W Carbon Resistor	Axial Mtg	
RP1,RP2	7 Resistor SIP (330 Ohm)	8	
RP3,RP4	9 Resistor SIP (4.7K)	10	
RP5	13 Resistor DIP (4.7K)	14	
R5	36K 1/4W Carbon Resistor	Axial Mtg	
C1	100 uF 16V Electrolytic Cap	Radial	
C2	2.2 uF 16V Tantalum Cap	Radial	
C3	470 uF 35V Electrolytic Cap (Mtd. on BR1)		
C4,C5,C6	1.0 uF 15V Tantalum Cap	Radial	
C7-C24	0.1 uF 12V Disc Cap	Radial	

BR1 Full-Wave Bridge Rectifier
 TR1 120/9 VAC 1A Wall-Mount Transformer
 VR1 7805C 5V 1.5A Voltage Regulator
 P1,P2 DB25 Female Wire Wrap Connectors

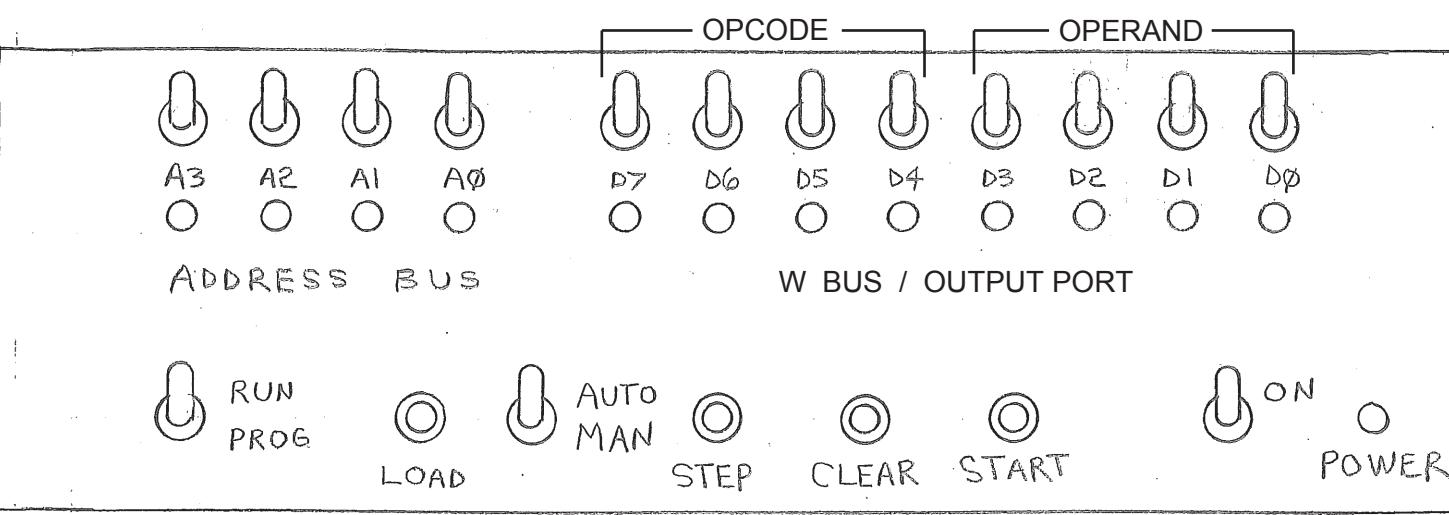
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Miscellaneous

Description	Quantity
Pushbutton, MOM, SPST, N.O.	2
Pushbutton, MOM, SPDT	1
Pushbutton, MOM, SPST, N.C.	1
Switch, Mini, SPST	15
14 Pin Wire Wrap Sockets	23
16 Pin Wire Wrap Sockets	13
20 Pin Wire Wrap Sockets	6
Red LED 1-3/4	12
Green LED 1-3/4	1
LED Mounting Sockets 4.5 x 6.5 Perfboard	13
Panel Mount Fuse Holder with 1A Fuse Enclosure (8.25 x 6 x 3 inches)	



LEGEND (1:1)

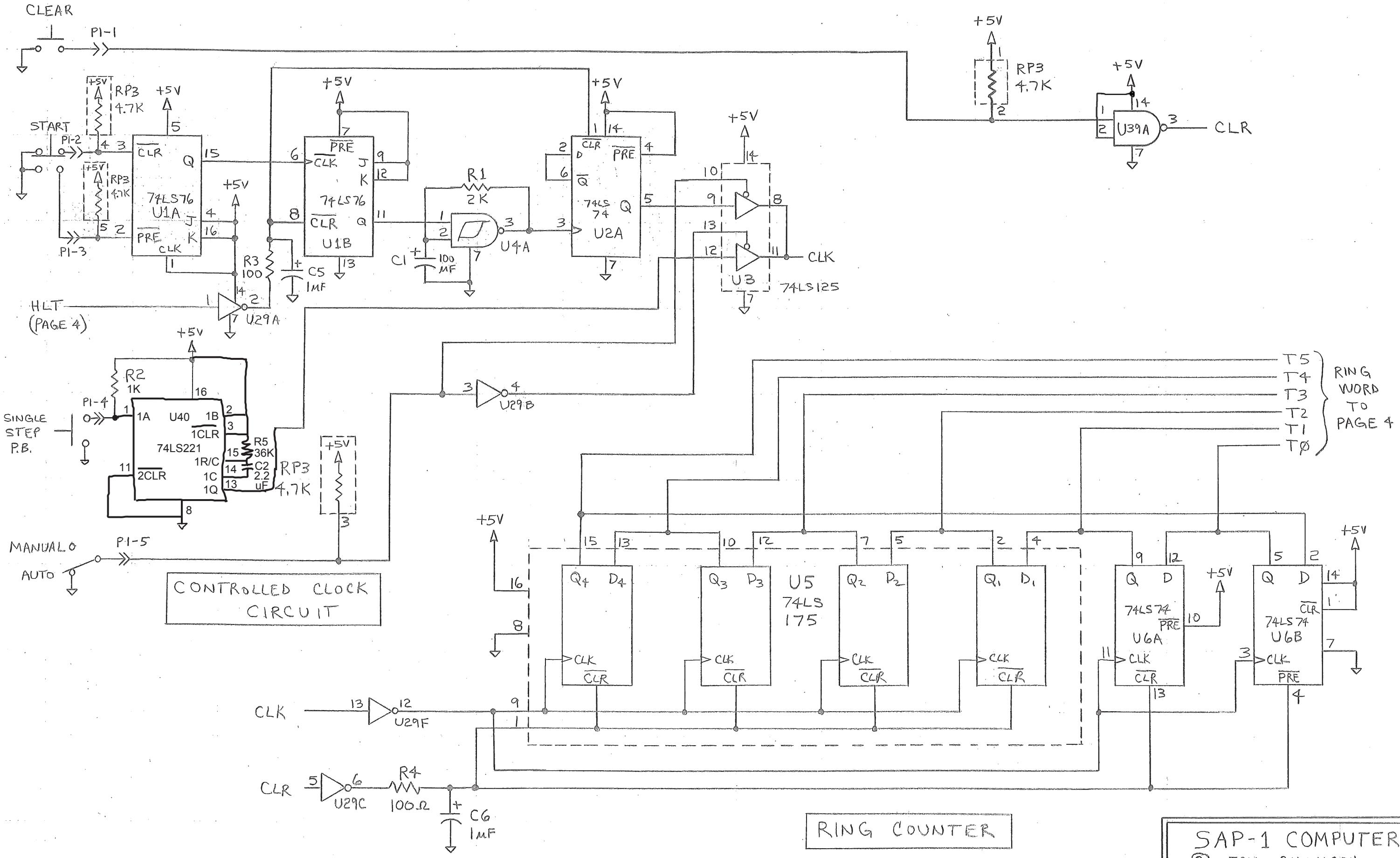


SAP-1 COMPUTER

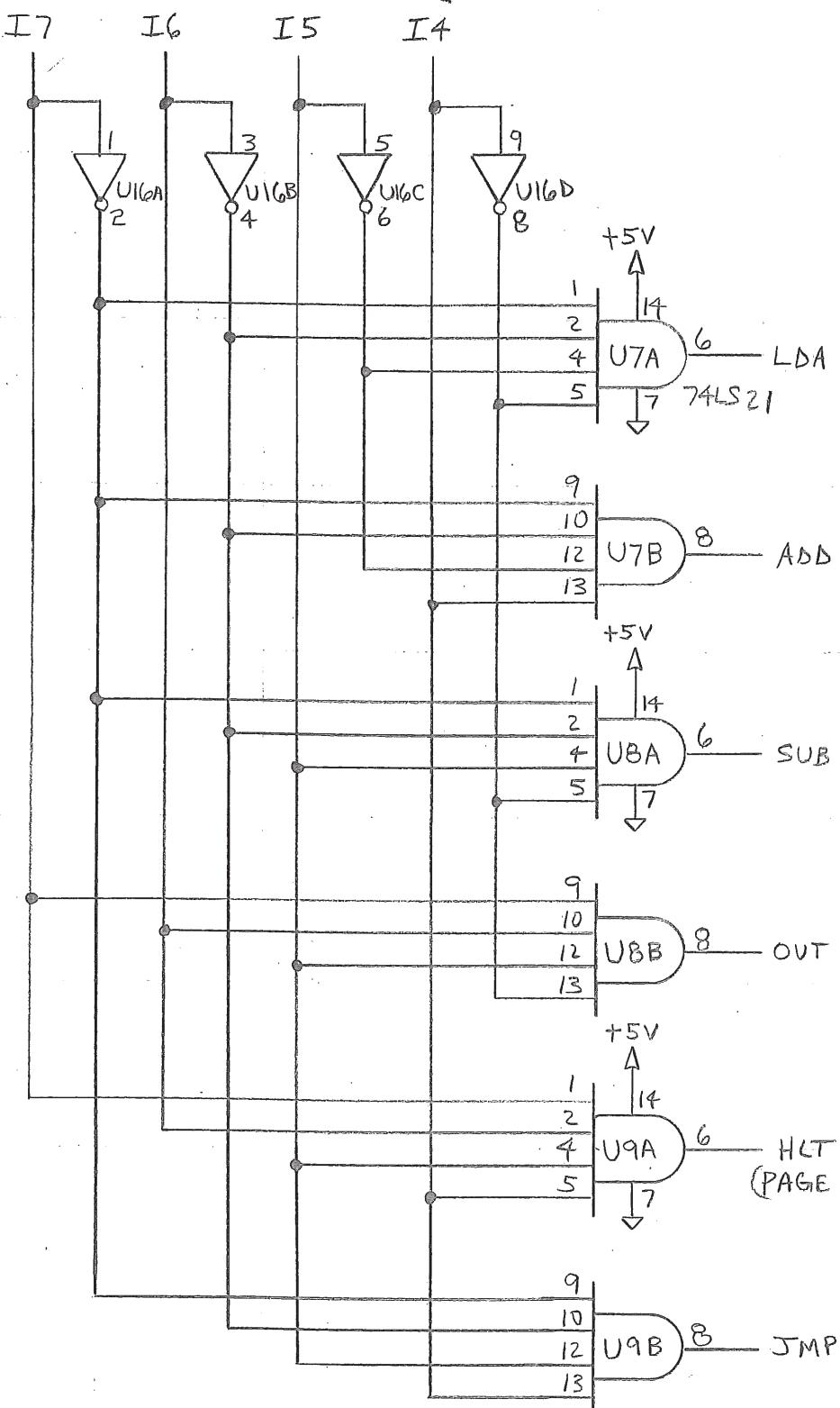
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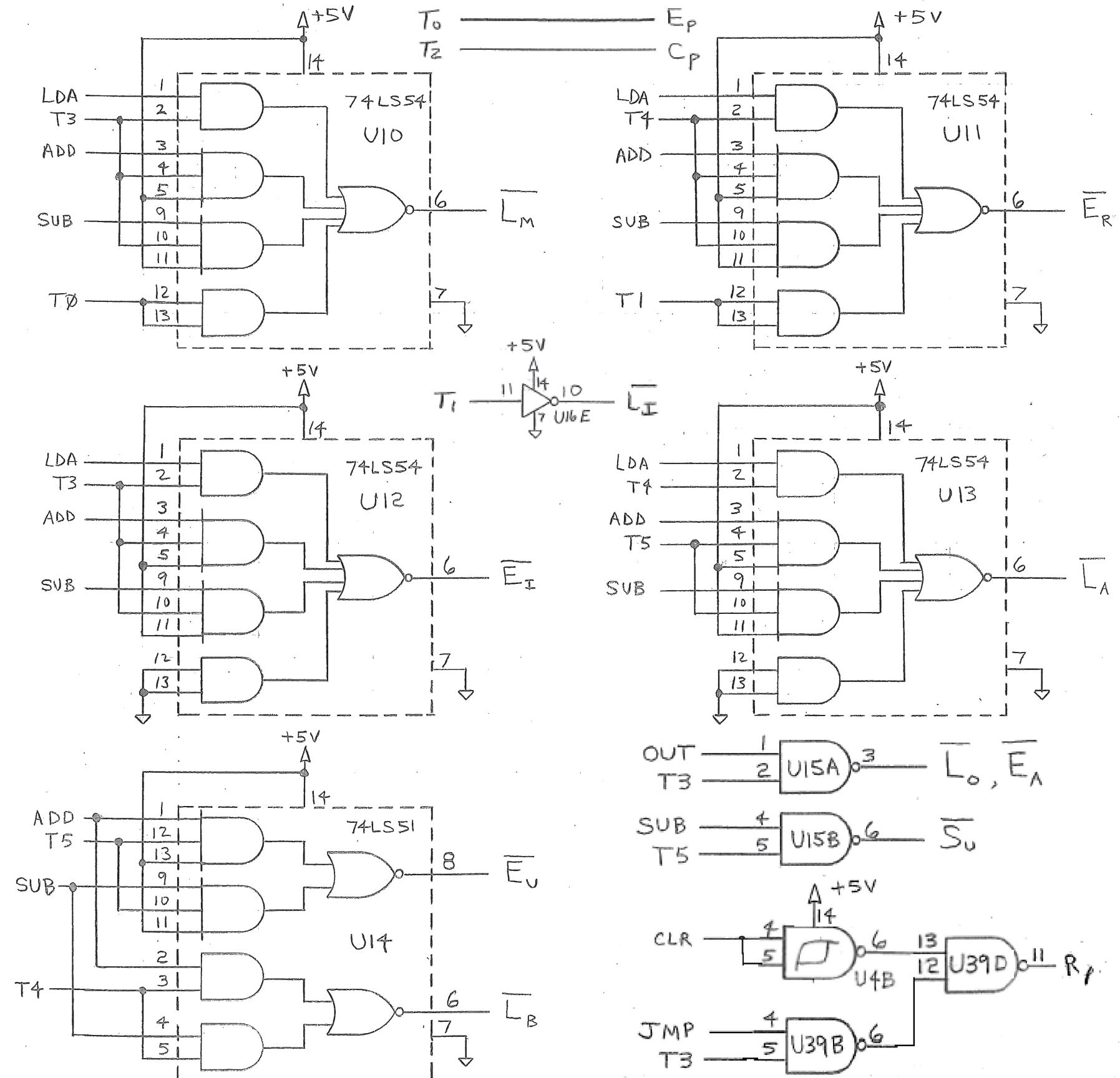
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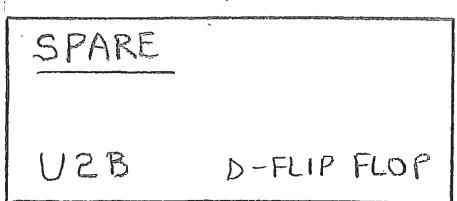
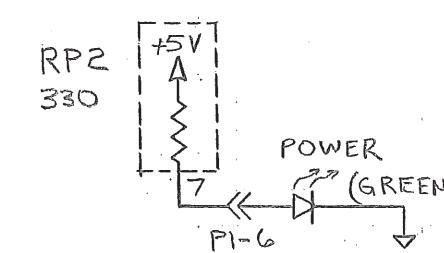
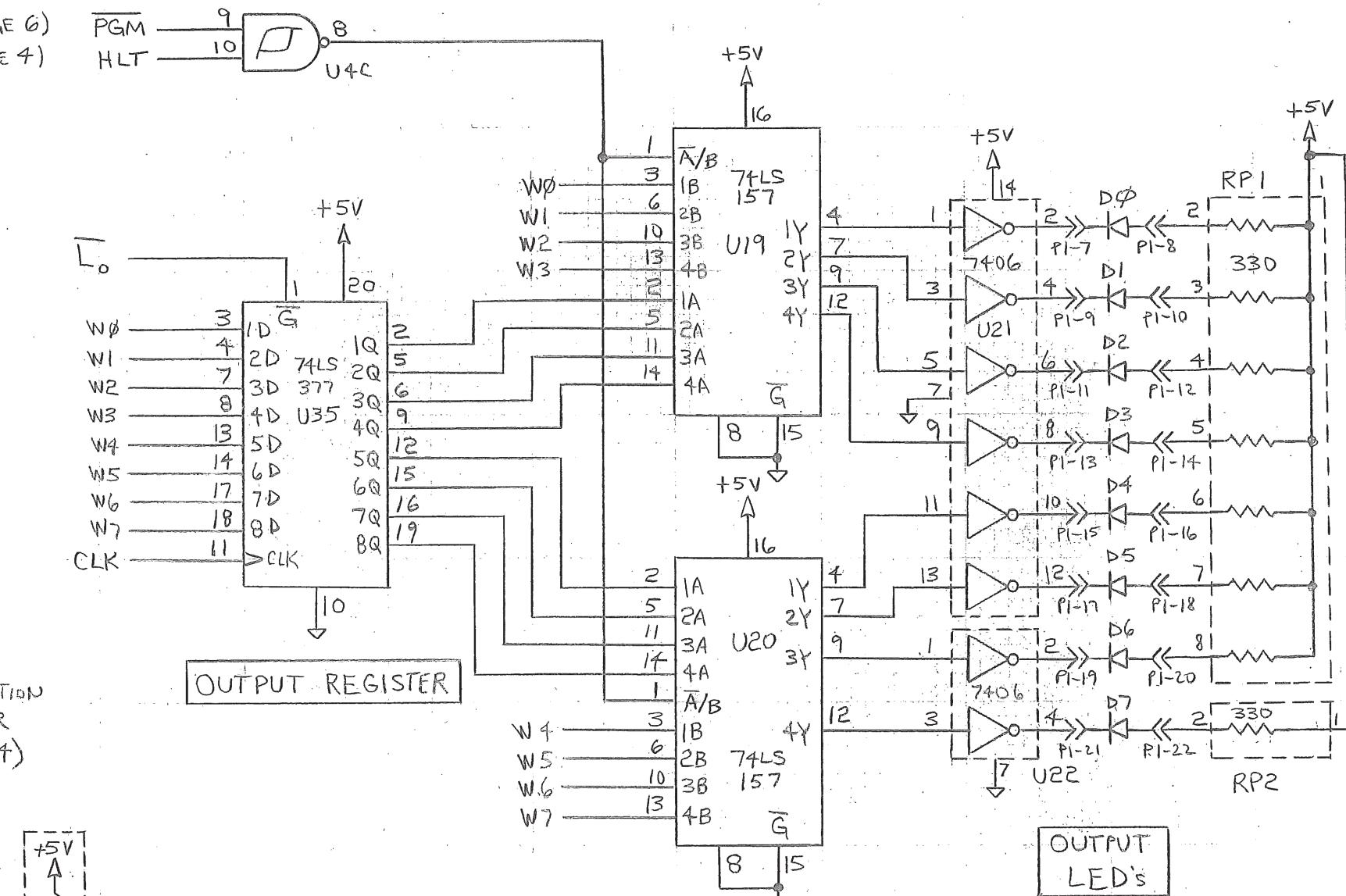
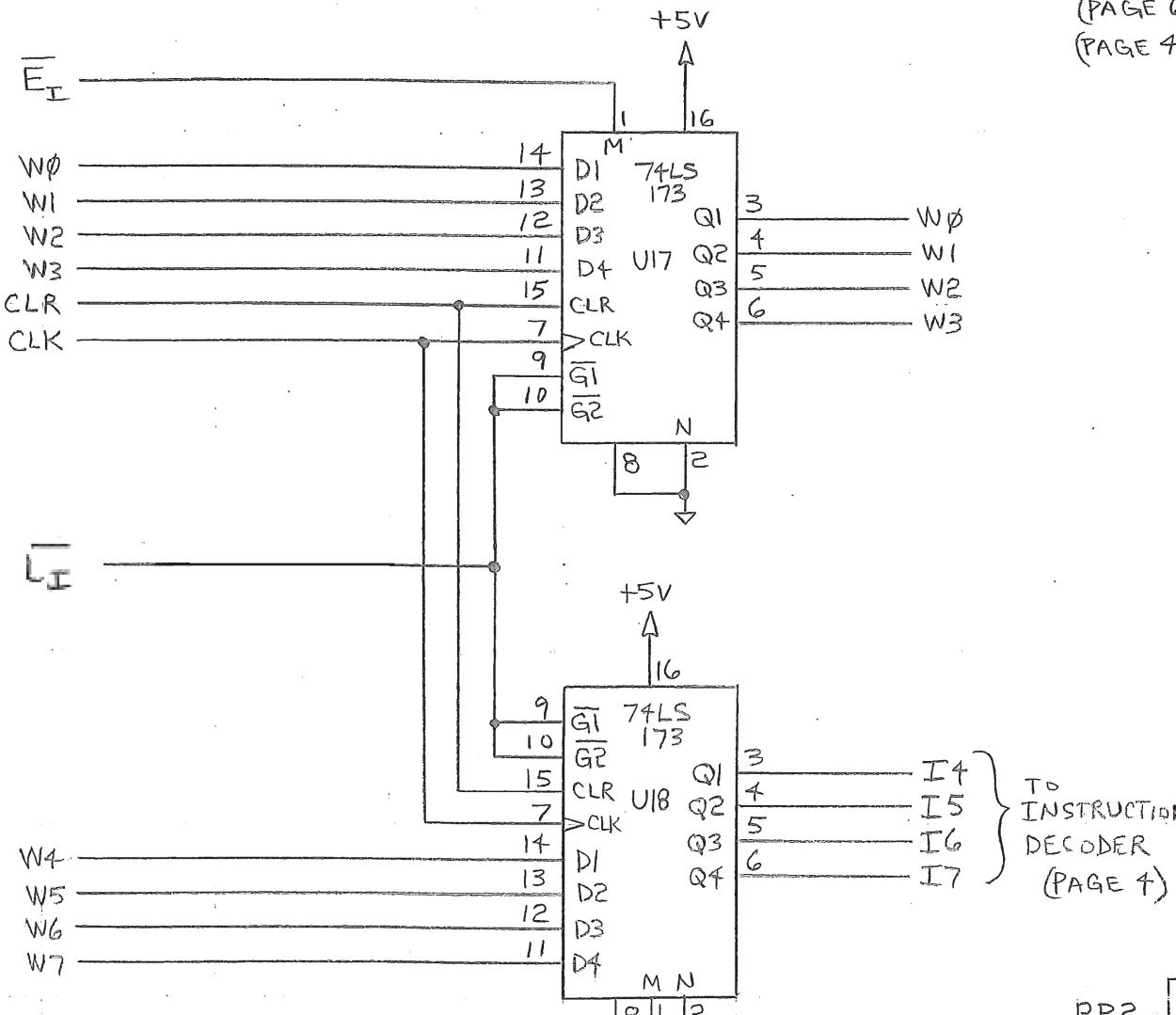


INSTRUCTION DECODER

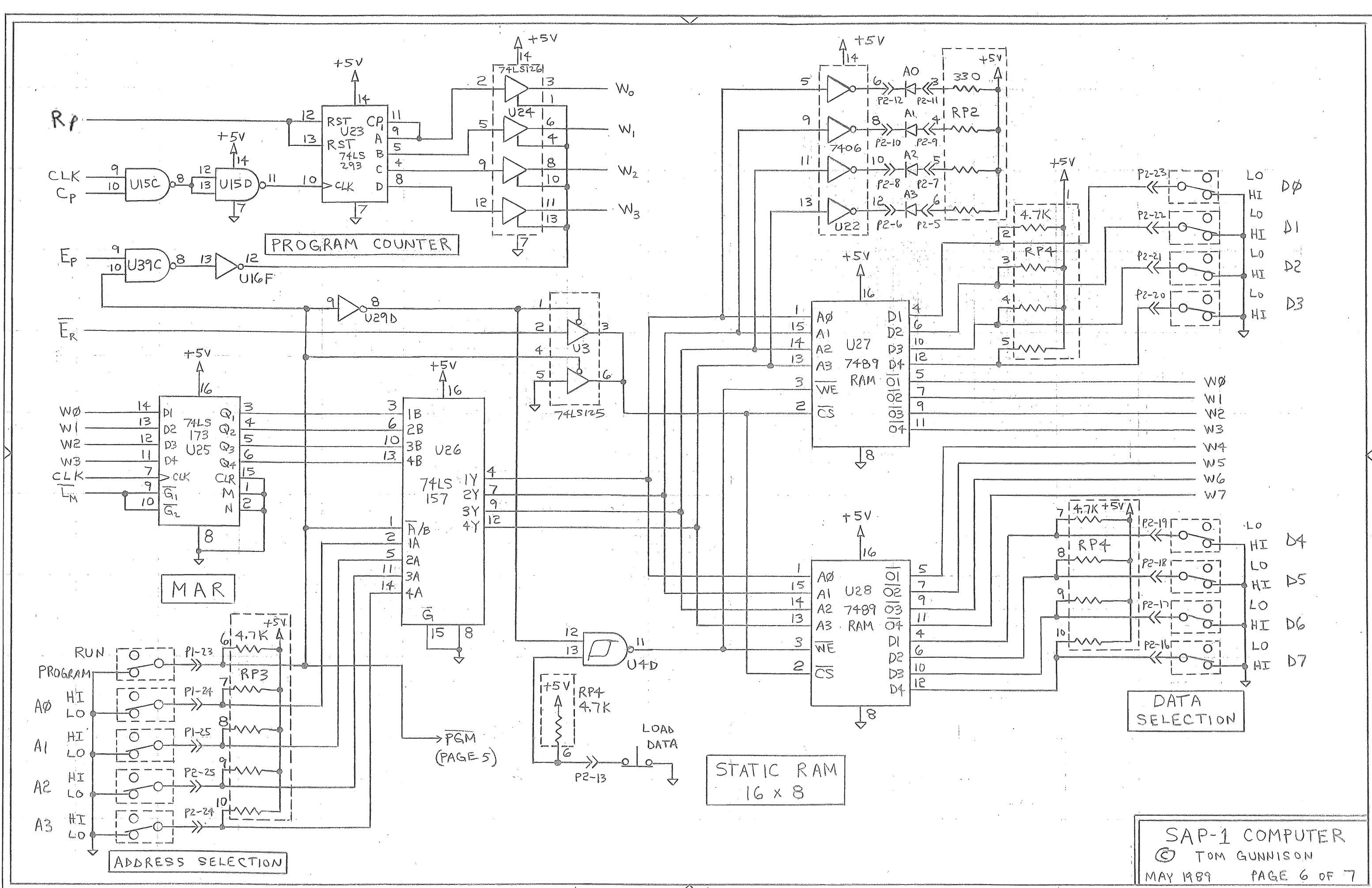


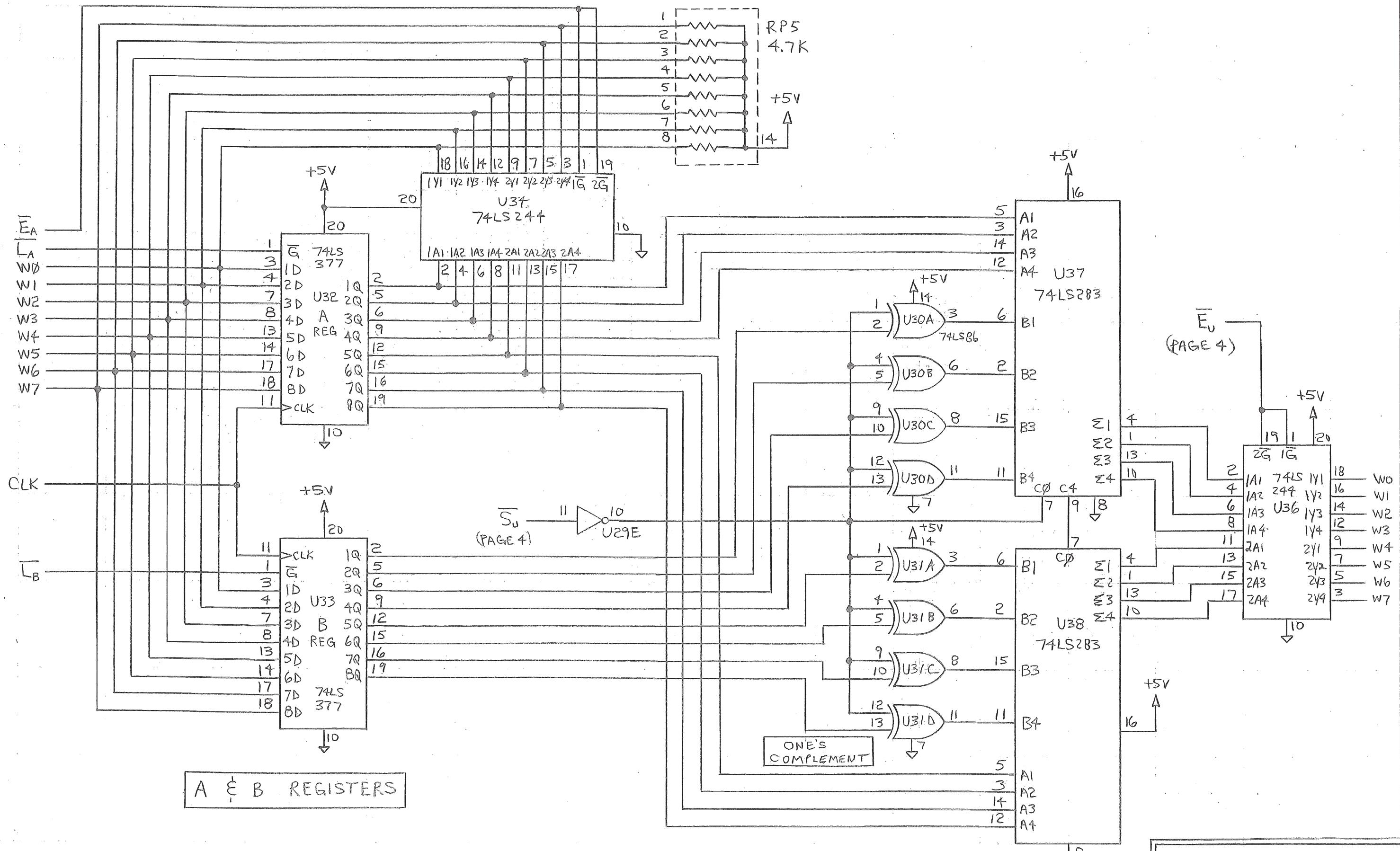
CONTROL MATRIX

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Note:
C7 to C24 are mounted across the various TTL chip power supply rails (not shown on the schematic pages).





A ∈ B REGISTERS

ARITHMETIC LOGIC UNIT

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