Instruction of implementing SROPEE

1. Put the S-parameter input file in the folder: .\SROPEE\Input
2. Open run_main.py program file in the folder: .\SROPEE
    - Write the full name of input file, including the file extension, in variable *Input_file_name*.
    - Set the desired number of poles for vector fitting algorithm as Num_poles.
    - Set number of iterations for vector fitting of column sum as VF_iter1.
    - Set number of iterations for vector fitting of function (f) as VF_iter2.
    - Set weighting type for vector fitting of function as weight_f.
    - Set weighting for vector fitting of column sum as weight_column_sum.
    - Enable/disable relaxed vector fitting by setting Boolean value in VF_relax.
    - Enable/disable enforcing stability of fitted poles by setting Boolean values in VF_stable.
    - Choose the fitting model options by setting VF_asymp equal to 0, 1, and 2.
    - Enable/disable passivity enforcement by setting Boolean values in Passivity_Enforcement_Enable.
    - Set an iteration upper limit for passivity enforcement as SMP_iter_upper_limit.
    - Set the desired order of reduction for Block SAPOR algorithm in variable n.
    - Write the port of input source as *in_port*.
3. Execute run_main.py program file.
4. After executing the main program file, the program continues and plots for each part of SROPEE.
    - If the plots of Full synthesis part are not matched well, you must increase the number of pairs of poles and restart the main program file.
    - If the plots of Full synthesis part are matched well, it means that this part is done perfectly, and you must check the results of Passive MOR part of SROPEE.
    - If the plots of Passive MOR part are not matched well, you must increase the order of reduction and restart the main program file.
    - If the plots of Passive MOR part are matched well, it means that this part is done perfectly, and you must validate the results of equivalent reduced-order circuit.
5. Congrats! SROPEE algorithm is done, and equivalent reduced circuit is created as “reduced_netlist.sp”.
6. To validate the equivalent reduced-order circuit[1]:
    - Open the Keysight ADS software.
    - Import the “reduced_netlist.sp”.

[1] This step is explained in the following section titled as “Instructions for simulating equivalent reduced-order netlist in ADS software, and exporting the reduced-order nodal voltages”.

- Add the simulation component and change the frequency characteristics.
- Simulate the equivalent reduced-order network.
- Export the reduced-order nodal voltages using Data File Tool.
- Name the exported data as “reduced_voltages_ADS.cti”.
- Copy the reduced_voltages_ADS.cti in the folder: .\SROPEE\Output.

7. Run the Reduced synthesis part of SROPEE again.
8. The Z-parameter results of equivalent reduced-order circuit will be saved in the folder: .\SROPEE\\Output\figure\Reduced_synthesis, and may be validated by comparing them with the graphs plotted in Passive MOR part.

Instructions for simulating equivalent reduced-order netlist in ADS software, and exporting the reduced-order nodal voltages

To validate the equivalent reduced-order circuit, please perform the following steps:

1. Open the Keysight ADS software
2. Choose new Workspace.
3. Write the name of Workspace, select the path to create in, and click on create workspace.
4. To import the equivalent netlist in the workspace:
    - Go to the File tab => Import => Design
    - Choose Netlist File from drop-down menu in File type
    - Browse and select your netlist file.
    - Click on the options:
        i. Choose HSPICE for Input Netlist Dialect
        ii. Mark the First line is a comment
        iii. Mark Suppress name mapping
        iv. Choose ADS Netlist for big networks
        v. Click on OK
    - Click on OK.
    - Write the library name, click on OK.
    - You will see a warning for the netlist subcircuit selection component, click on the OK.
    - In the new box, choose the equivalent_circuit with 0 pins, and click on the OK.
    - Click on OK for Information message box.
    - The equivalent reduced netlist will be imported as a component in a schematic.
5. To simulate the equivalent circuit, do not use the imported component directly. Open a new schematic using the new schematic icon below the File tab.
6. Choose a name and click on create schematic. A new empty schematic will be created.
7. Insert the component of equivalent circuit through the following steps:
    - Go to the Insert tab => Component => Component Library
    - Click on Workspace Libraries
    - Right click on the equivalent_circuit component
    - Click on Place component
    - Click on an empty space in schematic
    - Noe, the equivalent circuit is added to the schematic
8. Add a simulation component. For this project:
    - Choose the Simulation-AC from drop-down menu on the left side of schematic.
    - Choose AC, click on an empty space in schematic

- Double-click on the AC, set the frequency characteristics, click on OK

9. Click on the Simulate icon.
10. You will see a warning, click on Run Anyway.
11. A new window will appear if everything goes well.
12. Close the display window.
13. Export the data using Data File Tool through:
    - Click on the Tools tab in schematic => Data File Utilities => Data File Tool
    - Choose the “write data file from data set”
    - Write reduced_voltages_ADS in the input file name box
    - Choose Real/Imag in the drop-down menu of Complex data format
    - Choose the “Citifile” for the output format.
    - Click on your dataset
    - Click on Write to File
    - Click on Yes for warning message
    - A new file “reduced_voltages_ADS.cti” will be created in the data folder in directory of your workspace
14. Copy the reduced_voltages_ADS.cti from data folder of your workspace to the output folder in SROPEE.