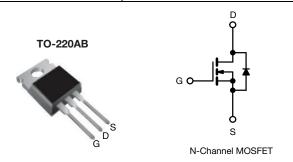
Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	200				
$R_{DS(on)}(\Omega)$	V _{GS} = 5.0 V 0.18				
Q _g max. (nC)	66				
Q _{gs} (nC)	9.0				
Q _{gd} (nC)	38				
Configuration	Single				



FEATURES

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- · Logic-level gate drive
- R_{DS(on)} specified at V_{GS} = 4 V and 5 V
- Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION			
Package	TO-220AB		
Load (Dh) froe	IRL640PbF		
Lead (Pb)-free	SiHL640-E3		
SnPb	IRL640		
SIPD	SiHL640		

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V_{DS}	200	V		
Gate-Source Voltage		V _{GS}	± 10	v	
Continuous Duais Current	V_{GS} at 5.0 V $\frac{T_C = 25^{\circ}}{T_C = 100}$	C ,	17		
Continuous Drain Current	V_{GS} at 5.0 V $T_{C} = 100$	°C I _D	11	Α	
Pulsed Drain Current ^a	I _{DM}	68			
Linear Derating Factor		1.0	W/°C		
Single Pulse Avalanche Energy b			580	mJ	
Repetitive Avalanche Current ^a			10	A	
Repetitive Avalanche Energy ^a	E _{AR}	13	mJ		
Maximum Power Dissipation $T_C = 25 ^{\circ}C$		P _D	125	W	
Peak Diode Recovery dV/dt ^c	dV/dt	5.0	V/ns		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C		
Soldering Recommendations (Peak temperature) ^d		300			
Mounting Torque	6-32 or M3 screw		10	lbf ⋅ in	
Mounting Torque	0-32 of M3 screw		1.1	N · m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD}=50$ V, starting $T_J=25$ °C, L=3.0 mH, $R_q=25$ Ω $I_{AS}=17$ A (see fig. 12). c. $I_{SD}\leq17$ A, $dI/dt\leq150$ A/ms, $V_{DD}\leq V_{DS}$, $T_J\leq150$ °C.

- d. 1.6 mm from case.



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	62		
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.50	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.0		

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		-			Į.	ļ.	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		200	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I _D = 1 mA	-	0.27	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		-	2.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 10		-	-	± 100	nA
Zava Cata Valtaga Dvais Coverant		V _{DS} = 200 V, V _{GS} = 0 V		-	-	25	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 160 V, V	/ _{GS} = 0 V, T _J = 125 °C	-	-	250	μA
Dunin Course On Chata Basistana	Б	V _{GS} = 5.0 V	I _D = 10 A ^b	-	-	0.18	Ω
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 4.0 V	I _D = 8.5 A ^b	-	-	0.27	
Forward Transconductance	9 _{fs}		0 V, I _D = 10 A b	16	-	_	S
Dynamic							
Input Capacitance	C _{iss}	V	$V_{GS} = 0 V$,		1800	-	
Output Capacitance	C _{oss}	V	_{DS} = 25 V	-	400	-	рF
Reverse Transfer Capacitance	C _{rss}	f = 1.0	MHz, see fig. 5	-	120	-	
Total Gate Charge	Qg		S = 5.0 V		-	66	nC
Gate-Source Charge	Q _{gs}	V _{GS} = 5.0 V			-	9.0	
Gate-Drain Charge	Q _{gd}	1	See lig. o and 15	-	-	38	1
Turn-On Delay Time	t _{d(on)}		'		8.0	-	- ns
Rise Time	t _r	V_{DD} = 100 V, I_{D} = 17 A R_{g} = 4.6 Ω, R_{D} = 5.7 Ω, see fig. 10 b		-	83	-	
Turn-Off Delay Time	t _{d(off)}			-	44	-	
Fall Time	t _f			-	52	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from		-	4.5	-	
Internal Source Inductance	L _S	package and ce die contact	package and center of die contact		7.5	-	- nH
Gate Input Resistance	Rg	f = 1 MHz, open drain		0.3	-	1.2	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbo	MOSFET symbol showing the		-	17	A
Pulsed Diode Forward Current ^a	I _{SM}	integral reverse p - n junction diode		-	-	68	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 17 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = 17 \text{ A}, dI/dt = 100 \text{ A/}\mu\text{s}^{\text{b}}$		-	310	470	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.2	4.8	μC
Forward Turn-On Time	t _{on}	Intrinsic turn	-on time is negligible (turn	on is do	minated b	v Ls and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

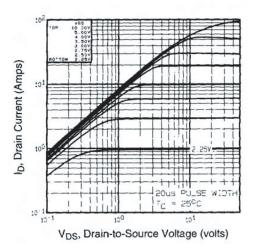


Fig. 1 - Typical Output Characteristics, T_C = 25 $^{\circ}C$

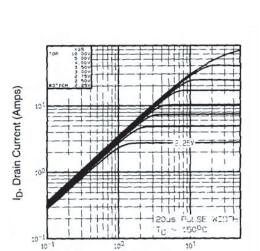


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

V_{DS}, Drain-to-Source Voltage (volts)

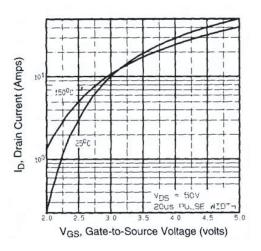


Fig. 3 - Typical Transfer Characteristics

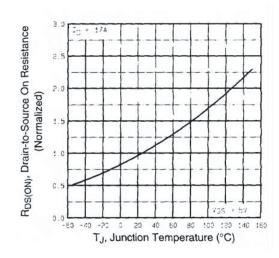


Fig. 4 - Normalized On-Resistance vs. Temperature



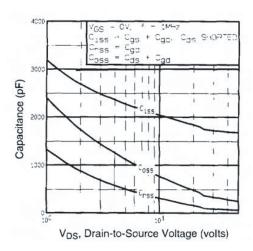


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

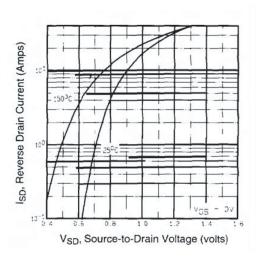


Fig. 7 - Typical Source-Drain Diode Forward Voltage

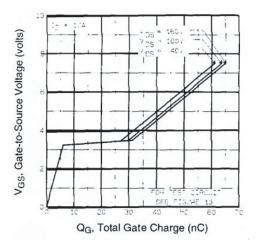


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

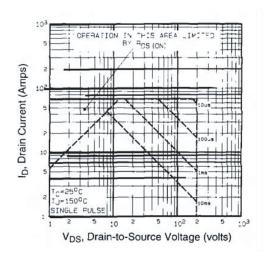


Fig. 8 - Maximum Safe Operating Area



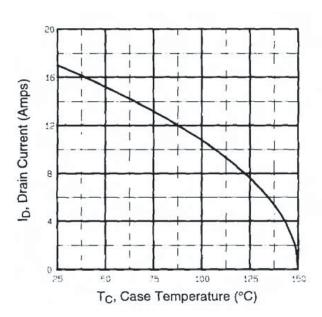


Fig. 9 - Maximum Drain Current vs. Case Temperature

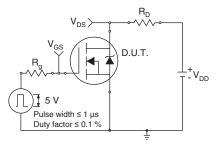


Fig. 10a - Switching Time Test Circuit

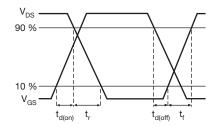


Fig. 10b - Switching Time Waveforms

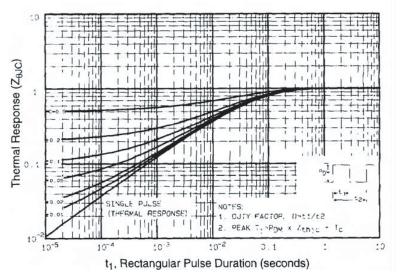


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

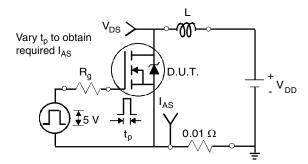


Fig. 12a - Unclamped Inductive Test Circuit

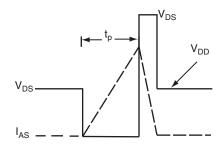


Fig. 12b - Unclamped Inductive Waveforms



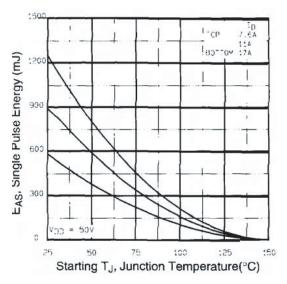


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

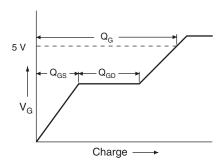


Fig. 13a - Basic Gate Charge Waveform

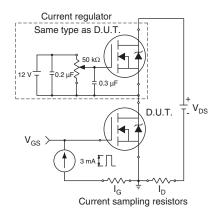
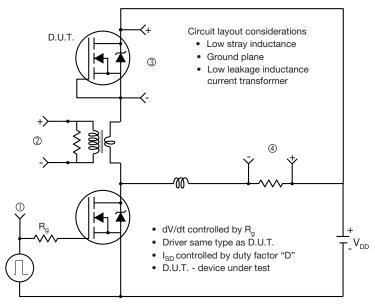


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



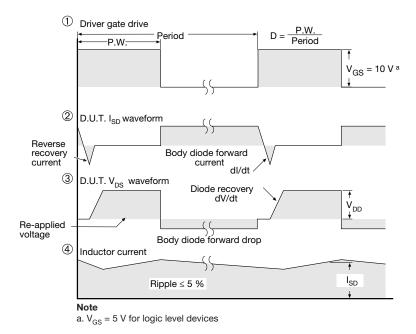


Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91305.





TO-220-1



DIM.	MILLIM	IETERS	INCHES		
DIIVI.	MIN.	MAX.	MIN.	MAX.	
Α	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
Е	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

 M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



Revison: 14-Dec-15 1 Document Number: 66542



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