

# Implementation of a Heterogeneous LDPC Decoder on ARM and GPU of Mobile Devices

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**Abstract**—Low density parity check (LDPC) codes have been extensively applied in mobile communication systems due to their excellent error correcting capabilities. However, their wide adoption has been hindered by the high complexity of the LDPC decoder. Although to date, dedicated hardware has been used to implement low latency LDPC decoders, recent advancements in the architecture of mobile processors has made it possible to develop software solutions. Here, unlike prior solutions that are based on either graphic processing units (GPUs) or advanced RISC machine (ARM) architectures, we propose a heterogeneous LDPC decoder that uses both the ARM and GPU processors of a mobile device to achieve efficient real-time decoding. The proposed solution is implemented on an NVIDIA development kit, where our results indicate that we can reduce the load on either the GPU or the ARM processor through the proposed heterogeneous structure, which in turn allows these resources to support other applications, simultaneously.

## I. INTRODUCTION

Originally proposed by Robert Gallager in 1962 [1] and rediscovered by MacKay and Neal in 1996 [2] Low Density Parity Check (LDPC) codes have been adopted by a wide range of applications including many communication standards such as IEEE 802.11n, 10 Gigabit Ethernet (IEEE 802.3an), Long Term Evolution (LTE) and DVB-S2. Recently, Chung and Richardson [3] showed that a class of LDPC codes can approach the Shannon limit to within 0.0045 dB. However, the error correcting strength of these codes comes at the cost of very high decoding complexity [4]. Moreover, to date, there are no closed-form solutions to determine the performance of LDPC codes in various wireless channels and systems. Thus, performance evaluation is typically carried out via simulations on computers or dedicated hardwares [5].

Since LDPC decoders are computationally-intensive and need powerful computer architectures to result in low latency and high throughput, to date, most LDPC decoders are implemented using application-specific integrated circuits (ASIC) or field-programmable gate array (FPGA) circuits [6]. However, their high speed often comes at a price of high development cost, low programming flexibility [7] and it is very challenging to design decoder hardware that supports various standards and multiple data rates [8]. On the other hand, iterative LDPC decoding schemes based on the sum-product algorithm (SPA) can fully be parallelized, leading to high-speed decoding [3]. For these reasons, designers have recently focused on

software implementations of LDPC decoders on multi/many-core devices [9] to meet the performance requirements of current communication systems through software defined radio (SDR). As in terms of multi-core architectures, researchers have used CPUs [10], [11], GPUs [5], [9], [12] and advanced RISC machine (ARM) [11], [13] architectures to develop high throughput, low latency SDRs.

In microarchitectures, increasing clock frequencies to obtain faster processing performance has reached the limits of silicon based architectures. Hence, to achieve gains in processing performance, other techniques based on parallel processing is being investigated [4]. Today's multi-core architectures support single instruction multiple data (SIMD), single program multiple data (SPMD) and single instruction multiple threads (SMT). The general purpose multi-core processors replicate a single core in a homogeneous way, typically with a x86 instruction set, and provide shared memory hardware mechanisms [9]. Such multi-core structures can be programmed at a high level by using different software technologies [14] such as OpenMP [15] which provides an effective and relatively straightforward approach for programming general-purpose multi-cores. On the other hand newer microarchitectures are trying to provide larger SIMD units for vector processing like streaming SIMD extensions (SSE), advanced vector extensions (AVX) and AVX2 [16] on Intel Architectures. In [4], the authors have used Intel SSE/AVX2 SIMD units to efficiently implement a high throughput LDPC decoder. Although the power consumption of x86 implementations are incompatible with most of the embedded systems which makes them useful for simulation purposes.

Mainly due to the demands for visualization technology in the gaming industry, the performance of graphics processing units (GPUs) has significantly improved over the last decade. With many cores driven by a considerable memory bandwidth, recent GPUs are targeted for solving computationally intensive algorithms in a multithreaded and highly parallel fashion. Hence, researchers in the high-performance computing field are applying GPUs to general-purpose applications (GPGPU). Pertaining to the field of communication, researchers have used Compute Unified Device Architecture (CUDA) from NVIDIA [5], [8], [12], [17], [18] and Open Computing Language (OpenCL) [19] platforms to develop LDPC decoders

on GPUs. The authors in [17] have achieved almost 1Gbps of through put on GPU devices. Although these works can achieve extremely high through puts, their latency that goes beyond second, their high power consumption and their cost, make them incompatible with embedded devices. The devices of the end users are usually mobile with limited access to a reliable power source. As such these devices must operate on limited resources - small processors, tiny memory and low power. In other words, the limited available resources must be used in the most effective and efficient fashion.

To solve this issue, ARM-based SDR systems have been proposed in recent years [11], [13] with the goal of developing an SDR based LDPC decoder that provides high throughput and low latency on a low-power embedded system. The authors in [13] have used ARM processor's SIMD and SIMT programming models to implement an LDPC decoder. This approach allows reaching high throughput while maintaining low-latency. However, the proposed ARM based solution in [13], is based on the assumption that the ARM processor is solely used for LDPC decoding but mobile devices need to support multiple applications simultaneously, and the processing resources cannot be extensively dedicated to the LDPC decoder. Moreover, recent works in SDR LDPC embedded systems are missing the fact that today's mobile devices have powerful CUDA enabled GPUs which can play a significant role as a computing resource in an embedded system. This paper considers limited resources of a mobile device and proposes an algorithm to reach high throughput and low latency decoding on an embedded device.

The contributions of this paper are threefold. First, it proposes an LDPC decoder for an embedded device which exploits GPU of the device. This allows the ARM processor to also support other applications on a mobile device. Second, as a consequence of this, by using the GPU of a mobile device, less memory from the ARM processor is being used which is typically limited in an embedded system. Third, the structure of the proposed decoder is based on multiple GPU streams which first makes it scalable to other architectures, and second the process imposed by decoding can be controlled by choosing correct number of data streams sent to the GPU device. On the other hand, since the ARM and GPU of an embedded device are sitting on a same die, latency issues of GPU implementations has been improved.

The remainder of the paper is structured as follows. Section II briefly introduces the LDPC code family and its decoding algorithms. Then the proposed heterogeneous algorithm on embedded targets is described in Section III. Finally, IV gives experimental results and some comparisons with other ARM implementations.

## II. LDPC CODES AND THEIR DECODING PROCESSES

LDPC codes are a class of linear block codes with a very sparse parity check matrix called H-matrix. Their main advantage is that they provide a performance which is very close to the channel capacity for a lot of different channels.

Furthermore, they are suited for implementations that make heavy use of parallelism [20].

Here, we present a very brief background on LDPC codes<sup>1</sup>. There are two ways to represent LDPC codes. Like all linear block codes they can be described by their H-matrix, while they can be represented by a Tanner graph which is a bipartite graph. An LDPC graph consists of a set of variable nodes (VNs), a set of check nodes (CNs), and a set of edges E. Each edge connects a variable node to a check node. For example, when the  $(i, j)$  element of an H-matrix is '1', the  $i$ th check node is connected to the  $j$ th variable node of the equivalent Tanner graph. Fig.1 illustrates the equivalent Tanner graph for a 10 VNs and 5 CNs, (10, 5), LDPC code with H-matrix in (1) [20].

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \quad (1)$$

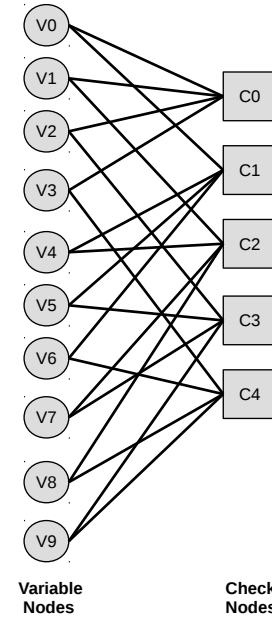


Fig. 1. An example of Tanner graph

The general decoding algorithm of LDPC codes is based on the standard two-phase message passing (TPMP) described in [9]. This algorithm works in two phases. In the first phase, all the variable nodes send messages to their neighboring parity check nodes, and in the second phase the parity check nodes send messages to their neighboring variable nodes. Due to transcendental operations and relying of message passing

<sup>1</sup>reader is referred to [20] for more information.

algorithm to the estimation of noise standard deviation, in practice Min-Sum (MS) variants are preferred by designers [13]. This algorithm is provided in Algorithm 1.

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**Algorithm 1** Min-Sum algorithm

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1: Loop 1: Initialization
2: for all  $m \in C, n \in V$  do
3:    $Lq_{nm} = 0$ 
4: end for
5: for all  $t = 1 \rightarrow (iter\_max)$  do
6:   Loop 2: LLR of message  $CN_m$  to  $VN_n$ 
7:   for all  $m \in C, n \in V$  do
8:      $\alpha_{nm} \triangleq \text{sign}(Lq_{nm})$ ,
9:      $\beta_{nm} \triangleq |Lq_{nm}|$ ,
10:     $Lr_{mn} = \prod_{n' \in N(m) \setminus n} \alpha_{n'm} \min_{n' \in N(m) \setminus n} \beta_{n'm}$ .
11:   end for
12:   Loop 3: LLR of message  $VN_n$  to  $CN_m$ 
13:   for all  $m \in C, n \in V$  do
14:      $Lq_{nm} = LP_n + \sum_{m' \in M(n) \setminus m} Lr_{m'n}$ .
15:   end for
16: end for
17: Loop 4: Hard decision from soft-values
18: for all  $n \in V$  do
19:    $LQ_n = LP_n + \sum_{m' \in M(n)} Lr_{m'n}$ ,
20:    $\forall n, \hat{c} = [LQ_n] > 0$ .
21: end for

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One major drawback of algorithm 1 is that, loops 2 and 3 are updated by separate processing and passed to each other iteratively. It means that variable nodes' update loop, will not start until all check nodes are updated. This characteristic affects the efficiency of parallel implementation of such algorithm.

Due to poor parallel mapping of MS algorithm, more efficient schedules, such as horizontal layered-based decoding algorithm, are proposed which allow updated information to be utilized more quickly in the algorithm, thus, speeding up the decoding [18], [21]. In fact, the H-matrix can be viewed as a layered graph that is decoded sequentially. The work in [17] has applied a form of layered belief propagation to irregular LDPC codes to reach 2x faster convergence in a given error rate. By using this method they have reduced memory bits usage by 45-50%. The layered decoding (Algorithm 2), which is used in the proposed algorithm, can be summarized as follow: all values for the check node computations are computed using variable node messages linked to them. Once, a check node is calculated, the corresponding variable nodes are updated immediately after receiving messages. This process is repeated to the maximum number of iterations.

This paper implements layered decoding of ldpc codes on the GPU device of a mobile processor with high throughput and low latency performance. By using GPU device as the processing unit, much less process of ARM processor is used for decoding compared to similar work in [13], thus there will be processing power for other applications of a mobile

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**Algorithm 2** Horizontal Layered Min-Sum algorithm

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1: Loop 1: Initialization
2: for all  $m \in C, n \in N(m)$  do
3:    $Lr_{mn}^{(0)} = 0$ 
4: end for
5: for all  $t = 1 \rightarrow (iter\_max)$  do
6:   Loop 2: For each check node
7:   for all  $m \in C$  do
8:     for all  $n \in N(m)$  do
9:        $Lr_{nm}^{(t)} = E_n - Lr_{nm}^{(t-1)}$ 
10:    end for
11:    for all  $n \in N(m)$  do
12:       $\alpha_{nm} \triangleq \text{sign}(Lr_{nm}^{(t)})$ ,
13:       $\beta_{nm} \triangleq |Lr_{nm}^{(t)}|$ ,
14:       $Lr_{mn}^{(t)} = \prod_{n' \in N(m) \setminus n} \alpha_{n'm} \min_{n' \in N(m) \setminus n} \beta_{n'm}$ .
15:    end for
16:    for all  $n \in N(m)$  do
17:       $E_n = Lr_{nm}^{(t)} + Lr_{mn}^{(t)}$ 
18:    end for
19:  end for
20:  Loop 3: Hard decision
21:  for all  $n \in V$  do
22:     $\forall n, \hat{c} = [E_n] > 0$ 
23:  end for
24: end for

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device. On the other hand, since the GPU and ARM of a mobile device are sitting on a same die, the latency issues in [17] are improved.

### III. ALGORITHM MAPPING

An efficient implementation of the layered decoding algorithm is a challenging task. The drawbacks of this algorithm as in terms of programming are: (i) the number of computations with respect to the number of memory access is low; (ii) the data reuse between consecutive computations is low; (iii) it requires a large set of irregular memory access due to the sparse H-matrix structure [4]. Considering these, a software-based decoder should take advantage of different parallelism levels offered by the target architecture to achieve high throughput efficiency. In this section, we detailed the different parallelism levels, target architecture along with the structure of proposed algorithm.

#### A. Parallelism levels in the proposed algorithm

To achieve high throughput performance, a software LDPC decoder has to exploit computation parallelism for taking advantage of multi-core architectures. Different parallelism levels are present in a layered decoding algorithm.

- First parallelism level is located inside the check node computations (Algorithm 2, loops located at line 8, 11 and 16). It is possible to execute such computations in parallel, however this atomic parallelism level is hard to exploit due to the low complexity of computations.

- Second parallelism level is located at check node level (Algorithm 2, line 7). Two check node computations can be done in parallel if there is no data dependency. Thus this level is hard to exploit and inefficient.
- Third parallelism level is located at frame level (Complete Algorithm 2 execution). A same computation sequence is executed over consecutive frames. This approach provides an efficient parallel processing algorithm.

So we have used single instruction multiple data (SIMD) programming model to decode  $F$  frames in parallel. In subsection III-D the parallel decoding of  $F$  frames is called kernel 2.

### B. Target architecture

In this study, we focused on embedded devices equipped with ARM and GPU processors. One example is Jetson K1 SoCs which consists of a 4-core Cortex-A15 and an NVIDIA GK20a GPU processor.

An ARM Cortex-A15 processor is composed of 15 integer/17-25 floating point pipeline stages. To limit the level of memory access latency, it has multi-level caches as 32 KB data plus 32 KB instruction L1 cache per core and an integrated low-latency L2 cache up to 4 MB. As in terms of GPU features, concurrent kernel execution capability of this device is most used in the proposed mapping. To achieve high throughput performance on such a low-power embedded processors, SIMD and SIMT programming models are exploited in the proposed LDPC decoder.

### C. Data Interleaving/deinterleaving

The implementation of the parallel frame processing is subject to massive irregular memory access due to the structure of H-matrix. As a matter of fact, to process the same  $VN_i$  element of the  $F$  frames at the same time, non-contiguous memory access would affect performance. To solve this issue, a data interleaving process has to be performed before and after decoding stage. So each  $F$  frames are reordered to achieve an aligned memory data structure. This reordering is shown in Figure 2 [4]. In the proposed structure, interleaving and deinterleaving of frames are called kernel 1 and kernel 3.

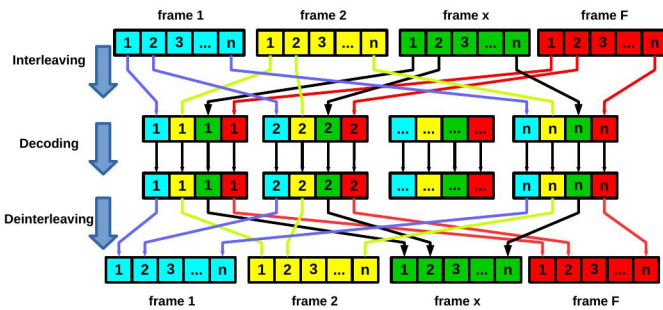


Fig. 2. Data interleaving/deinterleaving process [4]

### D. Multi Stream parallelism

SIMT programming model is used to decode  $W$  sets of  $F$  frames concurrently, with  $W$  denoting the number of concurrent streams on the GPU device. This multi-core programming is specified by CUDA API. Each GPU stream is controlled by a *pthread* called *worker* on the host machine (which is an ARM in this case). Each *worker* is responsible for its own sets of frames. By using stream based processing, the system can decode  $W \times F$  frames at the same time. The whole LDPC decoder system model is shown in Figure 3.

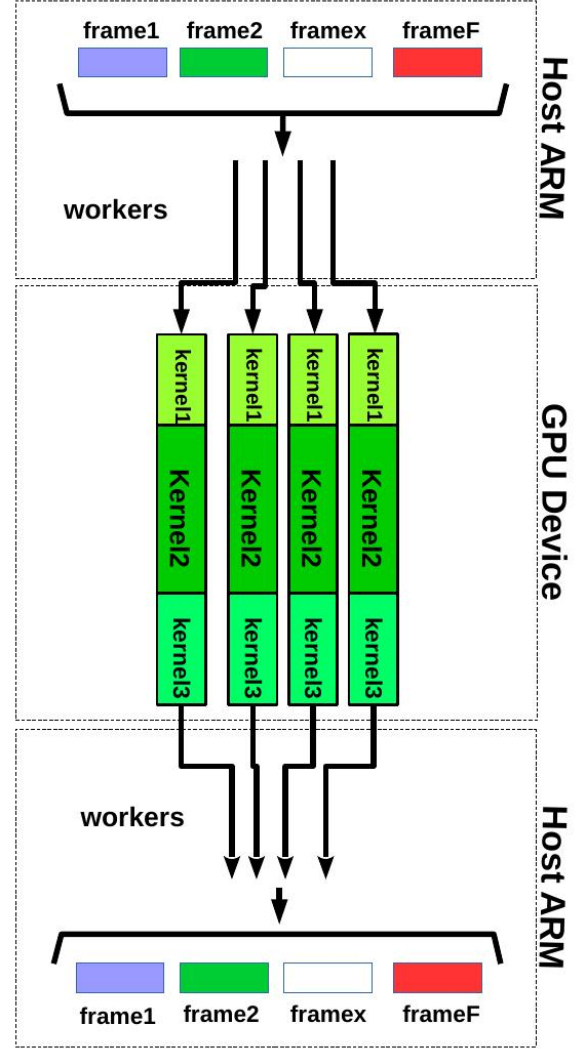


Fig. 3. LDPC Decoder Data Flow

## IV. EXPERIMENTAL RESULTS

The experiments were carried out by decoding LDPC codes using NVIDIA Tegra K1 SoCs. The programs compiled with GCC-4.8 and CUDA 6.5. The TK1 is composed of 4 cortex-A15 ARM processors and one NVIDIA Kepler "GK20a" GPU with 192 SM3.2 CUDA cores. The host platform uses a GNU/Linux kernel 3.10.40.

### A. Performance evaluation of proposed algorithm

First set of experiments was performed to achieve air throughput using different codes. The codes have different frame lengths: 576 to 9972. The air throughputs are provided in Fig.4 when {1,3} threads are used to handle {1,3} GPU streams. Measurements are performed for LDPC decoders that execute 10 layered-base decoding iterations.

Performance of one stream (or one thread) achieves 25 Mbps, while with 3 streams it can be as high as 35 Mbps. For (4000,2000) LDPC code and one thread, data transfer takes about  $2 \times 2.4$  ms, interleaving steps need about  $2 \times 5$  ms and decoding takes about 150 ms. For the same code with 3 threads, data transfer takes about  $2 \times 2.4$  ms, interleaving steps need about  $2 \times 5$  ms and decoding takes about 150 ms. So by introducing more streams to GPU device, its performance does not degrade. Comparing the latency introduced by data transfer between host and GPU device in [17] which is about 20 ms, it has been reduced to 4.8 ms because of the architecture of embedded device. On the other hand, with introducing 3 threads to GPU, its whole processing capacity is used which results to about 30% throughput improvement in most of our experiments.

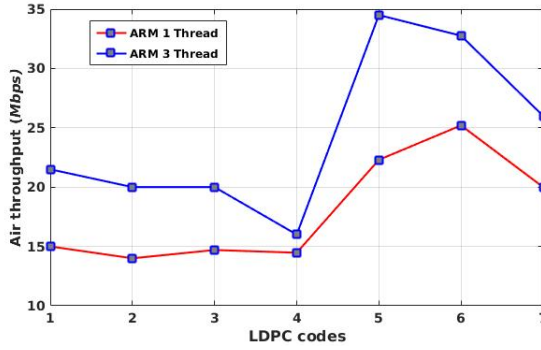


Fig. 4. Measured throughputs for 10 layered decoding iterations (1-7 LDPC codes:  $576 \times 288$ ,  $1024 \times 512$ ,  $1200 \times 600$ ,  $1944 \times 722$ ,  $4000 \times 2000$ ,  $8000 \times 4000$ ,  $9972 \times 4086$ )

### B. Performance comparison with related works

To demonstrate the efficiency of the proposed ARM decoder, its throughput was compared to ARM related work in [13]. In [13], ARM SIMD units are used to perform vector data processing in parallel frame decoding. In the experiment, the throughput of the proposed decoder is compared to their work by using 1 thread for work in [13] and 3 threads in the proposed algorithm. 10-iteration decoding performed on Tegra-K1 board gives us the results as shown in Table I. The work in [13] can achieve much higher throughputs by using more threads on ARM, but by introducing each thread, the whole capacity of one more ARM core is used for decoding. But in the proposed algorithm, by introducing one thread, just 8% process is used from ARM processor. Although by using more powerful GPU device, the algorithm can achieve much higher throughputs which has been shown

in next subsection. In Table I, it is shown that the proposed algorithm can achieve the same throughput in [13] with using 24% of ARM processing power and using its GPU device.

TABLE I  
THROUGHPUT (Mbps) COMPARISON WITH RELATED WORK

	ARM decoder , 1 thread		Proposed ARM decoder, 3 threads	
code	(Mbps)	Process	(Mbps)	Process
(4000,2000)	35	100%	34.5	24%
(8000,4000)	34	100%	33	24%

### C. Performance comparison on different GPU devices

GPU devices have different characteristics: amount of stream multiprocessors, CUDA cores, working frequencies, etc. A GPU based algorithm should have the scalability to use all processing capability of a GPU device. In Table II, proposed algorithm has been carried out on multiple GPU devices. GT540M and K620, are considered as mid-range and GTX680 and TeslaK20 are considered as high power GPU devices. The performance in Table II shows that the proposed algorithm can achieve up to 230 Mbps performance.

TABLE II  
THROUGHPUT (Mbps) OF ALGORITHM ON DIFFERENT GPUS

code	target	iter	#1 thread	#3 thread
(576,288)	GT540M	10	23	33
		5	44	61
	K620	10	23	30
		5	45	61
	GTX680	10	94	127
		5	163	217
(2304,1152)	TeslaK20	10	66	90
		5	123	165
	GT540M	10	25	37
		5	47	63
	K620	10	23	31.5
		5	47	63
(4000,2000)	GTX680	10	94	132
		5	170	226
	TeslaK20	10	66	94
		5	127	170
	GT540M	10	27	34
		5	27	37
(4000,2000)	K620	10	24	32
		5	44	60
	GTX680	10	98	131
		5	164	230
	TeslaK20	10	73	98
		5	139	196

## V. CONCLUSION

A heterogeneous approach for GPU-based LDPC decoding on embedded devices was introduced in this paper. This algorithm is based on running multiple concurrent kernels on GPU device to achieve its full processing capacity and using as less process as possible from ARM device. This approach helps to achieve desirable throughputs on embedded devices. Experimental results demonstrate that proposed algorithm is scalable and can achieve high throughputs on multiple GPU devices. Moreover, the proposed algorithm structure makes it easy for the operating system on the embedded device to control its process and performance by choosing number of streams created by the algorithm.

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