Si4700/01 Headphone and Antenna Interface

1. Introduction

This application note describes the circuit required for interfacing the Si4700/01 to a headphone antenna. When properly implemented, a 6 to 12 dB voltage gain improvement versus previous headphone recommendations is possible. It is strongly recommended that customers follow these schematic and layout recommendations in their designs to ensure optimal FM receiver performance. Silicon Laboratories will also review schematic and layout designs for qualified customers. Please work with your local Silicon Laboratories representative to assist with these reviews.

2. Headphone Antenna Overview

A typical headphone cable will contain three or more conductors. The left and right audio channels are driven by a headphone amplifier onto left and right audio conductors and the common audio conductor is used for the audio return path and FM antenna. Additional conductors may be used for microphone audio, switching, or other functions, and in some applications the FM antenna will be a separate conductor within the cable. A representation of a typical application is shown in Figure 1, “Typical Headphone Antenna Application”.

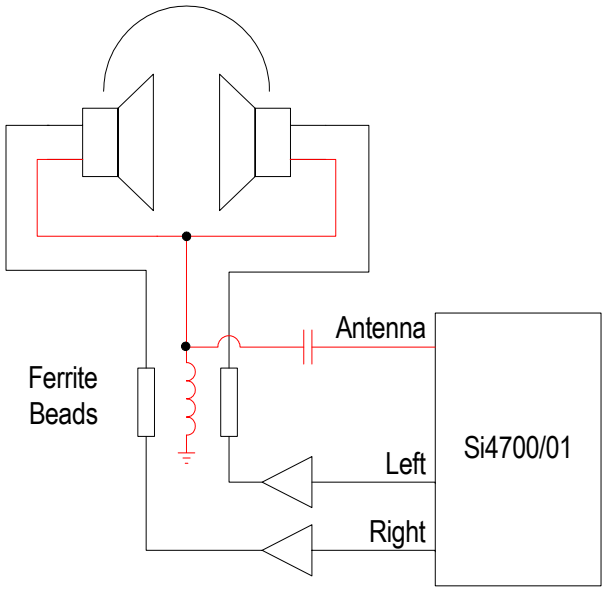

Figure 1. Typical Headphone Antenna Application

3. Si4700/01 Headphone Antenna Interface Model

The simplified circuit model for the Si4700/01 headphone antenna interface shown in Figure 2, “Si4700/01 Antenna and Matching Network Model”, and includes the headphone antenna, matching inductor, PCB and Si4700/01 LNA. This section discusses maximizing voltage gain across the FM band at the LNA input by varying headphone antenna and PCB parameters, and selecting the optimal matching inductor. It is very important to note that the Si4700/01 performance is optimized by maximizing input voltage, not power.

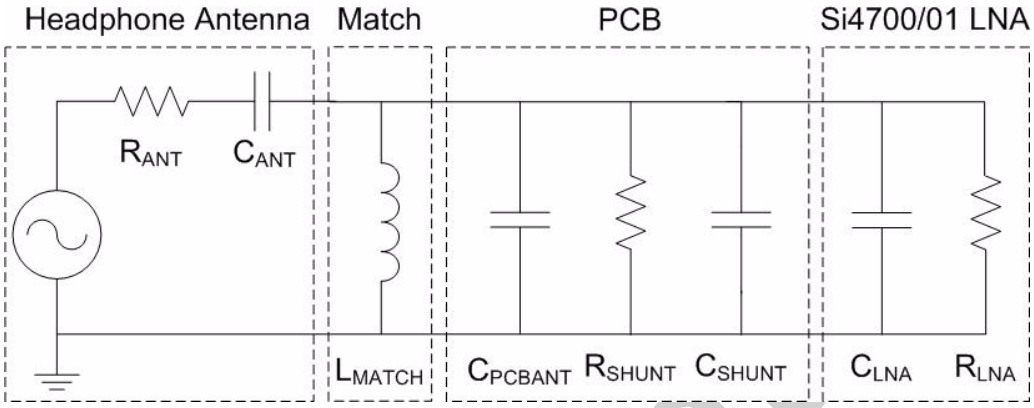

Figure 2. Si4700/01 Antenna and Matching Network Model

R_{ANT} - Antenna Resistance
C_{ANT} - Antenna Capacitance
L_{MATCH} - Inductance Match
C_{PCBANT} - PCB Antenna Trace Capacitance
R_{SHUNT} - Shunt Resistance of Ferrites
C_{SHUNT} - Audio Conductor Shunt Capacitance
C_{LNA} - LNA Capacitance
R_{LNA} - LNA Resistance

The Si4700/01 antenna and matching network model can be further simplified and represented in the form of a parallel resonant RLC circuit as shown in Figure 3, “Si4700/01 Parallel Resonant RLC Circuit Model”. In this simplified model the parallel resistance, R_P, represents the antenna resistance, R_{ANT}, the shunt resistance of ferrites on the left and right audio conductors, R_{SHUNT}, and the LNA resistance, R_{LNA}. The parallel capacitance, C_P, represents the antenna capacitance, C_{ANT}, PCB antenna trace capacitance, C_{PCBANT}, audio conductor shunt capacitance, C_{SHUNT}, and LNA capacitance, C_{LNA}.

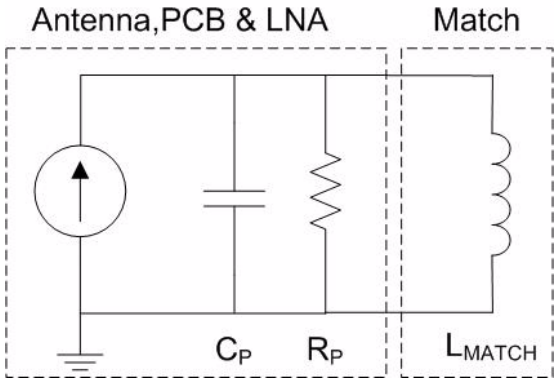

Figure 3. Si4700/01 Parallel Resonant RLC Circuit Model

C_P = Parallel capacitance

R_P = Parallel resistance

L_{MATCH} = Inductance Match

L_{MATCH} is required to prevent the antenna from being shorted to ground at RF frequencies and to provide a path to ground at audio frequencies for return current from the headphone amplifier. Selecting the proper value of L_{MATCH} will maximize voltage gain across the FM band for optimal RF performance.

To maximize voltage gain across the FM band:

1. The value of R_P should be maximized to maximize the voltage at the LNA input.
2. The Q of the circuit should be minimized to maintain a flat response across the FM band.
3. The value of L_{MATCH} should be chosen such that the circuit resonates in the center of the FM band.

The value of R_P should be maximized to maximize the voltage at the LNA input. The parallel resistance, R_P, shown in Figure 3, “Si4700/01 Parallel Resonant RLC Circuit Model” is defined as:

$$R_P = R_{LNA} \| R_{SHUNT} \| R_{ANT}^*$$

The LNA resistance, R_{LNA}, will range from 4 to 6 kΩ during normal operation. The shunt resistance, R_{SHUNT}, is the parallel addition of ferrite resistance on the left and right audio conductors, and other conductors for microphone audio, switching or other circuits, if applicable. R_{SHUNT} should be as large as possible to maximize RP. Specific recommendations for ferrite values can be found in Section “4. Si4700/01 Schematic Guidelines”. The antenna source resistance, R_{ANT}, will range from approximately 500 Ω for shorter antennas to several thousand ohms for longer antennas. R_{ANT}^* is the parallel circuit model for R_{ANT} near the resonant frequency, f, of the RLC circuit, and is approximated as:

$$R_{ANT}^* \approx R_{ANT}(Q_{ANT}^2 + 1) = R_{ANT}\left(\left(\frac{1}{2\pi f R_{ANT} C_{ANT}}\right)^2 + 1\right)$$

The antenna length should be 1.1 to 1.45 m, with optimal performance at 1.45 m to maximize R_{ANT}^*.

The Q of the parallel resonant RLC circuit shown in Figure 3, “Si4700/01 Parallel Resonant RLC Circuit Model” is defined as:

$$Q_P = \frac{R_P}{\sqrt{\frac{L_P}{C_P}}}$$

The Q of the circuit should be minimized to maintain a flat response across the FM band. To minimize the Q of the circuit with a parallel resistance, R_P, that is maximized, the parallel capacitance, C_P, should be minimized and L_{MATCH} should be maximized.

The parallel capacitance, C_P, shown in Figure 3, “Si4700/01 Parallel Resonant RLC Circuit Model” is defined as:

$$C_P = C_{PCBANT} \| C_{SHUNT} \| C_{LNA} \| C_{ANT}^*$$

The PCB antenna trace capacitance, C_{PCBANT}, is determined by the structure of the trace and is typically 3 to 4 pF per inch as a rule of thumb. The audio conductor shunt capacitance, C_{SHUNT}, is the parallel addition of PCB trace and component capacitance with respect to ground on the left and right audio conductors, and other conductors such as the microphone and switch if applicable. Both C_{PCBANT} and C_{SHUNT} should be as small as possible to minimize C_P. Specific schematic and layout recommendations minimizing C_{SHUNT} can be found in Section “4. Si4700/01 Schematic Guidelines” and Section “5. Si4700/01 Placement and Routing Guidelines”. Specific layout recommendation for minimizing C_{PCBANT} can be found in Section “5. Si4700/01 Placement and Routing Guidelines”. The LNA capacitance, C_{LNA}, will range from 4 to 6 pF during normal operation. The antenna capacitance, C_{ANT}, will range from zero to several picofarads, depending on antenna length. C_{ANT}^* is the parallel circuit model of C_{ANT} near the resonant frequency, f, of the RLC circuit, and is approximated as:

$$C_{ANT}^* \approx C_{ANT}\left(\frac{Q_{ANT}^2}{Q_{ANT}^2 + 1}\right) \approx C_{ANT} \text{ ,for } Q \gg 1$$

For a given value of parallel capacitance C_P, the inductor value L_{MATCH} should be chosen such that the circuit resonates at the center of the FM band. The resonant frequency, f, of the parallel RLC circuit shown in Figure 3, “Si4700/01 Parallel Resonant RLC Circuit Model” is defined as:

$$f = \frac{1}{2\pi \cdot \sqrt{L_{MATCH} C_P}}$$

Normally it is difficult to reliably measure all of the impedances required to calculate an optimal value for L_{MATCH}. An easier approach is to measure the system performance with different values of L_{MATCH} and choose the best values based on these measurements. Typical L_{MATCH} values range from 100 to 400 nH.

There are two test methods available for selecting the correct value of L_{MATCH} to properly tune the headphone antenna interface circuit. Both methods require injecting a test signal from a signal generator into the network through a source resistance, R_{TEST}, and adjusting the matching inductor, L_{MATCH}, to maximize the voltage at the LNA input at several points across the FM band. R_{TEST} should be 20 kΩ or larger to prevent loading of the resonant antenna circuit. Figure 4, “Parallel Resonant RLC Circuit Model Test Circuit” shows the parallel resonant RLC model test circuit required for both test methods.

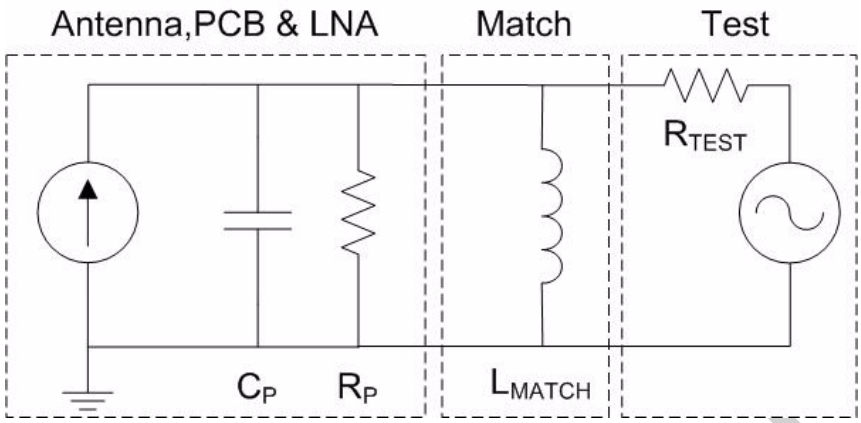

Figure 4. Parallel Resonant RLC Circuit Model Test Circuit

The first test method requires reading the received signal strength (RSSI) measured by the Si4700/01 and the second method requires probing the LNA input with a low-capacitance FET probe and spectrum analyzer. The advantage of the RSSI method is that no external measurement equipment is required; however, a provision must be made for reading RSSI from the device. The advantage of the FET probe method is that reading the RSSI from the Si4700/01 is not necessary, and measurement accuracy by using a spectrum analyzer and probe will be improved; however, excess capacitive loading of the FET probe may affect the measurement results. Care should be taken to select a probe with minimum capacitance when using this approach. Figure 5, "Si4700/01 Example Test Signal Injection Frequency Response" shows the frequency response for four values of L_{MATCH} using the RSSI tuning method.

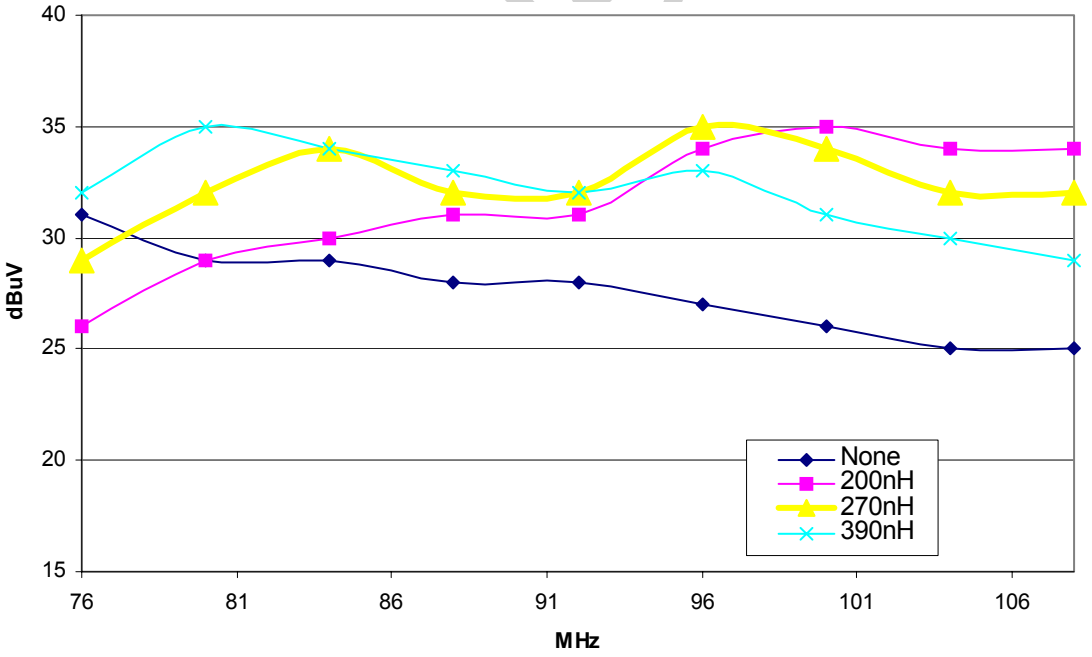

Figure 5. Si4700/01 Example Test Signal Injection Frequency Response

It is clear from Figure 5, “Si4700/01 Example Test Signal Injection Frequency Response” that the matching inductor, L_{MATCH}, is preferred to no matching inductor, however, selecting the best value for L_{MATCH} can be difficult by inspection.

Select the optimal value for L_{MATCH} by following these guidelines:

1. The mean value of RSSI should be maximized.
2. The standard deviation of RSSI should be minimized.

Table 1 shows 270 nH is the optimal choice for L_{MATCH} because it maximizes the mean RSSI and minimizes the RSSI standard deviation.

Table 1. Si4700/01 Example Test Signal Injection Mean and Standard Deviation

	200 nH	270 nH	390 nH
Mean (dB)	31.5	32.4	32.1
Standard Deviation (dB)	3.0	1.7	1.9

4. Si4700/01 Schematic Guidelines

Figure 6, “Minimal Application Schematic” shows an application schematic of the Si4700/01 with the minimal recommended components to use the headphone cable as an FM antenna.

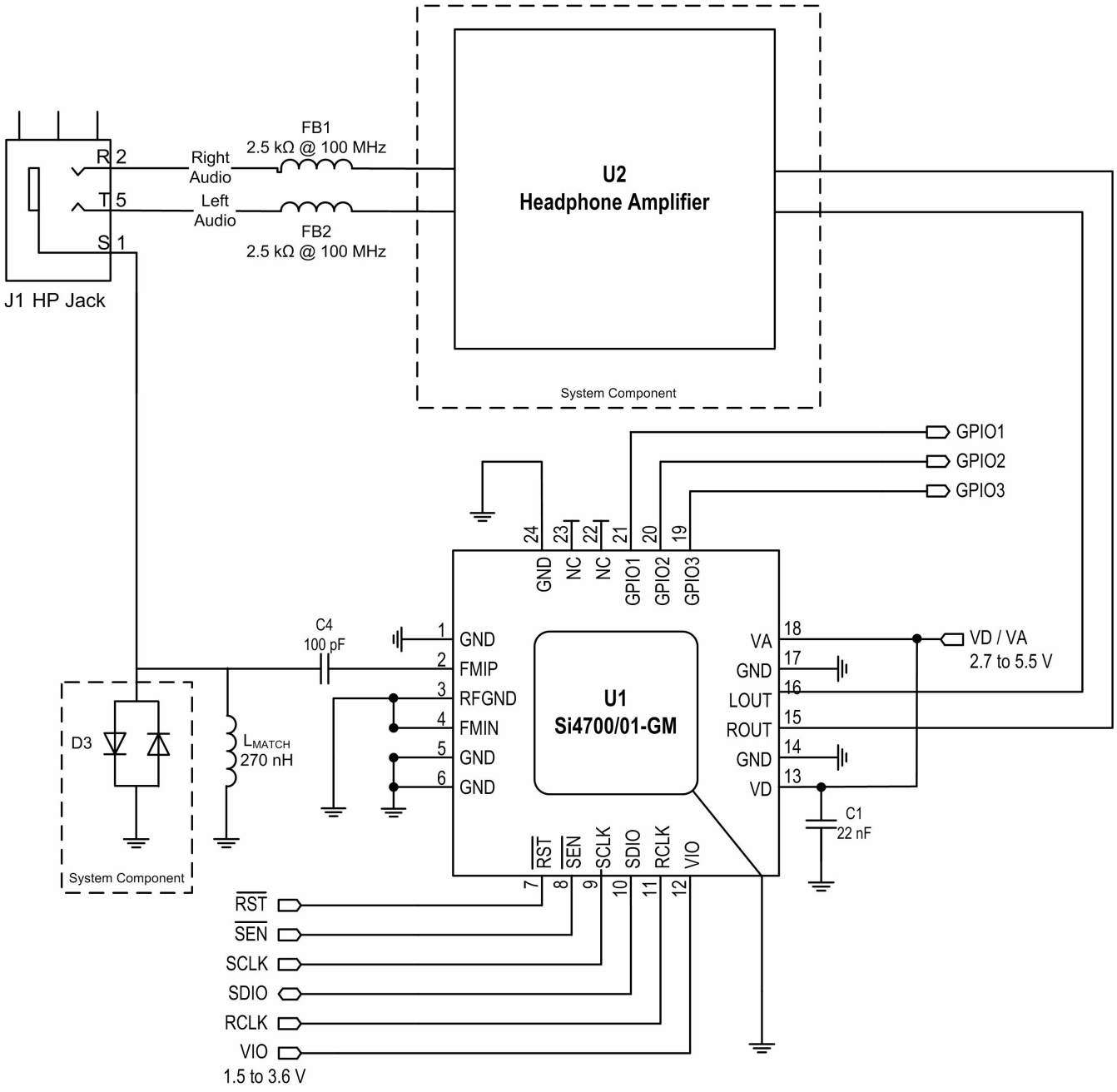

Figure 6. Minimal Application Schematic

Following the schematic and layout recommendations detailed in this document will result in optimal tuner performance with the minimal application schematic shown in Figure 6, “Minimal Application Schematic”.

For systems with constraints preventing implementation of these recommendations, optional components may be placed to address excess system noise or ESD concerns. Generally it is not the case that all optional components are required to return to optimal tuner performance.

The Si4700/01 requires components L_{MATCH}, C1, C4, FB1 and FB2 for a minimal implementation. The purpose of each of these components is described in later in this section. The ESD protection diode, D3, and headphone amplifier, U2, are system components that will be required for proper implementation of any tuner.

Figure 7, “Typical Application Schematic” shows an application schematic of the Si4700/01 with recommended components to use the headphone cable as an FM antenna.

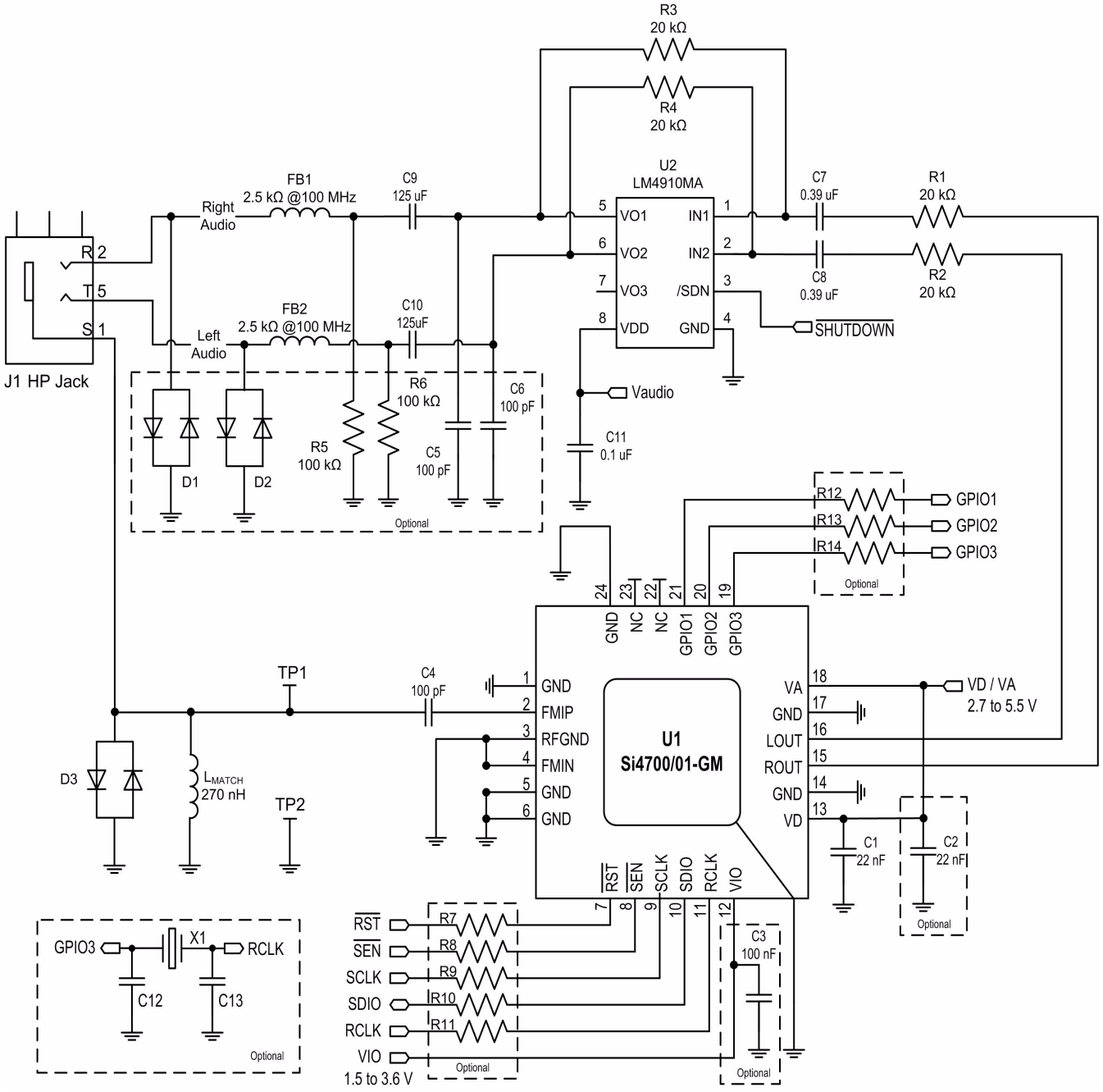

Figure 7. Typical Application Schematic

Ferrite beads FB1 and FB2 provide a low-impedance audio path and high-impedance RF path between the headphone amplifier and the headphone. Ferrite beads should be placed on each antenna conductor connected to nodes other than the FMIP such as left and right audio, microphone audio, switching, etc. In the example shown in Figure 7, “Typical Application Schematic”, these nodes are the left and right audio conductors. Ferrite beads should be 2.5 kΩ or greater at 100 MHz, such as the Murata BLM18BD252SN1. High resistance at 100 MHz is desirable to maximize R_{SHUNT}, and therefore, R_P.

ESD diodes D1, D2, and D3 are recommended if design requirements exceed the ESD rating of the headphone amplifier and the Si4700/01. Diodes should be chosen with no more than 1 pF parasitic capacitance, such as the California Micro Devices CM1210. Diode capacitance should be minimized to minimize C_{SHUNT}, and therefore, C_P. If D1 and D2 must be chosen with a capacitance greater than 1 pF, they should be placed between the ferrite beads FB1 and FB2 and the headphone amplifier to minimize C_{SHUNT}. This placement will, however, reduce the effectiveness of the ESD protection devices. Diode D3 may not be relocated and must therefore have a capacitance less than 1 pF. Note that each diode package contains two devices to protect against positive and negative polarity ESD events.

Inductor L_{MATCH} is selected to maximize the voltage gain across the FM band as described in Section “3. Si4700/01 Headphone Antenna Interface Model”. L_{MATCH} should be selected with a Q if 15 or greater at 100 MHz and minimal dc resistance. Test points TP1 and TP2 may be used for the purpose of injecting a test signal into the circuit for tuning L_{MATCH}. The size of TP1 and TP2 should be minimized to minimize PCB antenna trace capacitance, C_{PCBANT}.

Ac-coupling capacitors C9 and C10 are used to remove the headphone amplifier common mode voltage. The high pass corner frequency of the ac coupling capacitors, C9 and C10, and the headphone speaker element resistance, $R_{HEADPHONE}$, is defined as:

$$f_{CRIGHT} = \frac{1}{2\pi \cdot R_{HEADPHONE} \cdot C9}, f_{CLEFT} = \frac{1}{2\pi \cdot R_{HEADPHONE} \cdot C10}$$

Note that $R_{HEADPHONE}$ will typically be 16, 32 or 64 Ω.

Optional bleed resistors R5 and R6 may be desirable to discharge the ac-coupling capacitors when the headphone cable is removed. The high pass corner frequency of the ac coupling capacitors, C9 and C10, and the headphone resistance, $R_{HEADPHONE}$, and the bleed resistance is defined as:

$$f_{CRIGHT} = \frac{1}{2\pi \cdot R_{HEADHONE} \parallel R5 \cdot C9}, f_{CLEFT} = \frac{1}{2\pi \cdot R_{HEADHONE} \parallel R6 \cdot C10}$$

When R5 and R6 are significantly larger than the headphone resistance, $R_{HEADPHONE}$, their impact on the high pass corner frequency becomes negligible.

Ac-coupling capacitor C4 is used to remove a dc offset on the FMIP input of the Si4700/01. This capacitor must be chosen to be large enough to cause negligible loss with an LNA input capacitance of 4–6 pF. The recommended value is 100 pF–1 nF.

The Si4700/01 requires a single 22 nF bypass capacitor C1 for the VD supply pin. In addition, optional bypass capacitors C2 and C3 may be placed as a precaution against excessive supply noise. The recommended value for C2 is 22 nF and for C3 is 100 nF. Bypass capacitors should be placed as close as possible to the pins that they bypass.

Optional RF shunt capacitors C5 and C6 may be placed on the left and right audio traces at the headphone amplifier output to reduce the level of digital noise passed to the antenna. The recommended value is 100 pF or greater, however, the designer should confirm that the headphone amplifier is capable of driving the selected shunt capacitance.

Optional series termination resistors R7–R14 may be placed to reduce inductive coupling generated by system controller activity and noise. The recommended range of values for R7–R14 is 25 Ω to 2 kΩ, with 2 kΩ being the recommended value for optimal edge rate and noise suppression. When series termination resistors are being

used, the designer should confirm that the host controller drivers are capable of meeting the maximum and minimum input voltage thresholds for the Si4700/01. Refer to the V_{IL} and V_{IH} specifications for the control interface pins in the Si4700/01 data sheet.

This schematic example uses the National Semiconductor LM4910 headphone amplifier. Passive components R1–R4 and C7–C8 are required for the LM4910 headphone amplifier as described in the LM4910 data sheet. The gain of the right and left amplifiers is –R3/R1 and –R4/R2, respectively. These gains can be adjusted by changing the values of resistors R3 and R4. As a general guide, gain between 0.6 and 1.0 is recommended for the headphone amplifier, depending on the gain of the headphone elements. Capacitors C7 and C8 are ac-coupling capacitors required for the LM4910 interface. These capacitors, in conjunction with resistors R1 and R2, create a high-pass filter that sets the audio amplifier's lower frequency limit. The high-pass corner frequencies for the right and left amplifiers are:

$$f_{CRIGHT} = \frac{1}{2\pi \cdot R1 \cdot C7}, f_{CLEFT} = \frac{1}{2\pi \cdot R2 \cdot C8}$$

With the specified BOM components, the corner frequency of the headphone amplifier is approximately 12 Hz; however, the corner frequency of the headphone will be set by the ac coupling capacitors, C9 and C10, and the headphone resistance, $R_{HEADPHONE}$. For a $R_{HEADPHONE}$ value of 32 Ω and ac coupling capacitor value of 125 µF, the corner frequency for the headphones is approximately 40 Hz.

Capacitor C11 is the supply bypass capacitor for the audio amplifier. The LM4910 can also be shut down by applying a logic low voltage to the number 3 pin. The maximum logic low level is 0.4 V and the minimum logic high level is 1.5 V.

The bill of materials for the typical application schematic shown in Figure 6 is provided in Table 2. Note that manufacturer is not critical for resistors and capacitors.

Table 2. Typical Application Schematic Bill of Material

REF	DESCRIPTION	VALUE	Manufacturer	Part Number
C1,C2	CAP,SM,0402,X7R	22 NF		
C3	CAP,SM,0402,X7R	0.1 UF		
C4,C5,C6	CAP,SM,0402,X7R	100 PF		
C7,C8	CAP,SM,0603,0.33UF,X7R	0.33 UF		
C9,C10	CAP,SM,0805	125 UF		
C11	CAP,SM,0402,X7R	0.1 UF		
C12,C13	CAP,SM,0402,C0G	22 PF		
D1,D2,D3	IC,SM,ESD DIODE,SOT23-3		CALIFORNIA MICRO DEVICES	CM1210-01ST
FB1,FB2	FERRITE BEAD,SM,0603	2.5 K	MURATA	BLM18BD252SN1D
LMATCH	IND,0603,SM	270 nH	MURATA	LQW18ANR27J00D
R1,R2,R3,R4	RES,SM,0603	20 K		
R5,R6	RES,SM,0603	100 K		
R7-R14	RES,SM,0402	2 K		
U1	IC,SM,SI4700/01,MLP24		SILICON LABORATORIES	SI4700/01
U2	IC,SM,HEADPHONE AMP		NATIONAL SEMICONDUCTOR	LM4910MA
X1	CRYSTAL		EPSON	FC-135

5. Si4700/01 Placement and Routing Guidelines

Figure 8, “Primary and Secondary Side Placement” shows an example primary side and secondary side layout for the circuit shown in Figure 7, “Typical Application Schematic,” on page 8.

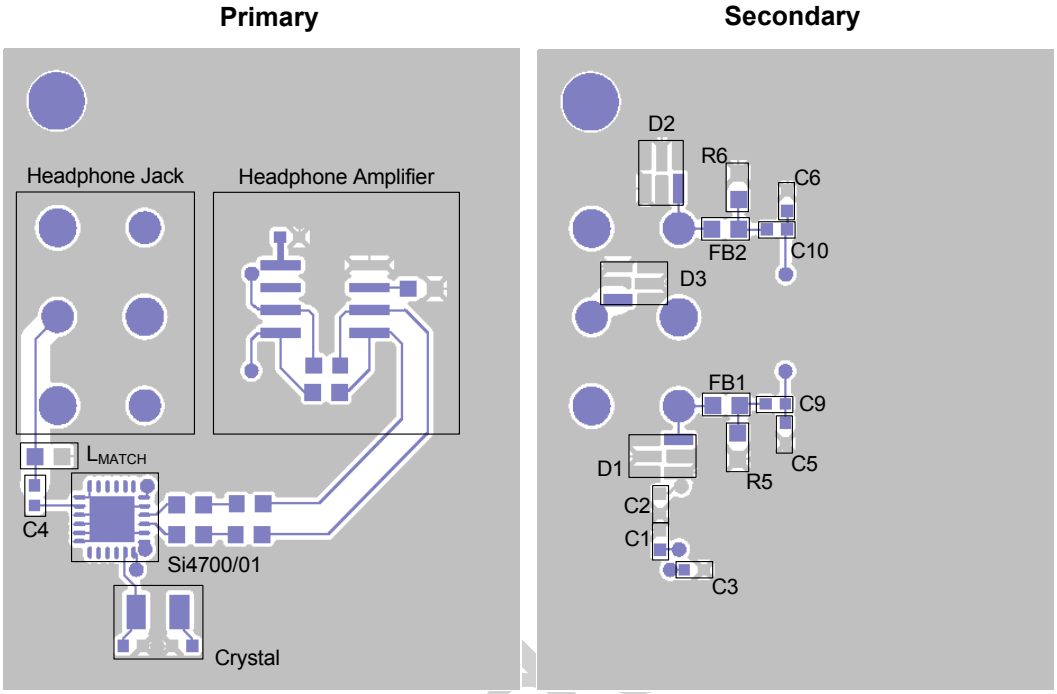

Figure 8. Primary and Secondary Side Placement

This is the recommended layer stack for a four layer PCB:

1. Primary Signal
2. GND
3. Power
4. Secondary Signal

To minimize inductive and capacitive coupling, inductor L_{MATCH} and headphone jack J1 should be placed together and as far from noise sources such as clocks and digital circuits as possible. L_{MATCH} should be placed near the headphone connector to keep audio currents away from the Si4700/01.

To minimize C_{SHUNT} and C_P, place ferrite beads FB1 and FB2 as close as possible to the headphone connector.

To maximize ESD protection diode effectiveness, place diodes D1, D2 and D3 as close as possible to the headphone connector. If capacitance larger than 1 pF is required for D1 and D2, both components should be placed between FB1 and FB2 and the headphone amplifier to minimize C_{SHUNT}.

To minimize antenna trace capacitance, C_{PCBANT}, keep trace length short and narrow and as far above the reference plane as possible, restrict the trace to a microstrip topology (trace routes on the top or bottom PCB layers only), minimize trace vias, and relieve ground fill on the trace layer. Note that minimizing capacitance has the effect of maximizing characteristic impedance. It is not necessary to design for 50 Ω transmission lines.

To reduce the level of digital noise passed to the antenna, RF shunt capacitors C5 and C6 may be placed on the left and right audio traces close to the headphone amplifier audio output pins. The recommended value is 100 pF or greater, however, the designer should confirm that the headphone amplifier is capable of driving the selected shunt capacitance.

To minimize inductive and capacitive coupling, avoid routing any digital, analog, or RF trace in parallel with each other and avoid routing signals traces under the IC without a reference plane between the IC and the trace. In particular, care should be taken to avoid routing digital signals or reference clock traces near or parallel to the LNA

inputs (pins 2,3,4), the VCO (pins 22,23), or the antenna trace. Avoid routing any digital or RF traces over ground or power plane breaks if the ground or power plane is being used as the reference plane. These recommendations can be best followed by using layer 2 as the ground plane.

To minimize ground pin potential differences, all GND (including RFGND) pins should be tied to the ground paddle and the ground paddle should be connected to the ground plane on layer 2 using multiple vias. Figure 9, “All GND pins (including RFGND and FMIN) tied to the Ground Paddle” shows an example of this routing.

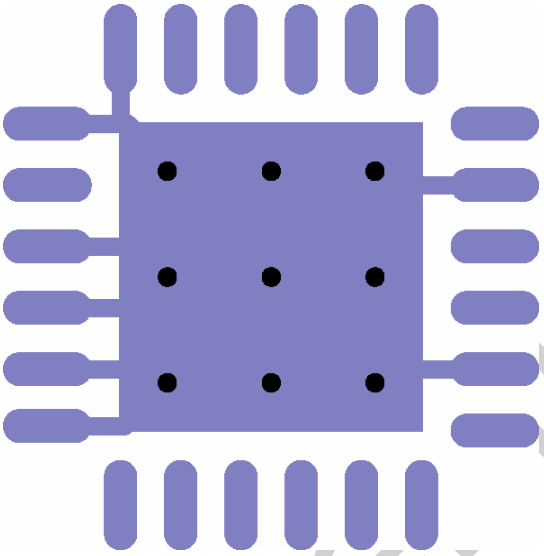

Figure 9. All GND pins (including RFGND and FMIN) tied to the Ground Paddle

If it isn't possible to connect the GND paddle directly to the ground plane on layer 2, it is permissible to connect each GND pin to the ground plane outside the IC perimeter with a via. Care should be taken to minimize the trace length for pins 5, 14, and 17 as they are the ground return paths for VIO, VD and VA supplies, respectively, and ensure an unobstructed ground return path to the power supply. Similarly, care should be taken to minimize the trace length for pins 3 and 4, as pin 3 is the RFGND return path to the LNA and pin 4 is grounded negative side of the LNA. Figure 10, “All GND pins (including RFGND and FMIN) tied to the layer 2 ground plane outside the IC Perimeter” shows an example of this routing.

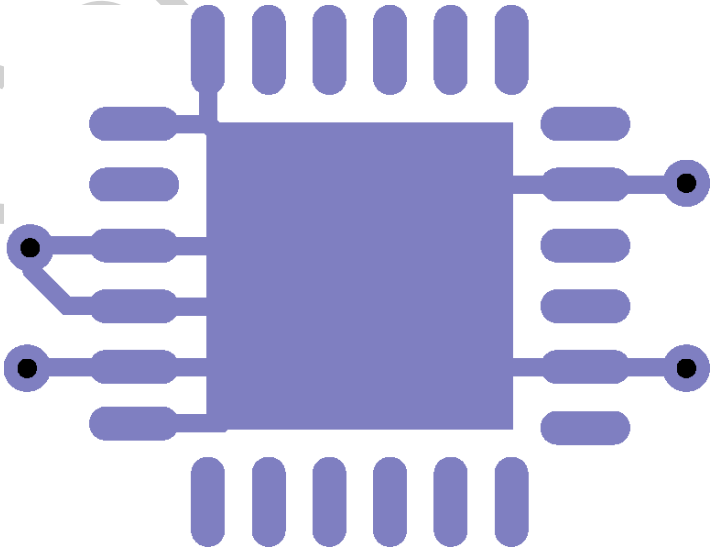

Figure 10. All GND pins (including RFGND and FMIN) tied to the layer 2 ground plane outside the IC Perimeter

To minimize inductive coupling generated by system controller activity and noise, place optional series termination resistors R7–R14 near the signal source. For bi-directional signal SDIO, the series termination should be placed near the SCLK series termination resistor.

To reduce inductive coupling to the antenna trace, the antenna loop inductance should be minimized. This can be accomplished by keeping the ground plane under the antenna trace should be free of obstructions such as breaks, slots or vias to provide a low impedance path for return currents to flow under the signal trace. Figure 8, “Primary and Secondary Side Placement” shows an optimized antenna trace layout.

To minimize inductive and capacitive coupling, other circuits in the system should be designed, placed and routed to minimize radiation in the FM band. This applies in particular to digital circuits such as SIM cards, memories, displays, and system controllers. **These devices often operate in a frequency range which lies inside the FM band, or generate harmonics that lie inside the FM band, and can interfere with radio**.

APPENDIX A—ANTENNA WITH AUDIO COMMON MODE

Figure 11, “Typical Application Schematic with Antenna at Audio Common Mode Voltage” shows a schematic of the Si4700/01 with components required to use the headphone cable as an FM antenna when the audio return and FM antenna are biased with a common mode voltage. This is the configuration used for all Si4700/01 EVBs.

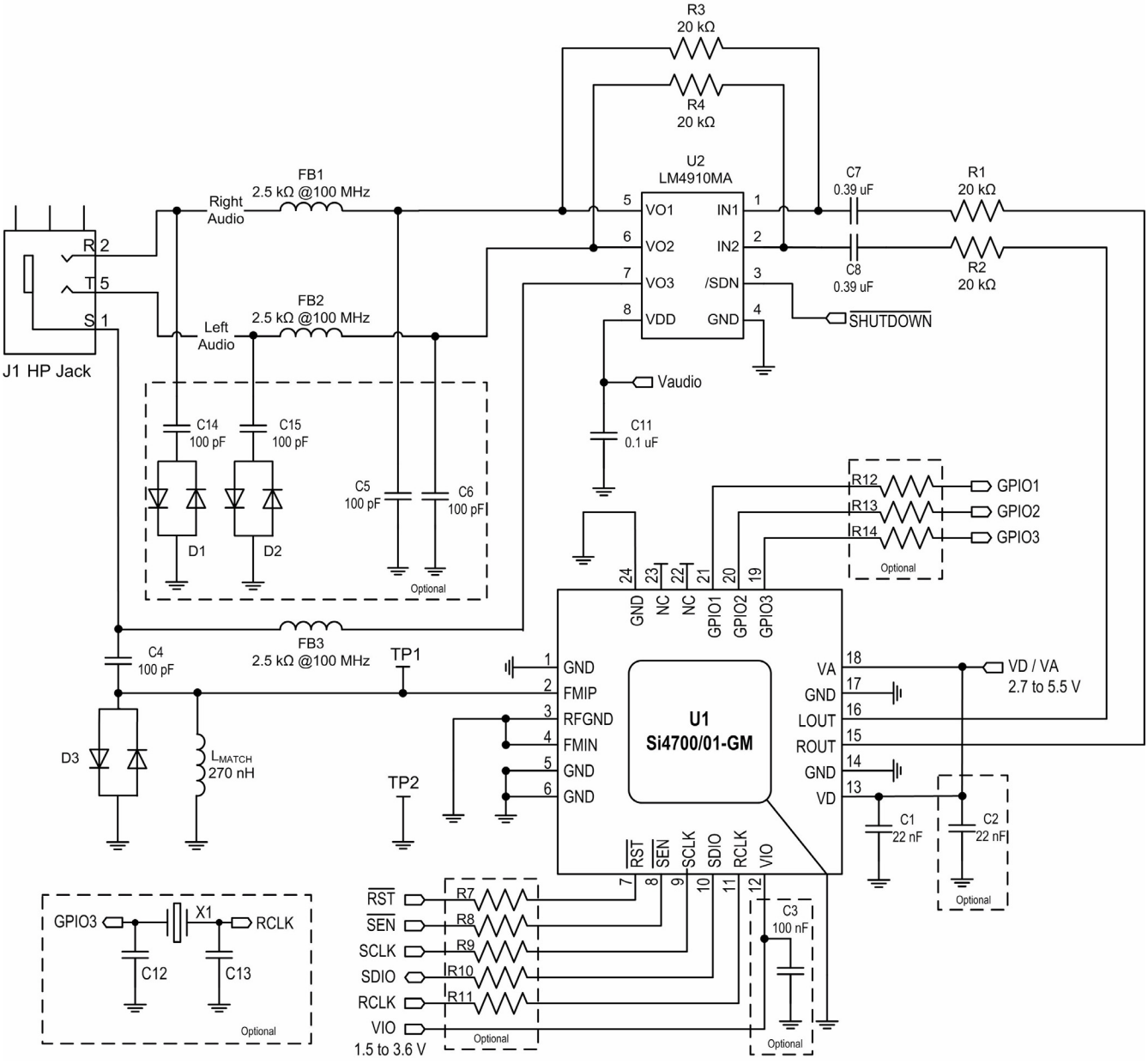

Figure 11. Typical Application Schematic with Antenna at Audio Common Mode Voltage

Ferrite bead FB3 provides a low-impedance audio path and high-impedance RF path for audio return currents. The ferrite bead should be 2.5 kΩ or greater at 100 MHz with low dc resistance of 0.9 Ω or less, such as the Murata BLM18BD252SN1. High resistance at 100 MHz is desirable to maximize R_{SHUNT}, and therefore, R_P, and low dc resistance is desirable to minimize audio crosstalk. To minimize C_{SHUNT}, and therefore C_P, ferrite bead FB3 should be placed near the headphone connector.

The common mode voltage is at approximately half the amplifier supply voltage and is at the same dc potential as the left and right amplifier outputs. This topology maximizes the swing for the headphone amplifiers and eliminates dc currents. This arrangement eliminates the need for ac-coupling capacitors C9 and C10 and bleed resistors R5 and R6 that are typically required in amplifiers with only two outputs and a return path to ground.

To prevent the positive side diode from clamping in response to the audio common mode voltage, the RF ac-coupling cap C4 must be placed between the ESD diode D3 and ferrite bead FB3. To maintain effectiveness of the ESD diode, D3 and therefore C4, must be placed near the headphone connector pin.

Similarly, cap C12 must be placed between the right audio trace and diode D1 and cap C13 must be placed between the left audio trace and diode D2. To maintain effectiveness of the ESD diodes, D1 and D2, and therefore C12 and C13, must be placed near the headphone connector pins.

The bill of materials for the antenna with audio common mode application circuit shown in Figure 11, “Typical Application Schematic with Antenna at Audio Common Mode Voltage” is provided in Table 3.

Table 3. Antenna with Common Audio Mode Application Bill of Materials

REF	DESCRIPTION	VALUE	Manufacturer	Part Number
C1,C2	CAP,SM,0402,X7R	22 NF		
C3	CAP,SM,0402,X7R	0.1 UF		
C4,C5,C6, C14,C15	CAP,SM,0402,X7R	100 PF		
C7,C8	CAP,SM,0603,0.33UF,X7R	0.33 UF		
C11	CAP,SM,0402,X7R	0.1 UF		
C12,C13	CAP,SM,0402,C0G	22 PF		
D1,D2,D3	IC,SM,ESD DIODE,SOT23-3		CALIFORNIA MICRO DEVICES	CM1210-01ST
FB1,FB2,FB3	FERRITE BEAD,SM,0603	2.5 K	MURATA	BLM18BD252SN1D
LMATCH	IND,0603,SM	270 NH	MURATA	LQW18ANR27J00D
R1,R2,R3,R4	RES,SM,0603	20 K		
R5,R6	RES,SM,0603	100 K		
R7-R14	RES,SM,0402	2 K		
U1	IC,SM,SI4700,MLP24		SILICON LABORATORIES	
U2	IC,SM,HEADPHONE AMP		NATIONAL SEMICONDUCTOR	LM4910MA
X1	CRYSTAL		EPSON	FC-135

APPENDIX B—DESIGN CHECKLIST

- **Select** an antenna length of 1.1 to 1.45 m.
- **Select** matching inductor L_{MATCH} to maximize signal strength across the FM band.
- **Select** matching inductor L_{MATCH} with a Q of 15 or greater at 100 MHz and minimal dc resistance.
- **Select** ferrite beads FB1-FB3 with 2.5 kΩ or greater resistance at 100 MHz to maximize R_{SHUNT}, and therefore R_P.
- **Select** ferrite bead FB3 (if applicable) with minimal dc resistance to reduce audio crosstalk.
- **Select** ESD diodes D1–D3 with minimum capacitance to reduce C_{SHUNT}, and therefore C_P.
- ***Place** the Si4700/01 close to the headphone connector to minimize antenna trace length. Minimizing trace length reduces C_P and the possibility for inductive and capacitive coupling into the antenna by noise sources. This recommendation must be followed for optimal device performance.*
- **Place** inductor L_{MATCH} and headphone connector together and as far from potential noise sources as possible to reduce capacitive and inductive coupling.
- **Place** ferrite beads FB1-FB3 close to the headphone connector to minimize C_{SHUNT}, and therefore, C_P.
- **Place** ESD diodes D1–D3 as close as possible to the headphone connector for maximum effectiveness.
- **Place** optional RF shunt capacitors near the headphone amplifier left and right audio output pins to reduce the level of digital noise passed to the antenna.
- **Place** optional system controller series termination resistors near the signal source, typically the system controller.
- **Place** VD bypass capacitor C1, and optional VA and VIO bypass capacitors C2 and C3, as close as possible to supply pins they bypass for maximum effectiveness.
- **Do Not Route** digital, analog and RF traces parallel with one-another to minimize inductive and capacitive coupling.
- **Do Not Route** traces under the Si4700/01 without a reference plane between the IC and the signal trace. In particular, care should be taken to avoid routing digital signals or reference clocks traces near or parallel to the LNA inputs (pins 2,3,4), the VCO (pins 22,23), the or antenna trace. This recommendation is made to minimize inductive and capacitive coupling.
- **Do Not Route** digital or RF traces over ground or power plane breaks. Signals and vias should be routed such that the ground plane is as solid as possible, with no large slots. Ground fills on other layers should have plentiful vias to the ground plane. This recommendation is made to minimize RF radiation.
- **Route** the antenna trace such that antenna capacitance, C_{PCBANT}, and therefore C_P, is minimized. To minimize capacitance, keep trace length short and narrow and as far above the reference plane as possible, restrict the antenna trace to a microstrip topology (trace routes on the top or bottom PCB layers only), minimize trace vias, relieve ground fill on the trace layer.
- **Route** the antenna trace over an unobstructed ground plane to minimize antenna loop area and inductive coupling.
- **Route** all Si4700/01 ground pins to the ground paddle to minimize ground potential differences.
- ***Design**, **Place** and **Route** other circuits such that radiation in the FM band is minimized.*

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.
4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: FMinfo@silabs.com
Internet: www.silabs.com