*ECE 382V Spring 2004*

# Optimization Issues in VLSI CAD

**Lecture 1, Jan. 21, 2004**

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## What is a good lecture?

1. Understandable to everyone
2. Understandable to intended audience
3. Understandable to experts only, such as the speaker
4. Understandable to nobody, including the speaker



## Intended Audience

- VLSI CAD (also known as EDA – electronic design automation) students, in particular for chip implementation (physical design) and planning
- Circuit design students to understand how tools work behind the scene
- Process students, to understand optimization to optimize process, such as metal wire width, thickness, and so on
- Mathematical/Computer Science majors who want to find tough problems to solve
  - Lots of VLSI CAD problems can be formulated into combinatorial optimization or mathematical programming problems.
  - Actually, most CAD problems are NP-complete -> heuristics



## Course Objectives

- Equip you with fundamental knowledge and optimization techniques with underlying modeling issues to solve modern VLSI CAD problems (mainly in the area of physical design closure and low power)
- Help you to identify PhD dissertation topics, improve your summer internship or job opportunities by working on relevant problems that industry cares
- Get deep into selected topics of your choice => publishable results
- Get broad into many cutting edge results by reading extensive set of research papers



## Course Logistics

- Lecture Hours: MW 2-:3:30pm
- Location: ENS 116
- Instructor: David Z. Pan
  - Email: dpan@ece.utexas.edu (best way to reach me)
  - Office: ACES 5.434; Phone: 471-1436
  - Office Hour: after class (3:30-4:30pm) & by appointment.
- Class web page
  - http://www.ece.utexas.edu/~dpan/ee382v_sp04
  - For class attendees only. Please do not distribute
  - UT Direct Blackboard for Discussion Forum (use your EID to login)
- Prerequisites
  - Basic understand of algorithms (EE360C)
  - Basic understand of VLSI (EE360R)



## Course Reader

- No textbook is required
- Some reference books are reserved at the Engineering Library for three-day loan
  - David Chinnery and Kurt Keutzer, *Closing the Gap Between ASIC & Custom, Kluwer*, Academic Publishers, 2002
  - Roy, Kaushik and Sharat Prasad, *Low Power CMOS VLSI Circuit Design*, J. Wiley, 2000.
- However, most of the course material will be based on papers and other collected material
  - The reading assignment will be posted on the class web page before class starts
  - Please read them before the lecture for better discussion

## Course Outline and Approach

- We will examine 3 key aspects for deep submicron (well, nowadays the buzz word is nano-meter) designs for performance and power constraints
  - Interconnect – modeling and optimization
  - Placement – which determines interconnect
  - Low power – which is an ultimate design limiter
- Topic-centered, with optimization techniques and modeling issues brought up when needed
  - Every week (or lecture), we will examine one topic
  - Instructor presentation will be complemented by student presentation occasionally
  - Discussion and critics are important in class



## VLSI Optimization Interlock (sample)

| Optimization Techniques | VLSI application |
|---|---|
| Graph algorithms | Partition |
| Graph algorithms, mathematical programming | Placement |
| Plain math. Dynamic programming, Mathematical programming<br>Greedy algorithm | Interconnect Optimization |

The most important thing is to find the right problem formulation



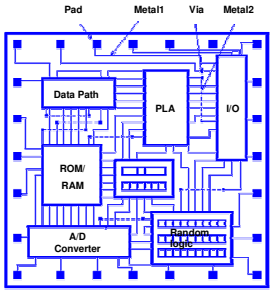
## Grading Policy

- Class participation: 20%
  - Class attendance expected
  - Class interaction welcomed
  - Student presentation on selected papers (peer reviewed by your classmates)
- Homework and midterm: 40%
  - Mainly to make sure you understand the course material
  - By reading, problem solving, and programming
- Project: 40%
  - Most important part!
  - Excellent project => conference paper
  - ICCAD submission (due in April 21) => automatic A
  - Will talk about it a bit later
- Bonus points will be given to active class participation



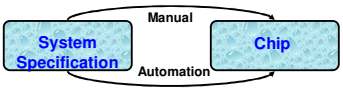
## Basic Components In VLSI Circuits

- Devices
  - Transistors
  - Logic gates and cells
  - Function blocks
- Interconnects
  - Local signals
  - Global signals
  - Clock signals
  - Power/ground nets





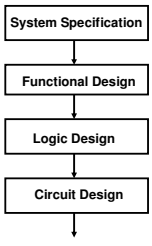

## VLSI Design Cycle

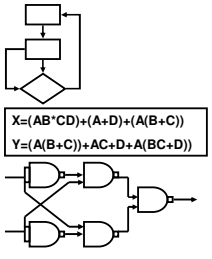



- **Large number of devices**
- **Optimization requirements for high performance**
- **Time-to-market competition**
- **Power (and other) constraints**

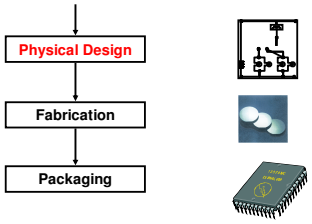


## VLSI Design Cycle



## VLSI Design Cycle (cont.)

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## Physical Design

**Physical design converts a circuit description into a geometric description. This description is used to manufacture a chip. The physical design cycle consists of**

**1 Partitioning**

**2 Floorplanning and Placement**

**3 Routing**

**4 Compaction**

Traditional View

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## History 101 of Physical Design

- Born in early 60's (board layout)
- Passed teenage in 70's (standard cell place and route)
- Entered early adulthood in 80's (over-the-cell routing)
- Declared dead in late 80's !!!
- Found alive and kicking in 90's
- PD has become a dominant force in overall design cycle,
  - thanks to the deep submicron scaling
  - expand vertically with logic synthesis and interconnect optimization, analysis…. => Design closure!

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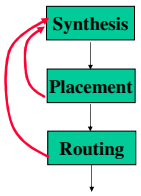
## Grand Challenge: Design Closure

- Conventional flow




**BIG problem: non-converging or too many iterations**

- **HUGE industry efforts**
  - **Cadence**
  - **Synopsys**
  - **Magma**
  - **Monterey**
  - **…...**
  - **Just saw a new startup news in EE Times today on SDI …**
  - **Semiconductor company internal tools: IBM, Intel, Motorola, Sun, …**

**Goal: converging flow**

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## Physical Design

**This course is NOT a hard-core classic physical design class (that covers every major step in PD). I will teach it in Fall 2004**

**Instead, we will be studying emerging topics for nanometer PD related to design closure, low power and so on**

**- Interconnect**

**- Placement**

**- Low power**

**1- 6**

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## Nanometer Challenges

- Interconnect-limited designs
  - Interconnect performance limitation
  - Interconnect modeling complexity
  - Interconnect reliability (noise and signal integrity)
- Placement, to large extend, determines interconnect
  - However, still far away from optimal
- Power barrier and other physical effects (such as noise and variability)
- High degree of on-chip integration
  - Complexity and productivity
  - Limitation of current design abstraction and hierarchy
  - System on a chip

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## Moore's Law

- The minimum transistor feature size decreases by 0.7X every three years (Electronics Magazine, Vol. 38, April 1965)
- Consequences of smaller transistors:
  - Faster transistor switching
  - More transisters per chip
- True in the past 38 years!
- And will be true in at least another 10 years, but now is facing lots of red brick walls
  - Need more CAD tools than ever

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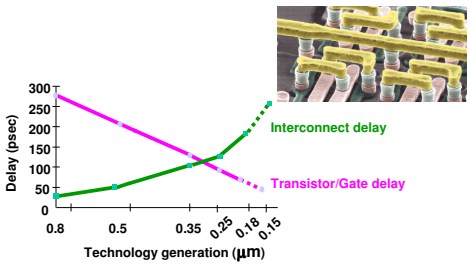
## Interconnects Dominate




Source: Gordon Moore, Chairman Emeritus, Intel Corp.

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## International Technology Roadmap for Semiconductor (ITRS'01): Near-Term Years (High Performance MPU)

| *Technology (nm)* | *130* | *115* | *100* | *90* | *80* | *70* | *65* |
|---|---|---|---|---|---|---|---|
| Year | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 |
| MPU ½ Pitch (nm) | 150 | 130 | 107 | 90 | 80 | 70 | 65 |
| MPU Physical Gate Length (nm) | 65 | 53 | 45 | 37 | 32 | 28 | 25 |
| # Transistors (M) | 276 | 348 | 439 | 553 | 697 | 878 | 1106 |
| Chip Size ($mm^2$) | 310 | 310 | 310 | 310 | 310 | 310 | 310 |
| Chip Frequency (MHz) | 1684 | 2317 | 3088 | 3990 | 5173 | 5631 | 6739 |
| Max # Wiring Levels | 7 | 8 | 8 | 8 | 9 | 9 | 9 |
| Power Supply Voltage (V) | 1.1 | 1.0 | 1.0 | 1.0 | 0.9 | 0.9 | 0.7 |
| Allowable Max Power (W) | 130 | 140 | 150 | 160 | 170 | 180 | 190 |

http://public.itrs.net/

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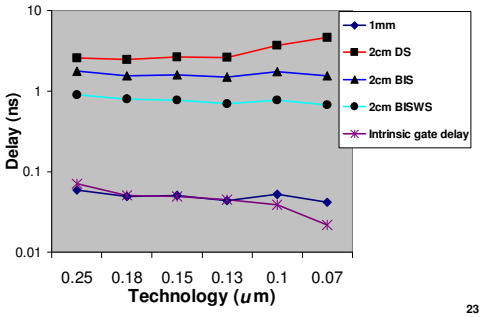
## Impact of Interconnect Optimization on Future Technology Generations

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## International Technology Roadmap for Semiconductor (ITRS'01): Long-Term Years (High Performance MPU)

| *Technology (nm)* | *45* | *32* | *22* |
|---|---|---|---|
| Year | 2010 | 2013 | 2016 |
| MPU ½ Pitch (nm) | 45 | 32 | 32 |
| MPU Physical Gate Length (nm) | 18 | 13 | 9 |
| # Transistors (M) | 2212 | 4424 | 8848 |
| Chip Size ($mm^2$) | 310 | 310 | 310 |
| Chip Frequency (MHz) | 11511 | 19348 | 28751 |
| Max # Wiring Levels | 10 | 10 | 10 |
| Power Supply Voltage (V) | 0.6 | 0.5 | 0.4 |
| Allowable Max Power (W) | 218 | 251 | 288 |

http://public.itrs.net/

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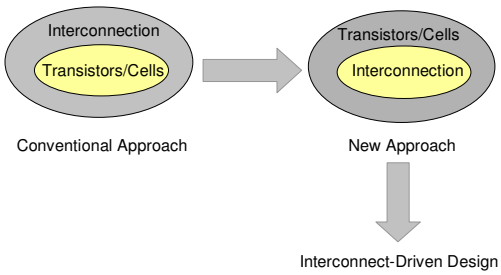
## New Paradigm for VLSI Design

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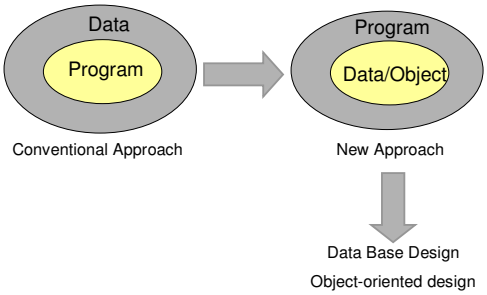
## Paradigm Change in Software Design

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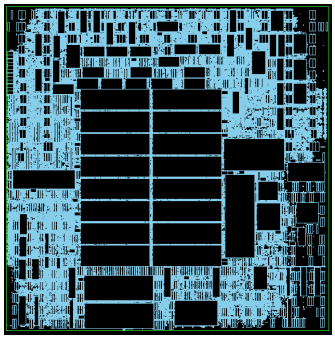
## FloorPlacer (Mix-mode Placement)



- Many macros
- data paths + dust logic
- I/O constraint (area I/O or wirebond)

(source: IBM)

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## Placement Challenge

- Placement, to large extend, determines the overall interconnect
- If it sucks, no matter how well you interconnect optimization engine works, the design will suck
- Placement is a very old problem, but got renewed interest
  - Mixed-size (large macro blocks and small standard cells)
  - Optimality study shows that placement still a bottleneck
  - Not even to mention performance driven, and coupled with buffering, interconnect optimizations, and so on (all you name)

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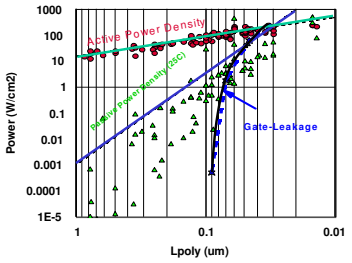
## Power Crisis

- Exponential increase in both gate and sub-threshold leakage presents one of the most challenging issues in sub-90nm technologies.




(courtesy of IBM)

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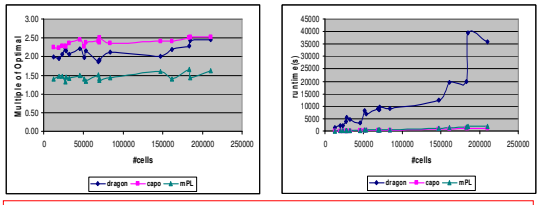
## Comparison with Optimal







- Capo: Based on recursive min-cut (UCLA-UMich)
- Dragon: Recursive min-cut + SA refinement at each level (NWU-UCLA)
- mPL: multi-level placer (UCLA)

There is significant room for improvement in placement algorithms: existing algorithms are 50-150% away from optimal!

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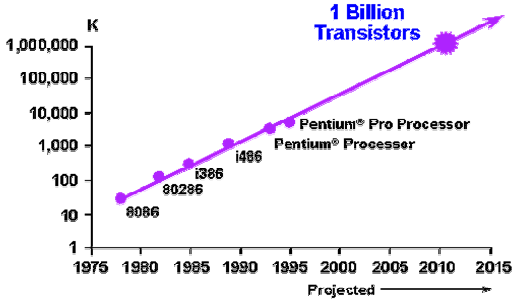
## Transistor Count vs. Year




Source: Intel

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## Interconnect Complexity

| *Technology (um)* | *0.25* | *0.18* | *0.13* | *0.10* | *0.07* |
|---|---|---|---|---|---|
| **Length (m)** | 820 | 1,480 | 2,840 | 5,140 | 10,000 |
| **Wiring Levels** | 6 | 6-7 | 7 | 7-8 | 8-9 |
| **Opt. # buffers per net** | few | → | | | many |
| **Opt. # wiresizes per net** | few | → | | | many |
| **Opt. # buffers per chip** | 5K | 25K | 54K | 230K | 797K |

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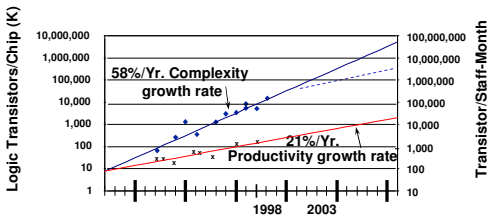
## Productivity Gap




**Chip Capacity and Designer Productivity**

Source: NTRS'97

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## Recap

- Technology scaling according to Moore's Law has been the driving force behind the exponential growth of the semiconductor industry
- Interconnect (esp. global interconnect) performance has become the bottleneck of the overall system performance => interconnect-centric design paradigm
- Placement has a lot of room to improve
- Power crisis needs to be tackled, together with other nanometer physical effects.
- Time to market and design productivity
- **You can make the change!**

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## Class Project

- The purpose is to explore a hot (or cool for low power's sake) research-level topic in depth
- Project and term paper outline
  - Introduction and motivation
  - Problem statement and/or formulation
  - Previous works (exhaustive search)
  - Your approach (new ideas)
  - Experimental results (implement your idea and show it works or state why if it doesn't work)
  - Summary, conclusion and future work
- Class presentation and term paper at the end of semester

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## Class Project

- Rough milestones for class project
  - Proposal by Feb. 16:
    - Project team and initial proposal on what topic to work on
  - First report by March 10:
    - Project proposal with initial literature review
    - And your ideas and plan of attack
  - Second report by April 14
    - Comprehensive literature review and
    - Initial implementation results
    - If you can make ICCAD submission deadline (April 21), and the quality of result sounds good to me: Congratulations, you've got A
  - Final project presentation and term paper
    - TBD, around final weeks

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## Class Project

- Possible topics
  - Interconnect optimization for variability, noise, low power
  - Placement for better variability
  - Mixed size placement (large blocks with lots of dust logics)
  - Simultaneous buffering and placement to handle congestion
  - Detailed placement for voltage island and power island
  - Multiple Vt/Tox/Vdd assignment
  - Pin swapping for gate tunneling leakage reduction
  - Vertical integration of physical design with higher level abstraction (such as architecture)
  - Suggest your own topics
- We will talk more later

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## Resources

- Please check the web site for a set of reference, papers and links (will be updated frequently)
  - *EE Times* (www.eetimes.com) for recent trend/development
- You are encouraged to attend the UT VLSI Seminar
  - http://www.cerc.utexas.edu/vlsi-seminar
- Unofficial, but lots of useful information for citation and paper search
  - http://citeseer.com/
  - Can go directly to http://citeseer.nj.nec.com/cs to search documents
- MIT OpenCourseWare
  - If need to make up some classes (like algorithm)
  - http://ocw.mit.edu/index.html

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## VLSI CAD Conferences

- DAC
  - Design Automation Conference
- ICCAD
  - Int'l Conference on Computer-Aided Design
- ISPD
  - Int'l Symposium on Physical Design
- ASP-DAC
  - Asia and South Pacific DAC
- DATE
  - Design Automation and Test in Europe
- ISCAS
  - Int'l Symposium on Circuits and Systems
- ICCD
  - Int'l Conference on Computer Design
- SLIP
  - Int'l Workshop on System Level Interconnect Prediction

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## VLSI CAD Journals

- IEEE TCAD
  - IEEE Transactions on CAD of Integrated Circuits and Systems
- ACM TODAES
  - ACM Transactions on Design Automation of Electronic Systems
- Integration, the VLSI Journal
- IEEE TCAS
  - IEEE Transactions on Circuits and Systems
- IEEE TVLSI
  - IEEE Transactions on VLSI Systems

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## Assignment #1

- Reading assignment: please get from the web page
- Read ITRS:
  - Get it from http://public.itrs.net/Files/2003ITRS/Home2003.htm
  - *Executive Summary* and *Design* (pay most attention to grand challenges related with design, in particular "Logical, Circuit, and Physical Design", page 19-25 of the chapter of *Design*)
- Write one page (or paragraph) summary
  - To identify one or two problems that you find are most interesting to you, which may potentially become your class project topic
  - State the reason why they are interesting to you and how your background and training can equip you to do a further investigation
  - Turn it in class next Monday

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## Questionnaire

- Help me to know your background better and thus teach the course more effectively.
- Please complete it and hand it in during/after the class.
- Thank you for your cooperation.

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