943/U0020

Physical Design for Nano-Technology (Nanometer ICs)

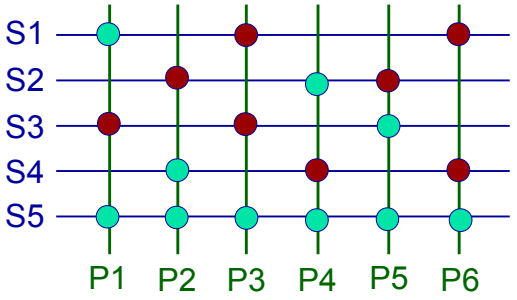
張耀文
Yao-Wen Chang
ywchang@cc.ee.ntu.edu.tw
http://cc.ee.ntu.edu.tw/~ywchang
Graduate Institute of Electronics Engineering
Department of Electrical Engineering
National Taiwan University
Spring 2004

Administrative Matters

- **Time/Location:** Tuesdays 9:10am--12:10pm; EE#2-503.
- **Instructor:** Yao-Wen Chang.
- **E-mail:** ywchang@cc.ee.ntu.edu.tw
- **URL:** http://cc.ee.ntu.edu.tw/~ywchang.
- **Office:** EE#2-548. (Tel) 2363-5251x 548; (Fax) 2364-1972.
- **Office Hours:** Thursdays 2-3pm
- **Teaching Assistants**
  - 陳泰蓁 Tai-Chen Chen (d0943008@ee.ntu.edu.tw)
  - 陳東傑 Tung-Chieh Chen (donnie@eda.ee.ntu.edu.tw)
- **Prerequisites:** data structures (or algorithms) & logic design.
- **Required Text: Any** of the following two books:
  - S. M. Sait and H. Youssef, *VLSI Physical Design Automation: Theory and Practice,* World Scientific Publishing Co., 1999.
  - N. Sherwani, *Algorithms for VLSI Physical Design Automation*, 3rd Ed., Kluwer Academic Publishers, 1999.
- **References:** Selected reading materials from recent publications.

Course Objectives

- Study techniques/algorithms for physical design (converting a circuit description into a geometric description) and their comparisons
- Study nanometer electrical effects and their impacts on the development of physical EDA tools
- **Study problem-solving (-finding) techniques!!!**



Course Contents

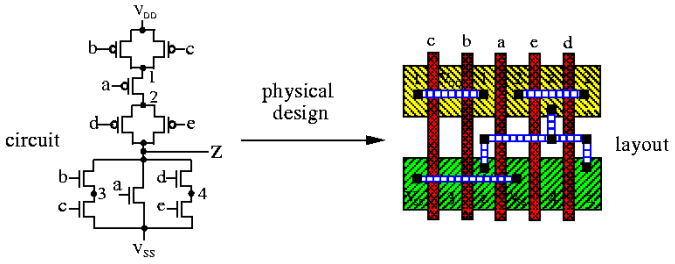
- Introduction to VLSI design flow/styles and technology roadmap
- Traditional physical design processes
  - Partitioning
  - Floorplanning
  - Placement & pin assignment
  - Routing (global, detailed, clock, and power/ground routing)
  - Post-layout optimization
- Signal/power integrity: noise modeling & optimization, IR drop
- Timing issues: timing modeling & optimization, performance-driven design
- Design methodology: large-scale design, interconnect-centric design flow, buffer/wiring planning.
- Design for manufacturability & reliability: process variation, antenna effects, optical proximity correction, metal-fill patterning, electromigration, thermal issues

Grading Policy

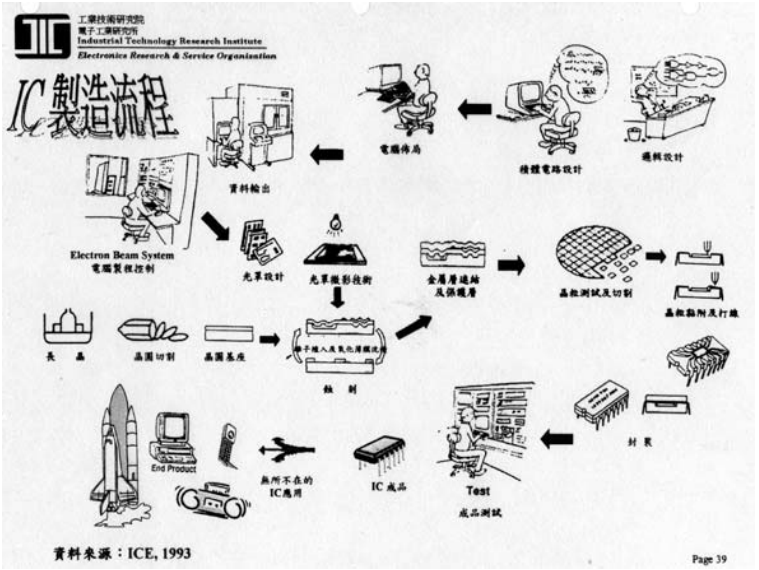
- **Grading Policy:**
  - Homework assignments: 25%
  - One in-class open-book, open-note test: 30% (June 15)
  - Programming assignment #1: 25% (due April 27)
    - Default programming assignment #1: Problem 2, 4, 5, or 6 of the 2004 MOE IC/CAD contest
    - Contest web site: http://www.cs.nthu.edu.tw/~cad
    - Team work (1--4 persons) is permitted (preferably 2 persons)
  - Programming assignment #2: 20% (due June 8)
    - No team work is allowed.
  - Bonus for class participation
- **Homework:** Penalty for late submission: 15% per day.
- **WWW:** http://cc.ee.ntu.edu.tw/~ywchang/Courses/PD04/pd04.html
- **Academic Honesty:** Avoiding *cheating* at all cost.

Unit 1: Introduction

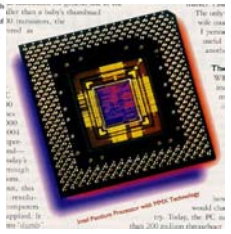
- Course contents:
  - Introduction to VLSI design flow/styles
  - Introduction to physical design automation
  - Semiconductor technology roadmap
- Readings
  - S&Y: Chapter 1
  - Sherwani: Chapter 1



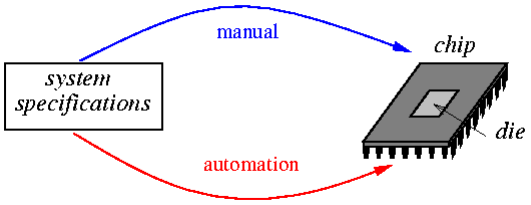
IC Design & Manufacturing Process



From Wafer to Chip



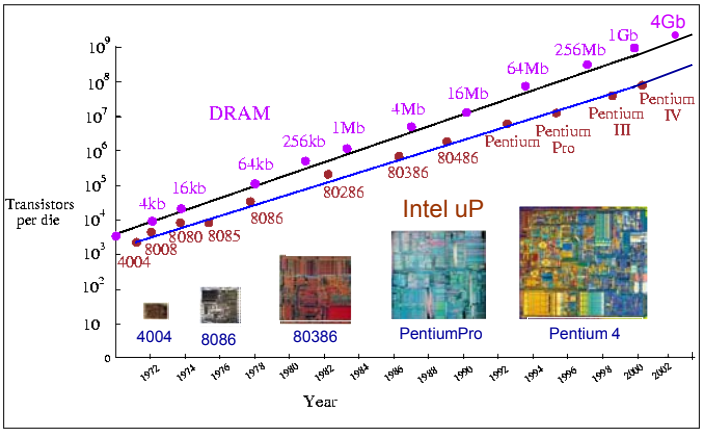
IC Design Considerations



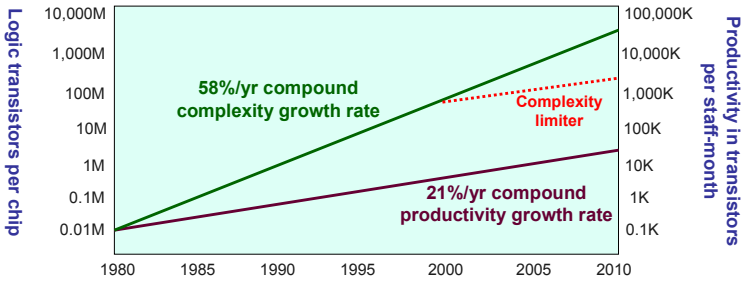
- Several conflicting considerations:
  - **Design Complexity:** large number of devices/transistors
  - **Performance:** optimization requirements for high performance
  - **Time-to-market:** about a 15% gain for early birds
  - **Cost:** die **area**, packaging, testing, etc.
  - Others: power, signal integrity (noise, etc), testability, reliability, manufacturability, etc

"Moore's" Law: Driving Technology Advances

- Logic capacity doubles per IC at a regular interval.
- Moore: Logic capacity doubles per IC every two years (1975).
- D. House: Computer performance doubles every 18 months (1975)



Design Productivity Crisis



- Human factors may limit design more than technology.
- Keys to solve the productivity crisis: CAD (tool & methodology), hierarchical design, abstraction, IP reuse, etc.

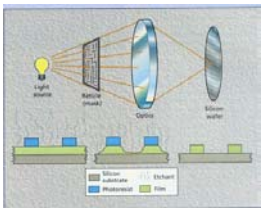
Technology Roadmap for Semiconductors

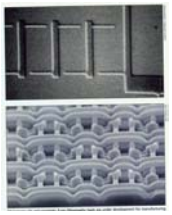
Year	1997	1999	2002	2005	2008	2011	2014
Technology node (nm)	250	180	130	100	70	50	35
On-chip local clock (GHz)	0.75	1.25	2.1	3.5	6.0	10	16.9
Microprocessor chip size (mm^2)	300	340	430	520	620	750	901
Microprocessor transistors/chip	11M	21M	76M	200M	520M	1.40B	3.62B
Microprocessor cost/transistor ($\times 10^{-8}$ USD)	3000	1735	580	255	110	49	22
DRAM bits per chip	256M	1G	4G	16G	64G	256G	1T
Wiring level	6	6–7	7	7–8	8–9	9	10
Supply voltage (V)	1.8–2.5	1.5–1.8	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6	0.37–0.42
Power (W)	70	90	130	160	170	175	183

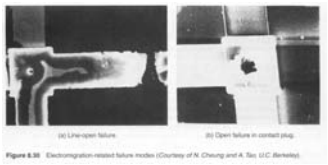
- Source: International Technology Roadmap for Semiconductors (ITRS), Nov. 2002. http://www.itrs.net/ntrs/publntrs.nsf.
- Deep submicron technology: node (**feature size**) < 0.25 μm.
- Nanometer Technology: node < 0.1 μm.

Nanometer Design Challenges

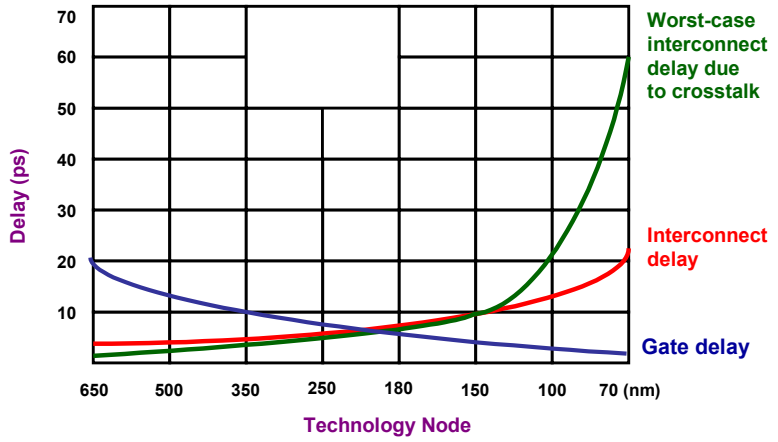
- In 2005, feature size ≈ 0.1 μm, μP frequency ≈ 3.5 GHz, die size ≈ 520 mm^2, μP transistor count per chip ≈ 200M, wiring level ≈ 8 layers, supply voltage ≈ 1 V, power consumption ≈ 160 W.
  - **Feature size ↓ → sub-wavelength lithography (impacts of process variation)? noise? wire coupling? reliability?**
  - **Frequency ↑, dimension ↑ → interconnect delay? electromagnetic field effects? timing closure?**
  - **Chip complexity ↑ → large-scale system design methodology?**
  - **Supply voltage ↓ → signal integrity (noise, IR drop, etc)?**
  - **Wiring level ↑ → manufacturability? 3D layout?**
  - **Power consumption ↑ → power & thermal issues?**



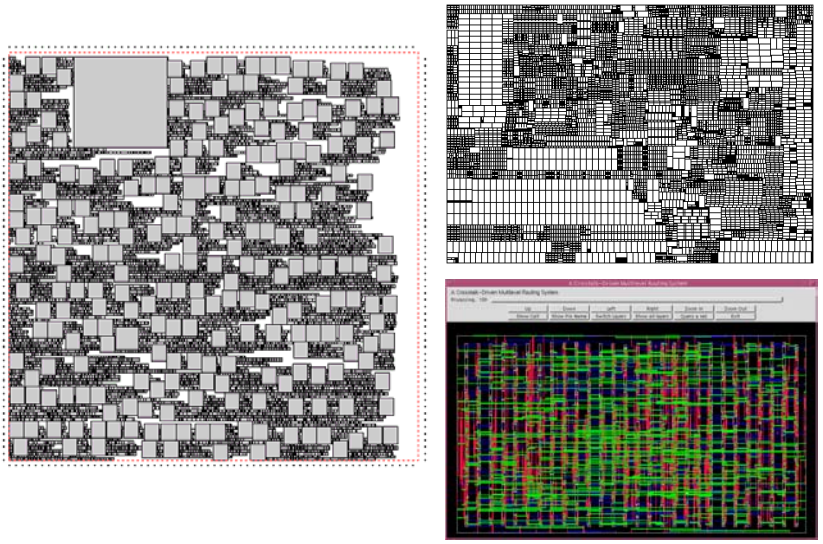




Interconnect Dominates Circuit Performance!!

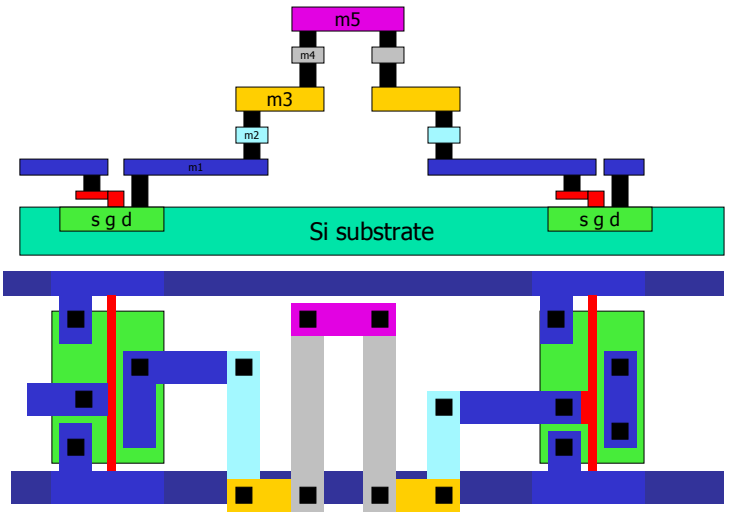


Design Complexity Increases Dramatically!!

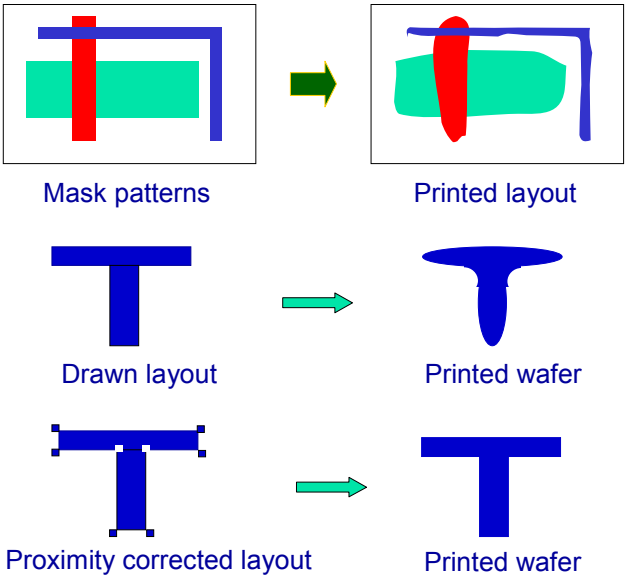


Manufacturability Becomes a 1st-Order Effect!!

- Problems with 10-layer metal?

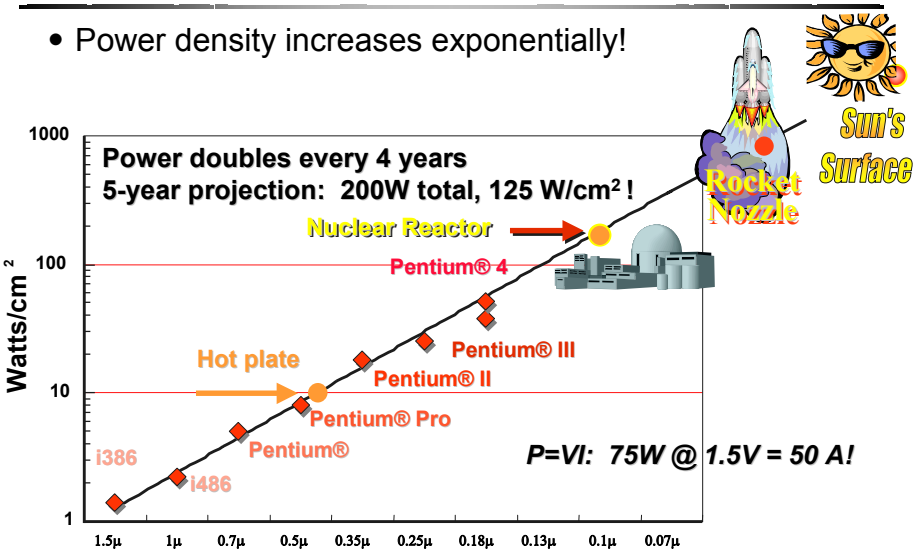


Sub-wavelength Lithography Causes Problems!!



Reliability Is Another Big Problem!!

- Power density increases exponentially!



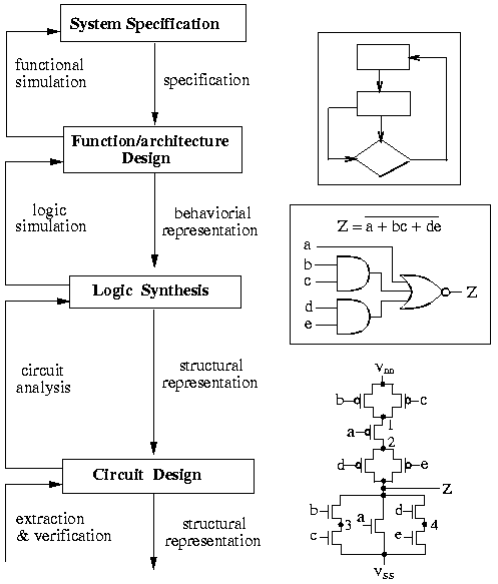
Fred Pollack, "New Microarchitecture Challenges in the Coming Generations of CMOS Process Technologies," 1999 Micro32 Conference keynote. Courtesy Avi Mendelson, Intel.

Traditional VLSI Design Cycles

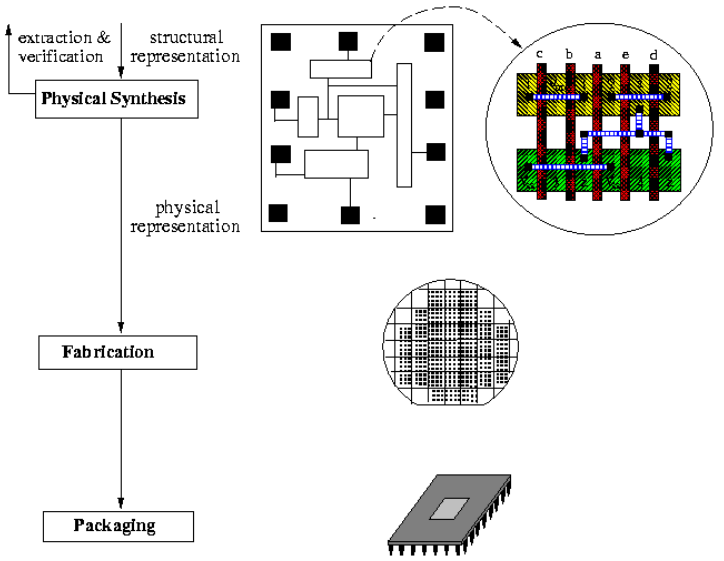
1. System specification
2. Functional design
3. Logic synthesis & formal verification
4. Circuit design
5. **Physical design and verification**
6. Fabrication
7. Packaging

- Other tasks involved: testing, simulation, etc.
- Design metrics: area, speed, power dissipation, noise, design time, testability, etc.
- Design revolution: interconnect (not gate) delay dominates circuit performance in deep submicron era.
  - Interconnects are determined in physical design.
  - Shall consider interconnections in early design stages.

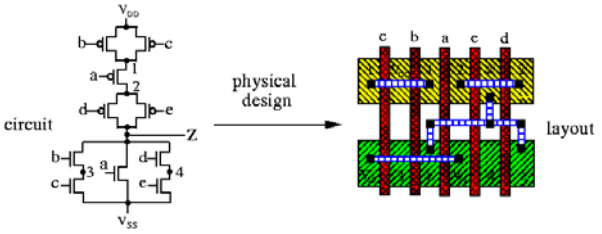
Traditional VLSI Design Cycle



Traditional VLSI Design Flow (Cont'd)

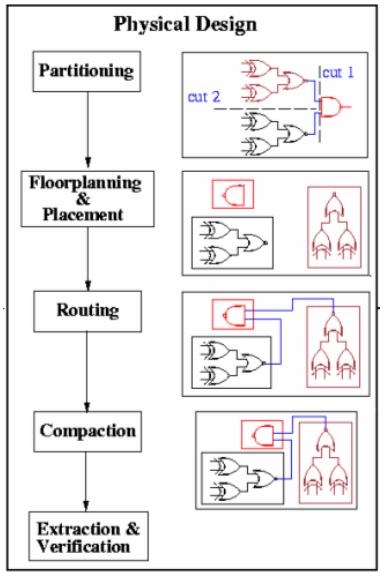


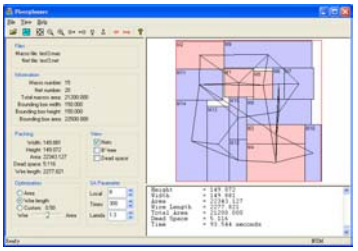
Physical Design



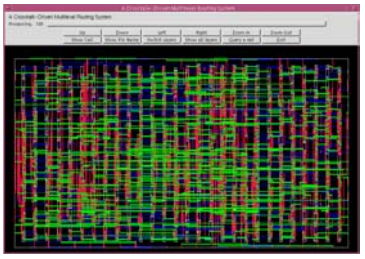
- Physical design converts a circuit description into a geometric description.
- The description is used to manufacture a chip.
- Physical design cycle:
  1. Partitioning
  2. Floorplanning and placement
  3. Routing
  4. Post-layout optimization
- Others: parasitic extraction, timing verification, and design rule checking

Physical Design Flow





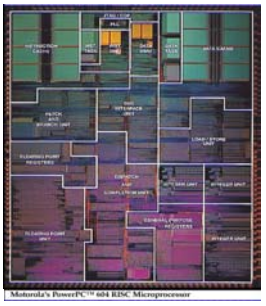
B*-tree based floorplanning system

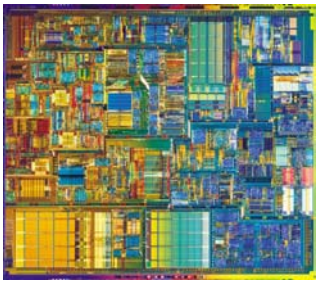


Timing, signal integrity, and antenna-driven routing systems

Floorplan Examples

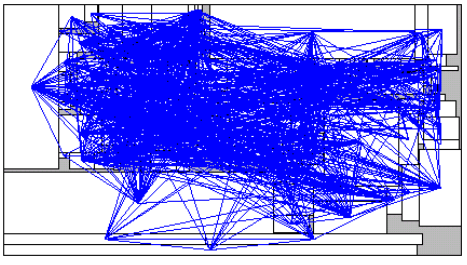
PowerPC 604





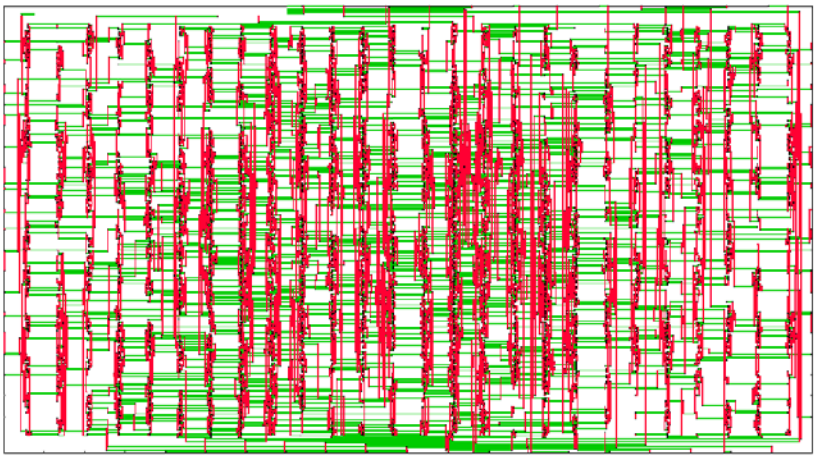
Intel Pentium 4

A floorplan with interconnections

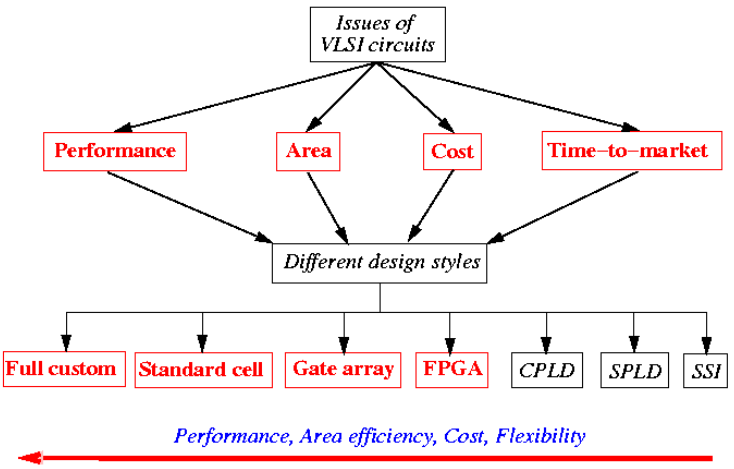


Routing Example

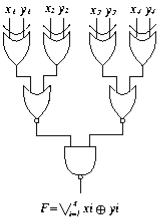
- 0.18um technology, pitch = 1 um, 2774 nets.



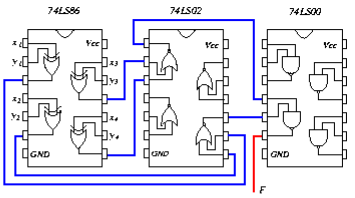
Design Styles



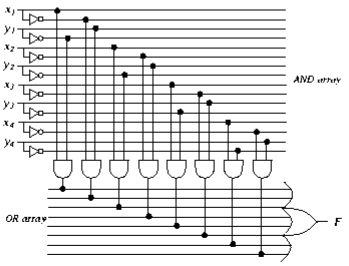
SSI/SPLD Design Style



(a) 4–bit comparator.



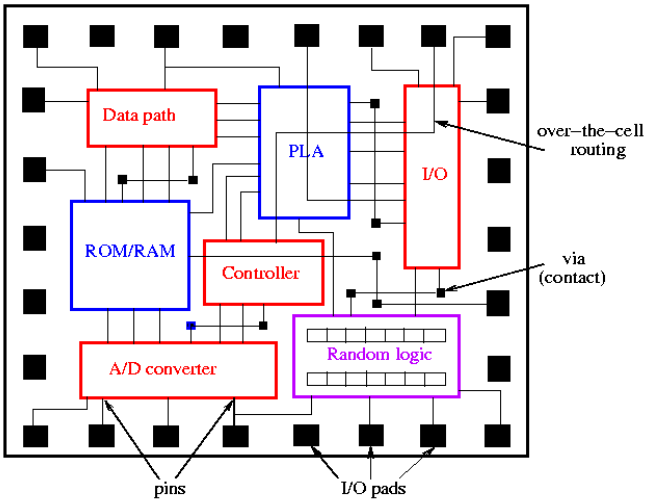
(b) SSI implementation.



(c) SPLD (PLA) implementation.

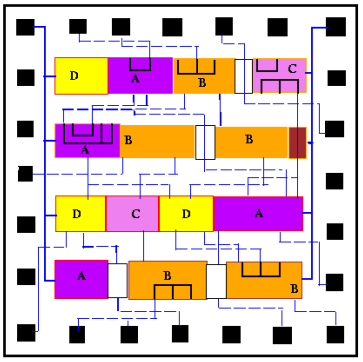
Full Custom Design Style

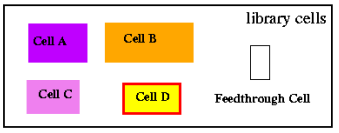
- Design every component from scratch



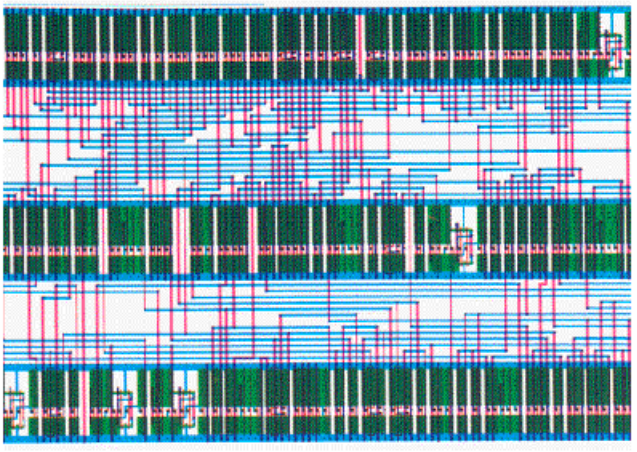
Standard Cell Design Style

- Selects pre-designed cells (of same height) to implement logic





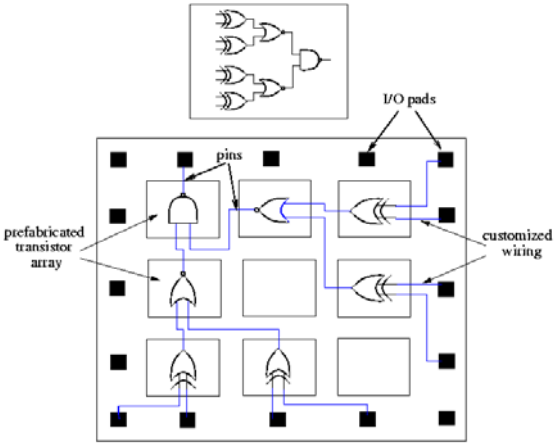
Standard Cell Example



Courtesy Newton/Pister, UC-Berkeley

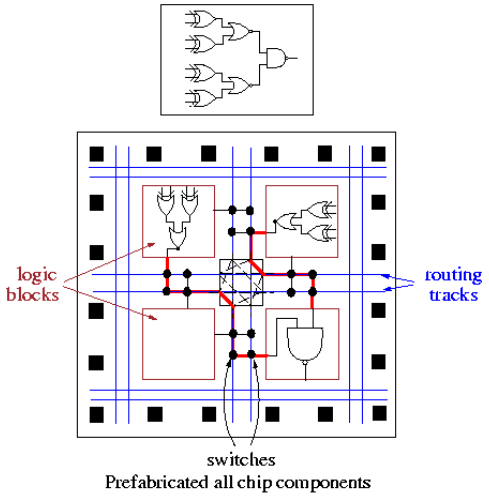
Gate Array Design Style

- Prefabricates a transistor array
- Needs wiring customization to implement logic

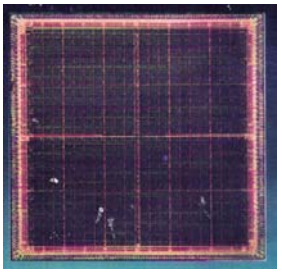


FPGA Design Style

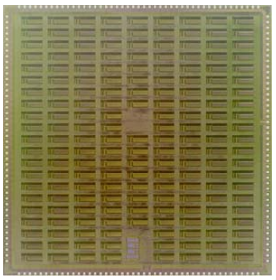
- Logic and interconnects are both prefabricated.
- Illustrated by a symmetric array-based FPGA



Array-Based FPGA Example



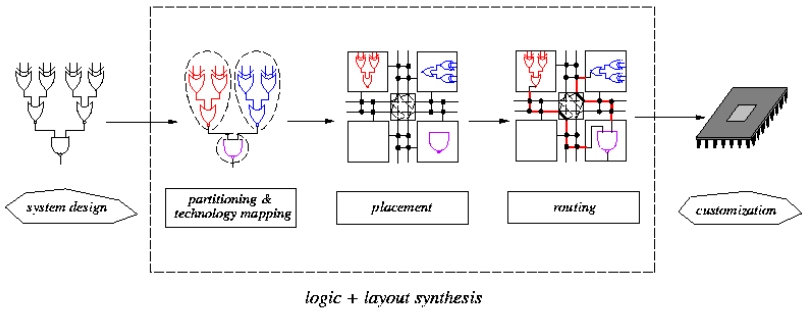
Lucent Technologies 15K ORCA FPGA, 1995
- 0.5 um 3LM CMOS
- 2.45 M Transistors
- 1600 Flip-flops
- 25K bit user RAM
- 320 I/Os



Fujitsu's non-volatile Dynamically Programmable Gate Array (DPGA), 2002

FPGA Design Process

- Illustrated by a symmetric array-based FPGA
- No fabrication is needed



Comparisons of Design Styles

	Full custom	Standard cell	Gate array	FPGA	SPLD
Cell size	variable	fixed height*	fixed	fixed	fixed
Cell type	variable	variable	fixed	programmable	programmable
Cell placement	variable	in row	fixed	fixed	fixed
Interconnections	variable	variable	variable	programmable	programmable

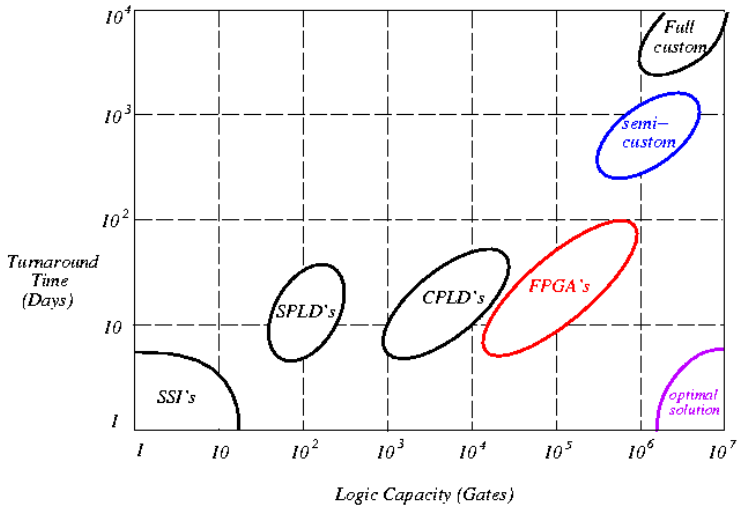
* Uneven height cells are also used.

Comparisons of Design Styles

	Full custom	Standard cell	Gate array	FPGA	SPLD
Fabrication time	− − −	− −	+	+++	++
Packing density	+++	++	+	− −	− − −
Unit cost in large quantity	+++	++	+	− −	−
Unit cost in small quantity	− − −	− −	+	+++	++
Easy design and simulation	− − −	− −	−	++	+
Easy design change	− − −	− −	−	++	++
Accuracy of timing simulation	−	−	−	+	++
Chip speed	+++	++	+	−	−−

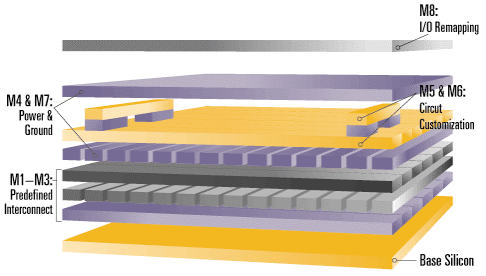
+ desirable; − not desirable

Design Style Trade-offs

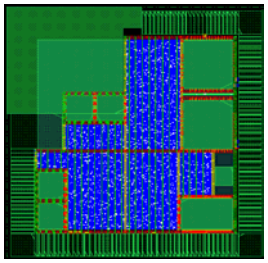


Structured ASIC??

- A structured ASIC consists of predefined metal and via layers, as well as a few of them for customization.
- The predefined layers support power distribution and local communications among the building blocks of the device.
- Advantages: fewer masks (lower cost) ; easier physical extraction and analysis.



A structured ASIC (M5 & M6 can be customized)



- Green blocks: I/C cells and other hard macro blocks
- Blue area: standard cells
- White points: the spare cells