Curve41417: Karatsuba revisited

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Joint work with Daniel J. Bernstein and Tanja Lange

Real-World Application



Performance budget

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 - $n, P \mapsto nP$
 - ARM Cortex-A8

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- Curve41417 (security level above 2²⁰⁰)
 - $\bullet \approx 1.6$ million cycles on FreeScale i.MX515
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Design of Curve41417

- High-security elliptic curve (security level above 2²⁰⁰)
- Defined over prime field \mathbf{F}_p where $p = 2^{414} 17$
- In Edwards curve form

$$x^2 + y^2 = 1 + 3617x^2y^2$$

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- Large prime-order subgroup (cofactor 8)
- IEEE P1363 criteria (large embedding degree, etc.)
- Twist secure, i.e., twist of Curve41417 also secure

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- Prevent software side-channel attack:
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 - no input-dependent branch
 - no input-dependent array index
- Constant-time table-lookup:
 - read entire table
 - select via arithmetic if c is 1, select tbl[i] if c is 0, ignore tbl[i]

$$t = (t \cdot (1-c)) + (tbl[i] \cdot (c))$$

$$t = (t \text{ and } (c-1)) \text{ xor } (\mathsf{tbl}[\mathsf{i}] \text{ and } (-c))$$

ECC Arithmetic

- Mix coordinate systems:
 - doubling: projective X, Y, Z
 - addition: extended X, Y, Z, T

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(See https://hyperelliptic.org/EFD/)
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- Scalar multiplication:
 - signed fixed windows of width w = 5
 - precompute $0P, 1P, 2P, \dots, 16P$ also multiply d = 3617 to T coordinate
 - special first doubling
 - compute T only before addition

ARM Cortex-A8 Vector Unit

- 128-bit vector
- Arithmetic and load/store unit can perform in parallel
- Operate in parallel on vectors of four 32-bit integers or two 64-bit integers
- Each cycle produces:

 four 32-bit integer additions: a₀+b₀, a₁+b₁, a₂+b₂, a₃+b₃

 or

 two 64-bit integer additions: c₀+d₀, c₁+d₁

 or

 one multiply-add instruction: a₀b₀ + c₀
 where a_i, b_i are 32- and c_i, d_i are 64-bit integers

Redundant Representation

- Use non-integer radix $2^{414/16} = 2^{25.875}$
- Decompose integer f modulo $2^{414} 17$ into 16 integer pieces
- Write f as

$$f_0 + 2^{26} f_1 + 2^{52} f_2 + 2^{78} f_3 + 2^{104} f_4 + 2^{130} f_5 + 2^{156} f_6 + 2^{182} f_7 + 2^{207} f_8 + 2^{233} f_9 + 2^{259} f_{10} + 2^{285} f_{11} + 2^{311} f_{12} + 2^{337} f_{13} + 2^{363} f_{14} + 2^{389} f_{15}$$

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• Increase throughput:

$$m_0 \rightarrow m_1 \rightarrow m_2$$

 $m_8 \rightarrow m_9 \rightarrow m_{10}$

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- Decrease latency:
 - $m_0 \rightarrow m_1$
 - $m_8 \rightarrow m_9$

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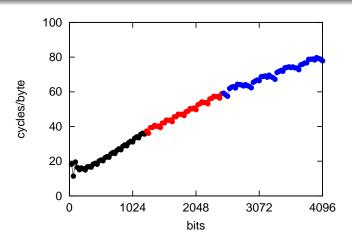
• Karatsuba splits 1 $(2n \times 2n)$ into 3 $(n \times n)$

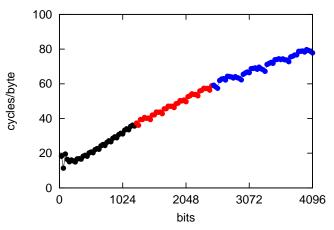
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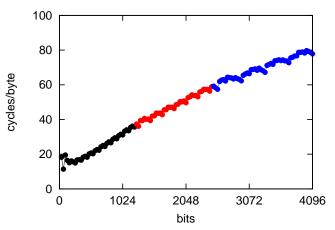
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- What is the zero-level/one-level cutoff for number of limbs?

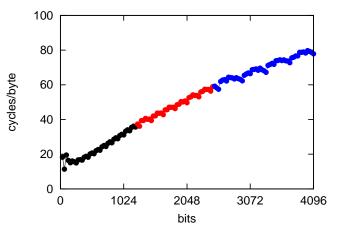




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- We reduce cutoff via redundant representation

Polynomial Multiplication

- Goal: Compute P = ABgiven $A = a_0 + a_1t^n$ and $B = b_0 + b_1t^n$
- Method 1: schoolbook $P = a_0b_0 + (a_0b_1 + a_1b_0)t^n + a_1b_1t^{2n}$
- Method 2: Karatsuba (8n-4 additions) $P = a_0b_0 + ((a_0+a_1)(b_0+b_1) - a_0b_0 - a_1b_1)t^n + a_1b_1t^{2n}$
- Method 3: refined Karatsuba (7n-3 additions) $P = (a_0b_0 - a_1b_1t^n)(1-t^n) + (a_0+a_1)(b_0+b_1)t^n$

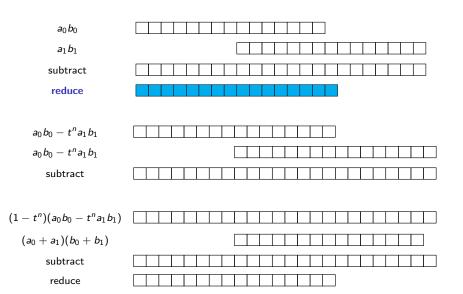
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- Method 4: reduced refined Karatsuba (6n-2 additions) (new) $P = (a_0b_0 a_1b_1t^n \mod Q)(1-t^n) + (a_0+a_1)(b_0+b_1)t^n \mod Q$

Reduced Refined Karatsuba



Cost Comparison (Karatsuba)

Level	Mult.	Add		Cost
		64-bit	32-bit	3333
0-level	256	15	0	256+8+0=264
1-level	192	59	16	192+30+4=226
2-level	144	119	40	144+60+10=214
3-level	108	191	76	108 + 96 + 19 = 223

Note: use multiply-add instructions

- 1 cycle per multiplication
- 0.5 cycle per 64-bit addition
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OpenSSL

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secp160r1	pprox 2.1 million	pprox~2.1 million
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nistp224	pprox 4.0 million	pprox 3.9 million
nistp256	pprox 4.0 million	pprox 3.9 million
nistp384	pprox 13.3 million	pprox 13.2 million
nistp521	pprox 29.7 million	pprox 29.7 million
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- Coming soon: Intel Haswell implementation with Sebastian Verschoor